Fabrication of Stress Controlled Silicon Oxide for Free-Standing MEMS Devices

by

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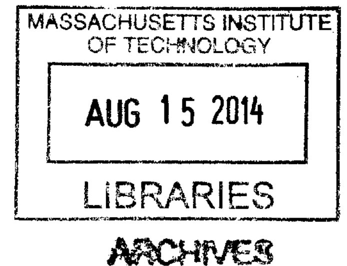
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Abstract

In development of the critical –angle transmission (CAT) grating, structural failure of the thin self-standing grating membrane posts a challenge for manufacturing yield. The major risk comes from the strongly compressive stressed buried oxide layer that creates loading to the thin silicon grating membranes. In an effort to find a solution, a process of fabricating silicon-on-insulator (SOI) wafers with tensile stressed buried oxide is studied in this work.

Thin silicon dioxide films have been studied as a function of deposition parameters and annealing temperatures. Films were deposited by tetraethoxysilane (TEOS) dual-frequency plasma enhanced chemical vapor deposition (PECVD) with different time interval fractions of high frequency and low frequency plasma deposition. The samples were subsequently annealed up to 930 °C to investigate their stress behavior. Films that were deposited in high-frequency dominated plasma were found to have tensile residual stress after annealing at temperatures higher than 800 °C. The residual stress can be controlled to slightly tensile by changing the annealing temperature. Large-area free-standing tensile stressed oxide membranes without risk of buckling were successfully fabricated.

A bonding process of the low tensile stressed oxide films into SOI wafers was developed. SOI wafers were successfully fabricated and examined by SEM inspection. The bonding surface energy was

estimated from a double cantilever beam theory (razor blade method). The bonding strength satisfied the processing requirements of CAT grating fabrication.

Other potential solutions to solve the problem of thin silicon grating membrane buckling are also presented. For obtaining tensile stress oxide films, a spin-on-glass approach was studied and showed promising results; an ion implantation approach is discussed with literature data.

A different strategy for solving the buckled membrane challenge is processing with thick grating membranes for better structural robustness, then reducing membrane thickness by oxidation and vapor hydrofluoric etch. Proof-of-concept experiments were designed and carried out, which demonstrated capability to fabricate thick grating bars, to oxidize the silicon membrane into silicon dioxide with nanometer scale thickness control, and to etch the oxide with vapor hydrofluoric etch.

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I would like to thank my advisor Dr. Mark Schattenburg, who let me join the Space Nanotechnology Lab and patiently coached me to excel in the field of nano/micro fabrication technology. I thank Dr. Ralf Heilmann for his contribution and knowledge in CAT grating and various efforts in the lab. I am also grateful for the help Dr. Alex Bruccoleri provided throughout the project, who trained me on most of the tools I needed, and made good suggestions when I was stuck in the project. I need to thank my lab mate Brandon Chalifoux for the inspiring discussions about optics, future plans, and stress measurement methods.

The great facility at MIT made this work happen. I want to thank MTL and all the staff who helped me in this work, especially Bob Bicchieri who kept the Oxford-100 PECVD tool alive; Bernard Alamariu, who gave many insights about annealing; Kurt Broderick showed me how to use Filmetrics; Eric Lim helped me with AFM, and RTP; Dennis Ward provided many tips in etching and wet processing; lastly James Daley, who answered many questions and let me work in NSL. I also want to thank the MIT Kavli Institute for logistics support, especially Jean Papagianopoulos who got my purchasing orders through promptly. I am thankful to NASA for supporting this work, and the SNL CAT grating work, under grants NNX08AI62G and NNX11AF30G.

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Chapter 1

Introduction

1.1 Silicon Oxide in Fabrication of Free-Standing Structures

Silicon oxide (SiO_2) is one of the most commonly used materials in MEMS (Micro-Electrical-Mechanical-System) devices. It serves as a good electrical insulator for integrated circuits, and also a commonly used mask or stop layer for fabrication process. For many of the MEMS devices, especially for optical applications, a thin silicon oxide membrane is commonly used as support layer for the final device or as an intermediate step in the fabrication process, for example in micro-mirrors[1], micro-pump for drug delivery [2], Critical Angle Transmission Gratings [3], and etc.

In fabricating free-standing structures, one scheme is to use silicon on insulator wafers, which have a buried oxide layer between silicon layers. First, pattern both front side and back side of the SOI wafer, then pattern transfer from both sides, till the two sides meet on the buried oxide layer. At the end, depending on the application, either remove the oxide by hydrofluoric acid etching, or leave with a very thin layer of silicon oxide, as shown in Figure 1-1.

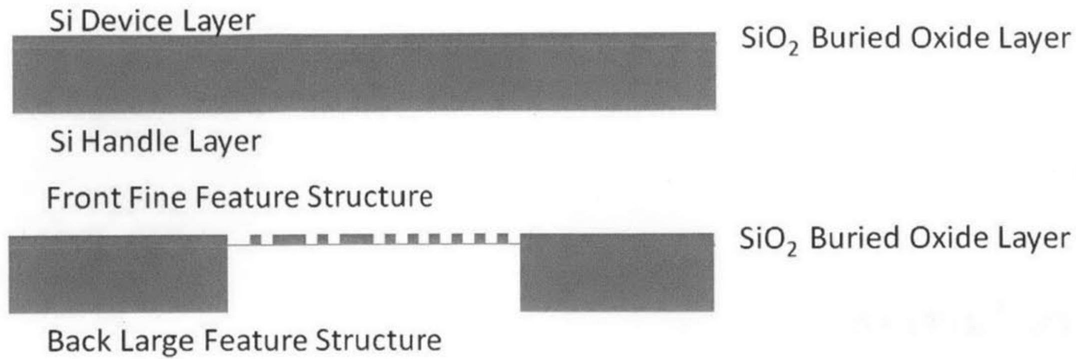


Figure 1-1: Free Standing Structure Fabrication Process Diagram

1.2 Critical Angle Transmission Grating and Fabrication Process

In the adventure of space studies, diffraction gratings are a key component for space instrumentation in analyzing x-rays from celestial objects. At the Space Nanotechnology Lab at MIT, we have developed a novel high efficiency CAT (Critical Angle Transmission) grating that combines the advantages of both conventional transmission and reflection gratings, such as high efficiency, low mass, relaxed alignment tolerances, and etc. [7, 8].

The working principal for the CAT grating is illustrated in Figure 1-2, where α is the incident angle, β_m is the angle for different diffraction orders relative to grating normal, p is the period of the grating, d is the depth, a is the opening length, and b is the grating bar thickness. The incident x-rays come into the narrow channels at an incident angle of α, then reflecting off the grating sidewalls. When the optical path length difference between parallel x-rays is an integer multiple m of the x-ray wavelength λ, diffraction orders occur governed by the grating equation

$$m\lambda = p\,(\sin\alpha - \sin\beta_m) \tag{1.1}$$

The CAT grating is designed to have narrow and deep channels, so that α and β_m are similar in value, which will lead to the "blazing effect" that improves the optical efficiency over traditional transmission gratings. As x-ray spectrographs often require high efficiency over a broad wavelength band, typically 2 – 7 nm, the blazed gratings can mostly avoid efficiency loss from absorption since most photons remain in vacuum. Moreover, blazed gratings can concentrate the diffracted intensity into the desired diffraction orders instead of being wasted in the 0th, $\pm 1^{st}$ orders as in the conventional grating. To meet the challenging requirement of above 50% efficiency, the dimensions of CAT gratings are carefully designed, as shown in Figure 1-3 [3]. As for the geometric dimensions, the grating bars have a period of 200 nm, depth of 4 μm, and bar width of 40 nm. The grating bars have to be free-standing to avoid absorbing the incident x-rays. To ensure structural robustness, the grating also has a level 1 support grating structure that has a period of 5 μm and a large hexagon structural support with a length of 1 mm.

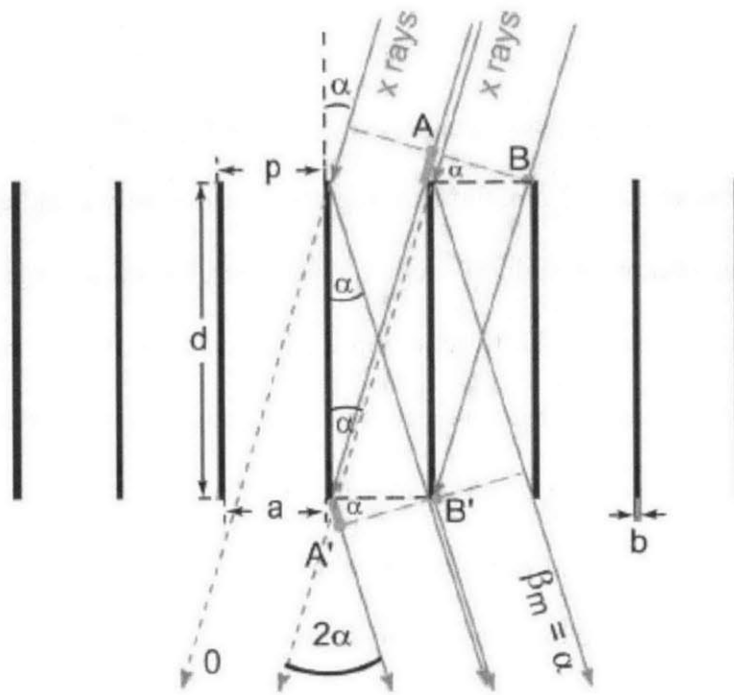


Figure 1- 2: Schematic cross section through a CAT grating. The *m*th diffraction order occurs at angle β_m where the optical path difference between AA′ and BB′ is mλ. [8]

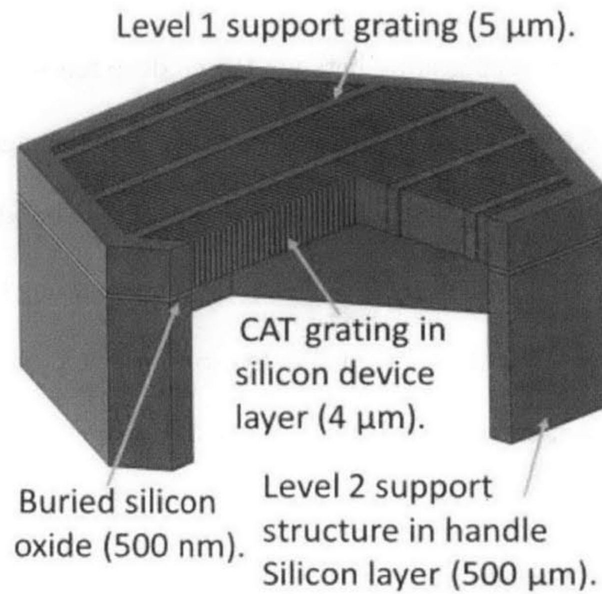


Figure1-3: Free Standing CAT Grating 3D Drawing [3]

Silicon is chosen to be the material for CAT grating because of the geometric requirements and its material properties. The design described in Figure 1-3 is very challenging to fabricate because of the scale. The grating bars have a desired thickness of 40 nm while the desired depth is 4 μm, which has an aspect ratio of 100. This required high aspect ratio for structures in the tens of nanometer range posts the largest challenge in fabricating CAT gratings.

A complex process has been developed in Space Nanotechnology Lab as shown in Figure 1-4, which involves two lithographic and pattern transfer processes, integrated together on a silicon-on-insulator (SOI) wafer. The CAT gratings start from special-ordered SOI wafers with 400 nm thermal oxide on top, 4 μm device silicon layer, 500 nm buried oxide layer, 500 μm handle silicon layer, and 4 μm PECVD oxide layer. In the next step, the front side and back side oxide is

patterned via interference lithography and reactive ion etching. In step F3, the silicon device layer is etched to yield 4 μm deep grating bars via Bosch deep reactive ion etch (DRIE) process, which stops on the buried oxide layer. To protect gratings from damage in later steps, photoresist is spun on the front side in step F4. Then the wafer is flipped and bonded to a carrier wafer via Crystal Bond to etch the back side via DRIE in step B1, and stopping on the buried oxide again. Finally, the remaining buried oxide is stripped in hydrofluoric acid (step B2), and the final device is obtained after cleaning (step B3).

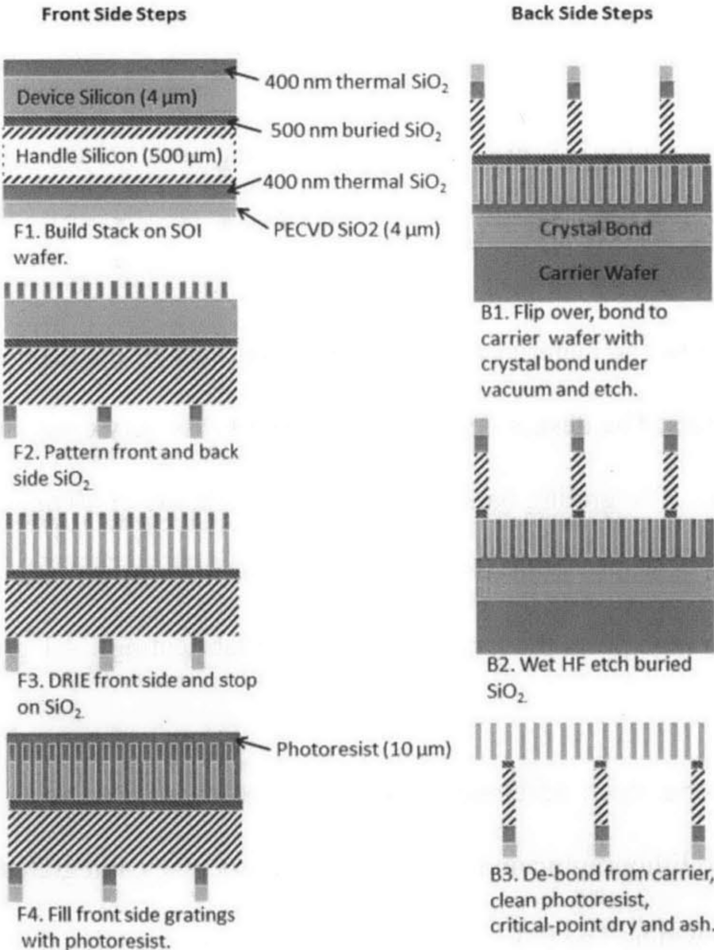


Figure 1- 4: Fabrication Process of CAT Grating [3]

1.3 Motivation for Stress Controlled Buried Layer Oxide

Commercial available SOI wafers can have a customized buried oxide layer thickness, usually ranging from 2000 Å to 10000 Å. Ideally, the thicker the buried oxide layer the better, because of improved fabrication process window, especially for the backside through wafer etch. However, the commonly used oxide is strongly compressive stressed, roughly 300 MPa compressive for thermal oxide and PECVD silane oxide. With such high compressive stress, the thicker the buried oxide layer is, the larger wafer bow it will cause for the entire wafer. More importantly, because of the compressive stress, the oxide layer suffers from buckling, and induces design constraints.

Specifically for fabricating the CAT gratings, in Figure 1-4 steps B1 and B2, after the ~500 μm ofbulk silicon is removed, the strong stress from the buried oxide layer can cause large structural distortions to the fine pitched grating bars, large deflections, or plate buckling, see Figure 1-5. This becomes a challenge for fabricating free-standing MEMS devices [9-11].

An alternative is to use silicon nitride as the buried layer, which can have a wide range of stress depending on deposition conditions, ranging from -200 MPa to 500 MPa [4], and have it polished and bonded with a silicon device layer [5]. The constraint of using a silicon nitride layer rather than silicon oxide is that silicon nitride has a ~10 times worse dry etching resistance than silicon oxide. Typical etch rate of silicon oxide during deep silicon etch by STS SF_6 ranges from 10-70 nm/min, while silicon nitride ranges from 150-200 nm/min [6]. For many applications that use dry etching for the coarse backside pattern transfer, that requires etching 550 um silicon

and stopping on the buried layer, a ~10x thicker nitride layer is needed to provide the same level of process window. Without the aid of an end-point detection system, the buried layer can be easily etched through, destroying the front side structures.

In this thesis, we present a new approach in preparing stress-controlled silicon oxide films and making them into bonded SOI wafers. The objective is to make a thick low-tensile-stress oxide film, with thickness ~2 um, and stress around ~100 MPa tensile, which will yield a stable and flat membrane once released from both sides. We believe such a technology will relax the design constraints in MEMS devices and enable innovative designs to be achieved.

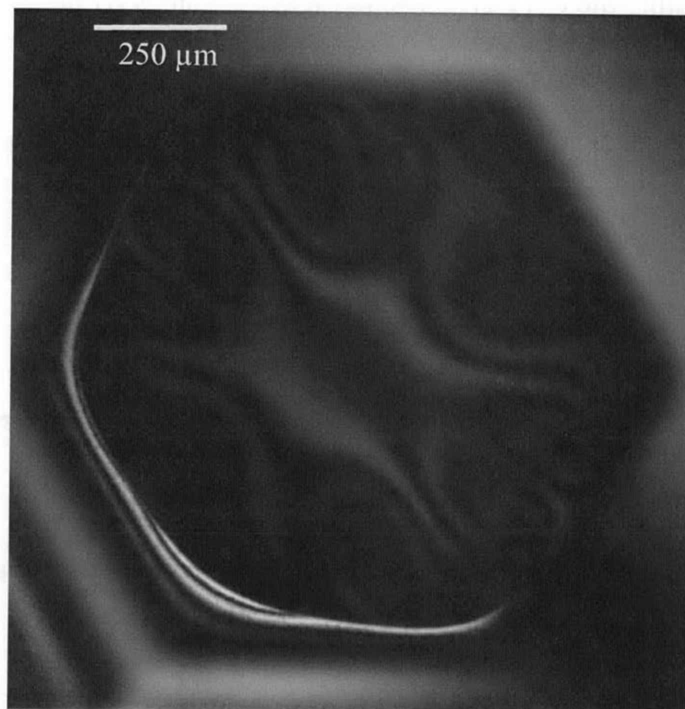


Figure 1-5: Optical microscope image of a buckled oxide membrane released from DRIE etching

1.4 CAT Grating Plate Buckling

The goal of tensile stressed buried oxide wafers is to reduce the stress level in the fabrication process and improve yield. With current fabrication process, we frequently observe broken or buckled grating lines with no sign of stiction or defects (see Figure 1-6).In case of stiction, all the grating lines will collapse together. The thin silicon grating bars often broke at roughly 1/4 of its length towards the L1 support structure, which corresponding to the positions with the largest radius of curvature, identified as the zero bending moment locations shown in Figure 1-7.

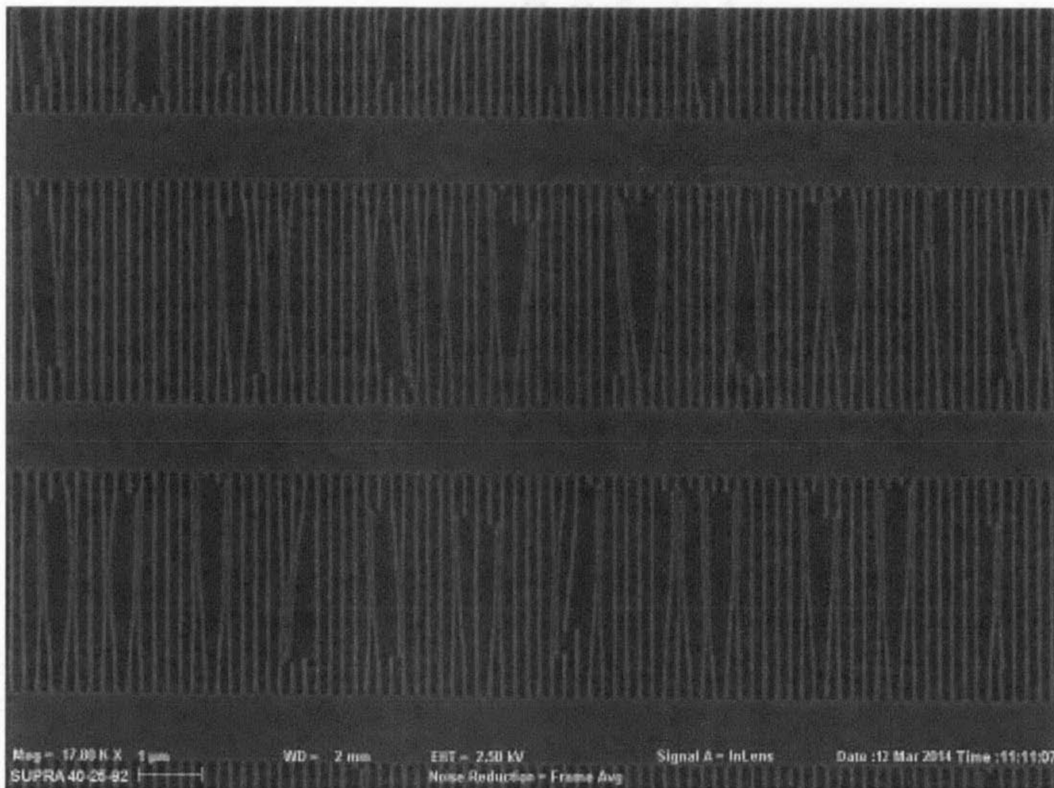


Figure 1-6: Top down view of fabricated CAT grating with broken lines. No sign of stiction. Broken lines likely to be buckled by compressive stress [12].

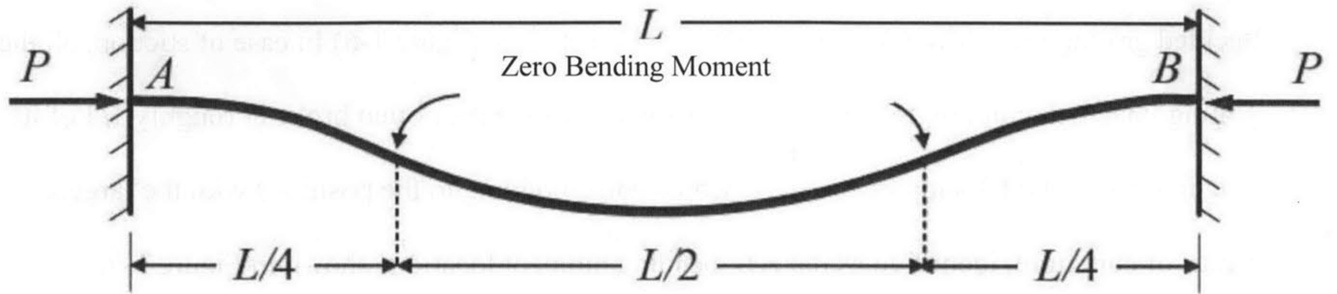


Figure 1 - 7: Schematic of top down view of first mode buckled plate with two cantilever ends.

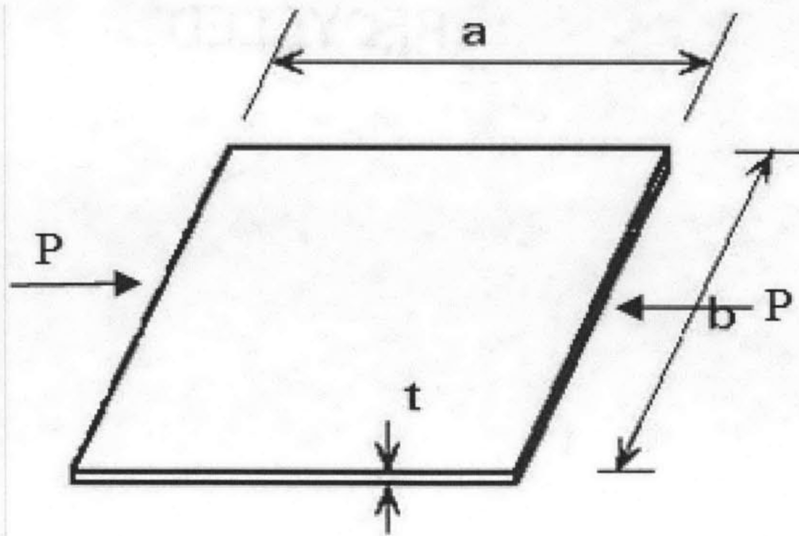


Figure 1- 8: Schematic of plate buckling.

The governing equation for axial compressive force P to a plate deflection is

$$\frac{P}{b} = \frac{\pi^2 D}{b^2} \left(\frac{mb}{a} + \frac{a}{mb}\right)^2 , \qquad (1.1)$$

where D is the bending rigidity defined by material properties in Equation 1.4, a is the length of the unloaded plate edge, b is the length of the loaded plate edge, integer m represents the number of waves in the shape of the plate, t is the plate thickness, and v is the Poisson's ratio. Denote the critical buckling coefficient in Equation 1.2,

$$k_c = \left(\frac{mb}{a} + \frac{a}{mb}\right)^2. \tag{1.2}$$

Therefore, we obtain Equation 1.3, where the critical buckling load is just a function of bending rigidity, buckling coefficient, and the loading edge length. Specific value of k_c can be found from Figure 1- 9.

$$\sigma_{cr} = \frac{P_{cr}}{bt} = k_c \frac{\pi^2 D}{b^2 t}, \tag{1.3}$$

$$D = \frac{Et^3}{12(1-\nu^2)}, \tag{1.4}$$

where E is the Young's modulus of the material. Combining Equations 1.3 and 1.4, we obtain,

$$\sigma_{cr} = k_c \frac{\pi^2 E}{12(1-\nu^2)} \left(\frac{t}{b}\right)^2. \tag{1.5}$$

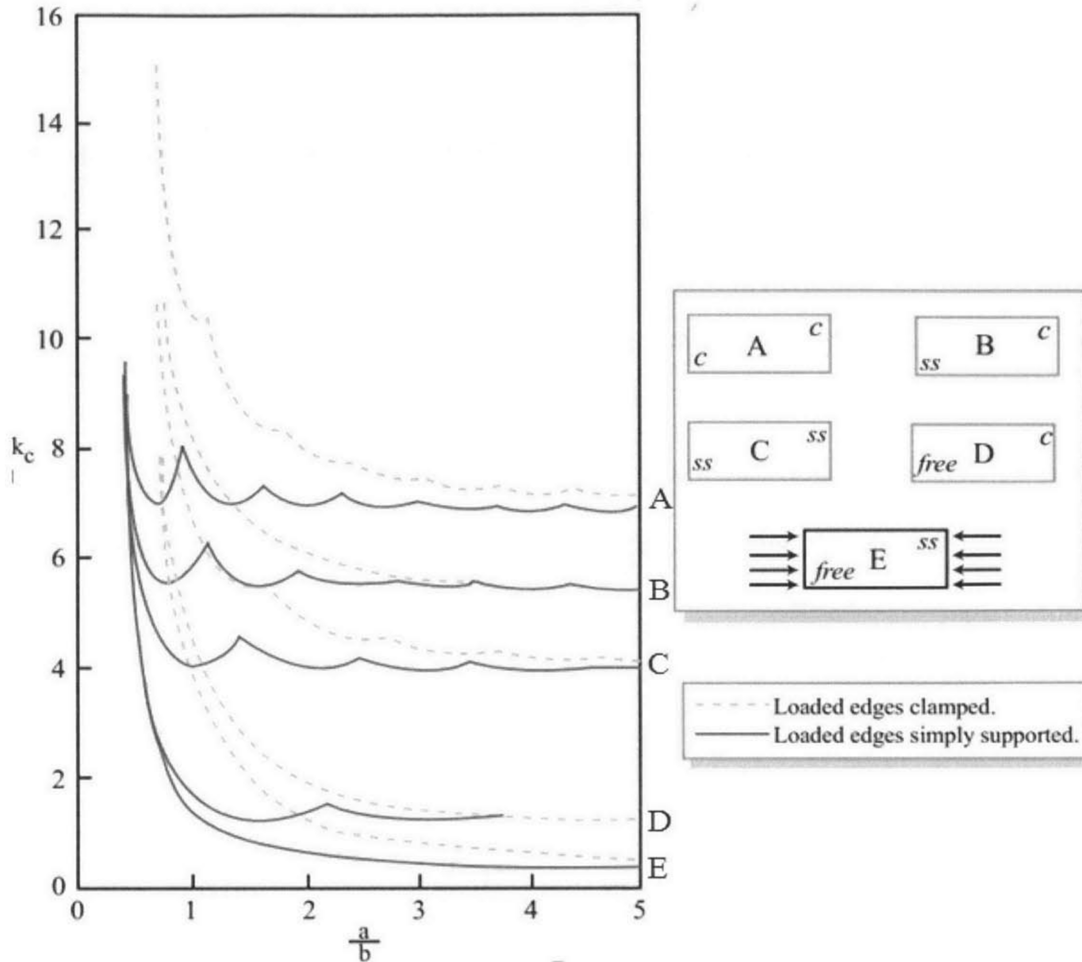


Figure 1- 9: Buckling coefficients of plates subjected to in-plane compressive loading with various boundary conditions [13]. C stands for clamped, ss stands for simply supported.

As for the CAT grating, grating bar thickness t is between 40 nm to 100 nm, grating bar height b is ~ 4 μm, and grating bar width a is also ~ 4 μm, therefore the aspect ratio is ~ 1. The top and bottom edges of the grating bar are free, while the other two edges are clamp supported by L1 structure, which corresponding to the solid curve A in Figure 1- 9. From Equation 1.5, the critical buckling stress can be calculated as a function of grating bar thickness, see Figure 1- 10. The buckling stress is inversely proportional to the grating bar thickness squared. When the thickness is 40 nm, the theoretical buckling stress is 81 MPa, which is more than double the

estimate in Dr. Minseung Ahn's thesis because of different geometry [14]. The dashed line indicates the intrinsic stress of silicon oxide, which is ~ 300 MPa compressive. With the current fabrication process, grating bars could undergo compressive stress induced by the buried oxide layer. Due to the complexity of fabrication process, the actual stress on the grating bars is not fully understood.

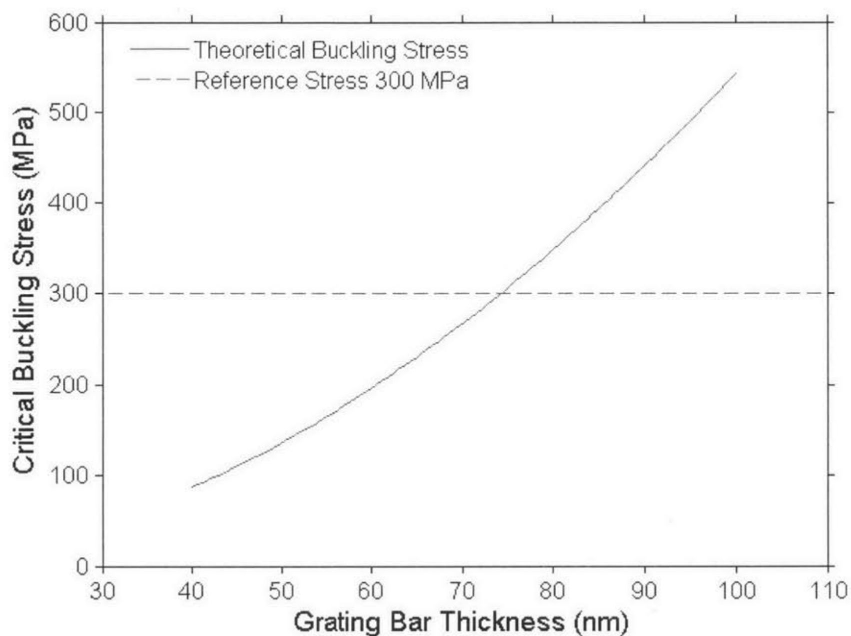


Figure 1- 10: Critical grating bar buckling stress vs. grating bar thickness.

Apart from fabricating SOI wafers with low tensile stress buried oxide, another strategy is to obtain thick grating bars (t > 100 nm), so that the buckling stress is way above the possible compressive stress the grating bars can reach. After all the other processes are completed, we can thin the grating bar by thermal oxidation and vapor hydrofluoric acid etch, see Chapter 5 for details.

Chapter 2

PECVD TEOS Deposition and Annealing

2.1 Overview

To obtain stable, tensile-stressed, and high temperature compatible silicon dioxide layers, one potential solution is PECVD oxide films from TEOS (tetraethoxysilane, $Si(OC_2H_5)_4$). PECVD has been extensively used for its ability of high deposition rate at low temperatures. The most common precursors for PECVD oxide are TEOS and silane. Thin oxide films prepared by TEOS PECVD at low temperature show superior step coverage. In addition, TEOS is chemically stable and easy to handle as it is in liquid form, unlike flammable and toxic silane. In this chapter, a film stress control process that combines PECVD deposition and annealing will be presented [15].

2.2 TEOS Film Stress Measurement

Film thickness was measured using a Filmetrics F-20 interferometric system by analyzing the spectral reflectance. The stress was then calculated from the Stoney Equation (2.1) under the assumption that the film thickness is much smaller than the substrate thickness. The substrate had a thickness of 525 μm, about ~1000 times larger than the film thicknesses in this study. The wafer radii of curvature were measured by a KLA-Tencor™ FLX-2320 system by directing a

laser at a surface with a known spatial angle. The reflected beam strikes a position sensitive photodiode and therefore the geometry of the film can be recorded by scanning the laser along the wafer surface.

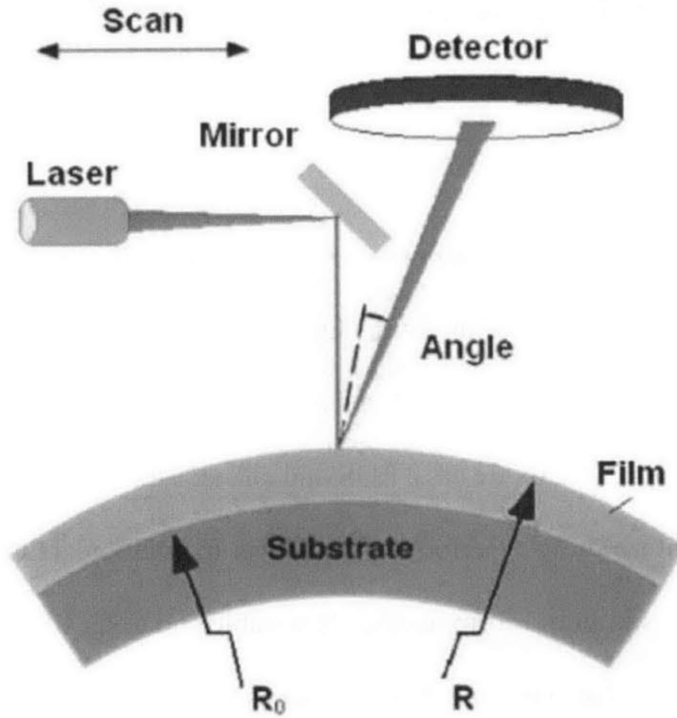


Figure 2-1: Schematic of measuring residual stress from interferometric system [16]

The stress equation is

$$\sigma_f = \frac{E_s h_s^2}{6h_f(1-v_s)} \times \left(\frac{1}{R_f} - \frac{1}{R_0}\right) \tag{2.1}$$

where E_s is the Young's modulus of substrate, v_s is the Poisson's ratio of substrate, h_s is the substrate thickness, h_f is the film thickness, R_0 is the initial substrate radius of curvature measured before deposition, and R_f is the radius of curvature when the film stress is measured. Literature values for silicon properties were used in this study with 130 GPa for E_s and 0.28 for

v_s [17]. A negative sign of stress indicates compressive stress, while a positive sign represents tensile stress. The errors from multiple measurements are negligible, typically less than 5 MPa, mainly caused by setting the wafer at slightly different positions.

2.3 Dual-Frequency Plasma Enhanced Chemical Vapor Deposition

Van de Ven et al. [18] demonstrated stress control of silicon oxide using dual-frequency PECVD with TEOS. Dual-frequency PECVD utilizes two RF power supplies, one at a frequency of 13.56 MHz and one at a frequency of 50 - 400 KHz [18]. The high frequency plasma deposits porous tensile stress films, while the low frequency plasma deposits dense compressive films [18]. Therefore, one can control the average oxide film stress by changing the fraction of the high frequency plasma and low frequency plasma. However, because the deposition happens at 350 °C, the film stress is unstable before high temperature annealing. Moreover, the film can absorb water vapor and the stress can change dramatically [19]. At high frequency (13.56 MHz), only the electrons are able to follow the RF field while the ions are limited in space by their heavier mass and inertia to move, given the fast alternating electric field. Depending upon the mass of the ions, the critical frequency at which the ions start to follow the electric field is between 1~5 MHz. As a result, when the plasma frequency is below 1 MHz, the ions are being driven by the electric field, and create ion bombardments that improve the film quality. The ion bombardment effects enhance chemical reactions, and also induce a low energy ion implantation which densifies the film.

A series of tests were conducted using the Oxford Instruments Plasmalab 100 tool located in ICL at MTL. TEOS is in liquid form at room temperature, it has a boiling point of 168 °C and a

freezing point of – 82 °C. In the Plasmalab 100 tool, TEOS is supplied by flowing Ar gas through the heated liquid TEOS cylinder. The TEOS will be mixed with oxygen, and with the aid of plasma, decomposes into oxide, water and other gas phase byproducts. The tool has two plasma sources at different frequencies, one is HF (High Frequency) at 13.56MHz, and the other one is LF (Low Frequency) at 50 KHz.

The TEOS oxide films in this study were deposited on 100 mm-diameter 525 μm-thick <100> silicon wafers with the conditions shown in Table 2.1. All the depositions had three steps before deposition: pump down the chamber, pre-heat at 350 °C for 3 min, and surface clean with 720 sccm nitrous oxide (N_2O) in 20 W HF plasma for 2 min. The deposition step used alternating high frequency and low frequency plasma deposition on the order of several seconds. The deposition rate of 100% LF plasma approximately ranges in 20 - 27 nm/min, depending on the deposition chamber conditions. The deposition rate for 100% HF plasma ranges from 22 – 34 nm /min. The film has thickness non-uniformity around ~5%, which means the edge of the wafer has 5% thicker oxide than in the center.

Table 2.1: Deposition Parameters on the Plasmalab 100 tool

Parameter	Value
Deposition pressure	500 mTorr
Temperature	350 °C
TEOS bubbler with Ar flow rate	50 sccm
TEOS Chamber Temperature	60 °C
O_2 flow rate	300 sccm
Low frequency (LF 50 KHz) plasma power	50 W
High frequency (HF 13.56 MHz) plasma power	40 W

Film stress was found to change approximately linearly with the fraction of HF plasma time, as shown in Figure 2-2. All the measurements were conducted in room temperature and immediately after the deposition. If pure LF plasma is used, the film becomes a highly compressive and dense layer of oxide. With the increased fraction of HF plasma during the deposition step, the stress also becomes more tensile until it reaches around 321 MPa. From experimental observations, stress of samples deposited from high HF fractions were unstable when storing in cleanroom ambient. The stress will decrease over time, and with higher fraction of HF plasma, the stress decreases faster. Detailed discussions are provided in Section 2.5.

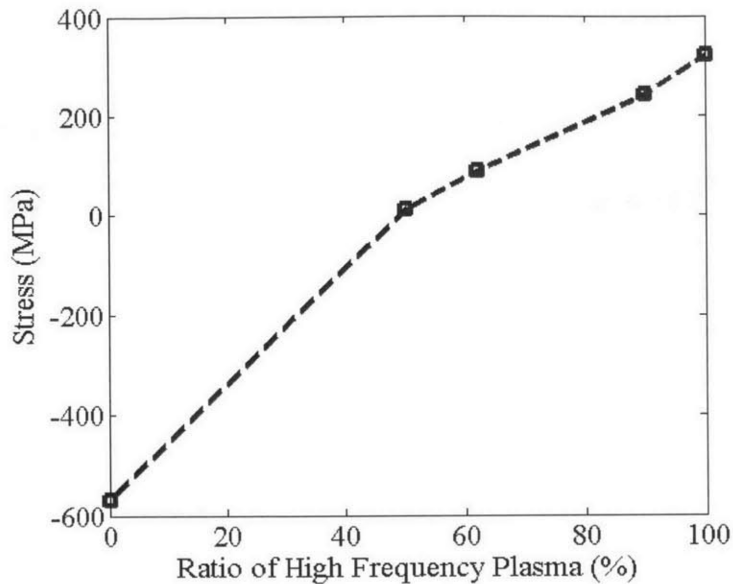


Figure 2-2: Deposited film stress vs. high frequency plasma duty cycle. Stress increases as the fraction of HF plasma time increases. Measurements were conducted ~15 min after the deposition.

2.4 Furnace Annealing

2.4.1 Stress vs. Annealing Temperature

To ensure the film is compatible with a wafer bonding process, which requires high temperature annealing ideally above 900 °C, the oxide film has to maintain tensile stress at high temperatures. Deposited films were annealed at various temperatures ranging from 350 °C to 930 °C in a nitrogen filled quartz furnace for 30 min to study the stress changes after annealing, shown in Figure 2-3. The quartz furnace has a heating rate of about 5 °C/min, and samples annealed above 600 °C were unloaded after cooling to 600 °C. Films were also annealed in an oxygen filled furnace where the annealing temperature ranged from 600 °C to 905 °C with 30 min annealing

time. The gas flow rate of nitrogen annealing is 8 SLPM (80% in TRL furnace B1), and flow rate of oxygen annealing is 4 SLPM (80% in TRL furnace B1). Stresses were measured immediately after the samples were cooled to room temperature. The wafers with the deposited films were stored in a class 100 cleanroom environment.

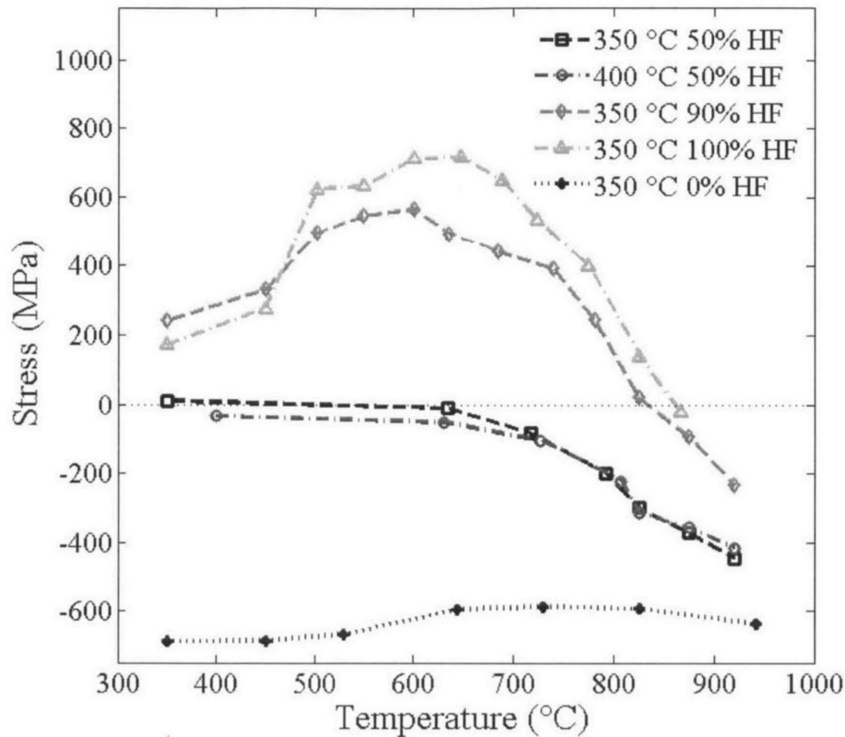


Figure 2-3: Film stress vs. annealing temperature in nitrogen ambient. Stress increases initially and decreases dramatically after 650 °C for the HF films. The initially neutral stressed films stay stable until 650 °C and become highly compressive at higher temperature.

As shown in Figure 2-3, five samples deposited under different conditions were annealed up to 930 °C in nitrogen ambient. The measured thickness of those films ranged from 360 – 496 nm. The stress of the 100% LF sample was stable over all the annealing temperatures with small

variations. The 50% HF samples, with no discernible initial stress, dramatically became compressive after annealing at temperatures higher than 650 °C. The stress of the 100% HF sample at first became more tensile with the temperature until reaching a maximum of 717 MPa at 648 °C. Beyond 648 °C, the stress became more compressive rapidly with the increase of temperature, and reached close to neutral stress around 860 °C. A similar trend applied to the 90% HF sample, which had slightly lower stress at all temperatures compared to the 100% HF sample. PECVD deposition utilizes plasma energy to overcome chemical inertness at low temperature and typically leaves radicals, gases, and intermediate species in the deposited films. The initial increase in tensile stress can be explained as a result of a degassing process and collapsing of vacant holes in microstructures. The residual hydrogen gas H_2 concentration in PECVD TEOS oxide films was found to decrease from the initial 4% to less than 1% after annealing [20]. The dramatic change for stress to become more compressive at high temperatures can be explained by stress relaxation [21]. The 100% LF film did not have a stress change towards compressive at high temperatures since the film itself was already densified by ion bombardment created in the low frequency plasma.

For the goal of bonding using a slightly tensile stressed oxide film into SOI (Silicon on insulator) wafers, the higher the post-bonding annealing temperature the better is the bonding strength. Therefore, from the results in Figure 2-3, annealing the 100% HF film gives the highest temperature that can be reached before becoming compressively stressed, which is around 860 °C. The temperature in MTL's quartz furnace was measured by the central thermostat, depending on where the wafer carrier was located, the temperature measurement can have ± 5 °C variation.

Other parameters can also increase the initial stress, and further increase the highest annealing temperature at which the film stays tensile stressed, which includes increasing plasma frequency, decreasing oxygen flow, and decreasing deposition temperature. Plasma frequency is determined by the equipment hardware, and is impossible to change. From experimental observations, decreasing oxygen flow does make the stress become even higher tensile, but the film uniformity becomes worse. As for decreasing temperature, when depositing film from PECVD, the higher the temperature, the better the film quality because of the higher kinetic energy that increases chemical reaction. Decreasing the deposition temperature also decreases the film thickness uniformity [22]. Because of the complex tradeoffs between higher annealing temperature and film properties, not enough experiments were conducted with decreased temperature.

2.4.2 Nitrogen vs. Oxygen Annealing

An additional annealing experiment was conducted to study the difference of oxygen and nitrogen annealing. The error bars in Figure 2-4 represent the stress variances in three samples. As shown in Figure 2-4, the films annealed in oxygen had lower tensile stress below 700 °C and underwent a less steep stress drop at higher temperatures. One possible explanation is that the deposited SiOx becomes further oxidized by annealing in oxygen and the oxidized silicon expands in volume, generating compressive stress, so that at temperatures below 700 °C, the tensile stress of films annealed in oxygen was lower than that of the films annealed in nitrogen. From experimental data shown in Figure 2-3, the lower fraction of HF plasma the film has during deposition, the slope of stress change toward compressive is less steep when annealing at higher temperatures.

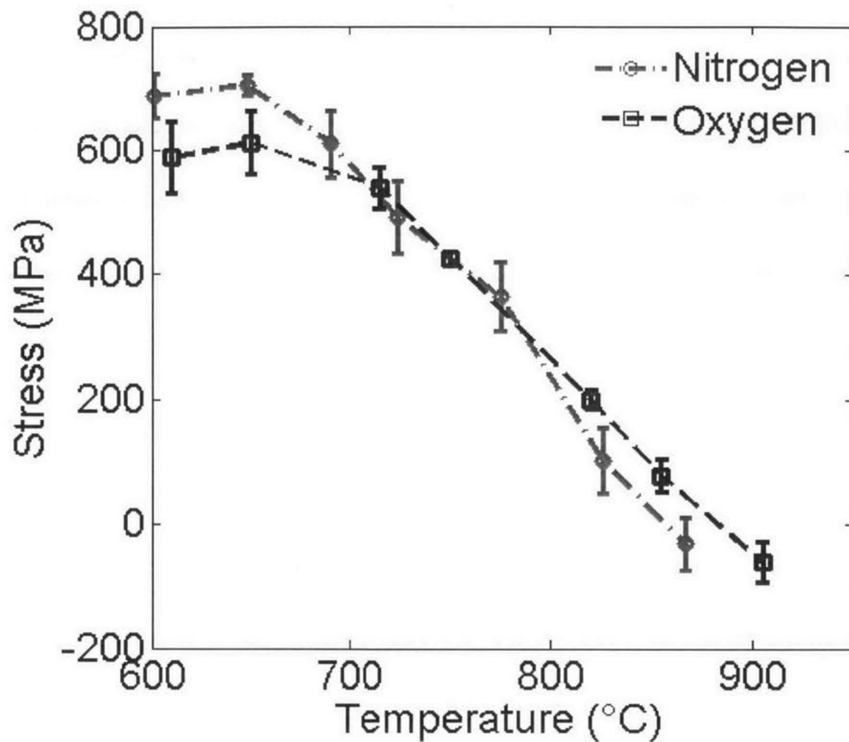


Figure 2-4: Stress comparison of oxygen vs. nitrogen ambient annealing. Annealing 100% HF films in oxygen ambient yields lower maximum stress and less steep stress drop above 800 °C compared to annealing in nitrogen ambient.

The HF plasma deposits porous films, while the LF plasma deposits dense films [18]. Similarly, the oxygen annealing process generates denser films because of the additional oxidation effect. Therefore, at annealing temperatures higher than 800 °C, the films annealed in oxygen have less stress change toward compressive compared to films annealed in nitrogen as temperature increases, as shown in Figure 2-4. For practical applications, the annealing in oxygen gives approximately an additional 30 °C in the highest annealing temperature at which the films still stay tensile.

2.4.3 Stress vs. Annealing Time

The annealing time of the previous reported annealing experiments were all around half hour. During wafer bonding, the silicon oxide will be fusion bonded with silicon, enhanced by high temperature and the high applied bonding pressure. The bonding strength depends on a few factors, including the surface roughness of the two contact surfaces, the pre-bonding surface treatment, the bonding pressure, the bonding temperature, the bonding time, the post-bonding annealing temperature, the annealing time, etc. A review by Maszara et al. [23] stated that the bonding strength was dominantly determined by the bonding and post-bonding annealing temperature, rather than the time. Maszara reported that wafers bonded at 800 °C, and with a 10 seconds annealing process at 800 °C can withstand standard mechanical thinning, chemical etching processes, and common device fabrication processes [23]. From the SOI bonding literature, the typical annealing time is between 2 hours to 4 hours [24 - 26].

However, our collaborator, Ultrasil Corporation, a professional SOI wafer manufacturer recommended a long annealing time (6 – 9 hours), claiming to strengthen the wafer bonding quality. The residual stress of the 100% HF PECVD silicon oxide films has to maintain tensile after the long annealing time. Another set of annealing experiments was conducted. Two 100% HF PECVD samples were deposited with thickness of 623 nm and 671 nm, then annealed in a 795 °C oxygen filled furnace up to 25 hours, with stress measurements at room temperature every one hour in the first 9 hours. The stress vs. annealing time curve in Figure 2-5, is an exponential decaying function for the first 9 – 10 hours, and follows the model of glass stress relaxation [27, 28]

$$s(t) \propto \exp[-\left(\frac{t}{\tau}\right)^{\alpha}], \qquad (2.2)$$

where s is the residual stress at time t, τ is the relaxation time, α is a constant with a value of 1/3 when $t \ll \tau$, a value of 1 when $t \gg \tau$, and a value of 0.5 when $t \approx \tau$. The relaxation time is also called Maxwell relaxation time, that can be determined from equation 2.3,

$$\tau = \frac{\eta}{G} \qquad (2.3)$$

where η is the shear viscosity and G is the shear modulus of glass. The relaxation time of SiO_2 is typically on the order of 1×10^5 seconds at 800 °C [29], which corresponds well to the timeframe of the 25 hours (9×10^5 seconds) long annealing experiment shown in Figure 2-5.

During the experiment, another key observation was that when the sample was accidentally left in the furnace at 695 °C for 12 hours, the stress surprisingly kept the same as before the annealing. That implies that stress change only happened at temperatures above 695 °C, which suggests the glass transition temperature of this TEOS 100% HF films is above 695 °C but lower than 795 °C.

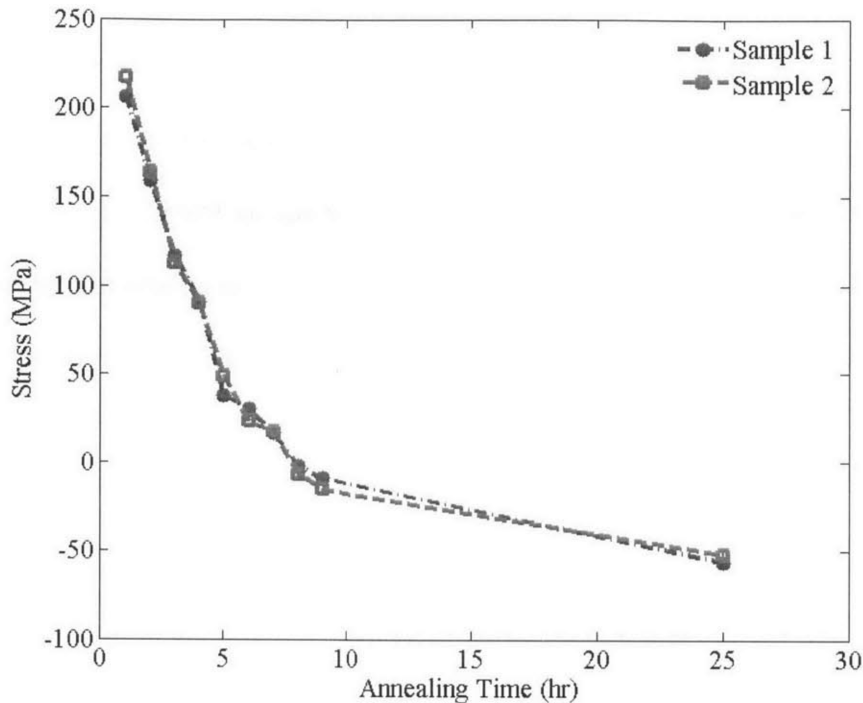


Figure 2-5: Stress vs. annealing time of two 100% HF sample annealed in oxygen filled furnace at 795 °C. The cross-over temperature for these two samples to become compressive is 7 hours of furnace annealing.

2.5 **Rapid Thermal Annealing**

In section 2.4, a furnace annealing process has been used to obtain low stress silicon oxide films. The process is repeatable, reliable, and is capable of annealing a large number of wafers at one time. On the other hand, furnace annealing takes a long time in heating up the temperature and also cooling down, which leads to long waiting time during process development. The half-hour annealing experiments described in section 2.4 actually took two hours to collect one data point, because the furnace has to be cooled to unload the sample.

Rapid thermal annealing (RTA) is a much shorter annealing process that typically lasts only a few minutes. It uses a high power lamp or laser to quickly heat up the wafer surface up to 1200 °C in just a few seconds. Because of the high heating speed, annealing effects from stress relaxation at high temperature, degassing, and thermal expansion from CTE mismatch, will be greatly depressed, which in return, we hope to further increase the critical annealing temperature at which we can keep the film tensile stressed. At the meantime, RTA can reduce the annealing time from ~ 2 hours down to a few minutes.

One TEOS 100% HF sample was subsequently annealed for 1 minute in the ICL RTA in 35 sccm nitrogen flow at 500 °C, 700 °C, 800 °C, and 900 °C respectively, shown in Figure 2-6. The stress curve decreases with the increase in annealing temperature and doesn't show a desirable higher critical temperature at which the film can stay compressive. Experiments with longer annealing time (2 minutes) and oxygen ambient were conducted, and similar results were obtained.

The residual stress mechanism is complicated, and in this case I suspect the short annealing time is not enough to degas the impurities in the film, including water and hydrogen molecules. Hydrogen concentration of PECVD-TEOS oxide films can be as high as 5%, and after furnace annealing at 700 °C for 1 hr, the concentration drops to 0.67%, measured by Rutherford backscattering spectroscopy (RBS) [20]. Therefore, one minute of annealing is most likely to be insufficient in driving out the dissolved gases from PECVD deposition. However, further analysis and experiments need to be conducted to be conclusive.

Please note the actual stress right after deposition at 350 °C was around 300 MPa tensile, but the first data point is compressive because of water vapor absorption, which will be discussed in detail in Section 3.4.1.

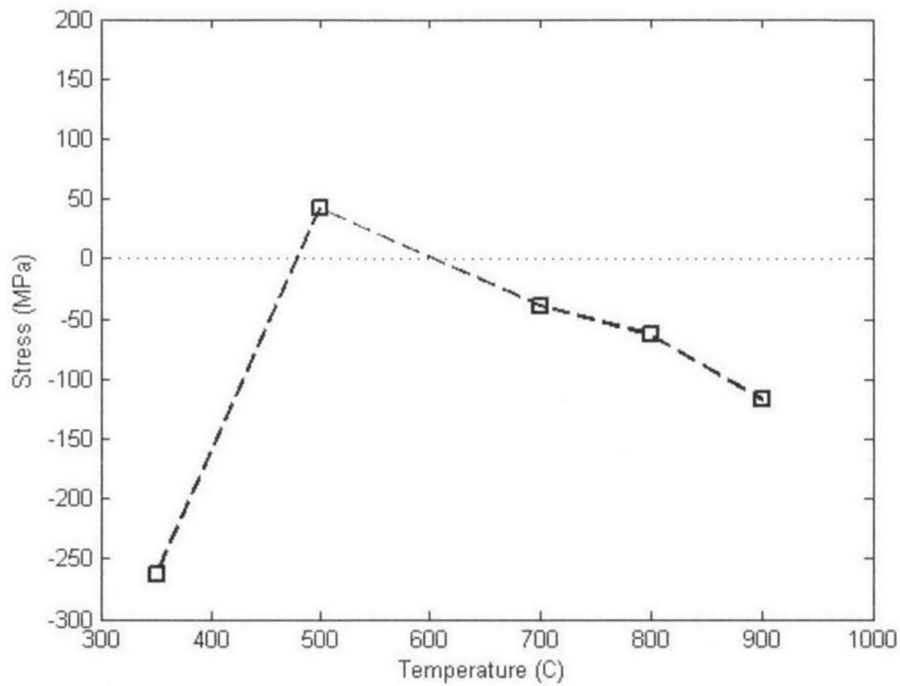


Figure 2-6: Stress vs. annealing temperatures at with Rapid Thermal Processing with nitrogen flow.

Chapter 3

Challenges and Engineered Solution

3.1 Thermal Stress and Intrinsic Stress during Annealing

The measured stress described in Chapter 2 was at room temperature measured by the FLX 2320 system. However, the film stress when the samples are being annealed in the furnace is unknown. The annealing furnace on campus is a shared multi-user tool without an in-situ stress measurement capability. We observed film cracks for films with thickness over a micron. The stress during the annealing process is important for analyzing film cracks, so in this section we will estimate the maximum stress based on the measured residual stress and the thermal stress model.

During the thermal annealing process, the maximum stress measured at room temperature is 717 MPa after annealing at 648 °C, see Figure 2-3. The total stress when the sample is in the furnace is a sum of the measured residual stress and the stress caused by thermal expansion difference between silicon and silicon oxide. The thermally induced stress can be estimated by equation 3.1, assuming that material properties are constant,

$$\sigma_t = \frac{\Delta T(\alpha_f - \alpha_s)E_f}{1 - v_f} \tag{3.1}$$

where σ_t is the thermally induced stress, ΔT is the temperature difference of room temperature and the annealing temperature, v_f and E_f are the Poisson's ratio and Young's modulus, and α_f, α_s are the thermal expansion coefficients of the film and substrate, respectively. In this case, room temperature is assumed to be 20 °C. Values of PECVD TEOS oxide and silicon from literature are used with 85 GPa for $E_f/(1-v_f)$, 2.6×10^{-6} K^{-1} for α_f and 3.6×10^{-6} K^{-1} for α_s [30].

The thermally induced stress is linear with the annealing temperature, shown in Figure 3-1. At 648 °C, where the maximum residual stress occurs, the thermal stress is estimated to be 53 MPa. The total maximum stress is estimated to be 770 MPa at 648 °C when the sample was in the furnace.

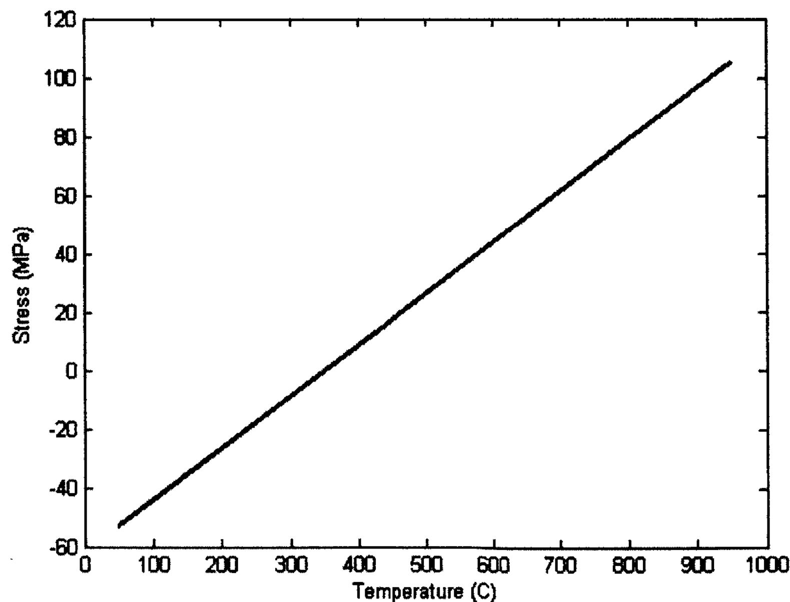


Figure 3-1: Theoretical thermal stress in TEOS oxide film with 350 °C as deposition temperature

3.2 Film Crack Mechanism

During the experiments, the high tensile stress did not cause any problem except excessive wafer bow for thin films with thickness less than 550 nm. However, for films that were more than ~800 nm thick, surface cracks were observed over the film surface. It is well-known that excess tensile stress can create surface cracks. Hutchinson and Suo provided a thorough study on thin film fracture mechanics [31, 32]. The model of a crack propagating in a thin film is governed by Equation 3.2,

$$G = Z\,\frac{(1-\nu_f)\sigma_f{}^2 h_f}{E_f} \geq G_c = \frac{(1-\nu_f{}^2){K_{IC}}^2}{E_f} \tag{3.2}$$

where G is the strain energy release rate, G_c is the critical strain energy release rate, σ_f is the film stress, Z is a dimensionless number, and K_{IC} is the mode I critical fracture toughness of silicon oxide that is reported to be 0.77 ± 0.15 MPa $\cdot$ m$^{0.5}$ [33]. The Poisson's ratio ν_f of PECVD TEOS oxide is reported to be 0.25 [30]. Z is 3.951 for a short isolated crack nucleated from a defect, and 1.976 for an unstable channeling crack that will lead to not just a single crack but a connected channeling crack network. An isolated crack is induced by defects, arrested by the interface and usually tolerable for most applications. If G becomes larger than the G_c, cracks will emerge and grow. Note from Equation 3.2, the critical film thickness without cracks is inversely proportional to $\sigma_f{}^2$. The predicted critical channeling crack-free film thickness is calculated to be 633 ± 246 nm. The large range comes from uncertainties in the reported mode I fracture toughness [33]. Throughout the experiments, the thickest film that had no observed channeling cracks after being annealed above 800 °C is 716 nm, but isolated cracks were observed at the

wafer edges where defects were created by handling. Therefore, the experimentally observed critical crack-free thickness falls in the range predicted by the model.

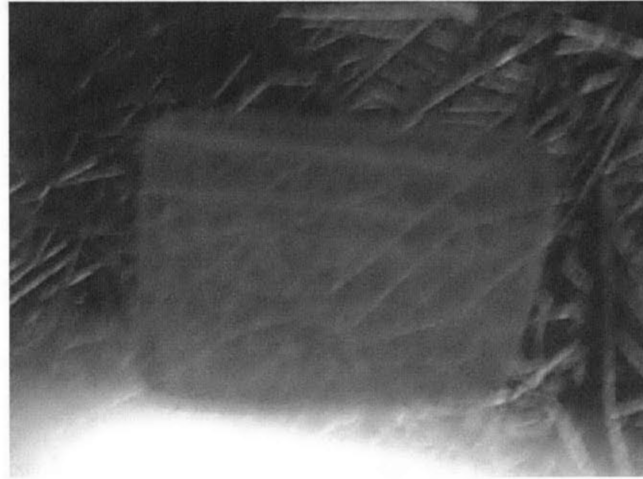


Figure 3-2: TEOS silicon oxide film cracks observed.

3.3 Multi-layer Annealing and Deposition

The water absorption effect and the cracks caused by high tensile stress are the major challenges for having thick oxide films with stable low tensile stress, especially if wet processing is involved. Experiments demonstrated that the stress will change towards compressive if the sample is exposed to water, see Section 3.4.

To obtain thick oxide film without cracks, we prepared multi-layer film by iterating deposition and annealing. The single layer thickness was less than the maximum critical thickness (around 716 nm), which experimentally guarantees no channeling cracks. After annealing above 800 °C, the stress will be less than or equal to 200 MPa tensile, and the film will have a predicted critical

crack thickness larger than 9.4 ± 3.6 μm from Equation 3.2. A film with thickness of 2.6 μm was obtained by depositing/annealing for 5 times. The thick film was etched back by 10:1 hydrofluoric solution. No cracks were observed during periodic examination under a microscope. To avoid having cracks, the film has to be annealed to low tensile stress with every thickness increase of 500 - 600 nm, which takes additional processing time especially because of the slow heating and cooling rate of our quartz furnace.

3.4 Humidity Induced Stress Change

3.4.1 Stress Change in Air Over Time

From experimental observations, films deposited from higher fraction of HF plasma have unstable stress. The stress will decrease rapidly if the film is kept in the cleanroom ambient, as shown in Figure 3-3.

A 90% HF film that was annealed at 600 °C was stored in a cleanroom ambient with relative humidity between 40% - 50%. Tensile stress was found to decrease from 522 MPa over time and stabilized at 234 MPa after 36 hours. Similar observations were found in the literature [19]. The cause of decrease in stress was found to be vapor water being absorbed into the porous oxide film from a series of experiments.

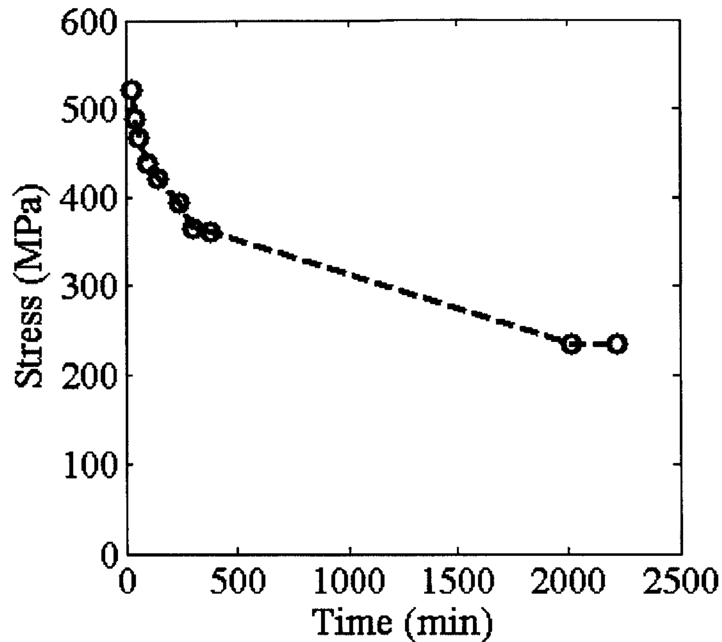


Figure 3-3: Film stress vs. exposure time to laboratory air. Stress drops over time for a 90% HF film annealed at 600 °C.

3.4.2 Water Rinse and Hot Plate

The sample described in Figure 3-3, which has a stress stabilized at 234 MPa tensile, was heated on a hotplate at 110 °C for 20 min to desorb water, and once the sample cooled to room temperature, the immediately measured stress recovered to 511 MPa, almost the same as its original stress. In contrast, the sample was then kept in a vacuum chamber at room temperature for five hours. The stress stayed constant around 507 MPa during a five-hour period with measurement every one hour. This first set of tests proved that 110 °C will vaporize the absorbed water, and can restore the stress back to high tensile.

A second set of experiments showed that abundant water will change the stress at a much faster rate than keeping it in the cleanroom ambient with water vapor in the air. The same sample was rinsed by deionized water for about 20 seconds, dried by nitrogen gun, and the immediately measured stress dropped rapidly below 300 MPa within 15 min. That stress change rate is at least 20 times faster than keeping the sample in the cleanroom ambient.

The discovery from the above two sets of experiments proved that water vapor can be absorbed in the porous film and cause dramatic stress change towards more compressive. This raises the concern for this type of oxide film to be used for any wet processing.

3.4.3 Piranha Cleaning

A series of wet cleaning experiments were conducted to understand the magnitude and impact of stress change caused by wet processing.

The stress of the sample shown in Figure 3-3 changed from 511 MPa to 234 MPa by keeping it in the cleanroom ambient. That sample was only annealed up to 600 °C. Table 3.1 shows stress change of different samples annealed at higher temperatures, after going through the piranha clean and DI water rinse. After high temperature annealing, the sample degases and becomes densified, and the stress change is less significant in these high temperature annealed films. The maximum stress decrease found was 40 MPa, for a 100% HF film that was annealed at 820 °C.

Intuitively, the oxide film deposited with LF plasma will be denser and will be less affected by the water vapor caused stress change. Therefore, a thin cap (~40 nm) of 100% LF dense oxide

was deposited on top of 2.1 μm 100% HF oxide. The entire stack was annealed at 785 °C, with residual tensile stress of 215 MPa which is the highest among the samples listed in Table 3.1. Surprisingly, the thin cap was dense enough to prevent water vapor diffusion, and the stress of that film did not change after wet processing at all. For applications without oxide etching, such a stack can serve as a stable low tensile stress film. For processes that will etch oxide, a designed stack with very thin LF oxide left after etching, will prevent stress from changing during wet processing.

From experimental observations, thicker films suffer less stress change due to water absorption. One possible explanation is that water can only diffuse through a smaller percentage of thicker films. Further analysis with SIMS for a water vapor concentration distribution can tell us how deep the water vapor can diffuse into the film.

Table 3.1: Stress change of high temperature annealed films before / after wet processing

Deposition Parameters	Oxide Thickness (nm)	Annealing Temp (°C)	Post Annealing Stress (MPa)	24hrs Post Piranha Stress (MPa)	Stress Change (MPa)
88% HF	307	820	36 (T)	6 (T)	30
100% HF	439	820	130 (T)	89 (T)	41
90% HF	589	827	51 (T)	33 (T)	18
3 layers 100% HF	1941	835	66 (T)	50 (T)	16
3 layers 100% HF	1650	847	25 (C)	30 (C)	5
4 layers 100% HF with 40nm dense cap	2130	785	215 (T)	215 (T)	0

3.5 Evaluation of the Multi-Layer Tensile Stressed Oxide Film

3.5.1 Plasma Etch Rate

To characterize the etch resistance, deposited films were etched in three ways (Table 3.2): buffered oxide etch (ammonium fluoride: hydrofluoric acid 7:1) 3 min, PlasmaQuest electron cyclotron resonance (ECR) etcher for 3mins (5 mTorr pressure, 10 sccm H_2 flow rate, 20 sccm CF_4 flow rate, 100 W ECR power, 20 W RF power), and STS deep reactive ion etch (DRIE) system for 3 min (30 mTorr pressure, 150 sccm SF_6 flow rate, 600 W RF power, 250 W platen power).

The selectivity of the oxide film over silicon is important for designing fabrication processes, especially for etching. Therefore, the etch resistance of this stress-controlled film was studied. The thermally grown oxide at 1050 °C, 100% HF TEOS oxide annealed at 803 °C and 100% LF TEOS oxide annealed at 803 °C were etched by ECR RIE, DRIE and buffered oxide etch to compare their etch resistance (see Table 3.2). The 100% HF deposited and annealed film showed slightly lower etch resistance to plasma etching, and much lower etch resistance to wet etching, compared to the etch rates of thermal oxide. The much lower wet etching resistance of 100% annealed film can be explained by the film porosity which allows water and acid absorption, and is logically consistent with results discussed in Section 3.4.3. The uncertainties for the data in Table 3.2 come from measurement errors of the film thickness (±10 nm); thus, the etch rate uncertainties are around ±3 nm/min.

Table 3.2: Etch rates of LF and HF oxide films compared to thermal oxide

	Thermal Oxide Etch Rate (nm/min)	Low Freq Annealed at 800 °C Etch Rate (nm/min)	High Freq Annealed at 800 °C Etch Rate (nm/min)
PlasmaQuest ECR	40	42	43
STS DRIE	39	46	50
Buffered Oxide Etch	72	73	123

3.5.2 Releasing into large area free-standing membranes

3.5.2.a Membrane Fabrication

Oxide films were then released to free-standing membrane by etching from the backside using a STS DRIE system and potassium hydroxide (KOH) etching. The membrane deflection was then measured by a WYKO NT3300 optical profilometer.

A 1.2 μm thick 100% HF TEOS oxide film that was annealed at 803 °C and a silane PECVD oxide film with similar thickness were released to free-standing membranes. The TEOS sample had a stress stabilized at 143 MPa tensile, while the silane sample had a stress of 322 MPa compressive. The samples were first silicon DRIE etched by the STS1 tool in MTL with SF_6 until ~50 μm of silicon was left, then 20% KOH etched at 80 °C to remove all the remaining silicon and finally rinsed in deionized water, depicted in Figure 3-4. The released films had an open area on the order of a few square millimeters.

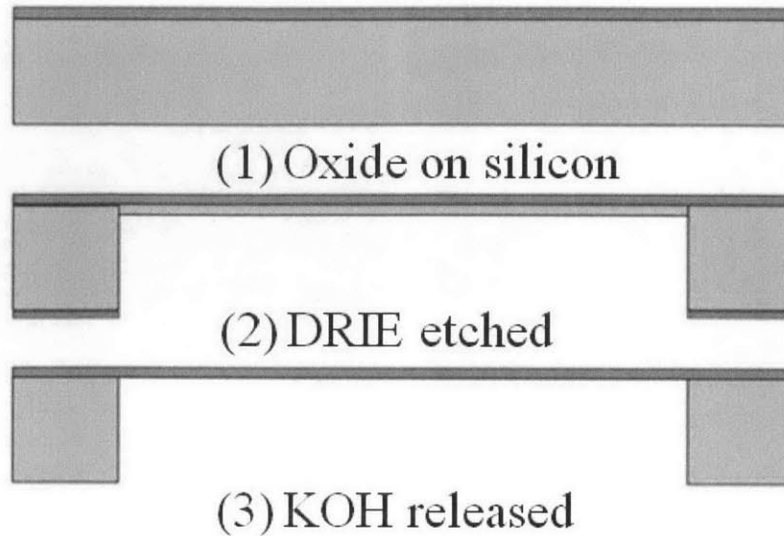


Figure 3-4: Process of DRIE with kapton tape as mask and KOH wet etching to release free-standing oxide membrane.

3.5.2.b Released Membranes

As shown in Figure 3-5, the compressively stressed oxide showed large out of plane wrinkling. The surface depth was measured by a WYKO optical profilometer, which showed that the surface depth peak-to-valley difference ranged from 40 to 100 μm. On the other hand, the TEOS film gave a tight and flat released film with no depth difference measured by WYKO. The residual stress of the released membrane is unknown. However, from previous experiments, the wet processing typically induces a less than 40 MPa stress drop, so the estimated stress of the released film is around 100 MPa tensile.

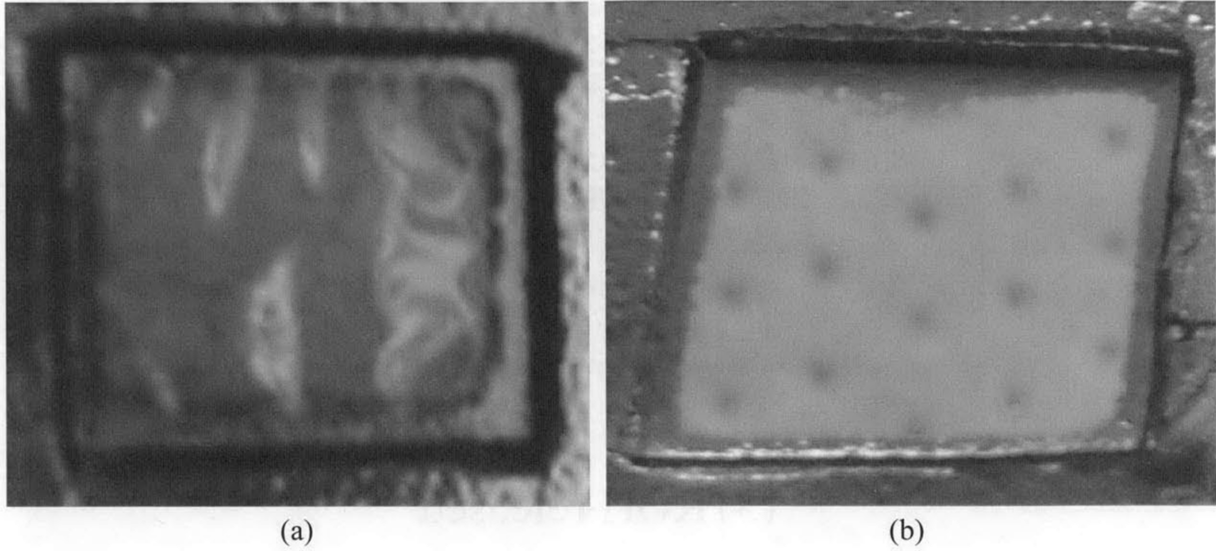
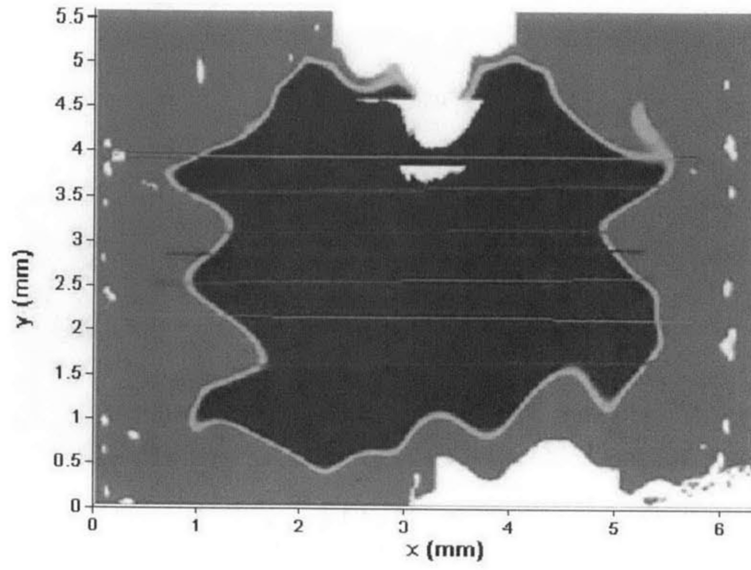


Figure 3-5 : (a) ~1 μm thick silane PECVD oxide with 322 MPa compressive stress, resulting in wrinkled membrane with 3 mm x 3 mm open area (b) ~1 μm thick TEOS PECVD 100% HF oxide annealed at 803 °C with 143 MPa tensile stress released to a flat membrane with 5 mm x 4 mm open area, seeing through to a dimpled clean room wipe.

Different samples were released to free-standing membranes as well. By comparison, Figure 3-6 and Figure 3-7 show optical profilometer data of one tensile stressed oxide membrane, and one compressive stressed oxide membrane, both with ~1 μm membrane thickness and similar opening area.



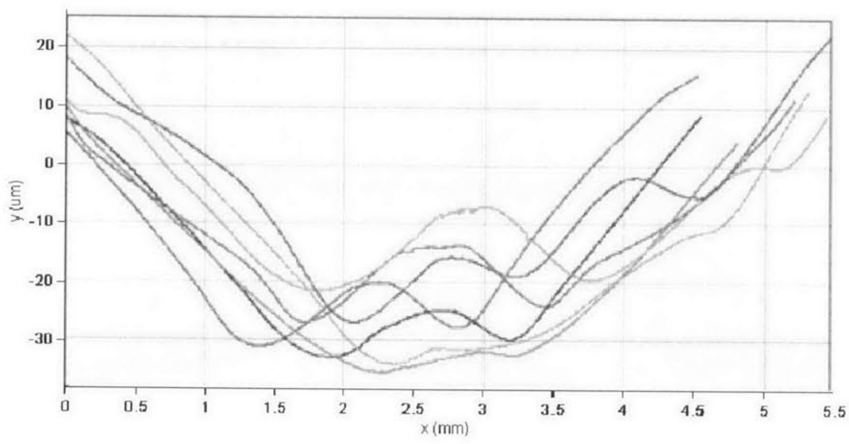
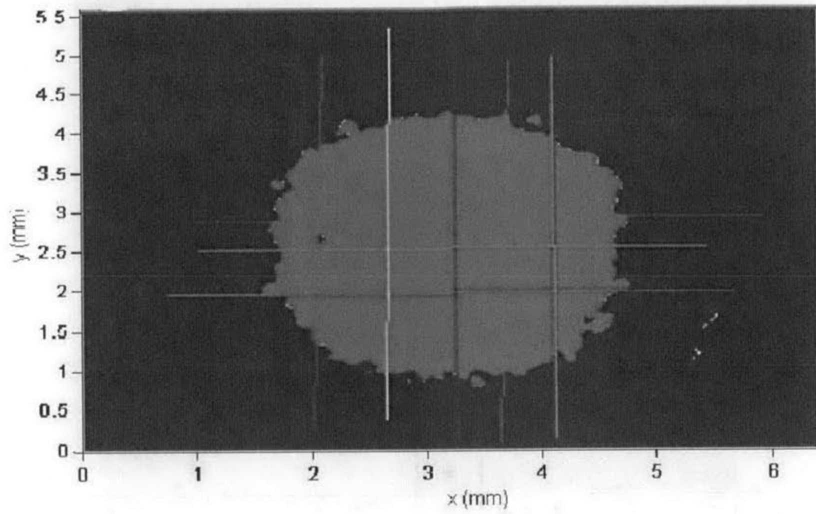


Figure 3-6 : (a) a ~1 μm thick oxide membrane fabricated from TEOS oxide, with large area opening of ~4 mm x ~ 4mm, and initial stress of ~100 MPa compressive stress (b) optical profiler indicates the membrane is wrinkled, and has a sag over 40 μm



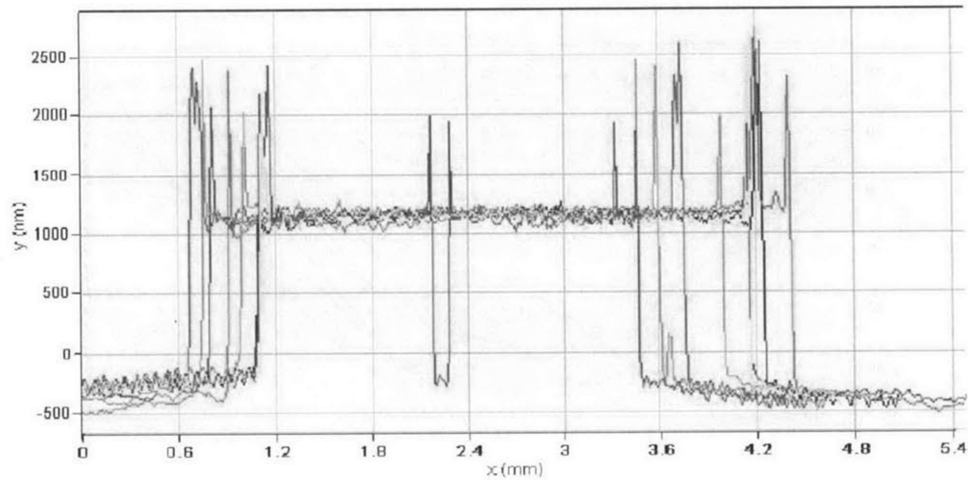


Figure 3-7 : (a) a ~1 μm thick oxide membrane fabricated from TEOS oxide, with large area opening of ~3 mm x ~ 3 mm, and initial stress of ~150 MPa tensile stress (b) optical profiler indicates the membrane is flat

3.6 Stress Balance Design

As discussed in Section 3.4, the tensile stressed TEOS oxide is vulnerable to water absorption. The stress will change towards compressive slightly if left in cleanroom ambient, which is not a problem in most cases. However, if the fabrication process requires wet processing, the stress will change from a few MPa to ~50 MPa towards compressive, as shown in Table 3.1. A very thin layer of LF deposited TEOS oxide (~40 nm) was demonstrated to be sufficient in preventing water diffusion into the film.

To completely eliminate water absorption risks, one solution is to deposit a sandwich oxide layer as depicted in Figure 3-8. First, on the substrate, use 100% LF plasma to deposit a protective layer with thickness t3. The thickness t3 has to be larger than potential thickness loss to prevent water absorption from the backside. Then, deposit the tensile stressed 100% HF layer to desired thickness t2, following the procedure described in Section 3.3. Finally, deposit another protective layer from 100% LF plasma with thickness t1, which has to cover thickness loss from CMP plus any potential thickness loss in any etch step. Thickness t2 has to be chosen to control the overall stress to be tensile to avoid buckling. All the values of t1, t2, and t3 need to be chosen with certain safety factor, depending on the application requirements.

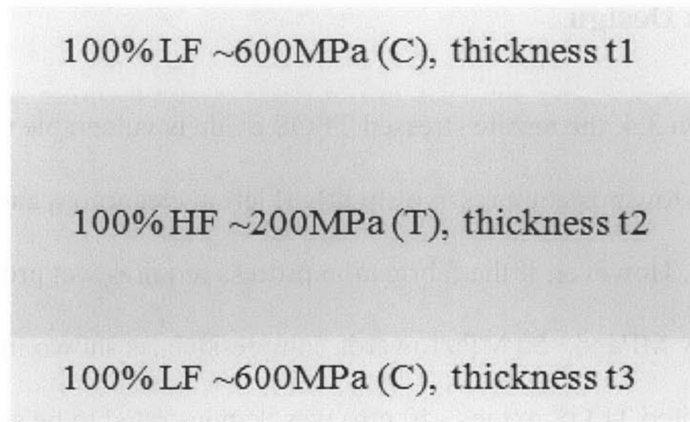


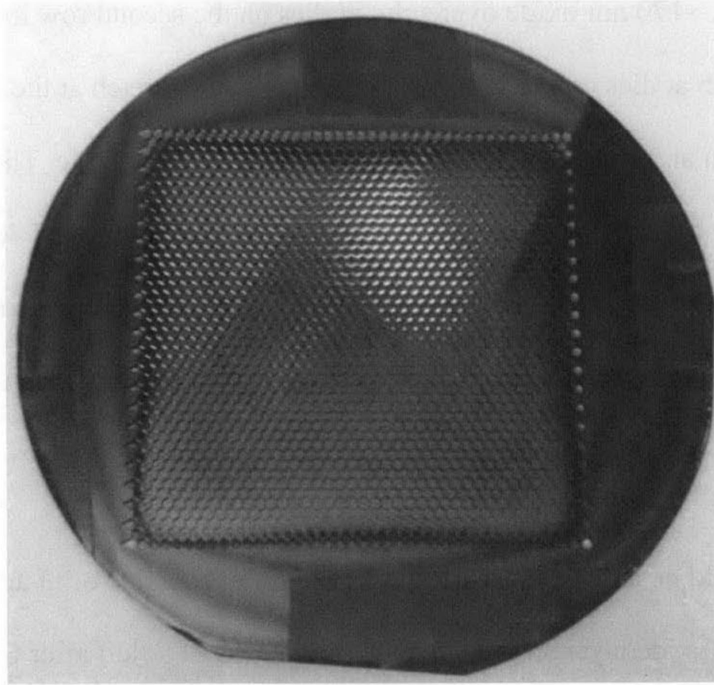
Figure 3-8: Diagram of stacked oxide layers with protective LF deposited layer, and HF deposited stress control layer.

For the fabrication of CAT gratings, the front grating etch is a deep silicon plasma etch that will stop on the buried oxide layer, see Figure 1-4 step F3. From past experimental data, the buried oxide thickness reduction from front side etch is not noticeable when under SEM inspection with zoomed in view for oxide notching. Therefore, we can safely assume the front side oxide loss is less than 30 nm. In current experiments, the CMP process removes 500 nm thick oxide, which may be an overkill. If tool setup is consistent, after a pilot wafer, ~ 100 nm oxide thickness reduction will yield the desired surface roughness. In conclusion, the thickness t1 should be 30 nm, plus the amount removed in CMP process, and plus an additional safety layer of 40 nm.

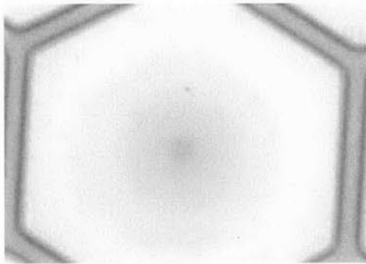
The backside etch is also a deep silicon plasma etch that will stop on the backside of the buried oxide layer, Figure 1-4 step B1. Figure 3-9 shows a sample deep etched with SPTS Pegasus tool to stop on the buried oxide. The original buried oxide thickness was 250 nm. In a test experiment ran at SPTS Pegasus with the Claritas end-point-detection system based on optical emission spectroscopy, the backside deep silicon etch stopped with only ~70 nm oxide overetch on the

center of the pattern, ~170 nm oxide overetch at dies on the second row to the edge, and more than 250 nm overetch at dies on the last row. The excessive overetch at the last row was caused by difference in open area, as one side was completed masked by oxide. Therefore, the value of t3 should be larger than 170 nm with certain safety factor, plus additional 40 nm safety layer, resulting in a total value of ~250 nm. However, if the end-point-detector is not available, then the thickness required will be significantly larger to cover the run-to-run variances.

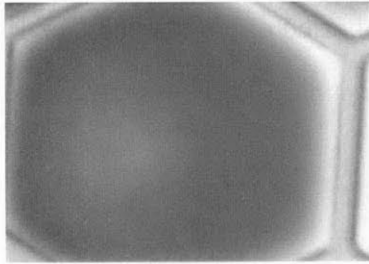
The value of t2 should be at least three times of the combined value of t3 and t1 left after CMP, to ensure the overall oxide layer stress is tensile. Thickness of t1 left after CMP will be less than 100 nm, and t3 is estimated to be ~250 nm. For CAT grating processing, t2 has to be larger or equal to 1050 nm, leading to a total buried oxide thickness of 1400 nm.



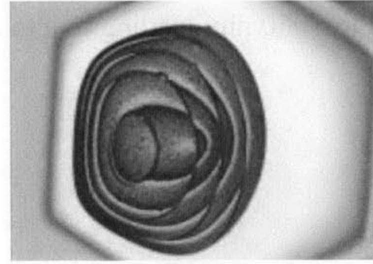
(a)



(b) 182 nm



(c) 80 nm



(d) 0- 30 nm

Figure 3-9: (a) Backside hexagon pattern deep silicon etched stopping on 250 nm buried oxide layer (b) Center die has 182 nm oxide left (c) Second row to edge has 80 nm thick oxide left (d) Last row has the oxide partially blown through with 0 – 30 nm oxide left.

Chapter 4

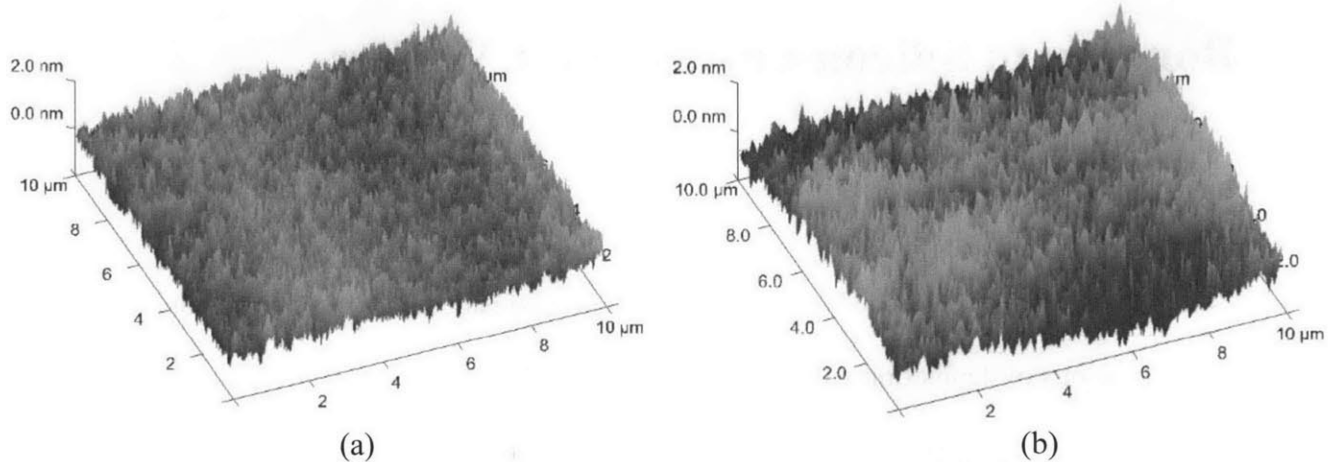
Bonding to Silicon-on-Insulator Wafers

4.1 Pre-bonding Preparation

Before the samples are bonded, pre-bonding preparation is necessary to ensure bonding quality. After iterations of deposition and annealing, dust and defects may appear on the deposited TEOS film. Moreover, the deposited film has thickness non-uniformity roughly about 5%, with thicker film at the edge than at the center. Literature shows if the root mean square (RMS) roughness is larger than 0.5 nm, fusion bonding is likely to have voids [34, 35]. Therefore the purpose of the pre-bonding preparation is to remove dusts and defects, reduce the non-uniformity, and ensure that the surface roughness is less than 0.5 nm [34].

Chemical and mechanical polish (CMP) process is used to achieve better bonding quality. After CMP, the RMS roughness typically decreases to less than 0.5 nm [34]. An edge-fast CMP setup can reduce the non-uniformity. For the CMP process, one wafer out of the batch has to serve as the pilot wafer for tuning the tool condition by polishing and measuring the polish rate. Samples with ~2 μm thick TEOS oxide layer were polished, with on average ~524 nm polished away for a targeted roughness of 0.5 nm, and the polish rate was 350 nm / min.

The surface roughness of the samples was measured by Atomic Force Microscope (AFM) before and after the CMP process, shown in Figure 4-1. Surprisingly, the RMS roughness of the polished film is larger than that of the as-deposited film.



(a) (b)

Figure 4-1: (a) AFM shows 0.25 nm RMS roughness of the as deposited TEOS oxide film in a 10 µm × 10 µm area (b) AFM shows 0.45 nm RMS roughness of the CMP polished TEOS oxide film in a 10 µm × 10 µm area.

4.2 Fusion Bonding Process

After the CMP polish, the next step is bonding the substrate with oxide layer to the device wafer, as illustrated in Figure 4-2. First the substrates with the oxide film and the device substrates need to be cleaned by RCA right before bonding. Then the surface may undergo surface treatments to increase the surface energy, or lower the required bonding temperature, by HF dip or short plasma etch [37, 38]. In our work, no special surface treatment was used. This could be looked into if the bonding quality needs to be improved in future applications.

The next step is the actual bonding. For proof of concept, we used Ultralsil, a wafer manufacturer, to have the samples bonded for us. MTL also has the capability for wafer bonding. First load the device wafer and the handle wafer into Electronic Vision EV450 for alignment using the fusion bonding program, then the program will start the EVG PV1 bonder to set the bonding conditions. In the bonding experiments, the temperature was set at 400 °C, the ambient pressure was pumped to less than 1×10^{-3} torr vacuum, and a pressure of 4000 mbar was applied to force the two samples together. The bonding strength was dominantly determined by the surface roughness, temperature, and the applied pressure. The bond strength is essentially not a function of the bonding time [36]. In practice, 30 min bonding duration was used. After the bonding, the samples were annealed in a furnace tube to increase the surface energy. The higher the annealing temperature, the higher the bonding strength [36]. After furnace annealing, the device was CMP polished to the desired thickness. In our case, the desired thickness is ~4 μm. Finally, to prepare the SOI wafer for CAT grating, ~300 nm of thermal oxide will be grown on the both the device layer and the handle layer, followed by PECVD oxide from saline on the back of the handle layer.

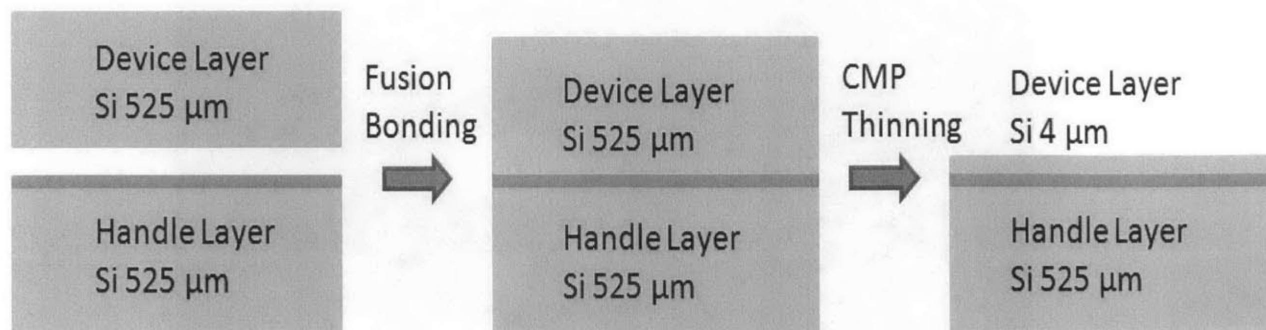


Figure 4-2: Diagram of bonding TEOS oxide into SOI wafer.

4.3 Post-bonding Annealing & Bonding Quality

After the samples being bonded and annealed, an infrared camera setup was used to check the bonding quality, as shown in Figure 4-3. The SOI wafer was illustrated by a bright broad band light bulb from the bottom, and the image was captured by an infrared camera on the top. If there were voids from the bonding, fringes will show up on the monitor.

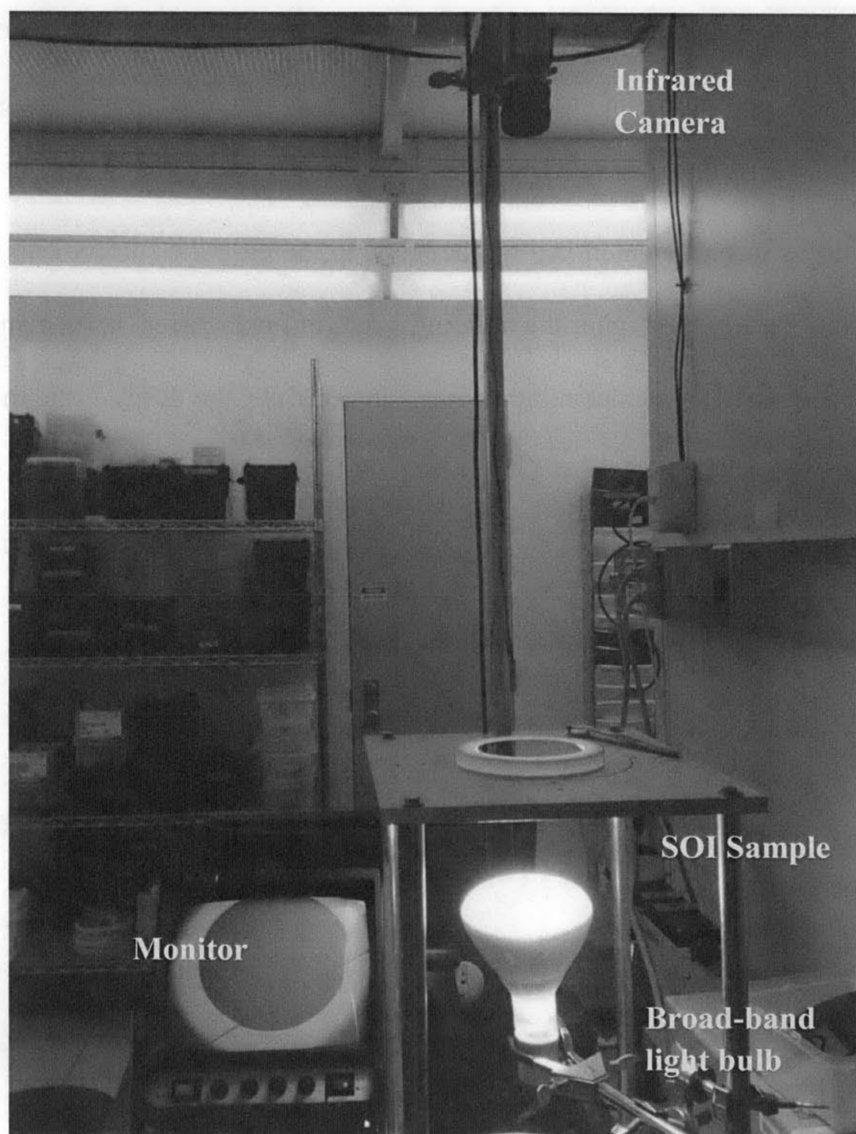


Figure 4-3: Setup of the infrared camera to detect bonding voids.

All the bonded wafers during the experiment did not show any sign of voids. The real indicator of the bonding quality is the surface bonding energy. A common evaluation approach was developed by Maszara called the double cantilever beam test [36, 39, 40], illustrated in Figure 4-4.

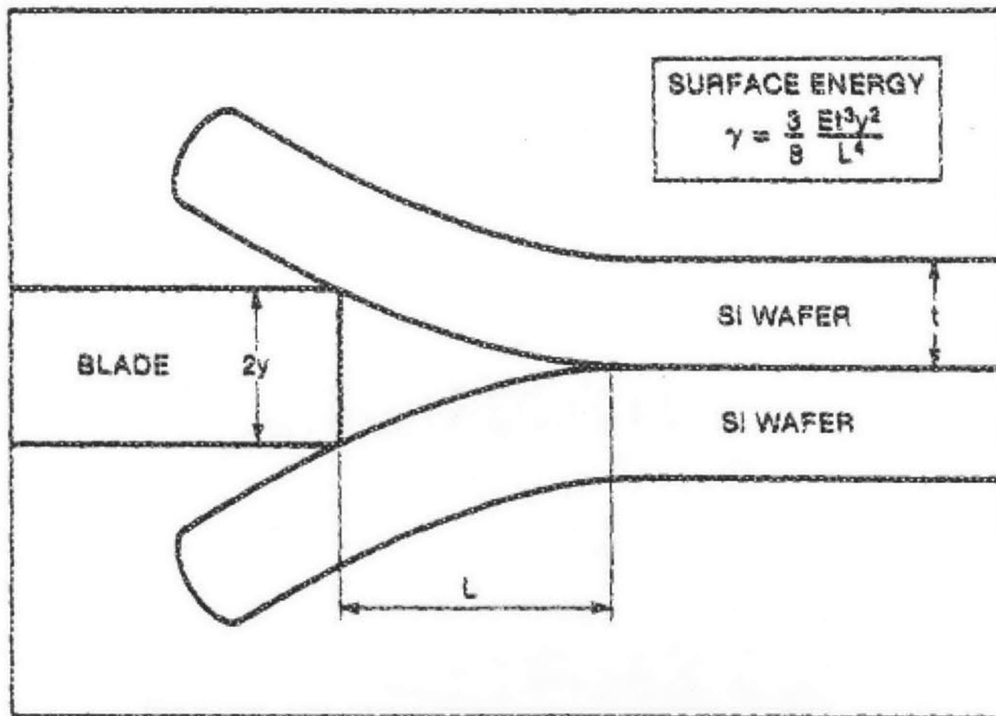


Figure 4-4: Diagram of inserting a razor blade for measuring the crack length that can be used for calculating surface energy [36]

The wafers were forced apart by insertion of a thin blade into the bond interface. The separated members of the crack at the bond interface are considered as two cantilever beams clamped at

the crack tip. From beam theory, the cohesive surface energy γ can be accurately estimated from Equation 4.1.

$$\gamma = \frac{3}{8}\frac{Et^3y^2}{L^4}, \tag{4.1}$$

where E is the young's modulus, t is the thickness of the wafer, y is half of the thickness of the inserted blade, and L is the measured crack propagation length. Figure 4-5 shows a bonded sample with a 100 μm thick blade inserted into the interface. The wafer was examined under the same infrared camera setup, and the crack length L was measured from the edge of the blade to the farthest fringe.

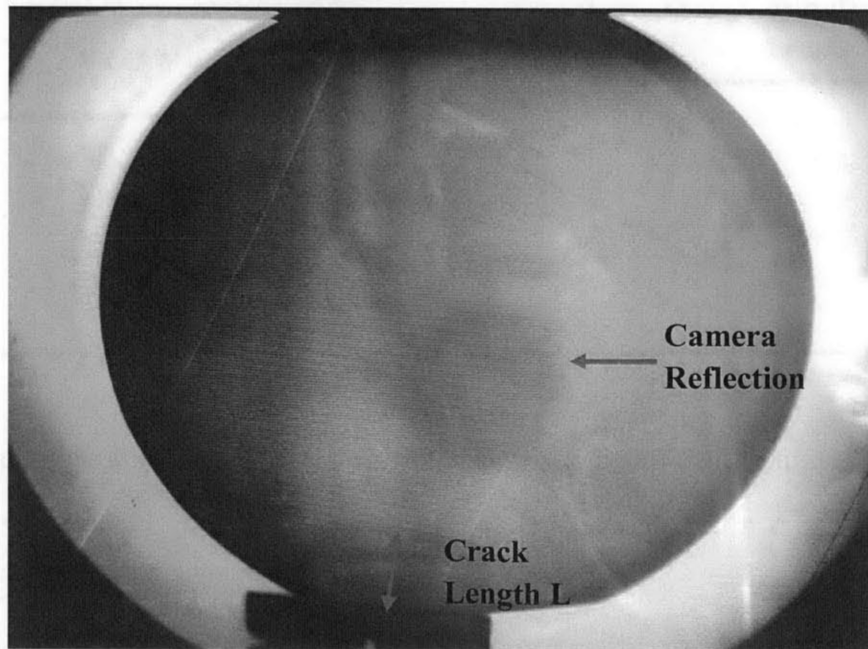


Figure 4-5: Measurement of the crack propagation length after the blade insertion

In total 9 samples were annealed at different conditions with a blade inserted to evaluate the bonding strength. Values in Table 4.1 were obtained from three samples, averaged over multiple measurements. Due to the poor resolution of the blade measurement, the uncertainties associated with the surface energy are large, as shown in Table 4.1. The surface energy values estimated were consistent with literature values [36]. Despite the large uncertainties, the surface energy increases as the annealing temperature increases.

From the following evaluation (section 4.4), the bonding strength of all three annealing conditions satisfies the processing requirements. Therefore, to make sure the buried oxide keeps a tensile stress after the bonding, and long annealing, post-bonding annealing at 700 °C was the safe condition. Since the annealing time has little impact on the surface energy, reducing the annealing time will also help keep the stress tensile, as the TEOS oxide stress becomes more compressive if annealed for a long time, see Figure 2-5.

Table 4.1: Surface energy and the annealing conditions

Annealed Temperature & Time	Crack Length (mm)	Surface Energy (erg/cm^2)
700 °C & 9 hrs	14.0 ± 0.5	593 ± 84
750 °C & 8 hrs	13.5 ± 0.5	686 ± 100
800 °C & 7 hrs	13.2 ± 0.5	740 ± 100

4.4 Bonded sample evaluation

After the optical examination with infrared camera and the blade test, samples were cleaved and imaged in SEM. Figure 4-6 shows the back side of a cleaved bonded sample. The fringes come from the TEOS oxide deposition.

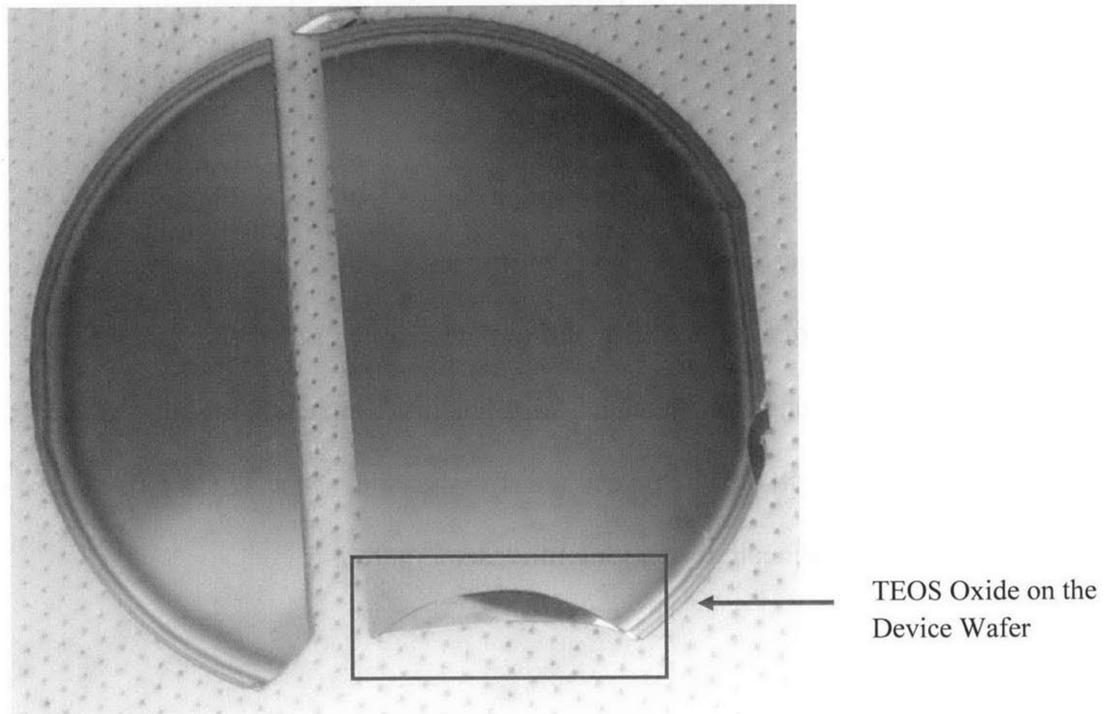


Figure 4-6: Picture of a cleaved SOI wafer, with TEOS oxide on the device wafer

Among the fabrication process of the CAT grating (Figure 1-4), rigorous cleaning and ultrasound agitation are the two critical steps that may cause the SOI wafer to debond due to weak surface energy. Therefore, small pieces of the cleaved sample were first piranha cleaned, RCA cleaned, then left in an ultrasound agitated water bath for more than 2 hours. The Crest 275D tru-sweep

ultrasonic cleaner has a frequency sweep of 42-45 KHz, and the power amplitude was set at maximum at 80 W.

After the rigorous cleaning, and the ultrasound agitated water bath, the samples were intact. Figure 4-7 showed one sample with 2.2 μm thick buried oxide. Under the SEM examination, no voids were observed. However at the edge of the sample, the buried oxide layer showed concentrated defects as shown in Figure 4-8, which were only observed at the edge of the wafer. Those defects were most likely come from the wafer handling during the complex processes of making the SOI wafer.

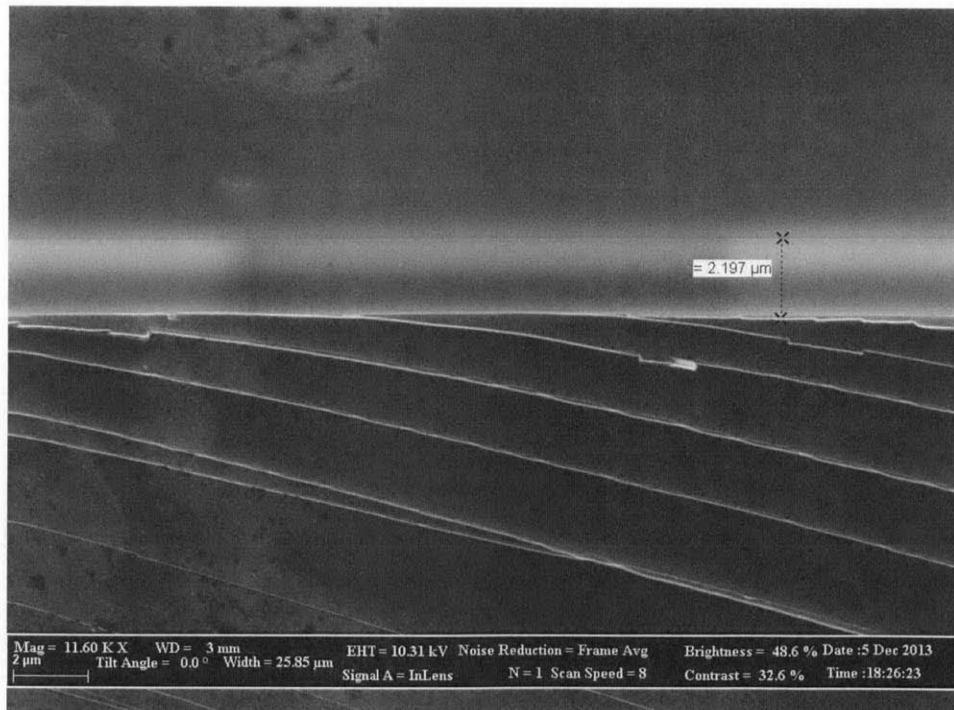


Figure 4-7: SEM image of the bonded SOI wafer, with a 2.2 μm thick buried oxide layer

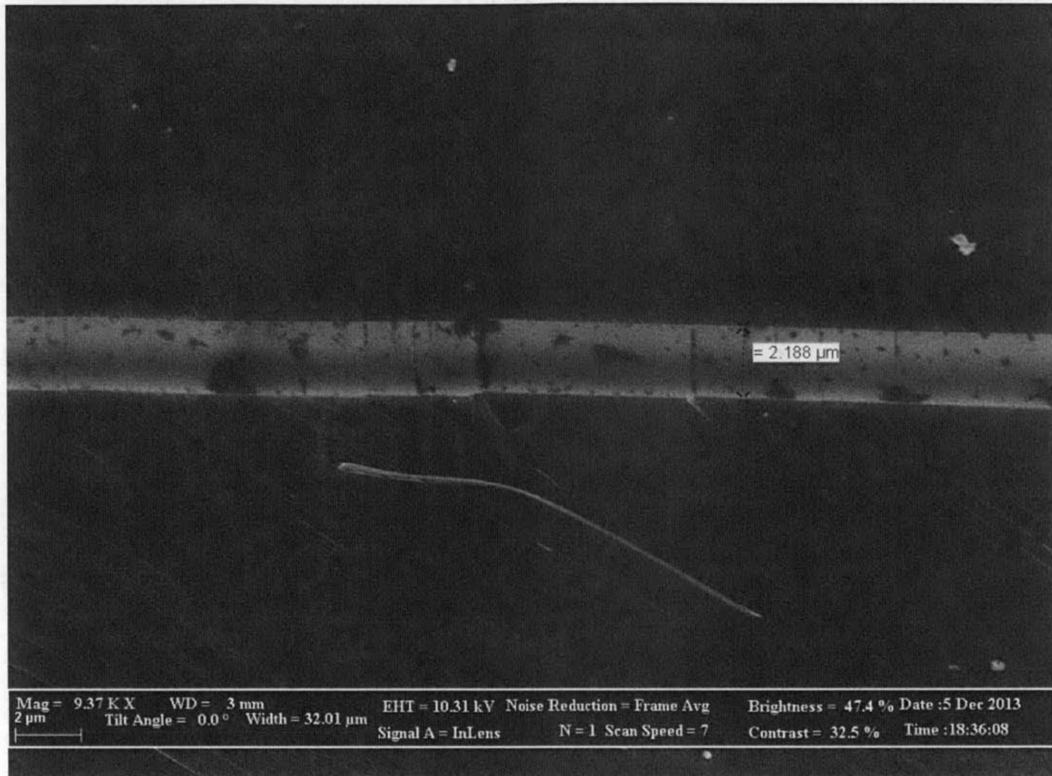


Figure 4-8: SEM image of bonded SOI wafer, with voids and defects from wafer handling

Chapter 5

Alternative Solutions

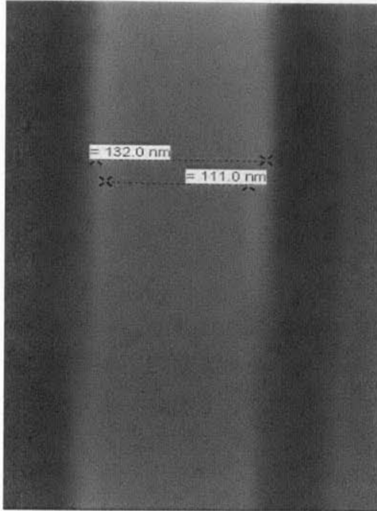
5.1 Oxidation and vapor hydrofluoric etch

From the plate buckling theory discussed in Chapter 1, the critical buckling load is proportional to the plate thickness squared, see Equation 1.5. To address the stress problem from the buried oxide layer, one alternative approach is to etch silicon grating bars with thickness over 100 nm. The theoretical buckling stress for the CAT grating bars with 4 μm depth is around 550 MPa, four times higher than that of grating bars with 50 nm thickness. With thicker grating bars, the robustness is significantly increased to allow a larger processing window. The process then uses hydrofluoric (HF) to etch the oxide, both the remaining oxide mask and the buried oxide. Once the oxide has been removed, the stress with it is also released. The next challenge is to reduce the silicon bar thickness to increase the overall CAT grating efficiency, by reducing the X-ray absorption from silicon grating bars.

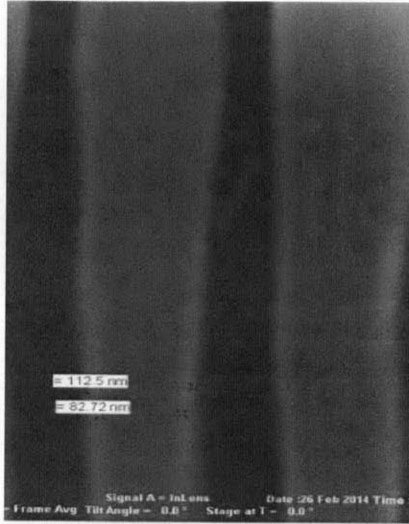
One promising approach to fine tune the silicon grating bar thickness is silicon dry oxidation with controlled growth speed followed by oxide etch. Sub-10 nm silicon dimension control has been demonstrated in fabrication of nanowires and nanopillars by dry oxidation [41, 42]. To prove the concept, a set of oxidation experiments were conducted. Three deep etched grating

samples with depth of ~ 4 μm, and grating bar thickness of ~110 nm were annealed for different durations, with temperature at 800 °C and oxygen flow rate at 5 liters per minute. The oxidation rate will increase with increased annealing temperature. 800 °C was a relatively low temperature to gain better control over the remaining silicon thickness. The samples were cross-sectional cleaved and checked by SEM every 60 min, starting from 30 min annealing. Sample SEM images were shown in Figure 5-1. For each measurement, multiple data points of the oxide thickness were estimated by SEM measurements. Figure 5-2 summarizes the oxide thickness per edge for annealing duration from 30 min to 390 min. The oxide growth rate per edge is roughly 9 nm / hr. After 390 min of 800 °C of annealing, we found the total thickness of the grating bars increased from ~110 nm to ~130 nm, because of the volume expansion in oxidation. The remaining silicon thickness becomes ~60 nm.

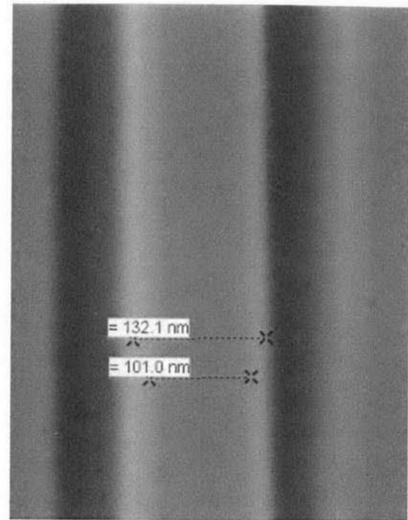
30 min



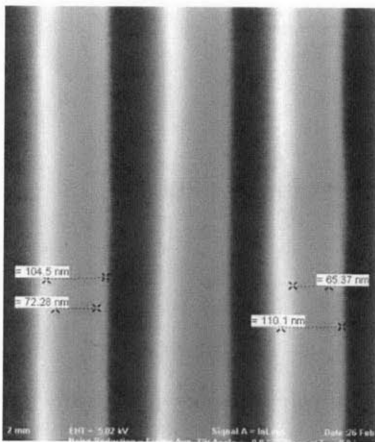
90 min



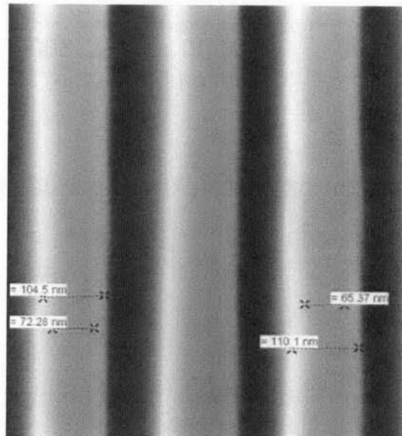
150 min



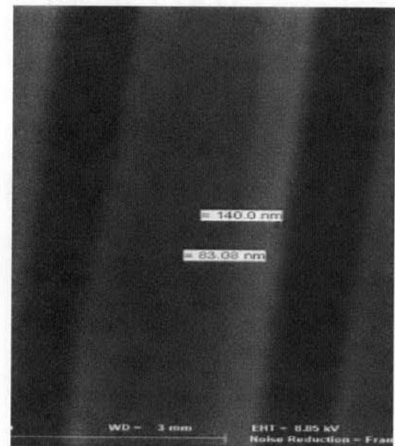
210 min



270 min



330 min



390 min

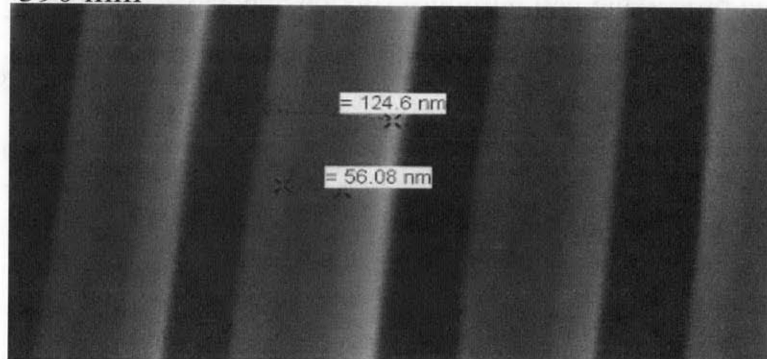


Figure 5-1: Cross-section SEM image of oxidized silicon grating bars.

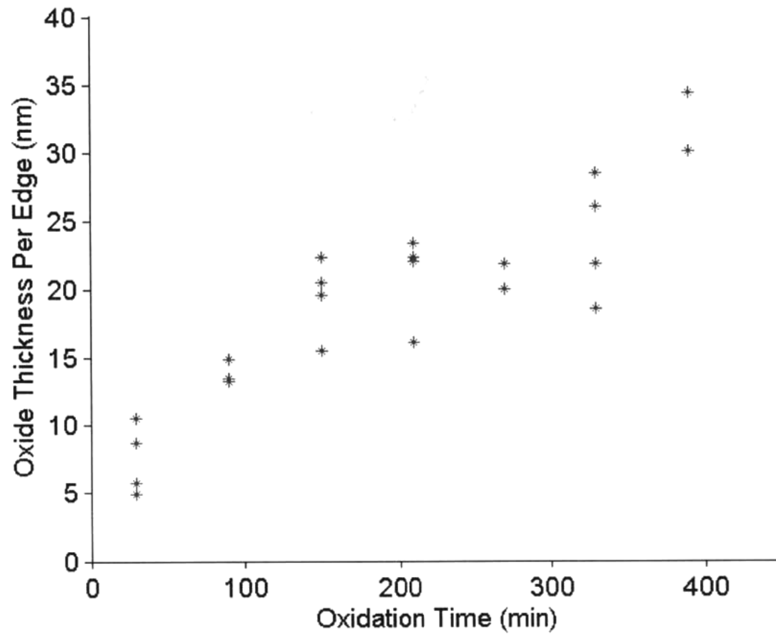


Figure 5-2: Oxidized silicon oxide thickness per edge of the grating at 800 °C.

For hydrofluoric etch, a common method is through wet etch, by immersing the sample into a low concentration hydrofluoric solution. However, for high aspect ratio structures, such as CAT gratings, the wet processing will introduce stiction and may cause grating bars to collapse. Previous fabrication used a critical point dryer to eliminate stiction caused by liquid adhesion, but that process still posts risk of stiction due to mishandling, such as exposing samples to air during transferring and excessive water brought by the sample into the critical point dryer. An alternate approach for eliminating the sticition problem is to use vapor hydrofluoric etching.

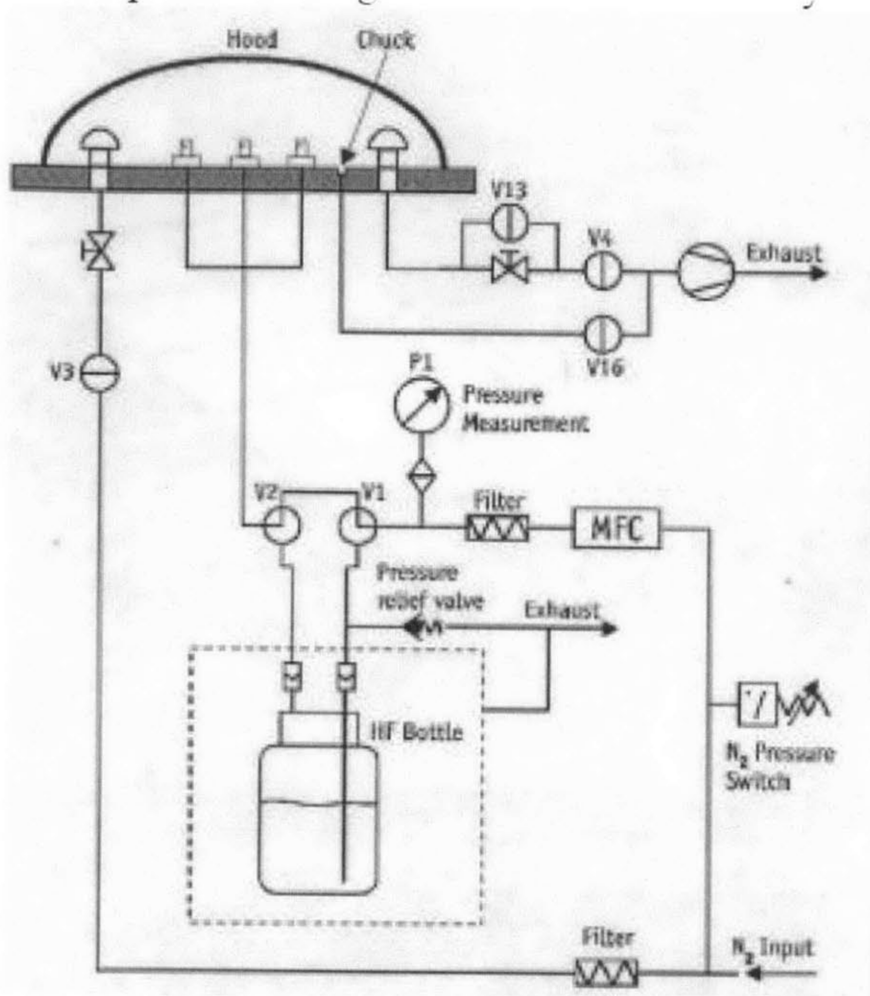


Figure 5-3: Schematic of a vapor HF etching tool with control capabilities [43].

To ensure consistent results, the vapor HF conditions have to be controlled. A sample schematic vapor HF etching device setup is shown in Figure 5-3. Nitrogen flow is passed through a MFC (mass flow controller), and bubbles through the HF solution and then into an enclosed closure with the sample in it. The wafer sample has to be heated to prevent water condensation on the sample, which will lead to structural collapse due to the stiction. The pressure in the closure can also be controlled by valves and pumps at the exhaust.

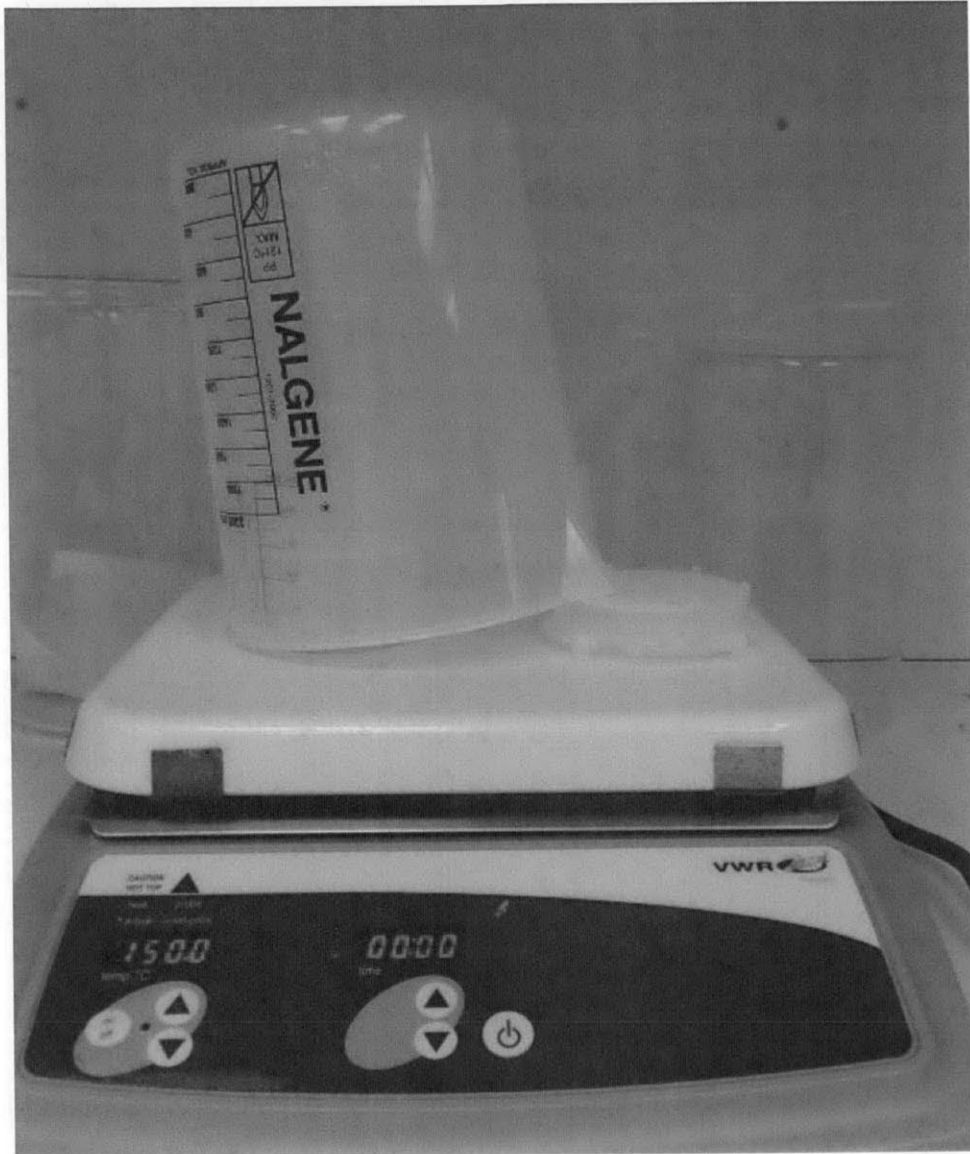


Figure 5-4: Vapor hydrofluoric etching setup.

To quickly get a preliminary etching result, a simplified vapor HF setup was established as shown in Figure 5-4. The samples and the HF solution were left on a hot plate with temperature set at 80 °C, enclosed by a large plastic beaker. 5% hydrofluoric solution was used in the experiment. The sample was left on the hot plate for 30 hr to deliberately over etch the oxide. The etch rate was unknown for this simplified setup. Literature has reported etch rate for vapor

HF etching on the order of a few nanometers per minute with the well designed setup shown in Figure 5-3 [43].

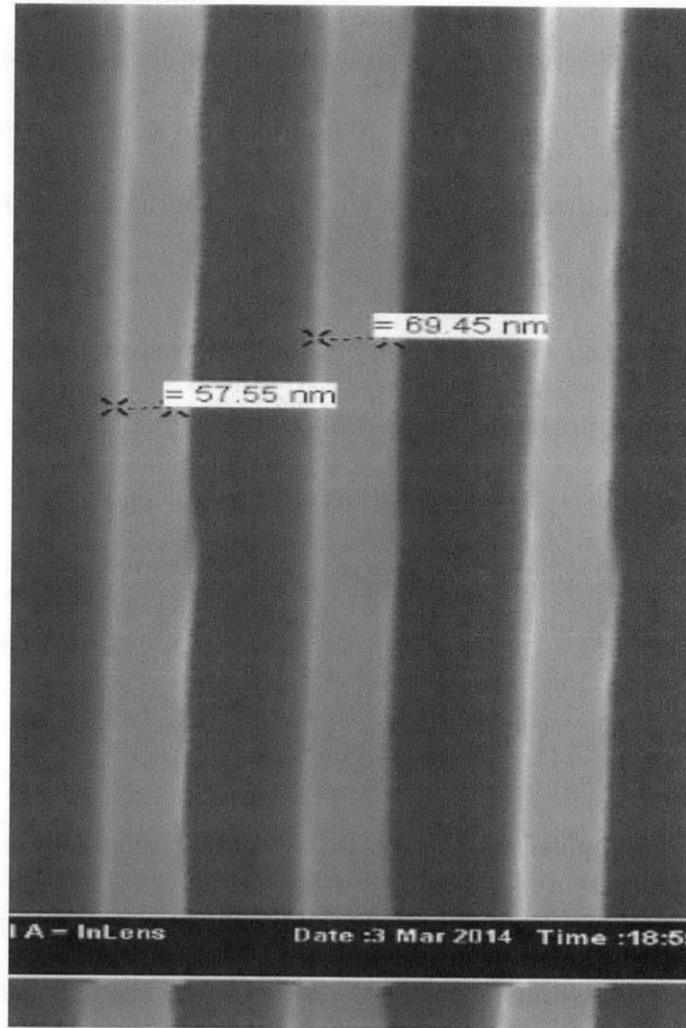


Figure 5-5: HF etched grating bars with reduced thickness from ~110 nm to ~ 60 nm after 390 min of dry oxidation at 800 °C.

Starting the silicon grating bars with thickness ~110 nm, after 390 min of annealing followed by vapor HF etch, the samples were examined in SEM. The oxide has been completely etched, and the grating bar thickness reduced from ~110 nm to ~60 nm, see Figure 5-5 and Figure 5-6 (a). However, with the thickness being uniformly reduced on the grating bar, the original profile gets translated to a much thinner grating bar, which leads to more obvious non-uniform profile. For instance, the original silicon grating bar has 110 nm thickness on top and bottom of the grating bar, and 100 nm thickness at the waist, which means 10% non-uniformity (also referred as bowing). After the oxidation and HF etch, the top and bottom may reduce to 60 nm and the waist changes to 50 nm thick, and the non-uniformity becomes 20% from the cross-sectional view. Therefore, this approach requires a high uniformity of the original profile from the deep silicon etching. The DRIE step needs to be optimized for uniform silicon profile. If necessary, KOH etching with the grating bars accurately aligned to <111> crystal plane can help reduce the bowing [44].

For the vapor HF etched samples, some of the areas showed collapsed grating bars, while other areas the grating bars were intact, see Figure 5-6 and Figure 5-7. Those collapsed grating bars could be explained by two possible mechanisms, one is stiction from water condensation on part of the sample. The other one is under the impact of cleaving energy, the grating bars collapsed together due to lack of horizontal support.

In Figure 5-7, the grating bars close to the cleaving edge all collapsed together, while at the other end far away from the cleaving edge, some of the grating bars were still separated with each

other by the same distance. This suggests that the collapsed grating bars were more likely caused by the cleaving energy, plus the fact that the sample was kept at an elevated temperature to prevent condensation. The hot plate was set at 80 °C. The temperature of the sample will be slightly lower depending on how well the contact is.

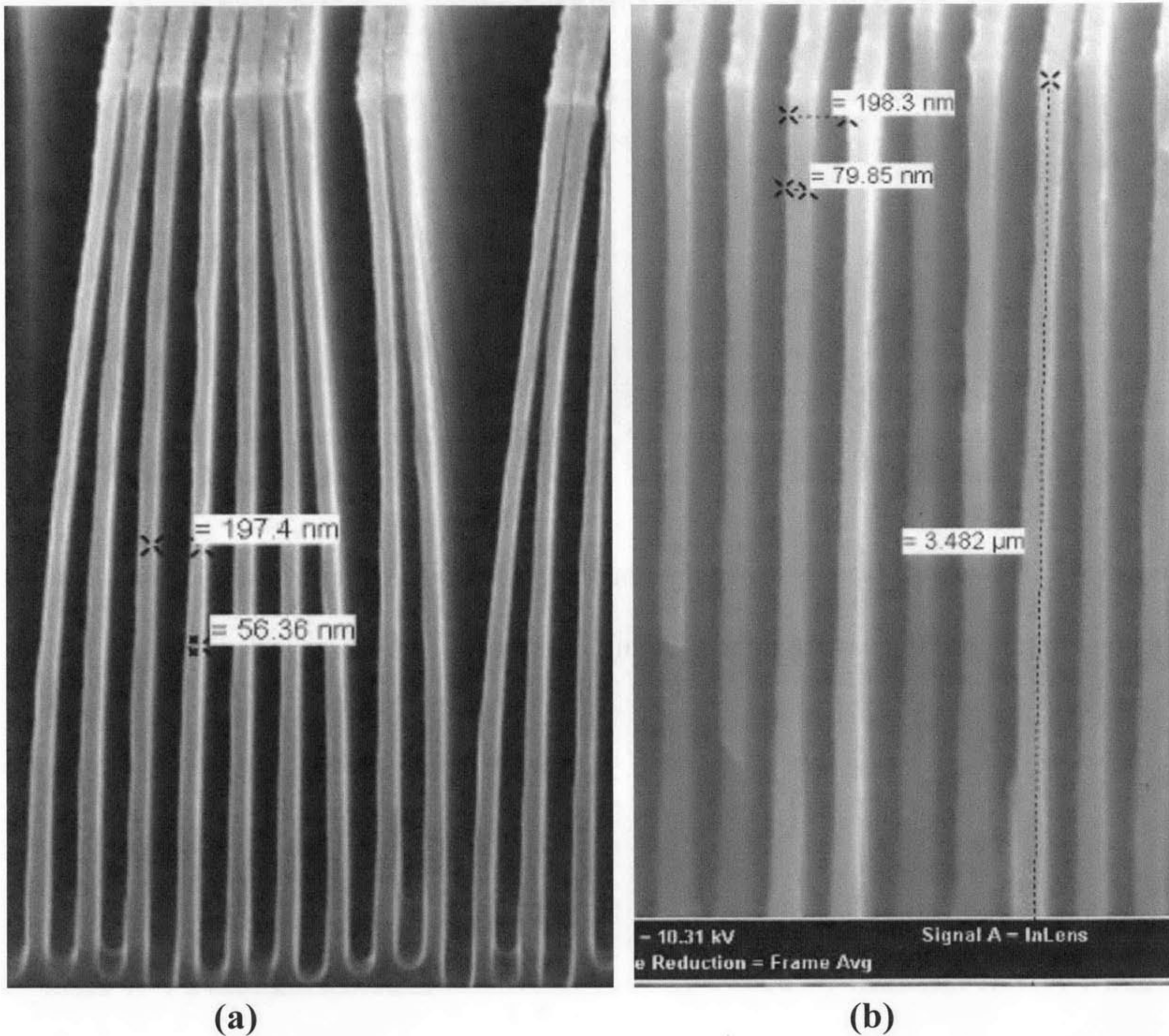


Figure 5-6: HF etched grating bars. (a) Collapsed grating bars observed on large areas (b) Intact grating bars on some areas.

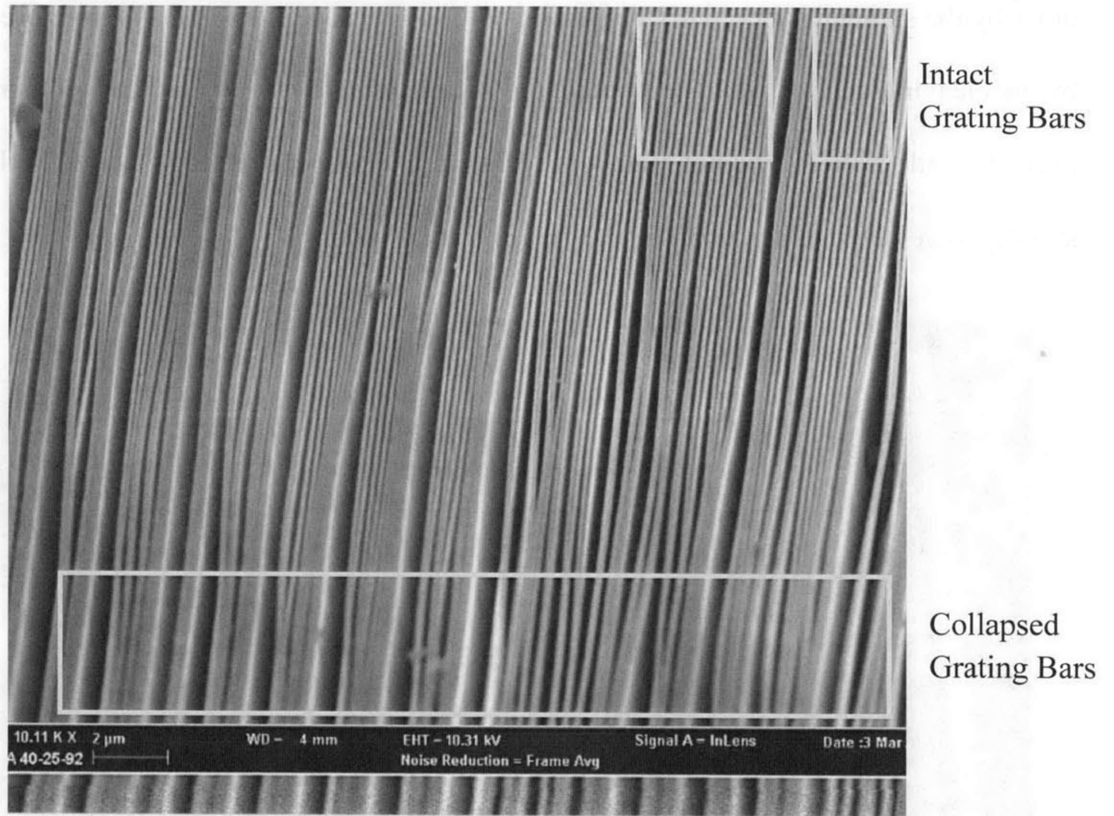


Figure 5-7: Top view of the HF etched grating bars. Observed collapse near cleaving location, intact grating lines far away from the cleaving location.

5.2 Spin-on-Glass

Apart from TEOS PECVD, another approach that may yield stable tensile stressed oxide that can withstand high temperature annealing is spin-on-glass (SOG). One paper showed that silicon oxide film obtained by spinning and baking hydrogen silsesquioxane (HSQ) can withstand high temperature and have high tensile stress [45]. The tensile stress was high enough to limit the maximum thickness without cracks after 800 °C annealing at 0.99 μm. From discussions around Equation 3.2, if the material properties are similar from this type of oxide with that from TEOS PECVD, the maximum stress in annealing the HSQ based oxide can reaches 480 – 720 MPa tensile from Equation 3.2.

Other literature shows the HSQ has tensile stress after annealing up to 550 °C, and becomes ~50 MPa compressive after annealing at 650 °C [46]. After furnace annealing at 800 °C, the stress becomes around 0 MPa. No literature shows stress data after annealing at temperatures higher than 800 °C. The precursor material used in this literature is series of Flowable-oxide from Dow Corning.

The HSQ material used in that paper is FOX-25 from Dow Corning [45]. The material is expensive (~$1200 for a bottle of 125 ml) and has long lead time (~2 months). Consequently, three similar materials spin-on-glass were explored. From the datasheet provided by vendor Filtronics, three materials will provide oxide with the right thickness and tensile stress: silicate 20F, methylsilsesquioxane 400F, and methylsiloxane 500F.

The standard procedure to spin the glass is first dispensing 2 ml of the solution on the wafer substrate. After spinning at 3000 rpm, quickly proceed to hot plate baking for 60 seconds each at 80 °C, 150 °C, and 250 °C. Finally, use the furnace to anneal the films for 1 hr at 425 °C with nitrogen ambient.

The film stress and thickness were measured after the standard procedure, shown in Table 5.1. The measured stresses were consistent with the datasheet. Then the samples were subsequently furnace annealed at 600 °C and 900 °C for half hour at both temperatures. Table 5.1 summarizes all the measured data. Unfortunately the residual stress after 900 °C annealing all became compressive.

The advantage of spin-on-glass is convenience in generating the oxide film. The three materials explored were not capable of maintaining a tensile stress after high temperature annealing, but showed promising low compressive stress after 900 °C furnace annealing. Many other similar solutions may yield the desired properties. Due to limitations of time and effort, the spin-on-glass approach was not fully studied in this work, due to the solution from TEOS PECVD. For future work, FOX-25 from Dow Corning is very promising in delivering the desired properties. Other potential precursor materials include HSQ T12 from Tokyo Ohka Kogyo Co., MSQ ACCUSPIN 418 from Honeywell Inc, and MSQ T7 and T9 from Tokyo Ohka Kogyo Co [47].

Table 5.1: Tensile stress changed to compressive after 900 °C annealing

Chemical Type	Film Thickness (nm)	Initial Stress (MPa)	Stress after 30 min 600 °C annealing (MPa)	Stress after 30 min 900 °C annealing (MPa)
20B	234	145	1	- 112
400F	488	87	83	-21
500F	496	152	117	-87

5.3 Ion Implantation

Ion implantation is a process of accelerating material ions under electrostatic forces, and impinging on the target material. The ions are accelerated to a high energy, and the collision with target material will change the target material both chemically and physically by transferring momentum and energy. The ion implantation process has been shown to change silicon oxide film stress by changing overall density, damaging co-covalent bonds, and causing plastic deformation [48, 49]. Volkert and Polman demonstrated stress changing of silicon oxide films from compressive to tensile by implanting 150 keV Si ions to a 510 nm thick thermal oxide film. The initial compressive stress first reduces in magnitude as the film being densified by Si ions, then becomes tensile. After reaching a maximum tensile stress, with increasing irradiation doses, the stress decreases in magnitude and eventually saturates around neutral stress [49].

The ion implantation approach is promising in obtaining tensile stressed oxide film. It can eliminate the tedious process of deposition/annealing process in TEOS PECVD oxide. However,

some challenges remain unknown. The ion concentration follows a Gaussian distribution along the depth of the target film, which means uneven stress distribution along the depth of the film. The energy level has to be carefully selected to avoid implantation through the oxide film into the silicon substrate, causing lattice damage in the device layer.

Chapter 6

Summary and Future Work Recommendation

The development of CAT grating fabrication technology is critical for enabling next generation space x-ray spectrometers and accumulates valuable nano/micro fabrication knowledge and insight. From the simple goal of solving the thin silicon grating bar buckling problem, a complete solution of fabricating SOI wafers with tensile stressed buried oxide was developed. Key components of the work include dual-frequency TEOS PECVD deposition, stress behavior after furnace annealing, pre-bonding surface preparation, and wafer fusion bonding. Two major challenges along this study were stress change caused by vapor absorption and film cracking caused by extreme high tensile stress. A thin protective layer of low frequency plasma-deposited oxide can prevent water absorption. The film crack mechanism was modeled by strain energy release theory, and the theoretical estimated maximum thickness without cracks is consistent with experimental results, 632 ± 246 nm. The bonding conditions were studied and the final bonded samples were evaluated by the double cantilever beam model.

Inconclusive results from other approaches to obtain tensile stressed oxide were also presented, including spin-on-glass of HSQ/MSQ and ion implantation. The initial experiments of spin-on-glass approach failed to keep a tensile stress after high temperature annealing, however, with

different precursor, the stress annealing behavior can vary in a large range. From literature, the most promising precursor Fox-25 was not studied due to the long lead time in ordering it.

A completely different approach to solve the buckling challenge is processing with thick silicon grating bars for stronger structural robustness. After all the high risk processes, we then reduce the grating membrane's thickness to boost efficiency, in a controlled and low damage manner. Experiments of thermal oxidation followed by vapor hydrofluoric acid etch were conducted and provided positive results to further explore this approach.

In summary, this new technology of tensile stressed oxide film that can withstand high temperature (~900 °C) could enable a wide variety of applications that are not possible previously due to limitations from buckling caused by compressive stress. The major disadvantage is high labor intensity involved with the process, with iterative deposition and time consuming furnace annealing. For future work, more effort should be invested into reducing the cost and labor involved in the process, including study of faster processes such as spin-on-glass and ion implantation.

Appendix A

Recipe for Fabricating SOI Wafers from TEOS Oxide

Start with <100> 4 inch silicon substrates, <110> 4 inch silicon wafers for device layer.

1. In ICL, standard procedure, piranha clean, rinse and dry wafers

2. In ICL, Oxford 100 Plasmalab deposition chamber, select recipe TEOS LF, change the deposition time by dividing the desired LF thickness by LF deposition rate (20 – 27 nm /min).

3. In ICL, Oxford 100 Plasmalab deposition chamber, select recipe TEOS HF, select deposition time with a maximum of 15 min, deposition rate (22- 34 nm / min).

4. In TRL, furnace tube A4 (green) or B1 (red), flow 60% oxygen, load the wafers into the furnace tube with a quartz boat, anneal the wafers at 700 °C for 30 min.

5. Repeat step 3 & 4, until the HF deposited oxide thickness reaches the desired value.

6. In ICL, Oxford 100 Plasmalab deposition chamber, select recipe TEOS LF, change the deposition time by dividing the desired LF thickness by LF deposition rate (20-27 nm/min).

7. In ICL, tool GnP CMP polish, select DI wafer for conditioning for 300 sec, load the wafer, go into auto mode select recipe auto 1, select 4 inch wafer and hit start. Alternatively, wafers can be sent to Entrepix for professional CMP services.

8. In TRL, standard procedure, RCA clean, rinse and dry wafers.

9. In TRL, tool Electronic Visions EV450 and AB1-PV bonder, load the substrates with the CMP polished oxide film, and the <110> silicon wafers, bond at 400 °C.

10. In TRL, tube Au B1, load the substrates into the furnace, flow 60% oxygen, anneal the samples for 5 hours at 750 °C, or 6 hours at 700 °C.

11. CMP polish the device layer to 4 μm, either in ICL GnP CMP tool.

12. In TRL, STS-CVD tool or in ICL Oxford 100 (if it allows red wafer), PECVD silane based oxide, 4 μm on the back of the bonded wafer, 300 nm on the front side of the device layer.

Note: After step 6, the extensive CMP and bonding work requires large amount of labor, working with fragile equipment and samples. The work after step 6 can be outsourced to professional wafer manufacturer Ultrasil Corporation.

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