Quantum Capacitance Measurements of Single-Layer Molybdenum Disulfide

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by

Alina Kononov

Submitted to the Department of Physics
in partial fulfillment of the requirements for the degree of

Bachelor of Science in Physics

at the

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Abstract

Through this thesis, heterostructures composed of a thin layer of hexagonal boron nitride atop a monolayer of molybdenum disulfide were fabricated with the goal of measuring quantum capacitance and probing the transition metal dichalcogenide's density of states. In the final devices, no modulation of the quantum capacitance was observed due to large Schottky barriers between the metal contacts and the molybdenum disulfide. Lessons learned from this investigation inform improved fabrication and measurement techniques for future iterations of these fascinating devices.

Thesis Supervisor: Raymond Ashoori
Title: Professor

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Acknowledgments

I am greatly indebted to Benjamin Hunt and Professor Raymond Ashoori, my wonderful thesis supervisors, for their unswerving guidance, unlimited patience, and invaluable assistance. I would also like to thank Professor Pablo Jarillo-Herrero, my academic advisor, as well his entire research group, particularly Javier Sanchez-Yamagishi, Hugh Churchill, and Joel I-Jan Wang, for allowing me to use their fabrication facilities and instructing me in doing so. None of my work could be possible without the vast resources and generous support of the MIT Physics Department and the MIT UROP Office.

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Chapter 1

Introduction and Background

1.1 Two Dimensional Crystals

Until recently, two dimensional electron systems (2DESs) have always been confined within the bulk of a three dimensional heterostructure, at the junction of two different materials. In the inversion mode of the common metal-oxide-semiconductor field-effect transistor (MOSFET), a 2DES forms at the interface of the semiconductor (typically silicon) and the oxide (typically silicon dioxide). The 2DES in heterojunctions of III-V compounds (such as at the interface of GaAs and AlGaAs in a modulated-doping field effect transistor) has also been extensively studied.[5]

Many three dimensional crystals have a layered structure with strong covalent bonds within a layer and weak van der Waals bonds between layers. This property was first exploited for the isolation of graphene from graphite in 2004.[12] Since then, the ability to isolate two dimensional crystals has allowed enormous advances in the study of semiconductors, transition metal dichalcogenides, and other interesting materials with the potential for developing novel electronic devices.

In addition to studying individual materials, layers of different crystals can be isolated and rearranged to form micro-scale van der Waals heterostructures, which vastly expand the range of measurable physical phenomena. A technique for controlled transfer of one flake onto another was first invented in 2010 in order to support graphene on hexagonal boron nitride (hBN), which provides a flatter and more chem-

ically inert surface than the usual silicon dioxide (SiO_2) substrate.[6] The breadth of available materials with different properties makes it possible to engineer very specific devices. This experiment focused on fabricating tiny capacitors for the purpose of investigating the density of states of monolayer molybdenum disulfide (MoS_2).

Low dimensional materials, particularly two dimensional crystals like monolayer MoS_2, exhibit such interesting physical phenomena because of their low density of states. Due to high in-plane conductivity, many two dimensional crystals can be modelled as a two-dimensional electron gas (2DEG), where electrons are tightly confined to a plane but move freely within it.

1.2 Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDCs) are materials with chemical formula AB_2, where A is a transition metal and B is a chalcogen such as sulfur, selenium, or tellurium. The crystals consist of atomic trilayers with a layer of the transition metal between two layers of chalcogen.[3] Strong covalent bonds within the trilayer and weak van der Waals bonds between the trilayers allow isolation and investigation of the trilayer unit.

Figure 1-1 depicts the crystal structure of molybdenum disulfide (MoS_2), the material studied in this experiment. Both the Mo and S planes are arranged in hexagonal lattices, comprising a trigonal prismatic structure.[9] Bulk MoS_2 has an indirect band gap of 1.29eV, but monolayer MoS_2 has a direct band gap of 1.88eV.[9]

TMDCs are endowed with mechanical flexibility and high charge carrier mobility,[3] [13] which in addition to novel and exciting physical phenomena, could lead to applications in field effect transistors for flexible electronics.[13] Ab initio calculations predict large Van Hove singularities in TMDCs' density of states that would cause high photon absorption rates, making the material a promising candidate for efficient photovoltaics.[4] Figure 1-2 depicts these predictions, which are supported by measurements of the quantum efficiency of photoresponsive graphene-TMDC heterostructures.[4]. This experiment sought to measure the density of states

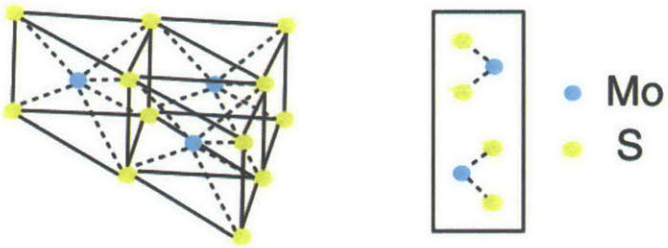

Figure 1-1: Crystal structure of MoS_2, adapted from [9]. Molybdenum atoms are shown in blue and sulfur atoms are shown in yellow. The left diagram depicts the within a single trilayer, while the right diagram depicts the arrangement of two adjacent trilayers.

of MoS_2 empirically.

1.3 Quantum Capacitance and Density of States

Classical parallel-plate capacitors are governed by the well-known equation $Q = CV$; that is, the charge on the plates is proportional to the voltage across the capacitor, and capacitance is defined as the constant of proportionality in this relationship. Classically, capacitance only depends on geometric properties of the plates and the electrical permittivity of the material in between ($C = \epsilon A/d$), but not on the material properties of the plates themselves. This classical capacitance is therefore referred to as geometric capacitance C_{geom}.

If N is the number of charges on each plate, we can use $Q = Ne$ to obtain the differential energy dE_{class}/dN required to move more electrons from the positive plate to the negative plate:

$$\frac{dE_{\text{class}}}{dN} = e\frac{dV}{dN} = \frac{e^2}{C_{\text{geom}}}$$

However, in a low dimensional material with a low density of states, adding electrons to the system costs an extra quantum energy.[8] The Pauli exclusion principle dictates that no two electrons can occupy the same quantum mechanical state, so when all of the given states within an energy level have been filled, another electron can only be added into a higher energy state. Thus, in a system with a low density of

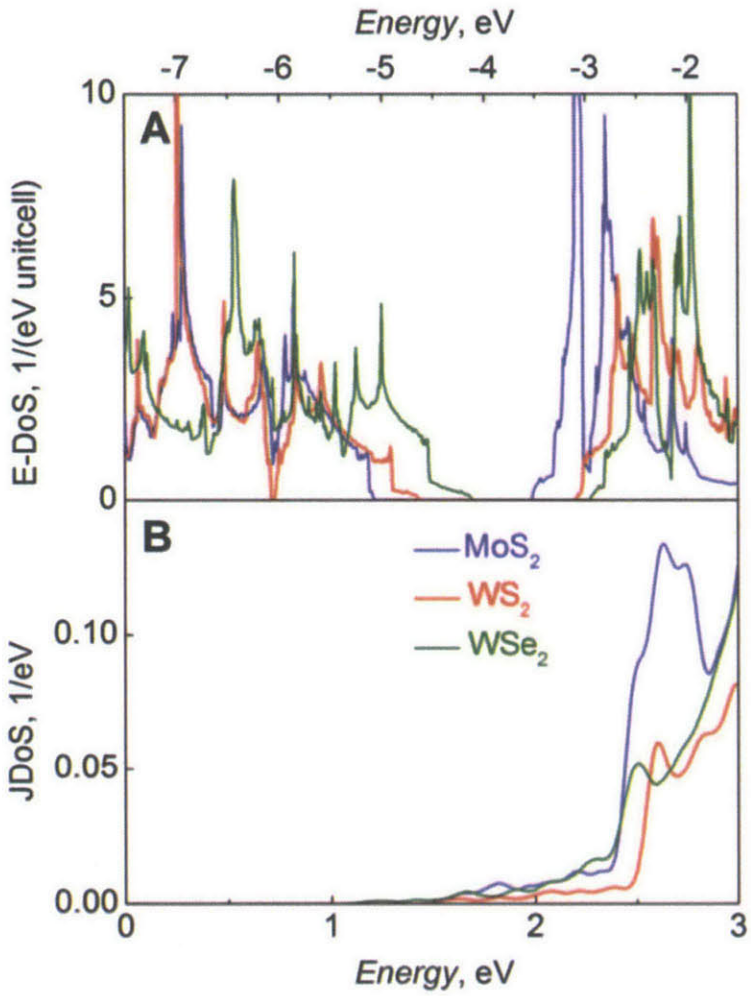

Figure 1-2: Predicted electron density of states (top) and joint density of states (bottom) of several TMDCs, adapted from [4].

states, adding electrons to the system costs an additional differential quantum energy $dE_{\text{quant}}/dN = d\mu/dN$, where $\mu(N)$ is the chemical potential. The total differential energy for adding electrons to the system is then:

$$\frac{dE_{\text{tot}}}{dN} = \frac{dE\text{class}}{dN} + \frac{dE\text{quant}}{dN} = \frac{e^2}{C_{\text{geom}}} + \frac{d\mu}{dN}$$

The corresponding total capacitance is given by

$$\frac{1}{C_{\text{tot}}} = \frac{1}{C_{\text{geom}}} + \frac{1}{e^2}\frac{d\mu}{dN}$$

We thus define the quantum capacitance as

$$\frac{1}{C_{\text{quant}}} = \frac{1}{e^2}\frac{d\mu}{dN}$$

The density of states is

$$\frac{dn}{d\mu} = \frac{1}{A}\frac{dN}{d\mu}$$

where A is the area of the capacitor plate, so

$$C_{\text{quant}} = e^2 A \frac{dn}{d\mu} \tag{1.1}$$

Since the quantum capacitance is proportional to the density of states, our quantum capacitance measurements directly probe the material's density of states.

Chapter 2

Apparatus

2.1 TMDC-hBN heterostructure

A schematic of the target device is shown in Figure 2-1. A heterostructure consisting of monolayer MoS_2 and 5-10nm thick hexagonal boron nitride (hBN) lies on a substrate of insulating silicon. hBN is an insulating, large-band gap material that tends to preserve the qualities of materials it is combined with.[6] Gold contacts on the exposed regions of MoS_2 and the hBN allow for the sensitive capacitance measurements that are explained in Section 2.4. The structure forms a capacitor where the MoS_2 and the top gold contact serve as the conductors and the hBN serves as the dielectric. The silicon chip containing the device is affixed to a chip carrier, with wire bonds connecting the gold contacts on the device to the pins of the chip carrier. The device is fabricated according to the methods described in Section 3.1.

2.2 Capacitance Bridge-on-a-chip

We use a custom-built capacitance bridge to measure the capacitance of nanoscale objects such as the heterostructures described in this thesis. This "bridge-on-a-chip" was first used to measure the capacitance of single quantum dots[2][1] and is described in detail in [15].

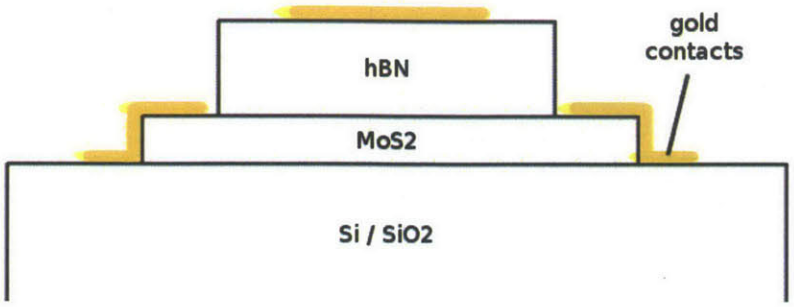

Figure 2-1: The target device consists of a thin flake of hBN atop a monolayer flake of MoS_2 on a substrate of insulating, oxidized silicon. Gold contacts to either side of the exposed MoS_2 and to the hBN gate allow the application and detection of electrical signals in the device.

The bridge-on-a-chip is also held on the chip carrier containing the MoS_2-hBN heterostructure. It contains two commercial devices – the FHX35X high electron mobility transistor (HEMT) [7] and the 150MΩ Sichrome MSHR series thin film resistor[11] – as well as a fabricated standard capacitor. The functions of these components are discussed in Section 2.4, while the procedure for fabricating the transistor circuit is described in Section 3.1.6.

2.3 Refrigerator and Probe Setup

A liquid helium dewar was used to achieve temperatures as low as 4°K. A probe consisting of a steel tube with a titanium insert holds the chip carrier containing the sample and transistor circuit on a stage at its bottom. Titanium is used for the insert because of its non-magnetic and elastic properties. The probe can be raised or lowered to adjust the sample's position along the temperature gradient in the dewar neck. Wires running up the length of the tube inside of the probe connect the chip carrier pins to a breakout box, which allows further electrical connections through coaxial cables.

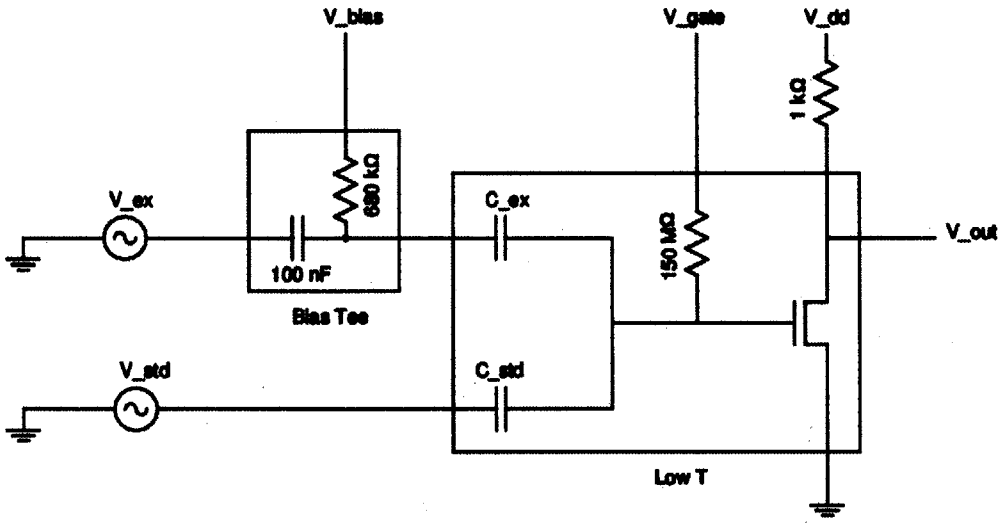

Figure 2-2: Schematic of the apparatus circuitry.

2.4 Circuitry and Signal Chain

A circuit diagram of the capacitance bridge is shown in Figure 2-2. The MoS_2-hBN heterostructure is modelled as the capacitor C_{ex}, with the MoS_2 as the left plate and the hBN gate contact as the right plate. The experimental device capacitance is measured relative to the standard capacitance C_{std} (typically around 100fF) by applying two AC excitations V_{ex} and V_{std} with equal frequencies and amplitudes on the order of 100μV. The amplitude and phase of V_{std} is adjusted to "balance" the circuit – that is, find V_{std} such that the AC voltage V_{bal} at the "balance point" between the two capacitors is zero.

If Z_{std} and Z_{ex} represent the impedances of the standard and experimental capacitors, then V_{bal} is given by

$$V_{bal} = V_{ex}\frac{Z_{std}}{Z_{std} + Z_{ex}} - V_{std}\frac{Z_{ex}}{Z_{std} + Z_{ex}} \tag{2.1}$$

When the circuit is balanced (that is, $V_{\text{bal}} = 0$), we have $V_{\text{ex}} Z_{\text{std}} = V_{\text{std}} Z_{\text{ex}}$ and therefore

$$\frac{C_{\text{ex}}}{C_{\text{std}}} = \frac{V_{\text{std}}}{V_{\text{ex}}} \tag{2.2}$$

Thus, C_{ex} can be determined relative to C_{std} by taking the ratio of the AC excitations that balance the circuit.

The transistor acts as a low-temperature amplifier with a typical gain of about two, allowing higher resolution balancing. It also serves as an impedance transformer: the cable capacitance of a coaxial cable attached to the balance point would degrade the measured signal by a factor of $C_{\text{ex}}/C_{\text{cable}}$. Including the HEMT transforms the capacitance to ground from $C_{\text{cable}} = 200\text{pF}$ to $C_{\text{HEMT}} = 2\text{fF}$. Two DC voltage sources V_{gate} and V_{dd} bias the transistor gate and drain, respectively. V_{gate} and V_{dd} are calibrated according to the methods in Section 3.2.1 to find an optimal operating point in a linear regime with a large gain. The $150\text{M}\Omega$ resistor forces the high frequency current from the balance point to pass through the transistor gate instead of being absorbed by V_{gate}.

Thus, small oscillations in V_{bal} are amplified by the transistor and detected in V_{out}. A lock-in amplifier compares the output signal with a reference signal (which is equal to V_{ex}), extracting the amplitude and phase of the desired frequency component of V_{out}, which may be much smaller than the surrounding noise. This amplitude and phase information is communicated to a computer controlling the voltage source through a shell script. Details of the balancing procedure are discussed in Section 3.3.

A bias tee composed of a 100nF capacitor and $680\text{k}\Omega$ resistor biases the MoS_2 with a DC voltage V_{bias}, altering the material's Fermi energy, density of states and hence C_{ex}. The goal is to measure C_{ex} as a function of V_{bias}, thereby extracting information about the quantum capacitance and density of states of MoS_2.

The electrical instruments used in this experiment included a home-built 24-bit 8-channel DC voltage source, Perkin Elmer 7280 DSP lock-in amplifier, and two frequency locked AC voltage sources. To reduce noise, all of the equipment is plugged

into a power line isolated from the building power, and an optoisolator (National Instruments GPIB 120-A) shields the experimental circuitry from computer noise.

Chapter 3

Methodology

3.1 Fabrication

3.1.1 Exfoliation and Optical Mapping of MoS_2

Monolayer MoS_2 flakes were exfoliated onto substrates consisting of insulating, oxidized silicon chips. Silicon chips 1-2cm^2 in area are cut from a commercially bought silicon wafer using a diamond scribe. Since silicon forms a highly ordered crystal, the wafer cleaves easily and cleanly when a small scratch is made along a crystallographic direction. The chips are rinsed with acetone and isopropyl alcohol (IPA) and dried with nitrogen gas to remove possible surface contaminants. Flakes of MoS_2 are exfoliated using the mechanical cleavage method – a layer of the material is peeled from the commercially bought mother-crystal with Ultron Systems R1011 low-tack sticky tape, thinned down by repeatedly peeling off thinner layers with other pieces of sticky tape, and finally deposited onto a silicon chip. The resulting samples can be heat cleaned at 350°C in argon and hydrogen gas to remove any possible organic contaminants (such as tape residue), but this was not done for this experiment.

The resulting MoS_2 flakes are then analyzed with an optical microscope. The 300nm oxidation of the silicon maximizes optical contrast, allowing flakes of different thickness to be distinguishable by color – the thickest flakes appear bright yellow, while the thinnest flakes appear faint purple. These flake thicknesses can be further

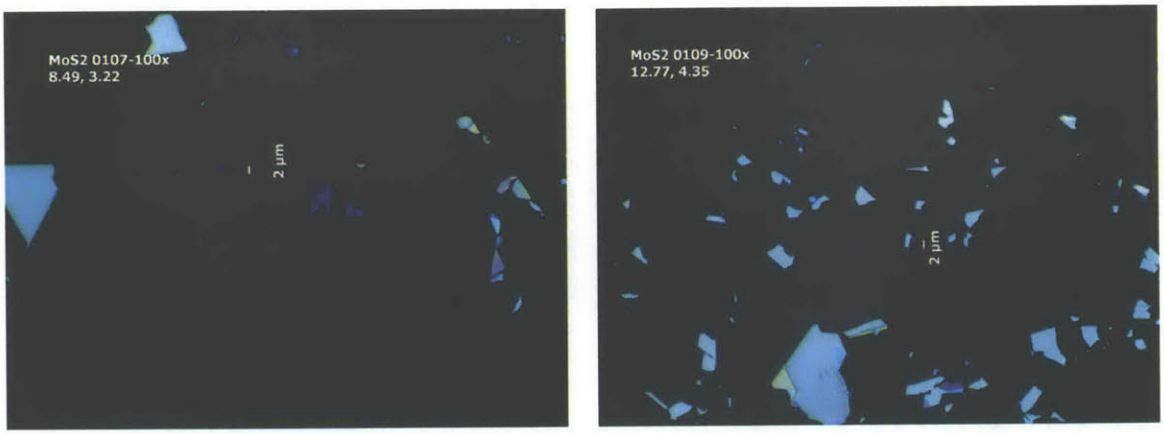

Figure 3-1: 1000x magnified optical images of the two MoS_2 flakes used in this experiment. The light purple regions about $2\mu m^2$ in area are the monolayer pieces.

confirmed by atomic force microscopy as described in Section 3.1.4. For each desirable flake, the coordinates relative to a chip corner are recorded using the digital micrometer on the microscope stage, and both 200x and 1000x magnified images are saved to assist in finding the flake again in the future.

This experiment required monolayer MoS_2 flakes large enough to leave some MoS_2 exposed on either side of the hBN after transferring (see Section 3.1.3). Since the in-plane bonds of TMDCs are fairly weak, the material tends to exfoliate into relatively small flakes a few μm in area. Thus, finding large, thin pieces of MoS_2 presented a challenge. Figure 3-1 shows optical images of the MoS_2 pieces used in this experiment.

3.1.2 Transparent Polymer Stack and Exfoliation of hBN

In order to construct a heterostructure containing two or more layers of different materials, each layer must be independently exfoliated onto a substrate and mapped with an optical microscope as described in Section 3.1.1. The upper layers must be successively transferred on top of the lowest layer.[1] To allow for flake alignment and transfer as described in Section 3.1.3, the upper layers must be exfoliated onto a transparent polymer stack that has been specially engineered for the dry transfer method. Figure 3-2 depicts the structure of the transparent polymer stack.

[1]Recently, some research has developed a technique for successively picking up lower layers,[16] but that technique was not used in this experiment.

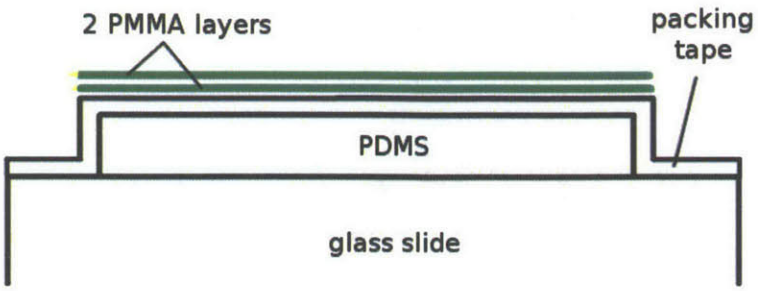

Figure 3-2: Diagram of the transparent polymer stack. Each layer is transparent, allowing the flakes to be seen through the stack under an optical microscope during transfer. A glass slide supports a 1mm layer of Sylgard 184 Silicone Elastomer (PDMS), a polymer that serves as cushioning. Transparent packing tape (Duck HD clear) provides a flatter surface and mediates adhesion for the PMMA. PMMA is a low melting point polymer, allowing it to peel off of the stack when the system is heated during the dry transfer method discussed in Section 3.1.3.

To fabricate the stack, PDMS is first prepared by mixing 11g of elastomer base with 1g curing agent (both commercially bought) in a petri dish, spreading the mixture out evenly on the petri dish, placing the dish atop a sonicator running at low power to eliminate bubbles, and curing overnight at room temperature. In a 14.5cm diameter petri dish, this recipe produces 1mm thick PDMS, but the amounts of elastomer base and curing agent may be proportionally adjusted to produce the desired thickness.[14]

To assemble the transparent polymer stack, a glass slide is cut in half with a diamond scriber and rinsed with IPA. A piece of PDMS is cut with a clean razor blade and carefully laid flat on top of the slide without leaving any bubbles at the interface. The PDMS piece must be small enough to leave a 2mm margin on all edges of the slide. This partial stack is irradiated in a UV Ozone cleaner to help the subsequent layers stick to the PDMS. A piece of transparent packing tape is laid flat on top of the PDMS, again without creating any air bubbles.

Next, 950PMMA A5 (PMMA formulated with 950,000 molecular weight resins and diluted in anisole with a 5% concentration) is spun atop the tape in two stages. The first layer is spun at 1000rpm for 70s, after which the stack is baked at 120°C for 10 minutes. The same spinning and baking procedure is repeated for the second

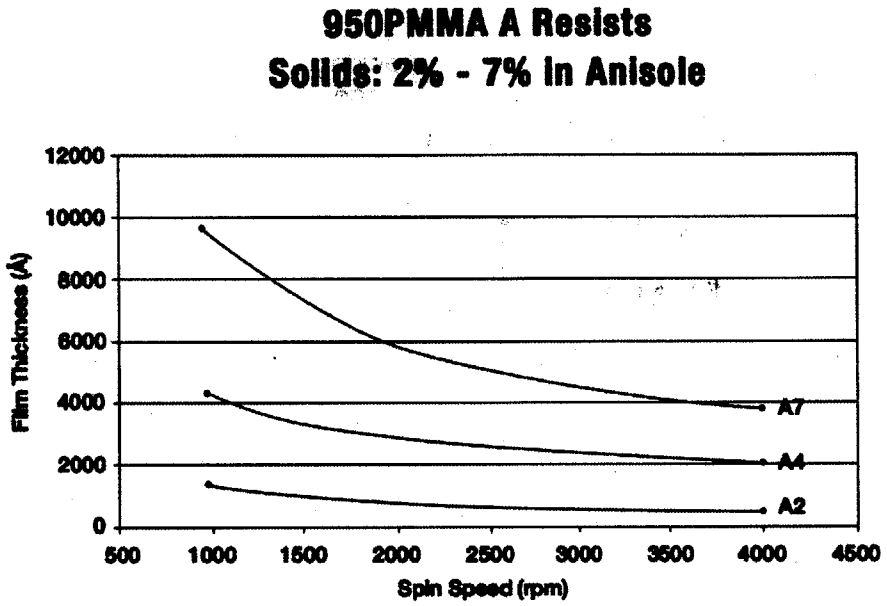

Figure 3-3: Layer thickness versus spin speed for different concentrations of 950PMMA A, adapted from [10]. Larger spin speeds produce thinner films, while larger PMMA concentrations produce thicker films. Spinning 950PMMA A5 at 1000 rpm produces a film about 700nm thick.

layer. The spin speed can be adjusted to obtain a different PMMA thickness. Figure 3-3 depicts the relationship between spin speed and layer thickness for various concentrations of 950PMMA A.

Once the stack is complete, the desired material (in this case hBN) is deposited atop the PMMA. The hBN is thinned down with low-tack tape as described in Section 3.1.1 and then slowly and gently transferred onto the PMMA. The hBN is then mapped with an optical microscope as described in Section 3.1.1. Flakes of different thicknesses are distinguishable by color in the same way, but the transparent stack provides less optical contrast, making thin pieces harder to see. Since the various polymer layers create a fairly rough surface, AFM is not useful in confirming hBN flake thicknesses until after they have been transferred onto the MoS_2. This experiment required hBN flakes that are 5-10nm thick (in order to serve as an insulator) and about 1μm wide (in order to fit on top of the very small MoS_2 flakes while leaving some MoS_2 left exposed on either side). Figure 3-4 shows optical images of the hBN

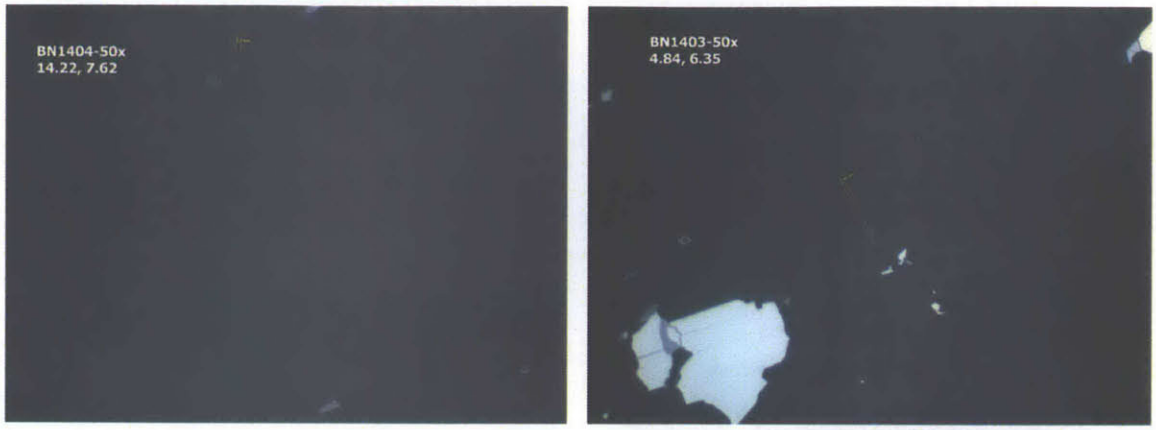

Figure 3-4: 500x magnified optical images of the two hBN flakes used in this experiment. The faint purple flakes that are about 1μm wide are the pieces used.

pieces used in this experiment.

Finally, 1mm squares containing the desirable hBN pieces are cut out of the transfer stack with a clean razor blade. Each square is placed on one end of a clean glass slide, completing preparation of the transparent polymer stack for the dry transfer method.

3.1.3 Dry Transfer of hBN onto MoS_2

Figure 3-5 shows the setup used for the dry transfer method. The transparent polymer stack holding the hBN flake is suspended upside-down above the silicon chip holding the MoS_2 flake. The two flakes can be alternately viewed in the microscope by adjusting the focus. After the flakes are carefully aligned, the hBN is slowly lowered while the alignment is further adjusted. The two surfaces are brought into contact at 35°C. They are fully in contact when interference patterns become visible and expand to cover the entire area.

Once in contact, the system is heated to 130°C, melting the PMMA layer. When the entire area has turned green, the PMMA is fully melted and the transfer arm along with the rest of the transparent polymer stack can be lifted away. Figure 3-6 displays optical images of each transfer step in progress. After the sample has cooled down to room temperature, the PMMA is rinsed off with acetone and IPA, leaving

Figure 3-5: Setup used to transfer hBN onto MoS_2. A stage containing a heating element supports the silicon chip under an optical microscope, while a vacuum keeps the chip stationary. The glass slide holding the transparent polymer stack is mounted upside-down on the transfer arm, which is supported by a magnet that allows coarse adjustments to the hBN position. Micromanipulators on the transfer arm allow fine control of the hBN position and tilt.

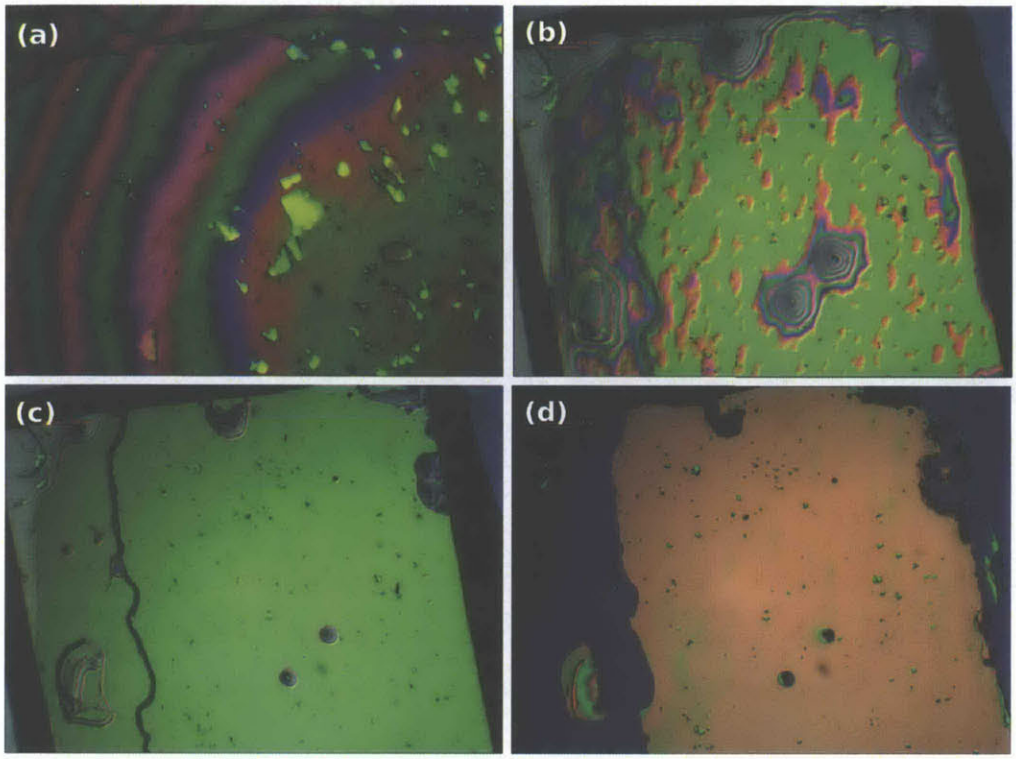

Figure 3-6: Optical images of steps in the dry transfer procedure. The flakes pictured were not used in this experiment, but the PMMA behavior shown here is typical. (a) 500x magnified image showing the onset of interference patterns. (b) 100x magnified image showing most of the transparent stack area in full contact with the silicon chip. Regions around very thick flakes still exhibit interference patterns. (c) Melted PMMA turns green and flattens out. The stripe down the left side is a tear in the PMMA. (d) Residual PMMA on the silicon chip after the rest of the transparent stack has been lifted away and the sample has cooled down.

the completed heterostructure on the silicon substrate. If desired, the sample can be heat cleaned again to remove any possible contaminants from the PMMA, but this was not done for this experiment. Figure 3-7 shows optical images of the completed heterostructures made in this experiment.

3.1.4 Atomic Force Microscopy

In atomic force microscopy (AFM), a vibrating cantilever tip scans a two-dimensional region of a sample, measuring surface heights within picometer accuracy. The technique produces clearer and more accurate visualizations, resolves smaller features,

Figure 3-7: 1000x magnified optical images of the two heterostructures made in this experiment.

and identifies layer thicknesses more accurately than optical microscopy. AFM also enables surface roughness analysis. Figures 3-8 and 3-9 display AFM images of the two devices that were successfully fabricated for this experiment along with several height profiles.

3.1.5 Electron Beam Lithography and Metal Evaporation

After the transfer is completed, electrical contacts are formed by evaporating metals over a mask. The mask is fabricated by first spinning two fresh layers of PMMA onto the sample; these serve as electron-sensitive resist for electron beam lithography. For the first layer, 495PMMA A4 is spun at 2000rpm for 60s and then baked at 180°C for 7 minutes. For the second layer, 950PMMA A2 is spun at 3000rpm for 60s and then baked at 180°C for 3 minutes. The dependences of the film thickness on spin speed and PMMA concentration are depicted in Figures 3-3 and 3-10 for 950PMMA A2 and 495PMMA A4, respectively. The 495PMMA A4 layer is about 200nm thick, while the 950PMMA A2 layer is about 700nm thick. The bottom PMMA layer is more sensitive and develops more, creating an undercut that aids lift-off after electron beam lithography.

CAD software is used to design alignment marks and contact patterns. Images taken by an optical microscope at 100x, 500x, and 1000x magnifications are inserted

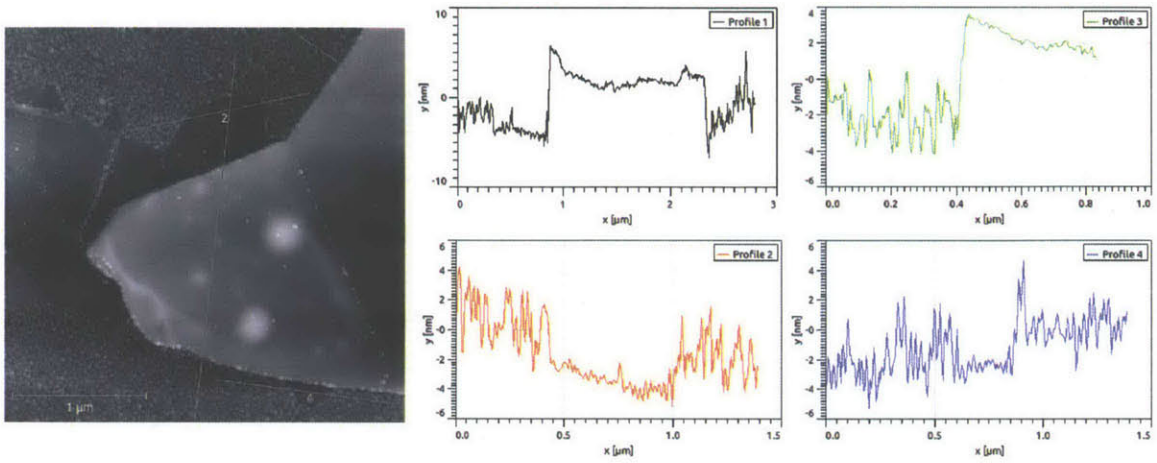

Figure 3-8: AFM image of the first MoS_2-hBN heterostructure along with several height profiles.

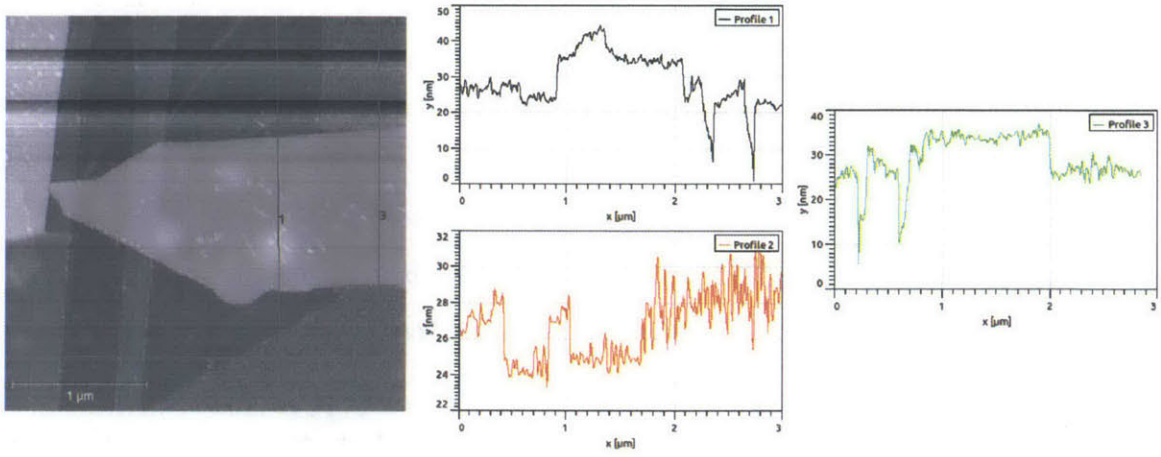

Figure 3-9: AFM image of the second MoS_2-hBN heterostructure along with several height profiles.

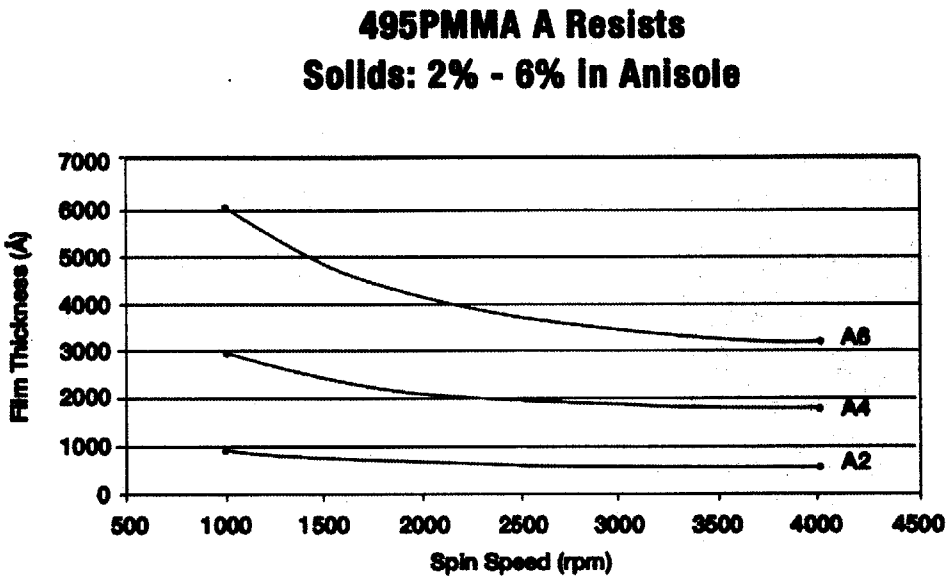

Figure 3-10: Layer thickness versus spin speed for different concentrations of 495PMMA A, adapted from [10]. Again, larger spin speeds produce thinner films, while larger PMMA concentrations produce thicker films.

and aligned within each design to provide a clear representation of each device and its surrounding area. The alignment marks are written into the mask first and are crucial for accurately aligning the contact pattern to the sample. Three coarse alignment marks that are spaced 1mm apart are used to locate three fine alignment marks that are spaced 100μm apart, which are then used to align the contact design. In each device, one contact connects to the hBN, while two contacts connect to the exposed regions of MoS_2 on either side of the hBN. Each contact connects to a large bonding pad, which is used for wire bonding as described in Section 3.1.7.

Images from the two CAD designs used in this experiment are shown in Figure 3-11. These CAD designs are converted into a run script that instructs the software controlling the electron beam in exposing the desired regions of the resist. All components of the CAD design reside in a separate layers whose designated functions are encoded in the run script.

After exposure, the mask is developed in an ice cold 1:3 water:IPA bath for two minutes, then immediately blown dry with nitrogen gas. The areas that had been

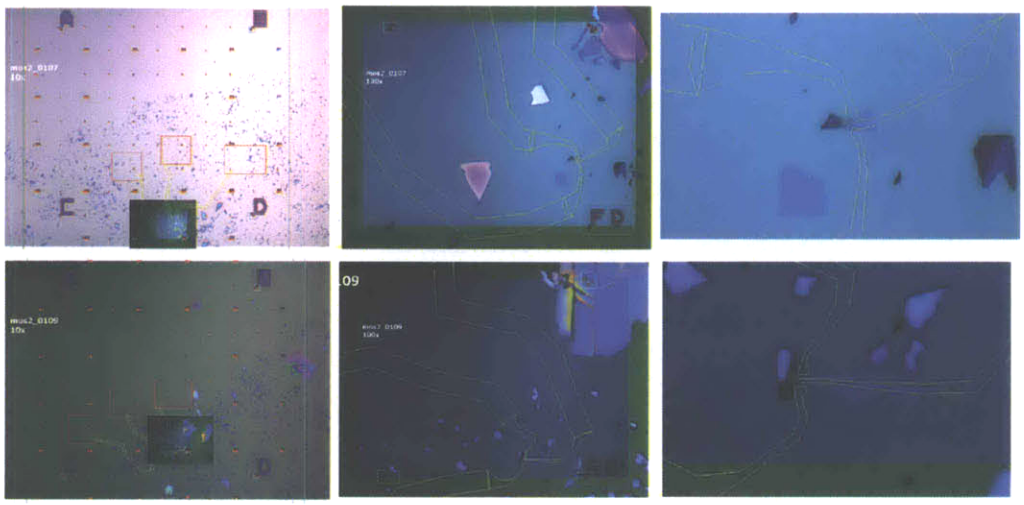

Figure 3-11: Two CAD designs used to produce electrical contacts in this experiment. Each row of images originates from one design, with images to the right showing enlarged regions around the device. In these images, the alignment marks have already been written into the mask and thus appear purple, the color of the exposed silicon. The large letters serve as coarse alignment marks, while the smaller, blocky patterns serve as fine alignment marks. Blue rectangles enclose the six alignment marks that will be used to align the design to the sample. Red rectangles outline the areas that will become bonding pads, while yellow lines outline the areas that will become contacts. The two bonding pads connecting to the MoS_2 are square-like, but the bonding pad corresponding to the hBN is elongated to make it easily distinguishable.

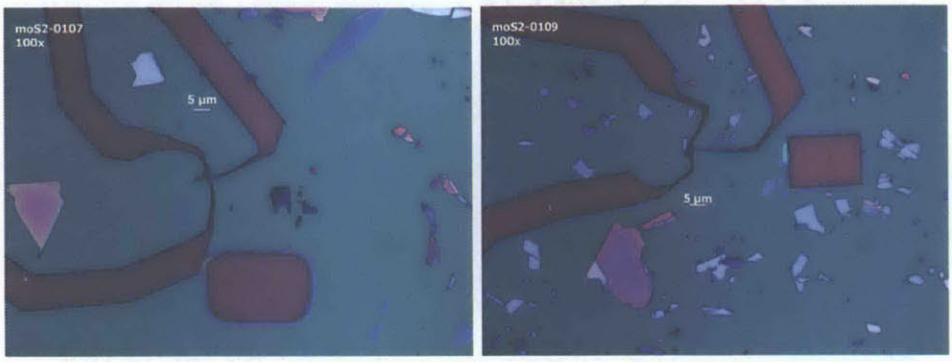

Figure 3-12: 100x magnified optical images of the two completed masks. The exposed silicon appears purple, while the PMMA resist appears blue.

exposed to the electron beam dissolve, while the rest of the PMMA remains intact. The mask is developed twice – once after the alignment marks have been written, and again after the contacts have been written. Figure 3-12 depicts the completed masks produced in this experiment.

Once the mask is complete, a thermal evaporator is used to deposit the metal contacts. A thin layer of chromium mediates the adhesion of a thicker layer of gold, which has superior low-temperature qualities. Finally, the PMMA mask and the excess metal are lifted off of the sample in an acetone bath. Heating the acetone bath can accelerate lift-off. Figure 3-13 displays the two completed samples produced in this experiment.

3.1.6 Transistor Circuit

A pre-fabricated transistor circuit was used in this experiment. Figure 3-14 shows a picture of a chip carrier holding a completed transistor circuit, which includes the HEMT, 150MΩ resistor, and standard capacitor from the circuit in Figure 2-2. These components are mounted on a structure consisting of two pieces of GaAs joined at a right angle. GaAs cleaves easily along its crystallographic directions, producing very flat edges and ensuring that the two pieces fit together well. Each piece of GaAs is covered with three gold stripes, which were evaporated onto the metal through a dedicated mask. Three drops of silver epoxy, a strong, conductive adhesive, provide

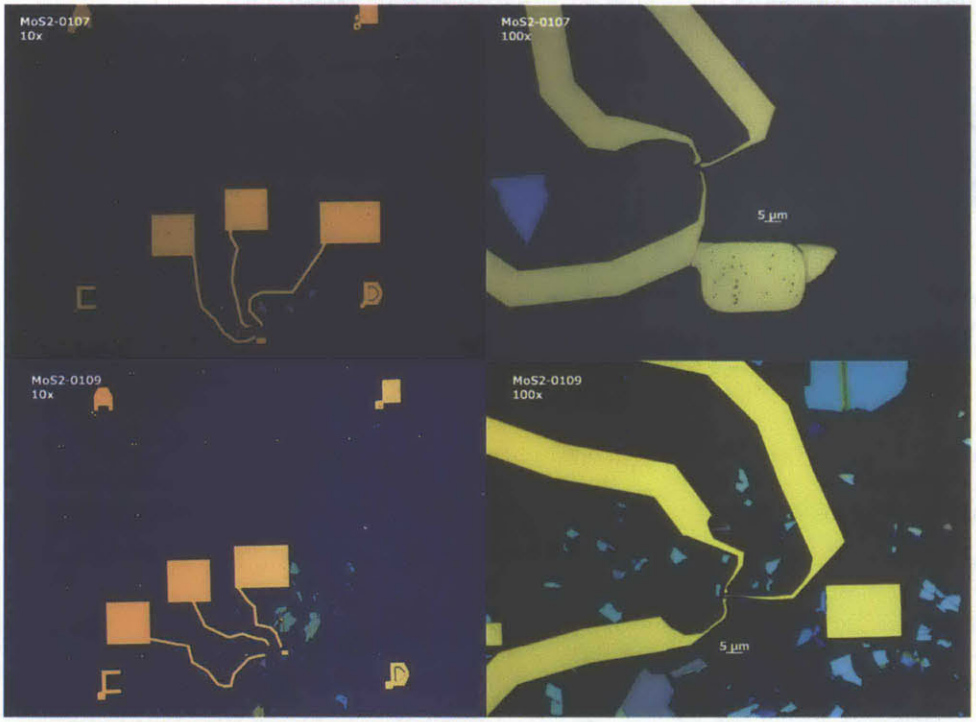

Figure 3-13: 100x and 1000x magnified optical images of two completed samples. The large gold rectangles are the bonding pads.

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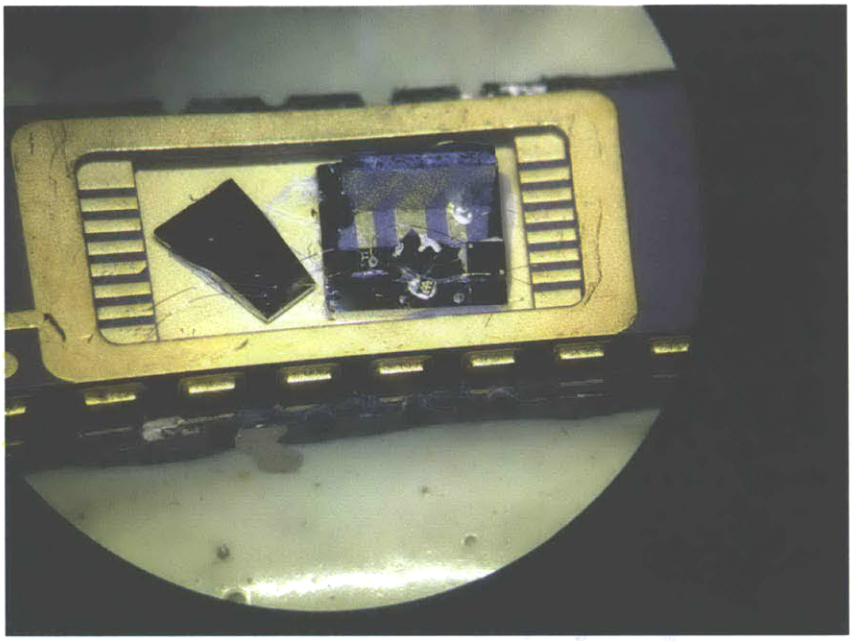

Figure 3-14: Picture of the chip carrier, magnified through an optical microscope. The silicon chip containing the sample is on the left, while the transistor mount is on the right. Wire bonds form electrical connections between the bonding pads on the silicon chip, the gold stripes on the transistor mount, and the pins of the chip carrier.

both structural strength and electrical connections between the corresponding gold stripes of the two pieces of GaAs.

The transistor and resistor are affixed to the GaAs structure with silver paste, a medium-strength adhesive. The resistor is mounted on the horizontal piece of GaAs, while the transistor is mounted on the vertical piece.[2]

The standard capacitor is formed making a scratch across one of the gold stripes. The capacitive coupling between the two sides of the gold stripe is comparable to the typical capacitances of heterostructures similar to the ones used in this experiment, making it ideal for use as the standard capacitor. The standard capacitance is determined empirically according to the procedure described in Section 3.2.2.

[2]In experiments employing a vertical magnetic field, this orientation keeps the magnetic field in the plane of the transistor even as the chip carrier is rotated to subject the sample to an angled magnetic field. The precaution is necessary because the transistor's operation is sensitive to out-of-plane magnetic fields. However, this experiment did not involve magnetic fields.

3.1.7 Circuit Assembly and Wire Bonding

The silicon chip and transistor mount are affixed to a chip carrier using silver paste, a medium-strength adhesive. A wire bonder is used to make electrical connections between the bonding pads of the silicon chip, the gold stripes on the transistor mount, and the pins of the chip carrier, completing the circuit depicted in Figure 2-2. A magnified picture of a fully assembled chip carrier is shown in Figure 3-14.

3.2 Calibrations

Before starting to collect data on a device, several calibrations are necessary to determine the optimal operating points for the transistor bias and source frequency. Also, the experimental capacitance will always be measured relative to the standard capacitance, so the value of the standard capacitance must be determined in order to interpret any results. Finally, each MoS_2-hBN device must be tested for current leakage between the MoS_2 contacts and hBN gate, which would render the device unsuitable for quantum capacitance measurements.

3.2.1 Transistor Drain and Gate Bias

The transistor calibration serves to determine operating points for two parameters: the drain bias V_{dd} and the gate bias V_{gate}. To find the optimal values, V_{out} is measured while V_{gate} is swept from -0.4V to -0.1V and V_{dd} is held at a constant voltage. The resulting data, characteristic of a transistor, is plotted in Figure 3-15 for six different values of V_{dd} ranging from 0.1V to 0.6V.

Since the transistor is to be used as an amplifier, the operating point should have a large, stable gain (defined as $|dV_{out}/dV_{gate}|$). Values of V_{dd} between 0.4V and 0.6V produce unstable outputs, but V_{dd}=0.3V is stable. Furthermore, V_{gate} must be chosen to produce a linear response (constant gain), which occurs around -0.27V. Thus, V_{dd}=0.3V and V_{gate}=-0.27V is a suitable operating point for the transistor used in this experiment.

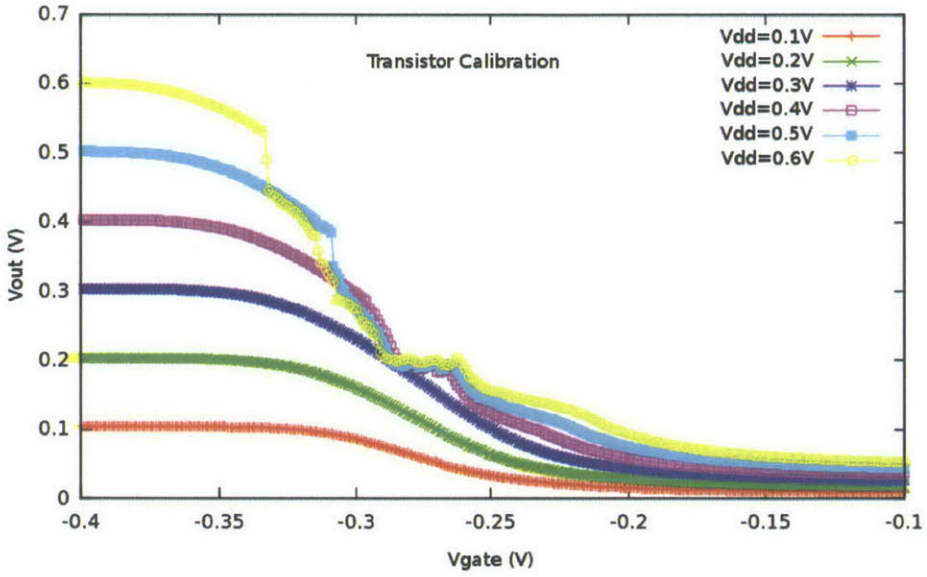

Figure 3-15: V_{out} versus V_{gate} for V_{dd} between 0.1V and 0.6V. All measurements were performed at room temperature.

3.2.2 Standard Capacitor

To determine the standard capacitance, the standard capacitor is balanced against the 150MΩ resistor in the set-up depicted in Figure 3-16. The standard capacitor, 150MΩ resistor, and the transistor are all contained in the transistor circuit as before. The 10MΩ resistor and the 1μF capacitor form a bias tee that allows the application of both the DC bias V_{gate} and the AC excitation V_{std}.

The balance measurement is largely equivalent to what is described in Section 2.4. Since no current can flow into the transistor gate, V_{ex} and V_{std} must balance as follows:

$$\frac{V_{ex}}{Z_{ex}} = \frac{V_{std}}{Z_{std}}$$

$$\frac{V_{ex}}{\frac{1}{i\omega C_{std}}} = \frac{V_{std}}{R_{bias}}$$

We can then find C_{std} in terms of R_{bias}:

$$C_{std} = \frac{1}{i\omega R_{bias}} \frac{V_{std}}{V_{ex}} = \frac{1}{i2\pi f R_{bias}} \frac{V_{std}}{V_{ex}}$$

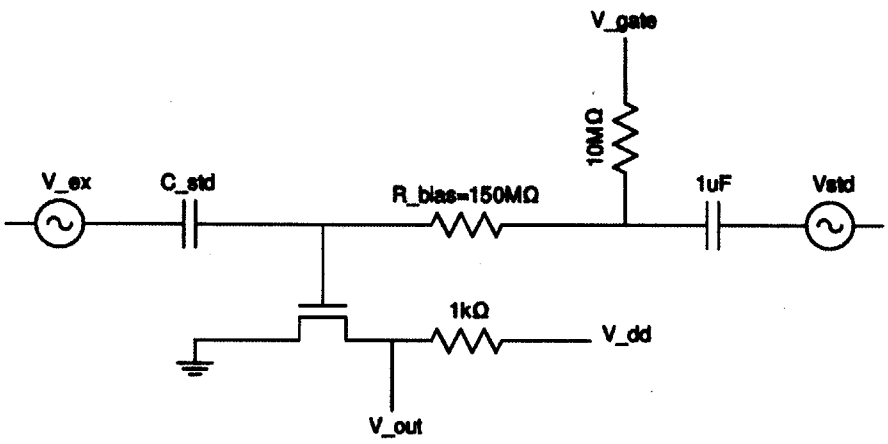

Figure 3-16: Circuit diagram of the set-up used to measure the standard capacitance.

As explained in Section 2.4, the balance measurement records $V_{\text{std}}/V_{\text{ex}}$. The imaginary component of the voltage ratio varies linearly with f, and C_{std} can be determined from the slope of the relationship. The real component, on the other hand, would correspond to a resistance inherent to C_{std} and should be zero.[3]

3.2.3 Leakage Test

A leakage test investigates a device's ability to function as a capacitor by checking whether charge is able to leak between the gate hBN contact and either of the MoS_2 contacts. It also determines an upper bound for the bias voltage – above some breakdown bias voltage, the hBN no longer behaves as an insulator, instead allowing current to pass through.

For each of the three breakout pins connected to the device, a Keithley 2400 Source Meter is used to simultaneously apply a voltage and measure the current on the pin while the other two pins are either grounded or left floating. The leakage current is measured for a voltage sweep between -4V and 4V. For an ideal device, the leakage current would be constantly 0, but many devices exhibit some leakage at higher voltages. The results of the leakage test are presented in Section 4.1.

[3]For larger f, the real component actually rises above zero because the self-capacitance of R_{bias} becomes appreciable. The measurement thus only works for small f.

3.2.4 Operating Frequency

An operating frequency must be carefully chosen to lie within the bounds of the device's physical properties and the measurement technique's capabilities. A frequency that is too high would have difficulty propagating through the device, which would behave as a series of capacitors separated by so-called spreading resistances instead of as a single capacitor. Thus, the operating frequency is bounded above by the device physics that we are interested in measuring. On the other hand, a frequency that is too low will cause some of the signal from the balance point to leak through the 150MΩ resistor instead of flowing into the HEMT gate, yielding a low signal to noise ratio. Thus, it is desirable to choose an operating frequency that is as high as possible without disrupting the device physics.

To do so, we fix the bias voltage at 0 and sweep the frequency between 1.5×10^6Hz and 1.5×10^1Hz on a log scale. At each frequency value, a computer script balances the experimental and standard capacitors via the method described in 2.4. The results of this measurement are presented in Section ??.

3.3 Measurements

Once all of the calibrations are complete, the circuit is ready for the quantum capacitance measurements described in Section 2.4. In order to determine the values of amplitude and phase for which V_{std} balances the circuit, two arbitrary values $V_{\text{std},1}$ and $V_{\text{std},2}$ are applied and the resulting values of $V_{\text{out},1}$ and $V_{\text{out},2}$ are measured. Since V_{out} is proportional to V_{bal}, Equation 2.1 implies that

$$V_{\text{out}} = MV_{\text{std}} + B \tag{3.1}$$

where M and B are complex scalars. Thus, substituting the off-balance points $(V_{\text{std},1}, V_{\text{out},1})$ and $(V_{\text{std},2}, V_{\text{out},2})$ into Equation 3.1 allows solving for M and B and consequently finding the V_{std} that produces $V_{\text{out}} = 0$, balancing the circuit. Equation 2.2 is then used to derive C_{ex}, which is proportional to the MoS_2 density of states via

Equation 1.1.

To vary the energy level of electrons in the MoS_2, bias voltage is swept from -7V to 7V, balancing the circuit to derive C_{ex} at each value of V_{bias}. Section 4.3 discusses the results of these measurements.

Chapter 4

Results

4.1 Leakage Test

Both of the devices fabricated for this experiment exhibited charge leakage, but the leakage behavior is asymmetric and unexpected. Figures 4-1 and 4-2 plot different leakage test results for different setups on the same device. Pins 2 and 14 correspond to the MoS_2 contacts, while pin 16 represents the gate hBN contact. As expected, there is no leakage when pin 16 is left floating (there would be nowhere for the leaked current to flow), but there is exponential leakage when voltage is applied to pin 14 and pin 16 is grounded. On the other hand, the leakage when the leads are switched (voltage applied to pin 16 and the other pins grounded) is negligible. Furthermore, the leakage from pin 2 to pin 16 is two orders of magnitude smaller than the leakage from pin 14 to pin 16. Possible explanations for this behavior are explained in Chapter 5.

4.2 Frequency Sweep

Figure 4-3 shows the results of a typical frequency sweep for the devices used in this experiment. The experimental capacitance was measured at zero bias for a wide range of frequencies and began to fall off in magnitude for frequencies greater than 2×10^5Hz. A frequency of about 1×10^4Hz, well within the range of acceptable

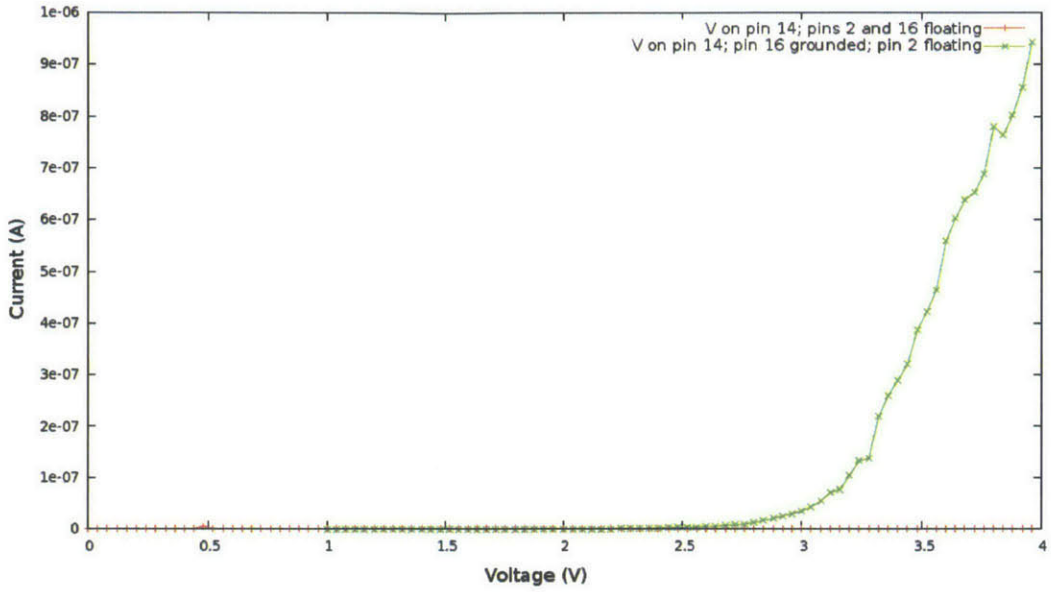

Figure 4-1: Leakage test performed between pins 14 and 16 at room temperature.

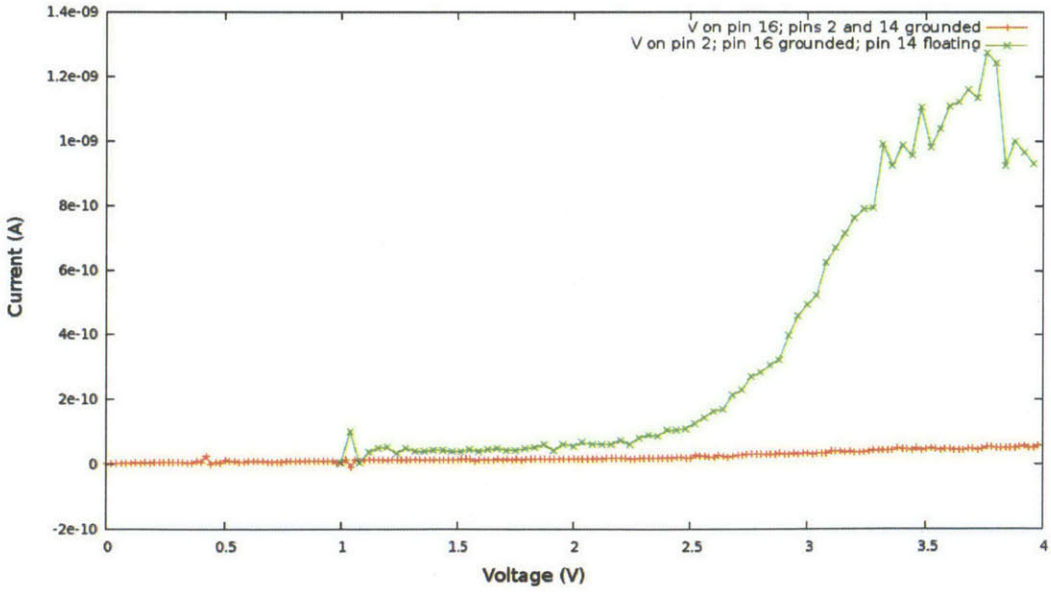

Figure 4-2: Leakage test performed between pins 2 and 16 at room temperature.

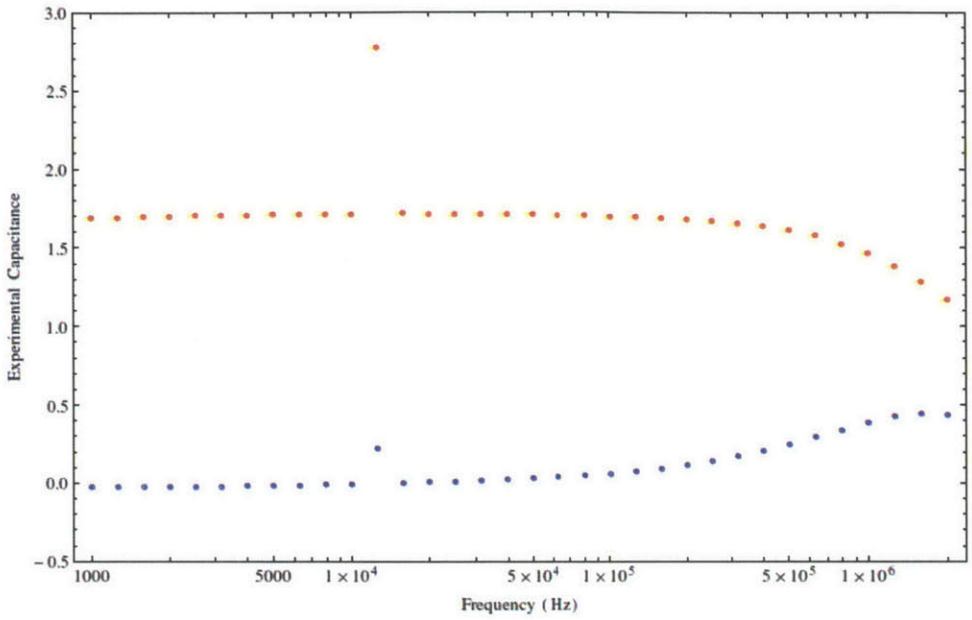

Figure 4-3: The results of a typical frequency calibration. The red points plot the experimental capacitance (real component), while the blue points plot the experimental resistance (imaginary component). The units of on the vertical axis are capacitance relative to the standard capacitance, which is about 100fF.

frequencies, was used in our measurements.

4.3 Capacitance Measurements

As described in Section 3.3, V_{bias} was swept from -7V to 7V at low temperature. No modulation in C_{ex} was observed in this range of V_{bias}; C_{ex} remained constant at a value of about $1C_{\text{std}}$. Possible explanations for this behavior are discussed in Chapter 5.

Chapter 5

Conclusions and Future Work

We postulate that no modulation of C_{ex} was observed as V_{bias} was varied because of a large Schottky barrier between the metal contacts and the MoS_2. Near a metal-semiconductor junction, the electronic bands of the semiconductor bend upwards, causing the Fermi level of the metal to fall within the band gap and creating a barrier that prevents electron conduction.[5] Although the MoS_2-hBN devices used did not produce interesting MoS_2 capacitance measurements, they do provide insights into improved fabrication and measurement techniques for future MoS_2-hBN capacitance devices.

In order to overcome the Schottky barrier, future experiments may measure capacitance while applying a large bias between the two MoS_2 contacts, allowing the sample to be charged through one side. Furthermore, the Fermi level could be raised into the conduction band of the semiconductor by vacuum annealing the sample, doping it with electrons and reducing Schottky behavior.[3]

In addition, several fabrication techniques may be improved to reduce sample charge leakage. First, the MoS_2 and hBN flakes used were extremely small, only 1-2μm^2 in area. This made small features difficult to resolve, making the devices especially sensitive to any small misalignments during transfer and contact writing. Larger flakes, whether produced by mechanical cleavage, chemical growth deposition, or other technique, would improve fabrication accuracy and increase device success rate.

Also, the risk of contamination was present during all steps of device fabrication and measurement. To mitigate this, samples were always handled with tweezers, gloves were always worn while handling samples, and samples were stored in a covered chip carrier inside a desiccator. The samples could have been more thoroughly cleaned by annealing in argon and hydrogen gases.

While this experiment focused primarily on MoS_2, future work should investigate other transition metal dichalcogenides as well. Developing methods for obtaining larger monolayer pieces would also advance this frontier, since MoS_2 tends to exfoliate into larger pieces than other TMDCs like WSe_2.

Further investigations could also achieve temperatures as low as 2°mK with a dilution refrigerator, which takes advantage of the phase separation occurring in mixtures of helium-3 and helium-4. Colder temperatures would reveal even purer physical phenomena with less noise from temperature effects.

Finally, applying a magnetic field to the TMDC-hBN heterostructure may allow measurements of Landau levels and the quantum Hall effect. This can be done by surrounding the deepest, coldest region of the refrigerator with a solenoid. The Ashoori Group at MIT operates a dilution refrigerator with an enclosed magnet capable of producing a vertical magnetic field as high as 13.5T. A mechanism at the top of the probe used allows the stage to be rotated about a horizontal axis so that the angle of the sample relative to the magnetic field can be varied. However, any electronic component whose operation is sensitive to magnetic fields (such as the transistor used in this experiment) would need to be mounted perpendicular to the axis of rotation so the magnetic field would remain in the plane of the component even as the sample stage is rotated.

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