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Massachusetts Institute of Technology

10.7 A 120nW 18.5kHz RC Oscillator with Comparator Offset Cancellation for ±0.25% Temperature Stability

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Integrated low-frequency oscillators can replace crystal oscillators as sleep-mode timers to reduce the size and cost of wireless sensors [1]. Since the timer is one of the few continuously functioning circuits, minimizing its power consumption can greatly reduce sleep-mode power of highly duty-cycled systems. Temperature stability of the oscillator is important in order to minimize timing uncertainly and guard time for the radios, and thus maximizing sleep time. The voltage-averaging feedback method described in [2] achieves high stability in the MHz frequencies, but when scaled to the kHz range, requires very large filters. On the other extreme, gate leakage-based timers have been designed for sub-nW power consumption, but operate in the sub-Hz frequencies [3]. In the past, high accuracy RC oscillators in the kHz range have been designed with feedforward correction [1] and self-chopped operation [4]. In this work, an offset cancellation architecture achieves long-term frequency stability and temperature stability while operating at lower power.

The architecture of the proposed offset-cancelling oscillator is shown in Fig. 10.7.1. When phase $\phi=0$, a current I passes through resistor R to generate a voltage $I \cdot R$ on node V_2. At the same time, a matched current source charges capacitor C_1, such that node V_1 crosses V_2 at time RC. After t_{delay} corresponding to the delay of the comparator and subsequent buffers, ϕ changes to 1, which then resets the capacitor voltage. In addition, the role of the two comparator inputs is reversed, with V_1 being the resistor voltage and V_2 the voltage across capacitor C_2. The period of the oscillator is thus nominally $2RC+2t_{delay}$. Two separate capacitors are used in the two phases so that the delay of capacitor discharge is not included in the period. This switching scheme also cancels comparator offset. For example, if the comparator has an offset V_{os}, as shown in Fig. 10.7.2, the duration of phase $\phi=0$ increases by CV_{os}/I, however the opposite phase $\phi=1$ decreases by the same amount, thus the total period of oscillation is constant. This cancellation scheme allows significant power reduction in the oscillator by: (a) permitting low-swing oscillations since offset and temperature variations of the offsets do not proportionally affect frequency stability, (b) requiring only one comparator as opposed to two in traditional architectures, and (c) relaxing the specifications on the comparator offset, and allowing optimization of gain and bandwidth. The offset cancellation also attenuates the effect of flicker noise, improving long-term stability of the oscillator.

In this design R is chosen to be 5MΩ and C_1 and C_2 are 5pF for an RC time constant of 25μs. The charging current I is 30nA on each branch, for a swing of only 150mV. Simulations show that a 10mV offset change (~6% of the swing) affects the frequency by only 0.06% thanks the offset cancellation scheme, a 100x improvement.

Temperature stability of the oscillator is affected by the on-resistance and off-leakage of switches S_1-S_6 in addition to comparator delay variations. For example, resistance changes of 5kΩ or leakage current variations of 30pA change the oscillation frequency by 0.1%. The switch size is optimized by considering that large devices give low on-resistance while smaller devices give lower leakage. For example, discharging switches S_5, S_6 are sized weak since the discharge delay does not affect frequency. Switches S_3, S_4, when off, see a V_{GS} of −150mV, decreasing leakage by >30x, and are hence sized for resistance.

The comparator and Schmitt trigger design is shown in Fig. 10.7.3. In order to handle low common-mode inputs, a PMOS-input design is used and saturation of the input pair is ensured by sub-threshold operation. Transconductance efficiency (g_m/I_d) is also maximized, hence reducing power. The bandwidth of the comparator is set such that its delay is about 100ns, <0.4% of the period. In addition, to keep the comparator delay independent of temperature, a PTAT current reference is used, ensuring constant g_m in sub-threshold, which in turn gives constant bandwidth. During the change of phase, when nodes V_1 and V_2 switch roles, the comparator has small voltage glitches, which may result in rail-

to-rail glitches at the output of the inverters. In order to prevent these glitches, and limit cycling, the first buffer stage connected to the comparator is a Schmitt trigger, implemented in a digital fashion. A small hysteresis minimizes asymmetry in the switching point of the comparator in the two phases. Weak high-VT transistors provide a hysteresis of a few 10s of mV, which is still sufficient to eliminate glitches. The Schmitt trigger and subsequent inverters add <10ns to the overall delay, and hence do not affect temperature stability of the oscillator.

The oscillator was fabricated in a 65nm CMOS process. The die photo is shown in Fig. 10.7.7. The RC oscillator consumes an area of 0.032mm². The oscillator operates from a 1V supply and consumes 120nW. The current sources charging R and C consume 30nA each, the comparator 40nA, current mirrors 10nA and the Schmitt triggers and buffers consume 10nA. The current reference, shared with the rest of the system, works from a system supply voltage of 1.5V-3.3V and consumes 25nA. It generates the 10nA PTAT current reference required for the oscillator. The center frequency is tunable from 9 to 30kHz through on-chip R and C tuning. All measurements described further are at the center of this range (~18.5kHz). The oscillator has a supply voltage dependence of less than 1%/V, allowing relaxed supply regulation requirements.

Temperature stability measurements are shown in Fig. 10.7.4. Over −40 to 90°C, the oscillator has a frequency variation of ±0.25%. In a reduced temperature range from 0 to 90°C, the frequency variation reduces to ±0.1% for an average of about 22ppm/°C. The effect of offset compensation is also demonstrated by comparing temperature stability of the total period with the period of one of the phases. Offset cancellation achieves a 7x reduction from ±1.8% down to ±0.25%. The effect of charging current values is characterized by comparing two charging currents, 20nA and 30nA. At 20nA, switch leakage and reduced slope on the capacitor charging degrades performance giving ±0.5% temperature variation. The total oscillator current consumption as a function of temperature is also plotted in Fig. 10.7.4.

Long term stability of the oscillator is also critical to sleep-mode timer performance, and is captured by the Allan deviation, plotted in Fig. 10.7.5 for a 24hr measurement in a typical office environment. At averaging times below 0.5s, it is white noise limited; and beyond this, it is flicker noise limited. The offset-cancellation scheme helps reduce the flicker noise and its contribution to the Allan deviation, leaving a floor below 20ppm for intervals over 0.5s. This indicates the ability of the oscillator to measure long sleep times accurately. Fig. 10.7.6 summarizes this work and compares it with previously published RC oscillators operating in various frequencies.

In conclusion, an offset cancellation scheme has been presented that helps achieve temperature stability of ±0.25%, ultra-low power operation at 120nW and long-term stability of better than 20ppm, advancing the state of fully-integrated timers for wireless sensors.

References:
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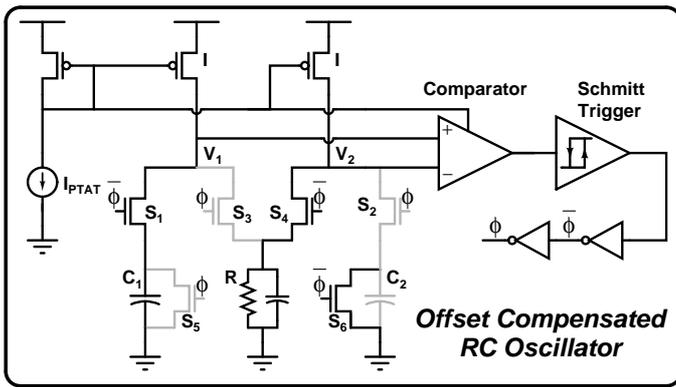
Figure 10.7.1: Architecture of the proposed offset compensated RC oscillator. The switch state for phase φ=0 is shown with off switches grayed out.

$$t_{\phi=1}=RC-CV_{OS}/I \quad t_{\phi=1}=RC+CV_{OS}/I \quad t_P=2(RC+t_{Delay})$$
$$+t_{Delay} \qquad +t_{Delay}$$
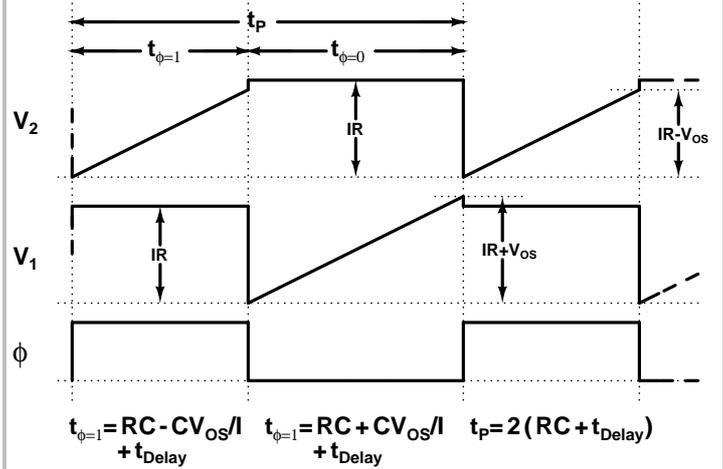
Figure 10.7.2: Timing diagram showing the operation of the offset-cancellation architecture for the case of positive comparator offset V_{OS}.
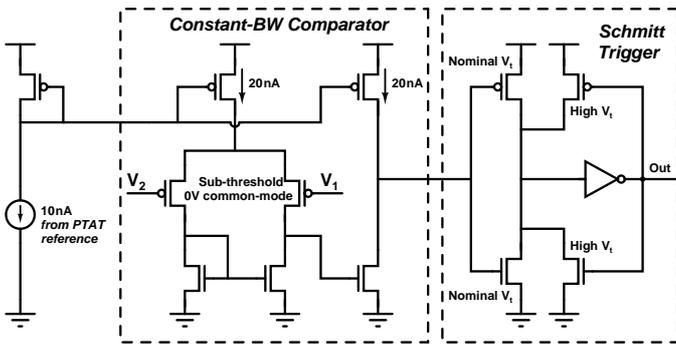
Figure 10.7.3: Implementation of the constant-BW comparator and the digital Schmitt trigger.
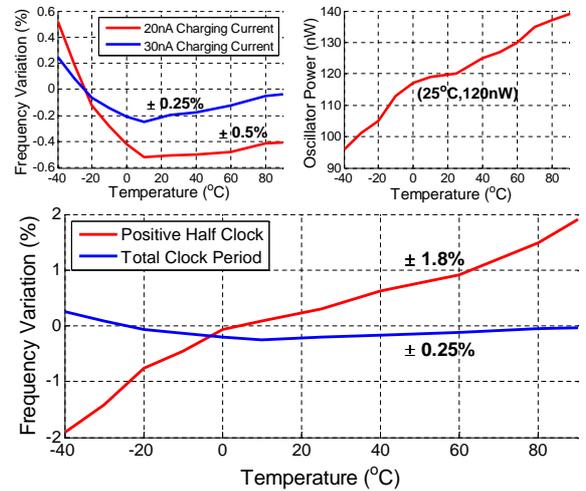
Figure 10.7.4: Temperature measurements for the oscillator showing the effect of varying charging current, total power consumption and effectiveness of the offset compensation scheme.
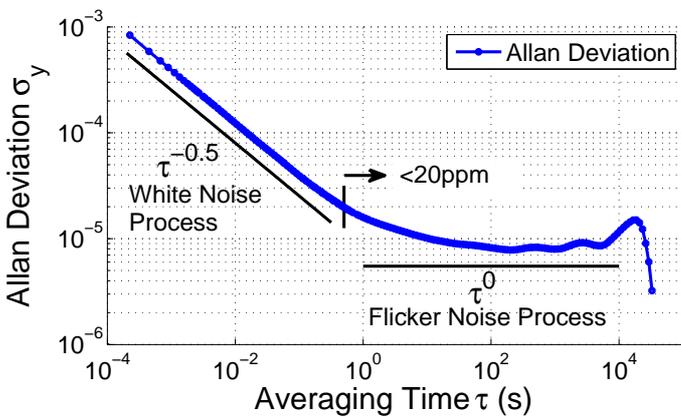
Figure 10.7.5: Allan Deviation measurement over 24 hours shows long-term stability of the oscillator.

Ref	Process	Area (mm^2)	Freq (kHz)	Power (µW)	Temp Accuracy	Temp Range (°C)	Voltage Accuracy
[1] VLSI'12	90nm	0.12	100	0.28	± 0.68%	-40 to 90	5.7%/V
[2] ISSCC'09	0.18µm	0.04	14000	45	± 0.19 %	-40 to 125	1.6%/V
[3] ISSCC'11	0.13µm	0.01	0.00037	0.00066	± 0.14%	-20 to 60	-
[4] VLSI'12	60nm	0.048	32.768	4.48	± 0.1%	-20 to 100	0.06%/V
[5] ISSCC'09	0.13µm	0.073	3200	38.2	± 0.25%	20 to 60	4%/V
[6] ESSCIRC'10	0.18µm	0.016	31.25	0.36	0.4%/C	-	5%/V
[7] JSSC'09	65nm	0.11	100	20.8	± 1.1%	-22 to 85	2.3%/V
This Work	**65nm**	**0.032**	**18.5**	**0.120**	± 0.1%	0 to 90	**1%/V**
					± 0.25%	-40 to 90	

Figure 10.7.6: Summary of measured results and comparison to previous work.
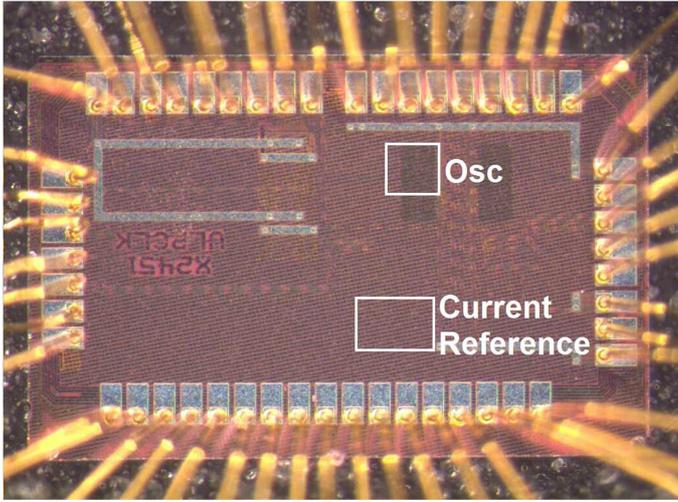
Figure 10.7.7: Die photo of the chip fabricated in 65nm CMOS.