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Upgrade of the ICRF Fault and Control Systems On Alcator C-Mod

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***Abstract*—The Ion Cyclotron RF Transmitter System (ICRF) at Alcator C-Mod comprises four separate transmitters each capable of driving 2 MW of power into plasma loads. Four separate transmission lines guide RF power into three antennas, each mounted in a separate horizontal port, in the C-Mod Tokamak.**

Protection for the antennas, matching elements and transmission line is accomplished by two unique but interdependent subsystems encompassed by the ICRF Fault System. The Antenna Protection System evaluates antenna phasing and voltage, sets fault thresholds, generates fault signals, and passes fault information to the Master Fault Processor. During operation, the Master Fault Processor is responsible for detecting hazards along the transmission line, generating faults, processing faults from the Antenna Protection System, terminating RF drive and extinguishing faults within 10μs. In addition, the system controls various delays and sets the boundaries for RF retries. The ICRF Control System provides amplitude regulation for all antennas and phase control for a four-strap antenna.

We are modifying some of the fault processing components and control elements of these systems in an effort to improve reliability and serviceability, and increase flexibility. This upgrade will reduce wired interconnections, add remote features to improve access to key operating parameters, improve RF isolation with new switching components, simplify phase control, and expand the RF regulation system to an active control regime whereby plasma parameters may become direct feedback elements for RF regulation. Details of the proposed upgrade to the system will be presented, and implementation of any new technological tools will be discussed.

I. INTRODUCTION

The present ICRF Master Fault Processor was designed and built in the early 1990's and employs four hand-wired electronic boards. Each of the four transmitter systems has a dedicated set of four boards whose cumulative purpose during an RF pulse is to receive, record and report faults, and provide signal to disable RF during fault conditions. A fifth mixed signal hand-wired board uses fault information to provide orderly fault handling for the RF Modulator.

A large portion of the upgrade effort is intended to modernize and consolidate these separate yet interdependent boards into two PC boards with up to date logic components and expanded features. Addition of remote access to key operating parameters will assist in antenna conditioning and plasma operations. Aside from reducing the number of wired interconnections the upgrade also gives an opportunity to develop Ethernet based communications with applications for other systems on C-Mod.

The installation of a new solid state Intermediate Power Amplifier (IPA) for the tunable ICRF transmitters on C-Mod provides the impetus for changing the design of some of the low level RF systems that drive the new IPA [1]. Additions and changes in low power RF components will include power adjustability, better isolation, and power monitoring among other features.

A new method of phase control for the four strap antenna is being evaluated for this upgrade as well. The present hardware, two interdependent phase-locked loops (PLL) circa 1980, contains obsolete components and is difficult to troubleshoot. Response time of the present controller is marginal for our purposes. We have a conceptual design for a phase controller that will eliminate PLL issues, and allow migration towards an active control regime whereby antenna "modes" can be controlled throughout the RF pulse.

II. ELECTRONICS MODERNIZATION

A. *Master Fault Processor*

The Master Fault Processor (MFP), receives detected faults, processes the information, and extinguishes RF in under 10 μS. The MFP also determines the time of RF suppression for each fault, keeps a record of the number of faults for a given RF pulse and permanently shuts down RF drive when a preset "retry" limit is reached.

A first-order goal of this modernization is to reduce interconnections between the major electronic elements with an eye towards solidifying system reliability and reducing manned entry during plasma operations. Since the time of the development of the present system, progress in Large Scale Integration provides a number of options for repackaging and improving the layout of these electronics.

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The Complex Programmable Logic Device (CPLD) allows a large number of programmable logic configurations and I/O options. These devices come in a variety of logic densities and may be programmed using either C, VHDL, or manufacturer provided software, some of which is free. Along with fairly inexpensive hardware, evaluation products, web based seminars and other assistance, getting into the CPLD market has become relatively easy.

The upgraded MFP employs a home-grown digital electronic board called the "General Purpose CPLD Board" (GPB). Developed by engineers at C-Mod, the board offers multi-channel access to a programmable logic device with the option of configuring each channel separately for Input/Output (I/O). In addition, each channel has the option of differential I/O connector or an optical receiver/transmitter. See Fig. 1.

Figure 1. General Purpose CPLD Board

The GPB consists of twelve I/O channels, each connected to an I/O pin on the CPLD. Two on-board headers provide access to twenty four additional CPLD I/O pins. The board is designed so that "mezzanine" boards can be attached and cabled to the headers. Up to two of these mezzanine boards can be attached giving access to the additional CPLD pins on the "mother" board. Pre-built mezzanine configurations are available with standard I/O connectors, but customization is also possible as discussed later.

The GPB provides sufficient I/O so all faults for one transmitter can be processed through a single board leaving spare channels for future use. The 128 macro-cell CPLD on-board allows programming of all the processing functions for inbound faults, maintaining fault counts, setting pulse widths, and outputting results from a single IC. Implementation of the GPB reduces the four board wired fault system to a single board with most of the interconnections internal to the CPLD IC.

B. RF Modulator

The second critical feature of the upgrade offers the RF operator remote access to setpoints within the Master Fault Processor and the RF Modulator (Modulator). Presently, these setpoints can only be changed manually through an on-board jumper, or removal and replacement of a soldered component, requiring manned entry to restricted areas and lost plasma operations time.

Establishing remote access to these values is an important tool for RF conditioning, troubleshooting, as well as plasma operations. The new design allows setting fault retry limit, fault retry delay, RF rise time delay, and feedback integration time. The basic function of the Modulator is unchanged, however improved buffering was added to analog output lines and some components were updated to address obsolescence.

Two setpoints we desire to control reside on the Modulator so it was packaged as a custom mezzanine board to the GPB with access to twenty-four unused CPLD I/O pins. The new Modulator features updated components and necessary hardware to establish Ethernet communications between the RF operations console and the CPLD on the GPB.

With an extensive private network established at C-Mod an Ethernet connection was designed at the remote site on the new Modulator board. The remote Ethernet link is designed around an IC dedicated to Ethernet communications. Data transmitted and received through the link is decoded by a companion PIC Microprocessor and converted to two address bits, four data bits and a control line along with a clock for synchronizing data operations. Fig. 2 provides a graphical representation of the Ethernet connection.

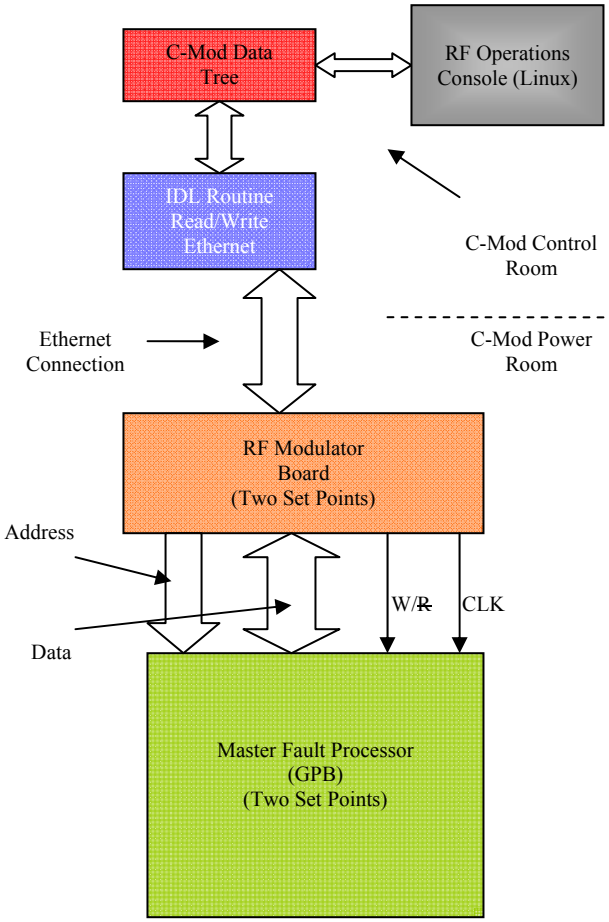

Figure 2. Data Flow Remote Ethernet Connection

The CPLD on the MFP is programmed with four addressable bidirectional registers. Each register is four bits wide and represents one of the setpoint quantities to be addressed. As a result, sixteen unique selections for each setpoint are possible. Programming allows for larger data registers and address buses to suit the application, limited only by the density of the CPLD array.

Two setpoints reside on the RF Modulator board. The "RF Rise Time" determines how quickly the RF rises to meet the demand waveform during a RF retry. Tweaking this rise time in some operating regimes can assist in fault recovery and improve RF performance. The "Integration Time" setting changes the speed of the feedback loop and is included as a means of experimenting with overall RF regulation.

On the Modulator, two dedicated four bit analog switches read data from the CPLD, toggle appropriate switches and insert or remove capacitors to alter rise time or integration time to meet the demand of the RF operator. The capacitors are arranged in rough multiples of two to emulate a binary progression. Provisions have been made, through the use of an additional analog switch, to engage default settings in the event of a communications link failure.

The remaining setpoints, "Retry Delay" and "Retry Limit", are handled internally by the CPLD. These two settings respectively control the RF suppression time during a fault and the number of times RF is retried during a RF pulse after a fault is encountered. Ability to alter the Retry Limit quickly and conveniently is a valuable asset during RF conditioning and troubleshooting and reduces the necessity of time consuming manned entries to the C-Mod Power Room.

III. RF Source Upgrade for Tunable Transmitters

Along with fault system upgrades an upgrade of the tunable transmitters Intermediate Power Amplifier (IPA) has been completed, providing the momentum to make changes and improvements to the low level RF power source [1].

The low level power chain contains a number of elements related to source power scaling, power regulation, fault handling, and phase control. The first phase of the low level power upgrade is to repackage three of these elements. Phase control, while part of the low level system, is a separate work and will be discussed later.

Fig. 3 shows the configuration of the new low level power chain and some of its features. When a RF related fault is detected a fault signal is generated by detection hardware and propagated through the fault system to the MFP. The MFP immediately outputs a fail safe signal called the "Gate" to an RF switch, located in the low level RF power chain, which opens and terminates the RF source to the IPA.

In order to improve RF isolation and lower insertion loss we replaced the switching element from a voltage controlled frequency mixer to a biased PIN diode switch. The new switch boosts RF isolation by 30-40 dB when bias is applied, and has a TTL control input compatible with MFP output logic. The switch also terminates lines into 50Ω when it is opened and switching speeds of 10ns are typical. The increased isolation is dependent on the presence of bias and therefore a new fault line has been introduced to the MFP to insure RF is disabled and fault is indicated if switch bias is lost.

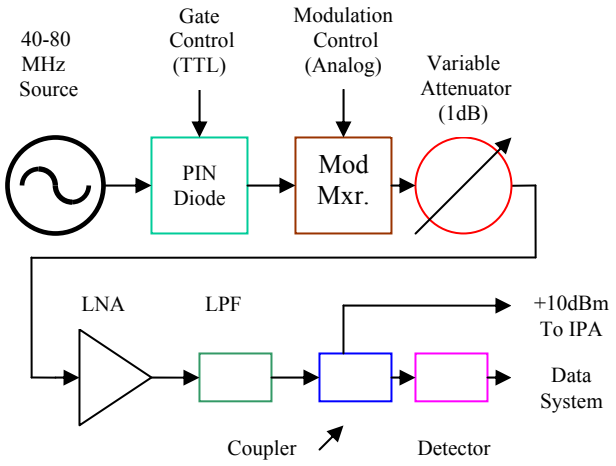

Figure 3. New Low Power Chain For Tunable Transmitters

Other changes made to this system include an adjustable 1dB attenuator to make fine adjustments to IPA input power, directional coupler allowing RF sampling and data system monitoring, a low noise amplifier to insure sufficient IPA drive, low pass filtering, and a new enclosure with panel LED's indicating switch bias and fault indications. This system has been prototyped, tested and is intended for use in the upcoming C-Mod run campaign.

IV. Phase Control

A. *Fundamental Phase Control Change*

For operation of the four strap antenna, a part of the tunable transmitter system, phase control between antenna elements is required. This is presently accomplished by a complicated dual Phase Locked Loop system containing a number of obsolete parts and whose time response is considered marginal for our purposes.

There are a few alternatives to this design and we are exploring one that moves the phase control from the complex analog PLL system to a digital scheme that brings the system into the modern era, simplifies hardware, resolves time response issues, allows for reconfiguration as necessary, and opens an array of experimental possibilities in the near future.

Since adequate amplitude control of RF power is available through the RF Modulator the focus will be on controlling phase only, however this method may also be expanded to include amplitude control as well. Inphase/Quadrature (I/Q) detectors are commonly used to measure the phase shift between two RF signals of the same frequency.

The I/Q detector outputs two analog signals related to the relative input phase shift, I and Q. From these signals the resulting magnitude $|M|$ and phase φ can be calculated separately. Magnitude is calculated as in (1).

$$|M| = \sqrt{(I^2 + Q^2)}. \quad (1)$$

Phase is calculated by (2):

$$\varphi = \tan^{-1}(I / Q). \quad (2)$$

Our proposed plan for making the phase measurement involves constructing a look-up table (LUT) within a flash memory. Contained in the LUT will be a unique, system specific, array of magnitudes and phases.

Output from the I/Q detector will be digitized and the digital result will be used to address to these vectors in the LUT. As we are only interested in the phase component of these data, magnitude information will be ignored and only phase information will be recovered from the LUT.

Digitized phase information coming from flash memory will then be reconverted to analog information and processed together with operator determined phase offsets and used to drive a voltage controlled phase shifter. The voltage controlled phase shifter will be connected to the low level RF drive of one of the antenna straps in order to make the phase correction.

B. Active Phase Control

This redesigned system will make possible the migration of ICRF operation towards an active phase control regime where the operating modes of the antenna could be changed from heating phase to current drive phase during RF pulses [2]. This system has been proposed, groundwork done and a prototype of this system is planned for the middle of the upcoming C-Mod run campaign.

V. FUTURE WORK

Active control experiments are likely to be expanded to an operating mode where plasma parameters become part of the feedback loop for RF power and mode control. This opens a wide opportunity for greater experimentation with current drive and heating using ICRF systems. In this operating regime the Digital Plasma Control System will become the feedback element for amplitude and phase control whereby ICRF will be regulated by plasma parameters. This work is not planned until FY 2010.

ACKNOWLEGMENTS

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[1] Alan S. Binus, S.J. Wukitch, Y. Lin, “An Intermediade Power Amplifier Upgrade for 40 to 80 MHz for the Alcator C-Mod ICRF Transmitters,” unpublished.

[2] S.J. Wukitch, Y. Lin, Private Communication.