

A Low Power Display Architecture for
Organic Light Emitting Diode Microdisplays

by

Valencia M. Joyner

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology

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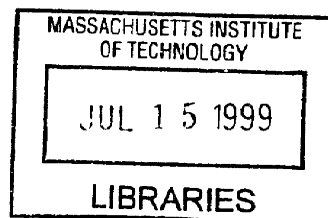
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Author _____
Department of Electrical Engineering and Computer Science
May 21, 1999

Certified by _____
Akintunde I. Akinwande
Associate Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by _____
Arthur C. Smith
Chairman, Department Committee on Graduate Theses

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ABSTRACT

Organic light-emitting diode (OLED) devices offer a very promising alternative to existing flat panel display technologies, such as liquid crystal displays (LCD) that currently dominate the market. OLED displays offer very attractive characteristics, including higher luminous, larger viewing angle, and low-power consumption, over the established LCD technology. The ability to integrate OLED devices on a silicon microchip is one of the most favorable characteristics of this new technology. The primary goal of this research project is to implement a low-power display driver circuit for an OLED microdisplay. The implementation will be chosen based on the outcome of a feasibility study aimed at investigating the various options available for addressing the display and the design requirements imposed by the operation of the OLED. There are three primary design options to be considered: 1). Passive Matrix Addressing with sequentially addressed rows/columns, 2). Active Matrix Addressing with sequentially addressed rows/columns and dynamic storage at each pixel, and 3). Active Matrix Addressing with sequentially addressed rows/columns and static storage at each pixel. Each implementation is compared in terms of the overall power consumed in driving the high capacitance row and column lines in the display matrix.

Thesis Supervisor: Akintunde I. Akinwande
Title: Associate Professor, MIT Electrical Engineering and Computer Science
Department

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To my beloved parents and family, for their continuous love, support, encouragement, and prayers.

Trust in the Lord with all thine heart;
and lean not unto thine own understanding.
In all thy ways *acknowledge* him, and he shall direct thy paths.
Proverbs 3:6-7

I can do all things through Christ which strengtheneth me.
Philippians 4:13

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1. Introduction

Until recently, cathode ray tubes (CRT) dominated the display market. In this new era of portable systems providing intensive communication capabilities, the demand for light-weight, low-power, high information content displays has increased. In order to meet this demand, a new breed of displays categorized as flat panel displays (FPD) have been engineered and marketed. Flat panel displays come in various forms, each with significant strengths and shortcomings in reaching the ideal goal of a compact, battery-powered display with CRT-like quality, large viewing angle, and full color capability. Research institutions and commercial industries around the world are making every effort to improve the performance of various flat panel display technologies in order to propel the new era forward and meet the demands of the expanding market.

Flat panel displays can be found in various sizes ranging from 40 in. diagonal bulletin board screens to 0.5 in. diagonal head-mounted projection displays. The emergence of a new industry is being seen among the miniature electronic displays that are less than one inch diagonally and are built on a silicon microchip. With the aid of magnifying optics, miniature displays can be used as a 'virtual' display to enable video conferencing on a portable cellular phone, or display text and images from a portable web browser, for example.

These microdisplays are implemented with an active matrix addressing scheme with imbedded control circuitry extending the operation time of each pixel , and thereby, improving the screen brightness. The ability to fabricate peripheral addressing circuitry simultaneously with the active matrix of pixels offers significant advantages that will be discussed in this introductory chapter.

The Active Matrix Liquid Crystal Displays (AMLCD) technology has risen to dominance in the flat panel display market over the past few years offering superior performance for high information content displays.. However, its inherent limitations in terms of power-efficiency and viewing angle have motivated researchers to search for alternative technologies that provide better performance. One of the more recent and promising alternatives are organic light-emitting diode (OLED) displays. OLEDs offer very attractive characteristics, including higher luminous efficiency, larger viewer angle, and low-power consumption, over the established LCD technology. The recent burst of technological advances to increase the performance of these devices has created a myriad of exciting new opportunities for OLEDs in the flat panel display market, particularly in the area of microdisplays. OLED device compatibility with existing addressing and display driving methods such as active matrix addressing has spurred great interest in this technology. This introductory chapter will briefly discuss the benefits of integrating display electronic circuitry with the pixel array and an overview of existing microdisplay technologies. A summary of the objectives and contributions of this research endeavor is also presented.

1.1 Liquid Crystal on Silicon Technology

There are several key advantages to integrating circuitry into the active matrix of the display. This technology is commonly known as Liquid Crystal on Silicon (LCOS) and it provides remarkable advantages for display applications, particularly microdisplays. In its beginning stages, this technology was targeted to liquid crystal displays. However, the overall concept can be applied to displays incorporating a variety of optical materials including electroluminescent phosphors, micro-machined mirrors, and organic light emitting devices. LCOS microdisplays are made by placing a thin layer of optical material directly on top of a silicon chip.

One of the primary reasons to move towards the LCOS technology is the reduction of overall system cost. The control needed to distribute timing and data signals to rows and columns can be simultaneously fabricated with the pixel array. This innovation reduces the number of external connections to the active matrix and improves the reliability and packaging yield of the display device. CMOS fabrication processes are well established and the advanced lithographic techniques available are capable of producing high density pixel arrays with superior resolution. In addition, VLSI circuits and low power design techniques that are readily used in microprocessors and memory circuits can be applied to addressing and controlling microdisplays. Another favorable attribute of LCOS is that the high frame rates achievable with digital CMOS circuitry have the potential to extend the grayscale capabilities of microdisplays. These characteristics of LCOS make this technology highly desirable for manufacturing microdisplays with superior image quality and low power consumption.

1.2 Overview of Microdisplay Technologies

The ideal flat panel display has excellent image quality, low power consumption, and compactness. Several technologies that can meet these requirements are under development. The technologies discussed in this section are representative of nearly 90% of the flat panel display technologies that are presently on the market. A more complete review of existing display technologies for portable systems can be found in [1,2].

1.2.1 Electroluminescent Displays

An electroluminescent display (ELD) is a type of emissive display that generates light through the excitation of a powder phosphor or thin film phosphor layer. There are four types of ELDs: (1) dc powder ELD, (2) ac powder ELD, (3) dc thin-film ELD, and (4) ac thin film ELD.

Overall, the ac thin film ELDs have made the most progress in the flat panel display industry out of the other four technologies. Light emission is initiated by producing a high electric field across the EL structure, which consists of a phosphor layer sandwiched between two insulating layers. The high electric field is produced by applying a voltage bias. When the voltage bias reaches a certain threshold level, a current flows in the phosphor layer. This current excites the electroluminescent center within the phosphor and light is emitted.

The performance of ELDs can be further enhanced by employing an active matrix approach to addressing the display. Active matrix electroluminescent displays (AMELD) have been developed for miniature head mounted display (HMD) applications. The low power, low weight, compactness, and brightness of AMELDs make them the ideal choice for these applications.

High density AMELDs with 2000 lines per inch in resolution have been reported.[3] Despite the reduction in size, these displays continue to maintain high brightness and high contrast. A diagram of the AMELD pixel is shown in Figure 1.1. The state of the pixel is programmed by the low voltage control transistor (M1). When M1 is turned on by the select line, the logic level present on the data line is passed to the hold capacitor, connected to the gate of the high voltage transistor (M2). A logic high level stored on the capacitor will turn on the device, providing a conducting path for current to illuminate the pixel. A logic low level will cause M2 to block current. In this configuration, each pixel operates in a manner similar to a DRAM memory cell. The hold capacitor is capable of holding the desired logic level at each pixel for the entire frame period, and thus, the screen brightness is significantly increased.

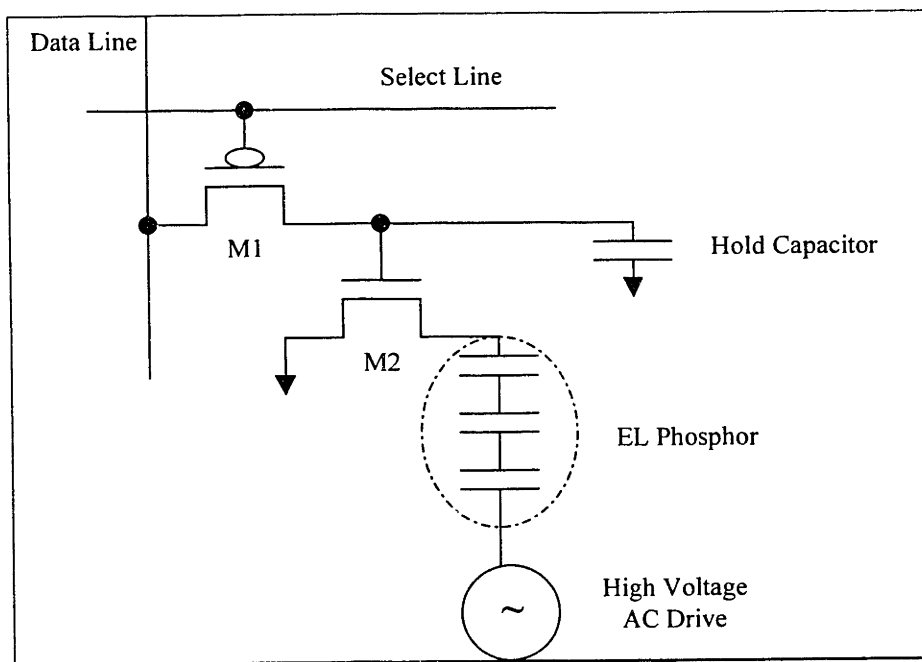


Figure 1.1 AMELD Pixel Structure

1.2.2 Vacuum Fluorescent Displays

Vacuum fluorescent displays (VFD) are also a type of emissive display. A hot wire thermionic filament is used to create a supply of relatively low energy (12-200eV) electrons. An electric field directs these electrons across a vacuum gap (0.5 – 2mm). Luminescence is initiated by the bombardment of these electrons on the phosphor material. Since 1977, VFDs have been implemented primarily in automotive applications. These displays are very rugged and offer high brightness, wide viewing angle, and low power consumption, and demonstrate stable operation over a wide temperature range. All of these characteristics make VFDs the display of choice for automotive head up display applications, for example.

Over the past few decades, this technology has evolved to an active matrix configuration further enhancing the performance. AMVFDs spot have shown luminance levels of 9600 ftL (32,500 cd/m²), a significant increase from the 700 ftL observed in the first displays that implemented direct pixel addressing [4]. The AMVFD integrates a CMOS static memory latch at each pixel as shown in Figure 1.2. The memory element and series transistor provide continuous drive to the phosphor material and maximizes display brightness. The pixel memory latch consists of two cross coupled inverters. Input signals are routed to the pixel by the row and column electrodes and on chip addressing circuitry.

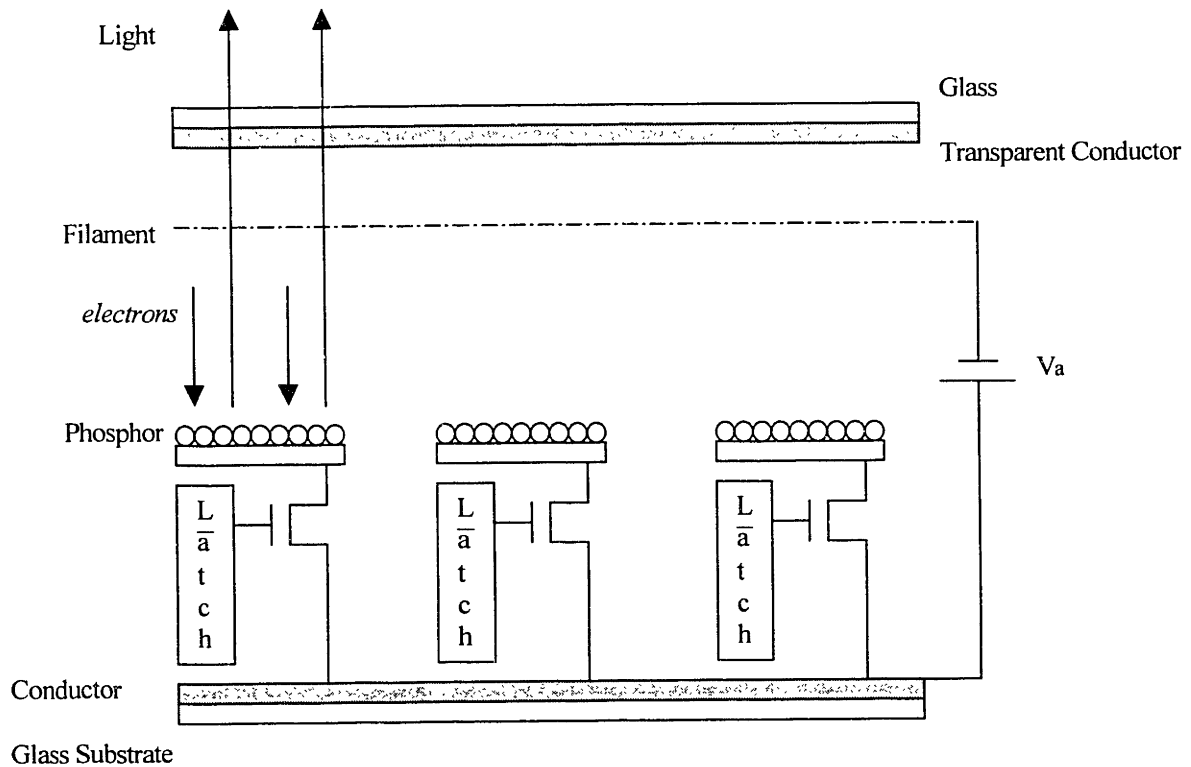


Figure 1.2 AMVFD Pixel Structure. $V_a=60v$ 1.2.3 Liquid Crystal Displays

Over 90% of the flat panel display market is dominated by the liquid crystal display (LCD) technology. LCDs have proven to be the most optimal flat panel display technology to simultaneously meet the critical requirements of low-power, high luminous efficiency and brightness, long battery lifetime, and full color capability for portable display systems. LCDs have also become the flat panel display of choice due to their low operating voltage and compatibility with CMOS logic.

There are many different types of liquid crystal materials including nematics, smectics, ferroelectrics, to name a few. A basic review of the operation of these materials will be presented here.

Liquid crystals consist of elongated organic molecules with an alignment that can be altered when an electric field is applied across the material. The alignment of the liquid crystal material will induce a polarization on the incoming light beam that reaches the material. The polarization angle will be a function of the voltage applied across the material, which is typically as low as 5v. The complete liquid crystal display structure also consists of optical polarizers placed on the front and back side to selectively pass or block the incoming light depending on the polarization angle. Thus, the liquid crystal acts as a light valve that controls the transmission of light, which is typically generated by a backlighting source, depending on the applied voltage.

For high information content display applications, Active-Matrix Liquid Crystal displays are the technology of choice. The high switching speeds of ferroelectric liquid crystal materials, for example, coupled with the high frequency addressing capabilities of digital CMOS circuitry have made 24-bit grayscale possible with high resolution displays [5].

Despite the prominence of all these technologies, there is still a need of improvement in certain areas such as power consumption and display fabrication. Electroluminescent displays are emissive and display bright images independent of a lighting source, but operate at very high voltages ($>100\text{v}$). Vacuum fluorescent displays require a vacuum environment. Liquid crystal displays operate at low voltages ($\sim 5\text{v}$), but they are non-emissive and require an external lamp to produce bright images. Liquid crystals are also highly sensitive and prone to severe chemical degradation by extreme temperatures and the presence of a non-zero net voltage across the material. The former condition adds complexity and additional constraints on the addressing circuitry for a

liquid crystal display. OLED displays, however, operate at low voltages ($<10\text{v}$) and are emissive in nature, and therefore, operate without an external power consuming, backlighting system. In addition, organic microdisplays are conveniently fabricated by depositing thin layers of organic materials directly on top of the silicon chip. These characteristics give OLED displays the potential to exceed the performance of existing flat panel display technologies in some applications. In the midst of efforts to improve the stability and reliability of organic materials, only recently has there been a focus on studying addressing and driver circuitry for this novel display technology.

1.3 Thesis Objectives and Contributions

The primary objective of this work is to implement a low power OLED microdisplay with grayscale capability. In terms of information content, the display design is targeted to applications where the display graphics are primarily static, such as in a portable video conferencing device, where there is minimal change in the background features of the image being displayed, or a personal digital assistant system, for example. These display specifications greatly influence the necessary design issues and constraints that one must consider when designing driver circuitry for an OLED display.

OLED technology offers many favorable characteristics that heighten its potential for growth in the flat panel display market. Various display architectures have been considered and investigated in order to evaluate their feasibility and power efficiency in driving OLED microdisplays. Minimizing power consumption continues to be a key design optimization for portable display systems, where the extension of battery lifetime is a one of several primary concerns.

2. Light Emitting Devices: An Overview

The recent discovery of organic and polymer materials that emit light has sparked a new interest in LED devices for use in microdisplays. This section will present background information on the operation of LEDs in general, including the physics of light emission, characteristics of light emitting devices, and a brief overview of organic semiconductors and OLED device properties.

2.1 Physics of Light Emission

Electroluminescence is the process by which electrical energy is converted to light. Light is emitted through the radiative recombination of electron-hole pairs in the lattice. During this recombination process, energy absorbed during carrier excitation is given off as light or heat. When an electron drops from an upper to a lower energy level and recombines with an hole, a photon is emitted. These levels can consist of either intrinsic band states or impurity levels. The primary goal in LED technology is to maximize the light output by increasing the probability of radiative recombination in semiconductor compounds, the most commonly used materials for these devices.

In order to maintain conservation of momentum, the change in momentum of an electron and hole involved in radiative recombination must equal the momentum of the photon emitted. In general, photons have negligible momentum, and therefore, there must be no net change in momentum of the electron and hole involved in recombination. Figure 1.3 shows a schematic energy band diagram versus momentum, represented as k , for two types semiconductor materials: direct and indirect bandgap semiconductors. The schematic shows that the momentum conservation requirement allows only vertical transitions. For direct bandgap semiconductors, there is a higher probability of vertical

transitions and these materials have been most successful in producing high performance LEDs.

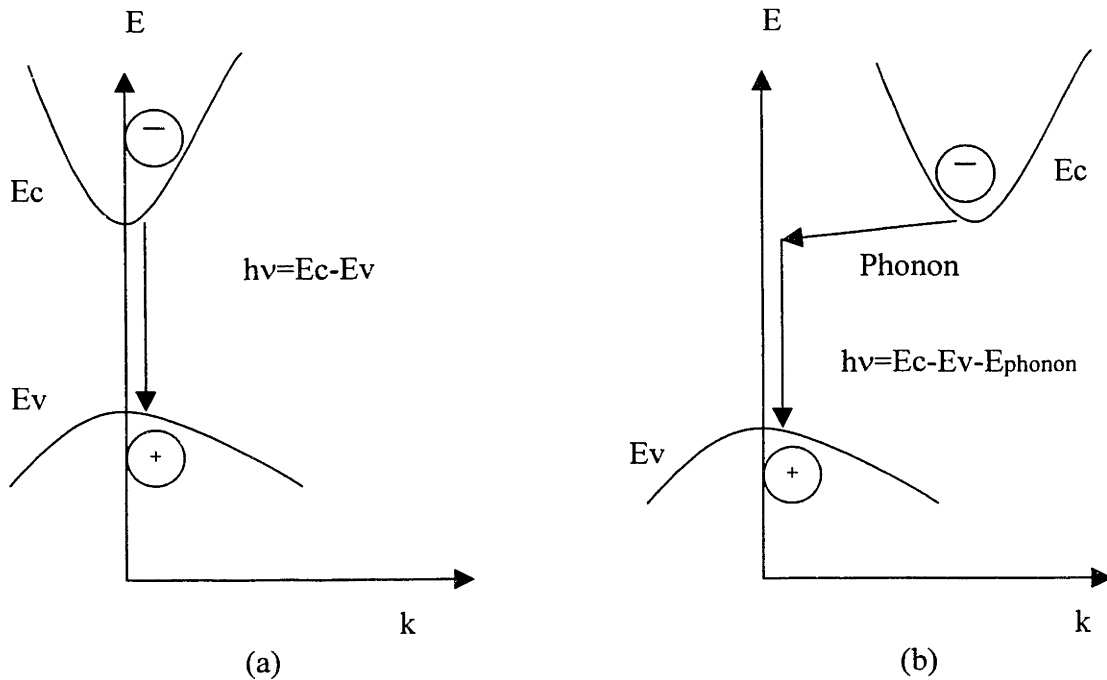


Figure 2.1 Radiative recombination in (a) direct gap semiconductors, (b) indirect gap semiconductors. Electron energy, E, versus momentum, k.

The wavelength of the radiation given off during this process is related to the bandgap energy that separates the valence and conduction bands of a particular material. This relationship is expressed in the following equation:

$$\lambda = \frac{h c}{E} \quad (2.1)$$

where, h is Plank's constant ($6.63 \cdot 10^{-34} \text{ J-s}$), c is the velocity of light ($3 \cdot 10^8 \text{ m/s}$), and E is the bandgap energy ($E_c - E_v$).

This equation can also be written in the more convenient form given below.

$$\lambda(nm) = \frac{1237}{E(eV)} \quad (2.2)$$

In this form the wavelength is expressed in units of nanometers (nm) and the bandgap energy is expressed in units of electron volts (eV). Therefore, a direct gap material such as gallium arsenide with a bandgap of 1.4 eV will have a wavelength of 883nm.

2.2 Emission Efficiency

The performance of an LED is measured in terms of a variety of parameters that characterize the efficiency of light emission in the device. A key parameter in measuring the efficiency of luminescence is the internal quantum efficiency, η_q . It indicates the relative number of radiative versus nonradiative transitions in the lattice. Nonradiative transitions are caused by the presence of recombination sites at crystalline defects and surface states resulting in heat generation instead of light.

The overall efficiency, also called the external quantum efficiency, η_{ext} , is the ratio of the number of photons generated internally to the number of photons that actually reach the outside of the material and can be seen. The overall efficiency is degraded by losses such as absorption and internal reflection, which affect the transmission of light across the surface of the device to the outside.

The quantum efficiency is dependent on the radiative and nonradiative lifetimes, T_r and T_{nr} respectively. The following expression describes the relationship:

$$\eta_q = \frac{1}{1 + T_r/T_{nr}} \quad (2.3)$$

The light attenuation caused by absorption at the surface of the device after traversing a distance, d , can be expressed as $\exp(-\alpha \cdot d)$, where α is the absorption coefficient and is dependent on the wavelength.

The partial reflection due to the different refractive indices that the light encounters at the surface of the device also contributes efficiency loss. This loss is quantified by the reflection coefficient, R , and is dependent on the index of refraction, n , inside the material through the following relationship:

$$R = \frac{(n-1)^2}{(n+1)^2} \quad (2.4)$$

Considering the above factors, the overall efficiency of an LED device can be condensed into the following expression:

$$\eta_{ext} = \eta q \cdot (1 - R) \cdot (1 - \cos \theta_c) \cdot \exp(-\alpha \cdot d) \quad (2.5)$$

where, θ_c , is the critical angle. All rays incident on the surface at an angle greater than this critical angle will experience total internal reflection. Typically, the overall efficiency of an LED is less than a few percent.

The power efficiency of an LED device is a measure of how much of the electrical power supplied by the source is converted to visible light. This quantity is dependent on the resistive losses at the metal-semiconductor contact regions, losses in the semiconductor itself, and the external quantum efficiency.

2.3 Excitation Mechanisms

In order to initiate electroluminescence, the free carriers must undergo excitation through the supply of either potential or kinetic energy to the system. The majority of commercially available LEDs are based on the operation of forward biased pn junctions.

Applying a forward bias leads to minority carrier injection across the pn junction. Radiative recombination of electrons and holes occurs at the junction resulting in photon emission. Confining minority carriers at the junction increases the carrier concentrations and improves the efficiency of the recombination process.

Confinement of carriers is most commonly achieved by using a device structure known as the double heterostructure diode. This device consists of a thin luminescent layer, used for confinement, sandwiched between a p-type and n-type region. Each surrounding region has a larger energy bandgap than the confinement layer, and therefore, carriers are injected into this luminescent layer leading to an increase in radiative recombination in the region.

Excitation can also occur through the bombardment of high energy carriers on other carriers in the lattice. Under the influence of an high electric field, an electron can gain enough kinetic energy to impact other electrons that are bound in the valence band or impurities and create electron-hole pairs. The number of electrons can be effectively multiplied by successive collisions in the lattice. The participation of both electrons and holes in this impact excitation process results in ‘avalanche’ breakdown. Through avalanching, the carrier concentration increases until the current saturates. The kinetic energy needed to create electron-hole pairs through impact excitation depends on the energy gap, E_g , and the effective masses of the electron and holes, m_e^* and m_h^* respectively. The energy and momentum must be conserved. The threshold energy for this process is given as:

$$Et = \frac{m_h^* + 2m_e^*}{m_h^* + m_e^*} \cdot E_g \quad (2.6)$$

The formation of these additional electron-hole pairs through impact excitation leads to an overall increase in free carriers in the lattice resulting in a higher probability of radiative recombination and photon emission.

2.4 Inorganic LEDs

According to equation 2.2, visible electroluminescence requires an energy gap of $\geq 1.8eV$. The semiconductor materials most commonly used in LED technology are inorganic compounds from the Group III and V elements. These compounds have been most successful at achieving the desired energy gap for visible electroluminescence. Both binary and ternary compounds, such as GaAs and $AlGa_{1-x}P_x$, are used to fabricate LED devices. Ternary compounds are particularly useful in terms of being able to adjust the energy gap by changing the composition 'x' of the alloy. The use of the $AlGa_{1-x}P_x$ compound has traditionally been successful in producing red LED devices only. However, in recent years other material structures have been explored, including InGaN/GaN heterostructures producing blue and green LED devices.

2.5 Organic LEDs

Until recently, high performance LED devices were primarily fabricated from inorganic Group III-V materials such as gallium arsenide phosphide (GaAsP) compounds [6]. However, the recent discovery of electroluminescence from organic substances has interested many in the field. The very first demonstration of electroluminescence in organic materials was made in 1963 by Pope using large (50um – 1mm thick) single crystals of anthracene, emitting blue light [7]. A high electric field was produced across the device causing injection of electrons and holes into the conduction and valence band of the anthracene crystal. In these energy bands the carriers

where capable of performing radiative recombination. This process produced very high quantum efficiencies near 8%. However, in order to obtain a reasonable amount of light output these devices were driven at very high voltages near 100v. As a consequence, there was a significant loss in power efficiency for the device [8].

Several scientists and engineers, to improve the efficiency and lower the operating voltage of these organic LED devices, attempted further improvements. Within the past decade, there have been significant research breakthroughs in the area of organic electroluminescence primarily molecular and polymer-based materials. Electroluminescence is due to the recombination of charge carriers injected from opposite sides of the diode and transported across the structure.

2.5.1 Organic Semiconductors

Organic materials with metallic and semiconducting properties are present in various forms. There are a number of materials currently being researched that differ in molecular structure, stability, reactivity with other elements and other characteristics. Two primary categories of organic materials are currently being investigated for use in display applications, in particular: molecular and polymer-based organic materials. This section will provide a brief overview of the properties of these materials and their feasibility in the development of OLED displays.

One of the first major successes in demonstrating efficient electroluminescence in organic materials was made in 1987 by Tang and Van Slyke at Kodak [9]. This group conducted their investigation primarily using a vacuum-deposited “small-molecule” organic material. The conventional structure of an organic electroluminescent diode consisted of a single layer of organic material sandwiched between two injecting

electrodes. The group at Kodak constructed a multi-layer structure consisting a hole transporting layer (aromatic diamine) and an emitting and electron transporting layer (Aluminium chelate complex:8-hydroxyquinoline aluminum (Alq3)). This unique structure demonstrated superior performance with a lower operating voltage below 10v, high quantum efficiencies, and high brightness over the whole visible spectrum.

Efficient polymer-based electroluminescence was first demonstrated in 1990 by Burroughs et al at the Cavendish Laboratory in Cambridge [10]. Experiments were performed on a organic LED device consisting of poly(p-phenylene vinylene) (PPV), a conjugated polymer material, flanked by two conducting electrodes. A low work function material (aluminum with a thin layer of aluminum dioxide, gold, and indium oxide) was used for the negative, electron injecting contact and high work function material (aluminum, magnesium silver alloy, and amorphous silicon hydrogen alloys) for the positive, hole injecting contact [8]. This structure demonstrated efficient light emission in the green-yellow portion of the visible spectrum. Figure 2.2 shows the Current-Voltage characteristics of the polymer LED device in the forward bias regime. From this graph, the device shows a turn-on voltage of approximately 14v. Figure 2.3 contains the electroluminescence characteristics of their experimental device versus the current.

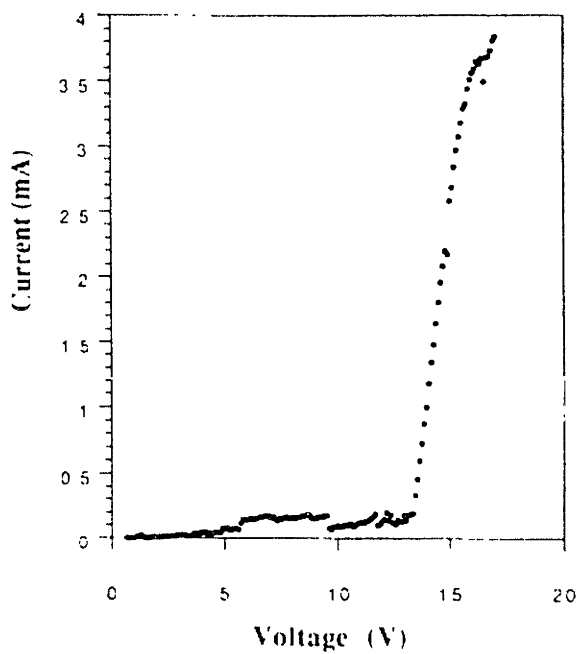


Figure 2.2 Current –Voltage Characteristics of Polymer OLED Device [10].

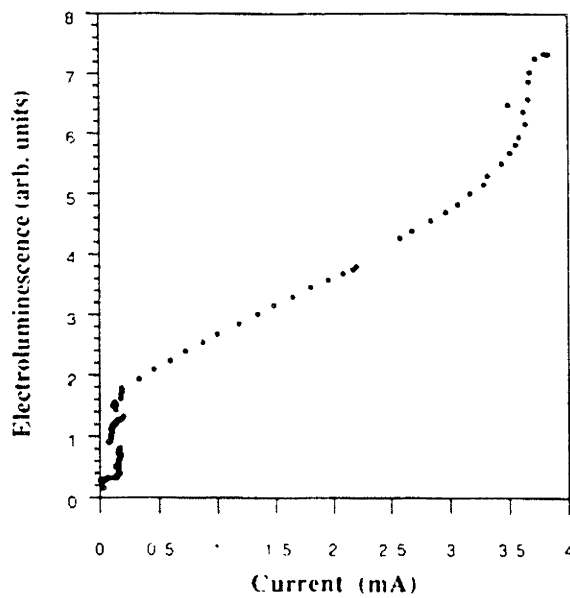


Figure 2.3 Electroluminescence of Polymer OLED Device [10].

Polymer based organic LEDs have shown significant advantages over molecular organic semiconductors in terms of their ability to form robust, homogeneous, and stable diode structures. They are also easier to fabricate and deposit. The quantum efficiencies of the first experimental devices fabricated at the Cavendish were limited to less than 0.05% due to failures at the polymer to metal interface hindering carrier injection.[10]

2.5.2 Electroluminescence in OLEDs

The exact details of the physics of light emission in organic materials are still being researched and reviewed. It is well known that trapped charged limited currents (TCL) are the dominant contributors to conduction in organic materials. Observation has shown that the optical properties of organic solids are primarily a result of the activity of small-radius Frenkel excitons [11]. Electroluminescence will be described in this section based on the device structure presented in [11]. A schematic of the OLED device is given in Figure 2.4. The structure consists of a transparent hole injecting indium-tin-oxide (ITO) contact, a hole transporting layer (HTL), an electron transport layer (ETL) consisting of Mq_3 , and an electron injecting metal contact made of a magnesium/silver alloy, MgAg. Mq_3 is a metal chelate complex, where $M=Al, In, Ga, \text{ and } Sc$ and $q=8$ -hydroxyquinoline.

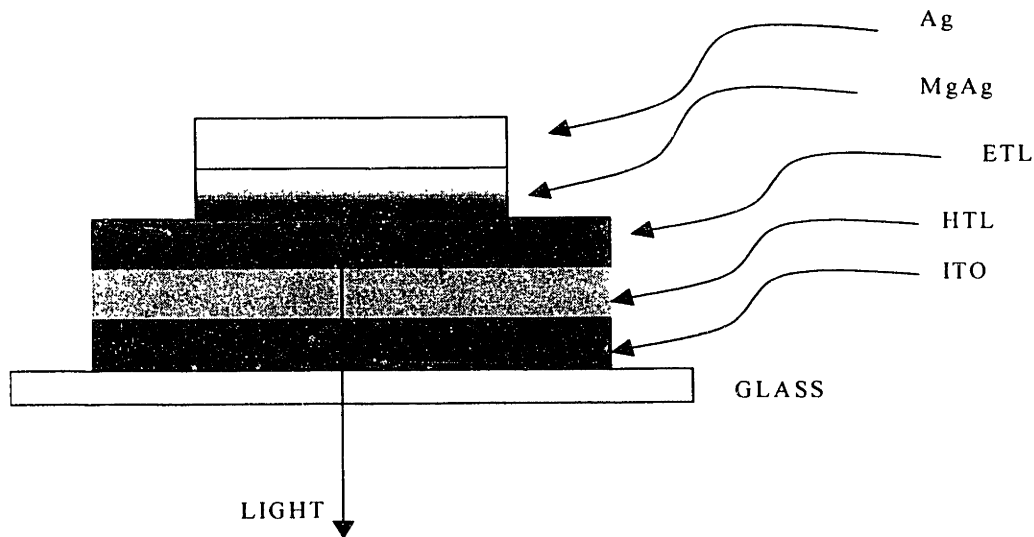


Figure 2.4 OLED Structure

It is assumed that electroluminescence is caused by the generation and radiative recombination of Frenkel excitons in the MgAg ETL layer. These excitons are formed by electrons, localized in traps in this region and holes injected from the HTL. As a result, radiative recombination primarily occurs near the ETL and HTL heterojunction, within a hole diffusion length. These results show that electroluminescence in molecular OLEDs is similar to the process that leads to luminescence in II-VI: metal complexes such as ZnS:Cu. The proposed energy band diagram illustrating the process of recombination in this organic structure along with the electron (E_n) and hole (E_p) quasi-Fermi levels under high current injection is shown in Figure 2.4.

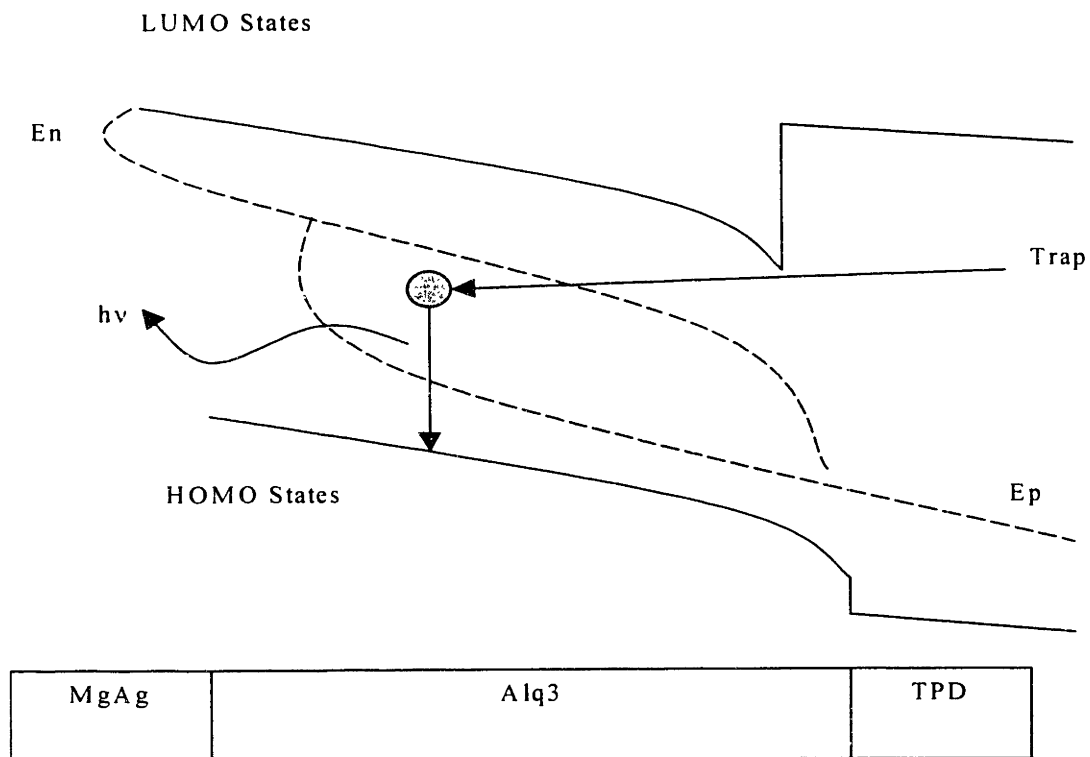


Figure 2.5 Schematic diagram showing trapped charge in the Alq3 (ETL) with a minority hole, to form a distribution of Frenkel electrons in the Alq3 band gap causing radiative recombination.

2.5.3 Carrier Transport in Organic Semiconductors

The conductive properties of most organic materials arise from the molecular arrangement of atoms in the material. This class of organic materials, displaying semiconductor and metallic properties, contain a system of sigma-bonded carbon atoms in the x-y plane of the lattice and a delocalized orbital of p-electrons in the z plan. This orthogonal orbital is called a pi-orbital and it consists of alternating patterns of single and double bonds all along the organic material's polymer chain. The localized pi-electrons in the double bonds can be excited to delocalized pi-electron states by the application of an electric field across the material. This unique molecular structure consisting of a delocalized pi-orbital system with pi-electrons that can move along the chain without a

significant change in energy is termed conjugation. The delocalised pi-electron system gives the polymer the ability to support positive and negative charge carriers with high mobilities along the polymer chain [12].

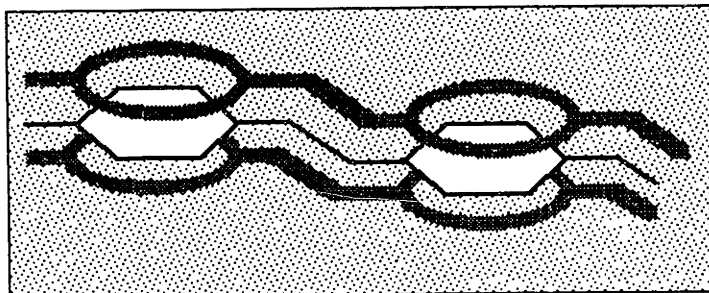


Figure 2.4 Delocalised pi electron cloud above and below the polymer chain.

Charge transport in polymer materials is different from mechanisms present in traditional inorganic materials due to the chain distortion of the polymer when charge is injected by an external field. Heterostructures, similar to inorganic Group III-V compounds, can be used to provide better control of carrier confinement, or for varying the offsets caused by injection electrodes [13].

2.5.4 OLED Displays

Organic materials are being investigated for use in a wide variety of applications including interconnects, displays, and transistors [14,15]. Overall, the primary focus for research in this field has been towards developing organic light emitting diode devices for use in flat-panel display applications. An OLED device is a heterostructure that consists of layers of electron/hole emitting and transporting layers. A forward bias across the device leads to minority carrier injection and photon emission. As previously stated, the exact physics of light emission in these devices is still being researched [8,11].

These devices achieve high brightness levels of greater than 100,000 cd/m², high contrast (100:1), full viewing angle, low operating voltage (5-15v), intrinsic response time of less than one microsecond. Despite challenges related to device stability and reliability, the rapid progress made in these areas of development have made OLED devices a viable technology in the display market.

Stability Issues

One primary limitation to the use of polymer organic materials in display applications has been the lifetime. Cambridge Display Technology has observed shelf-life of over 18 months and operating life times over 3,200 hours. Increasing the lifetime has been a major concern, especially in terms of increasing the marketability of these devices. Generally, commercial applications require shelf life time of at least 5 years and operating times of at least 20,000 hours [12]. Molecular organic materials offer longer lifetimes, however there is still a need to overcome this problem. Instability in an OLED device is caused by deterioration of the organic and contact electrode layers, and it is also dependent on the overall device structure. It has been shown that stability can be improved by doping the carrier transport layers, using injection contacts with better efficiency, and by using novel multilayer structures in the OLED device.[16]

Experiments show that some organic materials are detrimentally reactive with certain natural elements such as oxygen and water. Consequently, this stability issue creates a problem with processing and patterning organic materials. The details of the reaction and the exact process of degradation is still being investigated. Stability tests have shown that under certain environmental conditions, the performance of these materials can be enhanced. In particular, shielding of the polymer device from light

energy above the band gap of the polymer material can help to maintain the stability even in the presence of water vapor and oxygen. Thus, a primary objective in the design of polymer based OLED displays has been proper encapsulation of the material for protection against harmful elements.[13]

Color and Grayscale Capability

Considerable efforts have been made in investigating efficient techniques to produce OLED displays with full grayscale and color capability. The molecular composition of organic materials can be altered by doping and other methods to produce devices that only emit light in a narrow band of wavelengths [17]. Both molecular and polymer organic materials have demonstrated efficient light emission in all three of the primary colors.

There are five primary approaches that show promise in achieving full color displays: (1). The combination of selective color filters over a white-emitting organic material, (2) the implementation of red and green down-conversion phosphors with a single type of blue emitting device, (3) the use of three different microcavities to adjust the emission of a particular type of broadband organic emitting material, (4) the implementation of transparent organic layers that emit light at different wavelengths configured in a vertically stacked arrangement [18], (5) side-by-side arrangement of three organic layers that emit light at different wavelengths [19], similar to most full-color flat panel display applications such as LCDs.

Several fabrication and processing issues have been major obstacles to achieving efficient full-color OLED displays using the conventional side-by-side approach.

Organic materials are highly reactive to solvents, acids, and water, which are necessary ingredients to fully integrate different organic materials on a single substrate.

In the stacked OLED approach, layers of transparent organic materials are vertically stacked. Each layer forms a subpixel and is separated by a transparent metal contact electrode. Independent control of all three subpixels creates a structure that can be tuned to a particular grayscale or color. The brightness of each pixel can be varied by controlling the total current that passes through the stacked OLED structure. However, this scheme demands a more complex driver architecture with memory capabilities due to the sharing of contact electrodes that takes place in this structure.

2.6 Organic Light-Emitting Diode Model

Circuit models have been constructed based on device simulations and the resulting current-voltage characteristics of OLEDs. The analysis presented in this work is based on the model presented by Dawson et al in [20]. Figure 2.6 shows a schematic diagram of this circuit model. The OLED's multilayer composition consisting of organic electron/hole transporting and emitter layers create the diode structure.

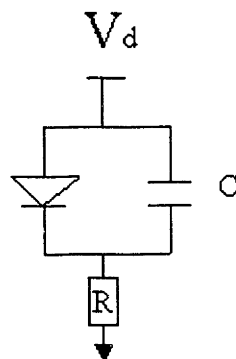


Figure 2.6 OLED Device Model

This diode has been approximated as a SPICE diode with the following forward bias current equation:

$$i = I_s \cdot A \cdot (\exp^{vd/Nv_t} - 1) \quad (2.7)$$

where I_s is the saturation current density, A is the active area of the OLED device, v_t is the thermal voltage (kt/q), vd is the diode voltage, and N is the emission coefficient. The following parameters were used in this particular model: $I_s = 10^{-7} A/cm^2$, $N=30$.

A parallel capacitance is added to the diode model to account for the capacitive nature of the organic layers sandwiched between metal contact layers on opposite sides of the structure. Molecular, as well as, polymer organic materials can be modeled by an effective capacitance of $25 nF/cm^2$. A series resistance of 80Ω is also present in the model. These estimates have proven to fit the actual device characteristics very accurately at high current levels. However, a more detailed analysis is needed to describe OLED device behavior in the low current regime. More discussion on this topic can be found in the design analysis presented in Section 3.

This model assumes that both polymer and molecular organic materials behave in the same manner in terms of conduction. Also, the high emission coefficient, N , suggests that a more accurate device model other than the diode model, such as field emission theory, for example, might be more appropriate.

2.6 Technological Developments in OLED Devices

Significant progress has been made in this area of OLED device research since the time of the first discoveries previously mentioned. Researchers have tried to enhance the electroluminescent properties of organic materials by trying to reach a better understanding of carrier injection and transport mechanisms in these structures.

Charge transport and device performance can be significantly improved by also choosing electron/hole transport layer interfaces that are similar in molecular structure and composition. Figure 2.7 shows an example of using a CN-PPV heterostructure for carrier transport. Due to the fact that the cyano group is electron withdrawing, it lowers the barrier to electron injection. This heterostructure layer also has a lower band gap energy than PPV, and thus, recombination will take place in this layer.

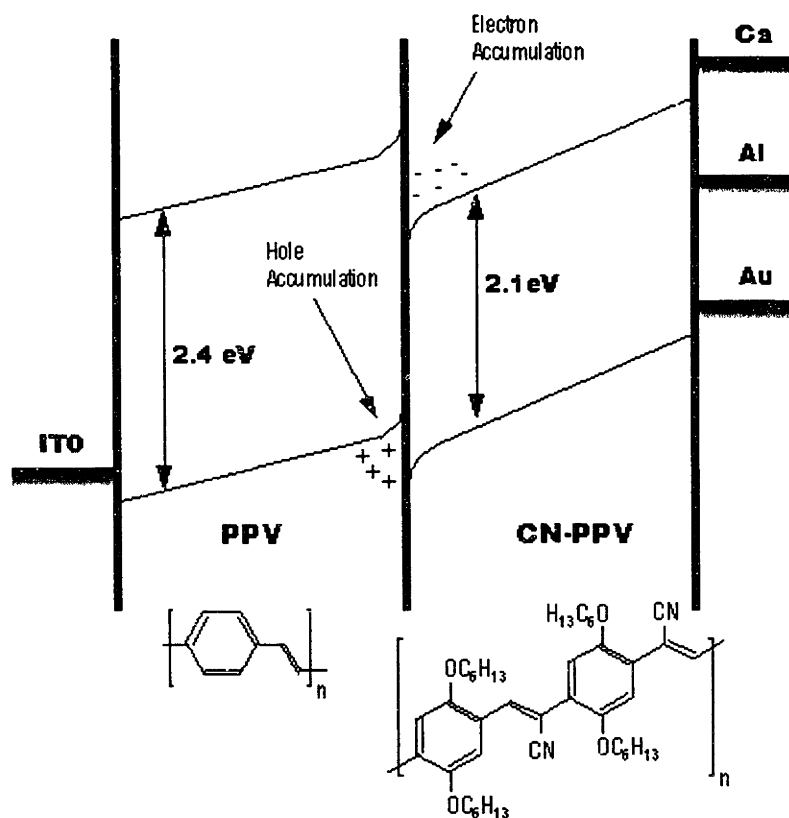


Figure 2.7 Organic CN-PPV Heterostructure

Recently, researchers at Cambridge Display Technology, Inc. have reported polymer LEDs with quantum efficiencies greater than 5%, turn-on voltages less than 3v, 180 degree---- viewing angle, and high resolution (5um pixel pitch). These devices also

exhibit excellent brightness up to several hundred cd/m^2 --- and switching speeds of less than 1 microsecond [12,13,21,22].

3. Display Addressing Schemes and Applications to OLED Displays

Organic displays are highly compatible with existing matrix addressing techniques that are commonly used in a majority of flat panel display applications. Pixels on the display are composed of individual OLED structures placed in a two dimensional array. Each pixel is controlled by orthogonal electrodes that are electrically isolated. Matrix addressing can be further subdivided into two approaches: passive matrix addressing, and active-matrix addressing. The various addressing approaches available add extra flexibility in the design of several aspects of the display architecture, including the pixel layout, the color/grayscale method, and the driver circuitry. The architecture will also be a determining factor in evaluating the power consumed by the display.

One of the key goals in the design of any portable display system is power minimization. It is desirable to keep power consumption under a tolerable level in these systems in order to extend battery lifetime and ensure circuit reliability. There are many components that contribute to power consumption on a display chip. Particularly for an OLED display, there will be a constant amount of power dissipated when a forward voltage bias is applied across the device. This component of power dissipation drives the electroluminescence process and is crucial to the overall performance of the display.

The addressing and driver circuitry controlling the operation of the display are the main contributors to power losses on the chip. In digital CMOS circuits, there are four components of power consumption: the dynamic power dissipation, the short-circuit power dissipation, leakage power dissipation, and static power dissipation.

$$P_{total} = \alpha \cdot (C_L \cdot V_{DD} \cdot V \cdot f) + I_{SC} \cdot V_{DD} + I_{leakage} \cdot V_{DD} + I_{static} \cdot V_{DD} \quad (3.1)$$

The dynamic power dissipation is due to the switching(f) of capacitive nodes (CL) in the circuit and is described by the first expression in Equation 3.1. The supply voltage is V_{dd} and the switching range is V . The switching range is typically equal to the supply voltage in digital circuits that operate on rail-to-rail switching. The α parameter found in the dynamic power expression is the switching activity factor and it represents the probability that a capacitive node will actually transition during the clocking period. For worst-case analysis, α is set to 1.

The short circuit component of power dissipation arises from losses occurring when there is a direct path for current flow from the supply voltage to ground. The leakage power component arises from device related affects such as subthreshold currents in MOSFET devices, and reverse-bias diode leakage, for example. The static power component is due to certain circuit related leakage, such as pre-charging, used to increase the speed of digital circuit.

By far, the dominant component of power loss in a digital CMOS circuit is due to dynamic power dissipation. This component contributes 90% of the total power dissipation, and therefore, the design analysis presented in this work, will focus on minimizing the dynamic power. The first expression given in Equation 3.1 shows that there are a number of factors to focus on in terms of minimizing the power loss in the chip due to dynamic switching. In most cases, it is necessary to increase the switching frequency for better resolution. However, this presents a trade-off in terms of an increase in power dissipation. On a display chip, depending on the addressing scheme and grayscale techniques being implemented, the switching capacitance, voltage swing, and supply voltages can be varied to achieve minimal power loss on the display chip.

The main goal of this feasibility study is to determine the best approach to designing an OLED display architecture that minimizes the overall power consumption on the display, while also maintaining good resolution, high brightness, and full color and gray scale capability. Each addressing scheme presented will be evaluated in terms of its overall effect on screen brightness, luminous efficiency, and power consumption.

The calculations presented in this section are based on worst-case conditions and are only estimates of the dominant components of the power consumption. The images being displayed are assumed to have high spatial frequencies. Consequently, the driver circuitry sees the maximum parasitic capacitance on the display chip. Table 5.1 contains a description of the variables that will be referenced throughout this section.

Table 5.1 Variable Descriptions for Power Calculations and Design Analysis

f	Display refresh frequency (typically 60Hz)
f_c	Column frequency ($N \times f$)
$M \times N$	Display size (Columns \times Rows)
V_{dd}	Supply voltage for digital CMOS circuits
$C_{g,n}$	Gate capacitance of NMOS device (min. size)
$C_{d,n}$	Junction capacitance of NMOS device (min. size)
K_{on}	Number of pixels in the ON state
I_d	Current of Organic Material
V_d	Voltage of Organic Material
$C_{wire,r}$	Row Line Wire Capacitance
$C_{wire,c}$	Column Line Wire Capacitance
C_{reg}	Capacitance seen by a clock driver from a dynamic register.
C_s	Dynamic Storage Capacitor (typically 50fF)
C_{pix}	OLED Capacitance

3.1 Passive Matrix Addressing

The most straightforward approach to designing an OLED display is the passive matrix addressing scheme as shown in Figure 5.1. In a passive matrix display, each pixel is directly selected by the orthogonal row and column electrodes. The luminance of the pixel is controlled by directly applying a forward bias applied across the device.

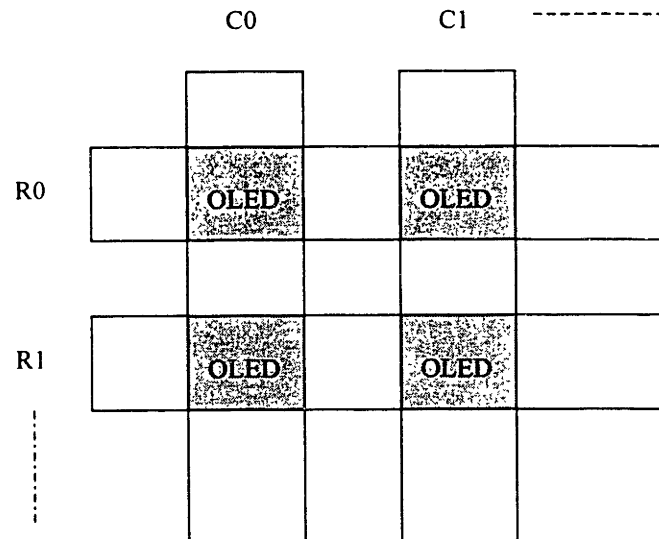


Figure 3.1 Passive Matrix OLED Display Schematic.

The following illustration assumes that the display is binary and monochrome, for simplicity. The OLED structure at each pixel is either ON (emitting light) or OFF (not emitting light). Each individual row is addressed in sequence and remains selected, while the remaining rows are unselected, for a period of time referred to as the row time, T_r . For a display operating at a refresh frequency, f :

$$T_r = \frac{1}{f \cdot N} \quad (3.2)$$

The columns can be selected in sequence or in parallel. The constraint is that the correct data must be sent to each pixel in the selected row within the period T_r , before the next row is selected.

For example, in order to turn-on the first row of pixels in the array, R_0 in Figure 3.1 is selected by driving its line voltage to ground and setting all remaining rows at $V_d/2$. The first column, C_0 , is driven to a voltage V_d . The turn-on voltage V_d appears across the OLED device and the pixel is directly driven to a particular luminance value. By driving both the row and column line of a particular pixel to $V_d/2$ simultaneously, a differential voltage of $0v$ appears and the device is turned off.

3.1.1 Color/Gray Scale Capability

There are several methods that can be used to achieve gray scale including amplitude modulation, and pulse width modulation. Amplitude modulation involves quantization of the voltage/current axis. The column driver outputs a level proportional to the pixel brightness desired for the entire row time, T_r . In the pulse width modulation implementation, the time axis is quantized into discrete levels and the pixel on time is varied as a function of the pixel brightness.

In order to implement grayscale in a passive matrix architecture, the most efficient means is by using the amplitude modulation drive scheme with direct digital to analog conversion to drive each pixel. A D/A converter is placed at each column to convert the eight-bit binary value to the appropriate analog signal that drives the column electrode for each addressed pixel. There are several options available for performing the digital to analog conversion, including switched capacitor and resistive string DAC architectures. One particular design presented in [23] implements a current amplifier

circuit scheme with output transistors that do not consume static power. The proposed scheme offers considerable area and power consumption reductions. The current mode output, as opposed to the conventional operational amplifier voltage output of commonly used DAC, is highly compatible with the OLED displays, where luminance is varied at each pixel by modulating the current through the device.

3.1.2 Pixel Addressing

Passive matrix displays are most conveniently addressed using the sequential row scanning scheme previously described. Shift registers are used to sequence through each row and DAC circuits are placed at each column to output data to each pixel. A display consisting of N rows requires an N -bit shift register. The dominant circuit components in terms of power consumption are the shift registers.

Static CMOS buffers are used as drivers to swing the high capacitance row and column lines from $0v$ to V_d . The OLED device is directly connected to the row and column lines, and therefore, when a pixel is turned ON the OLED capacitance adds a component to the parasitic capacitance contributed by the wire interconnections.

3.1.3 Power Consumption

The dominant components of power consumption in an organic display driven in a passive matrix addressing mode will be contributed from the shift registers in the row addressing circuitry, and driving the high capacitance row and column lines. As previously mentioned, the constant power consumed in operating the OLED devices is inherently a part of the electroluminescence process in these devices, and therefore, this component will not be considered in the power consumption calculations.

In general, the power consumed in addressing each row is proportional to the power consumed in driving the N-bit shift register. Each register is controlled by the same clock and the dominant power losses are in driving the high capacitance seen by the clock driver. The following expression describes these losses:

$$P_{reg} = (N \cdot C_{reg}) \cdot V_{dd}^2 \cdot f \quad (3.3)$$

The power consumed in driving the high capacitance row lines will depend on the area of the wire interconnections and the number of pixels in each row and column. Each row line is connected to M pixels. The following expression accounts for the losses in driving the row lines in a passive matrix OLED display:

$$P_{row} = (M \cdot C_{pix} + C_{wire,r}) \cdot V_d^2 \cdot f \quad (3.4)$$

The power consumed in driving each column will depend on the grayscale voltage value applied across each pixel and the current through the device. Under worst case conditions, each ON pixel is driven to the voltage value needed to achieve the maximum luminance. This power relationship can be expressed as:

$$P_{col} = (N \cdot C_{pix} + C_{wire,c}) \cdot V_d^2 \cdot f_{col} \quad (3.5)$$

The total estimate of the power consumed in driving a passive matrix OLED display is given by:

$$P_I = N \cdot P_{reg} + N \cdot P_{row} + M \cdot P_{col} \quad (3.6)$$

3.1.4 Design Analysis

There are various limitations and disadvantages to driving an OLED display in the passive matrix mode. Each pixel is directly addressed and maintains the desired

luminance for the entire row time, T_r , which is only a small fraction of the frame time. In other words, on a passive matrix display, there is high spot brightness at each pixel. However, the screen brightness and image contrast of the display are degraded. Each pixel is driven with a high current peak in order to reach the desired luminance level. Therefore, this design is limited in screen brightness and possibly luminous efficiency. In addition, every pixel in a given column is directly connected to its column line, and therefore, unselected pixels are affected by the driving waveform of a selected pixel. Consequently, cross talk and pixel corruption are concerns.

One of the most severe limitations to this approach is the inability to integrate storage components at each pixel to maintain the pixel's data throughout the frame time. For the applications intended for this OLED display design, the ability to store data at the pixel level can potentially reduce the power consumed in addressing and updating the display. If the image is not changing considerably from frame to frame, tremendous power savings can be gained by only driving the high capacitance row and columns of pixels that need updating.

Also, the transient analysis for OLED devices driven by a direct voltage is a concern for passive matrix OLED displays. Dawson et al have reported results relating to the transient response of OLED devices driven directly by a voltage source, analogous to a passive matrix addressing scheme.[15] Experiments were performed using a 0.1cm^2 OLED device directly connected to a voltage source. Plots of the current in the OLED structure at various voltage source values from 5.4 volts to 8.6 volts show that the step change in the voltage across the device instantaneously charges the parallel capacitance causing large current spikes to appear during the turn-on and turn-off period. This

group concluded that during turn-on, current is generated by the diode to cause recombination to occur in the transport layers of the structure. The luminance of the device increases steadily as carriers recombine until the injected charge reaches a stable state, determined by the applied voltage. A plot of the normalized light intensity of the structure at various applied voltages shows that the rate of increase in the light intensity during turn-on is slower for low drive voltages. These results are similar to previous published work on OLED device characteristics. These results can further be validated by consistency with the OLED device physics. In the low current regime, the filling of traps in the transport layers is much slower, and therefore, it takes longer for the device to reach the desired maximum light intensity output. This phenomena is a primary concern solely with passive matrix addressing because of the limited response time and on time of the pixel. It affects the ability to implement gray scale and the large current peaks at turn-on and turn-off can affect the power consumption.

3.2 Active Matrix Addressing

In addition to an orthogonal matrix of row and column electrodes, an active matrix addressing scheme incorporates a nonlinear device such as a transistor or diode to enhance the display's performance. In LCDs, the basic approach to active matrix addressing is to include one nonlinear device, usually a MOSFET transistor, at each pixel. The luminance of LC materials is varied by modulating the voltage applied across the structure. In non-emissive AMLCDs, the nonlinear device is used to control the flow of voltage to the high capacitance LC structure that stores the voltage level necessary to establish a certain luminance at the pixel. An OLED display is an emissive display, and therefore, a different active matrix structure is used to account for the fact that these

devices are current controlled and the OLED structure alone is not capable of storing the pixel data. The one transistor approach used for AMLCDs is not feasible in an active matrix OLED display because the device current leakage will affect the luminance of each pixel. Figure 3.2 shows a schematic diagram of the basic pixel architecture for an AMOLED display. A second transistor is added to control the modulation of current through the OLED device.

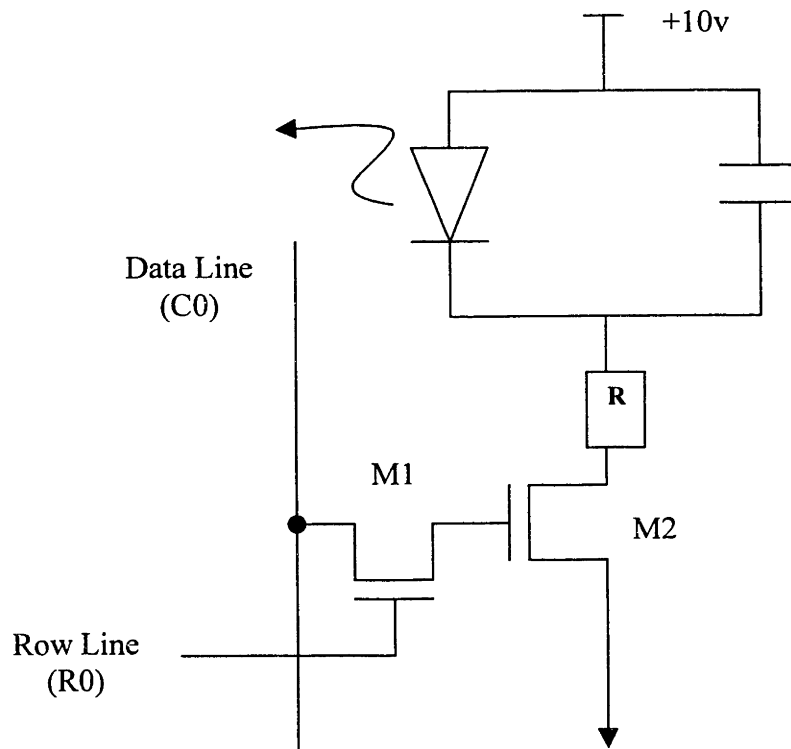


Figure 3.2 Active Matrix Pixel Schematic for OLED Displays.

Active matrix addressing has become the ideal approach for high quality displays. The control circuitry at each pixel improves the ON time of the pixel and the overall brightness and contrast of the display. The row lines are used to control the gate of the

control transistor (M1) and the data is passed to the series transistor (M2) providing a source of current for the device.

In this section, two different approaches will be evaluated in terms of their power consumption. The goal is to exploit the advantages of active matrix addressing by implementing storage at each pixel. Storage components will add the extra flexibility to be able to avoid redundantly addressing pixels on the display that are not experiencing any change in their luminance over a period of time.

3.2.1 Active Matrix OLED Display Implemented with Dynamic Pixel Storage

The schematic diagram of an OLED pixel integrated with a dynamic storage element is similar to Figure 3.2 with the addition of a storage capacitor, C_s , at the gate of the series transistor, M2. This configuration is similar to a memory cell in a DRAM architecture. The storage capacitor, C_s , is used to hold the gate voltage at the necessary level to establish the desired current through the series transistor. This current will drive the OLED device to a certain luminance value depending on the desired grayscale value.

3.2.1.A Color/Gray Scale Capability

D/A conversion can also be used in this display configuration to achieve grayscale. A D/A converter is placed at each column to convert the eight-bit binary value to the appropriate analog signal that drives the column electrode for each addressed pixel.

3.2.1.B Pixel Addressing

Typically, a row scanning addressing scheme is also implemented in an active-matrix display. The row drivers control the gates of the control transistor at each pixel. Column drivers are used to drive a particular voltage level to the drain of the control transistor where it is then passed to the storage capacitor, C_s , when the pixel is addressed.

When addressing the display in this fashion, most of the power is consumed in driving the gates of the control transistors at each pixel and charging the storage capacitance, C_s .

Each row is sequentially addressed using an N-bit shift register that outputs a voltage, V_{dd} , to sequentially turn on all of the gates of the control transistors in a given row. The column drivers charge the capacitance, C_s , at each pixel to the appropriate gray scale value.

3.2.1.C Power Consumption

Similar to the passive matrix case, the dominant components of power consumption in an organic display driven in a active matrix addressing mode will be contributed from the shift registers in the row addressing circuitry and driving the high capacitance row and column lines. However, in this configuration, the capacitive components being driven are smaller.

To evaluate the power consumed in driving the high capacitance row lines, the same relationship found in equation 3.4 holds. However, in this case the capacitance being driven depends on the gate capacitance of the control transistor (NFET) at each pixel. This gate capacitance is typically much smaller than the pixel capacitance.

$$P_{row} = [(M \cdot C_{g,n}) + C_{wire,r}] \cdot V_{dd}^2 \cdot f \quad (3.7)$$

The dominant capacitance seen by the column driver, will be proportional to the drain capacitance of each control transistor attached to a given column and the storage capacitance at the pixel being addressed. All of the remaining transistors are OFF and therefore the column wire is disconnected from the storage capacitance of these unselected pixels.

$$P_{col} = [(N \cdot C_{d,n}) + C_s + C_{wire,c}] \cdot V_d^2 \cdot f_{col} \quad (3.8)$$

Using Equations 3.3, 3.7, and 3.8, the total estimate of the power consumed in driving an active matrix OLED display implemented with dynamic storage is given by:

$$P_{II} = N \cdot P_{reg} + N \cdot P_{row} + M \cdot P_{col} \quad (3.9)$$

3.2.1.D Design Analysis

In the passive matrix approach, each pixel is directly addressed and remains in its ON state for only a fraction of the frame time. The active matrix approach with dynamic storage allows the pixel to remain in its ON state for the entire frame period. This design increases the screen brightness and the luminous efficiency of the display, because less electrical power is needed to achieve a certain light output from each OLED device on the display. However, leakage current components on the display can corrupt a pixel's data and degrade the image quality. This problem can be somewhat controlled by increasing C_s . However, there is a trade-off presented in terms of power consumption which is linearly related to C_s .

As previously discussed, implementing a storage element allows the possibility of exploiting the fact that there is little change in the image from frame to frame. In other words, the power consumption can be reduced under this condition by only updating pixel that have experienced a change in data. However, by using a dynamic storage element, the pixel data can only be saved for a finite amount of time depending on the value of C_s and the leakage current on the chip. As a consequence, additional overhead

circuitry is necessary to keep track of the pixels that need updating and those that need only a refresh.

In terms of the transient analysis of OLED devices in this configuration, there are a few issues worth noting. In the active matrix addressing mode, a constant current is provided by the series transistor, and therefore, there is no step change in voltage to cause a current spike during the turn-on and turn-off periods. As a result, the capacitance associated with the OLED device is not instantaneously charged and discharged. The transistor's current serves to both charge this capacitance and initiate luminance in the device. However, in this active matrix scheme the luminance rises more rapidly and the variations in the rate of change of luminance as the voltage decreases are less. The brightness of the device is improved by the continuous presence of constant current throughout the frame time.

There are a few concerns that must be addressed when implementing an active matrix drive scheme. One concern is the increase in the time constant of the diode's parasitic capacitance as the current decreases which causes a delay in reaching desired peak light intensities. Another concern is that during turn-off, the rate of decay to zero light intensity decreases as the voltage is lowered. As the capacitor discharges through the diode, the capacitor's time constant increases as the diode's turn-off resistance increases. These affects can impact the way in which active matrix addressing and grayscale are implemented in the display.

3.2.2 Active Matrix OLED Display Implemented with Static Pixel Storage

A schematic diagram of an OLED pixel integrated with a static storage element can be found in Figure 3.3. This configuration is similar to a memory cell in an SRAM

architecture. The cross coupled inverter, also known as a static latch, is used to provide static storage of binary data at each pixel. A high ('1') or low ('0') input voltage is passed into the selected pixel and the static latch drives the complement of the input voltage to the gate of the series transistor. Due to the binary nature of the static latch in this configuration, the OLED device is driven to a fully ON state (maximum luminance) or fully OFF. Static storage at each pixel greatly affects the grayscale capabilities of the display as discussed in the next section.

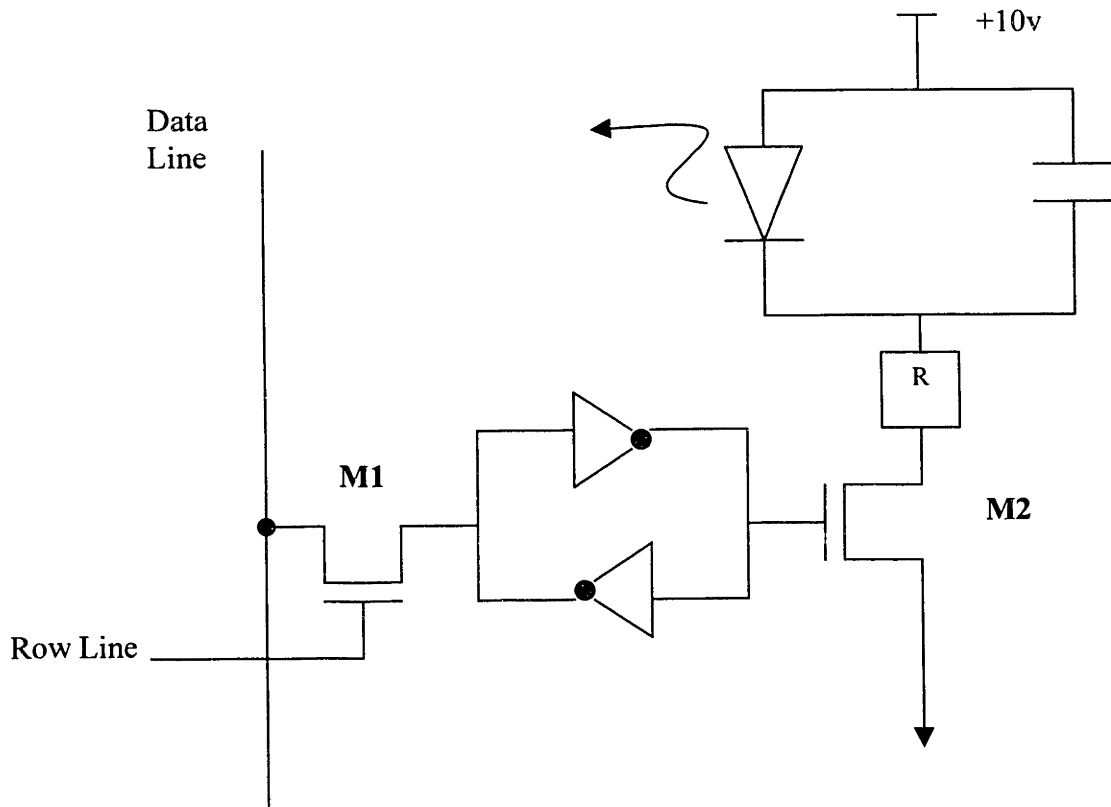


Figure 3.3 Active Matrix Pixel Schematic with Static Storage for OLED displays.

3.2.2.A Color/Gray Scale Capability

In the previous two designs, grayscale was conveniently achieved by driving the display with an analog signal that represented the appropriate voltage level necessary to achieve the desired luminance at each pixel. However, in this configuration the static latch acts a binary storage element. Under these conditions, other techniques such as pulse width modulation, and frame modulation are possibilities. Another option, is to place a static latch at each pixel for each bit of grayscale. Each design will have advantages and trade-offs in terms of power consumption, and pixel size. In pulse width modulation, extra overhead circuitry is necessary to keep track of the length of the pulse that is necessary to achieve the appropriate grayscale level. In frame modulation, the display refresh frequency, and therefore the power dissipated is driving the display, is effectively increased in proportion to the number of bits of grayscale.

Placing a static latch for each bit of grayscale at each pixel will increase the size of each pixel and possibly limit the resolution. However, this approach has the potential to offer great savings in terms of power consumption. In the other two schemes, even though static storage elements are used the data at each pixel must be refreshed because of luminance decay. By placing a storage element for each bit of grayscale, there is no need to refresh the pixels until an update is necessary. Implementing this approach will offer the greatest potential for minimizing the power losses associated with addressing and driving the display.

3.2.2.B Addressing/Driver Circuitry

In this approach, sequential addressing is not the most efficient means of addressing the display. The static latch will hold the data at each pixel indefinitely, and

therefore, it is only necessary to address the individual pixels that have experienced a change in their data. In most cases, the external system controlling the display exports data for each pixel every frame. It is quite feasible to program the external system to export information and data for the small percentage of pixels that have changed from the previous frame. This scheme will, however, require additional circuitry and memory for the purpose of keeping track of the location of pixels that need to be updated and the new pixel data. The trade-off between the power consumed in the overhead circuitry for this design and the power savings associated with minimizing the number of times the display is addressed must be considered.

Selecting only pixels that need updating leads to a random addressing approach to driving the display versus the traditional sequential approach, where all pixels are updated every frame regardless of the change in state of the pixel data. The address and driver circuitry for this approach will be similar to row and column address decoders commonly used in DRAM and SRAM memory circuits. To minimize power consumption, the decoders can be implemented using static CMOS AND gates or ROM circuits.

3.2.2.C Power Consumption

The dominant components of power consumption in this randomly addressed organic display with static pixel storage will be due to: driving the high capacitance row and column lines, and operating the overhead circuitry. Considering the fact that there is very little change in data from frame to frame, the power consumption can be further reduced. The power loss is reduced by the switching activity factor, α , which also represents the percentage of pixels on the display that will change from frame to frame.

Using static AND decoders for the rows and columns, the power consumption is:

$$P_{row} = [(M \cdot C_{g,n}) + C_{wire,r}] \cdot V_{dd}^2 \cdot f \cdot \alpha \quad (3.10)$$

$$P_{col} = [(N \cdot C_{g,n}) + C_{wire,c}] \cdot V_{dd}^2 \cdot f_c \cdot \alpha \quad (3.11)$$

The power consumed in driving data to each subpixel depends on the number of bits of gray scale, n , and can be expressed as:

$$P_{data} = [(N \cdot C_{d,n}) + C_{wire,c}] \cdot V_{dd}^2 \cdot f_c \cdot \alpha \quad (3.12)$$

Using Equations 3.3, 3.10, 3.11, 3.12:

$$P_{III} = N \cdot P_{row} + M \cdot P_{col} + n \cdot P_{data} + P_{overhead} \quad (3.13)$$

3.2.2.D Design Analysis

This architecture has a lot of advantages in terms of power savings and image quality. The desired luminance at each pixel can be maintained for extended periods of time. However, as the number of grayscale bits increases, the size of the pixel will increase and can potentially limit the resolution of the display. The row/column decoders and overhead circuitry can be operated at a much lower supply voltage to minimize power consumption as well. In the previous designs presented, the row and column addressing circuitry was operated at voltages needed to modulate current through the OLED device to implement grayscale, which can be up to 10v. However, in this design, the row/column addressing circuitry is being used to drive MOSFET control devices that operate at much lower voltage levels. Grayscale is implemented by storing each bit of data on a separate static latch. Spatial averaging (of the binary ON/OFF subpixels) performed by the human eye achieves the grayscale desired.

An added benefit of this architecture is the ability to limit the amount of data exported to the display. This achieves lower I/O data rates and limits the power consumed by the overall system in driving the high capacitance bus lines used to transport data from the external driving system to the display subsystem.

3.3 Power Consumption Evaluation and Comparison

In an effort to quantitatively compare the various display architectures discussed, this section will present typical values and estimates of the parameters mentioned in the power consumption analysis presented throughout this section. The values found in Table 3.1 are taken from the Parametric Test Results from a 0.5 micron CMOS process fabrication run performed by the MOSIS foundry. These values are typical for a minimum sized MOSFET devices. The PMOS device has a device width that is three times the width of an NMOS device. The λ parameter in Table 3.1 is set at 0.35 microns for this process. The display parameters for a typical VGA miniature display can be found in Table 3.2.

Table 3.1 MOSIS Parametric Test Results for 0.5micron process: Capacitance Measurements

NMOS Device		PMOS Device	
W _n	4 λ	W _p	12 λ
L _n	2 λ	L _p	2 λ
C _{g,n}	11fF	C _{g,p}	33fF
C _{j,n}	2.84fF	C _{j,p}	19.36fF
Metal1-Substrate		Metal2-Substrate	
31aF/um ²		16aF/um ²	
		Metal3-Substrate	
		11aF/um ²	

Table 3.2 VGA Miniature Display and Pixel Parameters

Display resolution	640x480
Display Size	16 mm x 12 mm
Pixel pitch	25 μ m
Pixel Capacitance (C_{pix})	0.2 pF
Pixel Current (I_p)	44 nA
OLED Operating Voltage (V_d)	10 v
Supply Voltage (V_{dd})	3.3 v
Bits of Grayscale (n)	8
Display Refresh Frequency (f)	60 Hz

The pixel current was estimated from measurements found in [29] to achieve a typical display luminance of 100 cd/m^2 at an OLED operating voltage of 10v. From the results found in [14], under these conditions the current density is approximately 7 mA/cm^2 . The pixel capacitance was found from the model presented in Section 2.6 for a pixel size of $20\mu\text{m} \times 20\mu\text{m}$.

For worst case analysis, the displayed images are assumed to have spatial frequency, and therefore, there is very high contrast and grayscale variation across the image. This assumption will increase the amount of switching of high capacitance lines on the display and will give a rough estimate of the maximum amount of power consumed.

Table 3.3 presents estimates of the maximum power consumed in addressing and driving a display based on the parameters in Tables 3.1 and 3.2 and the calculations presented throughout this section. The α parameter described in the power consumption analysis has been approximated as 0.1. Only 10% of the pixels on the display are expected to change from frame to frame.

Table 3.3 Power Consumption Estimate

Design Description	Power Estimate
Passive Matrix OLED Display <i>(Equation 3.6)</i>	178mW
Active Matrix OLED Display Implemented with Dynamic Storage <i>(Equation 3.9)</i>	95mW
Active Matrix OLED Display Implemented with Static Storage <i>(Equation 3.13)</i>	0.12mW+P _{overhead}

As shown in Table 3.3, the power consumed by an OLED display can be greatly reduced by implementing an active matrix architecture with static storage, under the condition that the power consumed by the overhead circuitry is kept at a minimum (<90mW). Typically the overhead circuitry would consist of an inexpensive, low-voltage DRAM memory circuit to hold the data from the previous frame for comparison with the current frame's data.

4. OLED Microdisplay Design Implementation

The active matrix display architecture with static storage was chosen for implementation in this work. After a review of the design considerations and the architectural trade-offs in terms of power consumption and feasibility, this implementation showed the most promise. The basic goal is to implement a low-power display architecture, including driver and addressing circuitry, with the capability of displaying grayscale images with minimal addressing of data to the display. Ideally, the display should only be addressed when it is completely necessary to update the pixels that have changed. This implementation avoids wasting power in addressing pixels or displaying portions of the image that are static. A block diagram of the overall display system can be found in the Appendix. This section will describe the display architecture and logic design.

4.1 The Display Array and Pixel Architecture

The display array for this prototype display design consisted of 64 x 64 array of pixels. Each pixel, or triad, contains 3 identical subpixels to achieve 8 levels of grayscale. A schematic diagram of the subpixel can be found in Figure 4.1 including the dimensions of the MOSFET devices. Each subpixel contains a row-control transistor (M1), a column-control transistor (M2), a static latch, and a current-sourcing transistor (M3). The OLED device model is also included for clarity. The column-control gates of all the subpixels within the triad are connected to the column line and the row-control gates to the row line. Three separate data lines are routed to each triad and connected to subpixels 1, 2, and 3 respectively within each triad.

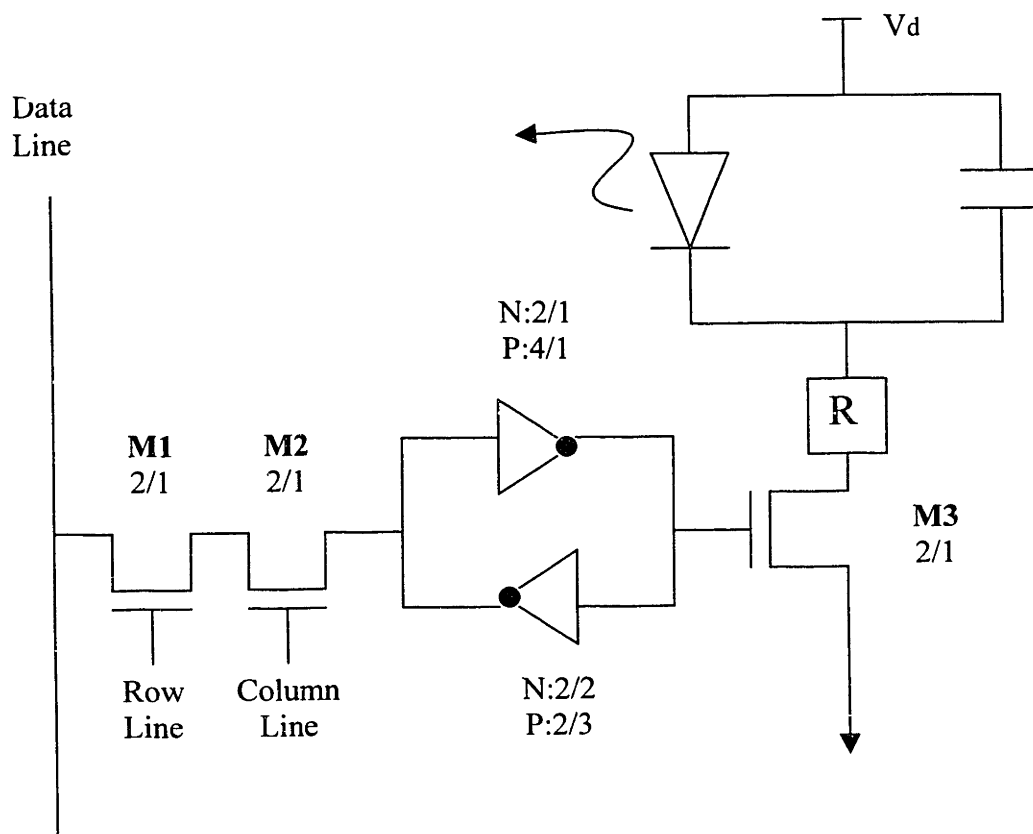


Figure 4.1 OLED Display Pixel Design

Once the row and column lines are driven high simultaneously, the data carried on each of the three data lines is read into each respective subpixel and the static latch is flipped. The sizing of the transistors in the static latch and the row/column-control transistors are critical to the operation of this circuit, similar to the operation of a SRAM memory cell. The static latch drives the current-sourcing transistor to the ON or OFF state. When the transistor is turned ON, a path for current is created and the OLED device emits light; turning OFF the transistor breaks the path for current and the device does not emit light.

Each pixel in the 64 x 64 array is designed to fill an area of approximately 80 microns x 60 microns to yield the typical display aspect ratio of 4:3. All three subpixels are compacted into this area with minimum spacing between each to avoid leakage in the silicon substrate caused by light reflected back into the display. The drain of the current-sourcing transistor has been contacted the top metal layer, where the organic material will be deposited.

4.2 Addressing/Driver Circuitry

As previously stated, this display architecture is very similar to a DRAM/SRAM memory circuit, and therefore, each pixel can be selected (addressed) and its data loaded into the display array using similar peripheral circuitry as implemented in these memory circuits. In order to avoid adding excessive memory and overhead circuitry to keep track of the addresses of pixels needing an update, an internal address counting scheme has been implemented. The details of the logic design of the addressing and data driving circuitry is outlined in this section.

4.2.1 Row/Column Decoder and Driver Implementation

In order to select a pixel for updating, the row and column decoders accept the location or address of the pixel. This address is specified in terms of the number of the row line, where the pixel resides and likewise for the column line. A 6-bit decoder is implemented for both the rows and columns in order to address all 64 lines in each direction. Conventional AND decoders have been implemented each consisting of 64 6-input static CMOS AND gates. The use of static gates that consume infinitesimally small amounts of power.

Figure 4.2 shows a diagram of one line of the row/column decoder and driver circuit. In addition to the 6-input AND gate, there are 2 transistors and a cascade of buffers attached to the decoder output. The two transistors are controlled by an enable signal (\overline{EN}) sent by the external control system. The enable signal alerts the display to the need to refresh the image. If $\overline{EN} = '0'$, the decoder's output is passed to the display; otherwise, the PMOS device is turned OFF and the NMOS device drives the row line to 0v to isolate the pixels in the array from the addressing circuitry and data lines during the static state of the displayed image. This additional control prevents pixels from being addressed prematurely by false transitions on the row and column lines.

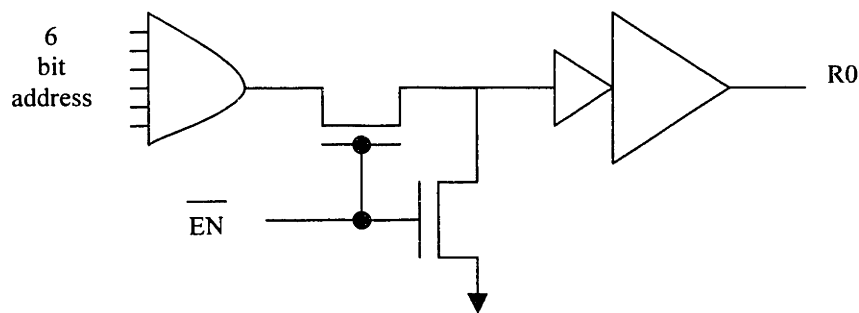


Figure 4.2 One line of the Row Decoder and Driver Circuit.

In most memory circuits, the row and columns are pre-charged high to increase the addressing speed. Consequently, the dynamic and static power consumed by these circuits are much higher. In this design, the row and column lines are pre-charged low to take advantage of the fact that the displayed image is not changing rapidly from frame to frame. As a result, fewer transitions on the row/column lines are necessary and speed is not an issue. A cascade of buffers are included at the output to help drive the capacitive row/column lines.

4.2.2 Address Counter Implementation

In an effort to minimize the overhead circuitry and control needed to implement this design architecture, an address counter was used to allow the display to keep track of the location of pixels on the array needing an update of data. The address counter was implemented with a commonly used 12-bit counter.

4.2.2.A Functionality

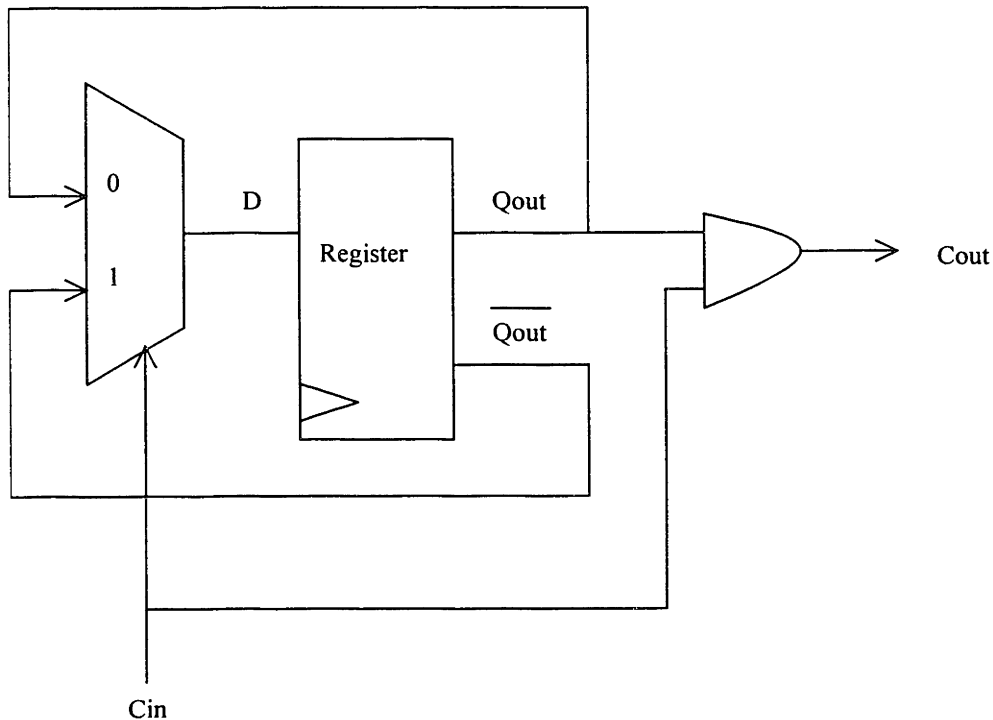


Figure 4.3 Block Diagram of Address Counter Bit.

A block diagram of one-bit of the counter can be found in Figure 4.3. The upper 6 bits of the counter are routed to the row decoder circuit and the lower 6 bits are routed to the column decoder. As the counter increments from 0 to 4095, it effectively points to

each pixel in the array in a raster scanning fashion. The counter is designed to be controlled by the same clocking frequency as the external system's control circuit that is responsible for comparing the previous and current frame's data for the display. Therefore, this external control system and the address counter work synchronously. As the external control checks each pixel and determines whether or not an update is necessary, the address counter carries the address of the pixel being checked. A pass transistor is placed at the output of each counter bit. When the high enable signal, along with the new pixel data, are sent to the display, the current address in the counter is sent to the row/column decoder and the pixel is selected and updated. For the following illustration assume that the display has been completely refreshed and a new image is being displayed. The clock frequency of the counter and external control will be equal to:

$$f_c = f \cdot M \cdot N \quad (4.1)$$

For $f=60\text{Hz}$, $M=N=64$, the clocking frequency is roughly $f_c=245\text{KHz}$, for simplicity. After the first frame has been loaded, the counter resets and the external control begins to compare the second frame's data with the first frame, starting with the first pixel in ROW0 (first row) and COL0 (first column) in the display array. Each row/column is referenced as ROW0, ROW1.....,ROW63 from top to bottom for the rows and left to right for the columns. The second frame requires a refresh for the last five pixels in ROW0, for example. At the rising edge of the 59th clock cycle for this frame, the enable signal will go high and the address counter will output 000000111011 (MSB...LSB). The upper 6 bits (000000) are being routed to row decoder and the lower six bits (111011) to the column decoder. The pass transistor turns ON and the row/column

address is passed and decoded to drive ROW0 and COL58 high as desired. The enable signal remains high for 4 more clock cycles. At the beginning of the 65th clock cycle the enable signal is driven low and counter contains 000001000000 pointing to the next pixel in ROW1, COL0, which does not need an update. All of the row and column lines are driven low at this point. The counter and external control continue to synchronously count and compare the pixel data while the display remains in a ‘sleep’ state until a refresh is necessary.

4.2.2.B Power Consumption

This address counter implementation consumes much less power than a design that uses a memory circuit to store the addresses of pixels that need updating. The dominant components of power are contributed from the driving of the row/column decoder address lines connected to the inputs of the AND gates. The clock only drives 12 dynamic registers, and therefore, the power consumed in clocking the counter is insignificant. A rough estimate of the power consumed in operating this address control circuit can be expressed as:

$$P_{overhead} = [C_{g,n}(k_1 \cdot 2^{(k_1-1)} + k_2 \cdot 2^{(k_2-1)})] \cdot V_{dd}^2 \cdot M \cdot N \cdot f \cdot \alpha \quad (4.2)$$

where k_1 is the number of bits needed to address the N rows, and k_2 is the number of bits needed to address the M columns. Using the parameters given in Section 3, $P_{overhead}$ is approximately 1.64mW.

4.3 Data Entry and Routing

In most flat panel display designs, such as LCDs, the display data for all the pixels in a particular column is routed to each respective column in a parallel fashion using shift registers and latches. This mode of operation increases the performance of the LCD by extending the ON time of pixels, and thus, improving brightness, and increases the overall efficiency of the addressing circuitry. The OLED display architecture presented in this work is not constrained by the limitations of LCDs in terms of addressability. In terms of displaying nearly static images, OLED displays with static storage are not limited by the time constraints imposed on LCDs. Pixel data is only routed when a refresh is necessary, and therefore, only one data port is required in this design.

Within the display array, all of the data lines of the first subpixel in each triad are connected together across the entire 64 x 64 array of pixels, and likewise for the second and third subpixels. This network creates three continuous lines of data throughout the array and eliminates the need to use separate column data drivers for each column in the display. A control circuit consisting of tristate buffers is placed at the top of each column as shown in Figure 4.4. These tristate buffers consist of pass transistors that connect the external pixel data to the three data lines extending from each column. The gates of the pass transistors are controlled by the column decoder output. Once a pixel is selected in a particular column for update, this column data selection circuit connects the external data to the data lines in the selected column while disconnecting all other lines. As a result, the capacitance seen by the data drivers is significantly reduced and the display has the capability of controlling and routing the external data as needed. This effective

decrease in capacitance lowers the power losses due to driving the data lines on the display chip.

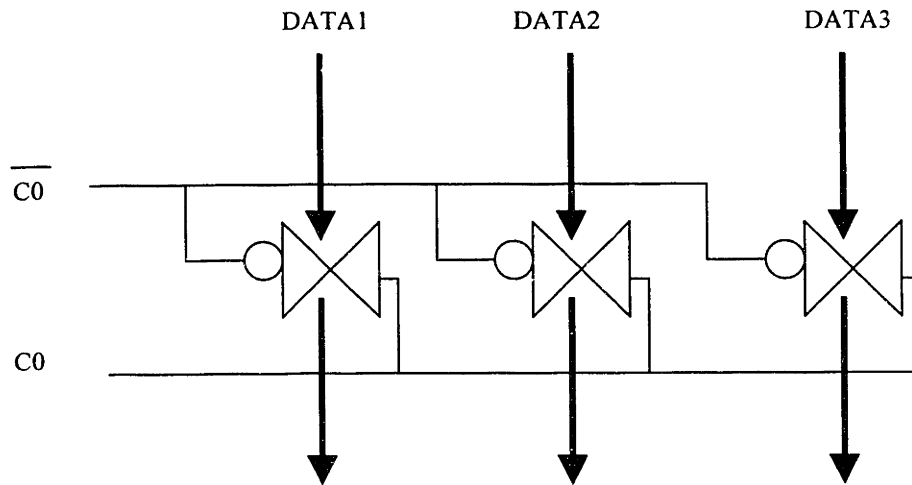


Figure 4.4 Column Selection Circuit (One Column Represented).

4.4 Performance Evaluation

The results obtained from the simulation and testing of the design presented were favorable overall. The design presented achieved the functionality and power consumption goals as expected. However, extensive testing of the display chip was limited by the evaluation tools available. Each component of the overall display system was tested and evaluated in terms of average power consumption. One main concern of this design is that the display system is not completely independent of the overall external system.

4.4.1 Pixel Architecture

The power consumed during the ON state of each pixel was tested under the condition that the data for each subpixel changed at the same time to cause the current to increase from 0 to its maximum value. The average power was measured as 0.2mW. For a 64 x 64 array, the total average power will be approximately 819mW. This power

consumption estimate is inherent to the operation of OLED devices. In this prototype design, a very conservative operating voltage of 10v was used for the OLED devices on the display. However, the power can be reduced by using currently available organic materials that operate at a much lower voltages.

The turn ON time of pixels was on the order of a few nanoseconds. When turning OFF the subpixels the fall time was slow. The current decreased to half of its maximum value after a 6.5 us delay. As discussed in Section 3.2.1.D, the slow turn OFF time of OLED devices is still a technological challenge. However, with a 60 Hz refresh frequency yielding a frame period of 17ms, this delay can be tolerated.

4.4.2 Addressing/Driver Circuitry

The address counter and row decoder consumed an average of 4mW of power, under worst case conditions, where each line is being addressed every cycle and the enable signal is always high. This measurement is slightly higher than the values obtained from the calculations, because the HSPICE simulation accounts for all components of power including static components. However, the hand calculations give a good estimate of the amount of power consumed in this implementation relative to the other two designs. The simulation was performed at a clock frequency of 250KHz. A 0.2pF capacitance was added at the output to simulate the capacitance of the row and column lines. The rise and fall times of the row and column lines was approximately 10ns. The performance of this combination of circuitry was very good. For an actual display, only a small fraction (α) of the row and column lines are being addressed during the frame time. During the time that a row/column line is not addressed, the main source of power consumption is from the address counter and this is minimal (0.4mW).

5. Conclusions and Future Work

The display architecture design plays an important role in the development of OLEDs as a viable flat panel display technology. One of the primary obstacles to be overcome in the design of any high performance flat panel display is power consumption. In the case of OLED displays, a forward bias voltage across the device causes a current to flow through the organic material to initiate light emission. The operating voltage and current of OLEDs are device properties that introduce a constant loss of power for the display system. The display driver electronics and system control circuitry, however, are components that can be efficiently optimized by the display designer to lower the overall power consumption of the system. Driver circuitry contributes a significant amount of power loss to the display system, and therefore, optimization of these components deserves consideration.

In this work a prototype OLED display has been designed and implemented. This display has been targeted to miniature display applications functioning on images that are primarily static with minimal change from frame to frame. These displays are fabricated on a silicon backplane and driven by control circuitry imbedded directly under the display panel. This targeted application is very significant considering the fact that miniature displays, including head-mounted projection displays, etc., have introduced a whole new market within the flat panel display industry.

The display architecture presented in this work has taken advantage of both system and circuit design techniques to achieve a greater reduction of power losses on the display chip. The key parts of the design that minimized the power consumption of the display were the use of static storage, active matrix addressing, and a simple low-power

address counter. An active matrix addressing scheme has been used to increase overall performance. Active matrix is commonly used in high performance LCDs and is very compatible with an OLED display. In general, active matrix addressing extends the operation of each pixel for the entire frame period. In this manner, a brighter image can be displayed. Also, by using an active matrix, the routing of data to each pixel can be controlled by MOSFET devices that operate at a much lower voltage than the OLED device in most instances. CMOS processes have already moved towards the 1.8v operating stage which is far lower than any OLED device operating voltage presented in the literature. The active matrix gives an added advantage over the more direct passive matrix in terms of being able to add performance enhancing circuitry, such as memory devices, at each pixel element.

Each pixel has been designed using a static storage element. With the use of static storage, portions of the displayed image that remain constant over long periods of time can be kept untouched by the addressing circuitry. In other words, the use of a static latch adds a 'self-refresh' property to each pixel. In this manner, the addressing and driver circuitry is only responsible for updating certain pixels each frame rather than the entire pixel array. Matrix addressing introduces a considerable amount of switching on high capacitance nodes, including row/column lines, in the display, which greatly contributes to power loss. Therefore, by reducing this switching using static storage, the overall power consumption of the display has been reduced. In addition, the 'self-refresh' property of each pixel, has reduced the amount of information that the external system must export to the display. The external control sends a display enable (EN) signal as a flag and the data pertaining only to pixels that are in need of update. The

location of pixels that have experienced a change in their data is kept by an address counter that operates synchronously with the external control system. During the time that the display is not in need of a refresh, the system is kept in a 'sleep state' in which no switching occurs and all row/column lines are grounded.

There are several improvements to be made to this design to enhance its performance. The pixel design achieved the desired functionality, however, the slow decay to the OFF state of the device is a limiting factor to the pixel time and the achievable resolution of the display. Additional circuitry can be added to the pixel to help discharge the OLED device and drive the current to 0. The use of static storage, as previously mentioned, offered savings in terms of power losses. Consequently, the most feasible means of implementing grayscale and color involved a dividing each pixel into subpixels in proportion to the number of grayscale bits, typically 8 bits. Using the side-by-side pixel approach, as the number of subpixels increase, the required size of the pixel also increases also affecting the achievable resolution of the display. Research effort is now being directed toward three-dimensional CMOS technologies where integrated circuit devices are stacked vertically. If the development of this new technology advances as expected, OLED displays would be a useful application. Ideally, subpixels would be vertically stacked and contacted to the upper surface of the chip for connection to the organic material.

As resolution increases and the pixel array increases, the speed requirements will also become an issue for consideration in the design of an OLED display. In this work, speed was not a primary issue considering the moderate array sizes used in the discussion and the low display refresh frequency of 60 Hz. However, as the array size increases, the

address counter, decoder circuits, and other peripheral circuits will require further optimization and design innovation to achieve high speed performance.

The main challenge to implementing the active matrix addressing scheme with dynamic storage was the affects of leakage currents on the storage capacitor. Further investigation can be performed to evaluate the issues involved in implementing low leakage storage components. If the affects of leakage are minimized, then the ‘lifetime’ of the dynamic storage capacitance can be extended. As a result, the dynamic implementation can be controlled to refresh the display once every 10, 100, or 1000 frames rather at the normal 60 frames per second. The overall savings in terms of power consumption and the trade-offs involved in incorporating overhead circuitry for the additional functionality should be evaluated.

This first pass design has not taken into account variations in device characteristics across the display due to fabrication process variations, etc. Variations in the threshold voltage of the current-sourcing transistor used in the pixel design can affect the current density in the device and the luminance of each pixel. These variations can affect the design considerations and the choice of implementation as well.

The overall functionality and success of the low power design approach presented in this work is highly dependent on the operation of the external control system that the display subsystem is connected. This design assumes that the external control is capable of storing the previous, as well as the current frame, of the image and determining the need for refresh. In the wake of ‘system on a chip’ architectures, this is quite feasible and realistic. Hardware and memory circuits present with the external control could possibly be partitioned and dedicated to manipulating the display’s image data at a minimal

expense to the overall system's performance and power consumption. Low-voltage, cheap DRAM circuits, circular buffers, and other memory architectures are readily available and these are all possible solutions to the necessity for overhead circuitry to determine the refresh needs of the display.

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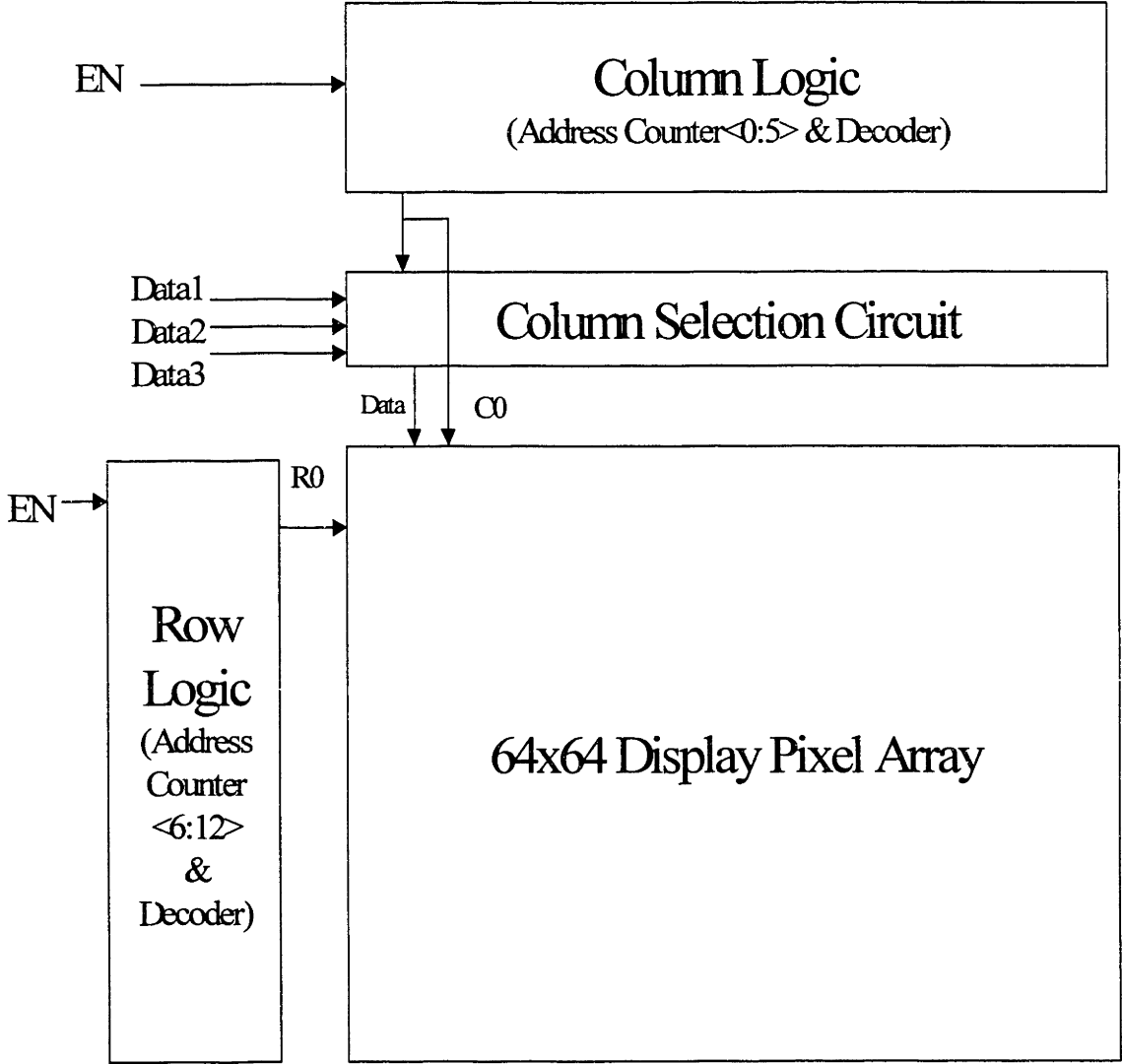
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7. Appendix



THESIS PROCESSING SLIP

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