A Pixel-Level A/D Converter For the Imaging Array of an Advanced Interferometer

by

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Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Electrical Engineering and

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

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Abstract

The objective of this thesis is to investigate the feasibility of pixel-level analog-to-digital conversion as a solution for the imaging array of the advanced interferometer project at Lincoln Laboratory. Six different pixel-level analog-to-digital conversion methods are examined. Four of the conversion methods are discarded after preliminary analysis because accuracy requirements cannot be met given the high-speed and area constraints. Two of these conversion techniques (voltage-to-frequency and sigma-delta) are further analyzed because they show promise to fit in a 60 μm × 60 μm area and be able to perform 14-bit, analog-to-digital conversion at frame rates of 5000 Hz. As a result of the analysis, the voltage-to-frequency converter is also discarded because comparator inconsistencies degrade the accuracy below specifications. The sigma-delta converter individually meets the imaging array requirements, but high power supply dissipation, large parasitic capacitance and noise introduce by other converters make pixel-level sigma-delta conversion impractical with current technology.

Thesis Supervisor: James Roberge
Title: Professor of Electrical Engineering

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1.0 Introduction

1.1 Background

Recently, the Sensor Technology and Systems group at Lincoln Laboratory has been investigating different methods to better measure weather sensing data. One project currently being investigated is called the geostationary advanced satellite (GAS) project. The purpose of the GAS project is to design an advanced interferometer to measure weather-sensing data that includes temperature profiles, humidity profiles, and chemistry constituents of the atmosphere.

An interferometer works by using a set of stationary and moving mirrors to capture a series of images that have undergone optical interference. Each of the images in the series has a different interference ranging from completely constructive to complete destructive interference. Further processing of these images, by using methods such as Fourier transforms, leads to the weather-sensing data desired.

An imaging array is used by the interferometer to capture the images and store them in memory. The array is comprised of numerous pixels, each with a single detector that transforms the incoming photons induced by light into a current (Figure 1.1). The current from the detector is stored as charge on a capacitor. After a fixed integration period, the voltage across the capacitor of each pixel is digitized and stored in memory.

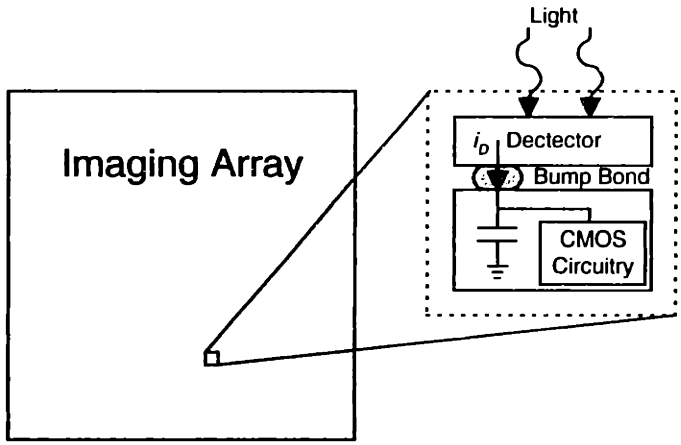

Figure 1.1: Imaging Array Using Bump Bonding

In an imaging array, there are two main ways the detector can be integrated with the rest of the CMOS circuitry. The detector can either be bump bonded to the CMOS circuitry or a CMOS photodector can be used. A bump bond is a small conductor that is used to transfer the output current from the detector to the CMOS circuitry below. A bump bond is necessary for detectors that cannot be built in silicon. Bump bonding is needed for the imaging array used for the advanced interferometer project because the detector must be made from specialized material.

The imaging array for the advanced interferometer project has other stringent constraints and requirements. The project has a coverage requirement that can be met using a 256×256 imaging array. The application is designed for very high light intensity situations. Under maximum light intensity, each detector of the imaging array is designed to produce an output of 10^{12} electrons per second. The interferometer is located on a geostationary satellite. In order to receive the required ground resolution a $60\ \mu m \times 60\ \mu m$ pixel size is needed. The maximum number of electrons per second produced by the detector and the maximum number of electrons a capacitor can hold before breaking down (well depth) determine a lower bound on the number of images captured per second (frame rate). If the frame rate is smaller than the lower bound, the capacitor could saturate. A $60\ \mu m \times 60\ \mu m$ capacitor can have a well depth of around $2 \times 10^8 e^-$.

Therefore, for the interferometer application, a frame rate of a least 5000 Hz ($\frac{10^{12}\frac{e^-}{s}}{2\times10^8 e^-}$) is needed to avoid potential erroneous results from saturated capacitors. However, the same performance could be attained with a lower frame rate using a higher precision analog-to-digital converter (ADC) if there were no well depth limitation on the capacitors.

Shot noise is inherent in any imaging array. Shot noise is introduced because for a fixed light intensity, the rate at which photons hit a sensor is not constant but the result of a Poisson process. The result of the noise is a fundamental limitation on the signal-to-noise ratio (SNR). The imaging array of the advanced interferometer project is shot noise limited to a SNR of 83 dB.

For the advanced interferometer project to be a success, the incoming current stored on the detector capacitors must be digitized in a way such that most of the 83 dB SNR is preserved. If an ADC is used that does not have enough quantization levels, quantization noise will lower the SNR substantially. In contrast, if an ADC has too many quantization levels then the SNR improvement is minuscule compared to the cost of the increasingly complex ADC. A 14-bit ADC is the simplest ADC that has enough quantization levels to preserve most of the SNR. Table 1.1 lists a summary of the imaging array requirements for the interferometer. A more in-depth derivation of the requirements is given in Reference [1].

Table 1.1: Imaging Array Requirements

256 x 256 pixels
10^{12} maximum flux
60 μm x 60 μm pixel size
5000 Hz frame rate
14-bit ADC

1.2 Motivation and Problem Statement

Imaging arrays differ in the order and manner in which the analog voltage across the capacitor of each pixel is digitized and read out to memory. Suitable imaging arrays depend on the application. The current, standard analog-to-digital (A/D) conversion method either senses or

multiplexes each capacitor's voltage to off-chip ADCs. An example of a current-imaging method is the charged coupled device (CCD). During readout, the CCD uses an analog shift-register to shift the charge packets, produced by the detectors during integration, off-chip. The charge packets are then, in turn, converted to a digital signal using one or several high-speed ADCs. For example, if 100 off-chip ADCs are used to digitize a 256 × 256 CCD imaging array that operates at 5000 Hz frame rates, each ADC would have to operate at over 32 million conversion per second.

For the Lincoln interferometer project, the standard imaging method is problematic, because due to the large array size and high frame rates, too many analog voltages have to be multiplexed to off-chip, high-precision ADCs. The number of off-chip ADCs necessary for this method to succeed is not feasible. Also, having analog signals communicating over the many output pins is a logistical nightmare and a potential source of noise from crosstalk and other phenomena. Thus, there is a need for a different imaging method.

One potential solution for the interferometer imaging array is to have a separate, very small ADC at each pixel. Each ADC digitizes the voltage across the capacitor of a single pixel and then a scheme is implemented to multiplex the value to memory. The conversion rate for each ADC is the same as the frame rate of the imaging array. In contrast to operating an ADC at possible millions of conversions per second, operating an ADC at frame rates of thousands of conversions per second is practical. Pixel-level conversion is also scaleable to larger arrays and eliminates many sources of noise associated with current methods, such as analog sensing and charge transfer. Another benefit of pixel-level conversion is that some types of pixel-level converters, which will be explained later, do not have well depth limitations on the capacitor, and therefore, the imaging array could run at lower frame rates. This modification would improve the SNR of the imager.

Along with the benefits of pixel-level conversion, there are some stringent constraints and obstacles that must be overcome. Each ADC must fit in a very small area, 60 μm × 60 μm

for the interferometer project. A readout scheme needs to be established to move the digital pixel voltages off the array. Also, noise, such as fixed pattern noise (FPN), must be reduced to a point below specifications.

The objective of this thesis is to investigate the feasibility of using on-chip, pixel-level A/D conversion as a solution for the imaging array of the advanced interferometer project at Lincoln Laboratory. The methods of pixel-level conversion discussed in this thesis do not only apply to interferometry, but can be applied to many other areas such as robotics, digital cameras, and surveillance equipment.

1.3 Previous Work

There has been some investigation of imaging arrays using on-chip, pixel-level conversion. A research team from Stanford University has built imaging array prototypes that used pixel-level sigma-delta ADCs[2,3] and pixel-level single-slope ADCs[4]. Woodward Yang, a Harvard professor, built an imaging array prototype that used pixel-level, voltage-to-frequency (V-to-F) ADCs[5].

The research team from Stanford University has been investigating pixel-level sigma-delta ADCs since before 1994. Their first imaging array with sigma-delta pixel-level converters used a 64×64 array size. Each pixel had a CMOS photodetector and a sigma-delta converter. Stanford's sigma-delta converter digitized the voltage across each capacitor to 1000 binary outputs per second. The outputs were later filtered to receive higher precision at a much lower frame rate. The samples were read out using a random access memory (RAM) structure that will be discussed in Section 3.1. The imaging array achieved a SNR of 61 dB, but produced 10% fixed pattern noise (FPN) between pixels[2]. FPN was caused by offset differences between the ADCs. Since their first prototype, the researchers at Stanford have improved the sigma-delta converter. Stanford's most recent imaging array prototype with pixel-level sigma-delta converters used a 128×128 array size that achieved a SNR of 83 dB with only 1% FPN[3].

The research team at Stanford University also has recently built an imaging array that uses pixel-level, 8-bit single-slope converters. This imaging array also has a photodetector in every pixel and uses a RAM readout structure. Stanford's imaging array of single-slope converters has several advantages over their imaging array of sigma-delta converters, such as lower FPN and less memory and processing required[4]. Overall the research team concluded that the signal-slope converter is good for low flux applications whereas the sigma-delta converter is better for high dynamic range, high flux applications[6].

In 1994, Woodward Yang, built a 32×32 imaging array using pixel-level V-to-F converters. Similar to the Stanford research group, Yang's imager had a CMOS photodetector and ADC in each pixel and used a RAM readout structure. Yang's imager provided a high dynamic range that could vary over 5-6 orders of magnitude and showed potential of further development[5]. However, since 1994, Yang has not published any other papers describing pixel-level V-to-F converters.

1.4 Thesis Overview

This thesis investigates the feasibility of pixel-level A/D conversion for the imaging array of an advanced interferometer. Chapter 2 is a preliminary examination of various pixel-level ADCs. Chapter 3 presents three different readout methods. The first two readout methods, the RAM structure and the non-sequential counter / shift-register, vary drastically in their implementation. The third method is a similar in theory to the non-sequential counter / shift-register, but was designed to improve power dissipation.

Chapter 4 and 5 focus on a pixel-level imaging array using V-to-F converters and sigma-delta converter respectively. These chapters present circuit design and analysis. Included in the analysis are HSPICE simulations and power dissipation estimates.

Chapter 6 discusses some obstacles that must be overcome to successfully build a large, high speed, precise imaging array using pixel-level A/D conversion. Chapter 7 states the conclusions of the thesis.

2.0 Possible A/D Conversion Methods

Various ADCs are simple enough to possibly fit within the 60 μm × 60 μm area allotted to each pixel in the interferometer imaging array. This chapter is an attempt to eliminate some such possibilities through cursory analysis, before a more in depth examination is conducted. The analysis in this chapter focuses on meeting the speed, area and accuracy requirements of the interferometer imager.

The following types of ADCs will be discussed: two types of V-to-F converters, a single-slope converter, a dual-slope converter and two types of sigma-delta converters. These ADCs were selected because they all can be made to fit in a small amount of area, and several of these methods have been, or are still being investigated by different organizations (see Section 1.3).

2.1 Voltage to Frequency

The principle of the V-to-F converter methods is that incoming photocurrent is transformed into a series of pulses. The greater the incoming current, the higher the pulse frequency will be.

Two different V-to-F converter methods were investigated for use in the advanced interferometer project. The first method uses a counter to count the number of pulses produced in one frame. The number on the counter at the end of each frame is a digital measurement of the light intensity. The second V-to-F method investigated measures the amount of time that elapses between two pulses. The time between two pulses can be inversely mapped to the rate of the incoming photocurrent.

2.1.1 Voltage-to-Frequency (counting pulses)

The operation of the pixel-level, V-to-F converter is as follows: the incoming current from the detector is integrated on a capacitor until a predetermined threshold voltage level is reached. Once the voltage across the capacitor reaches the threshold voltage, the capacitor is discharged, a pulse is generated that increments a counter, and the process is repeated (Figure 2.1). At the end of a frame, the number on the counter is the digitized light intensity.

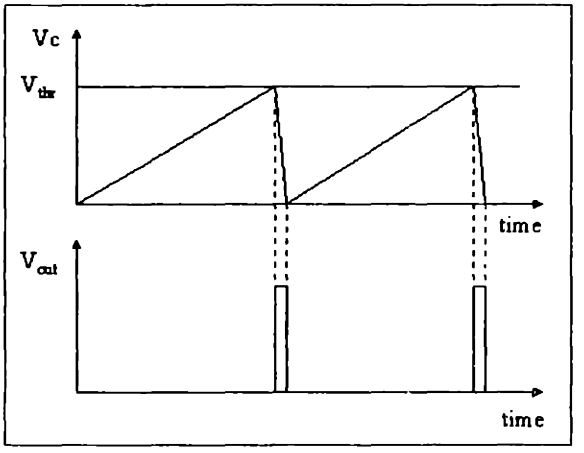

Figure 2.1: V-to-F Theory

A circuit diagram of the V-to-F converter is shown in Figure 2.2. The four inverters connected in series act as a comparator with the comparator reference voltage being the threshold voltage of the inverters. Once the capacitor voltage reaches the threshold voltage of the first inverter, the output of inverter starts to change. The output change of the first inverter then triggers the output of the second inverter to change even faster, and so on down the inverter chain. Therefore, a short time after the capacitor voltage reaches the threshold voltage of the first inverter, the output of the last inverter switches high. The high output turns on a transistor that discharges the capacitor. Once the capacitor is discharged, the inverters switch back to their original state, sending the output low. The low output shuts off the discharging transistor so that

integration can begin again. Using just two inverters connected in series could also act as a comparator but the comparator transition would be not be sharp and the propagation delay from two inverters would not be long enough to fully discharge the capacitor.

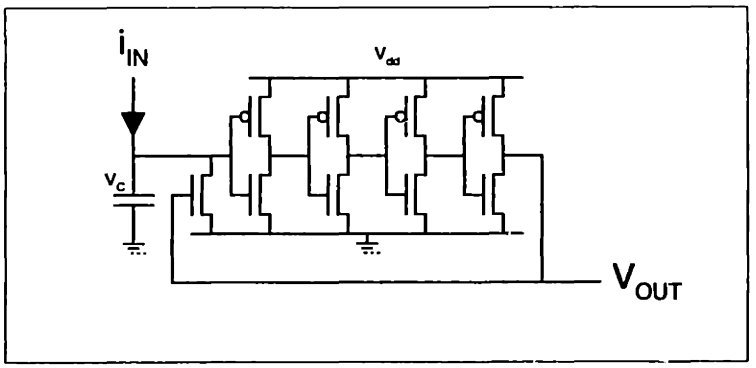

Figure 2.2: V-to-F Schematic

The V-to-F converter must be able to produce a rapid pulse stream. For the interferometer project to obtain the 14-bit accuracy needed, under maximum light intensity, the V-to-F converter must be designed to produce 82 million pulses per second, or one pulse every 12 ns. However, the V-to-F converter cannot count pulses continuously, because some time is needed to read out the digitized value to memory. Therefore, a time limit of 10 ns per pulse is more realistic.

For the V-to-F converter to produce a pulse every 10 ns under maximum light intensity, the sum of all the circuit propagation delays must be less than 10 ns. The longest propagation delay in the V-to-F circuit is that of the voltage comparator made from the series of inverters. The propagation delay of the comparator, t_{PDC}, is dependent on the difference between the threshold voltage of the comparator and the input voltage. HSPICE simulations have shown that if the difference in voltage is less than a milivolt, then t_{PDC} is greater than 10 ns. If the difference in voltage is greater than a few milivolts, then t_{PDC} is less than 2 ns.

Under maximum light intensity, voltage changes greatly with time (around 6 mV per nanosecond). After 1/3 ns, enough of a voltage difference exists between the threshold voltage and input voltage that the comparator propagation delay is small. Thus, the propagation delay of the whole circuit is less than the 10 ns constraint. When the light intensity is weak, however, the voltage change per unit time is small and therefore, the propagation delay of the comparator might be more than 10 ns. The longer propagation delay does not pose a problem though, because the under low light intensity, the pulse rate is much slower than 10 ns. If the pulse rate is slower than 10 ns, the propagation delay of the comparator can also be longer than 10 ns.

A benefit of the V-to-F converter is that during integration, the integrating capacitor is repeatedly discharged. Thus, a very small capacitor (on the order of femtofarads) can be used without saturation. Excluding the counter, the whole V-to-F converter can be built using nine transistors and a small capacitor (Figure 2.2), which could easily fit in a 10 $\mu m \times 10\ \mu m$ area. Therefore, if a small 14-bit counter can be built, the V-to-F converter can meet the size requirements for the interferometer imager.

After a preliminary examination, the proposed pixel-level V-to-F ADC demonstrates the potential to meet the interferometer imager requirements for accuracy, speed and area. Therefore, a closer investigation was conducted to further analyze the feasibility of using V-to-F converters in the interferometer imaging array (see Chapter 4).

2.1.2 Voltage to Frequency (time between pulses)

A variation on the V-to-F converter can be achieved by counting the number of clock cycles between pulses (Figure 2.3), instead of counting the number of pulses in a given time period. The number of clock cycles between pulses is an inverse measurement of the light intensity. If there is high light intensity, the capacitor will be charged in only a few clock cycles. However, if the flux rate is half the original rate, twice as many clock cycles will be counted.

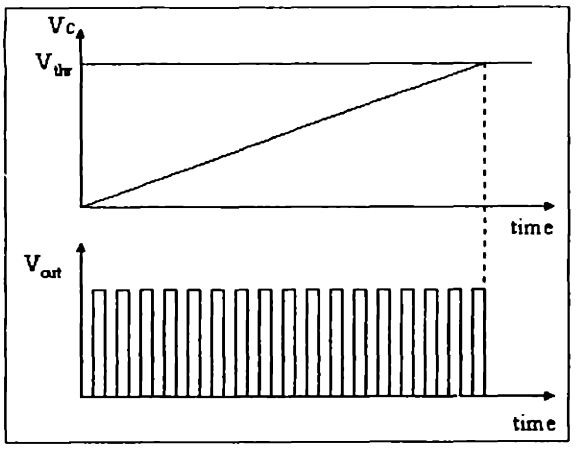

Figure 2.3: V-to-F Counting Clocks Between Pulses

This A/D conversion method provides high resolution for low light intensity situations but low resolution for high light intensity situations. For example, if during maximum light intensity 10 clock cycles are counted between pulses, 20 clock cycles will be counted between pulses during 50% light intensity. In this example, only 10 different quantization levels are possible for the upper half of the dynamic range. However, for light intensities between 1.56% and .78%, there are 640 different quantization levels.

To receive 14-bit precision, around 8,200 quantization levels are needed between 100% and 50% illumination. To create 8,200 quantization levels between 100% and 50% illumination, over 820,000 clock cycles are needed per frame in order to have a range from 100% - 1% of the maximum illumination. This design leads to more than 4.1 billion clock cycles per second. Building a V-to-F converter with sub-nanosecond clock rates is not feasible. Therefore, the modified V-to-F converter will not be investigated further.

2.2 Single-Slope

The single-slope ADC is conceptually very simple. The incoming photocurrent is integrated on a fully discharged capacitor for a given period of time. Once the time period is

over, the voltage across the capacitor, V_C, is proportional to the flux rate. To receive n-bit accuracy, V_C is compared to a ramp voltage, generated using a universal digital to analog converter (DAC), which uniformly increases every clock cycle (Figure 2.4). Every clock cycle in which V_C is higher than the ramp voltage, a counter is incremented. Once the ramp voltage passes V_C, the counter holds state. At the end of 2^n clock cycles, the binary count is the digitized flux rate.

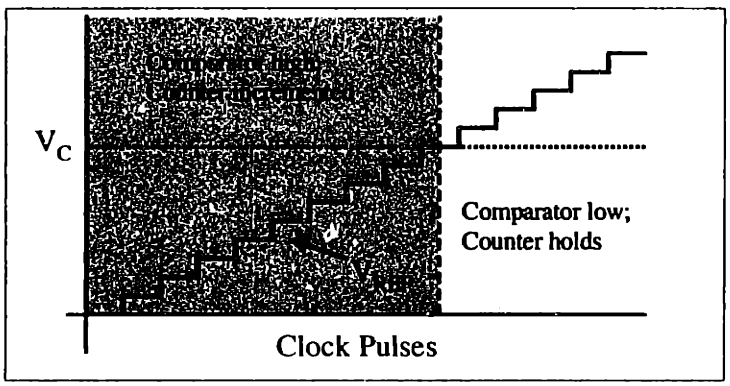

Figure 2.4: Single-Slope Theory

The single-slope converter, unlike the V-to-F converter, only discharges the capacitor once per frame. This can lead to good performance for low-light situations, but problems with well depth limitations and capacitor area limitations arise during high-light-intensity applications. A capacitor large enough to hold the maximum electrons per frame (2×10^8) requires most of the 60 μm × 60 μm pixel area[1]. Therefore, not enough area remains for the ADC circuitry.

The area constraint is not the only problem with the single-slope converter. The single-slope converter cannot jointly meet the speed and accuracy constraints. Under full illumination, a 14-bit ADC using a counter requires 2^{14} pulses. As mentioned in Section 2.1, 2^{14} pulses at a frame rate of 5000 Hz and allowing readout time leads to a cycle every 10 ns. Therefore, in order to receive the correct count, the propagation delay for the whole converter must be less than 10 ns. Using a 14-bit converter with a maximum V_C of 3 V (dictated by the breakdown voltage of silicon), the uniform ramp increments are .18 mV each clock cycle. A relatively small

comparator (under 25 transistors) that can operate within the 10 ns time constraint with a voltage difference of .18 mV is not known. The comparator used in the V-to-F converter satisfies the speed requirement because the voltage difference was on the order of millivolts.

Preliminary research indicates that the single-slope converter is not a viable solution for the interferometer project because of area constraints and unattainable comparator requirements. Therefore, the single-slope converter will not be further investigated.

2.3 Dual-slope

The dual-slope converter is a simple yet effective ADC. Current from the detector is integrated on a capacitor for a given amount of time and then discharged at a constant current (Figure 2.5). A counter records the number of clock cycles needed to discharge the capacitor. This count is proportional to the flux rate.

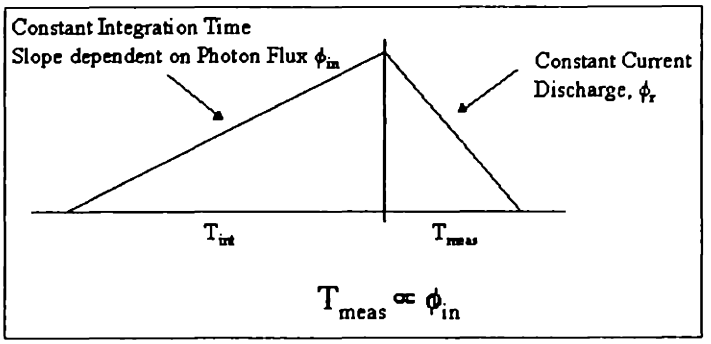

Figure 2.5: Dual-Slope Operation

A dual-slope converter can be made using a discharge transistor, a comparator, and a counter. During the integration period charge accumulates on the capacitor. Once the integration period is over, a transistor is switched on that discharges the capacitor. The transistor remains on until the first clock cycle in which the capacitor voltage is lower than a given reference voltage. Then, the voltage on the capacitor is held at the reference voltage until the next integration period.

The digitized voltage is calculated by totaling the number of clock cycles in which the capacitor was being discharged.

Similar to the single-slope converter, the precision of the dual-slope converter is limited by the comparator. For the dual-slope converter to achieve the required 14-bit accuracy, the comparator must distinguish between the capacitor voltage and the reference voltage with a small margin of error. The margin of error is determined by the number of quantization levels (2^{14}) divided by the breakdown voltage of the capacitor (approximately 3 V). Using these numbers, the dual-slope comparator must be able to distinguish a .18 mV difference with a propagation delay less than 10 ns.

Preliminary research indicates that the dual-slope is not a viable solution for the interferometer project and will therefore not be further examined. Similar to the signal-slope converter, the dual-slope converter has two major problems: a comparator design that fulfills the speed and accuracy requirements is not known, and the integrating capacitor needed would require too much area, since it is only discharged once per frame.

2.4 Sigma-Delta Converter

The sigma-delta converter is a 1-bit ADC that achieves higher accuracy by using feedback, oversampling of the data, and filtering. Feedback is used to shape noise by reducing noise in the bandwidth of interest at the expense of increased noise outside the bandwidth of interest (Figure 2.6). The data is then decimated to obtain a single digital value. The decimation method drastically effects the computational complexity and the oversampling rate needed for a given accuracy level.

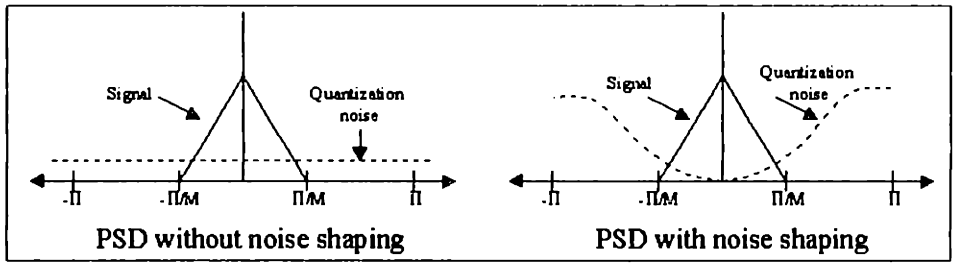

Figure 2.6: Noise Shaping

Two different decimation methods were investigated for use in the advanced interferometer application. The first decimation scheme uses an optimal FIR filter that has a different filter coefficient for every sample in the data. This scheme is computationally complex, but it obtains the same accuracy using a much smaller oversampling ratio than simpler decimation techniques. The second decimation scheme simply averages the output bit stream; thus a counter can be used as the filter. However, as shown in Table 2.1, the simple decimation scheme needs a large oversampling ratio.

Table 2.1: Two Decimation Methods

Decimation Method	Precision (bits)	Oversampling Ratio	Computation complexity per pixel per frame
FIR optimal filter	14	2^{10}	2^{10} multiple-bit adds
Average output bits	14	2^{14}	Counter – does all computation

2.4.1 Complex Filtering

The FIR optimal filter decimation technique could work well for a low-frame-rate application or low accuracy application, because the computational processing could be manageable. However, for high-frame-rate, high-accuracy applications such as the interferometer imager, the computational power needed is enormous. For 14-bit accuracy, 2^{10} multiple-bit additions are needed per pixel per frame. For the interferometer imaging array, this leads to

3.56×10^{11} additions per second. The colossal computation processing needed renders this decimation process unfeasible.

2.4.2 Simple Filtering

The averaging decimation technique does not need any extra processing. The drawback is the large oversampling rate. For the interferometer project to meet the accuracy requirement, 2^{14} times oversampling is needed per frame. As mentioned in Section 2.1, 2^{14} pulses at a frame rate of 5000 Hz and allowing readout time leads to a count every 10 ns. Therefore, in order for the simple filtering, sigma-delta converter to meet the speed requirement for the interferometer imager, the propagation delay of all the subcircuits must be less than 10 ns.

The sigma-delta converter operates using only a few essential subcircuits (Figure 2.7). An integrator, which can simply be the sensor's capacitor, holds the incoming photocurrent and the charge from the feedback DAC. A 1-bit ADC (comparator) determines the output sample. A register holds the state of the current sample for one clock cycle. A counter keeps track of the number of high output bits stored in the register during one frame. And a 1-bit DAC dumps a fixed amount of charge into the integrator each time the comparator goes high.

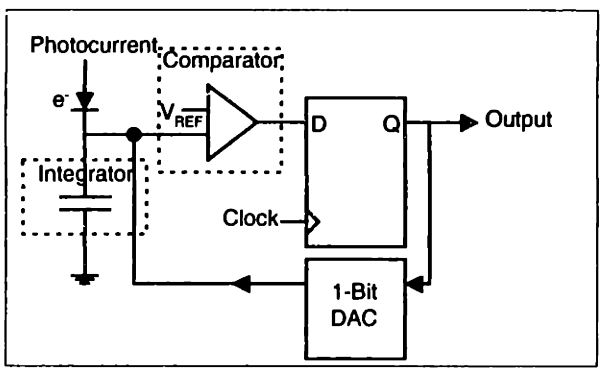

Figure 2.7: Sigma-Delta Block Diagram

The operation of the sigma-delta converter (Figure 2.8) is the most complex of the ADCs investigated. The incoming photocurrent causes the voltage on the capacitor to slope downwards until it goes lower than the threshold voltage of the comparator. Then, upon the rising clock edge, a high signal is loaded into the register. This high signal, in turn, increments the counter and triggers the DAC to dump a fixed amount of charge into the integrator. The voltage on the capacitor then continues to slope downwards until the next registered high signal.

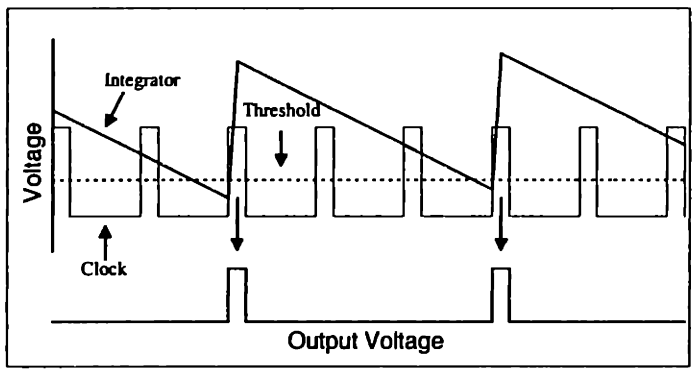

Figure 2.8: Sigma-delta Operation

To meet the speed constraints of the interferometer imager, a fast comparator and DAC must be built. Similar to the V-to-F converter, a series of inverters can be used as a comparator. The effects of the possibly long comparator delays are reduced by the feedback DAC, so the accuracy due to the comparator does not suffer as with the single-slope and dual-slope converters. The accuracy, however, could suffer from the DAC. One method of making an area-efficient, high speed DAC is by releasing a constant current onto a capacitor for a preset time resulting in fixed amount of charge dumped in the capacitor. The problem with this method is that the flow of electrons, similar to the rate at which photons hit a sensor, is not constant but the result of a Poisson process. Therefore, a constant current DAC could produce as much noise as the inherent shot noise of the imaging array. The result would be a reduction of the best achievable SNR by a factor of $\sqrt{2}$. The reduction in SNR is undesirable but does not render this method unfeasible.

One solution to the shot noise problem is to use a charge transfer DAC. A charge transfer DAC could reduce the additive shot noise greatly (see Section 5.2).

Similar to the capacitor in the V-to-F converter, the capacitor in the sigma-delta converter is repeatedly being discharged. Therefore, the capacitor can be on the order of a few femtofarads and still be able to handle a large photocurrent. By making the capacitor small and using state-of-the-art CMOS technology, there is potentially enough room to fit a counter, sensor capacitor, and sigma-delta circuitry in a single pixel.

After a preliminary examination, the proposed pixel-level sigma-delta ADC demonstrates the potential to meet the interferometer imager requirements for accuracy, speed and area. Therefore, a closer investigation was conducted to further analyze the feasibility of using V-to-F converters in the interferometer imaging array (see Chapter 5).

2.5 Conclusion

Six types of pixel-level ADCs were investigated to determine whether they had the potential to meet speed, area and accuracy specifications for the interferometer project. Out of these six ADCs, four were deemed not feasible while two of the ADCs show potential to meet the specifications for the interferometer imager.

The four ADCs were discarded for various reasons. The single-slope and dual-slope converters had two major problems. First, a comparator that satisfied the speed and accuracy constraints was not known. Secondly, the capacitor size was too large to fit in the allotted pixel size and leave room for other circuitry. The V-to-F converter (measuring time between pulses) failed to be a viable solution because, in order to receive the precision needed, unattainable clock rates were required. Last, the sigma-delta converter using extensive filtering was not feasible because of the enormous processing power needed.

The V-to-F converter (counting pulses) and the sigma-delta converter using simple filtering have the potential to meet the interferometer specifications. Both methods show promise to fit within a 60 μm × 60 μm pixel size, assuming a small 14-bit counter can be built. All the subcircuits are comprised of a small number of transistors, and the sensor capacitor can be small, because it is repeatedly discharged.

Both ADCs also show promise to operate fast enough to provide a maximum of 2^{14} pulses per frame needed to obtain the desired 14-bit accuracy. In the V-to-F converter under maximum illumination, the voltage difference across the comparator is large enough that the propagation delays of the comparator are much less than 10 ns. In the sigma-delta converter feedback is used so that the comparator inaccuracies caused by longer propagation delays are corrected over a short period of time.

Further analysis of the pixel-level V-to-F and sigma-delta ADCs is provided in Chapters 4 and 5 respectively. These chapters focus on a more in-depth investigation of the components of the ADCs, power dissipation, and design issues.

3.0 Readout Methods

3.1 Introduction

One of the problems with pixel-level conversion is that digital output from thousands of pixels must be moved off the imaging array and then multiplexed to memory. Therefore, selecting a proper readout method is imperative for successful design. For imaging arrays, there are two fundamentally different readout methods that have proven to work well. These techniques are the RAM readout method (Section 3.2) and the shift-register readout method (Section 3.3 & 3.4).

The readout methods examined in this chapter focus on moving the data from the pixels to off the array. Multiplexing the data from off the array to memory is a different issue that is not explored in this thesis.

3.2 RAM structure

The RAM structure uses row selects and bit lines to address each pixel (Figure 3.1). There is a different row select for each row in the array and individual bit lines for each column in the array. The row select chooses the row that is to be read out. If a row select is asserted, the bit of data from each pixel in that row is driven onto the bit line so it can be read out. For example, to read out the digital value of the pixel in the first column and the second row, row select two must be high. The data would be displayed at the bottom of bit line one.

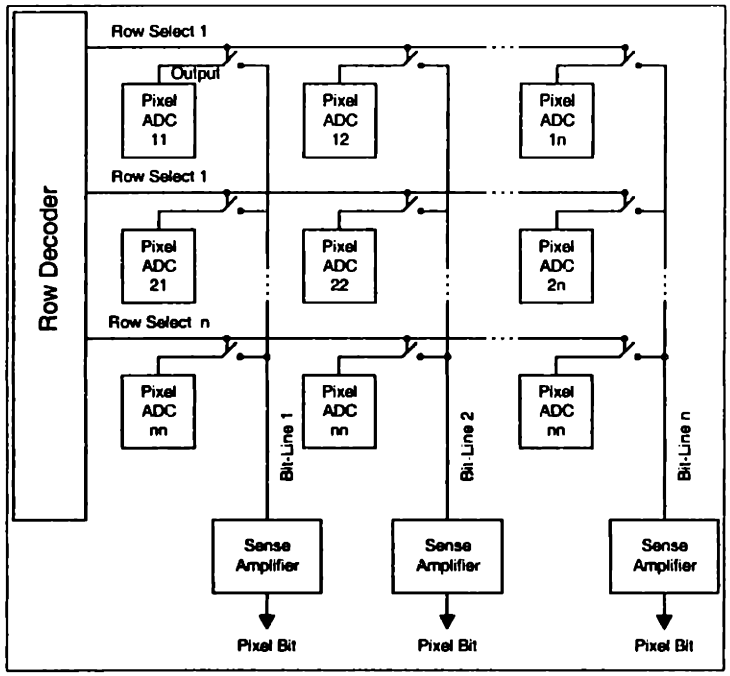

Figure 3.1: RAM Readout Structure

Use of the RAM readout structure has several advantages. Only a few extra transistors per pixel and some additional logic on the edge of the imaging array are needed for implementation. The small amount of area needed inside each pixel is especially desirable because of the tight area constraint associated with pixel-level conversion. Any portion of the array can be selected independently, which is extremely beneficial for large arrays that only need to view a small portion of the image at any given time.

Along with the benefits of the RAM readout structure, there are some disadvantages. The RAM readout structure does not work well for multiple-bit, pixel-level ADCs. It can sense only one bit at a time. In order to read out several bits per pixel, a multiplexer within every pixel is needed to serially select each bit for readout. Using the RAM readout structure for multiple-bit ADCs also leads to timing difficulties, because the allowable readout time per bit is reduced. Due to the timing problems and the additional area needed, the RAM structure is not a practical readout method for multiple-bit pixel level A/D conversion.

Becasause the RAM structure is not practical for multiple-bit pixel-level A/D conversion, only single-bit conversion should be examined. For single-bit, pixel-level ADCs, the RAM structure senses the data on each row of the imaging array once per sample. Therefore, for an n × n array, each row needs to be sensed no slower than 1/n of the time allowed per sample. For example, if a 10 × 10 array had pixel-level ADCs that produced a sample every 100 ns, the RAM structure would need to sense each bit in less than 10 ns.

For Lincoln Laboratory's interferometer project, a 256 × 256 imaging array with 14-bit accuracy having frame rates of 5000 Hz is required. Under these conditions the RAM readout structure is undesirable. To achieve 14-bit accuracy using a 1-bit ADC, the converter needs a sampling rate of $2^{14}\ \frac{samples}{pixel \times frame}$, or $8.19 \times 10^{7}\ \frac{samples}{pixel \times s}$. During each sample, all the rows of the imaging array would need to be read out separately, which reduces the readout time of each pixel by an additional factor of 256. For success, the RAM readout structure would have to sense each row at no slower then 50 ps. The 50 ps time constraint is not feasible. Therefore, other readout method should be explored for Lincoln Laboratory's interferometer project.

3.2 Non-Sequential Counter / Shift-register

A non-sequential counter can be built by connecting inverting or non-inverting registers in series and using a feedback XOR gate to generate the input to the first register[7] (Figure 3.2). Each input pulse will produce a new bit order that will not repeat for $2^n - 1$ counts (there is one trivial state. The trivial state, all zeros for non-inverting registers, will cycle in the same state until forced out. Therefore, it is important that the counters are not initialized to the trivial state. One small drawback of the counter is that although the counting sequence is unique, it is not easily decipherable, so a scheme is needed to decode the counting sequence to an understandable form.

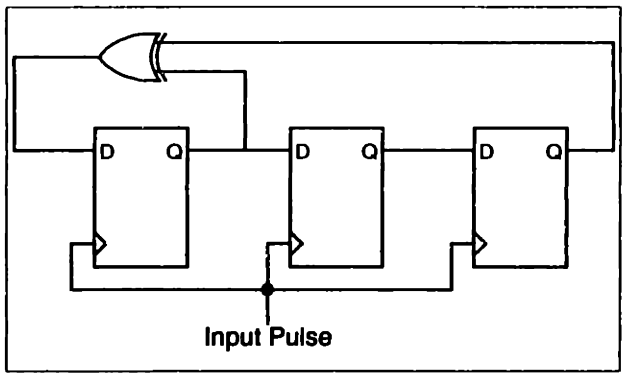

Figure 3.2: 3-Bit Non-sequential counter

The non-sequential counter can also operate as a shift-register. Once a frame period is finished, switching logic is used to alternate between the counting mode and the readout mode by disconnecting the XOR gate, joining together adjacent pixels, and connecting a shifting clock to the registers (Figure 3.3). The switching logic can be implemented using a few extra transistors per counter.

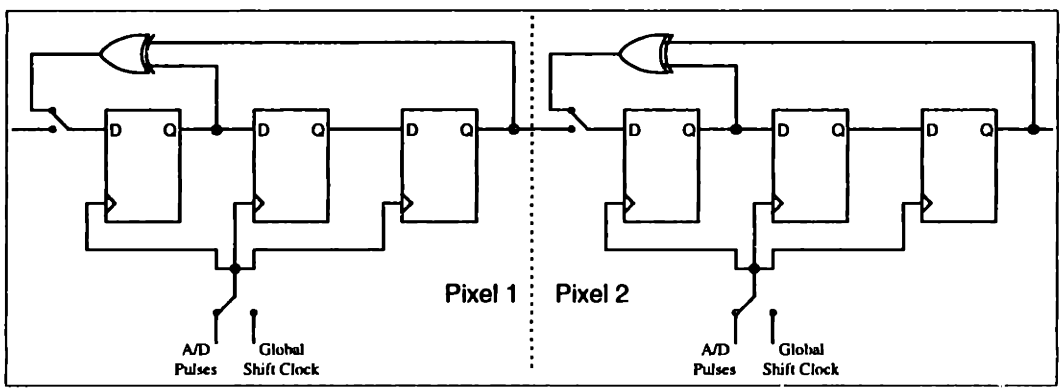

Figure 3.3: Non-Sequential Counter / Shift-register

During the readout mode, the counters of the pixels in a given row are transformed into a giant shift-register without effecting the data held on the counters. Then, the data is simply shifted from one pixel to an adjacent pixel until all the bits are off the imaging array (Figure 3.4).

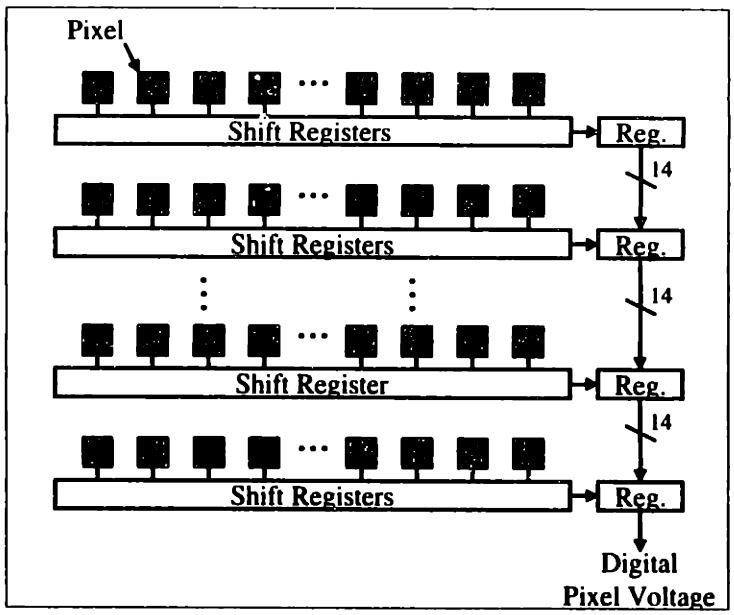

Figure 3.4: Shift-register Readout Operation

3.2.1 Area

There are two major advantages for using the non-sequential counter / shift-register (NSCSR). The NSCSR is fast and area efficient. A 15-bit, non-sequential counter has been built in 2.4 μm technology[7] that when scaled down directly will fit in a 22 μm × 53 μm area using 0.35 μm technology. Realistically, circuit sizes do not scale directly with the type of technology used; however, these results show that a high-speed, 14-bit counter should easily fit within a 60 μm × 60 μm area using 0.35 μm technology. Also, technology keeps shrinking at an alarming rate, so in the future, the NSCSR will be able to fit in an even smaller area.

A 14-bit NSCRS uses 15 registers, 1 XOR gate, and switch logic. A dynamic, inverting, single-clock register can be built using 9 transistors[7] (Figure 3.5). This register is used because it is fast, area-efficient and only uses a single clock. Due to charge leakage, the dynamic register can only hold charge for a few miliseconds; however, the registers used in the interferometer project get refreshed often enough that charge leakage is not a problem. The total number of transistors needed for a 14-bit NSCSR is 149 (15 registers × 9 transistors per register + 1 XOR

gate × 6 transistors + 1 switch logic × 8 transistors). In general, the following is needed to construct an n-bit NSCRS: n or n + 1 registers, one XOR gate and 8-transistor switch logic.

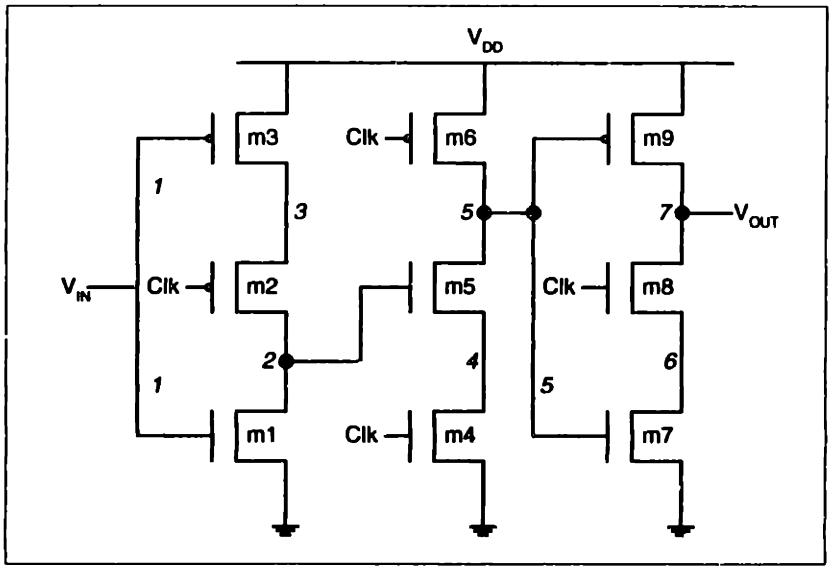

Figure 3.5: Dynamic, Inverting, Single-Clock Register

3.2.2 Speed Performance

As discussed in Chapter 2, both the sigma-delta converter and the V-to-F converter demand a high-speed counter. Under full illumination, the converters are designed so that 2^{14} pulses are generated per frame. This pulse rate leads to a maximum of 82 million pulses per second during integration (5000 frames per second × 2^{14} pulses per frame) and an additional 18 million pulses for readout (256 pixels × 14 bits per pixels × 5000 bits per frame). Precision increases with integration time. Therefore, the readout clock is designed for the fastest time possible. A counter / shift-register that counts and shifts at speeds of at least 100 MHz is needed. However, a faster shift-register is desired in order to receive a longer integration period per pulse. Table 3.1 shows the readout rate verses the integration rate during maximum light intensity. This table was created by fixing a readout rate, calculating the total amount of time spent on readout, and then calculating the maximum integration time allowed per sample.

Table 3.1: Readout Rate Verses Integration Time

Readout rate (bits per sec)	Integration rate (pulses per sec)	Integration time (sec per pulse)
100 MHz	100 MHz	10.0 ns
200 MHz	90 MHz	11.0 ns
500 MHz	85 MHz	11.7 ns
1000 MHz	83.5 MHz	11.9 ns

The speed of the NSCSR is limited by the propagation delay of the register (t_{PDR}) and the XOR gate (t_{PDX}). Hand calculations have shown and SPICE simulations have verified that t_{PDR} and t_{PDX} are under .5 ns for the MOSIS 0.35 μm process. Thus, during integration mode or readout mode, the NSCSR could easily be clocked at the necessary 100 MHz rate.

3.2.3 Power Dissipation

One of the major drawbacks of the NSCSR readout method is that this method has high power dissipation. There are two main contributors to power dissipation, dynamic and short circuit[7]. Short circuit power dissipation is usually small compared to dynamic power dissipation and so will not be considered in this chapter. However, short circuit power dissipation is discussed in Section 4.2. A good approximation for dynamic power dissipation (P_{DYN}) is given in equation 3.1, where C is the average capacitance, V_{dd} is the power supply voltage, F is the frequency and N is the average number of capacitors being charged per cycle.

$$P_{DYN} \approx C \times V_{dd}^2 \times F \times N \tag{3.1}$$

An approximation of the total power dissipation produced by the NSCSR during the interferometer project is found by combining the power dissipation of the integration period and readout period (Eq. 3.2). The power dissipation of the two modes is found by multiplying the power dissipation per register by the number of registers in the imaging array (Eq. 3.3).

$$P_{DYNtotal} = P_{DYNintegration} + P_{DYNreadout} \tag{3.2}$$

$$P_{DYN} \approx \frac{P_{DYN}}{register} \times \frac{registers}{pixel} \times \frac{pixels}{array} \tag{3.3}$$

Using the following circuit values for the readout and integration periods (from Appendix A),

C = 1 fF
N / register = 6.5
V_{dd} = 3.3 V
F = $2^{14} \times 5000$ (integration), 256×5000 (readout)
pixels / array = 256×256
registers / pixels = 15

and applying equation 3.1, 3.2 and 3.3, $P_{DYNintegration}$ = 5.7 W and $P_{DYNreadout}$ = .09 W for a $P_{DYNtotal}$ = 5.8 W.

The power dissipation of the imaging array must be kept at a minimum because for accurate results the detectors must be cryogenically cooled to below 70 K. In order to keep cost reasonable, the imaging array should not dissipate more than .2 W of power. The NSCSR alone uses more power than 25 times the acceptable limit. Therefore, an alternate readout method was investigated.

3.3 Ripple Counter / Shift-register

An n-bit ripple counter can be built using n inverting registers connected together in series (Figure 3.6). The first register is clocked from an incoming pulse train. The output of this register is used to clock the second register. The output of the second register is used to clock the third register, and so on down the line. In addition, the output of each inverting register is fed back to its input. Thus, upon the rising edge of the clock, the output takes on the inverted value

of the input. This inverted value is then fed back to the input, causing the register to change states.

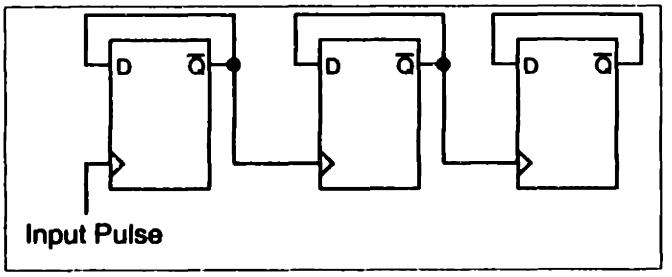

Figure 3.6: 3-Bit Ripple Counter

Similar to the NSCSR, although with significantly more transistors, this ripple counter can be constructed to operate as a shift-register. Once a frame period is finished, switching logic is used to alternate between the counting mode and the readout mode (Figure 3.7). The output of each pixel is disconnected from the feedback loop and the clock of the next register, and connected to the input of the adjacent register. Also, during the readout period a shifting clock is attached to the clock input of every register.

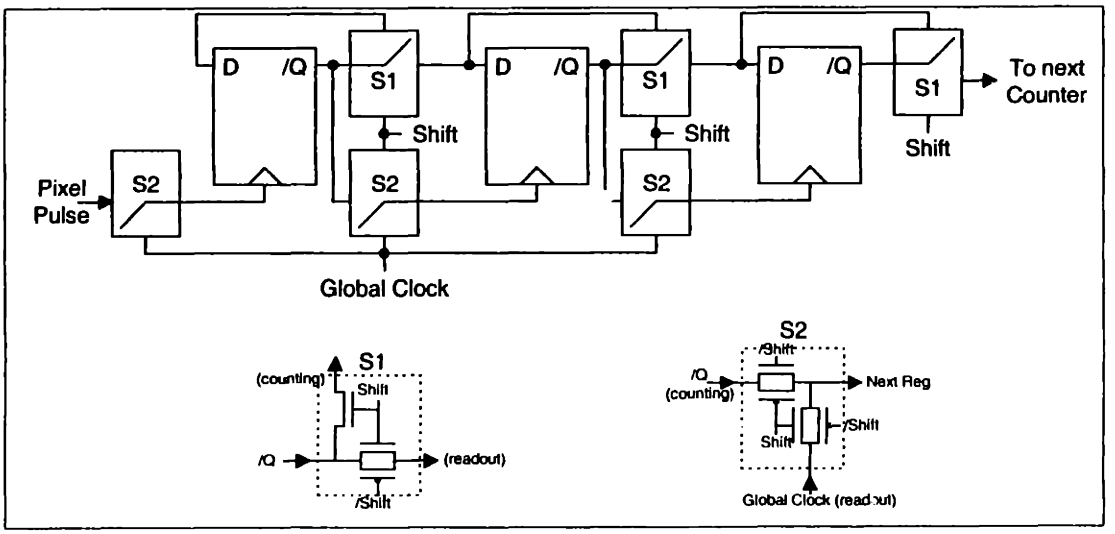

Figure 3.7: Ripple Counter / Shift-register

One major difference between the ripple counter / shift-register (RCSR) and the NSCSR is that the counting mode of the RCSR is not synchronous. In order for the n^{th} bit to change states, the $n^{th} - 1$ bit must change from low to high (for positive-edge triggered register). For each register that changes state, there is a propagation delay, t_{PDR}, before the next register can change states. Thus, the propagation delay for incrementing an n-bit counter be anywhere from t_{PDR}, if only the first register changes state, to $n \times t_{PDR}$, if all the registers change states. However, the RCSR can count at speeds faster than the maximum propagation delay, as long as enough time ($n \times t_{PDR}$) is allowed so that the output of the counter can settle before it is shifted off the array.

3.3.1 Area

In general, an n-bit RCSR is comprised of n registers and n switch logic blocks. Each register uses 9 transistors. Each switch logic block uses 7 transistors. Lincoln's interferometer project requires a 14-bit RCSR, so 224 transistors are need per pixel to implement the RCSR method. There has been no known implementation of RCSR, so the exact layout area is hard to determine, although, based solely on the number of transistors used, the RCSR is approximately 1.5 times larger than the NSCSR. If the 1.5 area proportion estimate and 0.35 μm CMOS process technology is used the RCSR should fit in a 33 μm × 53 μm area. Therefore, the RCSR should fit within the allotted 60 μm × 60 μm pixel size with enough area left over for the rest of the ADC circuitry to also fit in a pixel.

3.3.2 Power dissipation

The reason for changing from a synchronous counter to a ripple counter is that power dissipation is lowered. The main reason for the lower power dissipation is that with an n-bit

synchronous counter, every time a pulse is generated all of the registers in the counter are clocked. Clocking all the registers causes n times the average power dissipation of one register. With a ripple counter, every time a pulse is generated only the registers that change state are clocked. The first register changes every clock pulse, the second register changes once every two clock pulses, the third register change once every four clock pulses and so on. This sequence implies that on 50% of the pulses 1 register is changing, 25% of the pulses 2 registers are changing, and 12.5% of the pulses 3 registers are changing. For an infinite ripple counter, the above series would sum to 2 (Eq. 3. 4). Therefore, because the ripple counter is finite, on average less than two registers are clocked per pulse.

$$\sum_{n=1}^{\infty} n \times \frac{1}{2^n} = 2 \tag{3.4}$$

The power dissipation of the RCSR can be estimated with the same approach used in Section 3.2.3. Using the follow circuit values for the readout and integration periods (from Appendix A),

C = 1 fF
N / register =7.5 (integration), 6.5 (readout)
V_{dd} = 3.3 V
F = 2^{14} × 5000 (integration), 256 × 5000 (readout)
pixels / array = 256 × 256
registers / pixel = 2 (integration), 14 (readout)

and applying equation 3.1, 3.2 and 3.3, $P_{DYNintegration}$ = .88 W and $P_{DYNreadout}$ = .09 W for a $P_{DYNtotal}$ = .97 W

3.4 Conclusion

The RAM readout method cannot be used for the interferometer project because, among other reasons, each row would have to sense data at unattainable rates. Therefore, a counter / shift-register readout method must be used.

Both the NSCSR and the RCSR provide an effective way of transferring data off the imaging array. The NSCSR is about 1.5 times smaller than the RCSR, however, both readout methods should fix within the 60 μm × 60 μm pixel size leaving extra room for the rest of the ADC circuitry. Thus, the area difference between the two readout methods is not a major factor, although, if larger than 0.35 μm CMOS technology was used for the interferometer project, or if area intensive features were to be added, the NSCSR would be favored.

The NSCSR also has an advantage over the RCSR because the RCSR needs to wait for its data to settle before switching. Depending on the length of time the data takes to settle, an extra clock signal might be necessary, thus adding to the complexity of each converter. The NSCSR is synchronous, so the imaging array can switch from counting mode to readout mode without the need of an extra clock signal.

The major drawback of the NSCSR is that power dissipation is much higher than the RCSR. For the interferometer project the estimated difference of the dynamic power dissipation is 5.8 W compared to 1.0 W. As previously mentioned, for success, it is essential that the power dissipation of the imaging array is below .2 W. Both readout methods fails this constraint, but the hope is that with improving technology, the voltage level needed to operate the imaging array will decrease. The power dissipation decreases by approximately the square of the voltage level. Therefore, if the voltage level drops by a factor of 2, the RCSR will be near the .25 W constraint, but the NSCSR will still be significantly over the .25 W constraint. Therefore, for the interferometer project, the RCSR is the best readout scheme of the three methods discussed.

4.0 Voltage-to-Frequency Converter

4.1 Introduction

Chapter 4 further analyzes the pixel-level V-to-F converter presented in Section 2.1. As a caution to the reader, Chapter 4 starts out using knowledge of the V-to-F converter gained in Section 2.1. Therefore, Section 4.2 does not review the operations of the V-to-F converter, but instead dives into an important design parameter, the power dissipation. In Section 4.3, HSPICE simulations of a model pixel-level V-to-F converter are presented. These simulations aid in verifying the theory and in the understanding of the V-to-F converter's operations. Section 4.4 discusses discharging errors and their effect on the converter. Section 4.5 presents various factors that could reduce the accuracy of the V-to-F converter. Finally, Section 4.6 discusses whether the V-to-F converter should be used for the interferometer project.

4.2 Power Dissipation

Excluding the counter, which was discussed in Chapter 3, the V-to-F converter only has 9 transistors. Eight of the transistors form four inverters that function as a comparator. These inverters account for most of the power dissipation. A good estimate of power dissipation for the inverters is found by calculating the short circuit and dynamic power dissipation. The short circuit power dissipation cannot be disregarded in this section as it was in Chapter 3 because the low to high and high to low input transitions of the inverters are slow. The slow input transitions cause both the PMOS and the NMOS transistors to be on for an extended period of time, creating a path from power to ground. If the input transitions were fast, as with the counter, there is a negligible time that the NMOS and the PMOS transistors are on simultaneously and thus, a negligible short circuit power dissipation. An estimation of short circuit power dissipation (P_{SC}) is given in equation 4.1, where I_{PEAK} is the peak short circuit current, T_{BASE} is the length of time

there is a path from power to ground, and F is the inverter switching frequency. Note that $T_{BASE} \times$ F is equal to the percentage of time per second that the inverter has a path from power to ground.

$$P_{SC} \approx \frac{1}{2} \times I_{PEAK} \times T_{BASE} \times V_{dd} \times F \tag{4.1}$$

As mentioned in Section 2.2, for the V-to-F converter, the incoming current from the detector causes the voltage across the capacitor to ramp up until the threshold level of the inverters is reached. Once the threshold level is reached the inverters change state. This threshold level is reached when the inverter's input voltage is equal to its output voltage. Consequently, at the threshold voltage, the current of the PMOS transistor is equal to the current of the NMOS transistor. However, once the input voltage surpasses the threshold voltage, the NMOS transistor starts supplying more current than the PMOS transistor, which drives the output low. The threshold level, V_{THR} can be computed using equation 4.2, where V_{Tn} is the NMOS threshold voltage, V_{Tp} is the PMOS threshold voltage, and k is the mobility ratio μ_n / μ_p. Equation 4.2, which is only valid for $V_{DD} > V_{Tn} - V_{Tp}$, was derived using the basic current laws of a transistor.

$$V_{THR} = \frac{\sqrt{k} \times V_{Tn} + V_{DD} + V_{Tp}}{1 + \sqrt{k}} \tag{4.2}$$

Figure 4.1 shows an example of the input voltages verses time of the first two transistors in an inverter chain. The input voltage of the first inverter, V_{IN1}, increases linearly due to the constant incoming photocurrent. Once V_{IN1} passes V_{Tn}, the input voltage of the second inverter, V_{IN2}, starts to decline. V_{IN1} increase until it passes V_{THR}. Then, after a short propagation delay, the capacitor is discharged sending V_{IN1} back to 0 V. The P_{SC} region displayed on Figure 4.1 is a region where the NMOS and the PMOS transistors are on simultaneously. This region is between

$V_{dd} + V_{Tp}$ and V_{Tn}. If an inverter's input voltage is in the P_{SC} region, then the output of that inverter has a path from power to ground and thus short circuit power dissipation is occurring.

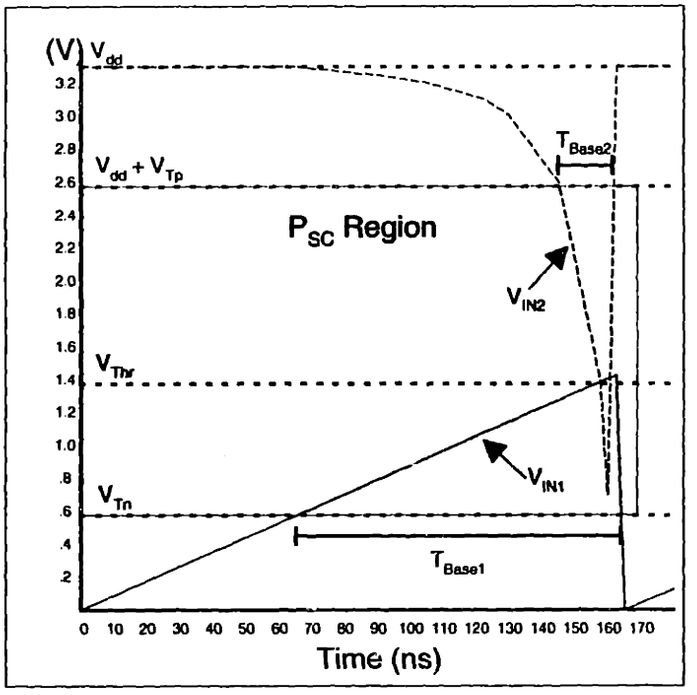

Figure 4.1: Two Inverters Input Voltages vs. Time

The percentage of time that the first inverter is in the short circuit power region is approximately V_{Tn} / V_{THR}. Using this approximation for a circuit using the MOSIS 0.35 μm process, the parameters of which are summarized in Table 4.1 and fully listed in Appendix B, the first inverter would be in the P_{SC} region 55% percent of the time. HSPICE modeling verified this approximation to a few percent. Simulations show that the percent time spent in the P_{SC} region for the other three transistors are 14%, 1%, and less than 1% respectively. Therefore, using the circuit values in Table 4.1 and equation 4.1, the P_{SC} per comparator is 167 μW. The V-to-F comparators used in constructing the interferometer imager alone would lead to a P_{SC} of greater than 10.9 W. This high power dissipation is not acceptable for the interferometer imager, so a method of reducing the short circuit power dissipation is needed.

Table 4.1: Important Process Parameters

MOSIS 0.35 μm Technology	
V_{Tn}	0.57 V
V_{Tp}	-0.63 V
Tox	7.6×10^{-9} M

A series of inverters could be powered such that the PMOS and the NMOS transistor cannot be on at the same time as long as $V_{dd} + V_{Tp} \leq V_{Tn}$. If the PMOS transistor and the NMOS transistor are not on simultaneously then there is not a path from V_{dd} to ground, and thus there is no short circuit power dissipation. For the MOSIS 0.35 μm process, V_{dd} would have to be 1.2 V or lower to eliminate short circuit power dissipation. The drawback of the low powered comparator for the V-to-F converter is that the output of the comparator is used to create a pulse that increments the counter. The 1.2 V pulse created by the comparator is not powerful enough to increment a counter that runs on the necessary 3.3 V, so a method of amplifying the pulse is needed. However, even with the amplifier, the lower powered comparator dissipates much less power than a comparator powered on 3.3 V.

Due to the fact that the low power comparator does not have any short circuit power dissipation, a power dissipation estimate can be obtained by examining the dynamic power dissipation. Using the following circuit values (Appendix A),

C = 1 fF
N / comparator = 4
V_{dd} = 1.2 V
F = $2^{14} \times 5000$
comparator / array = 256×256

and applying equation 3.1 and 3.3, the dynamic power dissipation of the imaging array due to the comparator is 31 mW. This power dissipation is negligible compared to the power dissipation due to the counter / readout circuitry.

4.3 HSPICE Simulations

A model of a single V-to-F converter (excluding the counter) was designed and examined using HSPICE (Figure 4.2). All the transistors in the model were minimum size and used the MOSIS 0.35 μm technology parameters. The HSPICE source file is listed in Appendix C.

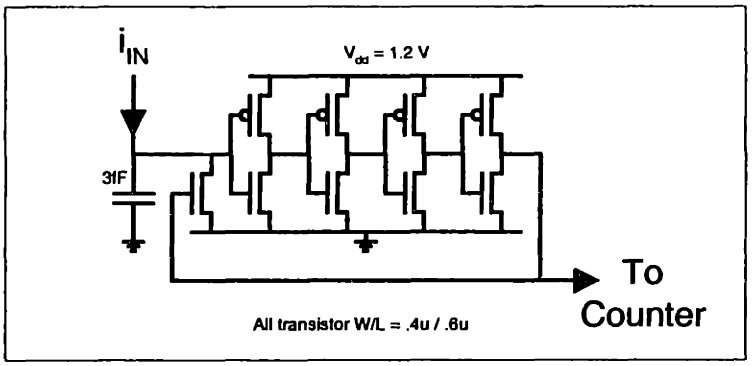

Figure 4.2: V-to-F HSPICE Model

The V-to-F model was built to closely resemble the interferometer specifications. Ideally, ignoring the reset noise, which will be discussed later, the V-to-F converter would be built for a maximum current of 160 nA. The maximum current is found by multiplying the maximum number of electrons coming from the detector each second (10^{12} e^-/s) by the charge per electron (1.6×10^{-19} q/e^-). For the MOSIS 0.35 μm process, the integrating capacitor would have to be approximately 3.3 fF to produce the 2^{14} pulses per frame necessary to achieve 14-bit conversion. In attempt to match the capacitance level, the integrating capacitor in the HSPICE model was set for 3 fF. However, gate, source, and drain parasitic capacitance from surrounding transistors add approximately 4.5 fF to the integrating capacitance. The greater the integrating capacitance, the more charge is needed to produce an output pulse. Therefore, because of the additional parasitic capacitance, the HSPICE V-to-F model needs a higher current than detectors used in the interferometer project allow to obtain the full range of quantization levels.

Figure 4.3a shows an HSPICE plot of the voltage across the integrating capacitor for incoming currents of 30 nA, 60 nA, and 120 nA respectively. The incoming current is varied at 400 ns and again at 700 ns to demonstrate the behavior of the V-to-F under different conditions. Figure 4.3b shows an HSPICE plot of the pulses produced by the V-to-F converter. These pulses are used to increment the counter. As can be seen from the diagrams, every time the integrating capacitor is discharged, a pulse is produced.

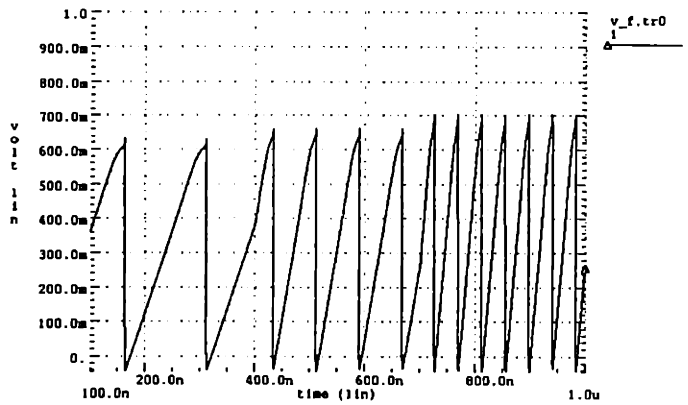

Figure 4.3a: Voltage across capacitor of V-to-F converter

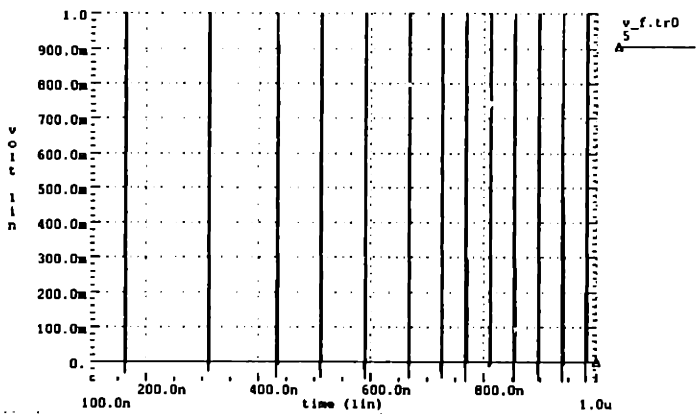

Figure 4.3b: Pulse Stream of V-to-F converter

There are several oddities that one should be aware of in the figures. First, at some points of time, the voltages are below zero. The sub zero voltages are errors produced by the HSPICE

model, but because the errors are constant they do not interfere with the analysis. Another phenomena that one should notice is that in Figure 4.3a, the maximum voltage across the integrating capacitor not only surpasses the threshold level of the comparator, 0.57 V, but also varies with the current. This result is due to the fact that there is a comparator propagation delay. The faster the current, more voltage will build up across the capacitor during the propagation delay. It is important to realize that from the time the capacitor's voltage passes the threshold level of the comparator and the time the capacitor is discharged, the incoming charge is not counted. The uncounted charge leads to reset noise.

4.4 Reset Noise

Reset noise is dependent on the ratio of the time per pulse that the incoming photocurrent is not being counted (reset time) to the pulse period. A higher ratio of the reset time to the pulse period leads to more reset noise. The reset time is approximately twice the propagation delay of the comparator. Table 4.2 shows input current verses reset time, integration time, pulse period and percent reset time per pulse for a V-to-F comparator. The first four entrees in the table were generated using HSPICE simulations of the V-to-F model mentioned in the previous section. The last two entrees were estimated by extrapolating the HSPICE data. As can be seen from the table, the reset time at any input current is a significant percentage of the pulse period, but for high input currents the reset time is a much greater percentage of the pulse period. For example, the reset time for an input current of 30 nA is 12% of the pulse period whereas the reset time for an input current of 240 nA is 34% of the pulse period.

Table 4.2: Reset Time for Various Input Currents

Input Current (nA)	T_R (ns)	T_I (ns)	Period (ns)	% Reset Time
30	18.0	130.5	148.5	12.1
60	14.0	64.0	78.0	18.0
120	10.5	32.25	42.75	24.6
240	8.25	16.5	24.25	34.0
480*	6.25	8.25	14.5	43.1
800*	5.5	5.0	10.5	52.4

The reset noise leads to erroneous results if the incoming current varies rapidly. However, if the assumption is made that the current is constant for a given frame, then the reset noise only adds a non-linearity. The non-linearity is introduced because at higher light intensities the reset time accounts for an increasing percentage of the pulse period. Figure 4.4 compares an ideal V-to-F converter with no reset noise to a V-to-F converter with reset noise.

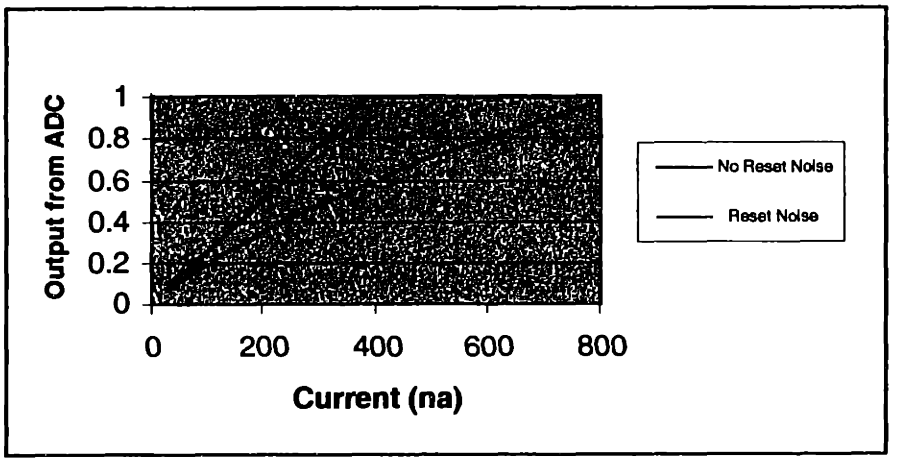

Figure 4.4 V-to-F Converter with Reset Noise vs. without Reset Noise

4.5 Accuracy

In order to build a 14-bit ADC, there must be at least a range of 2^{14} different quantization levels of light intensity. However, for the interferometer project, along with a 14-bit ADC, a high SNR must also be achieved. For an acceptable SNR, the V-to-F comparator, made using four

inverters in series, needs to be accurate enough so that shot and other inherent noise overshadows the comparator inaccuracies. The variance of shot noise per pulse is approximated as $\sqrt{N}$, where N is the number of electrons needed to generate one pulse. To satisfy the interferometer project specifications, N is designed to be around 12200 e^-/pulse (disregarding reset noise) so that under maximum light intensity there can be 2^{14} counts per frame, for frame rates of 5000 Hz. For the overall precision not to be noticeably affected by comparator inaccuracies, the variance of the comparator noise should be less than half the variance of the shot noise. Therefore, the comparator variance should be less than 55 e^- per count ($\frac{\sqrt{N}}{2}$), which is 2.9 mV using a 3 fF capacitor.

Threshold inaccuracies and propagation delay inconsistencies contribute to the comparator noise. Disregarding the effect of the propagation delay, the threshold must be accurate to 2.9 mV using a 3 fF capacitor. The threshold level of the comparator varies with temperature and power supply voltage. In the interferometer project the imaging array is cryogenically cooled, so minimal threshold variation should result from temperature fluctuations. However, power supply noise may effect the trigger voltage of the comparator. As mention in Section 4.2, as long as $V_{dd} + V_{Tp} \leq V_{Tn}$, then the trigger voltage is equal to Vtn. Therefore, as long as the equation $V_{dd} + \Delta V_{Noise} + V_{Tp} \leq V_{Tn}$ is satisfied, the trigger voltage is still V_{Tn}. If this constraint is not satisfied, the comparator trigger voltage will no longer be fixed at V_{Tn} because there will be a region in which both the NMOS and PMOS transistor will be on simultaneously. In order for the power supply noise to not effect the trigger voltage, ΔV_{Noise} must be small and $V_{dd} + V_{Tp} < V_{Tn} + V_{Margin}$ where V_{Margin} should be a few millivolts.

Unlike the possibly minimal effect of threshold inaccuracies, propagation delay inconsistencies will have a large impact on the comparator noise. For the interferometer project to have a comparator noise of less than 55 e^- per pulse, under maximum photocurrent, the

propagation delay inconsistencies of the comparator must be less than .05 ns ($\frac{55e^-}{10^{12}e^-/s}$). Under maximum current, the overall propagation delays of the comparator are approximately 5 ns. Therefore, the propagation delay would have to have less than a 1% variation. Numerous factors, such as power supply noise, shot noise, and temperature fluctuations, cause a variable propagation delay. Thus, it is unlikely to achieve the consistency desired. However, if the incoming photocurrent were reduced by a factor of 10, the comparator propagation delays would only need to have a consistency of 0.5 ns, which should be attainable.

Other factors that could significantly reduce the accuracy of the V-to-F converter include parasitic capacitance, discharge noise and fixed pattern noise (FPN). To receive 2^{14} different quantization levels under maximum flux the integrating capacitor must have a small, precise capacitance. Using a comparator that triggers at 0.58 V and accounting for the reset noise, the interferometer integrating capacitors for each pixel should be 1.7 fF to attain the correct number of quantization levels. However, parasitic capacitance from bump bonding and neighboring transistors is likely to increase the integrator's capacitance by well over 50 fF. The higher capacitance would result in several problems (see Section 6.2).

Discharge noise results from not fully discharging the capacitor before the next integration period. If the capacitor is not fully discharged erroneous results occur because less charge is needed to trigger the next pulse. Discharge noise must be very small in order to preserve the high SNR. For the HSPICE V-to-F model listed in Section 4.3, the discharge transistor is on for approximately 2 ns and the RC time constant is approximately 0.25 ns. Therefore, eight time constants pass during the time the discharge capacitor is on, which is enough time to ensure that the discharge noise is miniscule.

FPN could also reduce the overall accuracy of the imaging array. FPN is caused by offsets between the ADCs. These offsets can be very significant. FPN is not just applicable to

V-to-F converters; it is an inherent problem with all pixel-level conversion regardless of the conversion method used. Therefore, FPN will be discussed more generally in Section 6.3.2.

4.6 Conclusion

There are many benefits to using a V-to-F pixel level ADC. The V-to-F design is very simple to build and understand. The basic V-to-F converter only needs nine transistors. The integrating capacitor is discharged multiple times per frame and therefore no well-depth limitation exists for the capacitor. Having no well-depth limitation allows the capacitor size to be as small as possible. The small circuitry area and capacitor size of the V-to-F converter allows the converter to meet the 60 μm $\times$ 60 μm size constraint.

In theory, it is possible to create a V-to-F converter that can digitize the analog voltage to n-bits, as long as the V-to-F converter can produce and count 2^n pulses per frame. In principle, however, this converter does not lead to true n-bit accuracy because other factors besides the number of quantization levels effect the accuracy. The comparator's threshold and propagation delay variations also effect the overall accuracy of the converter. For the pixel-level V-to-F converter presented in this chapter, it is possible to generate and count 2^{14} pulses at a frame rate of 5000 Hz. However, with the current technology it is not feasible to obtain 14-bit accuracy at this high frame rate, mostly due to the variation of the propagation delay and the threshold voltage of the comparator.

In general, the V-to-F converter is a good design for high light intensity applications, such as interferometry. However, significantly lower frame rates or SNR requirements are needed for an imaging array that uses pixel-level V-to-F converters to be successful.

5.0 Sigma-Delta Converter

5.1 Introduction

Chapter 5 further analyzes the pixel-level sigma-delta converter presented in Section 2.4. As a caution to the reader, Chapter 5 starts out using knowledge of the sigma-delta converter gained in Section 2.4. Therefore, Section 5.2 does not review the operations of the sigma-delta converter but instead dives into perhaps the most difficult subcircuit to understand, the digital-to-analog converter (DAC). The DAC is the key subcircuit in the sigma-delta converter because the accuracy of the DAC limits the overall accuracy of the sigma-delta converter. In Section 5.3, HSPICE simulations of a model pixel-level sigma-delta ADC are presented. These simulations aid in verifying the theory and in understanding the operations of the ADC. In Section 5.4 power dissipation is analyzed. Section 5.5 presents various factors that could reduce the accuracy of the sigma-delta converter. Finally, Section 5.6 discusses whether the sigma-delta converter could be used for the interferometer project.

5.2 Charge Transfer DAC

The purpose of the DAC in the sigma-delta converter is to transfer a fixed amount of charge onto the integrating capacitor every time an output pulse is produced (see Section 2.5 for background). A charge transfer DAC can transfer a fixed amount of charge using only two transistors and two clock signals (Figure 5.1).

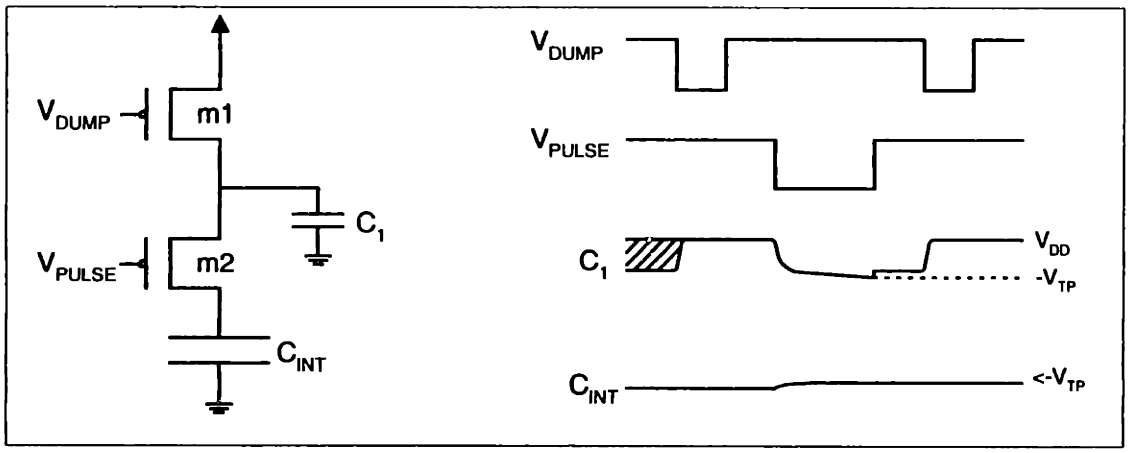

Figure 5.1: Charge Transfer DAC

The operation of the charge transfer DAC is as follows: V_{DUMP} pulses low for a short time period. The low pulse switches on transistor m1 causing current to charge up the parasitic capacitor C_1 until its voltage difference reaches V_{dd}. After V_{DUMP} returns high, depending on the output from the sigma delta converter, V_{PULSE} will either pulse low for several nanoseconds or remain high for the entire sample. If the output of the sigma delta converter is low, V_{PULSE} remains high for the entire clock cycle and no charge is transferred into the integrating capacitor, C_{int}. On the other hand, if the output of the sigma delta converter is high for a given sample then V_{PULSE} transitions low, turning on transistor m2 in the process. Due to the fact that C_{int} is at a lower potential than V_{dd}, the charge on C_1 flows into C_{int}. The charge continues to flow until either V_{PULSE} transitions high or the potential across C_1 is so low that the transistor m2 reaches cutoff.

The voltage at which a PMOS transistor shuts off is when $V_G - V_S = -V_{tp}$. Substituting the values $V_G = 0$ and $V_S = V_{C1}$, M2 reaches cutoff when the voltage across C_1 is $-V_{tp}$(0.63 V using MOSIS 0.35 μm technology parameters). Therefore, to avoid charge sharing, C_{int} is designed so that during charge transfer its voltage is always less than $-V_{tp}$. Charge sharing leads to an inconsistent amount of charge being transferred into C_{int}. Inconstancies in the DAC limit the overall accuracy of the sigma-delta converter.

In principle, charge transfer from C_1 into C_{int} is stopped because the voltage across C_1 becomes so low cutoff occurs. In that ideal case, the amount of charge dumped into C_{int} is fixed at $(V_{dd} + V_{tp}) \times C_1$. However, because the current flowing through a transistor decreases rapidly the closer to cutoff, m2 never quite reaches cutoff. Therefore, the amount of charge dumped on C_{int} is not fixed at $(V_{dd} + V_{tp}) \times C_1$, but is dependent on the current through m2 and the amount of time V_{PULSE} was held low. As discussed in Section 2.4.2, the dependence on current and time leads to shot noise effects. A benefit of the charge transfer DAC is the longer V_{PULSE} is low, the less shot noise is introduced. Unfortunately, it is difficult to quantify the shot noise reduction.

In order to meet the design goals, the charge transfer DAC not only has to produce a fixed amount of charge with relatively little shot noise, it also must be designed to transfer a fairly specific amount of charge. The amount of charge dumped is dependent on C_1. There are three main parasitic capacitances associated with a transistor: the drain capacitance, the source capacitance and the gate capacitance. The gate capacitance is generally several times larger than either the drain or the source capacitance, but does not effect the charge transfer DAC. For the charge transfer DAC, the capacitance of C_1 is determined by the drain capacitance of m1 (C_{dM1}) and the source capacitance of m2 (C_{sM2}).

Figures 5.2a – 5.2b show one cycle of an HSPICE simulation of the charge transfer DAC. Figure 5.2a shows the V_{DUMP} and V_{PULSE} verses time, whereas Figure 5.2b shows the voltage across C_1 and C_{int} verses time. As can be seen from the figures, as soon as V_{PULSE} goes low, charge is transferred from C_1 into C_{int}, which lowers the voltage across C_1 (V_1) and raises the voltage across C_{int} (V_{int}). Once V_{PULSE} switches high, charge transfer stops and the voltage across C_1 jumps from about 0.9 V to 1.25 V. The reason for this jump is because the parasitic capacitors of m2 act like a voltage divider between the V_1 and V_{PULSE}.

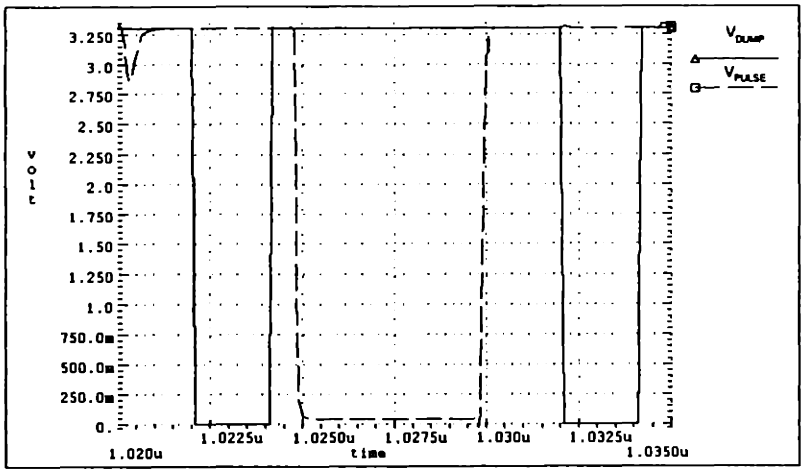

Figure 5.2a: HSPICE Model of DAC Clock Pulses

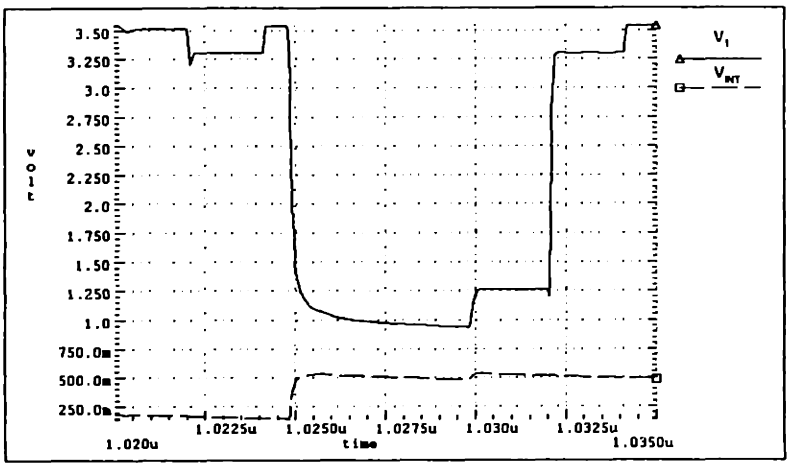

Figure 5.2b: HSPICE Model of DAC Voltages

5.3 HSPICE simulations

A 6-bit sigma-delta converter was designed and examined using HSPICE. The purpose of the model was to better understand, discover potential problems and verify the operation of the pixel-level sigma-delta converter. The 6-bit sigma-delta converter model could easily be upgraded to a higher bit converter by adding more registers to the counter; however, a 6-bit

converter is sufficient to satisfy the model's purpose. The HSPICE source file is listed in Appendix D.

A schematic of the 6-bit converter is shown in Figure 5.3. As can be seen from the Figure 5.3, the sigma-delta converter utilizes a comparator made from a series of inverters with V_{dd} = 1.0 V and V_{ss} = -0.2 V. The voltage values are designed to eliminate short circuit power dissipation (Section 4.2), and to insure that the voltage across C_{int} is low enough so that the DAC operates correctly (Section 5.2). For example, if V_{ss} were tied to ground, the comparator would trigger at V_{tn}. The comparator triggering would cause the DAC to dump charge into C_{int}. However, because the voltage difference between V_{tn} and $-V_{tp}$ is usually small and the voltage across C_{int} at the time of charge transfer could be as much as V_{tn}, the DAC could easily charge C_{int} past $-V_{tp}$. C_{int} being charged past $-V_{tp}$ would lead to charge sharing. The only way to avoid charge sharing is either lowering V_{ss} or if $-V_{tp}$ was sufficiently greater than V_{tn}. If, for instance, $-V_{tp}$ is 0.2 V larger than V_{tn}, then the DAC would operate properly even if V_{ss} were tied to ground, which would lead to a much easier circuit implementation.

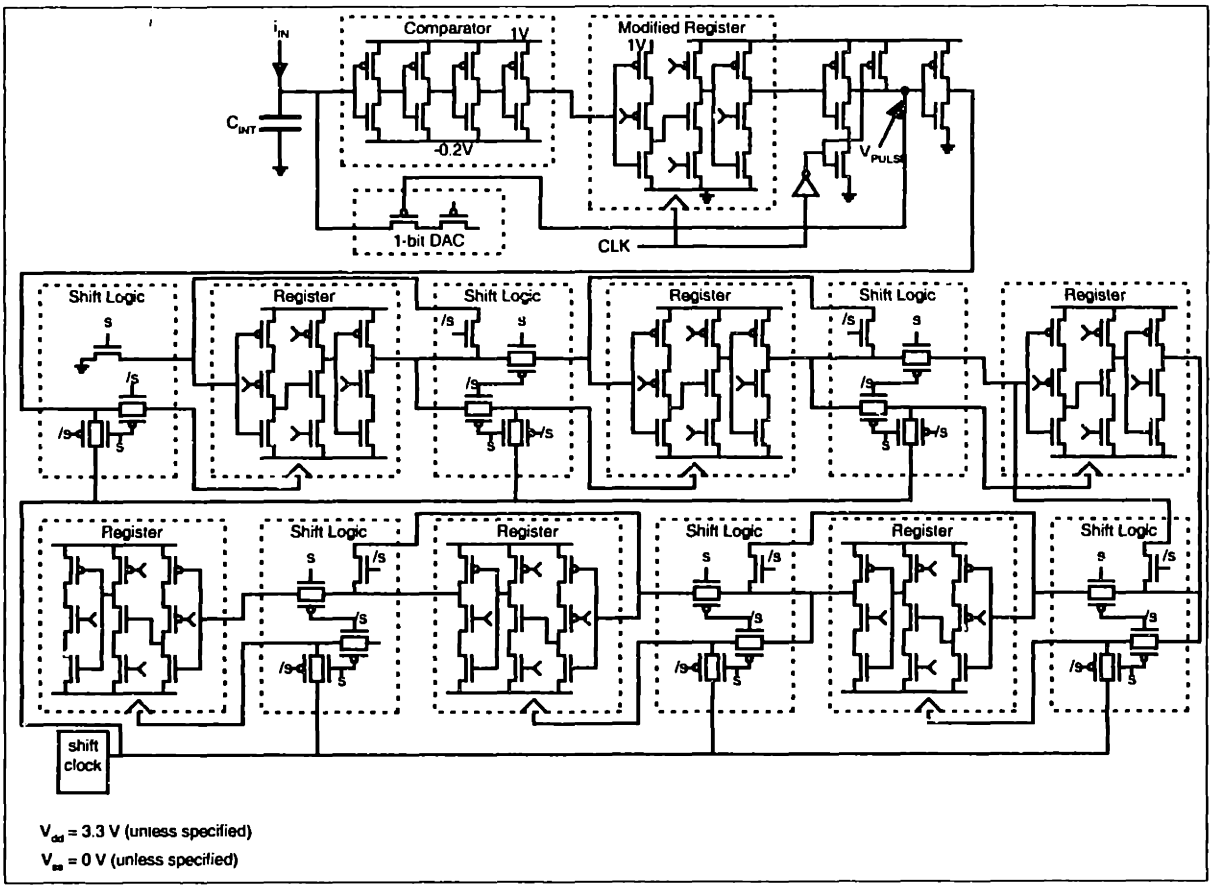

Figure 5.3: 6-Bit Sigma-Delta Converter Schematic

The 1 V power supply of the comparator would normally lead to a problem producing a pulse with enough voltage to increment the counter and to signal the DAC; however, the output of the comparator is fed into a modified inverting register. A slight modification of the nine-transistor inverter register discussed in Section 3.2 allows an input of -0.2 V and 1 V to produce an output of 3.3 V and 0 V respectively. The register was changed in the following manner, two transistors were widened and a 1 V instead of the usual 3.3 V power supply was attached to the source of a PMOS transistor.

The operation of the 6-bit HSPICE sigma-delta converter model is summarized below. Incoming photocurrent causes the voltage across C_{int} to slope downwards. This voltage is compared to a reference voltage, V_{REF}, that is determined by $V_{ss} + V_{tn}$ (0.38 V for the HSPICE model). The output of the comparator is fed to an inverting register that is driven by a clock

signal, CLK. The output of the register and /CLK are NANDed together to produce a signal V_{PULSE} which is used by the DAC and the counter.

An example of the model sigma-delta converter is as follows. If the voltage across C_{int} is higher than V_{REF}, the comparator output is high which, upon CLK's rising edge, causes a low signal on the output of the modified register. The low register output produces a high V_{PULSE} signal. When V_{PULSE} is high, no charge is dumped from the DAC and the counter is not incremented. V_{PULSE} will remain high until the voltage across C_{int} becomes lower than V_{REF}. When this happens, the low comparator output causing the register to be high upon the rising edge of CLK. The high register output causes V_{PULSE} to transition and stay low until the falling edge of CLK. The low V_{PULSE} signal causes the counter to be incremented and causes the DAC to transfer a fixed amount of charge onto C_{int}. The extra charge causes the voltage across C_{int} to rise past V_{REF} and the cycle repeats for the rest of the integration period.

Tests were conducted on the individual subcircuits of the sigma-delta converter focusing on the DAC, comparator, and the counter. After numerous simulations had verified the correct operation of these subcircuits, higher order functions were examined. Tests concluded a circuit that combined the comparator, the register, and the NAND gate generated output pulses correctly. A different set of tests also concluded that the pulses generated by the sigma-delta converter successfully incremented the counter and caused the DAC to transfer charge into C_{int}. Furthermore, readout simulations were conducted to verify that the counter could also act as a shift-register. The readout simulations also had positive results.

The rest of this section describes and depicts some of the HSPICE simulations. Figure 5.4 shows an HSPICE simulation of the voltage across C_{int} and the signal $/V_{PULSE}$. As one can see from the figure, the voltage across C_{int} decreases linearly until $/V_{PULSE}$ transitions high. When $/V_{PULSE}$ transitions high, a fixed amount of charge is dumped onto C_{int}. The experiment used an incoming current of 120 nA and ran for 1400 ns. During the experiment, 28 pulses were produced, for an average of a pulse every 50 ns. A $/V_{PULSE}$ pulse every 10 ns is possible, so this

model is design for a maximum input current of 600 nA, which is a few time higher than the design specifications for Lincoln Laboratory's advanced interferometer project. However, the maximum input current could be lowered by using a smaller capacitors in the DAC.

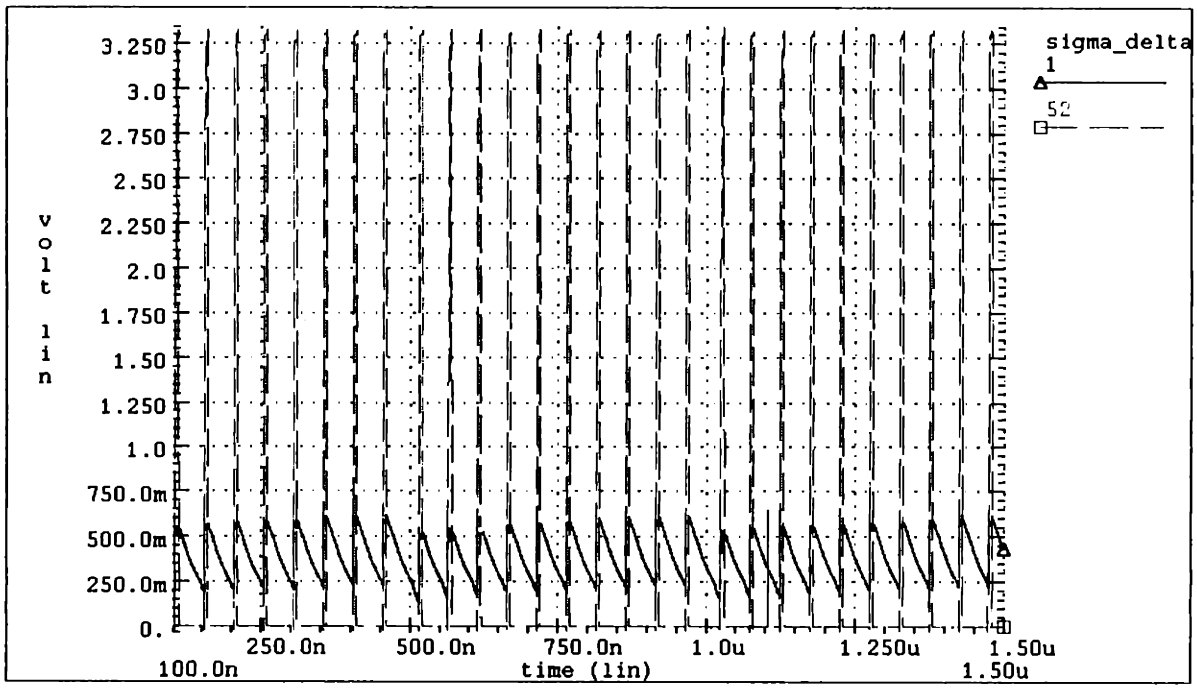

Figure 5.4: HSPICE Simulation of V_{int} & / V_{PULSE} vs. Time

Figures 5.5a – 5.5d display the voltage across C_{int} and the four least significant bits of the sigma-delta counter verses time. For the model ripple counter to operate correctly (decrease by one on every rising edge of /V_{PULSE}), its least significant bit (Figure 5.5a) should switch states upon the rising edge of /V_{PULSE}, or equivalently every time charge is transferred onto C_{int}. Also, every other state change of the first bit should lead to a state change in the second bit. Every other state change of the second bit should lead to a state change in the third bit, and so on down the line. From examining the Figures 5.5a-d one can verify that this counter is operating correctly. Another way to determine if the counter is operating properly is to list the output of the counter's binary bits along with the counter's decimal equivalent (Table 5.2). From examining

the Table 5.1, one can see that every time charge is transferred into C_{int}, the counter decreases by one.

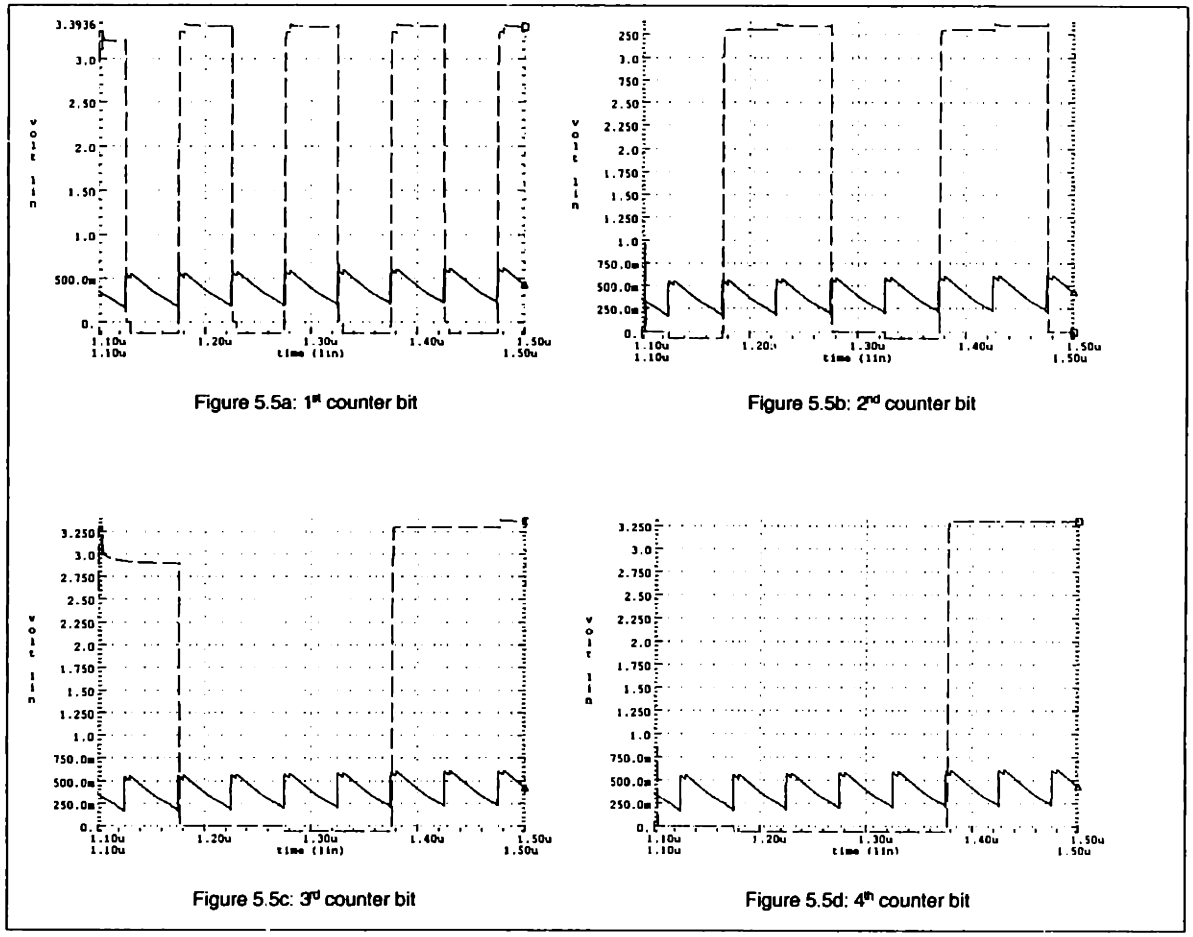

Figure 5.5a: 1st counter bit

Figure 5.5b: 2nd counter bit

Figure 5.5c: 3rd counter bit

Figure 5.5d: 4th counter bit

Figure 5.5: HSPCIE Model of the Four Least Significant Bits of the Counter

Table 5.1: First Four Least Significant Bits of the Counter

Charge Trans.	4^{th} LSB	3^{rd} LSB	2^{nd} LSB	LSB	Decimal
Start	0	1	0	1	05
1.10 μs	0	1	0	0	04
1.18 μs	0	0	1	1	03
1.23 μs	0	0	1	0	02
1.28 μs	0	0	0	1	01
1.33 μs	0	0	0	0	00
1.38 μs	1	1	1	1	15
1.43 μs	1	1	1	0	14
1.48 μs	1	1	0	1	13

Figures 5.6a – 5.6d display the shift signal and four bits of the ripple counter / shift register (RCSR) verses time. When the shift signal goes high the ripple counter switches to a shift-register for read out purposes. In this simulation, when the global shifting clock pulses high (every 10 ns increment), the output of the first readout bit is inverted and passed to the second readout bit. Simultaneously, the state of the second readout bit is inverted and passed the third readout bit and so on down the line. In the RCSR, the first readout bit would normally receive data from the last bit of the previous pixel, but because this simulation only has one converter, a high bit is always passed. Table 5.2 lists the data of the four readout bits upon the global clock's rising edges. At the start when the shift signal goes high, the first four bits are 1 1 0 0 respectively. Upon the rising edge of the global clock, a 1 is loaded into the first bit and bits 2 through 4 receive the inverted signal of their predecessors (e.g. 0 0 1). One can check the figure and the table and verify that the readout simulation was successful.

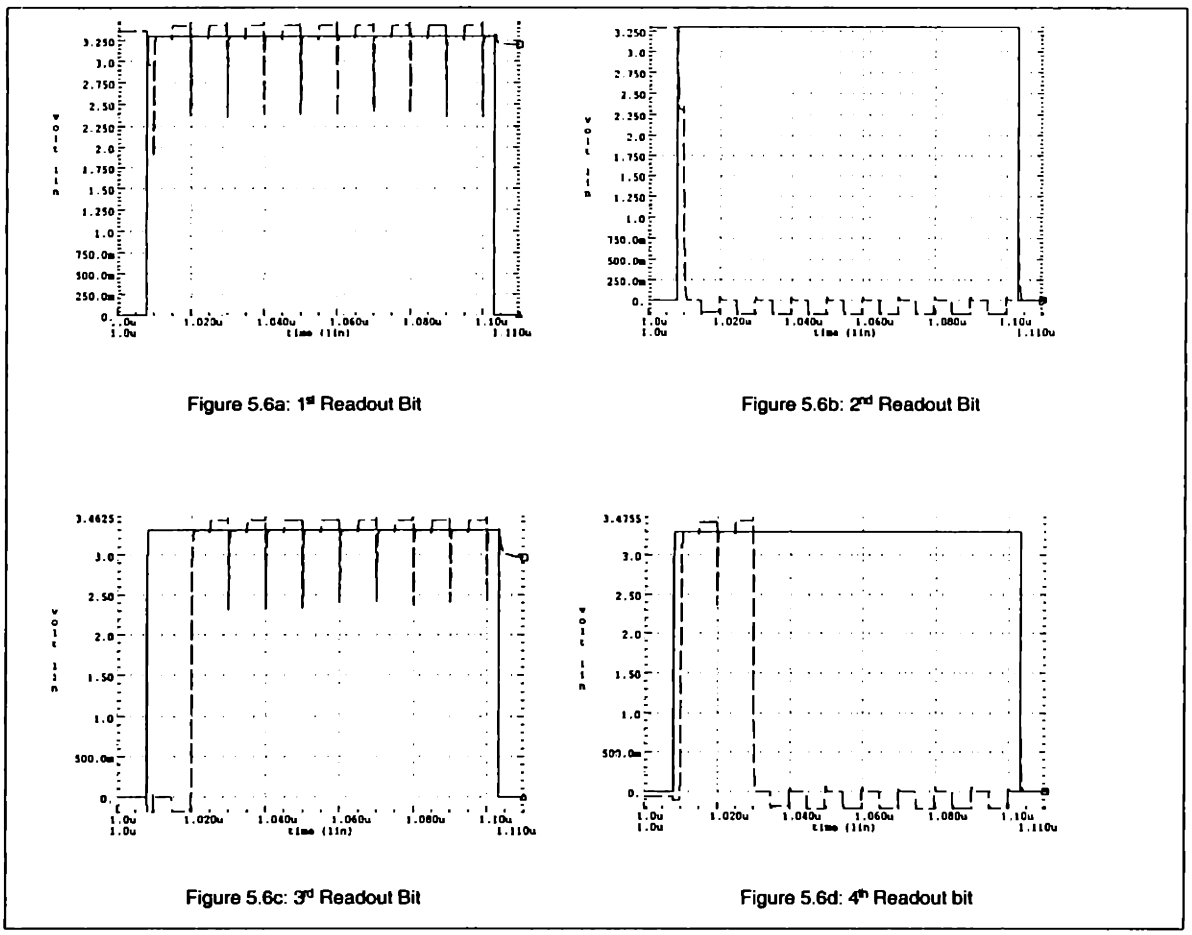

Figure 5.6a: 1st Readout Bit

Figure 5.6b: 2nd Readout Bit

Figure 5.6c: 3rd Readout Bit

Figure 5.6d: 4th Readout bit

Figure 5.6: HSPCIE Model of the Four Readout Bits of the Ripple Counter / Shift Register

Table 5.2: Data of Four Readout Bits of an HSPICE Simulation

↑ CLK	1st Bit	2nd Bit	3rd Bit	4th Bit
Start	1	1	0	0
1.01 μs	1	0	0	1
1.02 μs	1	0	1	1
1.03 μs	1	0	1	0
1.04 μs	1	0	1	0
1.05 μs	1	0	1	0
1.06 μs	1	0	1	0
1.07 μs	1	0	1	0
1.08 μs	1	0	1	0
1.09 μs	1	0	1	0
1.10 μs	1	0	1	0

5.4 Power Dissipation

There are many subcircuits used to construct the sigma-delta converter. To estimate the total power consumption of the sigma-delta converter, one can add the power of the subcircuits. These subcircuits can be broken down into a comparator, a register, a DAC, a NAND gate, an inverter and a counter / shift-register. As in Chapter 3, for a first order approximation, the total power dissipation can be estimated by calculating the dynamic power dissipation (P_{dyn}). The dynamic power dissipation can be computed using the equations listed in Section 3.3.

An estimate of the power dissipated by the register of the sigma-delta converter can be calculated by using the following numbers (from Appendix A),

C = 1 fF
N / register = 6.5
V_{dd} = 3.3 V
F = $2^{14} \times 5000$
registers / array = 256×256

and applying equation 3.1 and 3.2. This calculation leads to a power dissipation estimate of 380 mW.

The power dissipation of the NAND gate and the inverter can be analyzed together using the same numbers as for the register except that the capacitors on average are only charged three times per clock cycle instead of 6.5. Therefore, the dynamic power dissipation estimate is 175 mW. Similarly, the power dissipation of the DAC uses the same values as the register, except the DAC only has two transistor that have parasitic capacitors getting charged once per clock cycle (under maximum flux). This leads to a power dissipation of approximately 117 mW.

The comparator of the sigma-delta converter uses the same circuitry as the V-to-F converter discussed in Section 4.2. The estimated power dissipation of the comparator was computed to be 31 mW.

Finally, the last subcircuit, the counter / shift-register, has already been analyzed in Chapter 3. Using the non-sequential counter / shift register (NSCSR) readout method, the power dissipation is approximately 5.8 W. Using the RCSR readout method, the power dissipation is approximately 0.97 W. Therefore, the total dynamic power dissipation estimate of the sigma-delta converter using the RCSR readout method is 1.67 W.

5.5 Accuracy

In principle, by having a range of 2^{14} pulses in a signal frame period and having a 14-bit counter, the sigma-delta converter can achieve14-bit accuracy. However, like the V-to-F converter, the sigma-delta converter runs into many practical problems. The main problems are DAC and comparator inconsistencies and FPN.

Inconsistencies in the DAC directly effect the overall accuracy of the sigma-delta converter. If the amount of charge that the DAC transfers has a variance greater than 0.006% ($\frac{1}{2^{14}}$), the sigma-delta converter does not achieve true 14-bit accuracy. There are two major factors that cause variance in the amount of charge transferred by the DAC. The first factor is that the DAC has some shot noise, although, as discussed in 5.2, the DAC's shot noise is less than the inherent shot noise of the detectors. The other major factor is that when using the charge transfer DAC, power supply noise directly effects the amount of charge transferred. Therefore, unless the DAC's power supply voltage is virtually noise free, the accuracy of the sigma-delta converter suffers.

Comparator inconsistencies also cause the sigma-delta converter's accuracy to suffer. As previously mentioned, fluctuation in the comparator are reduced over time. However, these fluctuations could lead to the least significant bit(s) of the sigma-delta converter being incorrect if the frame ends before the comparator error was fixed. If the integrating capacitor can be designed to be under 20 fF, comparator fluctuations would probably only effect the least

significant bit sporadically. However, if the integrating capacitor is larger than 20 fF the least significant bit(s) are effected with more frequency (see Section 6.2).

FPN is present in all pixel-level converters and can lead to a significant accuracy reduction (see Section 6.3.2). However, FPN in the sigma-delta converter is larger than in other converter methods because the DAC relies on parasitic capacitance. Parasitic capacitance greatly varies between transistors; therefore, the amount of charge transferred will also vary greatly between DACs. Nonetheless, there are methods of greatly reducing FPN (Section 6.3.2).

5.6 Conclusion

The sigma-delta converter is most promising pixel-level ADC for the interferometer project. The sigma-delta converter circuitry can be built in fewer than 30 transistors (excluding the counter). The integrating capacitor is discharged multiple times per frame and therefore no well-depth limitation exists for the capacitor. Having no well-depth limitation allows the capacitor size to be as small as possible. Similar to the V-to-F converter, the small circuitry area and capacitor size of the sigma-delta converter allows it to meet the 60 μm × 60 μm size constraint.

Besides meeting the size constraint the sigma-delta converter has additional benefits. Unlike the V-to-F converter, comparator fluctuations of the sigma-delta converter are corrected over time. Also, the sigma-delta converter has a higher tolerance than the V-to-F converter for the size of the integrating capacitor. The sigma-delta converter could work well with an integrating capacitance of 20 fF. In contrast, to work well, the V-to-F converter needs an integrating capacitance below 10 fF. Another benefit is that the sigma-delta converter does not have any reset noise. During integration mode, the incoming photocurrent is constantly measured.

Along with the benefits there are still numerous problems with the sigma-delta converter. Power dissipation is about 1.5 times greater than the V-to-F converter. The sigma-delta converter needs multiple clock signal and voltage levels to operate correctly. The many different clock signals and voltages setting may be impractical to implement accurately and cost effectively. Power supply noise directly effects the accuracy of the DAC. If the DAC cannot transfer a fixed amount of charge with very high precision, the overall accuracy of the converter will fall below specifications. Also, comparator inaccuracies might not be fixed by the end of a frame period. These inaccuracies can lead to errors in the least significant bit(s) of the counter.

After an in-depth analysis of the pixel-level sigma-delta converter, the converter still demonstrates potential be a solution for the interferometer project. However, the power dissipation must be reduced and to obtain the 14-bit accuracy desired, numerous problems need to be solved.

6.0 Obstacles

The last two chapters analyzed the operation of the V-to-F and sigma-delta converters. Both chapters focused mostly on the plausibility of a single, pixel-level ADC meeting the specifications of Lincoln Laboratory's advanced interferometer. This chapter, on the other hand, carefully examines the major obstacles of not only the individual ADCs, but also of combining thousands of ADC's on a single imaging array.

These major obstacles include high power dissipation levels (Section 6.1), large parasitic capacitance sizes (Section 6.2), additional noise sources (Section 6.3) and multiple clock signals and voltage sources (Section 6.4). A method of solving or reducing the problems associated with the obstacles in this chapter should be contemplated thoroughly before a pixel-level conversion prototype is considered.

6.1 Power Dissipation

Power dissipation must be kept at a minimum for the imaging array of Lincoln Laboratory's advanced interferometer project because in order to receive the necessary performance, the detectors need to be cryogenically cooled. To keep cost reasonable, the imaging array should not dissipate more than 0.2 W of power[1].

The counter / readout method alone dissipates far more power than allowable. The RCSR method dissipated an estimated 0.97 W of power, whereas the NSCSR dissipated 5.8 W of power (over 25 times the acceptable power dissipation). These power estimates do not include multiplexing data from off the imaging array into memory, which depending on the multiplexing structure may add significant power dissipation to the cryogenically cooled circuit.

The power dissipation for the ADC circuitry of the V-to-F and sigma-delta converters using the RCSR method is an estimated 1 W and 1.67 W respectively. This power dissipation estimate does not include short circuit power dissipation or any extraneous hardware that could be

needed, such as buffers. Therefore, in reality the estimated power dissipation is a minimum estimate, and the actual figures are likely to be significantly higher.

In order to reduce the power dissipation, one of the following must be decreased: the power supply voltage, the capacitance, the frequency, or the number of capacitors being charged. For the interferometer project, the frequency and number of capacitors being charged is fixed, so the only variables are the power supply voltage and the capacitance. The dynamic power dissipation decreases with the square of the power supply voltage, and the capacitance decreases with smaller fabrication processes. Therefore, in order to reduce the power dissipation to an acceptable level, there has to be a significant improvement over current technologies.

6.2 Capacitor Size

To work well for the interferometer project, both the sigma-delta and the V-to-F conversion schemes require a very small integrating capacitor (on the order of ten femtofarads). In the case of the V-to-F converter, for the overall precision not to be noticeably affected by comparator inaccuracies, the variance of the comparator noise should be less than 55 e^- per count (see Section 4.5). A fixed amount of charge creates a greater voltage difference across a smaller capacitor than a larger capacitor. Thus, the smaller the V-to-F integrating capacitor, the greater the allowable comparator noise. Table 6.1 shows the trigger voltage of the V-to-F comparator and effect of 55 e^- across a capacitor for various integrating capacitor sizes. As one can see from the table, for a 1 fF capacitor the allowable comparator variation is 8.8 mV, whereas for a 100 fF capacitor it is 0.09 mV. Constructing a comparator with a variance of less than 8.8 mV is plausible but constructing one with less than a 1 mV variation is doubtful. Therefore, in order for comparator threshold variations not to diminish the overall accuracy of the V-to-F converter, the integrating capacitor must be less than 10 fF.

Table 6.1: Capacitor Size Vs. Allowable Comparator Variation

Capacitor Size	Comparator Threshold Voltage	Allowable Comparator Variation
1 fF	1.95 V	8.80 mV
5 fF	0.39 V	1.76 mV
10 fF	0.20 V	0.88 mV
50 fF	0.04 V	0.18 mV
100 fF	0.02 V	0.09 mV

Not only does a higher capacitance effect the allowable comparator variations, it also greatly increases the comparator propagation delay. The larger the comparator propagation delay, the more electrons per pulse are not being counted and thus the larger the reset noise. For example, assume that the comparator has a 1 ns propagation delay once the voltage difference between the comparator's threshold voltage (V_{ref}) and V_{int} is 0.02 V. If the integrating capacitor is 1 fF and V_{int} rises to the comparator's threshold voltage of 1.95 in 10 ns, it will take 0.1 ns until the voltage difference between V_{ref} and V_{int} is 0.02 V. It then takes an additional 1 ns propagation delay for the comparator to trigger and another 1 ns propagation delay before the capacitor stops discharging. Thus, a total of 82.6% of the time the incoming electrons were counted. However, if instead a 50 fF integrating capacitor is used with the same input current, it will take 10 ns to reach the comparator's threshold voltage of 0.04 volts. It then takes another 5 ns until V_{int} is 0.02 V above V_{ref} and an additional 2 ns delay for triggering the comparator and discharging C_{int}. Thus, the electrons were counted only 58.8 % of the time.

The sigma-delta converter is also effected by a large integrating capacitance. As with the V-to-F converter, a sigma-delta converter using a relatively large integrating capacitor (i.e. 100 fF) most likely will have a comparator propagation delay of greater than 10 ns, especially for low light intensity situations. If the comparator propagation delay is greater than 10 ns (the duration of a sigma-delta sample) and V_{int} goes lower than V_{ref}, it will take more than one clock cycle for the comparator to go high and trigger a pulse that increments the counter and starts the DAC. Once the comparator goes high and a pulse is triggered, it will also take more than one clock

cycle for the comparator to return low and stop triggering pulses. Therefore, with longer comparator delay pulses come in increments of two or more. Multiple pulse triggerings are a problem because at the end of a frame the count is likely to be off by one or two least significant bits. This phenomenon is portrayed in Figure 6.1. Figure 6.1 was created using an HSPICE simulation of the model sigma-delta converter discussed in Section 5.3 except with an integrating capacitor of 100 fF.

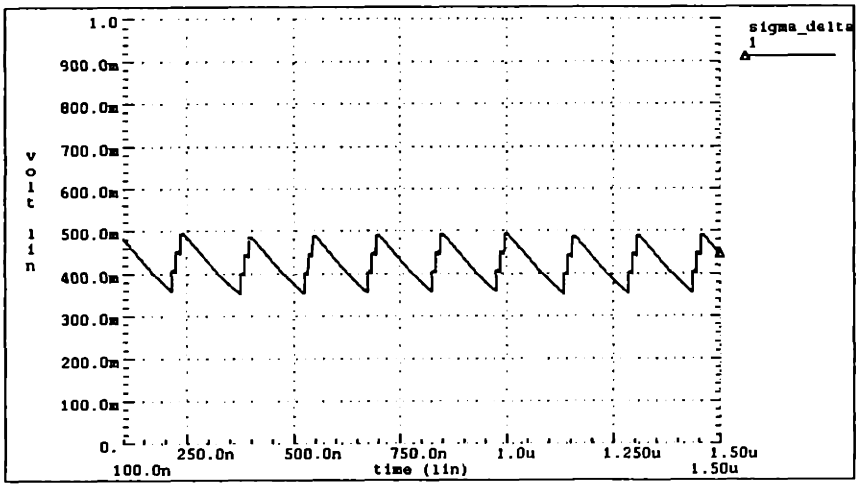

Figure 6.1: HSPICE Simulation of a Sigma-Delta Converter with a 100 fF Capacitor

The V-to-F and sigma-delta converters would not have a capacitor size problem if the integrating capacitor could be made small enough (under 8 fF for the V-to-F converter). However, the bump bond used in attaching the detectors to the imaging array along with the neighboring transistors greatly increases the integrating capacitance. For example, a bump-bonding technique very similar to the bump-bond technique that could be used in Lincoln's Interferometer project created a 200 fF parasitic capacitance[8].

In order for the pixel-level V-to-F and sigma-delta converter to be a success, the parasitic capacitance from bump bonding and neighboring transistors must be reduced. Reducing the parasitic capacitance under 8 fF, which is needed for the V-to-F converter to operate correctly, is unlikely to happen in the near future. The allowable parasitic capacitance for the sigma-delta

converter to operate correctly can be a little higher (around 20 fF). However, if one can tolerate a probable least significant bit error, the allowable parasitic capacitance for the sigma-delta converter could be as much as 100 fF, which should be obtainable in the near future.

6.3 Noise Sources

There are some noise sources that are non-existent in a single ADC, but lead to major problems when there are hundreds or thousands of ADCs on the same imaging array. The two main noise sources are power supply noise (Section 6.3.1) and FPN (Section 6.3.2). Both the power supply noise and FPN are difficult to quantize because an imaging array with hundreds of ADCs is too complicated to model using HSPICE simulations, not enough pixel-level imaging array experiments have been done to provide an example, and a good estimation technique is not known. Therefore, rather than trying to estimate the amount of noise that will be generated, some causes and effects of power supply noise and FPN will be described in this section.

6.3.1 Power supply noise

Power supply noise is caused by the power supply voltage and the ground voltage varying instead of staying constant at V_{dd} or ground. The main contribution to power supply noise is digital switching. Digital switching occurs when numerous circuits draw current simultaneously. The power supply cannot handle the large amount of current drawn in such a short time frame. As a consequence, the power supply voltage is lowed. In the interferometer project, during read out over 4 million transistors are clocked at the same time. A large percentage of these transistors try to draw current from the power supply. The power supply voltage cannot handle the sharp transition from comparatively no current being drawn to an immense amount of current being drawn. Therefore, the power supply voltage will be lowered.

The power supply noise could have drastic effects on the accuracy of the individual sigma-delta converters during integration mode and on the precision of data transfer during the read out mode. During integration mode power supply noise must be virtually non-existent, because it directly effects the consistency of the DAC and in turn the ADC. During the read out mode, the values held in the shift registers are digital, so a lot of power supply noise can be tolerated.

Although it is extremely hard to eliminate power supply noise in all cases, solutions exist which can reduce the magnitude of the noise. Circuits that need very consistent power can be connected to a separate power line from the rest of the circuit. Shielding could be placed between different power lines (although this could be very difficult). A clock skew could be introduced between columns so that far fewer transistors would be drawing power simultaneously. These techniques and more are discussed in greater detail in Reference 9.

6.3.2 – Fixed Pattern Noise

FPN is caused by offset differences between the ADCs within an imaging array. The current standard imaging array is comprised of only one or a few different ADCs, so FPN is very small or non-existent. However, with pixel-level conversion, there are thousands of different converters, which leads to large FPN. The magnitude of the offset varies with the conversion method used. For example, the FPN of the V-to-F converter mostly depends on the difference between comparator threshold voltages. Comparator threshold voltages are determined by V_{tn}, which remains fairly consistent between transistors. Therefore, the FPN between ADC will be comparatively small. On the hand, the FPN of the sigma-delta converter mostly depends on the amount of charge the DAC transfers onto C_{int}. This amount of charge is dependent on the parasitic capacitors of two transistors. From pixel to pixel, the parasitic capacitance of two

transistors is far less constant than V_{tn}. Thus, the FPN of the sigma-delta converter is larger than that of the V-to-F converter.

It is hard to estimate the FPN for the proposed ADCs; however, a prototype of a sigma-delta pixel-level converter built by Stanford had a FPN of 1%[2]. Unless corrected, a 1% offset difference between pixel converters could lead to a drastic reduction of the overall accuracy of the imaging array. Fortunately, there are methods of reducing the FPN. One method tests the imaging array at a constant light intensity. These results are used to determine the relationship between the various converters. When the actual data is available, the relationship between the converters is taken into account.

6.4 Multiple Clock Signals and Voltage Supply Levels

Another major obstacle is that the pixel-level ADCs and readout methods discussed in this thesis require multiple clock signals and voltage supply levels. The V-to-F and sigma-delta converters require four different voltage supply levels, two more than normal imaging arrays. Wiring these four power supplies to each of the thousands of ADCs will greatly add to the complexity of the circuit.

The two different counter / readout methods discussed only require two power supplies (ground and 3.3 V), however, they require several clock signals. The RCSR requires a switch clock, a /switch clock, a global shifting clock, and possibly a delay clock. The switch and /switch clock run at 5000 Hz and drive 98 transistors per ADC. The global shifting clock runs at speeds of at least 100 MHz and drives 14 transistor per ADC. A delay clock is necessary to insure that the ripple counter is allowed sufficient time for the data to settle before being shifted off the chip (see Section 3.4). The delay clock is not necessary if the ripple counter's propagation delay is small enough to ensure that the data will be settled before being shifted off-chip. The NSCSR

also requires a switch clock, a /switch clock, and a global shifting clock. However, the clocks need to drive far less transistors per converter and a delay clock is not necessary.

In addition to the three or four clock signals needed for the counter / readout method, the sigma-delta converter needs another two clock signals, the sample clock and the DAC clock. In some situations, the global shifting clock could be wired to the sample clock to reduce the additional clock signals needed by one. In total for a sigma-delta converter and a V-to-F converter using the RCSR method, three to six different clock signals are needed.

Multiple clock signals can lead to major problems that include additional wiring complexity, cross talk between signals, and greater power dissipation. These factors will in turn increase the effort and cost of producing a successful imaging array.

7.0 Conclusion / Future work

This thesis has explored six different types of pixel-level ADCs and three readout methods for Lincoln Laboratory's advanced imaging array. Out of the methods investigated, the simple filtering sigma-delta converter and the RCSR readout method were the best suited for the imaging array.

The sigma-delta converter combined with the RCSR demonstrates potential to be successful for the imaging array of interferometer project. It is small enough to fit within the allotted space, it can obtain the necessary 2^{14} different quantization levels per frame, and the comparator does not degrade the SNR.

However, before one starts to build an imaging array using pixel-level sigma-delta converters, there are many problems that should first be considered. Power dissipation is high: for the 256×256 imaging array using sigma-delta converter with the RCSR readout method, an estimated minimum of 1.67 W is dissipated under full illumination. The estimated power dissipation is a bare minimum that does not include short circuit power dissipation, leakage power dissipation or any extraneous hardware that could be needed such as buffers. Already, the estimated power dissipation is over 8 times greater than the allowable power dissipation and likely to be much more.

The power dissipation is not the only problem with the imaging array design. Power supply noise, DAC inaccuracies, threshold variations and other noise sources will most likely reduce the SNR significantly. It would be surprising to receive more than 12-bits of true accuracy without substantial funding and improvements in technology. If less than 12-bits of true accuracy were received the advantages of using pixel-level converters rather than multiple off-chip converters diminish.

Due to the facts that pixel-level conversion is not an established technology and the different methods in this thesis are problematic, Lincoln Laboratory should not pursue pixel-level

conversion for the advanced interferometer project or for other projects that are to be completed in the next few years. However, the idea of pixel-level conversion should not be discarded. In the future, with technological improvements, imaging arrays using pixel-level conversion could revolutionize the industry. Imaging arrays using pixel-level conversion could be more accurate, smaller, and cheaper than current imaging array methods that use off-chip converters. Therefore, although developing an imaging array prototype using pixel-level conversion would probably not be advantageous for Lincoln's advanced interferometer project, it could be extremely beneficial for less demanding or future imaging arrays.

Building a prototype 16 × 16 imaging array capable of 10-bit conversion at low frame rates would be a good first step towards developing a useful pixel-level conversion method. A prototype of this magnitude is small enough in size to be relatively inexpensive, while complex enough to produce valuable information. Constructing a prototype would provide concrete evidence as to whether or not imaging arrays using pixel-level have the potential to revolutionize the industry.

Appendix A

Dynamic Power Dissipation Parameters

C	→ The average capacitance
N / Register	→ The number of capacitors to be charged per register
V_{dd}	→ Power supply voltage
F	→ The frequency at which the capacitors are charged
Pixels / Array	→ Number of pixels per array
Register / Pixel	→ Number of registers per pixel

C – As a rough estimate, the average capacitance is formed from two transistor's parasitic capacitance. Therefore, an estimated 2 gate, 2 source and 2 drain capacitance are combined to calculate the total capacitance. Using the Mosis 0.35 μm technology on a minimum transistor, the approximate gate capacitance is 1.1 fF and the approximate source capacitance and drain capacitance are both 0.5 fF. From these numbers, C should be 4.2 fF instead of the listed 1 fF. However, using more advance technology such as a 0.1 μm, a C of 1 fF is reasonable.

N / Register – For the inverting register there are 4 clock inputs that have parasitic capacitance that get charged every clock cycle. In addition, depending on the state transitions, other capacitors might get charged: low-to-low transition (3 extra), low-to-high transition (2 extra), high-to-low (5 extra), high-to-high (0 extra). There is an equal probability for any of the four state changes in the NSCSR, the RCSR (readout), or the ΣΔ Register. Therefore, the average N / Register is 4 (from the clock) + 2.5 (from the state transitions). The RCSR integration only has low-to-high or high-to-low transitions. Therefore, the average N / Register is 7.5. The Comparator is comprised of four inverters, each with parasitic capacitance that must get charged.

V_{dd} – The power supply voltage is 3.3 V except for the comparator which is 1.2 V.

F – There can be a maximum of 2^{14} pulses per frame with frame rates of 5000 Hz. Therefore, during integration the maximum frequency per pixel is $2^{14} \times 5000$. During readout all the bits must be shifted off the array each frame. The bits are shifted off the array in rows that contain 256 pixels. At frame rates of 5000 Hz, the bits in each pixels are shifted at frequencies of 256×5000 Hz.

Pixels / Array – There are 256×256 pixels in an array

Register / Pixel – For the NSCSR all 15 registers in a pixel dissipate power each cycle. For the RCSR on average only 2 registers per pixel dissipate power each cycle. There is only one comparator and one ΣΔ Register per pixel that dissipates power each cycle.

	NSCSR (p. 31)	RCSR (p. 34)	Comparator (p. 39)	ΣΔ Register (p. 58)
C	1 fF	1 fF	1 fF	1 fF
N / Register * N / Comparator	7.5	7.5 (Integration) 6.5 (Readout)	4*	6.5
V_{dd}	3.3 V	3.3 V	1.2 V	3.3 V
F	$2^{14} \times 5000$ Hz (Int) 256×5000 Hz (R)	$2^{14} \times 5000$ Hz (Int) 256×5000 Hz (R)	$2^{14} \times 5000$ Hz	$2^{14} \times 5000$ Hz
Pixels / Array	256×256	256×256	256×256	256×256
Register / Pixel * Comp / Pixel	15	2 (Integration) 14 (Readout)	1*	1

Appendix B

MOSIS PARAMETRIC TEST RESULTS

RUN: N7CU VENDOR: HP-NID
TECHNOLOGY: SCN035H FEATURE SIZE: 0.35 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: Hewlett Packard GMOS10QA.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.60/0.4			
Vth		0.73	-0.66	Volts
SHORT	3.6/0.4			
Vth		0.74	-0.68	Volts
Vpt		10.0	-8.8	Volts
Vbkd		9.4	-6.9	Volts
Idss		494	-252	uA/um
WIDE	10/0.4			
Ids0		1.2	-0.4	pA/um
LARGE	3.6/3.6			
Vth		0.74	-0.72	Volts
Vjbkd		9.3	-8.4	Volts
Ijlk		-21.5	-4.6	pA
Gamma		0.48	0.55	V^0.5
Delta length (L_eff = L_drawn-DL)		-0.06	0.08	microns
Delta width (W_eff = W_drawn-DW)		0.21	0.16	microns
K' (Uo*Cox/2)		108.8	-24.0	uA/V^2

COMMENTS: Delta L varies with design technology as a result of the different mask biases applied for each technology. Please adjust the delta L in this report to reflect the actual design technology of your submission.

Design Technology	Delta L
SCN4M_SUBM (lambda=0.2), HP_CMOS10QA	no adjustment
SCN4M (lambda=0.25)	subtract 0.1 um

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	MTL4	UNITS
Sheet Resistance	3.1	2.8	2.6	0.06	0.06	0.06	0.03	ohms/sq
Width Variation (measured - drawn)	-0.16	-0.12	-0.00	-0.02	-0.12	-0.16	0.04	microns
Contact Resistance	2.8	2.7	2.4		0.90	0.69	0.90	ohms
Gate Oxide Thickness	76							angstrom

PROCESS PARAMETERS	N\PLY	N_WELL	UNITS
Sheet Resistance	1422	1393	ohms/sq
Width Variation (measured - drawn)			microns
Contact Resistance			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PAR.	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	MTL4	N_WELL	UNITS
Area (substrate)	934	857	88	32	14	7	5	92	aF/um^2
Area (N+active)			4550	49	20	13	11		aF/um^2
Area (P+active)			4558						aF/um^2
Area (poly)				78	19	11	7		aF/um^2
Area (metal1)					42	15	9		aF/um^2
Area (metal2)						40	15		aF/um^2
Area (metal3)							42		aF/um^2
Fringe (substrate)	177	166		40	19	18	25		aF/um
Fringe (N+active)			473						aF/um
Fringe (P+active)			508						aF/um
Fringe (poly)				70	42	31	25		aF/um
Fringe (metal1)					61	36	29		aF/um
Fringe (metal2)						57	37		aF/um
Fringe (metal3)							55		aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.36	Volts
Vinv	1.5	1.50	Volts
Vol (100 uA)	2.0	0.22	Volts
Voh (100 uA)	2.0	3.00	Volts
Vinv	2.0	1.60	Volts
Gain	2.0	-20.82	
Ring Oscillator Freq.			
DIV4 (31-stage,3.3V)		206.35	MHz
Ring Oscillator Power			
DIV4 (31-stage,3.3V)		5.49	uW/MHz/g

SPICE LEVEL2/LEVEL3 parameters not available.

N7CU SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS

```
* DATE: May 20/98
* LOT: N7CU              WAF: 23
.MODEL CMOSN NMOS                                                  LEVEL    = 49
+VERSION    = 3.1          TNOM       = 27          TOX        = 7.6E-9
+XJ         = 1.5E-7       NCH        = 1.7E17      VTH0       = 0.5710859
+K1         = 0.878501     K2         = -0.0300243  K3         = 11.3113085
+K3B        = -0.3965833   W0         = 1E-5        NLX        = 1.457884E-7
+DVT0W      = 0            DVT1W      = 5.3E6       DVT2W      = -0.032
+DVT0       = 7.4122244    DVT1       = 0.8466786   DVT2       = -0.0431829
+U0         = 392.1337916  UA         = 2.772806E-10 UB        = 1.277294E-18
+UC         = 5.063058E-11 VSAT       = 1.232875E5  A0         = 0.900086
+AGS        = 0.2495782    B0         = 3.808501E-8 B1         = 1.022E-6
+KETA       = -0.0935      A1         = 0           A2         = 1
+RDSW       = 832.2247571  PRWG       = -1.1278E-3  PRWB       = -1.035E-3
+WR         = 1            WINT       = 1.074592E-7 LINT       = 4.844866E-8
+DWG        = -1.076457E-8 DWB        = 5.072102E-9 VOFF       = -0.15
+NFACTOR    = 2            CIT        = 0           CDSC       = 2.4E-4
+CDSCD      = 0            CDSCB      = 0           ETA0       = 0.023341
+ETAB       = 0            DSUB       = 0.3151379   PCLM       = 0.7954879
+PDIBLC1    = 2.0677E-3    PDIBLC2    = 1.499374E-3 PDIBLCB    = 0
+DROUT      = 0.0263371    PSCBE1     = 6.472592E9  PSCBE2      = 5.003116E-9
+PVAG       = 0.1858763    DELTA      = 0.01        MOBMOD     = 1
+PRT        = 0            UTE        = -1.5        KT1        = -0.11
+KT1L       = 0            KT2        = 0.022       UA1        = 4.31E-9
+UB1        = -7.61E-18    UC1        = -5.6E-11    AT         = 3.3E4
+WL         = 0            WLN        = 1           WW         = 0
+WWN        = 1            WWL        = 0           LL         = 0
+LLN        = 1            LW         = 0           LWN        = 1
+LWL        = 0            CAPMOD     = 2           CGDO       = 4.7E-10
+CGSO       = 4.7E-10      CGBO       = 0           CJ         = 9.3406E-4
+PB         = 0.83492      MJ         = 0.3779      CJSW       = 2.0983E-10
+PBSW       = 0.83492      MJSW       = 0.39887     PVTH0      = -7.594092E-3
+PRDSW      = -83.6700093  PK2        = -2.428668E-3 WKETA      = -0.0203354
+LKETA   = -0.015649
*
*
.MODEL CMOSP PMOS                                                  LEVEL   = 49
+VERSION    = 3.1          TNOM       = 27          TOX        = 7.6E-9
+XJ         = 1.5E-7       NCH        = 1.7E17      VTH0       = -0.6337919
+K1         = 0.9029167    K2         = -0.034687   K3         = 15.6544439
+K3B        = -0.414614    W0         = 1E-5        NLX        = 8.659181E-8
+DVT0W      = 0            DVT1W      = 5.3E6       DVT2W      = -0.032
+DVT0       = 2.2415808    DVT1       = 0.4774944   DVT2       = -0.1499976
+U0         = 126.7415765  UA         = 1.546932E-9 UB         = 3.574984E-19
+UC         = -9.25937E-11 VSAT       = 1.400982E5  A0         = 0.9155035
+AGS        = 0.2126518    B0         = 3.11251E-8  B1         = -5.650557E-7
+KETA       = -0.13927     A1         = 0           A2         = 1
+RDSW       = 1.833498E3   PRWG       = -4.479053E-3 PRWB      = -5E-3
+WR         = 1            WINT       = 1.06155E-7  LINT       = 6.896986E-8
+DWG        = -1.056462E-8 DWB        = 2.438224E-9 VOFF       = -0.15
```

+NFACTOR	= 2	CIT	= 0	CDSC	= 6.593084E-4
+CDSCD	= 0	CDSCB	= 0	ETA0	= 0.0492433
+ETAB	= 0	DSUB	= 0.5	PCLM	= 2.0919478
+PDIBLC1	= 2.247498E-3	PDIBLC2	= 1.238699E-3	PDIBLCB = 0	
+DROUT	= 0.0580951	PSCBE1	= 4.785273E9	PSCBE2	= 5.406486E-9
+PVAG	= 1.8146291	DELTA	= 0.01	MOBMOD	= 1
+PRT	= 0	UTE	= -1.5	KT1	= -0.11
+KT1L	= 0	KT2	= 0.022	UA1	= 4.31E-9
+UB1	= -7.61E-18	UC1	= -5.6E-11	AT	= 3.3E4
+WL	= 0	WLN	= 1	WW	= 0
+WWN	= 1	WWL	= 0	LL	= 0
+LLN	= 1	LW	= 0	LWN	= 1
+LWL	= 0	CAPMOD	= 2	CGDO	= 4.5E-10
+CGSO	= 4.5E-10	CGBO	= 0	CJ	= 8.6341E-4
+PB	= 0.99	MJ	= 0.56727	CJSW	= 1.8343E-10
+PBSW	= 0.99	MJSW	= 0.36665	PVTH0	= 1.840766E-3
+PRDSW	= -165.4749549	PK2	= -5.732675E-3	WKETA	= -1.57284E-3
+LKETA	= 5.75928E-3				

APPENDIX C

HSPICE V-to-F Source File

```
□

□
.include 'MOSIS.350.mod'
□

□
.subckt INV 1 2
□
*input 1, output
□
vdd 3 0 1.2
□

□
m1  2 1 3 3   cmosp l=.4u w=.6u ad=.9p as=.9p pd=3.6u ps=3.6u
m2  2 1 0 0   cmosn l=.4u w=.6u ad=.9p as=.9p pd=3.6u ps=3.6u
.ends INV


iin 0 1 pwl(10ns 10na 11ns 30na 400ns 30na
+           401n 60na 700ns 60na 701ns 120na 1000ns 120na
+         1001ns 240na 1300ns 240ns)
cstart 1 0 3f
x1 1 2 INV
x2 2 3 INV
x3 3 4 INV
x4 4 5 INV
m1 1 5 0 0  cmosn l=.4u w=.6u ad=.9p as=.9p pd=3.6u ps=3.6u


.options post
.tran .05ns 1300ns
.end
```

APPENDIX D

HSPICE Sigma-Delta Source File

```
*** Pixel-Level Sigma Delta ADC


.include 'MOSIS.350.mod'
.include 'subcircuits4.cir'


*****************************
*Subcircuit
* INV
* REGISTER
* NAND
* DAC
*REGISTER2
*SHIFTER1
*SHIFTER2

**Vdd 10, Clk 5, Integrator 1,
**Vss 11, Vdd2 12


Vdd 10 0 3.3
Vss 11 0 -.2
Vdd2 12 0 1
Vclk 5 0 pulse(3.3 0 4.6n .1n .1n 5n 10n)
Vshift  50 0 pulse(0 3.3 8n .1n .1n 95n 1000n)
Vnshift 51 0 pulse(3.3 0 8n .1n .1n 95n 1000n)
*Vshift  50 0 pulse(0 3.3 0n .1n .1n 100n 1000n)
*Vnshift 51 0 pulse(3.3 0 0n .1n .1n 100n 1000n)


*****Integrator/Current Generator****

Cint 1 0 100f
iin 1 0 pwl(10ns -10na 11ns 120na 2000ns 120na)


*****Comparator*********************

x1 1 2 12 11 INV
x2 2 3 12 11 INV
x3 3 4 12 11 INV
x4 4 6 12 11 INV

******MAIN**********************

x6 6 5 7 10 0 12 REGISTER
x7 5 8 10 0 INV
x8 8 7 9 10 0 NAND
x9 9 1 DAC
```

```
*******Counter***************
x30 9 52 10 0 INV
x10 50 51 52 5 20 10 0 SHIFTER2
x11 21 20 22 10 0 REGISTER2

x12 50 51 22 21 24 10 0 SHIFTER1
x13 50 51 22 5 23 10 0 SHIFTER2
x14 24 23 25 10 0 REGISTER2

x15 50 51 25 24 27 10 0 SHIFTER1
x16 50 51 25 5 26 10 0 SHIFTER2
x17 27 26 28 10 0 REGISTER2

x18 50 51 28 27 30 10 0 SHIFTER1
x19 50 51 28 5 29 10 0 SHIFTER2
x20 30 29 31 10 0 REGISTER2

x21 50 51 31 30 33 10 0 SHIFTER1
x22 50 51 31 5 32 10 0 SHIFTER2
x23 33 32 34 10 0 REGISTER2

x24 50 51 34 33 36 10 0 SHIFTER1
x25 50 51 34 5 35 10 0 SHIFTER2
x26 36 35 37 10 0 REGISTER2

m1  21 50 0 0 cmosn l=.4u w=.6u ad=.9p as=.9p pd=3.6u ps=3.6u

Cs 26 0 10f
Cs2 27 0 10f
.options post
.tran .1ns 1500ns
.tran 1ns 100n UIC
.end
```

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