Monolithic Integration of III-V Semiconductor Materials and Devices with Silicon

By

Steve M. Ting

B. S. Materials Science and Engineering
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Submitted to the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electronic Materials

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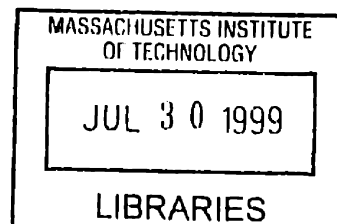
Signature of Author: ....
Department of Materials Science and Engineering
April 30, 1999

Certified by: ....
Eugene A. Fitzgerald
Professor of Electronic Materials

Accepted by: ....
Linn W. Hobbs
John F. Elliott Professor of Materials
Chairman, Departmental Committee on Graduate Students



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ABSTRACT

The realization of monolithic optical interconnects by integration of III-V materials with conventional Si circuitry has long been hindered by materials incompatibilities (i.e. lattice mismatch and heterovalent interface) and practical processing constraints.

We have examined the possibility of overcoming the 4.1% lattice mismatch between GaAs and Si by using relaxed, compositionally-graded $Ge/Ge_xSi_{1-x}/Si$ with low threading dislocation densities (~2 x $10^6/cm^2$) to bridge the gap in lattice constants. In doing so, we first addressed the issue of antiphase disorder and its suppression during GaAs growth on offcut (001) Ge and $Ge/Ge_xSi_{1-x}/Si$ substrates by solid-source molecular beam epitaxy and metal-organic chemical vapor deposition. In both growth techniques, the sublattice orientation of GaAs/Ge and $GaAs/Ge/Ge_xSi_{1-x}/Si$ is determined by the interaction of arsenic adsorbed on the Ge surface prior to actual GaAs nucleation; in particular, we suspect a temperature dependent rotation of arsenic dimers. By avoiding competition between the two possible dimerization mechanisms, single-domain, APB-free GaAs films have been grown. Comparisons of GaAs/Ge and $GaAs/Ge/Ge_xSi_{1-x}/Si$ films by defect-revealing etching and transmission electron microsopy indicate substrate-limited threading dislocation density. $GaAs/Ge/Ge_xSi_{1-x}/Si$ films with threading dislocation densities as low as 2-4 x 10^6 /cm^2 are currently possible, and further improvement is anticipated with continued optimization of $Ge/Ge_xSi_{1-x}/Si$ substrates. The I-V characteristics of identical p-n diode structures fabricated on $Ge/Ge_xSi_{1-x}/Si$ and GaAs substrates only appear sensitive to threading dislocation density in the zero-bias regime. Diodes on $Ge/Ge_xSi_{1-x}/Si$ feature R_0A as high as 10^7 Ω-cm^2, only a factor of 3 lower than those on GaAs.

To explore the processing incompatibilities of monolithic integration, we developed $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n diodes for growth on an MIT baseline CMOS host IC. Typical diodes featured a room temperature R_0A product of up to 20,000 Ω-cm^2 indicating acceptable performance as near infra-red photodetectors. No degradation of the PMOS and NMOS transistors directly attributable to the III-V integration cycle was observed.

Thesis Advisor: Eugene A. Fitzgerald
Title: Professor of Electronic Materials

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Chapter I

Overview of III-V on Si Materials Integration Issues

Motivation for III-V Materials Integration on Si

Silicon remains unrivaled as the dominant materials system for the manufacture of VLSI (very large scale integration) memory and logic integrated circuits (ICs). The major advantages of silicon over all other candidate materials include: aggressive feature-scaling afforded by highly developed process and design technologies; the availability of inexpensive, large-area substrates; and a stable native oxide suitable for dielectric passivation. Nevertheless, Si faces fundamental limits in terms of its carrier mobility and its lack of a direct bandgap, and for this reason the III-V compound semiconductors remain the materials of choice for high-speed and optoelectronic devices. Successful integration of III-V materials with silicon-based devices will extend the capabilities of current silicon-based IC technology.

Before discussing III-V integration any further, however, the distinction between hybrid integration and monolithic integration is an important one that should be mentioned here.[1,2] Hybrid integration typically involves the alignment and mounting of pre-fabricated III-V components to a host silicon IC (*e.g.* flip-chip bonding,[3] polyimide bonding,[4] wafer bonding[5]), whereas monolithic integration primarily refers to the heteroepitaxial growth of III-V device structures on silicon. Heteroepitaxial growth is an inherently self-aligned process similar to other high-volume, wafer-scale operations involved in conventional IC fabrication. Thus monolithic integration enjoys a tremendous economy of scale advantage over the volume-limited, labor-intensive hybrid approach which features processes more akin to electronics packaging.

Perhaps one of the most ambitious roles envisioned for monolithic III-V on Si integration is the fabrication of optoelectronic integrated circuits (OEICs).[6,7] Current silicon VLSI designs are fundamentally limited by the scaling rules of their densely packed electrical interconnects. Reducing the cross-sectional area of metal interconnects increases their resistance, thus increasing both the corresponding RC time delay and overall power consumption of the circuit. Additionally, as metal lines become more closely packed, crosstalk, or interference between neighboring lines due to capacitive and inductive coupling, becomes more pronounced especially at high bandwidths. Practical limits to silicon VLSI architecture are also imposed by the need to provide electrical I/O (input/output) pinouts along the chip edge.

Since perimeter increases merely as the square root of chip area, the trend towards larger-area chips with higher device and interconnect densities exacerbates the need for an alternative I/O technology.

Due to the inherent non-interaction of photons, optical interconnects can alleviate the chip-to-board, chip-to-chip, and even on-chip bottlenecks of conventional electrical interconnects by circumventing the scaling and density issues presented by capacitive loading, resistance, and crosstalk. Because optoelectronic signal transmission speed is limited not by RC delay or crosstalk, but rather by the speed of light itself and the signal conversion time from electrical-to-optical and back; significantly higher bandwidths can be realized for large interconnect distances. In addition, optical signal transmission may effectively isolate electrical noise, preventing its propagation in complex IC architectures. Freed from the need to design around the limitations of dense multi-layer metallization schemes, novel VLSI architectures could be expected to evolve around optical interconnect technology. Similarly, the ability to distribute optical I/O layout over the area of an OEIC removes the IC packaging constraint imposed by conventional perimeter I/O pinout. Figure I-1 illustrates the concept of a free-space optoelectronic interconnection consisting of paired LEDs and photodetectors.

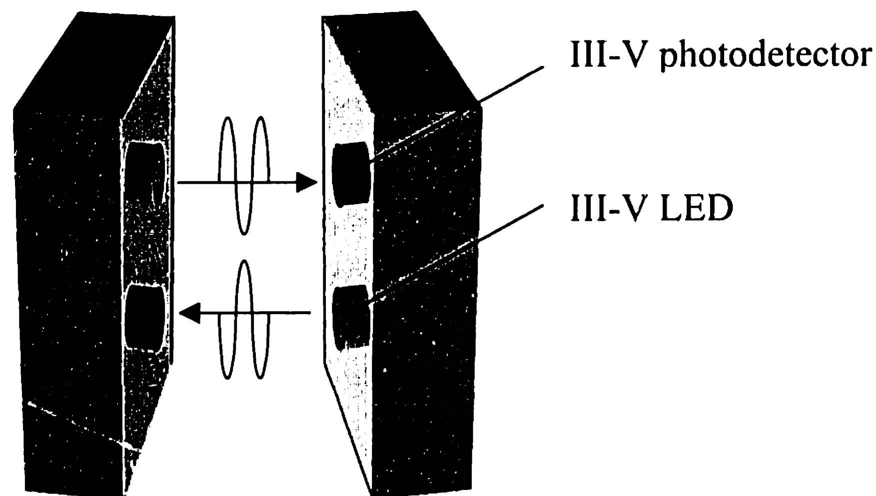


Figure I-1 *Example of a free-space optoeletronic interconnect between two OEICs.*

The current work focuses on the development of device quality III-V on Si heteroepitaxy towards the fabrication of a monolithically integrated OEIC. Specifically, the integration path explored employs the growth of relaxed, compositionally graded Ge_xSi_{1-x} to provide a larger-than-Si lattice constant on Si. To prove the viability of such substrates for III-V

heteroepitaxy, studies of GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si film growth, defect structure, and device fabrication were conducted. As a demonstration of materials and process compatibility, experimental results of monolithically integrated III-V devices grown and fabricated directly on Si CMOS wafers are also presented.

Note that much of the research lends itself not only to OEIC development, but also to any of a number of applications for which III-V on Si film growth is of interest. For example, the integration of III-V metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), or heterojunction bipolar transistors (HBTs) could add higher performance microwave or radio-frequency wireless communication capability to conventional Si CMOS circuitry. Also, with adequate defect control, it might be feasible to manufacture high efficiency III-V solar cells on Si substrates for space-based power systemes. Si substrates are not only larger and cheaper, but also lighter and stronger than the Ge substrates currently in use.

Barriers to III-V Materials Integration on Si

Given its compatibility with wafer scale processing, monolithic III-V integration on Si should offer greater reliability, superior performance, and lower cost than the hybrid option provided certain materials and processing issues can be resolved. The materials issues primarily consist of defect generation during III-V on Si growth due to lattice mismatch, polar on non-polar epitaxy, and thermal mismatch (See Table I-1); whereas the processing issues are imposed by the need to minimize any deleterious effects of III-V growth and device fabrication on the Si host IC.

Table I-1 *Materials Constants of Si, Ge, and GaAs*

	Crystal Structure	Lattice Constant (Å)	Coefficient of Thermal Expansion (K^{-1}) @ 300K
Si	diamond	5.430	2.33×10^{-6}
Ge	diamond	5.657	5.75×10^{-6}
GaAs	zinc-blende	5.653	5.8×10^{-6}

Lattice Mismatch

Lattice mismatch, the difference in equilibrium lattice constant between two materials, is perhaps the most pervasive problem in heteroepitaxy because of the limited selection of substrates.[8] The lattice constant vs. bandgap diagram featured in Figure I-2 (next page) illustrates the difficulties associated with integrating dissimilar semiconductor materials. Relatively few materials combinations are actually lattice-matched, such that optoelectronic performance at many wavelengths require defect engineering. In particular, note that there are no direct bandgap materials lattice matched to Si and there exists a significant 4.1% lattice mismatch between GaAs and Si.

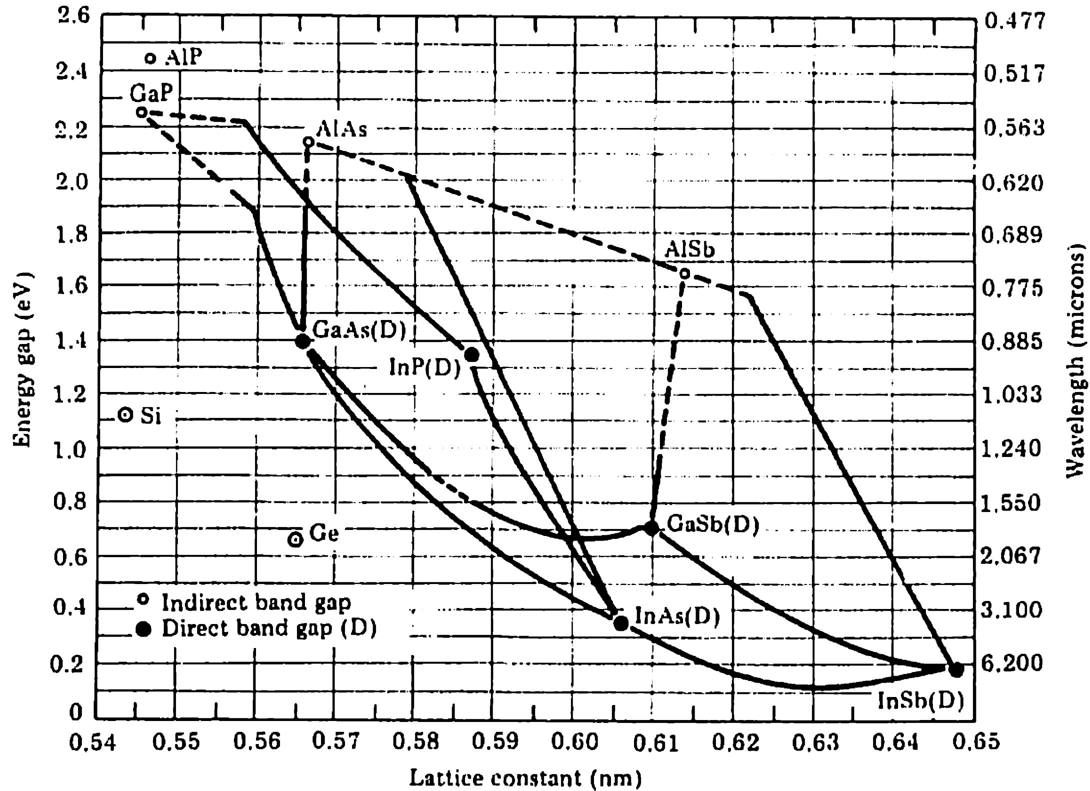


Figure I-2 *Lattice mismatch versus energy bandgap diagram*

Misfit Accommodation

During heteroepitaxial growth, lattice mismatch between the overlayer (film) and substrate gives rise to misfit strain:

$$f = \frac{a_s - a_o}{a_o} \tag{1.1}$$

where a_o and a_s are the equilibrium lattice constants of the overlayer and substrate, respectively. Initially, the misfit strain of the overlayer is accommodated by elastic strain ε, and the film is coherently strained to the substrate lattice constant, resulting in tetragonal distortion of overlayer unit cells as shown in Figure I-3. With increasing film thickness h the strain energy per area of the growing film accumulates:

$$E_\varepsilon = \varepsilon^2 Yh \tag{1.2}$$

Beyond a certain critical thickness h_c, however, the system finds it energetically favorable to relax the epilayer by nucleating dislocations that glide and form an array of misfit dislocations at the mismatched interface as shown in Figure I-3.

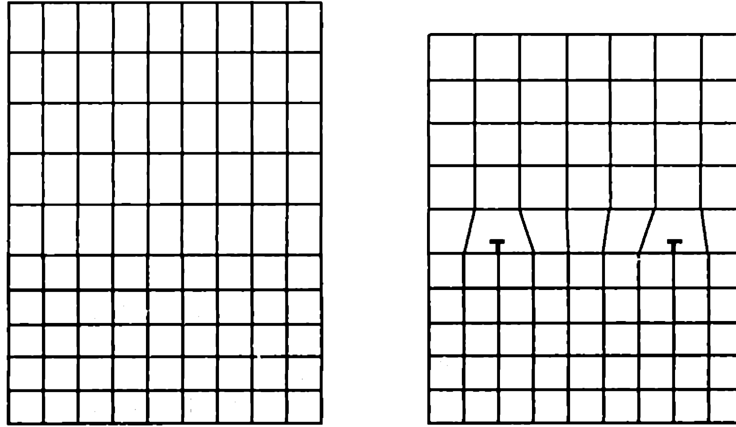


Figure I-3 *Strain-relaxation across a mismatched interface. Film growth is at first pseudomorphic, featuring elastic strain accommodation and tetragonal distortion (left), until past a critical thickness, when plastic deformation by misfit dislocations occurs (right).*

For growth on (001) surfaces this misfit array typically lies in the orthogonal [110] and $[1\bar{1}0]$ directions, due to the {111}<110> slip system common to the diamond and zinc-blende crystal structures common to most elemental and compound semiconductors. It can be shown that the energy per unit area of an orthogonal misfit dislocation array is:

$$E_d = D(b/b_{eff})\left(1-\nu\cos^2\alpha\right)\left(f-\varepsilon\right)\left[\ln\left(\frac{h}{b}\right)+1\right] \qquad (1.3)$$

where ν is Poisson's ratio, Y the bi-axial Young's modulus of the film, α the angle between Burgers vector b and dislocation line direction, and D the average shear modulus:

$$D = \frac{G_o G_s b}{\pi(G_o + G_s)(1-\nu)} \qquad (1.4)$$

where G_o and G_s are the shear moduli of overlayer and substrate, respectively. Minimizing the sum of E_s and E_d (equations) with respect to ε, Matthews derived the following expression for critical thickness:

$$h_c = \frac{D(1-\nu\cos^2\alpha)(b/b_{eff})\left[\ln\left(\frac{h_c}{b}\right)+1\right]}{2Yf} \qquad (1.5)$$

This equilibrium expression does not, however, take into account the kinetic limitations of dislocation nucleation and glide, which are both strain-dependent, thermally activated processes. Their suppression may lead to metastability (i. e., incomplete strain relaxation) even for film thicknesses $h > h_c$.

Threading Dislocations

Since a dislocation cannot terminate within a crystal, the formation of misfit dislocations during the onset of strain relaxation is often accompanied by the creation of threading dislocation segments that extend through the epilayer. Consider the case of a dislocation half-loop nucleating homogeneously at the surface of a mismatched film as shown in Figure I-4. As the half-loop expands and glides to the mismatched interface, a strain-relieving misfit segment bound by two threading segments is formed. Threading dislocations may also nucleate heterogeneously at other defects in the film or be inherited from the substrate.

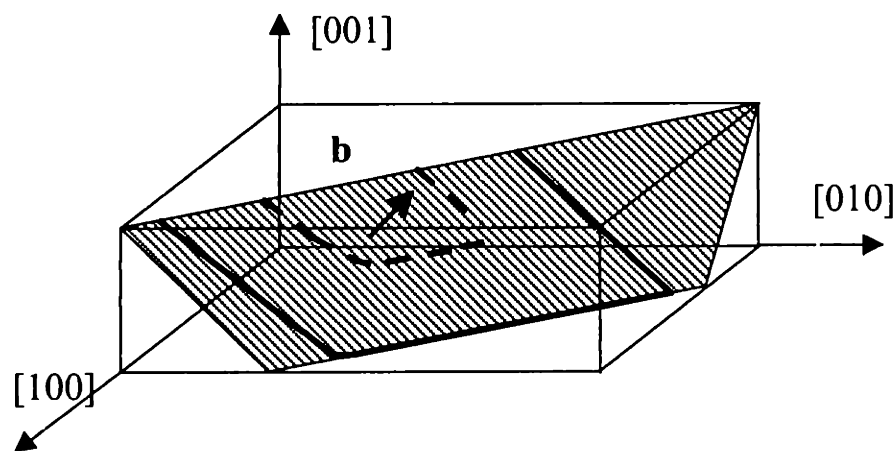


Figure I-4 *Homogeneous nucleation of a dislocation half-loop and glide to the (001) interface on the {111}<110> slip system.*

Glide of the threading segments extends the length of the misfit dislocation lying at the mismatched interface. Although associated with misfit dislocation nucleation, the threading dislocations themselves do not relieve strain and their presence in the film is in fact unfavorable due to the extra line energy they incur. Except for those able to glide to a free surface on the sample edge, residual threading dislocations will remain in the grown film as a by-product of strain-relaxation.

Gliding threading dislocations often react with, repulse, or otherwise obstruct one another as they come into close proximity with one another. Similarly, it has also been shown that threading dislocations may become impeded by the stress field of misfit dislocations lying in their path.[9] Dense pile-ups of immobilized dislocations inhibit strain relief, in turn promoting additional nucleation of threading dislocations. However, excessive nucleation or dislocation multiplication merely exacerbates the problem since the likelihood of dislocation interaction increases with threading dislocation density (TDD). Such dislocation multiplication is especially pronounced in the case of highly mismatched interfaces, due to the large driving force for dislocation nucleation.

Reducing the density of threading dislocations generated by lattice-mismatched heteroepitaxy is imperative since they are likely to propagate into active device regions. Dislocation cores are known to form mid-bandgap trap states that compromise the performance of minority carrier devices by decreasing the minority carrier lifetime. This and the ability of dislocations to getter metal impurity atoms can lead to excessive leakage current. These effects translate directly to the degradation of not only the radiative efficiency for light-emitting diodes (LEDs) and lasers but also the sensitivity of photodetectors and the energy conversion efficiency of solar cells.[10,11] In majority carrier devices such as FETs, high TDDs may also cause significant carrier scattering, thereby reducing mobility and transconductance.[12] Reliability is also an issue for LEDs and lasers, since the high injection current typical of device operation can nucleate dense dislocation networks at individual threads even in lattice-matched heterostructures. These so-called dark-line defects (DLDs) apparently propagate via point defect induced dislocation climb during device operation, resulting in rapid luminescence degradation.[13,14]

Estimated TDD limits for various III-V device applications are shown in Table I-2.[15]

Table I-2 ***Estimated TDD Limit vs. III-V Device***

Device	TDD (/cm^2)
FET	$<10^7$
Solar Cell	$<10^6$
LED	$<10^6$
Laser	$<10^5$

Lattice-Mismatch Engineering

Given the deleterious effects of high threading dislocation density (TDD) the vast majority of heterostructure devices employ closely lattice-matched materials. To expand the range of useful heteroepitaxial materials systems, one must turn to lattice-mismatch engineering, which consists of various techniques designed to minimize TDD in lattice-mismatched heterostructures.

A number of TDD reduction strategies, including thermal cycling and strained-layer growth, rely on added strain to actively promote threading dislocation glide and interaction after a high TDD has already been nucleated. For example, two glissile threading segments with the proper Burgers vectors may actually attract one another, combining to form a single sessile thread. Another possibility is the complete annihilation of two threading dislocations of opposite Burgers vectors. Note that the same effects are achieved passively by simply growing thicker films, which extends threading dislocation line lengths thereby increasing the probability of interaction. Despite their popularity for highly mismatched materials such as GaAs on Si, these techniques are limited by the very decrease in TDD they engender, however, since below a certain TDD (approximately 10^7 /cm^2) further interaction becomes unlikely.[16]

In low mismatch systems (< 2%) minimal dislocation nucleation is encountered upon film relaxation due to the low levels of strain involved. Incremental introduction and relaxation of strain by compositional grading of semiconductor alloys can extend this approach to higher

lattice mismatches while maintaining a low TDD. Rather than reducing excessive residual TDD after their nucleation, TDD is minimized throughout the grading process, and suppression, rather than promotion, of dislocation interaction maximizes the strain-relieving glide provided by each threading dislocation. Although compositional grading is restricted to mutually miscible substrate/epilayer solid solutions, graded buffers may themselves be designed as substrates available in a range of otherwise inaccessible lattice constants for further heteroepitaxy. For example, this work makes use of Ge/Ge_xSi_{1-x}/Si to lattice-match to GaAs, however, it might also be possible to fabricate yellow (577-597 nm) LEDs and lasers on Si by lattice-matching InGaP to $Ge_{0.70}Si_{0.30}$/Ge_xSi_{1-x}/Si substrates. Compositional grading has already been effectively applied to the $In_xGa_{1-x}As$/GaAs,[17,18] Ge_xSi_{1-x}/Si,[19,20] $GaAs_{1-x}P_x$/GaAs,[21] and $In_xGa_{1-x}P$/GaP[22] materials systems.

A final means of controlling threading dislocation density relies on substrate patterning; encompassing techniques such as selective-area epitaxy, epitaxial lateral overgrowth (ELO),[23]epitaxial necking,[24] and conformal epitaxy.[25] Selective area epitaxy serves to isolate heterogeneous dislocation nucleation sources and provide free edges for threads to glide to, whereas the other techniques attempt to altogether block the propagation of threading dislocations nucleated at the mismatched interface. Significant improvements in materials quality for ELO GaN on sapphire and conformal epitaxial GaAs on Si[25,26] and InP on Si[27] have been reported.

Polar on Non-Polar Epitaxy

In addition to lattice-mismatch, growth of a III-V compound semiconductor film on a group IV elemental semiconductor substrate poses a number of unique problems concerning the heterovalent interface.[28,29] If the III-V/IV interface consists of an unbroken plane of either exclusively III-IV or V-IV bonds then electrical neutrality is lost and the interface becomes polarized. In practice, interface polarity is likely compensated during growth by the presence of charged point defects and dislocation cores, as well as some degree of atomic exchange across the interface. Interdiffusion by itself presents the additional complication of unwanted autodoping across the interface. Group III and group V species dope p-type and n-type in the

group IV lattice, whereas group IV species are amphoteric in the zinc-blende crystal structure, though their preference for the group III sites tends to result in n-type doping (See Table 1-3).

Table 1-3 *Donor and Acceptor Levels Relevant to GaAs/Si and GaAs/Ge Autoping*[30]

Dopants in GaAs	Donor Level, E_c-E_d (eV)	Acceptor Level, E_a-E_v (eV)
Si	0.0058	0.035
Ge	0.006	0.04

Dopants in Si	Donor Level, E_c-E_d (eV)	Acceptor Level, E_a-E_v (eV)
Ga	-	0.072
As	0.054	-

Dopants in Ge	Donor Level, E_c-E_d (eV)	Acceptor Level, E_a-E_v (eV)
Ga	-	0.013
As	0.011	-

Hence, formation of a p-n junction at the III-V/IV interface due to autodoping looms as a distinct possibility. Interestingly, InGaP/GaAs/Ge solar cell manufacturers have turned this phenomenon to their advantage, creating a useful tandem junction by in-situ As diffusion into a p-type Ge substrate.[31]

Antiphase Disorder

Polarization and autodoping are near-interface effects that are likely second-order compared to the presence of a misfit dislocation array. As such, they are not a major concern for III-V on Si optoelectronic device fabrication so long as the active region remains several minority carrier diffusion lengths removed from the heterovalent interface. Moreover, devices can be designed such that the current path altogether bypasses the interface. Of far greater concern is the possibility of antiphase disorder, which if unchecked, can result in the propagation of planar defects, known as antiphase boundaries (APBs), through the entire thickness of a III-V epilayer.[32]

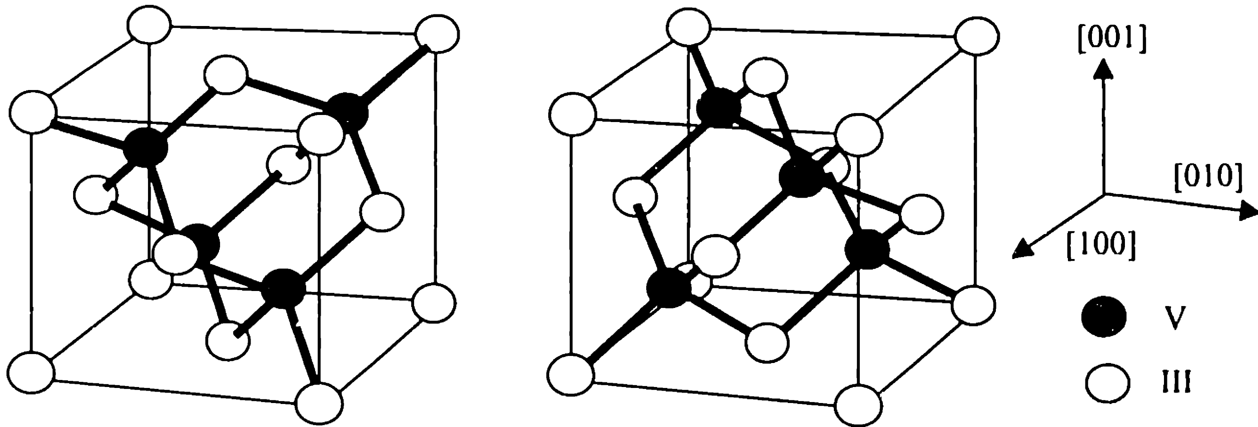


Figure I-5 *Two possible orientation of the zinc-blende cubic structure common to many of the III-V compound semiconductors, including GaAs. Each distinct orientation corresponds to a 90 ° rotation of the lattice.*

As illustrated in Figure I-5, two distinct crystallographic orientations of GaAs, are possible due to the chemical inequivalence of the two face-centered cubic (fcc) sublattices that comprise the zinc-blende crystal structure. Each orientation corresponds to a 90° rotation of the GaAs crystal that exchanges the position of anion and cation sublattices. The diamond cubic structure of Si and Ge is similarly two-fold symmetric about the [001] axis, however, the two fcc sublattices are chemically equivalent.

Nominally on-axis (001) Si and Ge surfaces always feature irregularly spaced single-atomic layer steps, a/4[001] high along the <110> directions. On alternating terraces separated by single-steps, or any odd-integer number of steps for that matter, the exposed sublattice shifts from one domain to the other. During heteroepitaxial growth of a GaAs film, this sublattice shift may nucleate an APB, which as shown in Figure I-6 (next page), consists of a plane of wrong nearest-neighbor bonds extending into the film, separating antiphase domains (APDs) of each sublattice orientation.

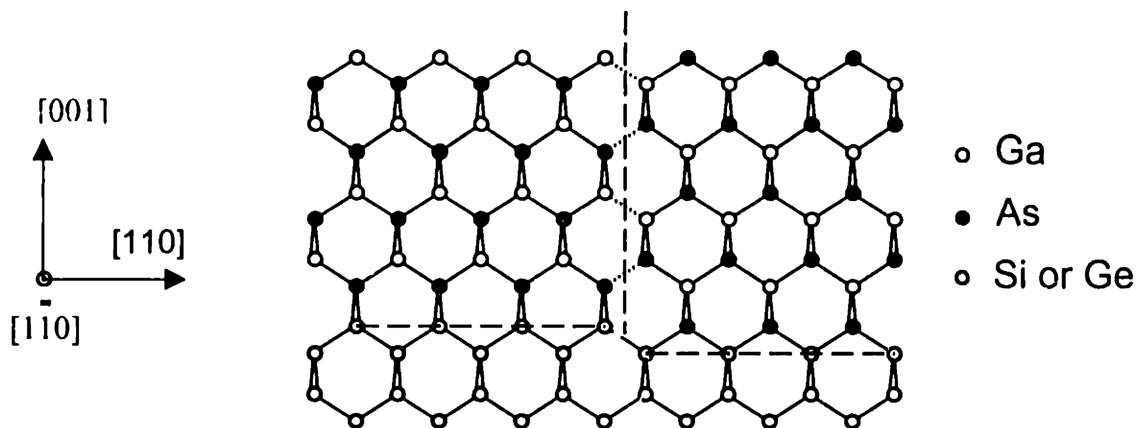


Figure I-6 *A GaAs antiphase boundary nucleated by the sublattic displacement of a single-step lying on the (001) Si or Ge substrate. The dashed line marks the wrong-nearest neighbor bonds lying along the plane of the APB.*

Antiphase boundaries of many crystallographic orientations have been experimentally observed and may be classified as stoichiometric (e.g. {110}, {112}); non-stoichiometric ({100}, {111}); or mixed depending on the ratio of As-As bonds to Ga-Ga bonds per unit area of boundary.[33] Stoichiometric APBs feature an equal number of As-As and Ga-Ga bonds, non-stoichiometric APBs consist of one type of bond exclusively, and mixed APBs contain unequal numbers of both bonds. APBs of all types are energetically unfavorable due to the formation energy of wrong nearest-neighbor bonds and the long-range electrostatic interaction energy of their excess charge.[32] Non-stoichiometry contributes an additional energy term and further exacerbates the polarization of the APB, which, in effect, becomes a δ-doped sheet. [34]

As is the case for dislocation cores, the electronic structure of APBs differs significantly from that of undistorted GaAs, hence they are likely to result in minority carrier lifetime degradation and majority carrier scattering.[32] Experimentally, cathodoluminescence (CL) imaging has demonstrated that APBs in GaAs/Ge act as non-radiative recombination centers[35] and electron beam induced current (EBIC) studies have further revealed a minority carrier surface recombination parameter $s = 20\ \mu m^{-1}$ at APBs:

$$s = \frac{v_s}{D} \qquad (1.6)$$

where v_s is the surface recombination velocity, and D is the GaAs minority carrier diffusion coefficient.[36,37] Hall mobility measurements on GaAs/Si have also shown degradation with increasing APB density.[38,39] Since APBs may extend well into a GaAs epilayer, any attempts

at monolithic integration of III-V devices on Si must address a means to suppress antiphase disorder.

Suppression of Antiphase Disorder

Clearly the suppression of antiphase disorder, demands control of the substrate surface structure prior to III-V growth. The usage of (001) substrates offcut to [110] has long been the strategy of choice to this end. In contrast to the irregular single-steps of nominally on-axis (001) Si and Ge surfaces, deliberately mis-orienting the substrate towards [110] introduces a regular array of single-steps running along the $[1\bar{1}0]$ direction. As the offcut angle ϕ is increased, the density of steps increases and the average terrace width *w* decreases according to the following relation:

$$w = h \tan^{-1} \phi \tag{1.7}$$

where *h* is the height of the step. At high temperatures and under ultra-high vacuum conditions, offcut (001) surfaces are known to transform from their initial single-stepped, two-domain configuration to a lower energy single-domain configuration of double-steps a/2[001] high.[40,41,42,43] Double-steps preserve sublattice orientation between neighboring terraces, thereby facilitating APB-free GaAs growth as shown below in Figure I-7.

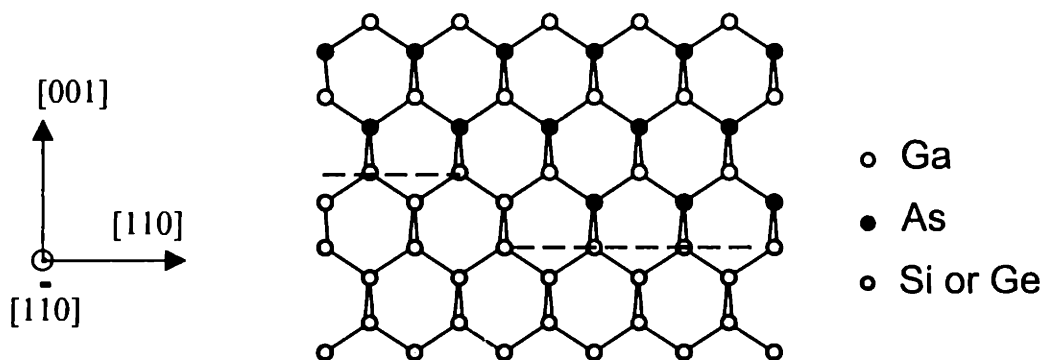


Figure I-7 *Suppression of antiphase disorder by a single-domain (001) Si or Ge surface featuring double atomic-layer steps.*

In the event that a single-domain, double-stepped surface is not achieved, substrate offcut may also serve to limit the extent of antiphase disorder by promoting APD self-annihilation as illustrated in Figure I-8. The high single-step density afforded by substrate misorientation decreases

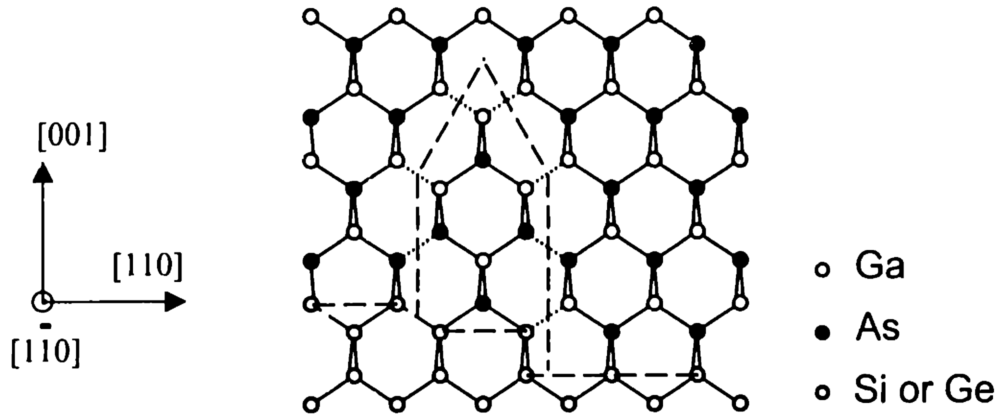


Figure I-8 *Self-annihilation of an APD made possible by the close proximity of bounding APB faces.*

the spacing between neighboring APBs, hence increasing the probability that neighboring APBs will find one another and form small closed domains. Many reports of single-domain GaAs/Si and GaAs/Ge in the literature actually refer to initial two-domain GaAs growth, followed by rapid annihilation of APBs near the interface, leaving a single dominant domain.[38,44,45,46,47] In the limit of vicinal (001) substrates, however, the spacing between adjacent APDs is thought to be quite large such that self-annihilation near the interface and single domain growth becomes less likely.

Thermal Mismatch

The significant thermal mismatch between the III-V compound semiconductors and Si may further complicate matters as illustrated by the case of GaAs on Si (Table I-1). Whereas relaxation of lattice mismatch strain occurs during growth at elevated temperatures, upon cooling, the lattice parameter of the GaAs film is constrained by the GaAs/Si interface and forced to follow the thermal contraction of the thicker Si substrate. This results in the accumulation of biaxial tensile strain in the GaAs epilayer:

$$\varepsilon = \Delta\alpha\Delta T \qquad (1.7)$$

where $\Delta\alpha$ is the difference in thermal expansion coefficients, and ΔT is the difference between growth and room temperatures. Inserting the constants from Table I-1, cooling a GaAs/Si film from a typical growth temperature of 600 °C incurs a biaxial tensile strain of approximately 0.2%.

Such a low level of strain, which is much less than the GaAs/Si lattice mismatch strain, is unlikely to result in significant nucleation of new dislocations despite some reports to the contrary.[48,49] Rather, the threading dislocations already present in the film are likely to respond by gliding to provide strain relief. Indeed, using thermal strain to promote threading dislocation interaction is the very premise behind TDD reduction by thermal cycling annealing.

At practical cooling rates, though, it is essentially impossible to achieve a relaxed GaAs/Si film at room temperature due to quenching of thermally-activated dislocation glide. Hence, the GaAs film becomes tetragonally distorted at room temperature and a certain amount of strain energy remains stored in the GaAs film as per Equation 1.2. In analogy to dislocation strain relief, past a certain critical thickness, an orthogonal array of cracks may nucleate in the epilayer to relieve the tensile strain, where the density of cracks is determined by a balance between accumulated strain energy and crack nucleation energy.

For growth of III-V devices in patterned selected areas, the likely scenario for optical interconnects on a host IC, residual thermal strain should not pose a problem until the lateral device dimensions approach the scale of crack density. However, cracking is of concern in applications that demand III-V on Si deposition over a large area, solar cells for instance, and beyond cooling slowly and maintaining a thin epilayer not much can be done to engineer around thermal strain. Second-order effects of thermal mismatch, which need to be considered on a III-V material and applications specific basis, include possible strain-induced shifts in bandgap and bandgap alignment, and splitting of band degeneracies.

Process Integration

Finally, it remains to be shown that III-V materials growth and device processing can be reliably incorporated into a conventional Si IC process. Note that the concept of monolithic integration has not yet reached a high level of process maturity even for optoelectronics on GaAs ICs.[50] At a minimum, a monolithic III-V integration scheme should not infringe upon thermal budget constraints nor introduce Si device contaminating species. Ideally, a III-V integration sequence can be dropped directly into a conventional Si process that remains otherwise unmodified before or after insertion, thereby incurring minimal additional processing.

The relative thermal stability of III-V and Si processes by and large determines when such an insertion is feasible. The volatility of group V species in III-V semiconductors at elevated temperatures (> 400 °C bare, or > 800 °C with dielectric encapsulation) precludes integration before high temperature front-end Si processes such as thermal oxidation or post-implantation annealing (> 1000 °C). Conversely, if integration occurs after much of the Si process has been completed, the temperatures necessary for III-V heteroepitaxial growth (typically > 600 °C to achieve reasonable growth rates and complete strain relaxation) may be an issue. At the very least, this necessitates completion of III-V growth prior to metal contact deposition. Perhaps the greatest concern, though, is the possibility of compromising sub-micron critical dimensions through unintentional dopant redistribution. One concern for metal-oxide-semiconductor (MOS) processes is dopant penetration from the polysilicon gate electrode through the thin (typically < 100 Å) gate oxide and into the channel region, leading to threshold voltage shifts. Another might be shortening of the effective gate length by lateral diffusion of source and drain wells, a situation that could lower threshold voltages and enhance short-channel effects. Similar concerns exist for bipolar junction transistor (BJT) technologies, where the critical dimension, in this case base width, is defined by a sharp vertical doping profile.

III-V growth and processing may further pose a contamination problem due to the necessary introduction of various chemical species and treatments that a Si process might otherwise not be exposed to. As previously noted, the group III and group V elements themselves dope p-

type and n-type in Si, respectively. Since typical III-V deposition conditions are not highly selective, areas of the un-finished host IC are may be susceptible to uncontrolled doping during III-V growth. Furthermore, III-V contact metallurgies differ considerably from those of Si. Ohmic contacts to GaAs often feature Au as a major constituent. Since Au is both a fast diffuser and deep-level trap in Si, alternative contact metallurgies need to be considered for monolithic integration. In all likelihood, though, each of these contamination issues can be overcome at the expense of implementing and/or developing appropriate passivation technologies (consider for example the recent development of copper interconnects).

Conclusions

A tremendous volume of research has already been dedicated to the various barriers to III-V integration on Si. Nevertheless, it has yet to be shown that the quality of III-V on Si material can offer the reliability and performance demanded of optoelectronic interconnect and other device applications. Moreover, whether monolithic III-V integration is a practical and cost-effective means of adding new capabilities to existing Si VLSi technology remains to be seen.

Chapter II

III-V Materials Integration Approach

Status of Progress Towards Monolithic III-V on Si

Next to elemental Si, GaAs is perhaps the most studied semiconductor material and has found use in a host of wide-ranging commercial applications including not only high speed MESFET and HEMT integrated circuits but also to solar cells and lattice-matched AlGaAs/GaAs and InGaP/GaAs LEDs and laser diodes. Thus an immense expanse of published research, more than for any other compound semiconductor on Si, has been devoted entirely towards reconciling the materials differences between heteroepitaxial GaAs/Si for monolithic integration, with the bulk of these efforts concerning the foremost problem of TDD reduction.

Unfortunately, the literature is rife with suspect claims sporting outlandishly low GaAs/Si TDD quotes. Much of the problem lies with the techniques typically relied upon for TDD characterization among which etch pit density measurement is perhaps the most common. Unfortunately, the rough surface morphology of GaAs/Si films and the high TDD itself makes proper characterization by etch pit density a tricky endeavor at best. Without additional correlation from other techniques, etch pit density counts alone cannot be taken at face value for accurate TDD characterization. Similarly, cross-section transmission electron microscopy (XTEM) is also often misused for TDD characterization and suffers from the inability to survey TDD on a statistically relevant scale.

Thus, while GaAs/Si TDD as low as the high end of GaAs substrate TDD (10^3 to 10^4 /cm^2) have been reported, attempts at achieving GaAs/Si with TDD low enough to realize III-V on Si device integration have continued unabated.[51] It is now a generally accepted fact that the high GaAs/Si lattice mismatch (~4.1% misfit) leads to massive homogeneous nucleation of dislocations during the early stages of direct GaAs/Si heteroepitaxy. Since homogeneous nucleation implies a near infinite number of nucleation sites reacting simultaneously to the same driving force, direct GaAs/Si growth invariably leads to TDD > 10^8 /cm^2 near the interface in the absence of additional defect engineering. Modest TDD decreases are observed with increasing film thickness as threads react, coalesce, and annihilate with one another, and realistic TDD figures on the order of 10^7 /cm^2 reflect the best possible GaAs/Si through thermal cycling and strained-layers.[52] However, there exists little hope for further

TDD improvement via these self-limiting mechanisms, which rely on TDD reduction after the fact. Lacking the ability to overcome lattice mismatch and facing the additional barriers of antiphase disorder, thermal mismatch, and process integration, direct GaAs/Si heteroepitaxy faces dim prospects for monolithic integration of high performance III-V devices on Si.

Experimental Synopsis

The Fitzgerald group CVD facility possesses the ability to grow not only low defect density Ge_xSi_{1-x} alloys by UHVCVD but also a wide variety of III-V materials including GaAs by MOCVD. MIT's on-campus Microsystems Technologies Laboratory (MTL) features a dedicated Si CMOS fab, the Integrated Circuits Laboratory, as well as a facility geared towards the processing of III-V and otherwise novel devices, the Technologies Research Laboratory. Together these facilities provided a unique opportunity to comprehensively address both the materials and processing aspects monolithic III-V on Si integration.

Recent progress in compositional grading of Ge_xSi_{1-x} alloys grown by UHVCVD with low TDD suggest their potential application as buffer layers between GaAs and Si.[19,20] The idea of using buffer layers to improve GaAs/Si TDD is not new by itself. Since GaAs and Ge are nearly lattice matched (~0.07% misfit), a number of studies have attempted GaAs heteroepitaxy on Ge/Si[5354] or abruptly graded Ge_xSi_{1-x}/Si.[55] Still others have grown or wafer bonded low-modulus buffer layers to facilitate strain relief before GaAs growth.[49] Regardless, Ge/Si and all otherwise abruptly mismatched buffers on Si still lead to high GaAs/Si TDD since the problem of homogeneous dislocation nucleation has merely been displaced rather than removed by these intervening layers.

However, when Ge_xSi_{1-x} is compositionally graded over a series of low mismatch interfaces, the misfit strain between Si and Ge lattice constants is evenly distributed over the thickness of the buffer rather than a single buffer, and strain relaxation via homogeneous dislocation nucleation may be averted. Maintaining low strain minimizes the driving force for dislocation nucleation, which therefore occurs heterogeneously from a limited number of sites. This is an important distinction, because the low density threads prevents their interaction and

maximizes not only the strain-relieving glide they provide but also their re-use in subsequent layers of the graded buffer.

Suppression of homogeneous nucleation and maintenance of low TDD as a fully relaxed Ge_xSi_{1-x} buffer is graded all the way to 100% Ge produces a viable, nearly lattice-matched substrate for GaAs heteroepitaxy. Note that continued reduction $Ge/Ge_xSi_{1-x}/Si$ substrates TDD was realized concurrently during the course this study.[56] Our approach towards monolithic III-V on Si relies heavily on the development of UHVCVD Ge_xSi_{1-x} compositional grading and the replacement of the highly mismatched GaAs/Si interface with numerous low mismatch Ge_xSi_{1-x} interfaces. Hence, much of the work is concerned with demonstrating that device quality GaAs can be grown on low-defect density $Ge/Ge_xSi_{1-x}/Si$ substrates. By further extending the concept of compositional grading to $In_xGa_{1-x}As/GaAs$ on $Ge/Ge_xSi_{1-x}/Si$, it should be possible to achieve infrared LEDs, lasers, and photodetectors for optical interconnects.

Having bypassed the GaAs/Si lattice mismatch hurdle through $Ge/Ge_xSi_{1-x}/Si$ substrates, it is now appropriate to consider the obstacle posed by antiphase disorder in GaAs/Ge films. In the past GaAs/Ge growth was primarily studied as a model system for heterovalent epitaxy due to its negligible lattice mismatch. Much of this early work was done by solid-source MBE, a natural starting point because of its non-equilibrium growth conditions and exceedingly simple chemistry, involving the fewest species of any growth technique. Furthermore, the availability of *in-situ* characterization techniques such as reflection high-energy electron diffraction (RHEED)[57] and low-energy electron diffraction[42,43] (LEED) has permitted observation of surface structure under growth conditions.[40]

Unfortunately antiphase disorder remains poorly understood, because many MBE studies relied exclusively on such techniques, neglecting a detailed correlation with film morphology.[46,47,57] Moreover, the recent development of interest in high-efficiency III-V on Ge solar cells, has applied increasing pressure to better understand the occurrence and accomplish the complete suppression of yield-limiting antiphase disorder. Since antiphase disorder will also be a threat to achieving device quality $GaAs/Ge/Ge_xSi_{1-x}/Si$ heteroepitaxy,

its suppression is essential to qualifying our integration approach. Our study of antiphase disorder at the GaAs/Ge interface thus begins where others left off, coupling MBE growth with a comprehensive defect morphology study by TEM in order to close this gap in the literature.[58]

The knowledge we gained of the GaAs/Ge interface was then applied to GaAs/Ge/Ge_xSi_{1-x}/Si using atmospheric-pressure metal-organic chemical vapor deposition (AP-MOCVD) in hopes of identifying a common theme in the occurrence of antiphase disorder. Though lacking the same *in-situ* monitoring tools and possessing a relatively complex growth chemistry, MOCVD features capacity for high-volume throughput, which, coupled with its exceptional versatility and high-purity, has increasingly made it the III-V epitaxy technique of choice for commercial device fabrication, including III-V solar cells. Although Ge/Ge_xSi_{1-x}/Si was expected to respond similarly to Ge with regards to the possibility of antiphase disorder, the switch to Ge/Ge_xSi_{1-x}/Si substrates brought the study one step closer to actual III-V on Si integration. Once adequate control of antiphase disorder was demonstrated, the TDD improvement in GaAs/Ge/Ge_xSi_{1-x}/Si afforded by the graded Ge_xSi_{1-x} was evaluated and device performance measurements made.

While previous attempts at monolithic integration of III-V devices with Si circuitry have been severely limited in scope and scale due to the seemingly insurmountable materials problems,[59,60,61] with progress in device quality GaAs/Ge/Ge_xSi_{1-x}/Si, the design of a practical processing scheme for integrating III-V devices on a Si IC can and should also now be reconsidered. The fact that III-V and Si processing technologies and facilities have developed along separate paths has tended to inhibit studies that combine the two dissimilar materials systems. It is thus fortuitous that we could attempt just that at MIT given the ICL's ability to produce a CMOS host IC and the TRL's ability to complete the fabrication of an OEIC after III-V MOCVD growth. Although the lack of a composite substrate featuring patterned areas of Ge/Ge_xSi_{1-x}/Si, necessitated direct GaAs/Si heteroepitaxy, we were still able to address the primary issue of whether or not III-V on Si heteroepitaxy could be accomplished without compromising a host CMOS IC. To assess the possibility optical interconnection, near-

infrared $In_{0.15}Ga_{0.85}As$ on GaAs/Si LED/p-i-n diodes were developed and integrated on an MIT fabricated CMOS IC in collaboration with Discovery Semiconductors.

Compositionally Graded Ge_xSi_{1-x}

Compositionally-graded buffers are capable of bridging the gap in lattice constants between a lattice-mismatched cap layer and substrate.[19,20] As shown in the single-lens binary phase diagram of Figure II-1, Ge and Si are completely miscible through the entire range of Ge_xSi_{1-x} solid solutions, indicating that such alloys are ideally suited to compositional grading.

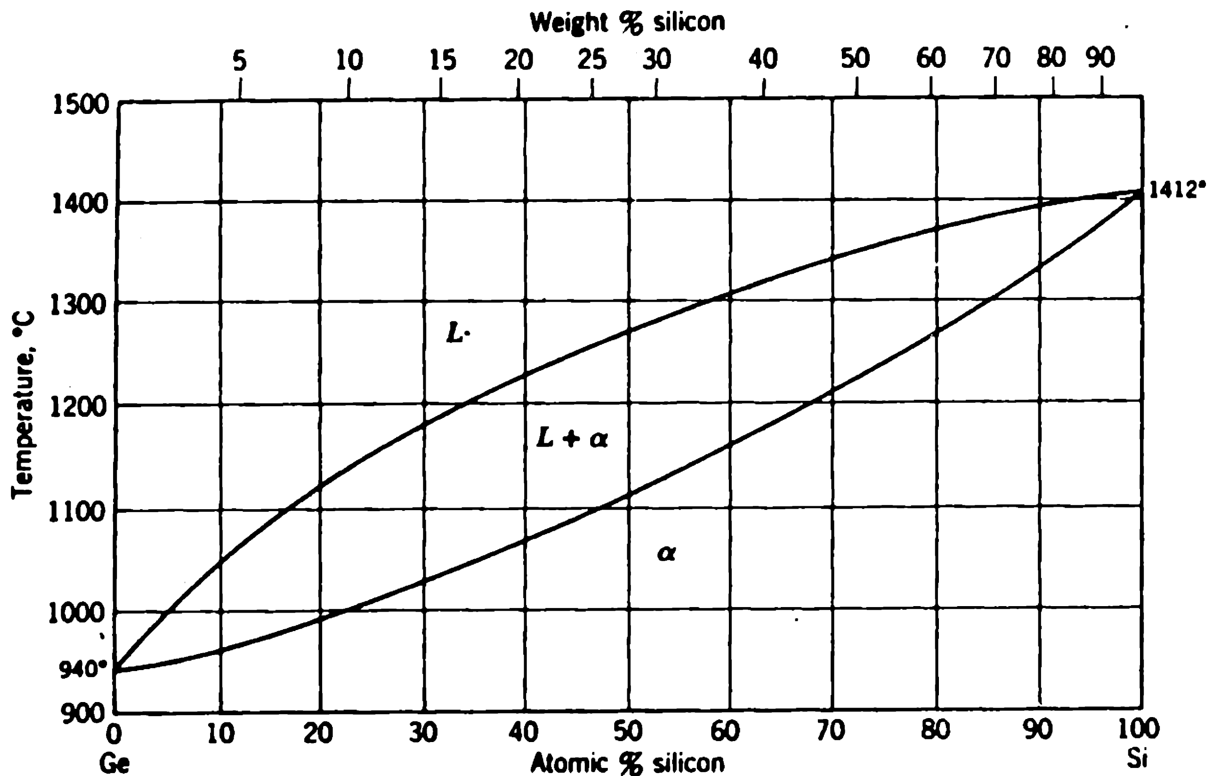


Figure II-1 *Phase diagram of Ge_xSi_{1-x} alloy*

Proper control of the grading rate and the growth temperature are essential to maintain a low TDD throughout the grading process. The fact that both the glide of pre-existing threads and the nucleation of new threads are thermally-activated phenomena complicates growth temperature optimization. In general, the homogeneous nucleation of dislocation half-loops (Figure I-4) from the film surface is to be avoided, and strain-relief from a limited number of heterogeneous dislocation sources is desirable. Ideally, the growth temperature can be

maintained high enough to promote glide while the grading rate introduces strain slowly enough to offset the risk of massive homogeneous dislocation nucleation, which features a higher activation barrier than heterogeneous nucleation or glide. Note, however, that each new increment of compositional grading also results in a concomitant change of the materials properties; for example the Young's modulus. Thus, it is often necessary to adjust grading parameters during growth to account for the shifts in dislocation glide and nucleation kinetics.

Although the compositional grading approach inherently minimizes dislocation interaction by distributing strain-relief in 3-D over numerous low-mismatch interfaces, surface roughness is an additional TDD limiting factor. The accumulated strain-fields of orthogonal misfit dislocations lying in the graded buffer typically result in periodic modulations of the surface morphology, often referred to as crosshatch.[62] At crosshatch trenches, where the film thickness is lowest, the misfit dislocation strain-field can propagate to the film surface and block threading dislocation glide. Thus, localized pinning of threads and dislocation pile-up formation can occur even in the absence of a high mismatch interface, driving further dislocation nucleation and interaction. Without adequate control of this dislocation interaction mechanism, the number of threading dislocations may quickly multiply despite compositional grading.

The growth parameter optimization for relaxed Ge_xSi_{1-x} buffers compositionally graded to Ge has been well documented, addressing all of the above considerations.[56] The Ge_xSi_{1-x} wafers produced as substrates for III-V growth in this work were grown by ultra-high vacuum chemical vapor deposition (UHVCVD) on (001) Si wafers offcut 6° towards [110]. It has previously been shown that substrate offcut towards [110] helps to reduce surface crosshatch buildup, thereby facilitating unhindered threading dislocation glide. To further reduce crosshatch effects, a chemical-mechanical polishing (CMP) step was incorporated at the midpoint of graded buffer growth. Etch pit density studies reveal that this method leads to a substantial reduction in overall TDD and dislocation pile-up density compared to samples grown without CMP, indicating the re-mobilization of threads once pinned by crosshatch. Ge_xSi_{1-x} buffers graded to 100% Ge at a rate of 10% Ge/μm featuring TDD as less than 8×10^5 /cm^2 can be reproducibly achieved by this technique. Figure II-2 (opposite) shows a

cross-section transmission electron microscopy (XTEM) image of a Ge_xSi_{1-x} buffer graded to Ge and Figure II-3 features a differential interference contrast microscopy (DICM) image revealing the etch pit density of the Ge cap layer.

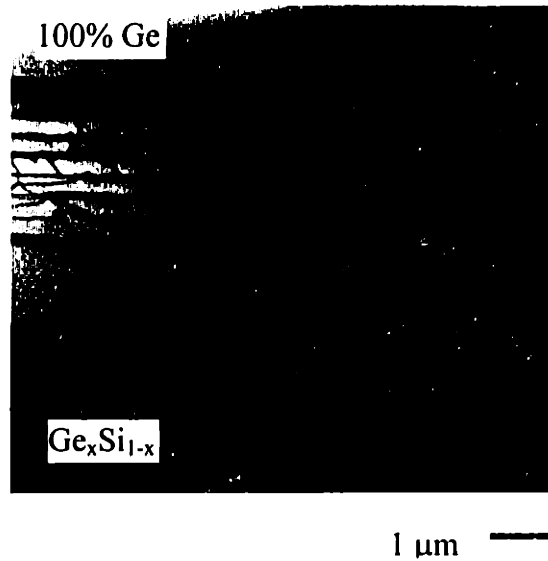


Figure II-2 *XTEM image of a Ge/Ge_xSi_{1-x}/Si film grown by UHVCVD*

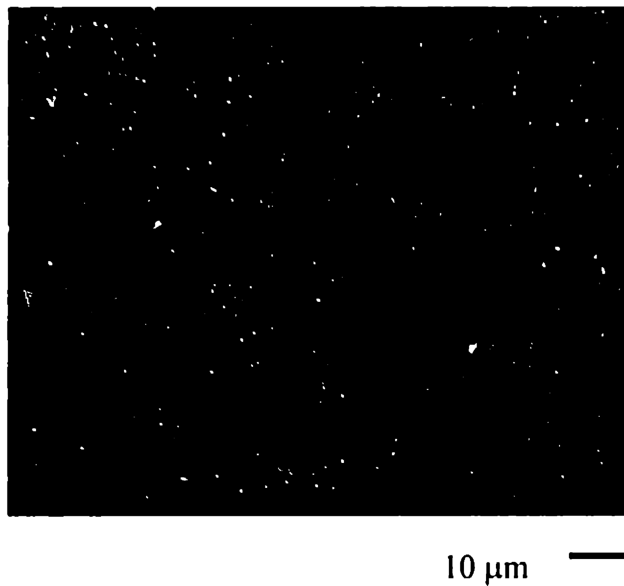


Figure II-3 *An etch-pitted Ge/Ge_xSi_{1-x}/Si film revealing a TDD density of 2 x 10^6/cm^2*

$GaAs/Ge/Ge_xSi_{1-x}/Si$ Heteroepitaxy Issues

Our work towards achieving low defect density $GaAs/Ge_xSi_{1-x}/Si$ shares the same goal as the voluminous published studies of GaAs/Si growth, but otherwise features more in common with the relatively few efforts directed towards GaAs/Ge heteroepitaxy.[63] Nonetheless understanding the GaAs/Si interface gives valuable added insight to the antiphase disorder problem since the clean (001) Si and Ge surfaces are remarkably similar, notwithstanding the disparity in their lattice constants. This similarity also extends to (001) Si and Ge surfaces exposed to arsenic precursors, with strong implications for GaAs domain orientation.

Surface Structure of (001) Si and Ge

Clean semiconductor surfaces are reconstructed, featuring atomic ordering that differs from the bulk material.[64] The surfaces of Si and Ge (001), which are of greatest interest for III-V epitaxy, are structurally characterized by dimer reconstructed terraces separated by steps.[40] Scanning tunneling microscopy (STM) is perhaps the most powerful tool for studying atomic step and dimer arrangements, although much of the same information can be extracted from interpreting *in-situ* RHEED or LEED patterns under UHV/MBE conditions. More recently, reflectance-difference spectroscopy (RDS) has emerged as an *in-situ* technique for detecting surface ordering that is compatible with the higher operating pressures of CVD systems.[41,65,66,67]

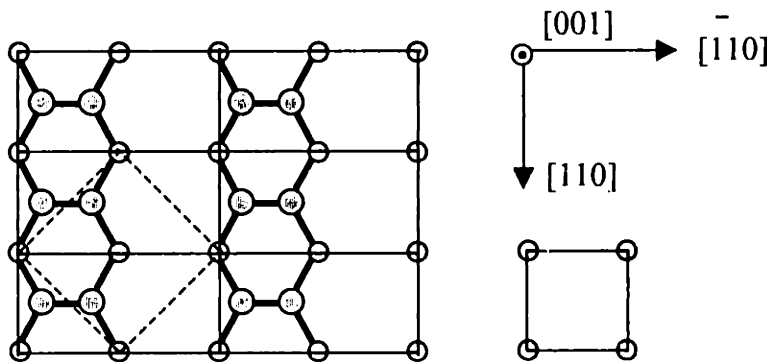


Figure II-4 *(001) Si or Ge (2 x 1) dimer reconstructed surface. The 1 x 1 surface primitive unit cell is shown to the right, and the bulk unit cell face is outlined in dashes.*

Pairing, or dimerization, of adjacent, four-fold coordinated Si or Ge atoms exposed on the (001) surface reduces the number of dangling bonds per atom from two to one and is therefore

energetically favorable. Figure II-4 (previous), a top-view of the reconstructed (001) surface, reveals dimer rows, occupying a (2 x 1) surface unit cell. Though not shown in Figure II-4, Si-Si and Ge-Ge dimers are often asymmetric, characterized by buckling of the dimerization axis both laterally and out of the surface plane.

The presence and distribution of steps running lengthwise along either [110] or $[1\bar{1}0]$ directions reflects any inadvertent or intentional deviation of the surface from the exact (001) orientation. Consider the single atomic-layer steps running along the $[1\bar{1}0]$ direction of the (001) Si or Ge surface as shown in Figure II-5. On alternating terraces separated by single-steps, or any odd-integer number of steps for that matter, the exposed sublattice shifts from one domain to the other, rotating the dimerization axis with it.

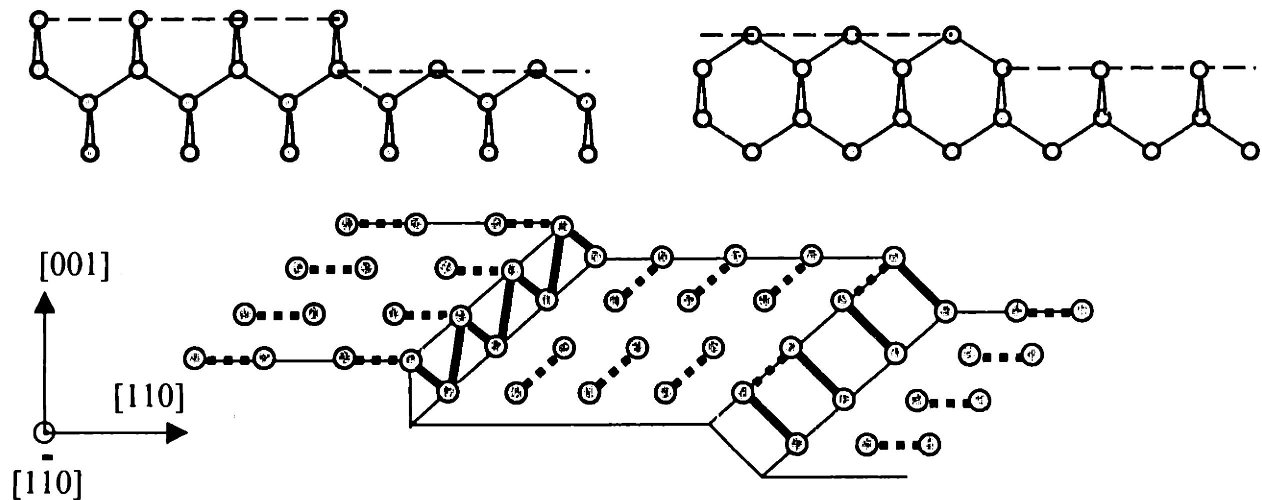


Figure II-5 *S_A (upper left) and S_B (upper right) single atomic-layer steps. On a mixed-domain surface (bottom) both types of single steps are evident. Note the rotation of dimerization axes and dimer rows on alternating terraces.*

Hence, surfaces featuring predominantly single atomic-layer steps are said to be double-domain, or mixed with (2x1) + (1x2) ordering, and it is possible to classify two distinct types of single-steps S_A and S_B.[68] On S_A steps the dimerization axis on the upper terrace is perpendicular to the step edge, whereas on S_B steps the dimerization axis on the upper terrace is parallel to the step edge. Since dimers arrange in distinct rows perpendicular to the dimerization axis, one may alternatively identify S_A and S_B steps as those with dimer rows parallel and perpendicular to the step edge, respectively.

Double atomic-layer steps, or any even-number layer steps, preserve the sublattice orientation on all terraces such that the surface is single-domain with only (2 x 1) or (1 x 2) ordering evident, not both. In analogy to the single-steps, it is possible to identify two types of double-steps D_A and D_B as shown below in Figure II-6.

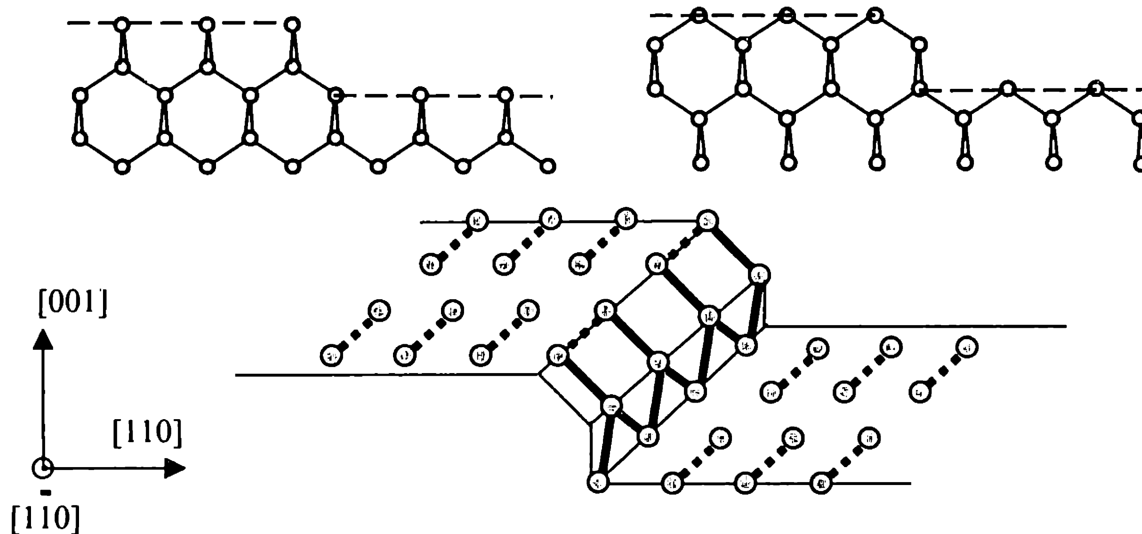


Figure II-6 *D_A (upper left) and D_B (upper right) double atomic-layer steps. Note that only D_B steps are observed experimentally, D_A steps are energetically unfavorable. On the single-domain surface (below) the dimerization axis and dimer rows are invariant across theD_B step.*

On surfaces featuring D_A steps the dimerization axis is always perpendicular to step edge, whereas surfaces featuring D_B steps the dimerization axis is parallel to the step edge. Likewise, all of the dimer rows are arranged either parallel or perpendicular to the D_A or D_B step edges, respectively.

S_A, S_B, and D_B steps on (001) Si and Ge have been observed experimentally by LEED,[42,43] and STM,[40] but never D_A steps. Calculations of step formation energy per unit length by Chadi have shown that D_A steps are in fact the least favorable on (001)Si; his results are summarized in Table II-1, note that the unit length *a* corresponds to the lattice constant of the (1 x 1) unit cell of the (001) surface.[68]

Table II-1 *Step Formation Energies per Unit Length on (001) Si (a = 3.85Å)*

Step	Formation Energy (eV/*a*)
S_A	0.01±0.01
S_B	0.15±0.03
D_A	0.54±0.10
D_B	0.05±0.02

Chadi's calculations were based on the so-called 're-bonded' step configuration, in which edge atoms on all steps reconstruct to form dimer-like bonds with lower terrace atoms. Aspnes and Ihm, suggested alternatively that D_B step formation was energetically favored by a π-bonded step reconstruction;[69] however, this configuration has never been observed, whereas re-bonding has.[70] The significant energy difference between a single D_B step versus a pair of $S_A + S_B$ steps promotes the formation of double-steps. On (001) Si and Ge substrates offcut to [110], the temperatures required to achieve the single-domain surface are approximately 1000 °C and 600 °C, respectively.

Arsenic-Terminated (001) Si and Ge Surfaces

Given an initially single-domain (001) Si or Ge surface, we may consider nucleating GaAs with an unbroken plane of either Ga or As atoms. This leads to two distinct sublattice orientations: GaAs-A and GaAs-B, respectively, which correspond to the same 90° rotation of the zinc-blende crystal structure illustrated earlier in Figure I-5. Thus, antiphase disorder could occur even on an initially single domain (001) Si or Ge surface due mixed nucleation of GaAs-A and GaAs-B as shown in Figure II-7.

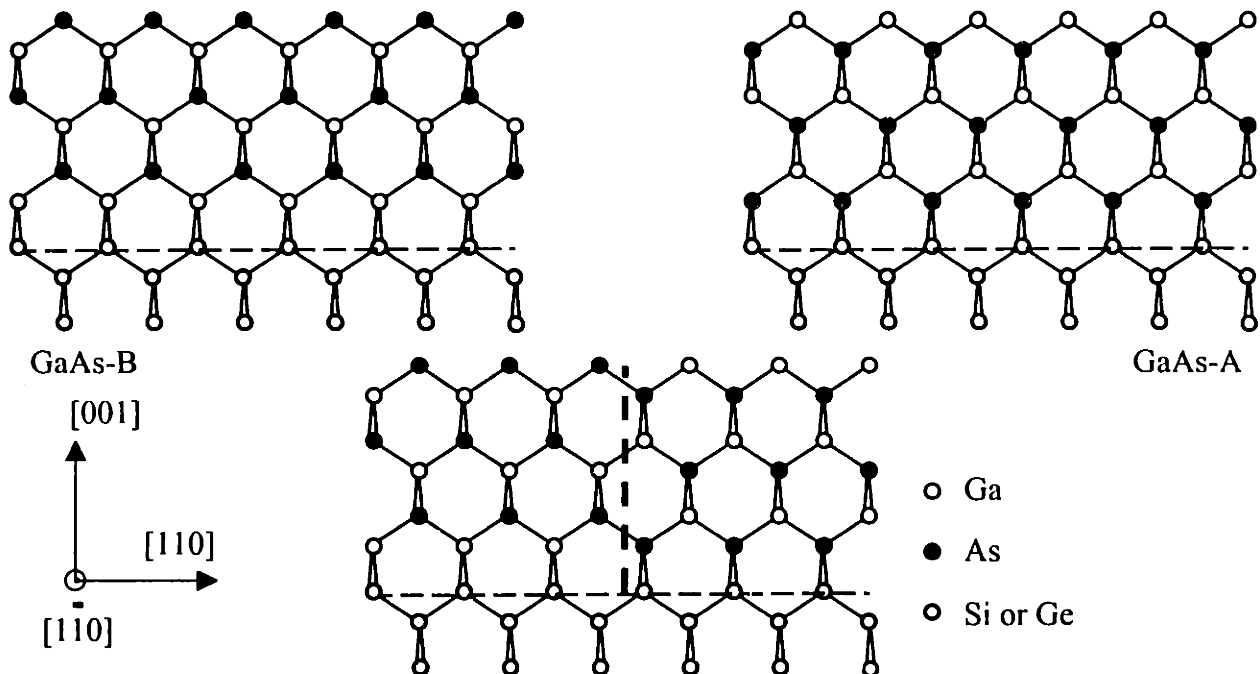


Figure II-7 *Single-domain GaAs-B (Ga-initiated), GaAs-A (As-initiated), and antiphase disorder (dashed line) due to mixed initiation on a single-domain (001) Ge or Si surface.*

In practice, initiation with a prelayer of Ga is complicated by the fact that Ga does not form a self-terminating monolayer on Si or Ge surfaces, but rather piles-up and diffuses rapidly. Control of Ga-initiated GaAs/Si or GaAs/Ge thus demands precisely controlled Ga dosage, usually only achieved under MBE conditions by calibrated measurements of RHEED intensity oscillations.[71] On the other hand, arsenic exposure is known to form a self-limiting monolayer coverage of symmetric arsenic dimers on Si and Ge surfaces. The resulting arsenic-passivated surface is inert with respect to further arsenic adsorption, and apparently lower in surface energy since each arsenic dimer atom possesses a fully-occupied lone

electron-pair state rather than a dangling bond. As a result, arsenic exposure, in the form of either As_4 or As_2 for MBE, and AsH_3 for MOCVD, is the most common means of initiating GaAs on Si or Ge.[57],[72] However, interaction with arsenic growth precursors may complicate the atomic structure of the clean (001) Si and Ge surfaces prior to film nucleation.[73,74,75]

There exists considerable evidence that arsenic pre-exposure can induce significant atomic rearrangement of the pre-existing Si and Ge surface structure, invalidating the assumption that an initially clean, double-stepped surface guarantees single-domain GaAs growth.[57,73,74,76,77] Arsenic-induced roughening of (001) Si surfaces has been reported prior to the onset of arsenic desorption at <600 °C,[73,77] and at lower temperatures, where a full monolayer of arsenic coverage exists, two distinct types of As adsorption have been observed by STM.[73,74] Apparently, arsenic dimers may either adsorb additively on top of the original Si dimers thereby rotating the sublattice domain by 90°, or they may altogether displace and substitute for Si dimers thereby preserving the original sublattice domain. As illustrated in Figure II-8, arsenic exposure of single-domain (2 x 1) Si (001) surface can actually result in two distinct single-domain As-terminated surfaces: (1 x 2) for additive arsenic dimerization and (2 x 1) for displacive arsenic dimerization, potentially allowing nucleation of either GaAs sublattice.

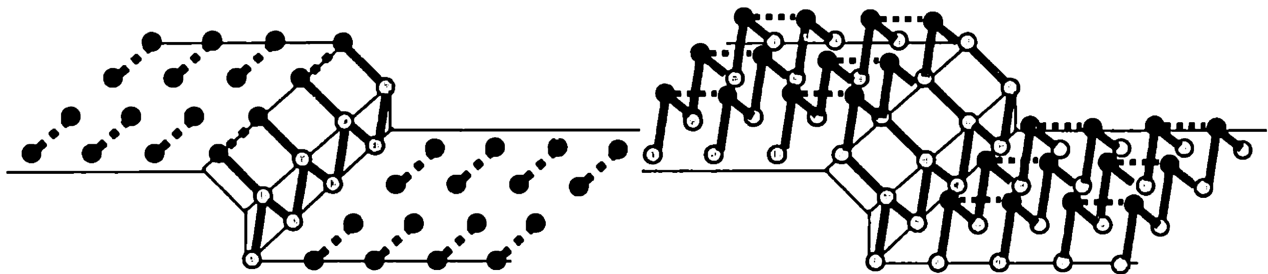


Figure II-8 *Displacive (left) and additive (right) dimerization of arsenic adsorbed on a single-domain (001) Si surface. Note the 90° rotation of arsenic dimers which may set the GaAs sublattice orientation.*

Moreover, as Bringans *et al.* first elucidated, the transition between adsorbed arsenic dimer orientations is not only temperature-dependent, but also sensitive to the sequence of arsenic exposure relative to the substrate temperature evolution.[74] Thus, arsenic exposure conditions alone can provide yet another possible mechanism for the occurrence of antiphase disorder.

Evidence for As dimer rotation and determination of GaAs sublattice determination thereby is not as conclusive for Ge (001) surfaces as for Si. Fitzgerald *et al.* noted that cracked AsH_3 exposure in GaAs/Ge grown by gas-source MBE invariably resulted in antiphase disorder, necessitating the usage of Ga prelayers.[78] On the other hand, Li *et al.* reported that MOCVD growth of GaAs/Ge of either sublattice orientation was possible, dependent upon the nucleation temperature, after annealing in AsH_3.[72] Pukite and Cohen did observe nearly identical As-induced atomic step rearrangements on Si and Ge offcut (001) substrates using RHEED, but their results were not otherwise consistent with others in the literature.[57,76] More recently, Gan *et al.* noted temperature dependent arsenic dimer orientation on Ge (001) during desorption from an arsenic passivated surface; however, their work neglected any evolution during arsenic adsorption and thus cannot be directly compared to earlier studies on Si.[79,80]

GaAs/Si vs. GaAs/Ge Heteroepitaxy

Despite the similarities of Ge and Si (001) surfaces, the growth modes and strain relaxation of GaAs/Si and GaAs/Ge films differ drastically. The GaAs/Si interface features a large surface energy due to not only the large lattice mismatch, but also the polarity of the interface. Hence there exists a strong tendency towards a Volmer-Weber growth mode, involving 3-D island formation at step edges during the initial stages of nucleation and leading to poor surface morphologies.[81,82] In general, the higher the GaAs initiation temperature, the larger the islands and the less dense they become. This problem is commonly dealt with by the so-called two-step growth process, which involves a low-temperature GaAs nucleation (< 400 °C) followed by growth at 'normal' elevated temperatures.[83] Low temperature nucleation allows the rapid coalescence of a continuous GaAs/Si film, which improves surface morphology at the price of higher point defect and stacking-fault density. Continued GaAs growth at high temperature essentially as GaAs preserves the smooth surface morphology and otherwise proceeds homoepitaxy would.

For planar growth, the critical thickness calculated for GaAs/Si from Equation 1.5 should be on the order of 10Å; however, the Matthews-Blakeslee equation is not valid for 3-D island growth.[81,84] In general, 3-D islands may remain coherently strained at thicknesses higher than

those predicted for continuous 2-D films, since the finite lateral dimensions reduce the effective epilayer strain. Nevertheless GaAs/Si strain relaxation occurs at such low thicknesses that dislocation climb, a diffusion mechanism, is initially dominant. Later, past a certain thickness, further strain relaxation occurs via glide of threads on the {111}<110> slip system. As previously discussed, homogeneous nucleation dominates and resulting in a high TDD.

GaAs/Ge heteroepitaxy is also characterized by the 3-D island nucleation, likely the effect of the polar interface.[29,85] Nevertheless, GaAs/Ge growth is often initiated at high temperatures > 600 °C with no reported degradation of surface morphology, suggesting rapid island coalescence and transition to a 2-D layer-by-layer Frank de Merwe growth mode.[72,86] As a result, normal strain relaxation proceeds as described by Equation 1.5 and the GaAs/Ge critical thickness is approximately 2200 Å. TDD of 5×10^5 cm^2 are typical, consistent with heterogeneous or substrate-limited nucleation of threads.[49]

Detection of Antiphase Disorder

Prior to actual GaAs/Si and GaAs/Ge film growth, ordering of Si and Ge surfaces may be monitored *in-situ* via RHEED, LEED, or RDS. It is thus possible to ascertain if the clean or As-terminated surfaces feature either mixed-domain (1 x 2) + (2 x 1), or single-domain (2 x 1) or (1 x 2) ordering. The corresponding surface reconstructions for GaAs(001) at ~ 600 °C are either mixed-domain (4 x 2) + (2 x 4), or single-domain (2 x 4) or (4 x 2), where the 2 x direction is set by As-As dimerization axis, see Figure II-9.[87]

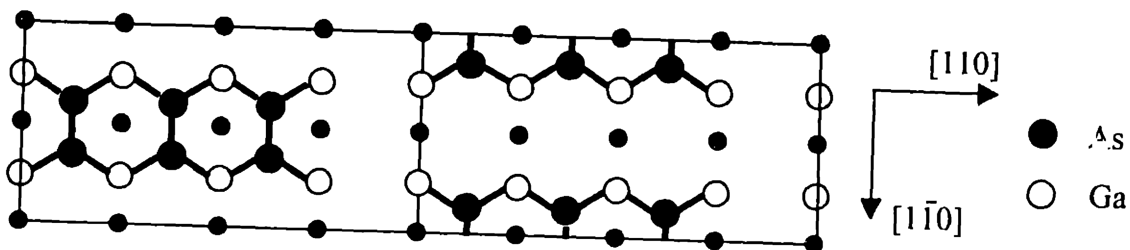


Figure II-9 *(2 x 4) reconstruction of the (001) GaAs surface.*

Mixed-domain reconstructions may usually be interpreted as the presence antiphase disorder; however, single-domain reconstructions may not be relied upon for definitively establishing the absence of antiphase disorder. In particular, antiphase disorder on a microscopic scale is

unlikely to be detected by *in-situ* surface spectroscopy techniques, since the relative areas of majority versus minority sublattice orientation may differ by orders of magnitude.

After growth, antiphase disorder in GaAs/Si or GaAs/Ge is often evidenced by rough surface morphologies due to the distortion of APBs that propagate to and intersect the film surface. Various defect-revealing chemical etches, molten KOH for example, have been used to further delineate and give a depth profile of APB density within the film.[72,88] Again, the primary limitation of these techniques is that small APDs and those that have annihilated close to the heterovalent interface are not likely to be observed. Although small, self-annihilated APDs may not pose a threat if device regions are integrated sufficiently far away, their presence indicates poor interface control and the factors determining APB propagation and annihilation are still not well understood.

To establish whether or not material is truly 'APB-free', depth profiling of GaAs/Si or GaAs/Ge films on the scale of APBs is required. For this task, characterization by transmission electron microscopy (TEM), in plan-view and cross-section (imaging perpendicular and parallel to the (001) plane, respectively), is useful for determining the size and distribution of APBs in a GaAs film. Holt predicted that APBs in the zinc-blende structure could only be imaged by two-beam dark-field diffraction conditions using {hkl} reflections satisfying the condition $h + k + l = 4n + 2$.[32] Later, Taftø *et al.* showed that convergent beam electron diffraction (CBED) could also provide APB contrast in TEM.[89] Despite these exotic proposed APB imaging conditions, it turns out that conventional two-beam bright-field (220) diffraction in fact reveals a strong stacking-fault-like contrast for APBs in GaAs due to the lattice displacement induced by wrong nearest-neighbor bonds.[33]

Monolithic Integration of III-V Devices on Si

Lacking a host IC with integrated Ge_xSi_{1-x} buffers for lattice-matched III-V heteroepitaxy, our monolithic integration demonstration demanded direct III-V on Si growth. Various studies in the literature have fabricated working III-V on Si optoelectronic devices albeit at substrantially reduced reliability and efficiency. For our purposes, we merely wish to integrate functional III-V components of a two-way optical link without compromising a host Si CMOS IC. Based on our development of low defect density GaAs/Ge/Ge_xSi_{1-x}/Si, it is expected that the development of a Ge_xSi_{1-x} composite IC will yield the necessary improvements in both performance and reliability to qualify our III-V on Si monolithic integration approach.

Defect Engineering of Direct III-V on Si Epitaxy

Our direct epitaxy approach was not at a complete loss for defect engineering since monolithic integration demands that some area of the host IC be set aside and patterned to reveal the bare Si surface for III-V growth. This requirement naturally lends itself to some TDD reduction since the finite dimensions of the device may allow some mobile threads to glide out to the perimeter of the growth area.[90] By comparison, for a blanket mismatched film deposited on a large substrate, few dislocations are likely to glide to the edge of a wafer before full strain relaxation has occurred. This concept of dislocation filtering by growth on patterned substrates is illustrated below in Figure II-10.

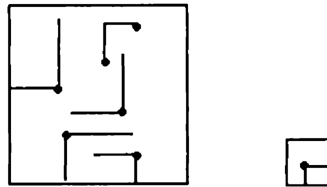


Figure II-10 *Dislocation filtering by patterning. Given a certain density of active heterogeneous sources or pre-existing glissile threads, a certain number of threads may glide to the pattern edges with additional applied strain. The smaller the patterned area, the greater the TDD reduction.*

Unfortunately, it has been shown that GaAs/Si growth on reduced areas does not result in TDD reduction.[49] Due to the high mismatch interface, strain relaxation occurs primarily by the uncontrolled homogeneous nucleation of many dislocations rather than the sustained glide of relatively few heterogeneously nucleated dislocations. The interaction and immobilization of a significant fraction of threads further minimizes the possibility of dislocation filtering via substrate patterning.

However, the addition of strained layers to a GaAs/Si film may allow some mobile threads to glide to pattern edges. Knall *et al.* reported factors of between 5 to 15 reduction in TDD for patterned growth of $In_xGa_{1-x}As$/GaAs/Si graded by various profiles to $In_{0.15}Ga_{0.85}As$.[91] Recent progress in $In_xGa_{1-x}As$/GaAs graded to $In_{0.3}Ga_{0.7}As$ (2% strain) in our own MOCVD reactor has achieved TDD less than 8.5×10^6 /cm^2. Since graded $In_xGa_{1-x}As$/GaAs is already an active area of research for infrared optical fiber interconnects at 1.3 μm and 1.55 μm wavelengths, fabricating our integrated optical interconnects using $In_xGa_{1-x}As$/GaAs/Si on selected areas was therefore a logical choice towards TDD reduction.

Grading to $In_{0.15}Ga_{0.85}As$, which gives only 1% additional strain over GaAs/Si, is an attractive option for optical interconnects since the 1.12 μm peak emission wavelength sits just below the 1.1 eV band-edge of Si, suggesting potential for through-wafer optical interconntects.[61] Note that an intervening blanket Ge_xSi_{1-x} buffer would absorb at similar wavelengths and might actually become a liability for this particular application.

Integrated III-V LED/p-i-n Diodes

The $In_{0.15}Ga_{0.85}As$/$In_xGa_{1-x}As$/GaAs/Si LED/p-i-n device structure chosen for this study simplified matters by allowing operation of the same diode, fabricated in just one III-V growth cycle, as either an emitter in forward bias or as a detector in reverse bias. In addition, this design also assured that the detector-emitter pairs would have their peak wavelengths matched to one another.

Nevertheless, the LED/p-i-n simplification also represents a significant design compromise. The purpose for the i-region in a photodetector is to expand the depletion region of the diode

junction thereby decreasing junction capacitance and increasing the volume of material where photons may adsorb and generate electron-hole pairs. However, increasing the depletion width also increases the volume of material in which a high TDD can interact with the diode. In reverse bias operation as a photodetector, the enhanced adsorption provided by the i-region must be weighed against an increased generation noise component to the dark current.

In forward bias operation as an LED, the expanded depletion region serves no useful purpose and increases the distance that electrons and holes must diffuse before they are injected as minority carriers across the junction. In a material featuring a high TDD, considerable non-radiative recombination may be expected of carriers traversing the depletion region resulting in a reduced internal quantum efficiency for the LED.

For characterizing the sensitivity of diodes to dislocation and other defect induced generation-recombination currents, one common figure of merit is the zero-bias resistance area product:

$$R_0A = (\partial V/\partial I \,|_{V=0})\, A \qquad (2.1)$$

where A is the active area of the detector.[92,93] Basically a normalized measure of leakage current, R_0A is easily extracted from the reverse bias diode I-V characteristic. For photodetectors, higher R_0A translates directly to lower dark current density and less detector-generated noise.

Process Integration

Conveniently, MIT's on-campus Microsystems Technology Laboratories (MTL) allowed complete fabrication of Discovery Semiconductor's host CMOS IC at MIT in the ICL up until III-V growth, after which the remainder of OEIC processing could be completed in the TRL. One outstanding complication encountered, however, was the incompatibility of photolithography tools between the labs. As a result, the OEIC masks had to be designed to account for the transition from the 10:1 reduction steppers in the ICL to the 1:1 contact aligners in the TRL.

In many ways the omission of integrated Ge_xSi_{1-x} buffers for III-V epitaxy simplified our integration task enormously. In addition to the thermal cycle incurred, a Ge_xSi_{1-x} buffer graded to Ge at the typical 10% Ge/μm produces a 10 μm protrusion above the original Si surface. By itself this poses numerous difficulties including poor step coverage and essentially impossible lithography. Having opted to process the OEIC without Ge_xSi_{1-x}, however, further discussion of these considerations and possible solutions will be postponed until Chapter VII.

The primary integration issue thus consisted of when and how to insert the III-V growth and processing sequence. Prior to growth, selected areas on the IC substrate were to be exposed to bare Si and isolated for III-V epitaxy, while CMOS device structures had to remain passivated. After growth, excess polycrystalline III-V deposit must be removed, and further processing is completed to passivate, contact, and finally connect the LED/p-i-n diodes to the CMOS driver circuits.

As previously stated, III-V growth must occur before final metallization of the IC and after any potentially compromising high temperature Si processes. An additional consideration was that after III-V growth, the remainder of processing would need to be completed in the TRL, which lacks many of the tools and recipes especially developed for Si IC processing. Hence, we naturally desired to postpone III-V growth and have as much as possible of the OEIC completed in the ICL along the lines of the standard MIT baseline CMOS process.

Conclusions

Our approach to III-V on Si monolithic integration is fundamentally different from other defect engineeering strategies in that it relies on suppressing TDD during heteroepitaxy rather than after the fact. Chapters III and IV deal primarily with the study of antiphase disorder in GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si, leading to the optimization of APB-free MBE and MOCVD growth. Chapter V evaluates the effectiveness of TDD reduction by grading Ge_xSi_{1-x} to the GaAs lattice constant. Direct III-V on Si epitaxy and the monolithic integration of $In_{0.15}Ga_{0.85}As$/ $In_xGa_{1-x}As$/GaAs/Si devices with Si CMOS are presented in Chapter VI.

Chapter III

GaAs/Ge Heteroepitaxy by Solid-Source MBE

GaAs growth by MBE

Molecular beam epitaxy is a UHV thin film deposition process in which a highly controlled flux of growth precursors is delivered to a heated substrate. In solid-source MBE of GaAs, the precursor flux is generated by thermal evaporation of elemental arsenic and gallium from shuttered crucibles known as effusion cells. Since precursor vapor pressure is governed by effusion cell temperature, the evaporated flux of impinging precursor atoms and the GaAs growth rate is entirely independent of substrate temperature. Film morphology is, however, a strong function of substrate temperature, since it determines adatom mobility and the desorption rate of arsenic back to the vapor. In the limit of very low substrate temperature, non-stoichiometric, poly-crystalline, or even amorphous film growth may occur. At high temperatures, growth of GaAs and other arsenide compounds above the typical 600-650 °C is limited by the ability to maintain an arsenic flux high enough to prevent net arsenic desorption from the substrate.

The remaining important MBE GaAs growth parameter is the As/Ga flux ratio. The vapor pressure of gallium over GaAs at 600-650 °C is much less than that of arsenic, allowing the assumption that all impinging gallium atoms stick to the substrate. Excessive gallium adsorption may lead to the coalescence of gallium droplets, whereas impinging arsenic atoms will readily desorb from the substrate unless combined with gallium adatoms to form GaAs. Hence growth usually takes place in an excess arsenic flux which consists of either tetrameric As_4 or cracked As_4, which gives dimeric As_2. Whereas As_2 can adsorb directly on the gallium-stabilized surface, the temperature dependent dissociation of As_4 determines its rate of incorporation in the GaAs film. Exactly which arsenic species produces the highest quality GaAs films still remains debated.[94,95]

The UHV (10^{-10} torr) growth environment not only minimizes background contaminant incorporation but also allows *in-situ* monitoring of the film surface by RHEED. The diffraction pattern created by a high-energy electron beam at grazing incidence to the substrate is highly sensitive to the atomic structure of the surface. Clean 2-D surfaces are marked by elongated streaks whereas distinct spots appear at the onset of 3-D roughening due to bulk-like diffraction. RHEED intensity are sensitive to the degree of surface adatom

coverage and their oscillations provide a convenient means of monitoring layer by layer 2-D film growth. In addition, RHEED patterns can be used to identify the atomic ordering of specific surface reconstructions that appear at various GaAs growth regimes.

In the current work, close monitoring of RHEED pattern evolution proved critical for the identification of a single-domain Ge surface for GaAs nucleation. However, the additional defect morphology correlation provided by our study, sets it apart from previous MBE GaAs/Ge studies[46,47,57] based on the dubious premise that RHEED alone can verify if material is 'APB-free.'

Preparation and Growth of GaAs/Ge samples

A Varian Gen II MBE system with a 10^{-10} torr base pressure was used at OSU to grow the GaAs/Ge samples for our defect morphology study.[71] In addition to dimeric As_2 and Ga precursor cells, the reactor was also fitted with a Ge effusion cell for the deposition of epitaxial Ge buffers. Starting materials consisted of quarter-pieces of 2" (001) Ge substrates offcut 6° toward the [110] direction obtained from Eagle-Picher. Prior to growth, samples were cleaned by alternately oxidizing the Ge surface in H_2O_2, stripping the grown oxide in 10 DI H_2O: 1 HF, and rinsing in DI H_2O.[96] This cleaning procedure minimizes carbon contamination of the Ge surface, which has been shown to hinder atomic step rearrangements.[97] Substrates were mounted in the reactor chamber on a Mo block with either clips or indium bonding and substrate temperature was monitored during growth via either an optical pyrometer at > 500 °C or a thermocouple at < 500 °C fixed to the mounting block. An Auger electron spectrometer (AES) and a 16-18 kV RHEED electron beam provided further *in-situ* monitoring of the Ge surface.

Growth of the most generic GaAs/Ge heterostructure began with a 20 minute anneal at 650 °C for thermal oxide desorption, followed by deposition of a 0.1 μm Ge buffer layer on the original substrate surface at 350 °C. This layer served to reduce the effects of any residual surface contamination as confirmed by AES to promote smooth step-flow. GaAs growth was then initiated on the Ge buffer either as-grown or after an additional 20 minute anneal at 650 °C followed by a quench to 350 °C. The 650 °C anneal promoted formation of a single-

domain Ge surface as evidenced by the appearance of a (2 x 1) RHEED pattern featuring half-order streaks along the offcut [110] direction. Dropping the temperature back to 350 °C prepared the substrate for low temperature GaAs nucleation.

To test the effect of GaAs initiation by either an As prelayer or a Ga prelayer, a number of samples of both types were grown for comparison. Whereas the application of an As_2 flux to the Ge surface resulted in a self-limiting As monolayer, growth initiated with a Ga prelayer required previous calibration of the Ga exposure time using RHEED intensity oscillations to confirm full monolayer coverage of the surface. The next step, growth of the migration-enhanced epitaxy layer (MEE), consisted of 10 alternating monolayers of Ga and As_2 at 350 °C. This low temperature MEE layer was intended to maintain a 2-D surface morphology and to minimize autodoping effects by limiting surface exchange of Ge during GaAs film initiation. Bulk GaAs growth at beam equivalent pressure (BEP) As_2/Ga ratios of ~10-15 commenced with the co-evaporation of a 100 nm layer at a substrate temperature of 350 or 500 °C (~ 0.1 μm/hour) followed by GaAs growth (~ 1 μm/hour) of various thicknesses at ~600 °C. Figure III-1 illustrates the growth sequence of a generic sample as described above.

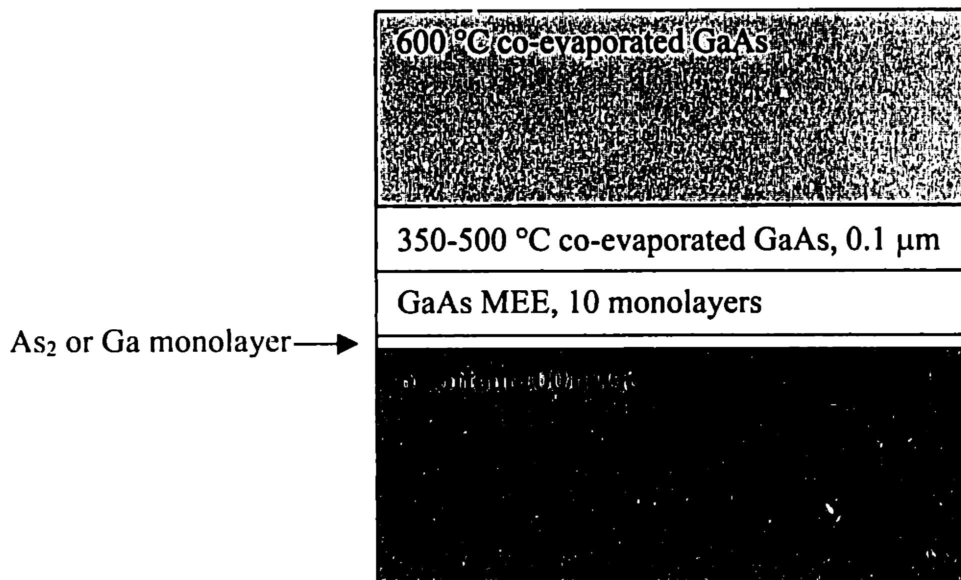


Figure III-1 *Generic GaAs/Ge sample structure.*

JEOL 200CX and 2000FX transmission electron microscopes equipped with LaB_6 filaments were operated at 200kV to examine cross-section (XTEM) and plan-view (PVTEM) samples prepared by mechanical polishing and argon ion-milling.

GaAs/Ge Defect Morphology

Worst Case GaAs/Ge

Since GaAs is nearly lattice-matched to Ge, GaAs/Ge films are expected to exhibit a fairly perfect misfit dislocation array and a very low density of threading dislocations ($<10^6$ cm^{-2}). However, if proper control of the Ge surface and the initial GaAs buffer layer are not obtained, the resulting GaAs/Ge epilayers may feature an irregular misfit dislocation array as well as a high density of both threading dislocations and APDs.

One such worst case sample, among the first in the series grown for this study, is featured in Figure III-2 which shows PV and XTEM images of a 1 μm thick GaAs/Ge film grown without a Ge buffer and initiated with a Ga prelayer at 350 °C.

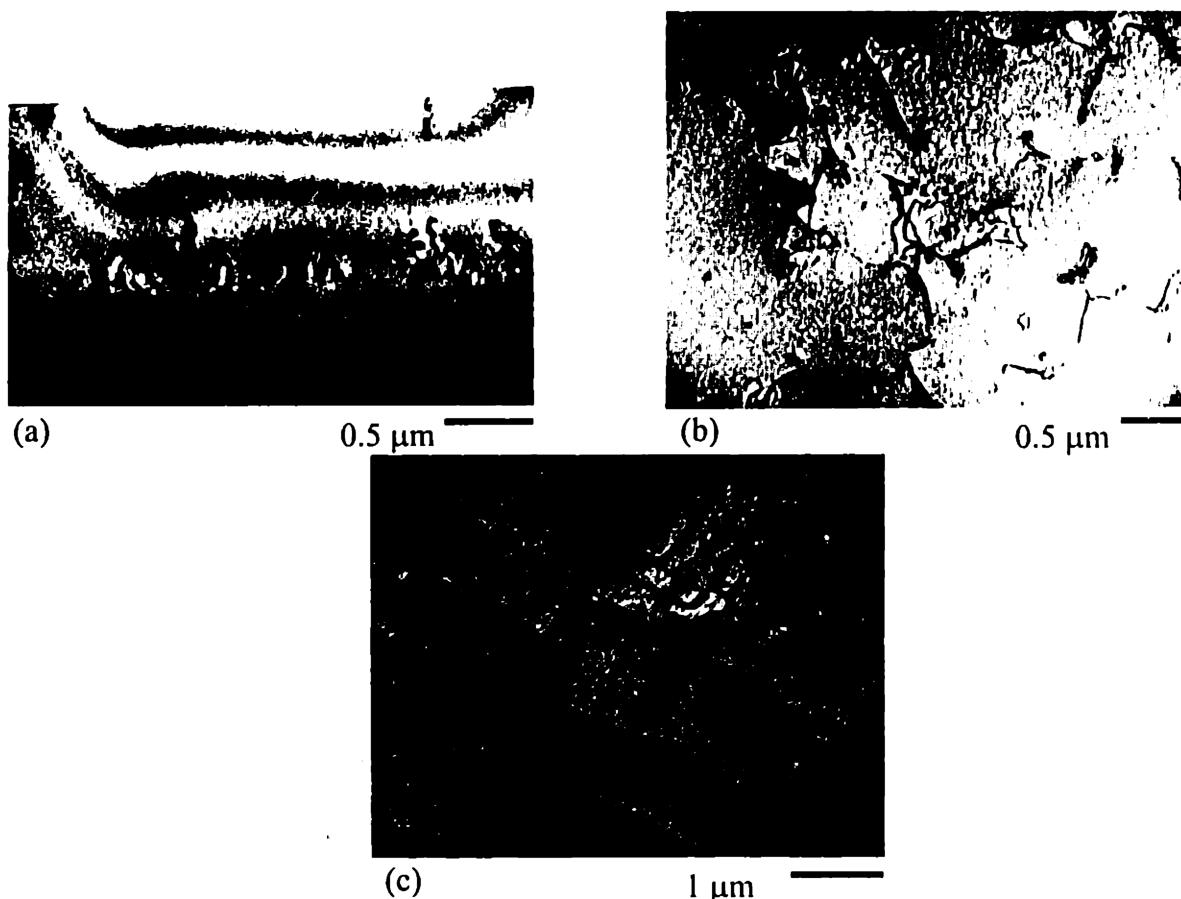


Figure III-2 *TEM images of a 1 μm Ga-initiated GaAs/Ge film in cross section (a) and plan-view (b) reveal numerous threading dislocations and APDs propagating well above the GaAs/Ge interface. An irregular misfit dislocation network is also evident in plan-view (c).*

Both the MEE layer and the 0.1 μm low-temperature GaAs layer were grown at 350 °C. Despite the pre-growth anneal at 650 °C, the XTEM image in Figure III-2 (a) indicates the presence of APDs propagating well into the film. A high density of threading dislocations is also evident. In Figure III-2 (b), a PVTEM image of the same sample near the interface, also reveals numerous small APDs and a TDD > 2 x 10^8 /cm^2. Figure III-2 (c), another plan-view of the GaAs/Ge interface shows that a somewhat irregular misfit dislocation network has formed in lieu of the regular orthogonal misfit network expected of a low-mismatch system.

In the following discussion we will demonstrate that an unexpectedly high density of threading dislocations as well as numerous antiphase boundaries can occur when growth conditions are not well controlled. We will then show that high quality, low defect density GaAs/Ge can be achieved by solid-source MBE with the proper interface control and optimum growth sequence.

Threading Dislocations

Arsenic Loop Condensation

Epitaxial GaAs is often non-stoichiometric under typical As-rich growth conditions, especially at low temperatures, resulting in high concentrations of various arsenic point defects. As reported by Melloch *et al.*, high temperature annealing (~600 °C) of LT-GaAs grown by MBE at 250-400 °C can leads to the condensation of excess As point defects and the formation of As precipitates.[98] In bulk, non-stoichiometric GaAs grown by the horizontal Bridgman technique, the condensation of As point defects to form dislocation loops as well as As precipitates has been reported to occur at about ~600 °C.[99] In the current work, although As precipitates were not observed in the low temperature GaAs buffer layer which followed the MEE layer, a high concentration of arsenic point defects incorporated during the low temperature growth is apparently responsible for the condensation of dislocation loops during the subsequent high temperature GaAs growth. Our observations are consistent with the mechanism of excess As interstitial condensation on {111} planes to form dislocation loops with a/2 <110> Burgers vectors, as proposed by B. T. Lee *et al.*[99]

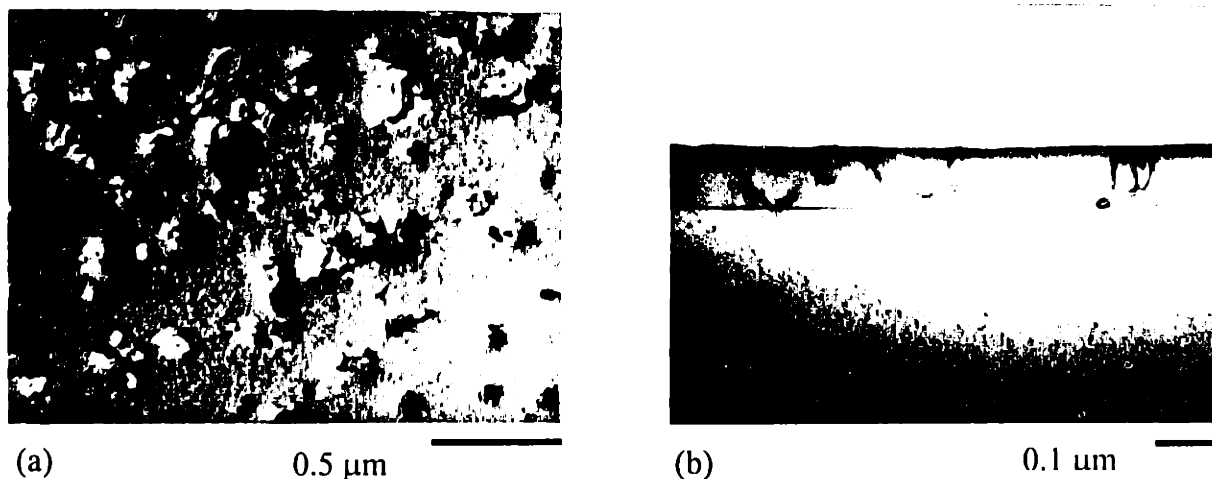


Figure III-3 *PVTEM (a) and XTEM (b) images of a 0.1 μm GaAs/Ge film similar to that of Figure III-2. Numerous dislocation loops have nucleated as a result of point defect incorporation during GaAs buffer growth at 350 °C followed by their condensation after high temperature annealing at ~ 600 °C.*

Loop formation is clearly observed in the plan-view TEM image shown in Figure III-3 (a). The 0.1 μm GaAs/Ge film is grown under conditions identical to that of the sample featured

in Figure III-2; however, a 600 °C anneal has replaced the additional GaAs coevaporation at 600 °C. Since the film is below the 2200 Å equilibrium critical thickness for GaAs/Ge, it is not likely that dislocations have nucleated in response to strain and no misfit dislocations are evident. Rather, the loops must have originated from point defect condensation. In Figure III-3 (b), an XTEM image of the same sample, it is evident that many dislocation segments have threaded to the surface of the film.

Excess Nucleation of Threads

Given the opportunity to condense at the GaAs/Ge interface and expand to the surface of the film at 600 °C, each dislocation loop can generate a pair of threading dislocations. Once the thickness of the film exceeds the critical thickness, these threads may glide to form an irregular misfit dislocation network as illustrated below in Figure III-4.

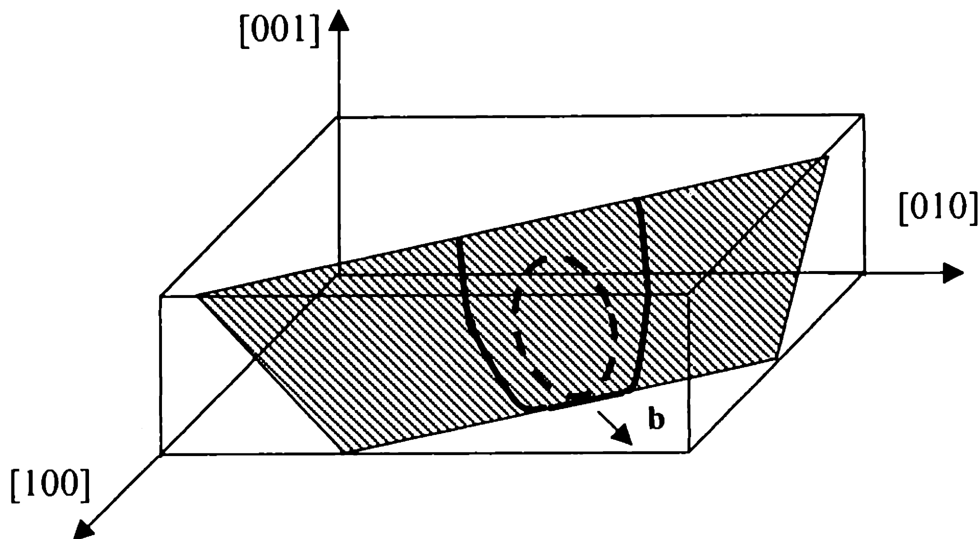


Figure III-4 *Condensation and expansion of a dislocation loop. Due to the in-plane* a/2[110] *Burgers vector, the loop cannot glide on the* (111) *plane, but instead climbs to the GaAs/Ge interface and film surface. This frees two threading dislocations that may now glide on the* $(1\bar{1}\bar{1})$ *or* $(1\bar{1}1)$ *planes.*

Figure III-5 (opposite), which features plan-views of an As_2-initiated 1 μm GaAs/Ge film grown on an un-annealed Ge buffer without MEE, but otherwise identical to the samples in Figure III-2 and Figure III-3, seems to confirm this idea. Taken at diffraction vectors of [220], $[2\bar{2}0]$, and [400] respectively, Figure III-5 (a)-(c) together comprise a **g•b** analysis of the dislocation network at the GaAs/Ge interface.

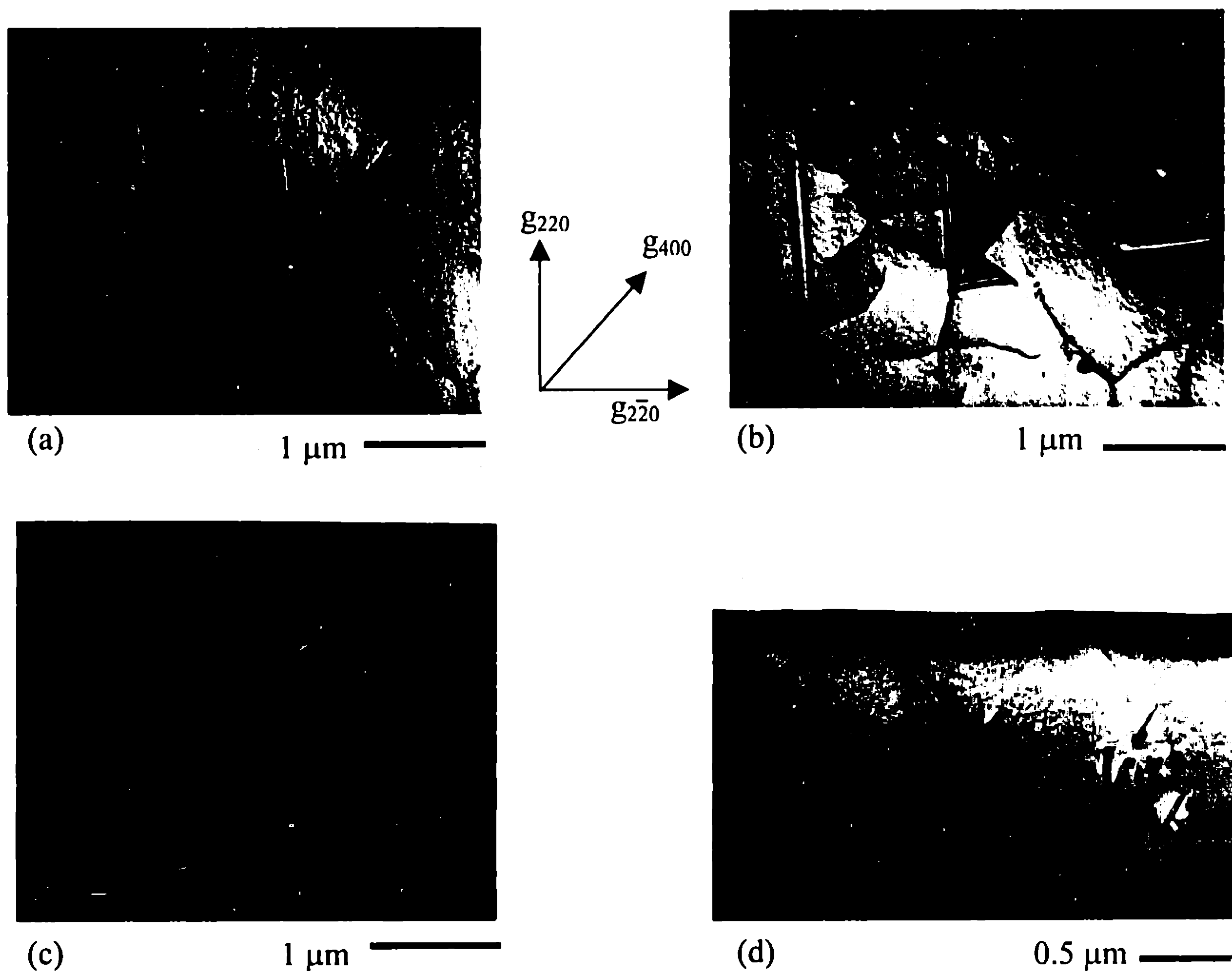


Figure III-5 [220] *(a),* [400] *(b), and* [$2\bar{2}0$] *(c) PVTEM images of an As_2-initiated 1 μm GaAs/Ge film interface. Note the loss of contrast for dislocation loops in (a) indicating an in-plane Burgers vector of* a/2[$1\bar{1}0$]. *Stacking faults and threads also disappear alternately in (a) and (b). 5 (d) shows the same film in cross-section.*

Strong contrast for the dislocation loops is apparent in Figure III-5 (b) and (c); weak contrast is evident in Figure III-5 (a) with complete extinction evident along the [$1\bar{1}0$] direction. Complete extinction under the **g** [220] condition indicates satisfaction of the invisibility criterion **g•b** = **0**, such that the Burgers vector **b** for the loops lies along [$1\bar{1}0$]. The residual contrast arises where the dislocation is no longer purely edge, i.e. where the line direction **u** is not parallel to [$1\bar{1}0$] such that **g•b x u** ≠ **0**. The loss of contrast for many of the threading dislocation segments in Figure III-5 (a), also indicates that they have the same in-plane Burgers vector as the dislocation loops. Therefore it seems likely that they are the result of

loop expansion to the surface of the film as the sample is heated to ~600 °C, the final growth temperature.

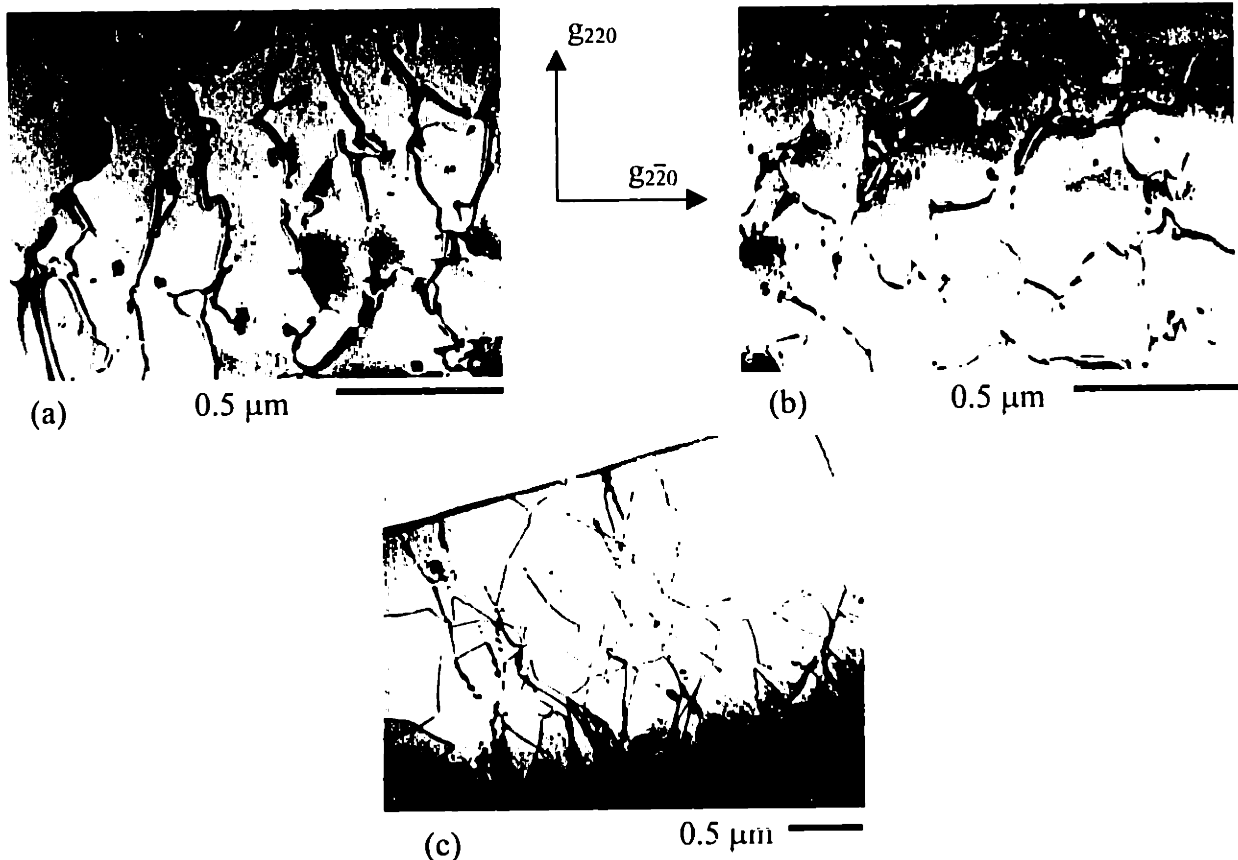


Figure III-6 [220] *(a) and* [2 $\bar{2}$ 0] *(b), PVTEM images of the interface of a 2.5 μm GaAs/Ge film similar to that of Figure III-5. A highly irregular misfit dislocation network has formed as a result of loop-dominated strain relief. Orthogonal dislocation components disappear alternately, revealing the in-plane Burgers vector, again. A very high density of threading dislocations is observed in XTEM (c).*

The 2.5 μm film in Figure III-6 also includes a 350 °C initial GaAs layer and is otherwise identical to the previous films, but the more dense and irregular dislocation network suggests the complete expansion of many more loops due to mismatch strain. Whereas both orthogonal dislocation components (lying along the [110] and [1 $\bar{1}$ 0] directions) are clearly evident in the [220] bright-field image of the 1 μm film in Figure III-2 (c), they appear alternately in the [220] and [2 $\bar{2}$ 0] plan-view images of the 2.5 μm film of Figure III-6 (a) and (b). From such a **g•b** analysis it may be concluded that this irregular misfit network consists of sessile edge dislocations with in-plane [1 $\bar{1}$ 0] and [110] Burgers vectors. Such misfit

segments are consistent with expansion of dislocation loops whose threading arms are free to glide as a result of their out-of-plane line direction.

These results suggest that above the GaAs/Ge critical thickness there may exist competition between the propagation of 60° dislocations normally responsible for film relaxation in low-mismatch systems and the expansion of previously nucleated dislocation loops at the strained interface. Which relaxation mechanism ultimately prevails seems to depend on the presence or absence of MEE following the initial prelayer. The samples in Figure III-5 and Figure III-6, grown without MEE, are dominated by the expansion of nucleated dislocation loops whereas a more normal-looking misfit network is still observed forming in the sample in Figure III-2, grown with MEE.

Since the MEE layer consists of alternately applied monolayers of Ga or As rather than co-evaporated fluxes of both in an As_2 overpressure, it may be expected that fewer As point defects are incorporated during its growth, even at 350 °C. The MEE may thus serve to suppress the condensation of As point defects and the loop nucleation rate at the GaAs/Ge interface which might otherwise be a highly effective sink for such defects. In such a case, the incorporated As point defects would be forced to condense and nucleate loops in the bulk GaAs above the interface instead, resulting in a considerably lower density of nucleated loops overall. Moreover, the in-plane Burgers vector of the dislocation loops would limit participation in strain-relief by preventing glide to the interface. Nevertheless, uncontrolled variation in low temperature measurements by thermocouple cannot be entirely ruled out as an alternative explanation for the wide range of dislocation network morphologies.

Regardless of whether or not the nucleated dislocation loops participate in strain relief, their residual threading arms readily interact with other dislocations and obstruct their gliding motion. The net result is an excess of threading dislocations as revealed by the XTEM images of Figure III-2 (a), Figure III-3 (b), Figure III-5 (d), and Figure III-6 (c). The measured threading dislocation densities, on the order of 10^8-10^{10} cm^{-2}, are in fact comparable to higher mismatch GaAs/Si films.

Once dislocation loop nucleation due to excess arsenic incorporation was diagnosed as the cause of unexpectedly high threading dislocation densities, their removal became a simple matter of increasing the growth temperature of the initial 0.1 μm GaAs buffer layer to 500 °C, thus restoring stoichiometry.

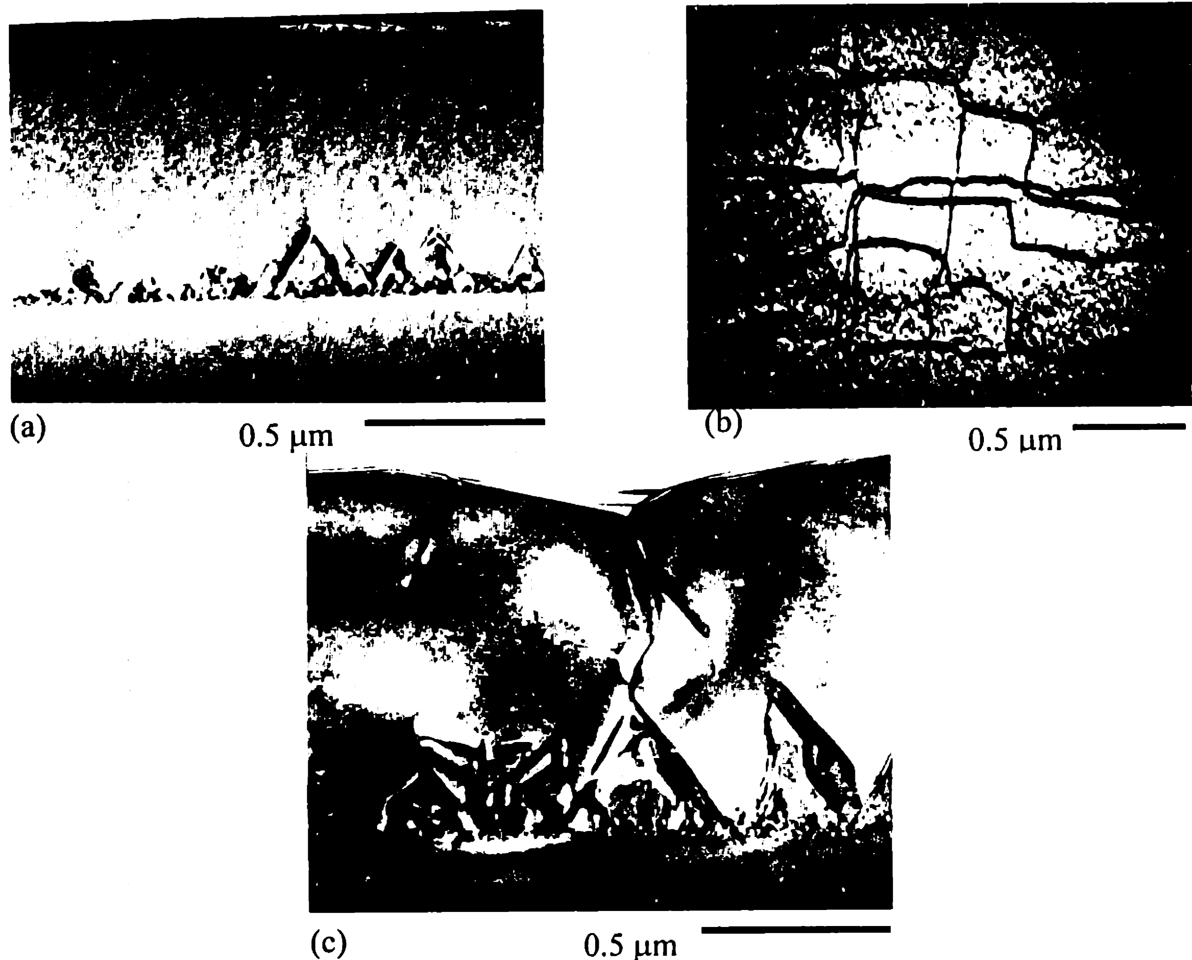


Figure III-7 *XTEM (a), (c), and plan-view (b) TEM of a 1 μm As_2-initiated GaAs film grown directly on un-annealed Ge. Raising the GaAs buffer growth temperature to 500 °C prevented loop nucleation. A uniform layer of annihilated APDs is evident in (a), but APDs extend to the film surface elsewhere in (c), suggesting contamination.*

Figure III-7 (a) is an XTEM image of a 1 μm GaAs/Ge film initiated by As_2 exposure at 500 °C after a ~600 °C anneal without an MEE layer or Ge buffer. Note the conspicuous absence of threading dislocations and the uniform layer of APDs above the GaAs/Ge interface. In Figure III-7 (b), the plan-view of the GaAs/Ge interface in the same sample, a heavily kinked, orthogonal misfit dislocation network is observed and no dislocation loops are in evidence.

The crooked appearance of the dislocation segments reflects their glide over or around APBs as a result of their inability to cut through them. It has been speculated that a trade-off between strain energy vs. APB energy is the origin of such APB/dislocation interactions.[63,100] However, we suspect that electrostatics may play a role as well, since both the dislocation cores of III-V materials and APBs themselves are charged defects. Figure III-7 (c), an XTEM image taken elsewhere on the same sample reveals the presence of APDs extending to the film surface and blocking the glide of dislocations. The drastic difference in film quality compared to Figure III-7 (a) is thought to be evidence of Ge surface contamination.

Antiphase Disorder

APD Self-annihilation

The most common strategy for eliminating APDs entirely from III-V on IV epilayers has already been discussed; namely the use of (001) wafers offcut to [110] subjected to a high temperature pre-growth anneal to promote a single-domain surface. In the event of incomplete surface reconstruction, antiphase disorder substrate offcut should also facilitate the self-annihilating behavior of APDs. Enhanced APD self-annihilation for GaAs/Ge grown on offcut substrates has been reported by both N. Guelton *et al.* and Y. Li *et al.*[63,72]

Our experimental results indicate that the annihilation height of APDs in GaAs/Ge heteroepitaxy can vary considerably even on substrates featuring the same 6° misorientation angle.

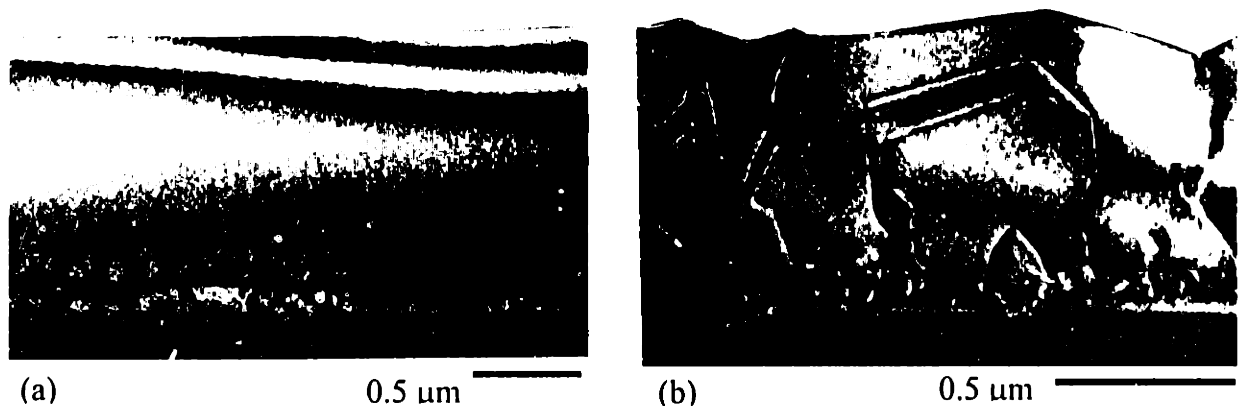


Figure III-8 *Bright-field [220] XTEM images of 1 μm As_2-initiated GaAs grown on an un-annealed Ge buffer. Despite identical growth conditions, wide variations in APD height are observed which were attributed to un-controlled As_2 exposure of the Ge surface at 500 °C.*

This point is clearly illustrated in Figure III-8, a pair of [220] bright-field XTEM photos of 1 μm thick GaAs/Ge films grown exposed to As_2 at 500 °C under conditions similar to those of the sample in Figure III-7. However, to reduce the effects of surface contamination, a 0.1 μm Ge buffer was grown on the original substrate surface at 350 °C. Such a surface should feature evenly spaced, single atomic layer steps a/4[110] high. In both micrographs III-8 (a) and III-8 (b), a dense layer of annihilated APDs is evident close to (within 200 nm) the interface as might be expected of GaAs/Ge at a high offcut angle. Whereas no APDs extend

into the remainder of the film in III-8 (a), consistent with previous reports of 'single-domain' GaAs/Ge by APD annihilation,[46,47] in III-8 (b), APDs propagate to the sample surface.

Clearly this behavior does not follow the simplistic relationship between step density and average APD annihilation height previously discussed. A close examination of the GaAs/Ge interface is provided in Figure III-11 (b) which shows [200] dark-field images of the same films in Figure III-8.

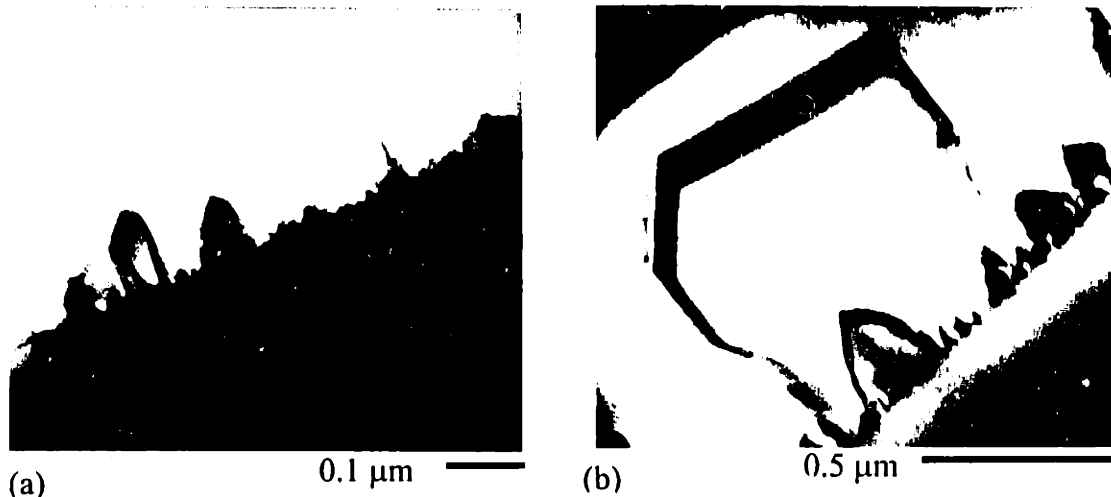


Figure III-9 *Dark-field [200] XTEM images of the same GaAs films featured in Figure III-8. In each image a dense layer of small APDs exists at the interface while only a few larger APD extend well above the interface. At left, APD height is limited by self-annihilation at ~100 nm, whereas at right, this behavior persists until APDs reach the film surface. Note also the enclosure of an APD within a larger APD in (b).*

It is immediately evident that the annihilated layer of APDs consists of many self-annihilated micro-domains within the first ~10-20 nm above the GaAs/Ge interface, in addition to a smaller number of taller APDs extend up to ~150 nm into the film before annihilating as well. For a 6° offcut Ge substrate, the average single-step separation distance should be on the order of 13.5 Å such that the observed APDs might well be the product of a single-stepped Ge surface. The presence of those APDs that are an order of magnitude larger than others, however, suggests that they may be the products of domain coalescence. Figure III-11 (b) shows the same film as in Figure III-8 (b) imaged in under a [200] dark-field such that single large APD is observed enclosing many smaller domains.

APD Coalescence

We propose that given an initial density APDs nucleated at the GaAs/Ge interface, a certain fraction of those APDs will annihilate boundaries with one another rather than self-annihilate with continued film growth as a result of their close proximity. Such APD coalescence may dominate in the limit of a very dense APDs, whereas self-annihilation becomes the limiting behavior for low density APD distributions. As is the case for domain self-annihilation, domain coalescence results in an energetically favorable reduction in APB energy. However, rather than reducing the average APD height as in the case of self-annihilation, increased APD height is possible with domain coalescence because APDs of a larger mean width are produced in a distribution less dense than the original. Further coalescence may occur as the film grows creating an overall APD 'coarsening' effect that is ultimately self-limited by the decreased density of APDs with continued coalescence. In this manner, self-annihilation of APDs by crystallographic propagation of APBs should prevail in the end as suggested by Y. Li *et al.*, but the 'coarsened' APDs may be so large and sparse in distribution that for practical film thicknesses, complete annihilation is never achieved.[88] Figure III-10 illustrates the competing mechanisms of self-annihilation and coalescence and their influence on APD distribution in a grown film.

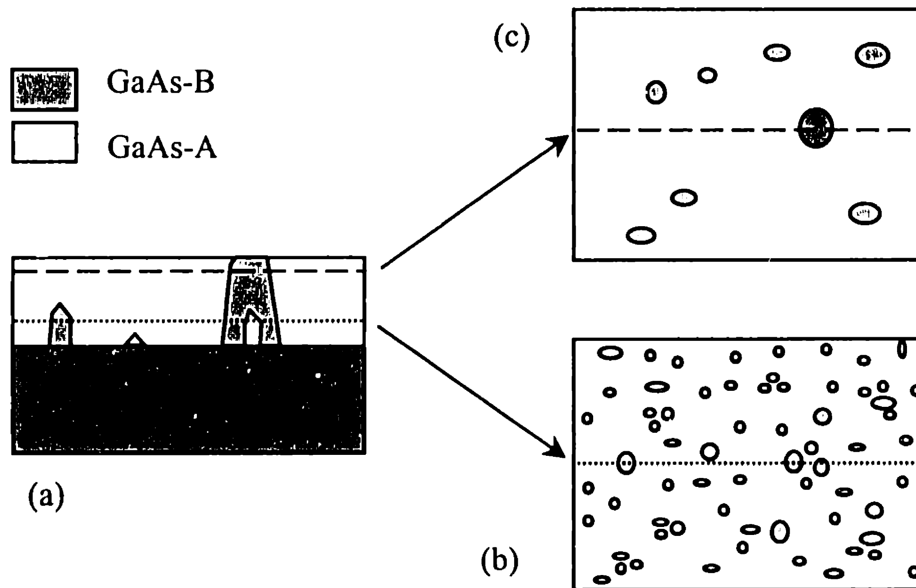


Figure III-10 *APD self-annihilation vs. coalescence. A GaAs/Ge film viewed in cross-section (a) features APDs of various heights. Horizontal slices through the film viewed from above are featured in (b) and (c) where the relative position of the cross-section (a) is indicated by the dashed lines. A dense distribution of small APDs evident near the GaAs/Ge interface in (b) develops into a looser distribution of larger APDs featured in (c). Many of the smaller APDs self-annihilate their boundaries, but neighboring APDs in close proximity may annihilate boundaries with one another instead. This may result in the enclosure of one phase of GaAs, by the other, as illustrated in (a.)*

The variation in final APD heights observed in Figure III-8 are apparently the result of a wide disparity in the density of nucleated antiphase domains during GaAs initiation at 500 °C. Figure III-11 shows PVTEM images across the GaAs/Ge interface which correspond to the to the XTEM images of Figure III-8.

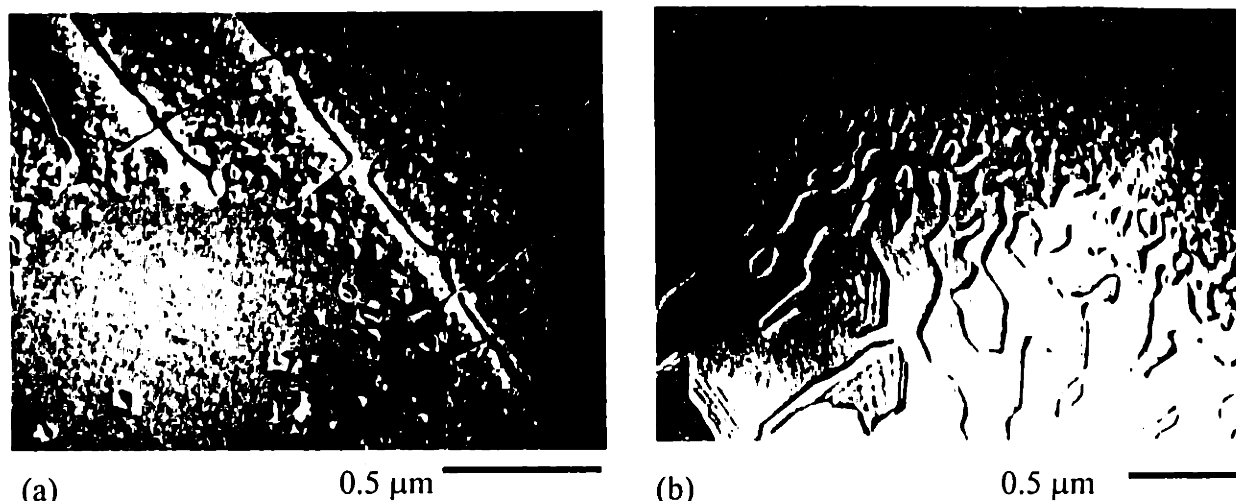


Figure III-11 *PVTEM images of the GaAs/Ge interfaces corresponding to the XTEM images of Figures III-8 and 9. At left, the APDs in have largely self-annihilated above the interface, whereas at right a coarsened APD distribution has developed. Note the enclosure of one phase GaAs by the another.*

By ion milling the PVTEM samples at an angle to the film normal, the GaAs/Ge interface was thinned for examination along a shallow bevel, revealing both the interface and the GaAs epilayer. The GaAs/Ge interface itself is delineated in the micrographs by a slight change in contrast. In Figure III-11 (left), as before, the misfit dislocations are slightly kinked and ride slightly above the GaAs/Ge interface due to the layer of APDs. However, it is of interest to note that in Figure III-11 (right), no misfit dislocations are evident since the presence of APDs at the film surface has altogether prevented dislocation glide to the interface.

Numerous small APDs are seen in the vicinity of the GaAs/Ge interface in Figure III-11 (a), but very few extend well into the GaAs epilayer. From the previous discussion, these observations are consistent with the dominance of self-annihilating behavior early in the GaAs growth. In stark contrast, Figure III-11 (b) provides evidence that APD coalescence

prevails, resulting in APDs extending through the film thickness as shown in Figure III-8 (b). There exists a much denser interfacial layer of APDs in Figure III-11 (b); furthermore, it is evident that the mean APD size increases with distance from the GaAs/Ge interface. Strong evidence for APD coalescence is observed in Figure III-11 (b), where a volume of one phase GaAs has completely enclosed a volume of the opposite phase GaAs. Such a defect structure is likely to arise if annihilation of boundary area between several neighboring APDs has occurred.

The Role of Arsenic Exposure

Having attributed the difference in final APD height to a disparity in initial APD density, the source of the latter discrepancy should also be examined. Since growth of the two GaAs films compared in Figures III-7, III-8, and III-11 was initiated under identical controlled conditions, only an uncontrolled variable can have been responsible. In particular, we imediately suspected the initial As_2 exposure conditions at 500 °C were a factor since Fitzgerald *et al.* earlier associated the prevalence of APDs with As_2 exposure (from cracked AsH_3) during GaAs/Ge by gas-source MBE.[78]

Previous studies of (001) arsenic-adsorbed Si surfaces (Si:As), have indicated reconstructions that are highly sensitive to both temperature and arsenic flux. Working with MBE growth of GaAs on Si initiated with As_4 exposure, Kawabe *et al.* identified two distinct single-domain reconstructions for offcut (001) Si:As surfaces: a (2 x 1) at low temperature (< 450 °C) and a (1 x 2) at high temperature (>600 °C).[75] On the contrary, STM studies by Becker *et al.*, revealed the same reconstructions, but the opposite temperature dependence: (1 x 2) at 400 °C and (2 x 1) at 600 °C.[73] Bringans *et al.* corroborated Becker's results and further revealed that kinetic barriers to the formation of (001) Si:As reconstructions were the likely source of inconsistency.[73]

Recall from Figure II-8 that the (1 x 2) and (2 x 1) Si:As reconstructions correspond to additive or displacive arsenic adsorption and dimerization on an originally clean (2 x 1) Si surface. As noted earlier, the reconstructed (001) surfaces of clean Si and Ge are remarkably similar, such that (001) Ge:As dimer reconstructions might also be sensitive to temperature

and As flux. Incomplete arsenic domain rotation would invariably lead to a mixed-domain (1 x 2) + (2 x 1) Ge:As surface and subsequent antiphase disorder. Hence the APDs observed in Figures III-8, III-9, and III-11 suggest that the 500 °C initiation temperature lies near an arsenic-induced surface transition. Although these samples were initially mixed domain, lack of control over the duration and pressure of the initial As_2 flux might account for varying degrees of domain rotation, which in turn might account for the variations in initial APD density and the resulting average APD height.

A re-examination of Figures III-5 and III-6 provides further suggest a temperature dependent arsenic effect. The featured samples are both initiated with As_2 at 350 °C, and although the GaAs/Ge interfaces are somewhat obscured by excessive dislocation nucleation, both PV and XTEM reveal a conspicuous absence of APDs. Apparently the suspected As-induced transition observed at 500 °C is completely avoided at 350 °C. Despite the relatively clean GaAs/Ge interface in these samples, a number of irregularly-distributed small APDs were observed in plan-view elsewhere as shown in Figure III-12. These are most likely attributable to the lack of a high temperature Ge surface anneal.

0.5 μm

Figure III-12 *PVTEM image of small APDs near the GaAs/Ge interface in the sample previously imaged in Figure III-5. Although initiated on an un-annealed Ge buffer, the images of Figure III-5 featured no evidence of antiphase disorder, the few APDs observed here perhaps indicate residual single-steps due to kinetic limitations.*

Optimized GaAs/Ge Growth Procedure

Based on the above discussion, we arrived at an optimized growth procedure to simultaneously avoid the rampant nucleation of threads and APDs. Previous samples had relied on either 650 °C annealing of the original Ge surface or the deposition of a Ge buffer at 350 °C without further annealing to suppress antiphase disorder. Falling short of success, both approaches were now combined to allow GaAs growth on an epitaxial Ge buffer annealed at 650 °C after its deposition. RHEED pattern observations verified that a (2 x 1) single-domain Ge surface was obtained on the epitaxial buffer (note, however, that the azimuths were misidentified in Reference 71). Furthermore, the initial As_2 exposure temperature was now reduced from 500 °C to 350 °C to avoid the suspected Ge:As surface transition. To prevent the condensation of excess As point defects into dislocation loops, however, the substrate temperature was raised from 350 °C to 500 °C after the MEE layer.

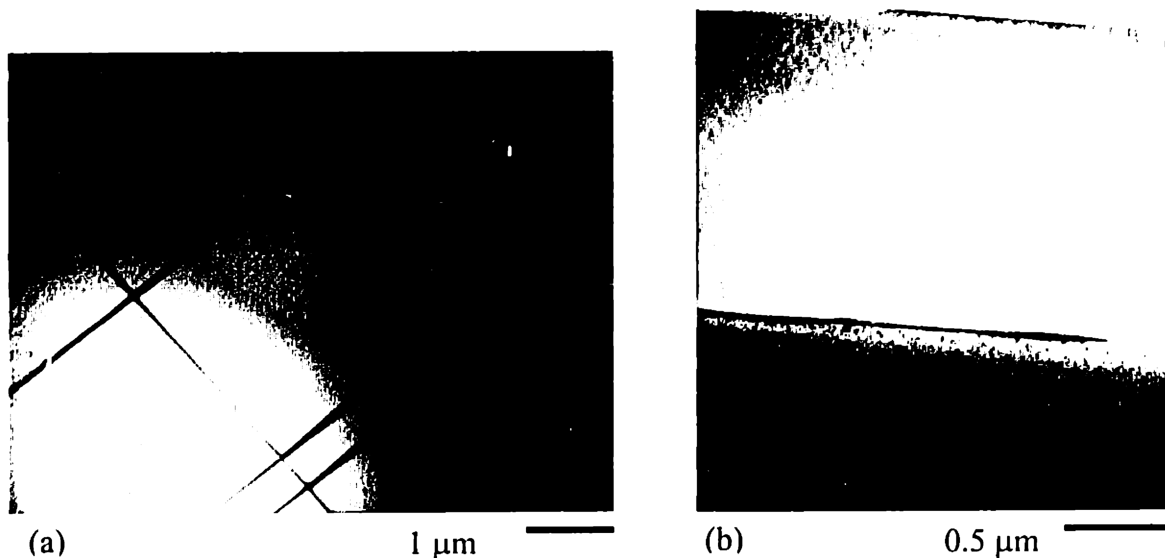


Figure III-13 *PVTEM (a) and XTEM (b) images of a 1 μm GaAs/Ge film grown on an annealed Ge buffer with As_2 exposure at 350 °C. Neither threading dislocations nor APDs are evident.*

Figure III-13 features PV and XTEM images of a 1 μm GaAs film initiated with As_2 exposure at 350 °C on an annealed Ge buffer. It is immediately apparent that the GaAs/Ge interface is extremely clean and APD-free to within the detection limits of TEM. Furthermore, by limiting low temperature GaAs growth to just the 350 °C MEE layer, nucleation of dislocation loops was avoided altogether and a regular array of unperturbed misfit

dislocations characteristic of an ideal low-mismatch heteroepitaxial system has formed. Very few residual threading dislocations were observed over many PVTEM images suggesting a density of less than $10^7/cm^2$.

Similar film quality was achieved with Ga-initiated growth on annealed Ge buffers. Figure III-14 features images of two such 1 μm GaAs/Ge films whose growth sequences were otherwise identical to the previous As_2-initiated sample.

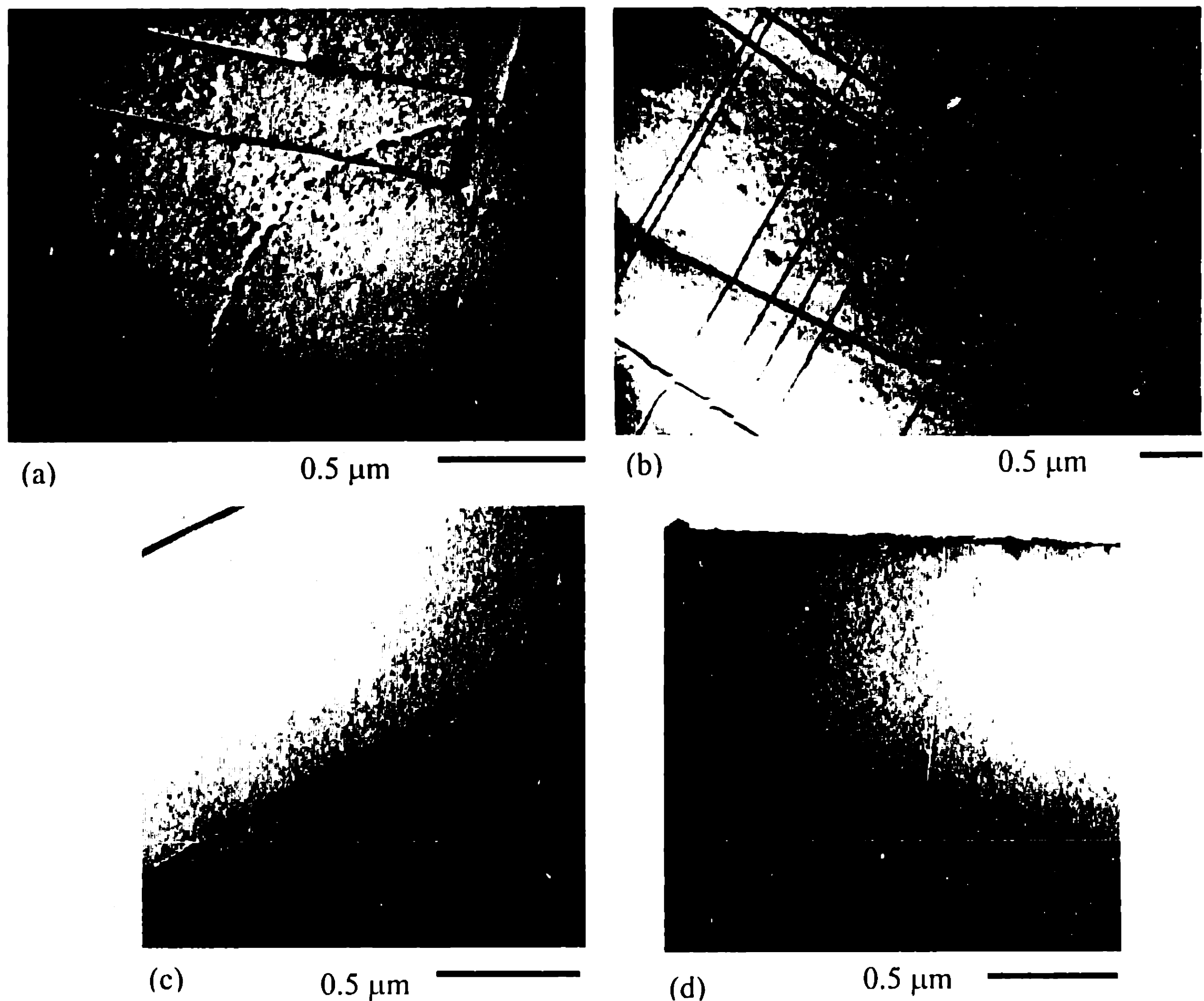


Figure III-14 *PVTEM (upper) and XTEM (lower) images of two Ga-initiated 1 μm GaAs/Ge films grown on annealed Ge buffers. The sample featured in (a) and (c) was initiated at a higher background pressure (>10^{-9} torr) than that shown in (b) and (d). Contamination of the Ga prelayer due to the presence of background species results in APD nucleation.*

Whereas the PV-TEM images featured in Figure III-14 (a) exhibits a layer of sparsely distributed APDs, the plan-view in 14 (b) does not. The same is shown in the corresponding XTEM images (c) and (d), respectively. The contrast in film quality demonstrates the chemical sensitivity of the Ga prelayer since the sample in 14 (a) was initiated at a higher background pressure (10^{-9} torr) than that of the sample in 14 (b). Since As_2-initiated samples at comparable background pressures were APD free, this suggests that prelayer contamination by low levels of residual arsenic and other background species is the source of antiphase disorder in Ga-initiated samples. Nevertheless, given a lower background pressures ($< 10^{-9}$ torr), the Ga-initiated sample exhibits virtually identical film quality to that of the As-initiated sample.

RHEED patterns of GaAs/Ge growth under these optimized conditions revealed a (2 x 4) GaAs reconstruction (see Figure II-9) regardless of the pre-exposure species, As_2 or Ga, to give the GaAs-A sublattice orientation (see Figure II-7)[71] For As_2-initiated samples, the 2 x azimuth, aligned with the [110] offcut direction, indicates the arsenic dimerization axis lies perpendicular to the Ge step edges, consistent with the low temperature additive arsenic adsorption observed by Bringans on offcut Si (see Figure II-8).[74] In the context of antiphase disorder appearing during As_2 exposure at 500 °C, this suggests that onset of competing displacive arsenic dimerization. That the same reconstruction and GaAs-A growth may be achieved with Ga initiation most likely indicates atomic exchange between the Ga monolayer and the subsequent As_2 exposure.[101]

Conclusions

Based on our study of GaAs/Ge defect morphologies, we have identified MBE growth parameters and strategies that minimize antiphase disorder and prevent unexpectedly high threading dislocation densities. An epitaxial Ge buffer annealed at high temperature provides the cleanest, uniformly single domain surface for the initiation of APD-free GaAs-A on Ge. Control of the As_2 exposure conditions must be maintained to prevent APD nucleation. The effects of As_2 exposure are minimized at substrates temperatures well below 500 °C, although As_2 flux may be a factor as well. Ga-initiated GaAs/Ge is particularly sensitive to APD nucleation via prelayer contamination; hence, maintaining a low background pressure is

essential. To prevent incorporation of excess arsenic point defects, low temperature GaAs co-evaporation should be avoided altogether. Nucleation and subsequent expansion of dislocation loops from point defects might otherwise compete with normal GaAs/Ge strain relaxation, resulting in a high density of residual threading dislocations.

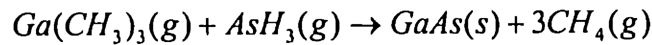
Chapter IV

GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si Heteroepitaxy by MOCVD

GaAs epitaxy by MOCVD

MOCVD GaAs

MOCVD film growth relies on the vapor phase mass transport of reactant molecules that decompose pyrolytically at the heated substrate. Typical MOCVD reactors operate at pressures ranging from 0.1 to 1.0 atm, and the most commonly used growth precursors for GaAs epitaxy are arsine (AsH_3) and trimethylgallium (TMG).[102] The driving force for epitaxy is vapor-phase supersaturation of these reactants over the substrate and an overall growth reaction may be expressed:



$$Ga(CH_3)_3(g) + AsH_3(g) \rightarrow GaAs(s) + 3CH_4(g)$$

Note, however, this is an extreme simplification of a complex growth chemistry, neglecting numerous side and intermediate reactions which take place simultaneously in both the gas-phase and on the GaAs surface.[103]

In contrast to MBE, the supply of precursor molecules is intimately related to substrate temperature, which controls not only their decomposition rate, but also the hydrodynamic properties of the carrier gas stream (typically H_2) and reactor system as a whole. Three limiting temperature regimes for film growth rate exist: kinetic, mass-transport, and thermodynamic. At low temperatures, growth is limited by the decomposition of reactants at or near the substrate surface and increases exponentially with temperature. AsH_3 decomposes or 'cracks' heterogeneously at the surface, whereas TMG decomposes homogeneously; both are 100% pyrolyzed at about 500-550 °C. Above this limit, the growth rate is determined by mass transport of reactants to the vapor/solid interface, ideally by diffusion through a well-behaved boundary layer created by laminar flow conditions. Only weak temperature dependence is exhibited since vapor phase diffusion D increases as approximately $T^{3/2}$ and reactant flux through the boundary layer may be described:

$$J = \frac{D(p_o - p_i)}{RT\delta} \tag{4.1}$$

where R is the universal gas constant, δ is the boundary layer thickness, and p_0 and p_i are the reactant partial pressures at the boundary layer and vapor-phase interface, respectively. Above 750 °C, the growth rate gradually decreases as the overall reaction equilibrium shifts back towards the vapor phase.

GaAs epitaxy is usually performed between 600-650 °C in the mass transport regime where growth efficiency and film quality are optimum. An important exception, as previously noted, is low temperature GaAs/Si nucleation via the two-step growth process. The input V/III partial pressure ratio, typically » 1, plays a large part in determining the stoichiometry and background doping characteristics of the GaAs film.[104,105] In analogy to As-rich MBE growth, an overpressure of AsH_3 is maintained to prevent arsenic desorption from the GaAs substrate at high temperatures, even when not growing a film. Under these conditions, TMG is nearly depleted at the vapor-solid interface and its input partial pressure determines the growth rate according to Equation 4.1.

The Thomas Swan atmospheric-pressure MOCVD research reactor used in this study features a horizontal quartz chamber with a water-cooled top-wall as shown in Figure IV-1. This type of reactor configuration provides optimum growth uniformity as previously noted by Giling *et al.*[106] Substrates are manually placed onto the tilted graphite susceptor which is then loaded through the rear of the reactor chamber. A quartz-sheathed thermocouple inserted into the radiatively heated susceptor provides feedback to a temperature controller coupled to a water-cooled halogen lamp/reflector assembly.

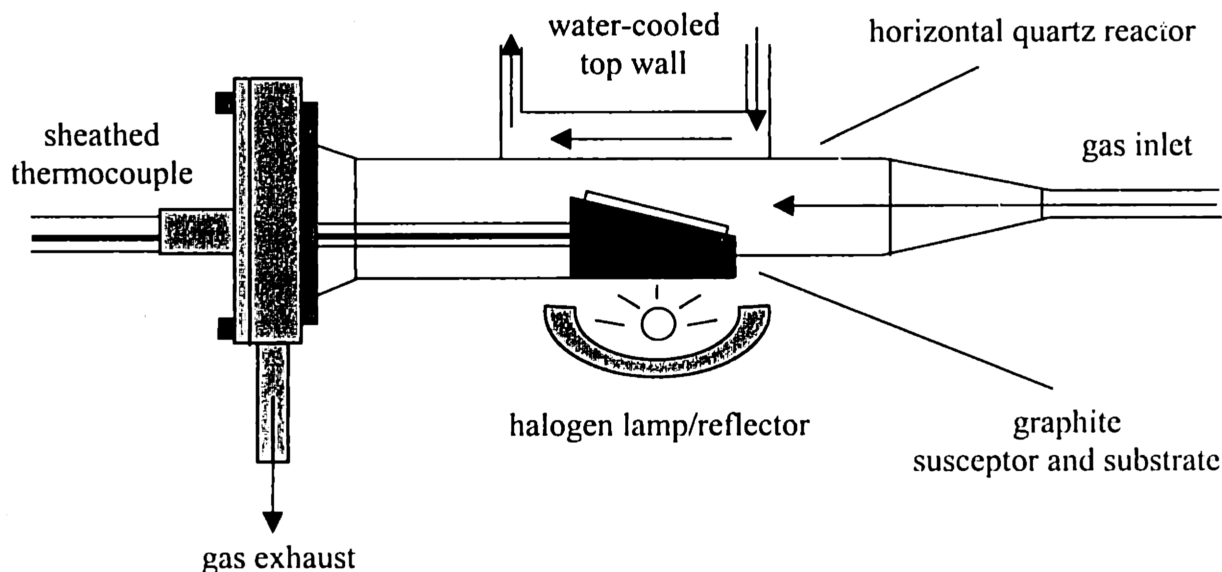


Figure IV-1 *Schematic of the horizontal AP-MOCVD reactor used for the study of GaAs/Ge/Ge$_x$Si$_{1-x}$/Si heteroepitaxy.*

There are relatively few studies in the literature of GaAs/Ge heteroepitaxy by MOCVD which have dealt specifically with controlling antiphase disorder.[37,72,107] It is unlikely that the well understood bulk GaAs growth parameters such as V/III ratio and growth rate, impact the occurrence of antiphase disorder. Rather the pre-nucleation Ge surface structure, which remains poorly understood under MOCVD conditions, should determine the GaAs sublattice orientation. Based on our OSU GaAs/Ge collaboration, we are well prepared to extrapolate our MBE experience to our MOCVD results.

Sample Preparation and Growth Conditions

Substrate material was cleaved from Ge or $Ge/Ge_xSi_{1-x}/Si$ wafers to a size of several square centimeters in order to fit the graphite susceptor. The fully-relaxed, compositionally-graded $Ge/Ge_xSi_{1-x}/Si$ wafers were grown by UHVCVD under a variety of experimental conditions as the grading process was optimized. The original (001) Si wafers used to grow $Ge/Ge_xSi_{1-x}/Si$ were offcut 6° to [110]. Ge (001) 6° offcut substrates donated from OSU were originally purchased from Eagle-Picher.

Following the OSU procedure, prior to growth, the Ge surfaces were cleaned by alternately dipping in solutions of 30% H_2O_2 and 10:1 diluted HF with de-ionized (DI) water rinses between dips. The final dip in dilute HF left the Ge surface hydrophobic prior to loading. The effectiveness of similar Ge cleaning procedures has previously been noted. [96,97]

The growth sequence for samples in this study was designed to evaluate the effects of pre-nucleation annealing in a variety of ambients and through a range of temperatures. A typical growth cycle starts with an initial 10 minute bake at 350 °C and a 5 minute anneal at 650 °C, both in N_2. A ten minute pre-nucleation anneal in N_2 or H_2, with or without flowing arsine (AsH_3), was then conducted at temperatures ranging from 400-650 °C, and GaAs was subsequently nucleated at the same temperature by adding either trimethylgallium (TMG) and AsH_3, or TMG to the previously established carrier flow. The nucleation layer was grown for ~0.1 μm, followed by an additional GaAs growth of varying thicknesses at 650 °C in H_2. At all times, an input V/III ratio >100 was maintained.

Anisotropic sidewall etching in a 1:8:1 solution of de-ionized H_20 : 30 % H_20_2 : H_2SO_4 was performed on 5 μm thick GaAs films grown on Ge substrates using a deposited oxide mask of stripes along the [110] direction. In this manner the sublattice orientation of the GaAs film was identified and correlated to sublattice orientation surface morphology features as characterized by differential interference contrast microscopy (DICM). Argon ion milling was used to prepare samples for plan-view and cross-section transmission electron microscopy (TEM) performed in a JEOL 2000FX to inspect the quality of the GaAs/Ge interface.

Single Domain GaAs/Ge and GaAs/Ge_xSi_{1-x}/Si

Annealing the Ge surface at > 600 °C before dropping to the nucleation temperature is essential for single-domain GaAs growth. To illustrate this point, annealing for 5 minutes at 400 °C instead of 650 °C before simultaneous exposure to AsH_3 and TMG results in a clouded GaAs/Ge/Ge_xSi_{1-x}/Si film. The rough surface morphology, as revealed by DICM in Figure IV-2 (right)

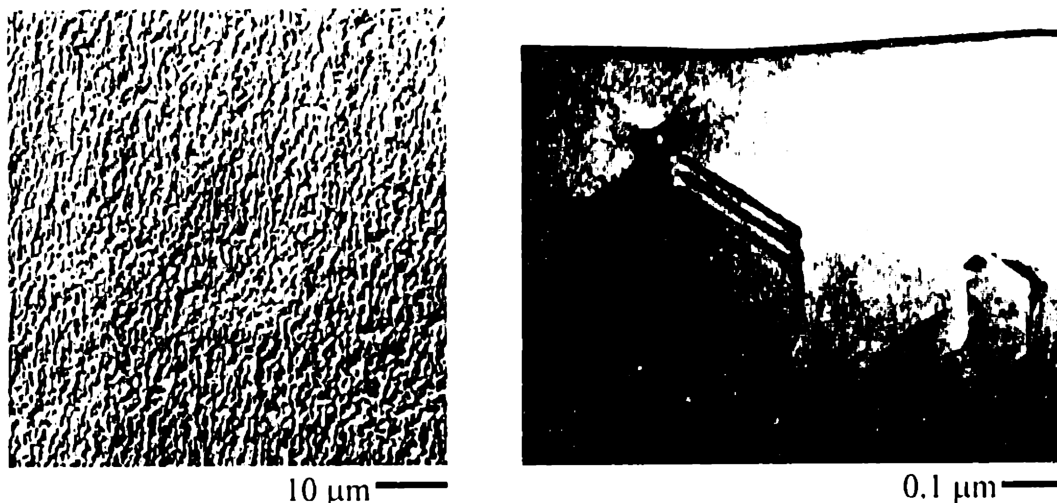


Figure IV-2 *DICM image showing rough surface morphology and XTEM image revealing the presence of APBs in a GaAs/Ge/Ge_xSi_{1-x}/Si film grown without 650 °C annealing.*

can be attributed to the numerous APBs propagating through the film in XTEM Figure IV-2 (left). Figure IV-3 and Figure IV-4 (opposite) feature XTEM, plan-view TEM, and surface DICM of two GaAs/Ge/Ge_xSi_{1-x}/Si films both initially baked at 650 °C, but then nucleated after additional annealing in N_2 at 650 °C (left) and 400 °C (right), respectively. Note the marked absence of APBs and the resultant smooth surface morphology of both films. This suggests that high temperature annealing under AP-MOCVD conditions induces a favorable surface transition equivalent to double-step formation on Ge and Si substrates in ultra-high vacuum MBE systems.

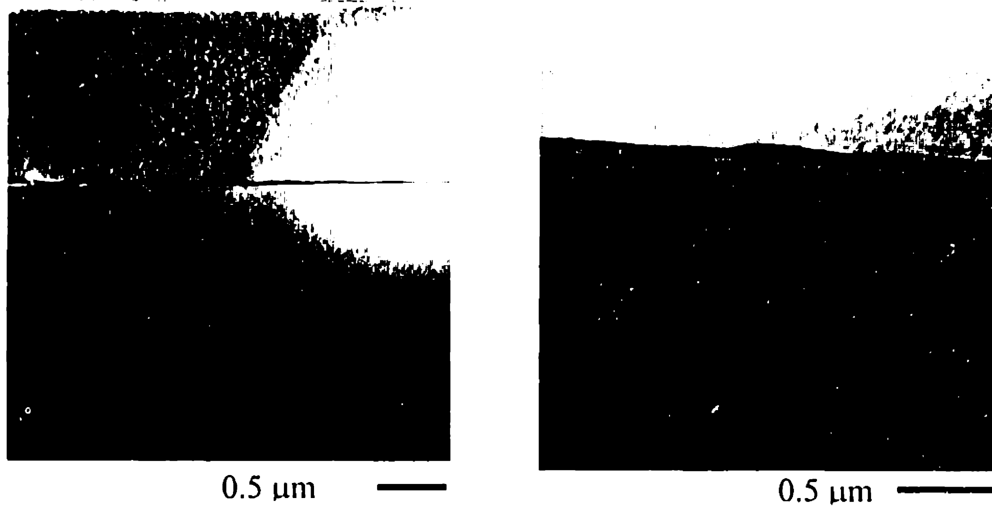


Figure IV-3 *XTEM of GaAs/Ge/Ge_xSi_{1-x}/Si grown at 650 °C (left) and 400 °C (right).*

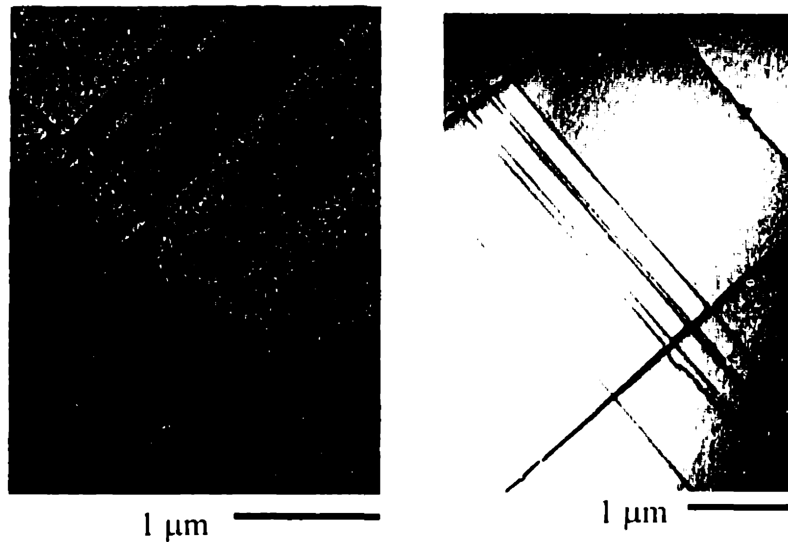


Figure IV-4 *PVTEM of GaAs/Ge/GeSi/Si grown at 650 °C (left) and 400 °C (right).*

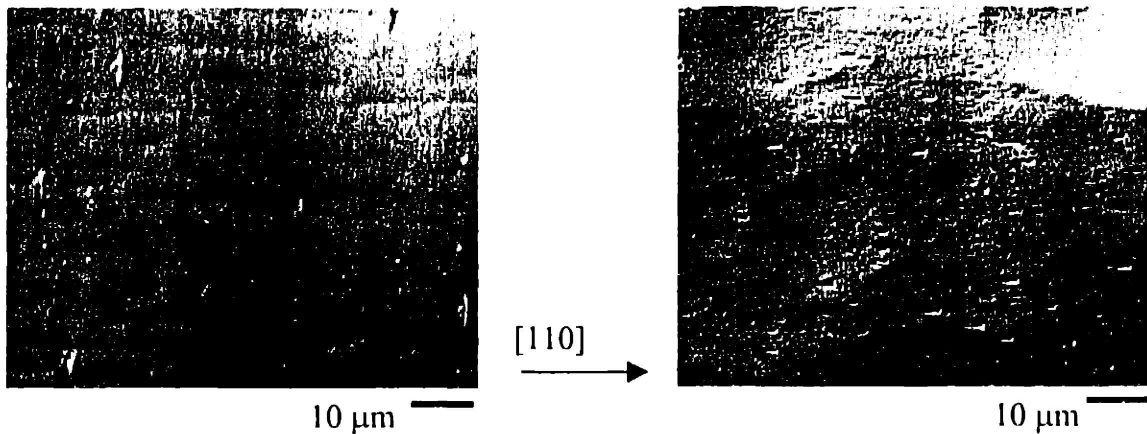


Figure IV-5 *DICM surface morphology images of GaAs/Ge/Ge_xSi_{1-x}/Si grown at 650 °C (left) and 400 °C (right).*

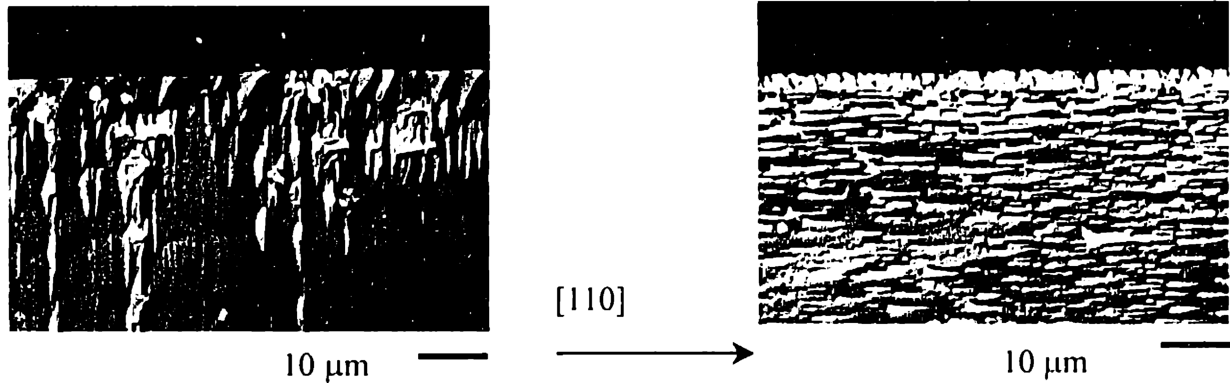


Figure IV-6 *DICM of edge surface morphology showing texture rotation of GaAs films grown at 650 ℃ (left) and 400 ℃ (right).*

GaAs/Ge$_x$Si$_{1-x}$/Si Texture Rotation

Although the 650 °C anneal promotes single domain growth, the pre-nucleation annealing temperature seems to determine the particular GaAs sublattice location. Figure IV-6 shows close-up DIC micrographs from the edges of the same samples featured in Figure IV-5 demonstrating a 90° rotation of GaAs growth hillocks with respect to the [110] offcut direction. Repeated experiments on both GaAs/Ge$_x$Si$_{1-x}$/Si and GaAs/Ge show that high temperature (> 600 °C) pre-nucleation annealing results in a GaAs epilayer texture perpendicular to the substrate offcut, whereas low temperature pre-nucleation annealing (< 500 °C) rotates the texture parallel to the offcut. GaAs/Ge$_x$Si$_{1-x}$/Si and GaAs/Ge films grown after cooling to between 500-600 °C also frequently featureed clouded surface regions of mixed texture indicating the nucleation of both GaAs phases. These morphologies seem consistent with a temperature dependent preference for GaAs sublattice orientation that may be conveniently identified by texture alignment.

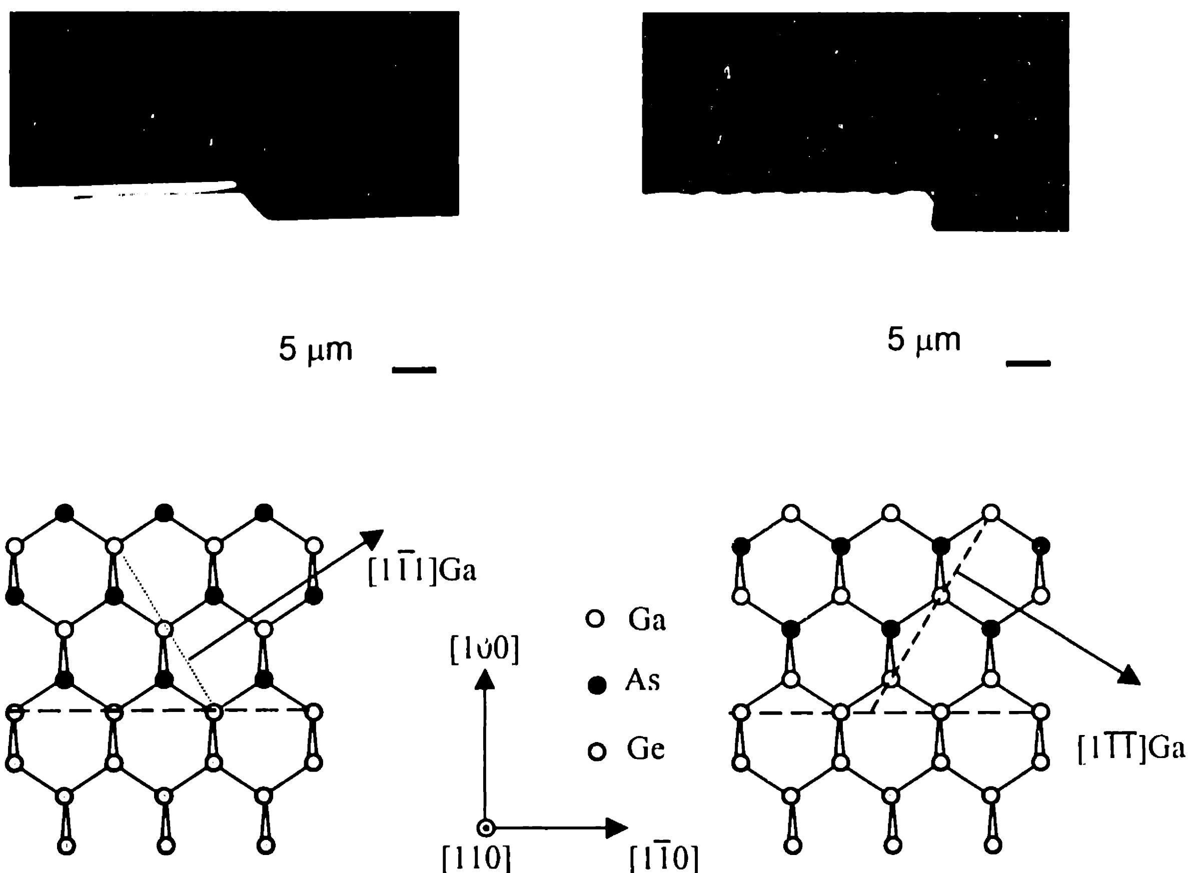


Figure IV-7 *Anisotropic sidewall profiles of 5 μm GaAs/Ge films and the {111}Ga plames revealed by etching in a 1 : 8 : 1 solution of DI H_2O : 30% H_2O_2 : H_2SO_4.*

GaAs/Ge Domain Identification by Anisotropic Sidewall Profile Etching

The same 90° texture rotation with respect to offcut is also observed in MOCVD GaAs/Ge films nucleated under equivalent conditions as demonstrated at Figure IV-7 (top). Anisotropic etching of these 5 μm GaAs/Ge films in 1:8:1 DI H_2O : 30% H_2O_2 : H_2SO_4 establishes the particular sublattice orientation associated with each surface texture. The optical micrographs of Figure IV-7 show cleaved cross-sections of etched sidewalls facing the [1$\bar{1}$0] direction (perpendicular to substrate offcut). Sidewalls of the GaAs-⊥ film have faceted out from the edge of the etch mask, whereas sidewalls of the GaAs-|| film have faceted in, producing an undercut profile. These facets primarily expose the electron-deficient {111}Ga surfaces which are largely responsible for kinetically-limited etch anisotropy.[108] As shown in Figure IV-7 (bottom) the difference in etch profiles reflects a shift of the {111} polar axes relative to substrate offcut, corresponding to a 90° sublatttice rotation.

The GaAs-⊥ etch profile corresponds to exposure of the $(1\bar{1}1)$Ga surface and the GaAs-|| profile corresponds to exposure of the $(1\bar{1}\bar{1})$Ga surface. Etching studies of bulk (001) GaAs in acidic-peroxide solutions have demonstrated similar kinetically-limited profiles for sidewalls facing orthogonal $\langle 110 \rangle$ directions.[109]

From the above discussion, we conclude that the surfaces of Ge and Ge/Ge_xSi_{1-x}/Si substrates are equivalent with respect to the nucleated GaAs sublattice orientation. In reference to the GaAs phases illustrated in Figure II-7 (note the rotation of axes with respect to Figure IV-7), the GaAs-⊥ surface morphology corresponds to the GaAs-A sublattice orientation where $(11\bar{1})$Ga and (111)As planes face the offcut [110] direction and conversely the GaAs-|| surface morphology corresponds to the GaAs-B sublattice orientation where (111)Ga and $(11\bar{1})$As planes face [110]. Furthermore, it seems that the GaAs-A and GaAs-B phases are the dominant high and low temperature sublattice orientations for GaAs on Ge, respectively. In this respect, our results corroborate the earlier findings of Li *et al.*, who similarly reported a domain rotation from GaAs-A nucleated at high temperature to GaAs-B nucleated at low temperatures in MOCVD GaAs/Ge.[72]

Localized Antiphase Disorder

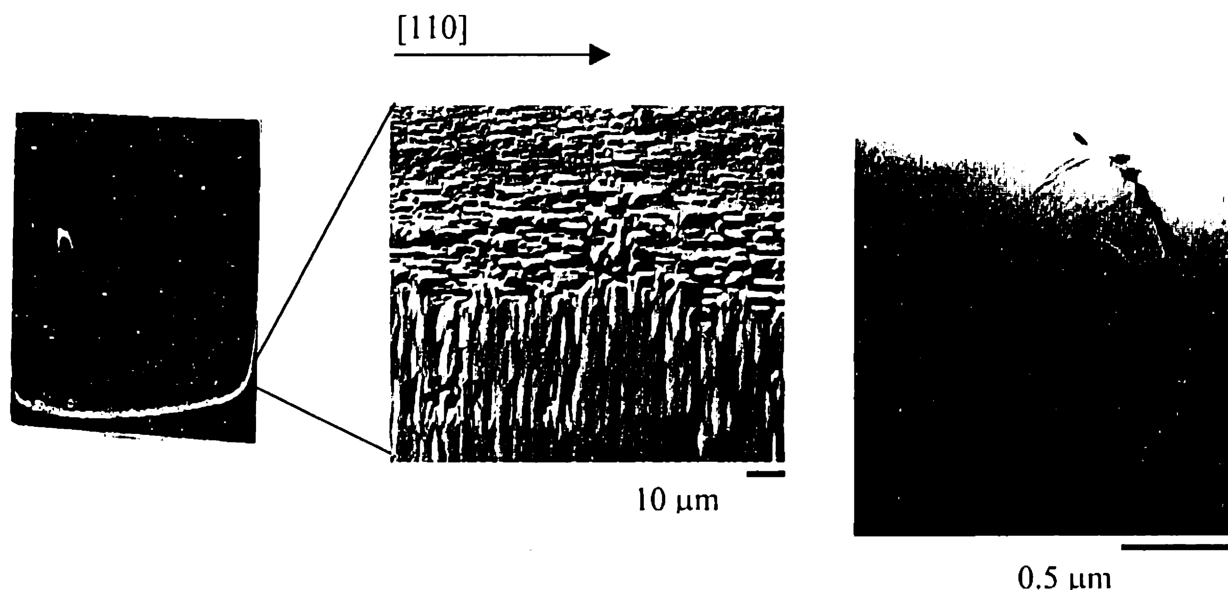


Figure IV-8 *At left, localized antiphase disorder on a GaAs/Ge/Ge_xSi_{1-x}/Si film nucleated at 450 °C after quenching from 650 °C. DICM of the film surface (center) reveals a 90° GaAs texture rotation and numerous antiphase boundaries appear in XTEM (right).*

In many of the GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si films grown at low temperatures (< 500 °C), regions of the GaAs-A phase often appear towards the leading edge of the sample although GaAs-B is the expected majority phase as seen in Figure IV-8, left. Where these two phases intersect, the surface appears clouded to the eye and DICM reveals a narrow band across which the GaAs texture has rotated 90° (Figure IV-8, center) suggesting the appearance of localized antiphase disorder, which is confirmed in XTEM (Figure IV-8, right). Similar rotation bands or clouding of the GaAs surface, indicative of a macrosopic antiphase boundary, were also observed for samples grown between 600-500 °C, though not always as severely localized. In the literature, 90° texture rotations towards the sample periphery have been previously reported in the growth of GaAs/Si and GaAs/Ge films by MBE[83], hydride VPE[110], and MOCVD[37]. Although the bulk of such GaAs films is single domain, material in the vicinity of the localized APB bands is clearly defective, reflecting a recurrent yield problem for device fabrication efforts.

Adding to the conundrum, a few samples nucleated after cooling to 400 °C exhibited not one, but two bands of antiphase disorder, separating three distinct regions of the GaAs film. The sample in Figure IV-9 (next page, top), grown on Ge/Ge_xSi_{1-x}/Si, was nucleated immediately upon cooling to 400 °C with no arsine exposure, whereas the sample in Figure IV-9 (next page, bottom), grown on Ge, was nucleated after an additional 10 minute anneal in arsine at 400 °C. Both samples feature the GaAs-A phase towards the sample periphery, followed by a narrow region of GaAs-B phase between the two bands, but the interior of the sample is again GaAs-A. Strangely enough, in these samples the high temperature phase, GaAs-A, is now actually the majority phase despite low temperature nucleation. Holt *et al.* reported a similar double-banded structure in GaAs/Ge solar cells grown by MOCVD, although the phases of the individual regions were not identified.[37]

Given that GaAs-B is the dominant low temperature GaAs/Ge phase, the localized presence of GaAs-A seems odd. However, it should be noted that the leading edge where it consistently shows up is also the coolest region of the sample where incoming gas first makes contact with the heated susceptor. There, surface transition kinetics are most likely to be limited upon cooling from high temperature. The appearance of residual GaAs-A phase at the leading edge therefore suggests that the temperature-dependent surface transition that normally leads to GaAs-B nucleation elsewhere has been quenched, and that the high temperature preference for GaAs-A has been preserved. Hence a band of localized antiphase disorder delineates the boundary between the two nucleation regimes.

For whatever reasons, the double-banded samples reflect an incomplete transition towards GaAs-B preference. The outer band of antiphase disorder marks the boundary of the quenched edge, as before, and the inner band marks the extent of the transition's completion upon cooling to 400 °C. That GaAs-A can remain the majority phase despite annealing for 10 minutes at 400 °C demonstrates that domain orientation preference is not established during actual nucleation, since the sample temperature should have already equilibrated. Rather, the thermal transients encountered during pre-nucleation thermal cycling. At high temperature, the annealed Ge surface structure somehow develops a preference for GaAs-A nucleation, and at low temperature the preference shifts in favor of GaAs-B nucleation of, but may encounter

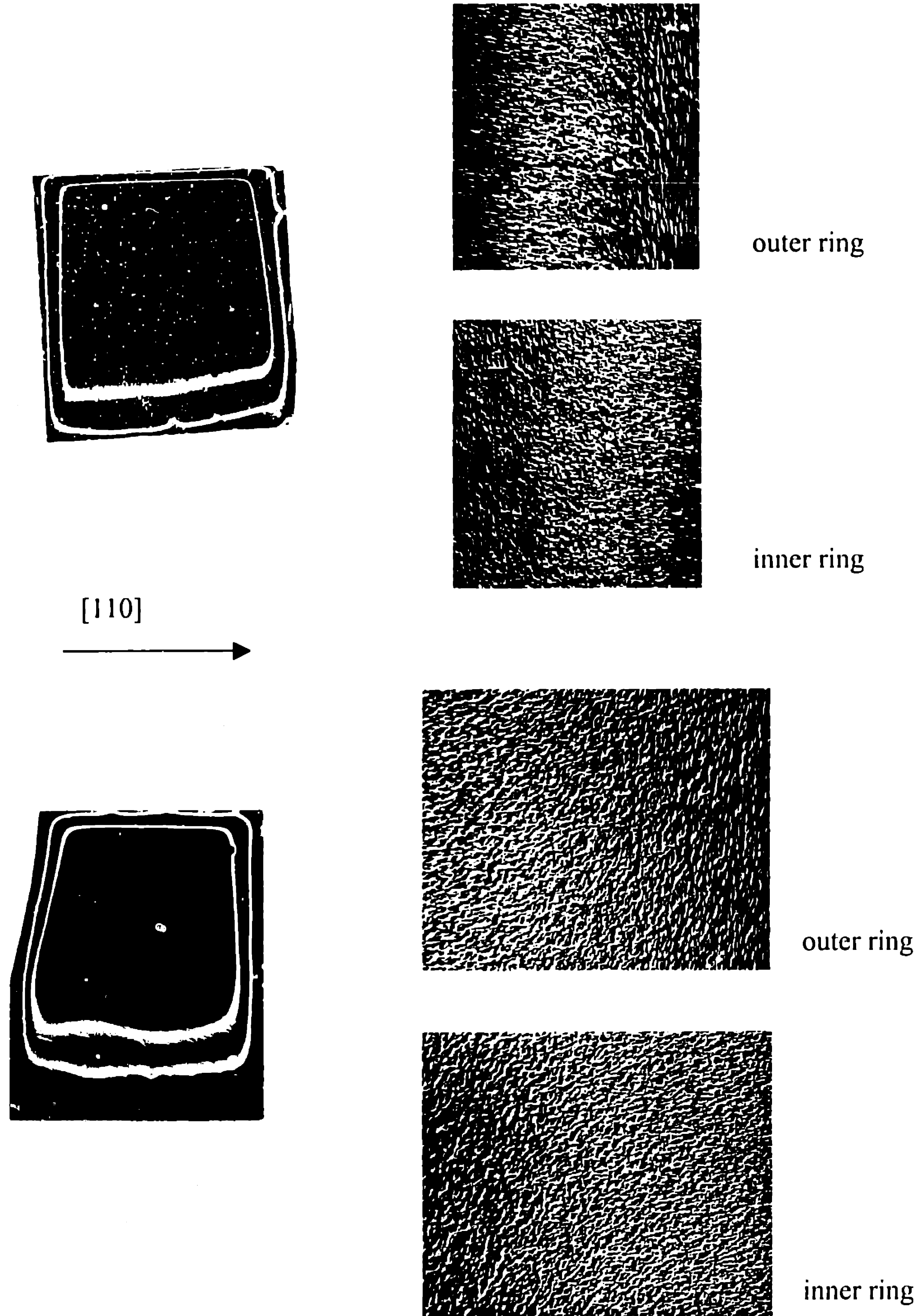


Figure IV-9 *Double banded GaAs/Ge_xSi_{1-x}/Si (top) and GaAs/Ge (bottom) samples. The area bound by both bands is GaAs-B (parallel texture) whereas the sample periphery and interior are GaAs-A (perpendicular texture).*

kinetic limitations.

Although Li *et al.* observed the same GaAs-A to GaAs-B domain rotation on offcut Ge substrates, they attributed this phenomenon to a temperature-dependent change of the GaAs nucleation mode. Assuming that GaAs-A nucleates on surface terraces and that GaAs-B nucleates on surface steps, they concluded that domain rotation is a result of relative intensity of nucleation on steps versus terraces as determined by the nucleation temperature. Unfortunately, no mechanism explaining why step nucleation should differ from terrace nucleation was proposed. Furthermore, our results definitively prove that the GaAs domain rotation occurs as a consequence of a temperature-dependent surface transition that is taking place prior to nucleation.

Suspected Role of Arsenic

At this juncture, the atomistic nature of the temperature dependent GaAs sublattice rotation (henceforth referred to as the A-B phase transition) must be considered. Our samples suggest a transition from one single-domain GaAs orientation to another upon cooling from 650 °C. The clean offcut (001) Ge surface only exhibits one single-domain orientation featuring D_B, never D_A, double-steps. Therefore, we believe another mechanism must be responsible for the A-B transition on both GaAs/Ge and GaAs/Ge_xSi_{1-x}/Si.

Our earlier experiences working solid-source MBE growth of GaAs/Ge suggest a strong correlation between pre-growth arsenic exposure and antiphase order. Therefore, it is not unreasonable to suspect the A-B transition arises due to a background arsenic pressure in our MOCVD reactor. Figure IV-10 shows a plot of the vapor pressure P of arsenic in atm as a function of temperature T calculated from the expression:[111]

$$\log P = \frac{-6950}{T} + 7.92 \tag{4.2}$$

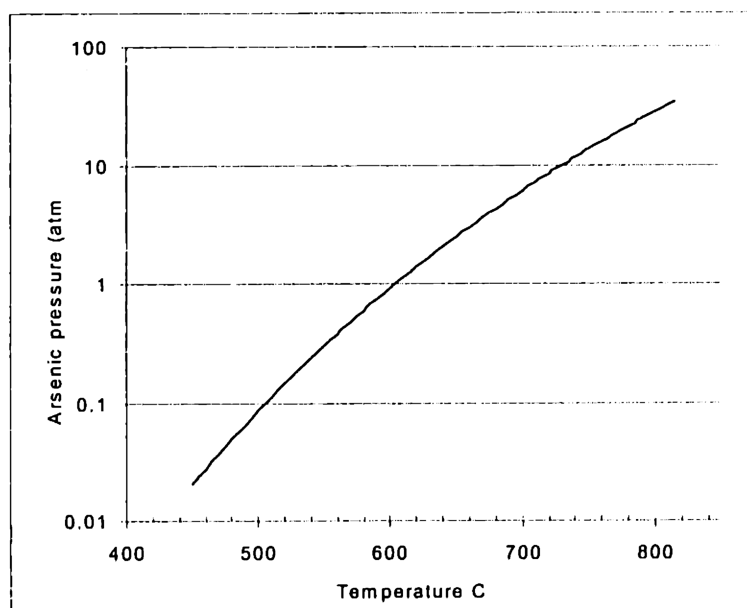


Figure IV-10 *Vapor pressure of solid arsenic as a function of temperature*

Solid arsenic sublimates at 605 °C and arsenic bearing species also readily volatalize from GaAs at elevated temperatures. The 650 °C baking step common to all samples is probably

responsible for significant desorption of arsenic bearing species from the GaAs and arsenic deposit-laden reactor sidewalls and graphite susceptor. Furthermore, upon cooling to the GaAs nucleation temperature, it is likely that this residual arsenic adsorbs onto and interacts with the Ge surface. Although pyrolysis of arsine also results in arsenic coverage, our experiments have demonstrated that the A-B transition initiates even in the absence of arsine during the pre-nucleation thermal cycle.

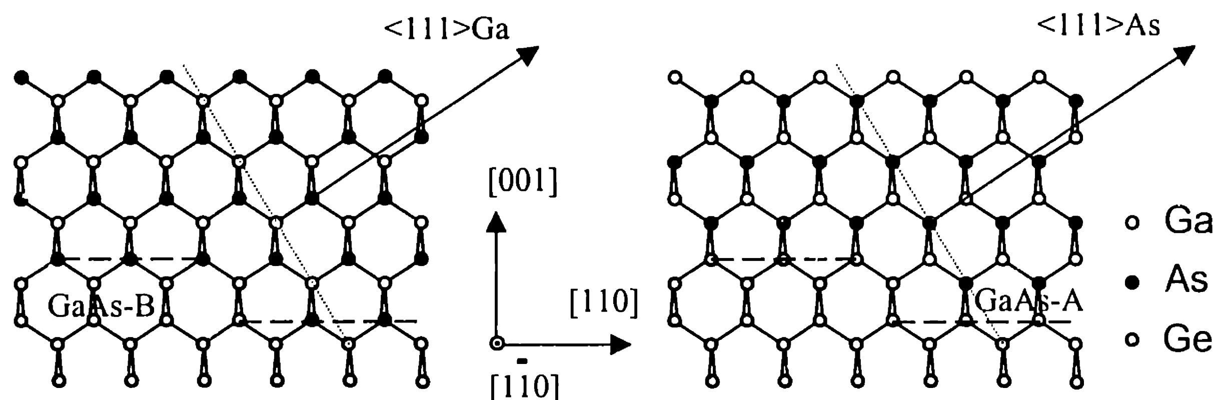
Ge(001):As Domain Rotation?

Lacking the means to evaluate behavior of the As adsorbed Ge surface other than growth and characterization of GaAs films after the fact, our discussion must rely on studies of As-adsorbed Ge and Si (001) surfaces, Ge(001):As and Si(001):As, directly observed under UHV conditions. For these studies to add any meaningful insight, however, the correlation between UHV and AP-MOCVD GaAs growth conditions must first be considered. The most striking demonstration of such a correlation was reported by Kamiya *et al.*, who used reflectance-difference spectroscopy to compare the evolution of GaAs surface structure with temperature under both MOCVD and UHV conditions.[112] By comparing the RDS spectra of GaAs surfaces of a known reconstruction (determined by RHEED) to the RDS spectra of GaAs surfaces under atmospheric conditions, they concluded that local atomic order (dimerization) is equivalent regardless of ambient (UHV, H_2, N_2, or He). Additionally, evidence of long-range order under MOCVD has been reported by Lamelas *et al.*, who observed similarities to UHV GaAs reconstructions by surface x-ray scattering at near atmospheric pressure in H_2 prior to film growth.[113] In light of these results, we believe that Ge:As and Si:As surface reconstructions observed under UHV conditions by RHEED, LEED, or STM are highly relevant to the AP-MOCVD environment.

As discussed earlier in Chapter II, Bringans *et al.* conducted definitive STM studies of the As-adsorbed 4° offcut (001) Si surface which illustrate how As coverage might affect subsequent GaAs nucleation.[74] Starting from a clean double-stepped Si surface with dimer pairs aligned parallel to the step edges, they found that an applied As_4 flux resulted in two possible single-domain configurations of As dimers depending on the initial exposure/adsorption temperature (Figure II-8). In the temperature range between 600-400 °C, As may adsorb by displacing the

Si dimer pairs via a rearrangement of the atomic step structure, forming As dimer pairs in their place, aligned parallel to the step edge ($As_{||}$). This mechanism competes with direct adsorption of arsenic onto unmodified terraces of the original Si surface which instead results in As dimer pairs aligned perpendicular to the step edges ($As_{\perp}$). At temperatures lower than 400 °C, arsenic only adsorbs to the Si surface in the latter additive fashion. Above 600 °C, prior to complete arsenic desorption from the Si surface, the $As_{\perp}$ configuration also dominates. (Note, however, that Becker *et al.*, who first observed temperature dependent As dimer rotation, reported facetting of the (001) Si:As surface in the high temperature regime instead.)[73] Inspection of the LEED pattern during GaAs on Si growth by MBE confirmed that the initial As dimer orientation indeed determines the resultant GaAs sublattice orientation as shown below in Figure IV-11.

Figure IV-11 *Domain rotation due to arsenic dimer rotation. At left, GaAs-B, arsenic displaces the first monolayer of the single-domain Ge surface. At right, GaAs-*



A, arsenic merely adsorbs additively. Compare with Figure II-8. Note also this geometry is rotated 90° from that of Figure IV-7.

Our growth results are well explained in the context of the temperature-dependent As dimer orientation. If the GaAs sublattice orientation is indeed pre-determined by As dimer orientation, the A-B transition corresponds to the temperature-dependent dimer rotation from $As_{\perp}$ to $As_{||}$. Nucleation of GaAs on the Ge:$As_{||}$ surface is equivalent to initiating growth on an initially single-domain Ge surface with a monolayer of Ga, since $As_{||}$ dimers will have displaced the first monolayer of Ge. Conversely, nucleation on the Ge:$As_{\perp}$ surface corresponds to GaAs initiation with a monolayer of arsenic since no modification of the Ge

surface has occurred. Thus Ge:As$_{\parallel}$ leads to GaAs-A growth and Ge:As$_{\perp}$ leads to GaAs-growth.

Kinetics of Ge(001):As Domain Rotation

If our hypothesis is correct, then the appearance of GaAs-A and GaAs-B as high and low temperature majority phases ultimately reflects the thermodynamic and kinetic constraints that define competition between As$_{\parallel}$ and As$_{\perp}$ dimers. Moreover, the occurrence of localized antiphase disorder describes the boundaries between limiting regimes of arsenic adsorption.

Becker *et al.*, the first to observe As$_{\parallel}$ dimerization, suggested it was the thermodynamic minimum energy state of the Si(001):As surface.[73] In support of this hypothesis, Alerhand *et al.* proposed and calculated an energy difference of 0.20 ± 0.02 eV per unit atomic length at each step edge between Si(001):As$_{\parallel}$ and Si(001):As$_{\perp}$ surfaces due to stress relaxation at the step edges.[114] However, Tromp *et al.* directly observed As$_{\parallel}$ incorporation on micron-sized Si terraces with no apparent preference for step-nucleation on <0.5° offcut (001) substrates, by both low energy electron microscopy (LEEM) and STM.[115] Furthermore, they qualitatively described how localized relaxation of intrinsic surface stress might provide the driving force for arsenic displacement. Alternatively, Yu *et al.* proposed a dimer exchange mechanism based on a calculated 0.7 eV gain realized by π-bonding of the Si atoms displaced to the surface by arsenic adatoms.[116]

Thermodynamics notwithstanding, arsenic initially condenses in the As$_{\perp}$ orientation since no displacement of substrate atoms is required. Under conditions that As$_{\parallel}$ incorporation rate is limited with respect to arsenic adsorption, As$_{\perp}$ dimerization can be expected to dominate. In terms of Langmuir adsorption and first-order reaction kinetics, the rates at which As$_{\perp}$ and As$_{\parallel}$ surface coverages Θ_A and Θ_B change with substrate temperature T in a background pressure p^i of i various arsenic species (mostly As_4, some As_2, or perhaps As) may be written:

$$\frac{\partial \Theta_A}{\partial t} = \sum_i C_1^{\,i} \cdot [1-\Theta] \cdot \frac{p^i(T_h)}{\sqrt{2\pi m^i kT}} \cdot \exp\left\{\frac{-\Delta G^{i}{}_A^{ads}}{kT}\right\} - C_2^{\,i} \cdot \Theta_A \cdot \exp\left\{\frac{-\Delta G^{i}{}_A^{des}}{kT}\right\} - \frac{\partial \Theta_B}{\partial t} \quad (4.3)$$

$$\frac{\partial \Theta_B}{\partial t} = C_3 \cdot [1-\Theta] \cdot \Theta_A \exp\left\{\frac{-\Delta G_{A-B}}{kT}\right\} - C_4 \cdot [1-\Theta] \cdot \Theta_B \cdot \exp\left\{\frac{-\Delta G_{B-A}}{kT}\right\} \quad (4.4)$$

where the $C_{1\text{-}4}$ are rate constants, m^i is the mass of each arsenic species, k is Boltzmann's constant, $\Delta G^i{}_A{}^{ads}$ and $\Delta G^i{}_A{}^{des}$ are respectively the activation barriers to adsorption and desorption of $As_\perp$, $\Delta G_{A\text{-}B}$ and $\Delta G_{B\text{-}A}$ are respectively the activation barriers for the forward and reverse $As_{||}$ incorporation reactions, and:

$$\Theta = \Theta_A + \Theta_B \quad (4.5)$$

equals the total arsenic coverage site fraction such that a factor of $[1\text{-}\Theta]$ represents the fraction of dimer sites unoccupied by arsenic. Note also that the p^i are dependent on the background temperature T_b as they represent a desorption arsenic flux from the reactor walls and susceptor. Hence, from left-to-right, the terms on the right-hand-side of equation 4.3, represent the rate of $As_\perp$ adsorption from the vapor minus the rates of desorption and $As_{||}$ incorporation. Equation 4.4 expresses the total rate of $As_{||}$ dimerization as a sum of forward and reverse rates of conversion from $As_\perp$ dimerization.

In the high temperature limit, it is conceivable that the rate of $As_\perp$desorption is much greater than the $As_\perp$-$As_{||}$ transition rate or that the reverse transition reaction may be thermally-activated. As a result the substrate surface remains essentially un-modified before GaAs nucleation despite the background arsenic flux. This accounts for the appearance of GaAs-A as the high temperature (> 600 °C) majority phase in our samples.

As the substrate temperature decreases, though, the ratio of adsorbed As to desorbed As increases such that, at a transition temperature T_{trans}, the average residence time of an $As_\perp$ dimer equals the incubation time τ_{inc} required for exchange with a Ge dimer. Below T_{trans} then, $As_{||}$ dimerization becomes dominant resulting in GaAs-B as the low temperature (< 600 °C) majority phase.

However, a low temperature limit (< 500 °C) to $As_{||}$ incorporation may be posed by rapid arsenic adsorption. At some quenching temperature T_{quench}, the time required to condense a single $As_\perp$ dimer equals τ_{inc}. Further drop in substrate temperature quenches $As_{||}$

incorporation altogether with respect to $As_{\perp}$ adsorption, allowing residual nucleation of GaAs-A (note, the phase regularly achieved by 350 °C As_2 exposure during our MBE study). Additionally, pre-nucleation arsine exposure below the desorption limit may lock in the $As_{\perp}$ orientation by suddenly raising the effective arsenic flux and saturating all available surface sites. In a similar manner, low temperature may also curb the A-B transition by decreasing the mobility of displaced Ge atoms. If prevented from successfully diffusing to an adjacent step edge, Ge atoms may effectively block further $As_{\parallel}$ incorporation by occupying terrace sites. Therefore, the high step density afforded by an offcut substrate remains desirable whether or not the $As_{\parallel}$ dimerization mechanism involves step nucleation.

The T-T-T (time-temperature-transformation) diagram in Figure IV-12 illustrates different kinetically limited regimes of Ge(001):As dimerization that are encountered upon cooling linearly in an arsenic background pressure. For the sake of simplicity, a constant background arsenic flux and a constant dimer exchange rate between T_{trans} and T_{quench} have been assumed.

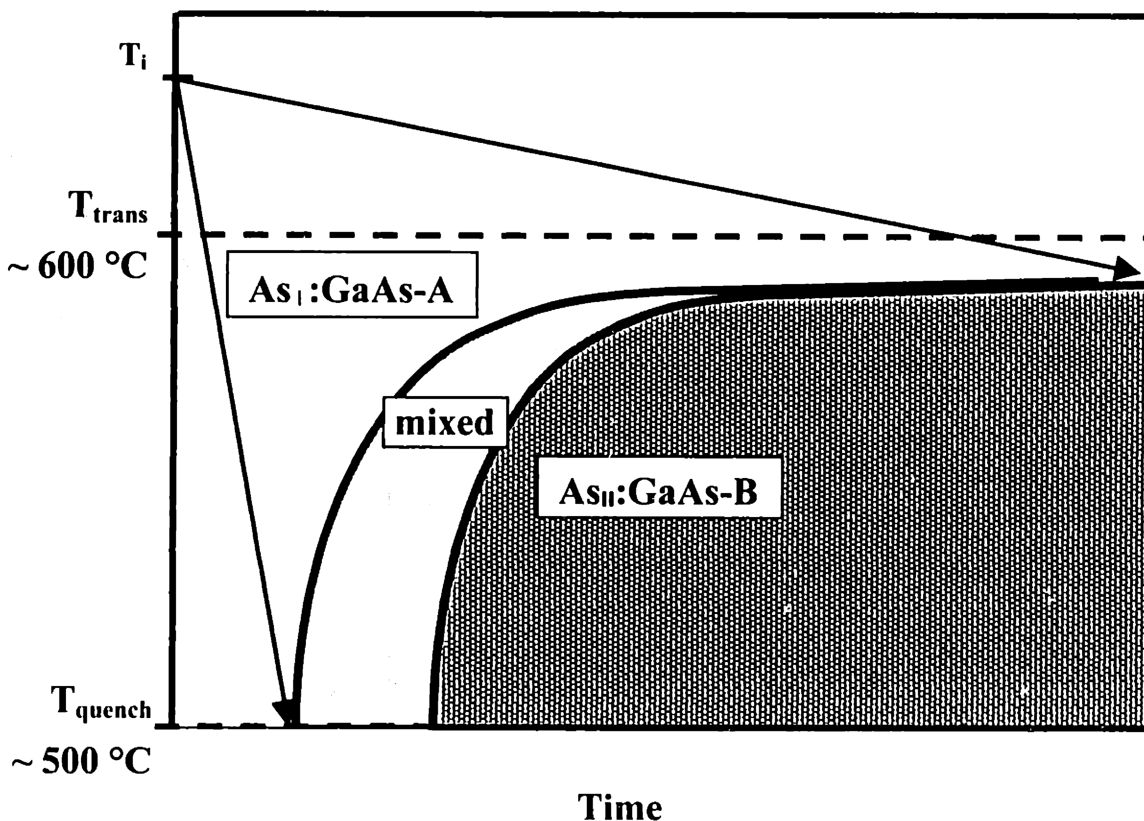


Figure IV-12 *T-T-T diagram for Ge(001):As dimerization and GaAs sublattice determination thereby.*

At T_i the sample is assumed to be single-domain and arsenic desorbed such that no arsenic-induced modification of the surface is possible. As the sample cools through T_{trans} and into the A-B transition region between T_{trans} and T_{quench}, net arsenic adsorption occurs and the dimer orientation will be determined by the cooling rate. At the slowest cooling rate, the net arsenic dimer exchange rate is comparable to net arsenic adsorption and the Ge surface can reach complete $As_{\parallel}$ incorporation. In terms of equations 4.3-4.5 the condition:

$$\frac{\partial \Theta_B}{\partial t} \approx \frac{\partial \Theta_A}{\partial t} \tag{4.6}$$

is maintained until $\Theta = \Theta_B = 1$. At the highest cooling rate, the initially desorbed Ge surface becomes suddenly $As_{\perp}$ adsorbed such that the condition:

$$\frac{\partial \Theta_A}{\partial t} >> \frac{\partial \Theta_B}{\partial t} \tag{4.7}$$

quickly dominates over that of expression 4.6, quenching arsenic dimer exchange such that $\Theta = \Theta_A = 1$ and GaAs-A is nucleated. Mixed dimerization may occur between these extremes as the two adsorption mechansims compete resulting in antiphase disorder.

Spatial Distribution of Localized Antiphase Disorder

The distribution of localized antiphase disorder is ultimately determined by the relative temporal and spatial evolution of T_{trans} and T_{quench} isotherms on the sample surface upon cooling; see Figure IV-13, (opposite). These isotherms are in turn set by the thermal boundary conditions imposed by the carrier gas flow and the relative positions and geometries of the substrate, susceptor, and horizontal reactor tube. In the high temperature desorption limit, both isotherms are effectively pinned together by the sharp thermal gradient at the edges of the sample. Upon cooling, the T_{trans} isotherm separates and sweeps inwards across the sample surface. However, the T_{quench} isotherm leaves the leading edge shortly thereafter, following the path of the T_{trans} isotherm as it contracts and collapses inwards towards the trailing edge of the sample.

Clearly, the T_{quench} boundary condition at the sample edge favors $As_{\perp}$, explaining the tendency towards GaAs-A nucleation there. Away from the sample periphery however, the thermal gradient imposed by the carrier gas stream is less severe, and once the T_{trans} isotherm unpins from the edge and contracts inwards, dimer exchange becomes possible. Thus, $As_{\parallel}$ first nucleates in a narrow ring somewhat inside the sample edge and as the T_{trans} isotherm further contracts, a continuous region of $As_{\parallel}$ forms within the interior where GaAs-B may subsequently nucleate as illustrated in the upper sample shown in Figure IV-13 (opposite).

The above scenario explains the commonly observed single band of antiphase disorder that separates GaAs-B in the sample interior from GaAs-A towards the edge. The double-banded samples featured in Figure IV-9 might arise if GaAs nucleation occurs before the T_{trans} isotherm completely contracts. If such is the case, then the inner band and outer bands of antiphase disorder reflect the actual positions of the T_{trans} and T_{quench} isotherms, respectively, at the moment of GaAs nucleation. However, it seems rather unlikely that any part of the sample should be above T_{trans} at a sample temperature of 400 °C, especially after prolonged annealing.

A more likely explanation for the second, inner band is that rapid, non-linear heat loss from the susceptor (commonly observed in our reactor), accelerates contraction of the T_{quench}

isotherm relative to the T_{trans} isotherm. If the motion of the T_{quench} isotherm does not sufficiently lag that of the T_{trans} isotherm, then regions of the sample which were previously desorption-limited abruptly find themselves adsorption-limited instead, without significant $As_{||}$ incorporation. Thus, whereas the initial separation of the T_{trans} isotherm from the sample edge might nucleate a ring of $As_{||}$ dimerization, the sudden unpinning and acceleration of the T_{quench} isotherm could prevent further $As_{||}$ incorporation in the sample interior as seen in the lower sample in Figure IV-13.

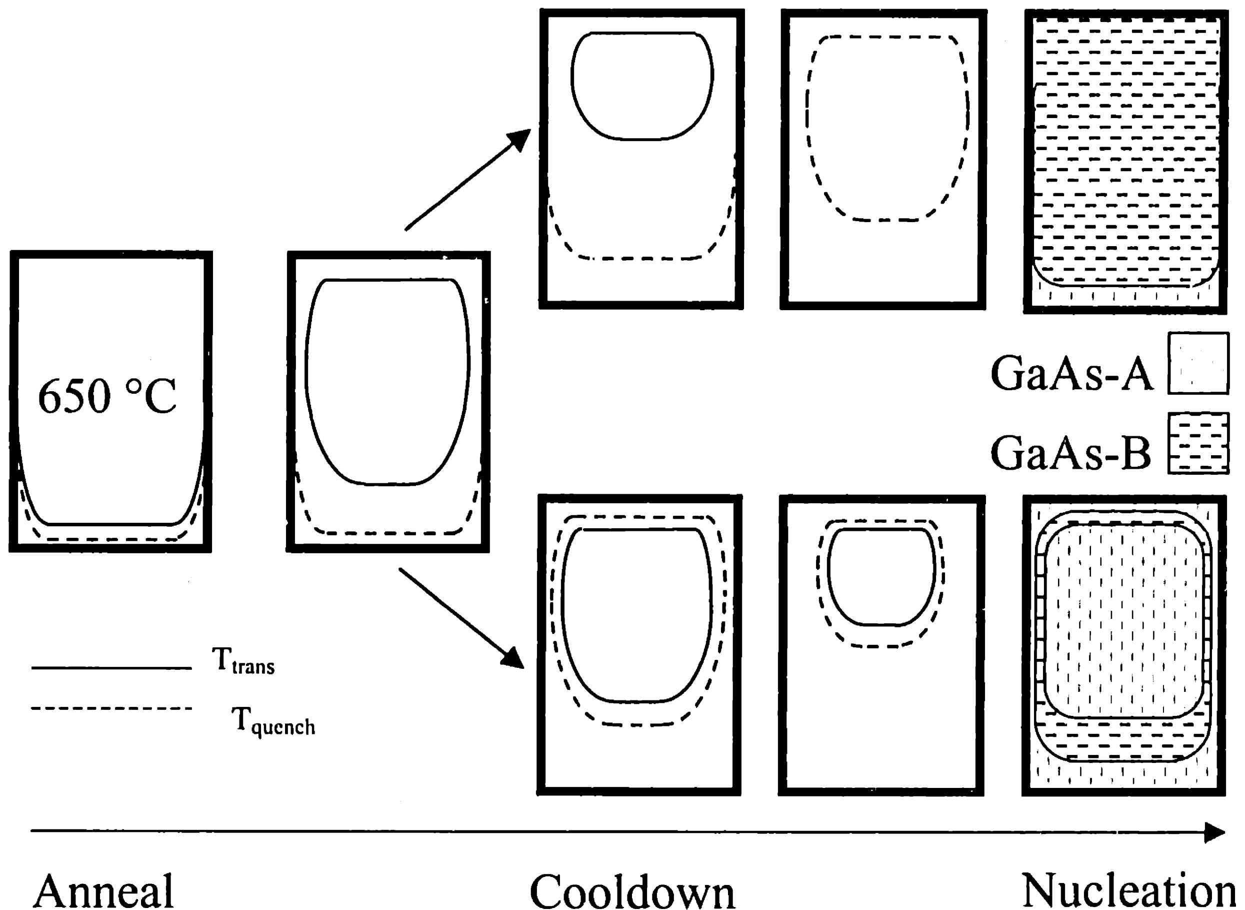


Figure IV-13 *Spatial and temporal evolution of T_{trans} (solid) and T_{quench} (dashed) upon cooling through the A-B transition and the resultant spatial distribution of GaAs/Ge domain orientation.*

Based on the above discussion, it is apparent that completion of the A-B transition across the entire substrate demands both controlled cooling of the susceptor to minimize formation of quenched regions. In practice, single-domain GaAs-B growth was usually obtainable

regardless of ambient environment by cooling through 600-500 °C in approximately 2 minutes, then annealing at 500-400 °C prior to GaAs nucleation. Since the thermal gradients imposed by the carrier gas are always present, though, some residual GaAs-A nucleation may be expected towards the edges. Nevertheless, low temperature nucleation may prove advantageous for certain device applications in order to limit interdiffusion at the GaAs/Ge interface. Nucleation at high temperatures may cause unintentional doping of both the Ge substrate and GaAs film resulting in an un-wanted p-n junction. When interdiffusion effects are not a concern though, the problem of antiphase disorder may be avoided altogether by nucleating single-domain GaAs-A above the transition regime (> 600 °C).

Plausibility of (001)Ge:As Domain Rotation

Much of our argument hinges on establishing a common link between the behavior of offcut Ge(001):As and Si(001):As surfaces. Unfortunately, relatively few detailed studies of Ge(001):As surfaces are to be found in the literature, reflecting the recent development of technological interest in GaAs/Ge heteroepitaxy. Moreover, the task is complicated by confusion regarding arsenic adsorbed Si and Ge surfaces in general, with various authors reporting seemingly contradictory data. Fortunately in the case of Si(001):As, Bringans was able to resolve many apparent contradictions by noting that As dimer orientation depends on the timing of arsenic exposure with respect to the substrate annealing sequence, in addition to the actual values of the As_4 flux and the exposure temperature. We suspect that Ge:As ordering is likewise sensitive to the particulars of arsenic exposure conditions, which must be carefully weighed when drawing comparisons between the various studies.

In two separate studies, Pukite and Cohen used RHEED to examine arsenic adsorption on 1000Å Ge[57] films (grown on 2° and 6° offcut (001) GaAs substrates) and on 2.5° offcut (001) Si[76] substrates. Starting with single-stepped, two-domain Ge and Si surfaces (obtained after annealing at 500 °C and 900 °C, respectively) a reversible transition involving major step reorganization was observed upon application of an arsenic flux. The resulting two-domain Ge:As and Si:As step structures were strikingly similar, both featuring a four-layer periodicity, suggesting the possible formation of alternating single and triple steps. In addition, formation of a metastable single-layer Si:As structure was observed at temperatures

below 650 °C, indicating kinetically-limited step rearrangement. Despite the lack of any pre-existing single-domain step structure, single-domain GaAs growth of both sublattice orientations was achieved by subsequent MBE and attributed to preferential nucleation and overgrowth of one domain versus the other at different steps. Lack of single-domain ordering prior to arsenic exposure makes comparison with Bringans' findings difficult, nonetheless a common theme is apparent. Each study features reordering of initial step structure upon arsenic exposure requiring considerable migration of substrate atoms which may become kinetically limited. Moreover, the re-ordering process itself and/or the extent of its completion somehow determines the ultimate GaAs sublattice orientation.

More recent work by Gan *et al.* has investigated the step structure evolution of annealed 9° offcut Ge(001):As surfaces.[79,80] Ge:As surfaces were prepared by exposure to tertiarybutylarsine in an MOCVD reactor at 650 °C followed by cooling to room temperature, then transferred and annealed under UHV for characterization by LEED and STEM. Unfortunately, Gan's experiments neglect evolution of the Ge:As surface during the initial cooling cycle. This immediately complicates direct comparison with our study, which suggests that cooling from 650 °C in the presence of arsenic results in significant modification of the original surface structure with considerable spatial variation from sample to sample. Nevertheless, Gan's report of a single-domain Ge surface ordering after complete arsenic desorption at 600 °C corroborates our assumption of such a surface prior to arsenic adsorption. Also, their observation of two-domain Ge:As ordering for samples annealed at 410-480 °C is consistent with competition between $As_{\parallel}$ and $As_{\perp}$ dimer formation during the cooling cycle.

Overall, we find it reasonable to suspect that cooling the Ge surface in a background arsenic pressure is responsible for the A-B transition observed in our MOCVD reactor. Although there exists no definitive Ge:As study which allows a one-to-one comparison with Bringans' results, at the very least, it is very reasonable to expect temperature dependent Ge:As ordering which affects the GaAs sublattice orientation. Furthermore, the correlation between antiphase disorder and As_2 exposure at 500 °C during our study MBE GaAs/Ge growth is consistent with our A-B transition. In a broader sense, regardless of the actual atomistic mechanism that

determines GaAs sublattice orientation, our findings are consistent with an A-B transition that features high and low temperature kinetic limits.

Conclusions

We have demonstrated the APB-free growth of GaAs on Ge and Ge/Ge_xSi_{1-x}/Si by AP-MOCVD and have conducted an investigation into the nature of GaAs domain rotations. Single domain GaAs growth is achieved at high (GaAs-A > 600 °C) and low (GaAs-B < 500 °C) temperatures, but domain orientations are rotated 90° with respect to one another. A Ge surface transition occurs between 500-600 °C, regardless of ambient, which determines the domain orientation of subsequently nucleated GaAs. Corroborating our MBE sudy, it is strongly suspected that a background arsenic pressure in the reactor is responsible for arsenic adsorption on the Ge surface, and that competition between arsenic dimerization mechansims leading to the observed temperature domain rotation.

Chapter V

Measurement of GaAs/Ge/Ge_xSi_{1-x}/Si Threading Dislocation Density and Diode Fabrication

Threading Dislocation Density Characterization

To differentiate between those defect-engineering approaches that are useful as opposed to useless, accurate TDD characterization is imperative. This implies the ability to examine material on a scale representative of the overall defect morphology while maintaining sufficient sensitivity and resolution to distinguish individual threading dislocations.

Unfortunately, high resolution inspection typically implies characterization at a diminished scale. XTEM, for example, is a poor choice for TDD measurements despite possessing the resolution and sensitivity adequate to directly image the diffraction contrast of individual dislocations. The volume of sampled material in a typical XTEM sample is so minimal that for TDD on the scale of 10^6 /cm^2, the chances of observing a thread and the statistical relevance of each field-of-view are basically negligible.

TDD characterization by etch pit density (EPD) lies at the opposite end of spectrum, allowing wafer-scale characterization at the price of resolution and perhaps sensitivity for particular chemistries. Molten KOH, for example, is one of the most commonly used etchants for characterizing the low TDD of bulk GaAs wafers. However, it has been observed that the size of KOH etch pits themselves can limit the resolution of closely spaced dislocations, such that the discrepancies between actual TDD and measured EPD increases with actual TDD.[117] As revealed by Ishida *et al.*, KOH EPD values are essentially useless for the characterization of GaAs/Si with TDD on the order of 10^8 /cm^2.[118]

Lying between these extremes, are techniques such as plan-view TEM, cathodoluminescence (CL) and electron-beam induced current (EBIC) imaging. PVTEM features the same resolution and sensitivity of XTEM while sampling more volume per image, usually on the scale of 10,000X. CL and EBIC relies on the efficient recombination of excess carriers generated by an electron beam to image dislocations as dark spots. Maps of CL and EBIC intensity taken in scanning electron microscope (SEM) allow characterization on the order of 1000X. The sensitivity and resolution of CL and EBIC are a function of materials system and determined respectively by the rates of non-radiative recombination and minority carrier lifetime degradation induced by individual threading dislocations.

Characterization of GaAs/Ge$_x$Si$_{1-x}$/Si TDD

Cathodoluminescence

Our first attempts at TDD characterization relied upon CL mapping in a JEOL JSM-6400 SEM equipped with an Oxford Instruments CL attachment and North Coast EO-817L Ge p-i-n photodetector tube. Typical CL spectrum for APB-free GaAs/Ge grown by MBE and GaAs/Ge$_x$Si$_{1-x}$/Si by MOCVD are shown in Figure V-1. The full-width at half maximum (FWHM) of both peaks is approximately 28 nm, suggesting roughly equivalent crystalline quality.

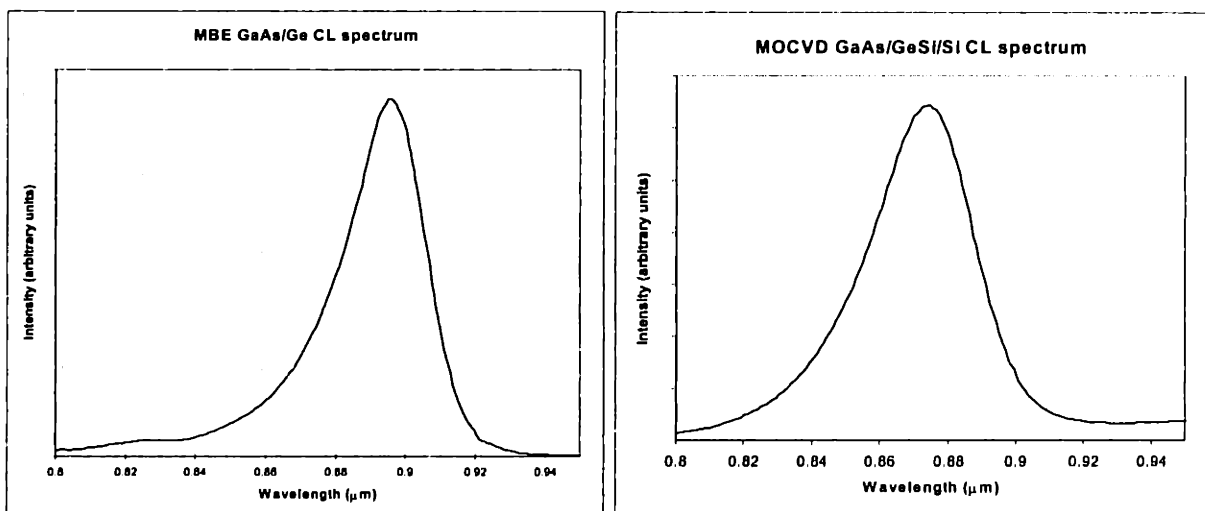


Figure V-1 *Cathodoluminescence spectra of GaAs/Ge and GaAs/Ge/GeSi/Si samples grown by MBE and MOCVD respectively. Both feature a FWHM of ~28 nm.*

The representative CL images of similar 2µm highly doped GaAs/Ge and GaAs/Ge/Ge$_x$Si$_{1-x}$/Si films shown in Figure V-2 were generated by mapping out the CL intensity at the peak emission wavelength as a function of 15kV electron beam position. Although there is sufficient resolution and contrast to image some dark spots, in general the distribution of different sizes makes it difficult to identify them as individual threading dislocations. Despite efforts to improve this resolution and contrast by growing different GaAs structures, it is likely that the Ge detector which operates at only one-third of its peak response at 900 nm, was the ultimate limiting factor.

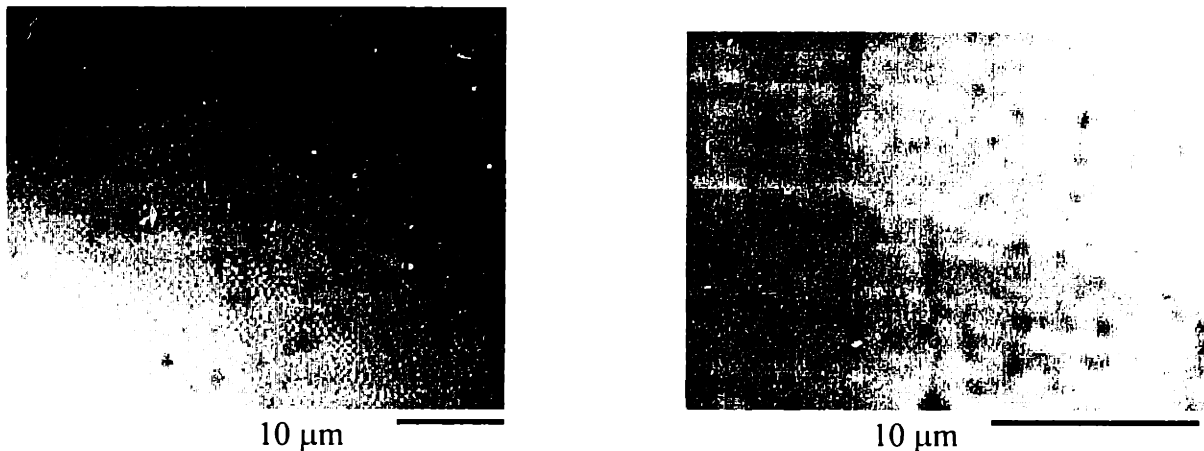


Figure V-2 *Cathodoluminescence maps of GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si films.*

Etch Hillock Density

The defect revealing properties of light-assisted HF-CrO_3 based solutions for n-type GaAs have been studied in depth by Weyher *et al.*[119,120] Often referred to as the $D_{1:x}S_{a/b}L$ etch, where *x* is the dilution D of *a* parts HF to *b* parts 33 wt. % aqueous CrO_3 solution S in DI H_20, and L denotes the use of light. Localized recombination of photo-generated carriers at defects apparently retards etching such that hillocks, rather than the usual pits, indicate the presence of threading dislocations.

The particular solution chosen for our study, $D_{1:8}S_{1/2}L$ is ideal for shallow defect-revealing of thin epitaxial GaAs layers. To explore this option, 2 μm GaAs films, Si doped to nominally 10^{18} /cm^3, were grown by MOCVD on Ge/Ge_xSi_{1-x}/Si substrate pieces of known TDD and a Ge control substrate, all (001) offcut 6° to [110]. Three minutes of etching under illumination from an ordinary halogen lamp removed approximately 0.5μm of the GaAs film for etch hillock density (EHD) measurements.

Figure V-3 shows a DICM image of a $D_{1:8}S_{1/2}L$ etched GaAs/Ge/Ge_xSi_{1-x}/Si film revealing an EHD of approximately 2.1 x 10^6 /cm^2. For comparison, an otherwise identically grown GaAs film on a Ge substrate is shown after the same etch. Only a few threading dislocations are evident in the field of view making an accurate EHD estimate difficult. At best, an upper bound of < 10^4 /cm^2 seems appropriate, consistent with Eagle-Picher's quoted TDD value of

< 5000 /cm^2. Clearly, GaAs growth on Ge or Ge/Ge$_x$Si$_{1-x}$/Si, by itself, results in minimal nucleation of additional threading dislocations.

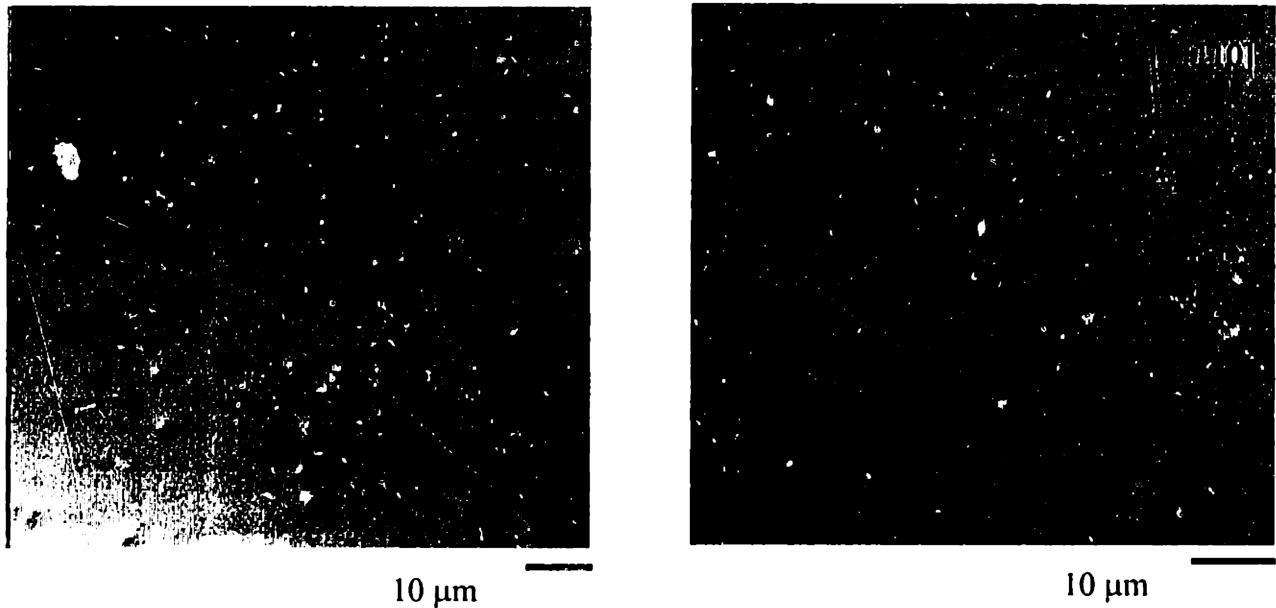


Figure V-3 *Typi l morphologies of MOCVD GaAs/Ge/Ge$_x$Si$_{1-x}$/Si and GaAs/Ge films after 3 minutes $D_{1:8}S_{1/2}L$ etching. Note the nearly orthogonal crosshatch pattern revealed on the GaAs/Ge film; the [110] offcut direction lies along the set of intersecting crosshatch lines.*

Note the distinct crosshatch pattern revealed by etching the GaAs/Ge film, indicative of misfit dislocations at the mismatched interface. The offcut [110] direction is clearly visible as is considerable strain relaxation asymmetry. Surface crosshatch features are not as distinct on the GaAs/Ge/Ge$_x$Si$_{1-x}$/Si sample perhaps due to the higher TDD or by the surface morphology of the Ge/Ge$_x$Si$_{1-x}$/Si substrate.

TEM

To confirm that our EHD measurements were reasonable for estimating TDD, TEM samples were prepared by argon ion milling and examined using a JEOL 2000FX microscope operated at 200kV. Figure V-4 shows an XTEM image of the as-etched $GaAs/Ge/Ge_xSi_{1-x}/Si$ film. The GaAs/Ge interface is free of antiphase disorder, and the only dislocations in evidence are strain relieving misfit segments at the lattice mismatched interface and the dislocation network of the graded Ge_xSi_{1-x} buffer below the Ge cap layer.

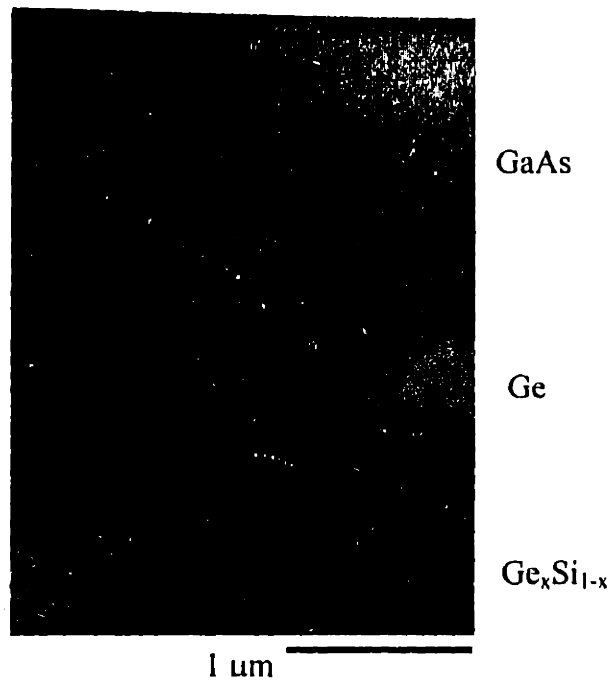


Figure V-4 *XTEM image of an as-etched $GaAs/Ge/Ge_xSi_{1-x}/Si$ sample.*

Threading dislocations directly imaged by PVTEM ere counted over twenty-five 10,000X fields of view, totaling an area of ~1600 μm^2, and the TDD was estimated at 3.7 x 10^6 /cm^2.

Figure V-5 features two representative PVTEM micrographs used for dislocation counting purposes. The slight discrepancy between EHD and PVTEM TDD estimates, which lies within a factor of ~2, is likely due to the resolution limit of the $D_{1:8}S_{1/2}L$ etch. It is unlikely that etching is capable of distinguishing closely paired dislocations from single threading dislocations. By comparison, no threading dislocations were observed by plan-view TEM in the GaAs/Ge control sample, indicative of the very low TDD.

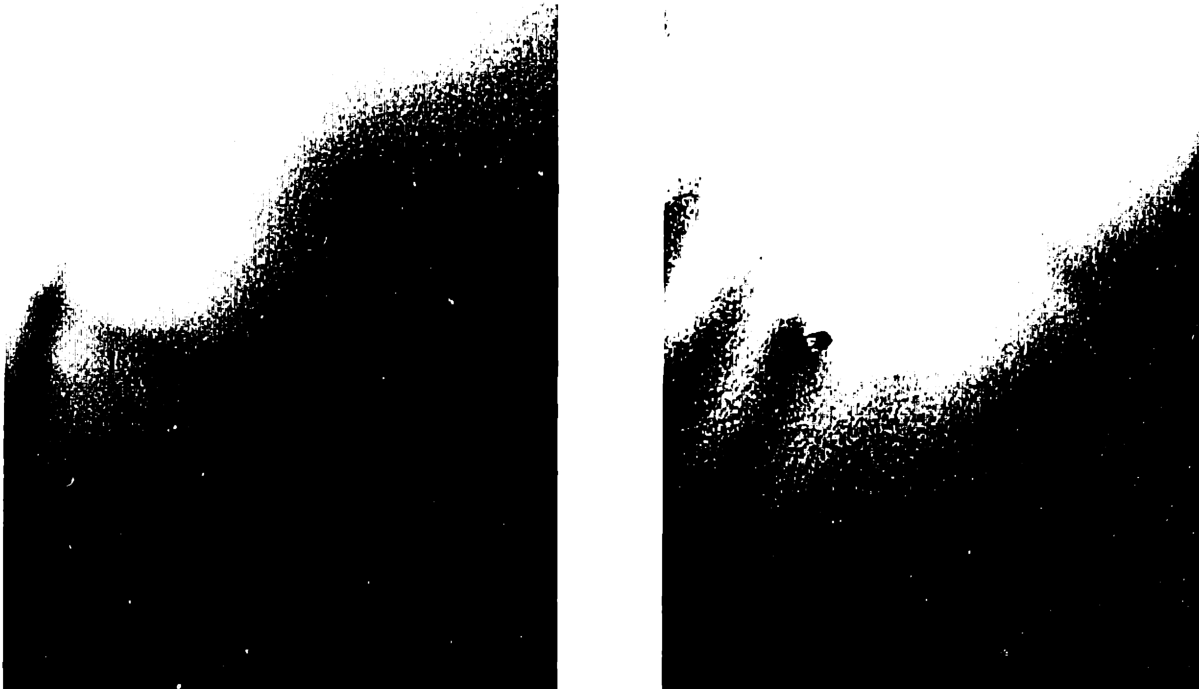


Figure V-5 *PVTEM images of GaAs/Ge/Ge_xSi_{1-x}/Si. At right the single threading dislocation is likely to be adequately resolved by $D_{1:8}S_{1/2}L$ etching, whereas the closely paired threads at left are unlikely to be distinguished from one another.*

Our results demonstrate that the TDD of GaAs/Ge/Ge_xSi_{1-x}/Si films is primarily limited by the TDD of the Ge/Ge_xSi_{1-x}/Si substrate. The correlation between $D_{1:8}S_{1/2}L$ etching and PVTEM measurements allows us to establish lower and upper limits, respectively, on the TDD. With further optimization of Ge_xSi_{1-x} graded buffer growth, we expect a commensurate decrease in the TDD of GaAs epilayers.

Table V-1 summarizes the TDD characterization results. The quoted TDD of Ge substrates obtained from Eagle-Picher industries was $< 5000/cm^2$ and the Ge/Ge_xSi_{1-x}/Si UHVCVD

grown substrates featured EPD between 2-4 x 10^6 /cm^2, and PVTEM TDD counts between 4-6 x 10^6 /cm^2.

Table V-1 *TDDs of GaAs/Ge and GaAs/Ge/Ge_xSi_{1-x}/Si films and their substrates*

Sample	Substrate TDD (/cm^2)	TDD- EHD (/cm^2)	TDD- PVTEM (/cm^2)
GaAs/Ge	< 5,000	< 10,000	?
GaAs/UHV23	2 x 10^6	2 x 10^6	4 x 10^6
GaAs/UHV115	4 x 10^6	4 x 10^6	6 x 10^6

GaAs/Ge/Ge_xSi_{1-x}/Si Diode Fabrication and Testing

To demonstrate of the viability of monolithic III-V device integration through Ge_xSi_{1-x} buffers, a comparison set of GaAs diodes was fabricated on on-axis (001) GaAs and 6° offcut (001) Ge/Ge_xSi_{1-x}/Si. The measured TDD of the GaAs (by $D_{1:8}S_{1/2}L$ etching) and Ge/Ge_xSi_{1-x}/Si (by Schimmel etching) substrates were 6 x 10^4 /cm^2 and 2 x 10^6 /cm^2. Identical structures, consisting of 2500Å p-GaAs on 7500Å n-GaAs, both nominally doped to ~10^{18} /cm^3, were grown as a blanket film on both substrates by MOCVD at 650 °C. A simple two mask process consisting of mesa definition and SiO_2 passivation followed by patterning and deposition of 50Å Ti/ 750Å Au contacts to both anode and cathode completed the devices for testing. A finished 20 μm x 20 μm GaAs diode on a Ge/Ge_xSi_{1-x}/Si substrate is shown below in Figure V-6.

Figure V-6 *20 μm x 20 μm GaAs diode on Ge/Ge_xSi_{1-x}/Si*

Diode I-V curves were collected using an HP4145B and probe station with probe tips directly contacting cathode (on the top of the etched mesa structure) and anode (metal areas below the mesa).

Figure V-7 shows representative I-V curves of various size diodes:

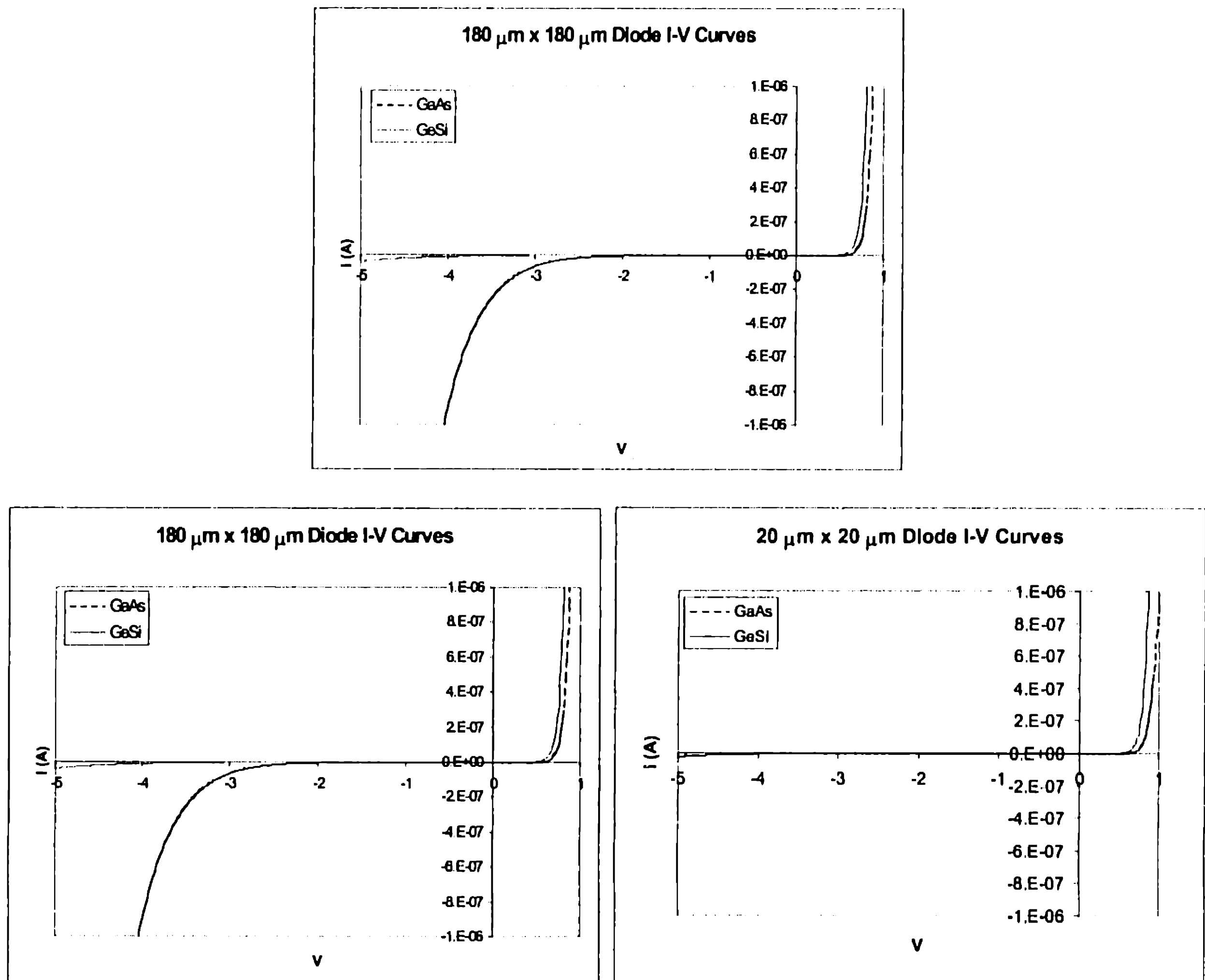


Figure V-7 *I-V characteristics of various sizes of GaAs diodes on Ge/Ge$_x$Si$_{1-x}$/Si and GaAs substrates.*

Breakdown

It is immediately apparent that the diodes of all sizes on GaAs inexplicably breakdown in reverse bias earlier than their counterparts on Ge/Ge$_x$Si$_{1-x}$/Si. During testing, a large number of diodes on GaAs also exhibited irreversible degradation in reverse bias (the I-V curves shown in Figure V-7 represent the best of those that survived the initial burn-in). This is highly unexpected considering the devices were grown in back-to-back runs on the same day and processed together thereafter. If anything, the higher TDD of the Ge/Ge$_x$Si$_{1-x}$/Si substrate should lead to higher leakage currents, earlier breakdown, and reduced reliability. We therefore suspect an unknown failure mechanism at high reverse bias, which is entirely unrelated to TDD. One possibility is the presence of doping transients in our MOCVD

reactor, since higher doping of the diodes on GaAs could lead to earlier breakdown, whether by avalanche or tunneling. Alternatively, it is also possible that the un-annealed Ti/Au metallization may have featured a high contact resistance leading to thermal breakdown, or that the direct contact of the probe tips may have damaged the devices, but again, no similar effect was noted on the GaAs/Ge/Ge_xSi_{1-x}/Si diodes.

Turn-on

In forward bias, the turn-on characteristic of diodes on both substrates are nearly identical, featuring ideality factors *n* ranging from between 1.7 and 2.2, calculated under the somewhat dubious assumption that the devices remained at room temperature throughout testing. This suggests a significant generation current component, however, it does not appear to be the effect of TDD either since the only clear trend is that *n* increases with decreasing device size. Indeed, some of the devices on Ge/Ge_xSi_{1-x}/Si substrates feature lower *n* than those on GaAs. As plotted in Figure V-8, it seems that surface rather than bulk recombination is the main source of leakage since the ratio of exposed perimeter increases with decreasing mesa size. Excessive surface leakage has been a persistent problem for III-V devices due to their lack of a passivating native oxide. [121,122]

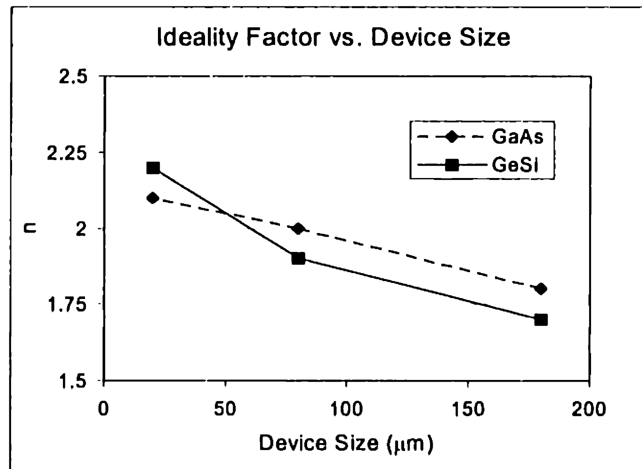


Figure V-8 *Ideality factor vs. device size of GaAs diodes on Ge/Ge_xSi_{1-x}/Si and GaAs substrates*

Zero-bias

R_0A measurements, calculated from the linear portion of the I-V curves at nearly zero reverse bias (recall Equation 2.1), probably best reflect the influence of TDD on our devices. Values

range between 10^5-10^7 Ω-cm^2, and despite their early breakdown at higher reverse bias, diodes on GaAs consistently feature R_0A a factor of 3-4 times higher than those on $Ge/Ge_xSi_{1-x}/Si$, as shown below in Figure V-9. Although a dependence on device size is still evident, indicative of a surface generation component, the improvement with increasing device size seems to taper off, especially for the devices on $Ge/Ge_xSi_{1-x}/Si$, reflecting measurement of TDD- limited bulk generation.

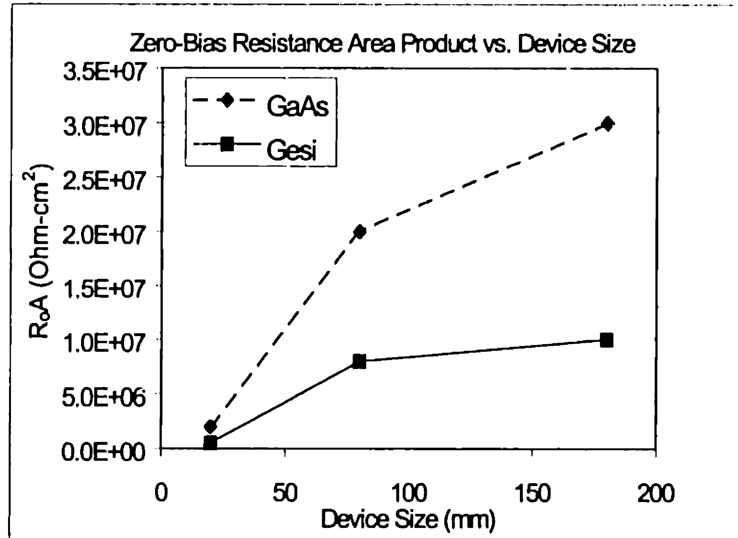


Figure V-9 *Zero-bias resistance area product of GaAs diodes on $Ge/Ge_xSi_{1-x}/Si$ and GaAs substrates plotted vs. lateral device dimension.*

Table V-2 summarizes the diode performance characteristics and trends discussed above.

Table V-2 *Performance of various size GaAs diodes on GaAs and Ge_xSi_{1-x} substrates*

180 um x 180 um	J_o (A/cm^2) @ -5V	R_0A (Ω-cm^2)	n
GaAs	2.6×10^{-2}	3×10^7	1.8
$Ge/Ge_xSi_{1-x}/Si$	1.2×10^{-4}	1×10^7	1.7
80 um x 80 um			
GaAs	7.2×10^{-3}	2×10^7	2.0
$Ge/Ge_xSi_{1-x}/Si$	1.4×10^{-4}	8×10^6	1.9
20 um x 20 um			
GaAs	4.8×10^{-3}	2×10^6	2.1
$Ge/Ge_xSi_{1-x}/Si$	2.6×10^{-5}	5×10^5	2.2

Conclusions

We have determined that the TDD of GaAs films grown on $Ge/Ge_xSi_{1-x}/Si$ is indeed limited by that of the substrate. Minimizing dislocation nucleation as Ge_xSi_{1-x}/Si is compositionally graded to the GaAs lattice constant is therefore an effective means of overcoming the 4.1% lattice mismatch between GaAs and Si. Additional reduction in $GaAs/Ge/Ge_xSi_{1-x}/Si$ TDD is expected with further optimization of Ge_xSi_{1-x} grading. At present the TDD of $Ge/Ge_xSi_{1-x}/Si$ substrates is probably limited by particulate contamination due to either gas-phase nucleation in the UHVCVD reactor or the lack of a cleanroom environment in our growth facility.

As indicated by the figures in Table I-2, the low 10^6 /cm^2 TDD of $GaAs/Ge/Ge_xSi_{1-x}/Si$ is already suitable for the integration of III-V FETs and on the verge of the acceptable limit for solar cells and LEDs. Record GaAs on Si minority carrier lifetimes have already been demonstrated on OSU's MBE-grown $GaAs/Ge/Ge_xSi_{1-x}/Si$.[123] In our comparison of GaAs diodes fabricated on GaAs vs. $Ge/Ge_xSi_{1-x}/Si$ substrates, the TDD difference can only be observed as a modest factor of 2-3 decrease in R_0A.

Chapter VI

Monolithic Integration of $In_xGa_{1-x}As$/GaAs Devices on Si CMOS

MOCVD GaAs/Si

The first step in the development of our monolithic integration demonstration was direct GaAs/Si heteroepitaxy in the same MOCVD reactor described in Chapter V. Substrates consisted of pieces cleaved to fit the graphite susceptor from (001) Si wafers offcut 6° to [110]. In general, epitaxy on Si in atmospheric pressure CVD reactors is problematic due to the tendency for Si to form a native oxide unless very high source and carrier gas purity is maintained. In an atmospheric reactor, the low carrier gas flow rates translate to a significant partial pressure of any oxidizing impurities, which increases the risk of poly-crystalline rather than epitaxial film growth. Furthermore, temperatures in excess of 850 °C are difficult to achieve in our reactor, whereas thermal oxide desorption does not usually take place until 1000 °C. The standard growth procedure that emerged out of these considerations thus included the following Si cleaning procedure:

1.) 5-10 minute piranha clean in 3 H_2SO_4 : 1 H_2O_2 (30%) to clean and oxidize the Si surface

2.) 1 minute dip in 10 DI H_2O : 1 HF to strip native oxide and hydrogen-passivate the Si surface

After loading into the reactor, the samples were annealed at 350 °C to desorb water and at 850 °C to promote single-domain reconstruction of the Si surface. A thin epitaxial Si buffer layer deposited at this point served to bury any surface contamination. Quenching the substrates to 400 °C, a two-step GaAs growth was then initiated; the full growth sequence consisted of:

1.) 10 minute bake at 350 °C in flowing N_2 to reduce water vapor
2.) 10 minute bake at 800-850 °C in N_2, to promote ordering of the Si surface
3.) 10 second flow of 1% SiH_4 to grow a thin 100Å Si buffer.
4.) 10 minute 1000Å GaAs buffer growth in H_2 at 400 °C
5.) GaAs growth at 650 °C

Figure VI-1 shows typical XTEM image of a 0.5 μm single-crystal GaAs/Si film achieved by this technique. Note the very high TDD, on the order of 10^8-10^{10} /cm^2, originating from the GaAs/Si interface. The sheer density of threads makes it difficult to detect the presence or confirm the absence of antiphase disorder; nevertheless, at least it seems that no APBs propagate to the surface of the film.

Figure VI-1 *XTEM image of a GaAs/Si film grown by MOCVD*

Although a detailed study of the occurrence antiphase disorder in GaAs/Si heteroepitaxy was not conducted as part of this study, temperature-dependent texture rotation, accompanied by bands of localized antiphase disorder, were observed on GaAs/Si grown in this manner. Following the work of Bringans *et al.* and our own study of as for GaAs/Ge/Ge_xSi_{1-x}/Si and GaAs/Ge, this observation suggests that (001) Si and Ge surfaces respond identically to and feature the same arsenic-induced sublattice allocation mechanism.

$In_xGa_{1-x}As$ on GaAs/Si LED/p-i-n Diodes

Having achieved reasonable MOCVD GaAs/Si growth we proceeded to develop $In_xGa_{1-x}As$ /GaAs/Si heterostructures for device fabrication. Despite the high TDD nucleated the GaAs/Si interface, it was hoped that compositional grading of $In_xGa_{1-x}As$/GaAs on GaAs/Si grown on patterned substrates could provide sufficient TDD decrease to allow reliable LED/p-i-n diode operation.

MBE $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs/Si LED p-i-n Prototype

Considerable promise for this effort was shown in an early demonstration of a single set of $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs/Si LED/p-i-n diodes grown by solid-source MBE in collaboration with Professor Fonstad's group in the Electrical Engineering Department. The final $In_{0.3}Ga_{0.7}As$ composition was chosen to explore the option of devices featuring 1.3 μm emission and detection for coupling to optical fiber. A schematic of the device structure is illustrated in Figure VI-2 (left) next to an XTEM shot (right) of a similar device structure that was never processed.

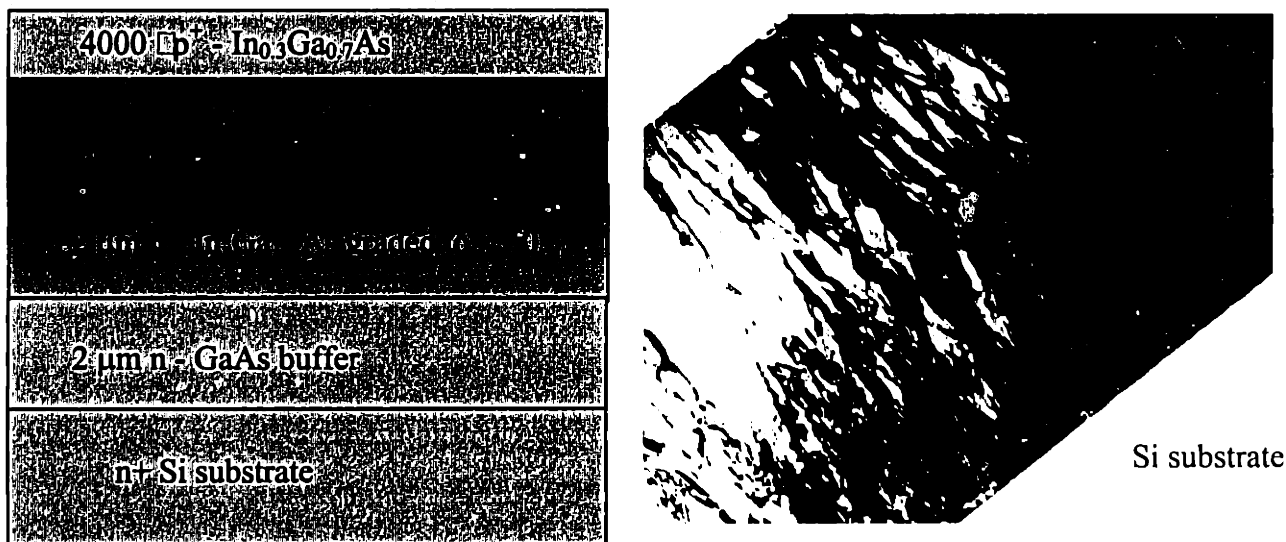


Figure VI-2 *MBE $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As$/GaAs/Si LED p-i-n prototype device structure and XTEM image. Note that there is no evidence of an $In_xGa_{1-x}As$ graded buffer suggesting poor growth calibration.*

Prior to III-V growth, trenches and mesas were patterned to isolate selected areas of the Si substrate where the devices would later be fabricated. After growth, III-V material was wet

etched in 20 H_2O:1 30 % H_2O_2:1 H_3PO_4 away from the Si surface at all but the selected device areas and a 2000Å PECVD oxide passivation was deposited and patterned. Image reversal photolithography was used to define ohmic contacts consisting of 1000Å Pt /50Å Ti (Au-free for future CMOS process compatibility) deposited by e-beam and photo-lithographically patterned by image-reversal liftoff.

A representative room temperature electroluminescence spectrum and the I-V curve of a 150 μm x 150 μm diode are shown below in Figure VI-3.

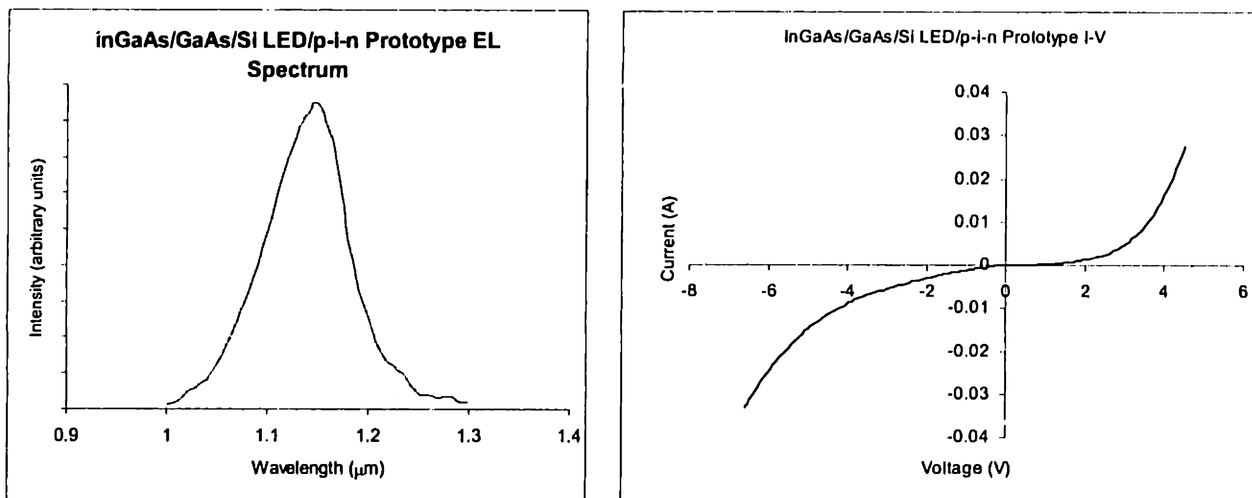


Figure VI-3 *Room temperature electroluminescence spectrum and I-V curve of a 150 μm x 150 μm MBE $In_{0.3}Ga_{0.7}As/In_xGa_{1-x}As/GaAs/Si$ LED p-i-n prototype device*

The forward bias I-V features an ideality factor of approximately 30 and is dominated by a high series resistance judging by its linearity. In reverse bias the diodes are very leaky, with typical R_0A values of 40 Ω-cm^2. Additionally, the 1.17 μm emission wavelength is well off the 1.3 μm target suggesting a final indium composition of 20% rather than 30%. The lack of calibration leading up to growth of this device structure and a group III overexposure error may account for these discrepancies. Nevertheless, achieving electroluminescence in a one-shot effort such as this one was encouraging by itself and spurred our own efforts towards developing improved devices by MOCVD.

MOCVD $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n Diode Prototypes

The calibration of our MOCVD reactor for graded $In_xGa_{1-x}As$ on GaAs devices and structures was developed concurrently with this study and the results have been documented elsewhere.[18,124] To evaluate the expected improvement in TDD achieved by $In_xGa_{1-x}As$ grading on GaAs/Si, we grew and compared $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ (graded at a rate of ~6% In/μm) and $In_{0.15}Ga_{0.85}As/GaAs/Si$ (ungraded) blanket films and patterned devices of equivalent 4 μm thicknesses. Starting materials consisted of 6° offcut (001) n^+ Si pieces cleaned in the same manner as earlier described for GaAs/Si growth. The difference in film morphology is shown by XTEM in Figure VI-4.

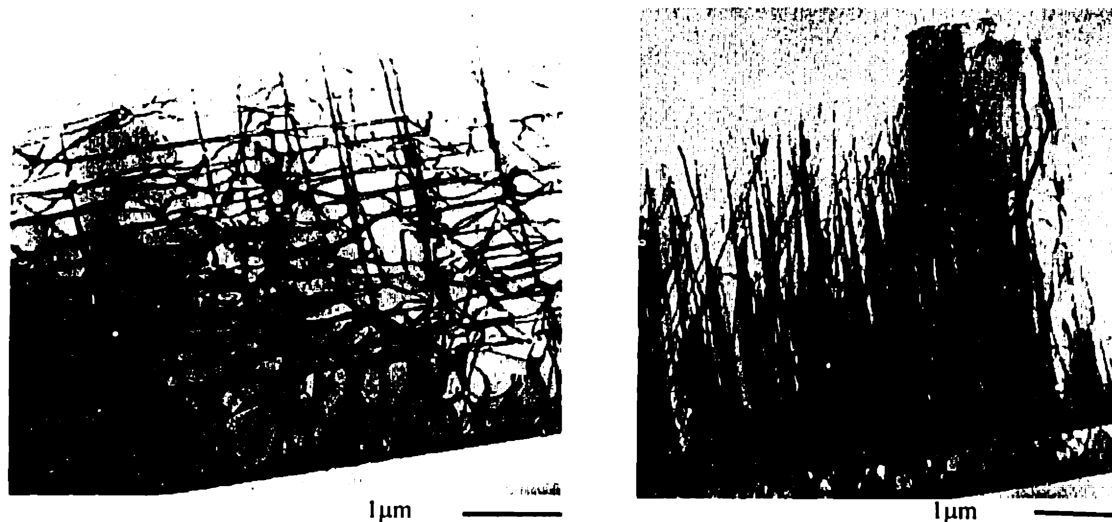


Figure VI-4 *XTEM micrographs of $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ (left) and $In_{0.15}Ga_{0.85}As/GaAs/Si$ (right) test structures.*

The direct growth of $In_{0.15}Ga_{0.85}As$ on GaAs/Si is marked by a very high TDD as a result of homogeneous nucleation at both of the highly mismatched interfaces. By comparison, some TDD reduction is achieved by grading $In_xGa_{1-x}As$ to $In_{0.15}Ga_{0.85}As$ on GaAs/Si. Apparently, the re-use of mobile threads from the GaAs/Si layer rather than homogeneous nucleation is responsible for strain relaxation in the $In_xGa_{1-x}As$ graded buffer. Although the observation of threads in both films in XTEM suggests TDD > 10^8 /cm^2, the TDD in the ungraded $In_{0.15}Ga_{0.85}As/GaAs/Si$ film is likely at least an order of magnitude higher than $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ film.

Identical $In_{0.15}Ga_{0.85}As$ LED/p-i-n device structures were subsequently grown and fabricated on the similar $In_{0.15}Ga_{0.85}As/GaAs$ and $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ structures. Note that in contrast to the TEM study presented above, these films were grown on (001) offcut Si substrates patterned with trenches and mesas to isolate individual growth areas. The devices were processed in the same manner as the MBE prototype devices. Figure VI-5 illustrates their structures in cross-section.

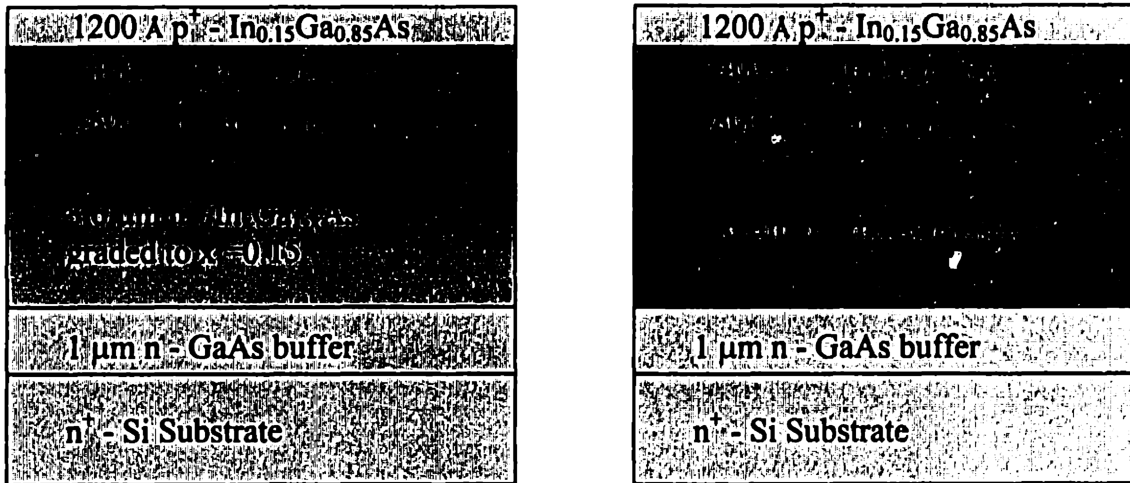


Figure VI-5 *$In_{0.15}Ga_{0.85}As/GaAs$ (left) and $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ (right) LED/p-i-n devices grown by MOCVD. The XTEM images in Figure VI-4 are of similar structures minus the final 7200 Å LED/p-i-n device layers.*

Figure VI-6 compares the I-V response of 150 µm x 150 µm for these two structures.

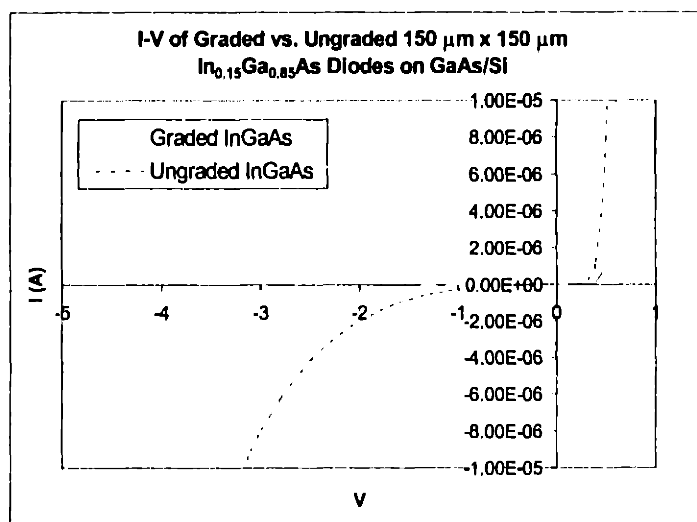


Figure VI-6 *I-V comparison of 150 µm x 150 µm $In_{0.15}Ga_{0.85}As$ diodes $In_xGa_{1-x}As/GaAs/Si$ and GaAs/Si.*

Clearly, the $In_{0.15}Ga_{0.85}As$ diodes with the intervening $In_xGa_{1-x}As$ graded buffer feature significantly less leakage current than those grown directly on GaAs/Si. Similarly, the $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ devices exhibit a superior ideality factor and R_0A as summarized in Table VI-1. Since no dependence on device size was noted, we were able to conclude that enhanced performance was entirely due to TDD reduction via compositional grading.

Table VI-1 *$In_{0.15}Ga_{0.85}As$ diode performance*

	J_0 (A/cm^2) @ -1V	R_0A (Ω-cm^2)	n
$In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$	2.3×10^{-4}	1×10^4	1.7
$In_{0.15}Ga_{0.85}As/GaAs/Si$	1.2×10^{-3}	1×10^3	2.1

Unfortunately, poor metal step coverage between the device contacts and bonding pads prevented mounting of the diodes for electroluminescence testing. Nevertheless, the room temperature R_0A of 10^4 Ω-cm^2 suggests that the $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ devices are suitable for near-infrared photodetector applications. Despite the high mismatch interface and the unavoidably high TDD in the device structure, these R_0A lie within an order of magnitude of room temperature values for commercially produced 1.55 μm lattice-matched $In_{0.53}Ga_{0.47}As/InP$ photodetectors, although $R_0A > 10^6$ Ω-cm^2 have been reported.[125] Assuming equivalent material quality, $In_{0.15}Ga_{0.85}As$ diodes would be expected to have a lower leakage current and higher R_0A than $In_{0.53}Ga_{0.47}As$ diodes due to the larger energy bandgap. That this is not the case for the OEIC devices clearly indicates that the $In_{0.15}Ga_{0.85}As$ diodes are indeed limited by TDD generation-recombination current.

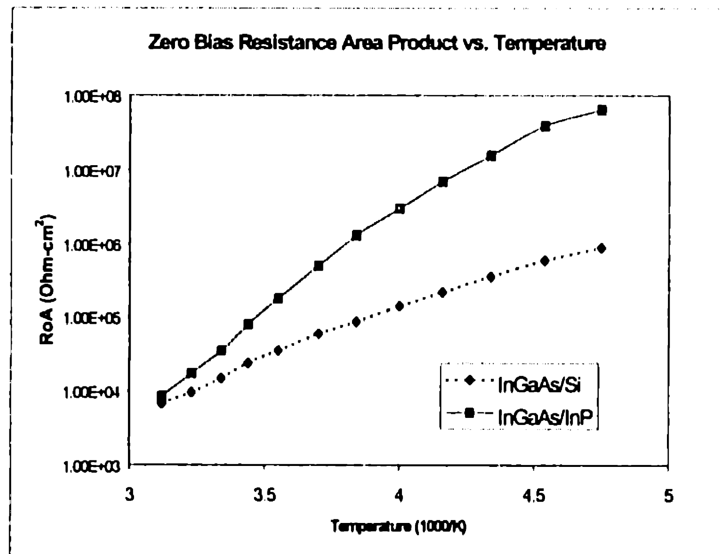


Figure VI-7 *R_0A vs. Temperature for $In_{0.53}Ga_{0.47}As/InP$ photodetector and $In_{0.15}Ga_{0.85}As/In_{1-x}Ga_xAs/GaAs/Si$ LED/p-i-n diode*

Figure VI-7 plots R_0A versus temperature for a commercially produced $In_{0.53}Ga_{0.47}As/InP$ photodetector alongside our $In_{0.15}Ga_{0.85}As/In_{1-x}Ga_xAs/GaAs/Si$ LED/p-i-n. As expected, R_0A increases upon cooling due to the decrease in intrinsic carrier concentration. However, the $In_{0.15}Ga_{0.85}As$ diodes exhibit markedly less improvement than the $In_{0.53}Ga_{0.47}As$ diodes suggesting that deep-level traps rather than thermal carrier generation dominate the leakage current.

$In_xGa_{1-x}As/GaAs/Si$ on CMOS Process Integration

MIT Baseline CMOS

Based on the above performance results, the $In_{0.15}Ga_{0.85}As/In_{1-x}Ga_xAs/GaAs/Si$ LED/p-i-n devices were chosen for our OEIC demonstration. The substrate silicon IC was fabricated at the ICL according to the MTL baseline twin-well CMOS process.[126] The MIT baseline process, featuring 1.5 μm gate lengths, a 230Å gate oxide, and a single-level aluminum metallization, is designed for ± 5 V operation and optimized for analog applications. Four inch p^- (2-10 ohm–cm) boron doped (001) Si wafers offcut 6° towards [110] were used for actual OEIC host wafers, which were processed alongside p^- epi on p^+ (001) Si wafers used as monitors for the conventional CMOS process. The only modification to the original CMOS process involved the ion implantation of the offcut wafers. Whereas on-axis (001) wafers are usually tilted 7° from (001) during implantation to avoid ion channeling, the offcut wafers were un-tilted and implanted directly to achieve the same effect.

Growth and Integration of $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n Diodes

The last pair of ion implantations in the baseline CMOS process define the PMOS and NMOS source/drain and gate electrode contacts, which are subject to a simultaneous drive-in diffusion at 950 °C. Shortly thereafter, a boron-phospho-silicate glass (BPSG) passivation layer is deposited at 925 °C. The $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ devices were inserted at this point where the risk of contaminating the active CMOS device regions is minimal, and whereafter there is no further high temperature annealing in the normal CMOS process. Again, our main integration concern was thus not the survivability of the $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n diodes, but rather the possibility of compromising the CMOS process during their 2 hour growth cycle at 650-700 °C.

In preparation for III-V growth, the incomplete CMOS wafers were first transferred to the TRL prior to BPSG deposition. There, device growth areas were defined by patterning and etching through the 0.5 μm field oxide to reveal n-well Si regions. The wafers were then taken back to the ICL where 3 μm trenches were dry etched into the selected growth areas to provide isolation from adjacent regions of the host IC surface. BPSG deposition and the opening of contacts to the CMOS devices were then completed in the ICL as usual. Finally,

the III-V growth areas were once again etched to remove BPSG in preparation for direct III-V heteroepitaxy.

In order to accommodate our reactor's graphite susceptor, 2 cm x 2 cm pieces of the host IC/substrate wafer were then die-sawed, allowing simultaneous III-V growth on two complete ICs per run. The same cleaning procedure as for GaAs/Si was used prior to loading the MOCVD reactor, however, a loss of N_2 carrier gas purity necessitated modification of the GaAs initiation procedure as follows:

1.) 10 minute bake at 350 °C in flowing H_2 to reduce water vapor
2.) Raise temperature to 550 °C in H_2 and 1% SiH_4.
3.) Flow 1% SiH_4 for one minute to grow 100Å Si buffer at 550 °C.
4.) Drop to 400 °C, 10 minute 1000Å GaAs buffer in H_2
5.) GaAs growth at 650 °C

Although the lack of a high temperature anneal at 850 °C may have prevented single-domain ordering, it did restore the ability to grow single-crystalline GaAs/Si, whereas the original procedure had begun yielding poly-crystalline material. Selective growth of a 2 μm single-crystalline GaAs/Si film in the host IC n-well is shown in Figure VI-8.

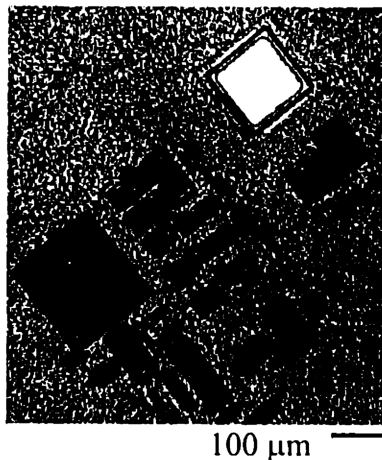


Figure VI-8 *2μm GaAs growth on host Si IC. Note the specular single-crystalline growth in the defined device region and poly-crystalline deposition elsewhere.*

After $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ device growth in our reactor, the ICs were taken to TRL where all further processing was conducted. The first step was removal of poly-crystalline III-V material that had deposited simultaneously on the BPSG surface during growth in the selected device areas. A patterned PECVD oxide hard mask protected the actual device areas while the excess poly-crystalline material was stripped in a solution of 20 H_20 : 1 30% H_20_2 : 1 H_3PO_4. Another 2000 Å layer PECVD oxide layer was deposited to passivate the resulting III-V device mesas and contact windows were then etched in diluted HF. Ohmic ring contacts to the diode cathode were formed by e-beam evaporation of 1000Å Pt/50Å Ti and image-reversal liftoff. Pad contacts to the anode and cathode were formed in conjunction with the CMOS metallization by a blanket 1 μm Al evaporation that was subsequently patterned and dry-etched in a BCl_3/Cl_2 chemistry. A 30s rapid thermal anneal at 450 °C completed the OEIC.

An unfortunate consequence of the III-V growth cycle was the effect of thermal stress on the BPSG passivation layer. The optical micrograph in Figure VI-9 shows $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ diodes fabricated alongside CMOS circuitry on the finished OEIC.

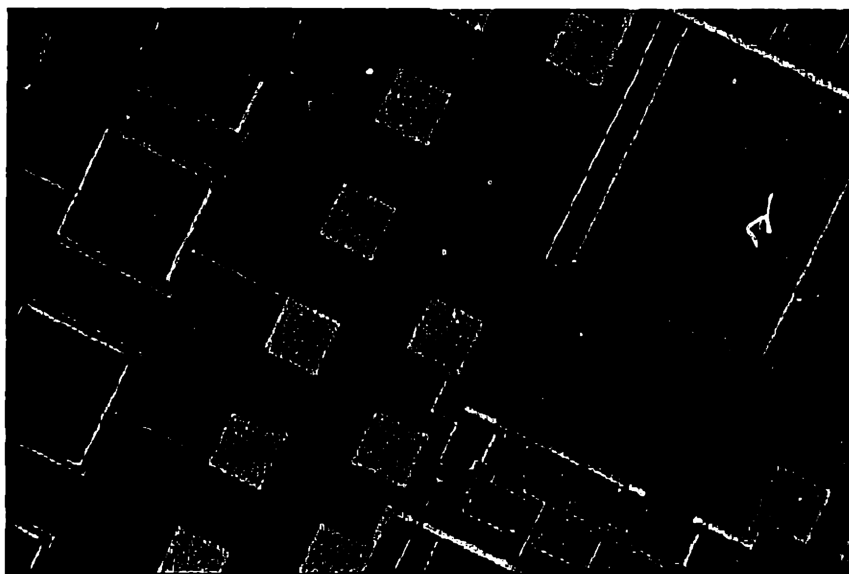


Figure VI-9 *Optical micrograph of integrated OEIC featuring $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ p-i-n detectors and CMOS circuitry. Note the formation of cracks in the BPSG passivation.*

Exposure of the BPSG to dilute HF acid during patterning of the III-V diodes reveals the presence of micro-cracks in the passivation layer which apparently formed upon cooling the host IC from 700 °C to room temperature. Since their presence was not initially noted, appropriate control of the cooling rate was not implemented. Although the larger CMOS driver circuits were thus shorted-out or otherwise destroyed, smaller test structures, featuring individual NMOS and PMOS transistors remained testable.

Integrated $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n Diode Performance

As expected, the integrated $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n diodes exhibited approximately the same performance as the earlier device fabricated on patterned Si. Table VI-2 and Figure VI-10 show typical I-V measurements from a 180 μm x 180 μm integrated diode. Although the leakage current density and ideality factor are higher than previously, the R_0A is superior. Despite the change in GaAs initiation procedure the differences between integrated and prototype devices probably reflect no more than minor run to run variation in doping profiles or direct III-V on Si materials quality.

Table VI-2 *Integrated $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ diode performance*

	J_0 (A/cm^2) @ -1V	$\overline{R_0A}$ (Ω-cm^2)	n
$In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$	1.1 x 10^{-3}	2 x 10^4	2.4

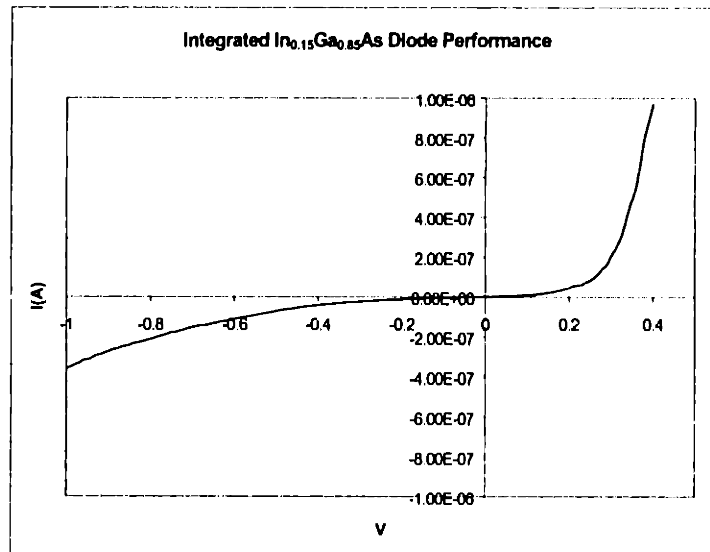


Figure VI-10 *I-V curve of a 180 μm x 180 μm integrated $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ LED/p-i-n diode.*

The same metal step coverage problem encountered during processing of our prototype devices resurfaced during OEIC fabrication resulting in discontinuity between the aluminum runners from the mesa cathode contact to the bonding pad as shown below in Figure VI-11.

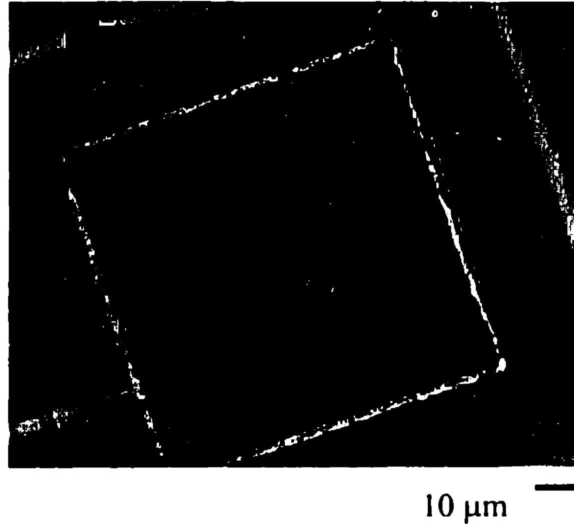


Figure VI-11 *Loss of metal step coverage at the edge of an* $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ *mesa diode.*

Again, this prevented electroluminescence testing and effectively killed our hopes of establishing an two-way optical link between OEICs.

CMOS Performance

In recent work, Gerard *et al.* demonstrated the negligible impact of both substrate offcut and a simulated III-V growth cycle (750 °C for 4 hrs.) on a 0.8 μm gate length CMOS host IC.[127,128] As a result we fully expected our more modest growth cycle to be compatible with the more tolerant 1.5 μm MIT baseline CMOS.

Of the four on-axis p^- epi on p (001) Si wafers processed as monitors alongside the 6° offcut wafers intended for actual III-V integration, only one survived the entire CMOS process. To test the performance of CMOS devices without III-V integration, it and one of the offcut wafers were processed to completion in the ICL. Although a higher density of interface states at the gate oxide might be expected of the 6° offcut wafers, to our surprise we discovered that the offcut devices performed normally, whereas the on-axis devices were so leaky they could not saturate or be turned off as shown below (Figure VI-12).

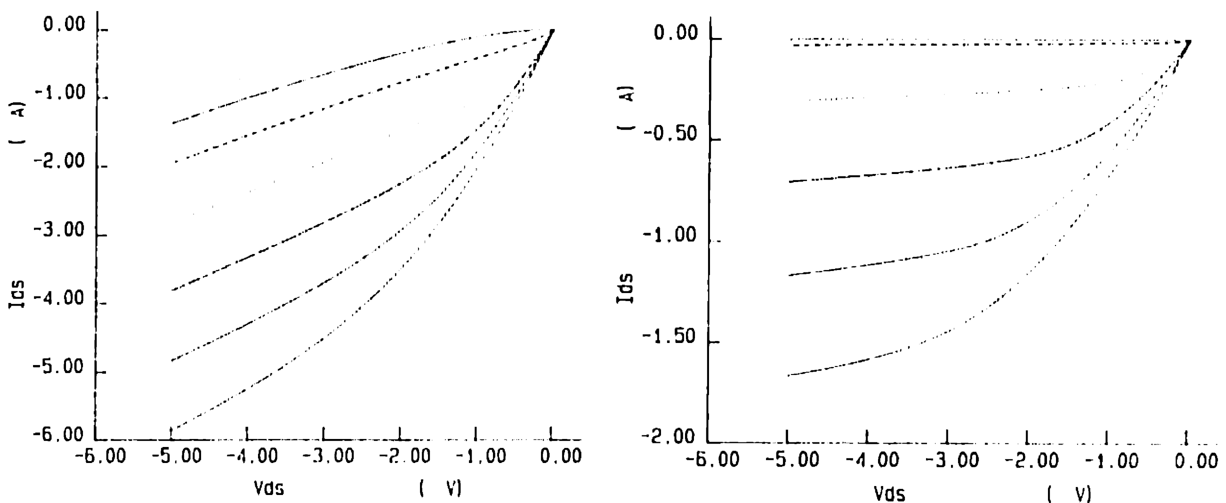


Figure VI-12 *Comparison of I_{ds} vs. V_{ds} (V_g stepped from 0 to –5V) for 2μm gate length PMOS device on on-axis and 6 °offcut (001) Si. Note the leaky on-axis performance, which fails to saturate. The I_{ds} scale is actually in mA, not A.*

Tests of the CMOS devices after the III-V growth and integration cycle revealed at worst a minor shift in the NMOS threshold voltage V_{th}. The topmost I_{ds} vs. V_{ds} plots in Figure VI-13 are for 1.5μm PMOS and NMOS transistors fabricated on conventional (001) Si according to the MIT baseline process. For comparison the bottom pair of I_{ds} vs. V_{ds} plots in Figure VI-13 show the same devices fabricated on (001) Si offcut 6° to [110] with integrated $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ LED/p-i-n diodes.

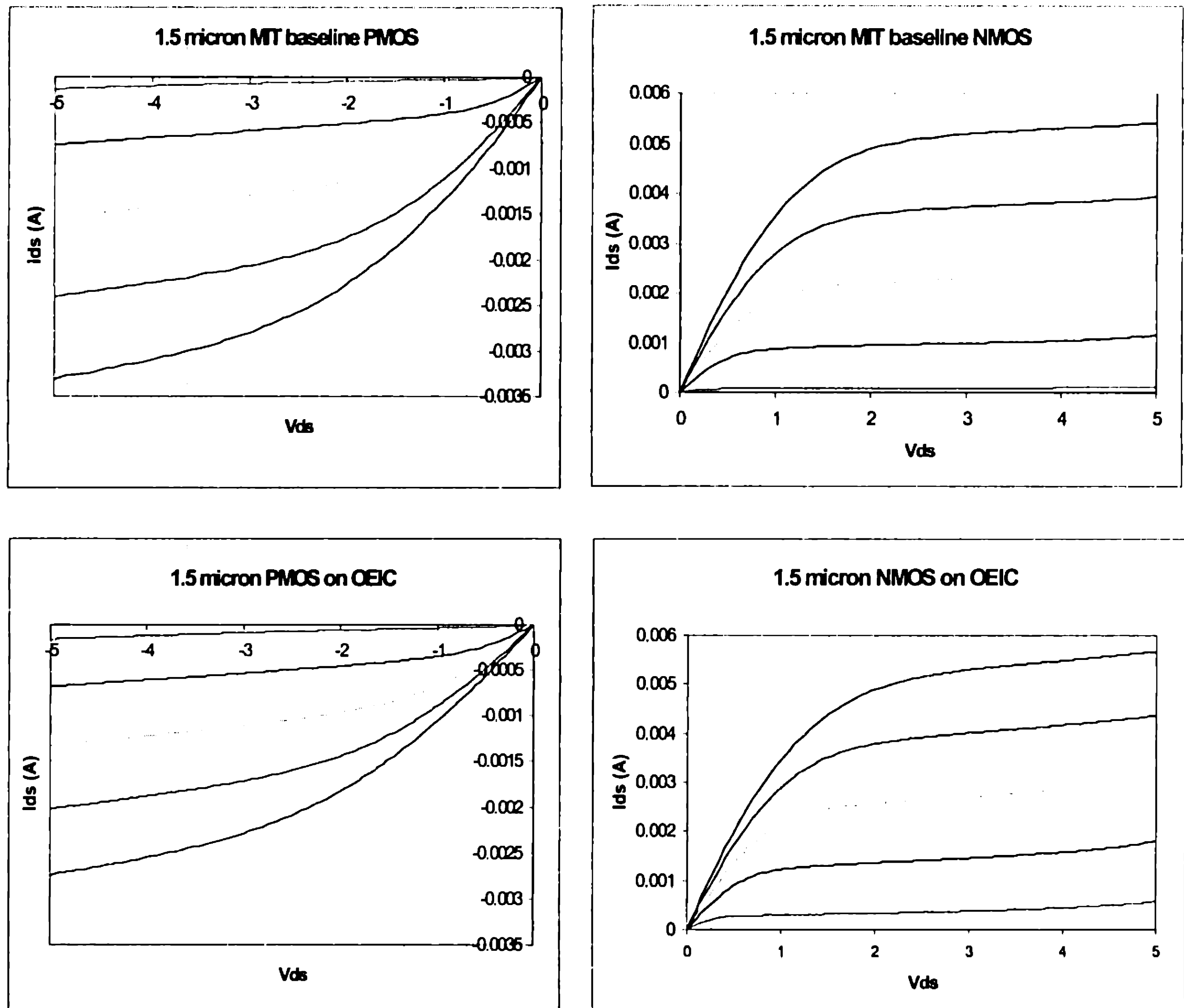


Figure VI-13 *At top, I_{ds}-V_{ds} curves (V_g stepped from 0 to 5V or –5V) of 1.5 μm gate length PMOS and NMOS transistors fabricated according to the MIT baseline process on (001) Si. The bottom curves show identical devices from the OEIC that were tested after III-V growth and processing.*

Clearly, normal PMOS and NMOS normal transistor operation is not compromised despite III-V integration, and we speculate that the integrated circuits would likewise have been functional, had passivation remained intact. Note, however, that I_{ds} at V_g = 1 V saturates higher on the OEIC NMOS than on the baseline NMOS. This suggests a threshold voltage decrease that allows the OEIC NMOS to turn on earlier than usual. No threshold voltage shift is observed of the OEIC PMOS devices.

Dopant penetration of the 230 Å gate oxide is the most likely candidate for a thermal cycle induced threshold voltage variation. In the baseline process, the NMOS and PMOS poly-silicon gate electrodes are respectively As and BF_2 ion-implanted simultaneously with the formation of source and drain wells. Diffusion of As or BF_2 through the oxide and into the channel regions could lead to early inversion, hence a threshold voltage shift.[129] However, it has been noted that the thermal budget for penetration of NMOS devices is always larger than that of PMOS devices, and our thermal cycle does not even approach that required for BF_2 penetration of a 30 Å gate oxide.[130] Moreover, not only does As diffuse more slowly than BF_2 through oxide, but As also has a higher segregation coefficient at the oxide/silicon interface. Thus, if there were any thermal cycle induced threshold voltage variation, one would expect to first see it in the OEIC PMOS rather than the NMOS.

Another possible source of threshold voltage shift could be lateral diffusion of the source and drain wells, which could shorten the effective channel length. Diffusion of As and B through silicon is orders of magnitude faster than through oxide, but the gate length is also two orders of magnitude wider than the gate oxide thickness. Regardless of these considerations, As has a lower diffusion coefficient than B in silicon as well, such that one would again first expect short-channel behavior of the OEIC PMOS rather than the NMOS.

We believe the threshold voltage variation is not in fact directly attributable to the III-V integration cycle. First of all, MIT baseline CMOS I_{ds} vs. V_{ds} curves that the OEIC devices are compared against Figure VI-13 are of test devices fabricated from a much earlier baseline lot. Unfortunately, the threshold voltage of the single on-axis CMOS wafer that survived the baseline process in our lot was effectively zero. Hence we have ample evidence to support

wafer to wafer threshold voltage variation within individual lots of the MIT CMOS process independent of further $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ integration. Ideally, it would have been possible to measure CMOS characteristics of each individual host IC prior to growth and processing of the $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs/Si$ devices. For practical purposes, though, this simply wasn't possible, and it is fortunate that the wafer from which the OEIC die were chosen from happened to have respectable NMOS and PMOS device characteristics, despite the threshold voltage shift of unknown origin.

Conclusions

Despite the high mismatch, it is possible to grow and process integrate $In_{0.15}Ga_{0.85}As/In_xGa_{1-x}As/GaAs$ devices on Si with acceptable performance for some applications. Although a two-way through-wafer optical link was never achieved, our device results, in particular the room temperature R_0A of 10^4 Ω–cm^2, were well suited to Discovery Semiconductors' interest in satellite-based NIR focal plane array detection systems.

We find it unlikely that the MOCVD thermal cycle or process integration scheme should pose a significant barrier to monolithic III-V on Si integration. Given the wafer to wafer variation in CMOS performance in the MIT baseline process itself, the threshold voltage shift observed in the OEIC cannot directly be attributed III-V integration. It is, however, instructive that the individual PMOS and NMOS transistors were certainly not entirely destroyed.

Cracking of the BPSG is representative of the many unanticipated processing obstacles encountered during OEIC fabrication, but is not a phenomenon that will fundamentally limit successful III-V/CMOS integration. It is likely that cracking could be altogether avoided with proper optimization of the growth temperature cycle or by changing the process integration sequence. Likewise, if thermal budget had been identified as a problem, the original baseline CMOS process might have been modified to account for the growth cycle by shortening the high temperature diffusion anneals. In general, any alternative III-V integration sequence can be expected to introduce a set of different obstacles, each demanding some level of process innovation.

Chapter VII

Conclusions and Recommendations

Conclusions

Summary of Experimental Findings

Low defect density Ge_xSi_{1-x} buffers graded to 100% Ge have effectively bridged the gap between GaAs and Si lattice constants. This work, which has further demonstrated the ability to suppress antiphase disorder and maintain the low TDD of Ge/Ge_xSi_{1-x}/Si substrates during GaAs heteroepitaxy, removes two fundamental materials obstacles to the monolithic integration of III-V materials and devices on Si.

Although it has long been known that high temperature annealing of offcut substrates facilitates the suppression of antiphase disorder, we have further demonstrated by solid-source MBE and inferred from MOCVD that arsenic exposure conditions, whether intentional or inadvertent, also play a pivotal role in determining the sublattice location of GaAs on Ge. In GaAs/Ge by solid-source MBE, antiphase disorder may be averted by As_2 exposure at 350 °C, allowing the growth of single-domain GaAs-A. Exposure to As_2 at 500 °C, regardless of the original Ge surface reconstruction, single-domain or not, invariably leads to antiphase disorder. In MOCVD GaAs/Ge heteroepitaxy, arsenic exposure conditions cannot be controlled as carefully due to the presence of a background arsenic vapor pressure originating from susceptor and reactor sidewall deposits. Nevertheless, single-domain GaAs/Ge of both sublattice orientations may be grown: GaAs-A at high temperatures > 600 °C and GaAs-B at low temperatures < 500 °C. The transition between sublattice orientations is determined by competition between kinetically limited arsenic dimerization mechanisms. The appearance of residual GaAs-A at low temperature in the form of localized antiphase disorder is consistent with single-domain MBE GaAs/Ge and reflects the effect of cooling in a background arsenic vapor pressure.

For MBE GaAs/Ge, excess arsenic point defect incorporation during low temperature (350 °C) GaAs co-evaporation was identified and eliminated as a source of excess threading dislocation density. In the absence of such extrinsic threading dislocation nucleation mechanisms, we verified by PVTEM and EHD measurements that the low $10^6/cm^2$ TDD of Ge/Ge_xSi_{1-x}/Si substrates translates to similar TDD for MOCVD GaAs/Ge/Ge_xSi_{1-x}/Si. The

recent achievement of Ge/Ge_xSi_{1-x}/Si TDD < 10^6/cm^2 suggests that similar improvements for GaAs/Ge/Ge_xSi_{1-x}/Si TDD will be forthcoming.

Low defect density GaAs/Ge/Ge_xSi_{1-x}/Si paves the way for the development of a host of potential III-V on Si applications. To evaluate the enhanced device performance achieved by Ge/Ge_xSi_{1-x}/Si substrates, the zero-bias resistance area product versus estimated TDD has been plotted in for the various MOCVD devices grown in this study.

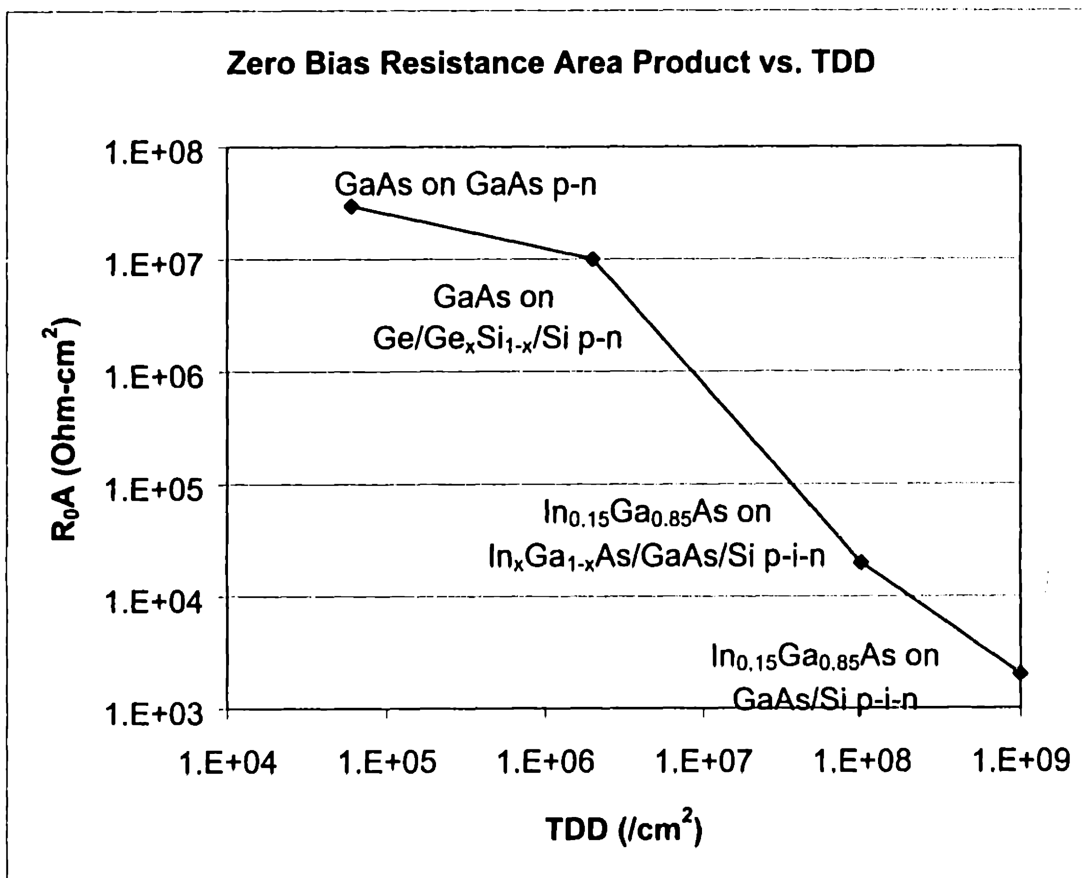


Figure VII-1 *R_0A versus TDD for the diodes fabricated in this study. Nearly three orders of magnitude improvement in R_0A is achieved on Ge/Ge_xSi_{1-x}/Si substrates versus Si. Only an additional factor of three improvement is achieved on GaAs versus Ge/Ge_xSi_{1-x}/Si.*

Although the wider depletion region and smaller bandgap of the $In_{0.15}Ga_{0.85}As$ on Si LED/p-i-n diodes complicates direct comparison with the GaAs diodes, the trend described clearly suggests that as TDD decreases to the level of Ge/Ge_xSi_{1-x}/Si substrates, the average

dislocation spacing approaches the bulk minority carrier diffusion length such that the TDD induced leakage current becomes negligible. These results correlate well with OSU's record GaAs/Ge/Ge_xSi_{1-x}/Si minority carrier lifetime measurements and indicate the defect densities we have achieved are approaching the acceptable limits for integration of solar cells, laser diodes, and LEDs. The only degradation of GaAs diodes on Ge/Ge_xSi_{1-x}/Si directly attributable to the higher defect density of Ge/Ge_xSi_{1-x}/Si versus GaAs substrates was a modest factor of 2-3 reduction in the zero bias resistance area product.

Since the III-V semiconductors are typically grown epitaxially at temperatures (< 700 °C) well below those encountered during oxidation, diffusion, and post-implantation annealing (> 900 °C) of SI ICs, we believe that monolithic integration of III-V materials on Si is a viable means of OEIC fabrication with distinct economy of scale advantages over the hybrid alternative. Our III-V on CMOS demonstration revealed no degradation of PMOS and NMOS transistor characteristics that could definitively be attributed to the MOCVD growth cycle. The ability to directly grow working $In_{0.15}Ga_{0.85}As$/$In_xGa_{1-x}As$/GaAs LED/p-i-n devices without compromising the host IC suggests future attempts at integrating improved devices that take full advantage of Ge_xSi_{1-x} buffer technology.

Directions for Future Experimental Work

Numerous applications exist for GaAs/Ge/Ge_xSi_{1-x}/Si heteroepitaxy, each of which faces its own unique challenges beyond the mere suppression of antiphase disorder and TDD. We fully expect the TDD of GaAs/Ge/Ge_xSi_{1-x}/Si films to decrease below the acceptable limits of performance for solar cells, lasers, and LEDs. To build on the preliminary device work presented in this thesis, it is necessary to further optimize growth and processing of homoepitaxial III-V devices in our MOCVD reactor to more accurately assess and qualify the same devices on Ge/Ge_xSi_{1-x}/Si substrates. In addition to performance, reliability of III-V on Ge/Ge_xSi_{1-x}/Si devices also needs to be evaluated, especially for high current density LEDs and laser diodes where DLD propagation is a threat. The recent achievements of 2000 hour and 7000 hour continuous wave operation of direct growth InGaP/GaAs/Si[131] and InP/Si[132] laser diodes, respectively, suggests that the lower defect densities possible with Ge/Ge_xSi_{1-x}/Si substrates should allow fabrication of commercial quality III-V on Si optoelectronic devices.

The one fundamental materials barrier not addressed in this work is the significant thermal mismatch between GaAs and Si. Cracking of GaAs/Ge/Ge_xSi_{1-x}/Si films was often observed at GaAs thicknesses greater than 2 μm as shown in Figure VII-2, apparently in response to tensile strain accumulation upon cooling from elevated GaAs growth temperatures.

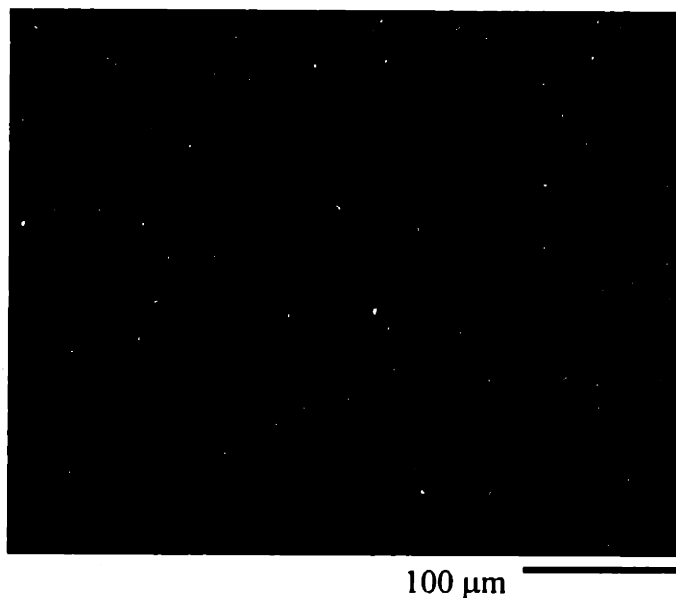


Figure VII-2 *Cracks in a ~2 μm GaAs/Ge/Ge_xSi_{1-x}/Si film due to thermal strain.*

For large area devices such as III-V solar cells or integrated GaAs MESFET circuitry, epilayer cracking poses severe reliability issues. One strategy to alleviate cracking relies upon further optimization of Ge_xSi_{1-x} grading to achieve the same low TDD while decreasing the overall thickness of the buffer. This approach decreases the overall tensile strain energy of a GaAs/Ge/Ge_xSi_{1-x}/Si film as per Equations 1.1 and 1.7. Alternatively, it might be possible to achieve GaAs/Ge/Ge_xSi_{1-x}/Si heteroepitaxy without complete relaxation of misfit compressive strain during growth such that the thermal strain incurred upon cooling is sufficiently offset to prevent cracking. The remaining possibility is to accept a certain density of cracks in the GaAs epilayer but to control and confine their nucleation by substrate patterning or to develop a means of filling or otherwise passivating them.

Another materials barrier exists specific to the application of GaAs/Ge/Ge_xSi_{1-x}/Si MESFETs for integrated wireless communication capability. Microwave and radio-frequency GaAs MESFET ICs require semi-insulating substrates to minimize signal loss to free carrier

adsorption. Semi-insulating GaAs substrates are produced by controlling the point defect concentrations of liquid-encapsulated Czochralski grown material. Heteroepitaxial GaAs is usually not semi-insulating; MOCVD GaAs, for example, may be p-type or n-type depending on the V/III ratio. At low V/III ratios, p-type doping dominates due to carbon incorporation from TMG, whereas at high V/III ratios, n-type doping prevails due to the presence GeH_4 as an impurity in arsine. It remains to be seen whether the point-defect concentrations of heteroepitaxial GaAs films and Si substrates can be manipulated to the point where reliable and effective substrate isolation is achieved. Barring such a solution, processing alternatives such as dielectric isolation of the GaAs epilayer may need to be developed.

The failure to demonstrate a two-way optical link on a Si host IC using III-V optoelectronic devices renders our OEIC demonstration incomplete and should be remedied as a continuation of this study. Although we did not observe CMOS degradation attributable to our MOCVD growth cycle, the mere four OEICs processed do not constitute an exhaustive, statistically relevant treatment of the process integration obstacle. Given the potential for a monolithic III-V on Si OEIC, reliability evaluation concerning the thermal degradation of host ICs featuring even more aggressively scaled critical dimensions may be appropriate, as are studies of the impact that successful III-V integration is likely to have on Si IC design trends.

Finally, in light of the defect densities and device performance attainable via GaAs/Ge/Ge_xSi_{1-x}/Si heteroepitaxy, it is also now appropriate to consider the process integration obstacles of Ge_xSi_{1-x} buffers on selected areas of a host IC for III-V growth. The two primary considerations for fabrication of such a Ge_xSi_{1-x} composite substrate are buffer thickness and thermal budget infringement. A 10 μm Ge_xSi_{1-x} buffer protruding above the Si surface compromises planarity, therefore, a realistic integration approach must incorporate recessed Ge_xSi_{1-x} buffers grown in patterned trenches to leave the Ge cap layer relatively co-planar with the Si substrate. It is not clear whether or not the same TDD optimized for Ge_xSi_{1-x} growth large substrates can be maintained for a composite Ge_xSi_{1-x} substrate. Regarding the thermal budget constraint, optimal Ge_xSi_{1-x} growth at low Ge concentrations takes place near 900 °C. Maintaining these growth conditions while remaining CMOS compatible will require front-end integration of Ge_xSi_{1-x} to avoid compromising sensitive doping profiles. Since Ge is

chemically benign in Si, one possibility is coplanar integration of 50% Ge_xSi_{1-x} buffers on a bare Si wafer prior to any CMOS processing. This altogether avoids the possibility of thermal budget infringement since the high Ge concentrations may be grown later optimally at 550 °C, and the 50% Ge_xSi_{1-x} may be polished back to remove surface roughness as is current practice for maintaining low TDD. The second half of the Ge_xSi_{1-x} buffer and any III-V growth might later be planarized, not with the Si substrate, but with the dielectric encapsulation.

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