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A 93% Efficiency Reconfigurable Switched-Capacitor DC-DC Converter Using On-Chip Ferroelectric Capacitors

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Dynamic Voltage Scaling (DVS) has become one of the standard techniques for energy efficient operation of systems by powering circuit blocks at the minimum voltage that meets the desired performance [1]. Switched Capacitor (SC) DC-DC converters have gained significant interest as a promising candidate for an integrated energy conversion solution that eliminates the need for inductors [2,3]. However, SC converters efficiency is limited by the conduction loss, bottom plate parasitic capacitance, gate drive loss in addition to the overhead of the control circuit. Reconfigurable SC converters supporting multi-gain settings have been proposed to allow efficient operation across wide output range [2,4]. Also, High density deep trench capacitors with low bottom plate parasitic capacitance have been utilized in [5] achieving a peak efficiency of 90%. In this work, we exploit on-chip ferroelectric capacitors (Fe-Caps) for charge transfer owing to their high density and extremely low bottom plate parasitic capacitance [6]. High efficiency conversion is achieved by combining the Fe-Caps with multi-gain setting converter in a reconfigurable architecture with dynamic gain selection.

Figure 21.7.1 shows the top level architecture of the whole power management IC. It consists of reconfigurable switched capacitor DC-DC converter split in four modules (M_1-M_4) that are interleaved for output voltage ripple reduction [3,4], pulse frequency modulation (PFM) regulation logic, clock generator, gain selection block that include programmable low duty cycle timers, and a voltage reference. The transistor level implementation of the SC module is shown in Figure 21.7.2a which can be reconfigured for four gain settings (1-2/3-1/2-1/3) as shown in Fig. 21.7.2b. Each module consists of two charge transfer capacitors, 1nF each, and ten switches. Since the implementation of gain settings (2/3, 1/3) requires two capacitors while (1,1/2) can be achieved with one only, thus, for the latter each module is reconfigured into two identical sub-modules running with 180 degree phase shifted clocks for further ripple reduction.

The losses due to the bottom plate parasitic capacitance of on-chip capacitors usually limit the peak efficiency of the converter. These losses occur as SC converters supply power to the load through the charge and discharge of flying capacitors (C_1 and C_2). A direct non-desirable impact to this process is the charge and discharge of the bottom plate parasitic capacitance, αC, every clock cycle [2]. As an example, for gain setting 1/2, the converter charges C_1 to (V_{in}-V_{out}) in phase 1 and discharges it to V_{out} in phase 2. In companion to this process the bottom plate capacitance gets charged to V_{out} and discharged to ground wasting an energy of $\alpha C_1 V_{out}^2$ per cycle where α is technology dependent (the same process applied for capacitor C_2 but with the reverse order of phases). Highly efficient conversion is achieved by utilizing the ferroelectric capacitors, that posses extremely low bottom plate parasitics, for charge transfer. In addition, the architectures utilized for each gain setting are selected to minimize the voltage swing across the bottom plate capacitors for maximizing efficiency. Since the output load current is directly proportional to the capacitance of the flying caps [8], therefore, the Fe-Caps high density allows for supplying the power demands of the load without a highly significant area overhead.

Figure 21.7.3a depicts the control logic for the converter output voltage regulation. The PMIC employs a PFM modulation scheme using a Strong-Arm comparator running at f_{CLK} which is 4 times the maximum desired switching speed, f_{sw}. The comparator output is fed into cascaded clock dividers and non-overlap clock generators for providing the multi-phase control signals for the four modules of the converter [7]. The comparator clock is generated on-chip using a ring oscillator (RO) with external digital calibration. The voltage reference can be provided externally or internally using on-chip reference with embedded resistor string DAC.

Each configuration of the switched capacitor DC-DC converter can supply an output voltage lower than the no-load voltage (V_{NL}) which is equal to the input voltage multiplied by the gain setting [2]. Thus, the converter gain is selected based on the ratio of the reference to the input voltage as shown in Fig. 21.7.3b where the latter is applied to a resistor string to generate three intermediate volt-

age levels Vin/3, Vin/2, 2Vin/3. Dynamic comparators and gain select decoder are utilized to configure the converter for the proper gain. In order to minimize the power consumption of the gain selection block, NMOS footer switch N1 is used to avoid static power consumption in the resistor string. The control signals (GCtrl1, GCtrl2) of the gain selection block are generated internally using programmable timers. First GCtrl1 is applied to turn on the footer switch N1 as shown in Fig. 21.7.3b. The dynamic comparators are commanded to enter the evaluation mode using GCtrl2 after sufficient time that allows their negative input terminals to settle to the desired values. After the gain decoder block has stored the outputs of the comparators, the footer switch is turned off for power saving. The whole PMIC runs from the input supply and doesn't need any external voltage sources other than the reference in comparison with previous work [2,3] which required an external additional supply.

Figure 21.7.4a shows the measured efficiency of the PMIC versus the output voltage. The system achieves a peak efficiency of 93% including the control overhead while supplying 500µA at an output voltage of 0.963V and a peak of 92% while supplying 1mA. The SC DC-DC converter alone achieves a peak of 94% while supplying a load current of 500µA. An off-chip output capacitor of 10nF was utilized while performing the measurements. Figure 21.7.4b depicts the measured overall efficiency of the IC versus the output load current at the peak efficiency point while using a comparator clock of 8.2MHz. The control circuit power consumption impact the efficiency for load currents below 100µA which can be mitigated by scaling the comparator clock speed with the output load current [2]. Figure 21.7.5 shows the measured transient response of the system while stepping the reference from 0.95V to 0.45V. The output voltage tracks the reference voltage while gain hopping is performed from gain setting 2/3 to 1/3 to maximize the converter efficiency. Figure 21.7.6 shows a comparison of the performance of the PMIC presented to previously published work. The system is fabricated in 0.13µm CMOS and occupies an area of 600×610µm^2 as shown in Fig. 21.7.7.

The work advances the state of the art by achieving a bench mark for switched capacitor DC-DC converters with on-chip capacitors reporting a 93% peak efficiency including the control overhead which well exceeds all the previous reported work [3].

References:
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[2] Y. Ramadass and A. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," *IEEE Power Electronics Specialists Conference*, pp. 2353-2359, June 2007.
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[8] Y. Ramadass, *et al.*, "A 0.16mm² Completely On-Chip Switched-Capacitor Converter using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS," *IEEE ISSCC Dig. Tech. Paper,* pp. 208-209, Feb. 2010.
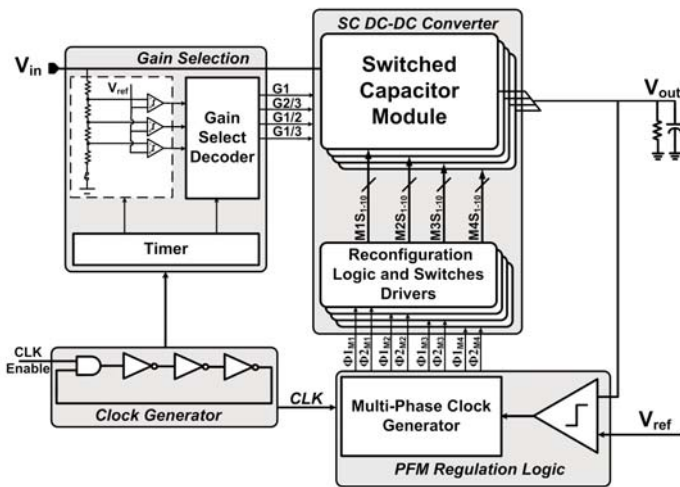
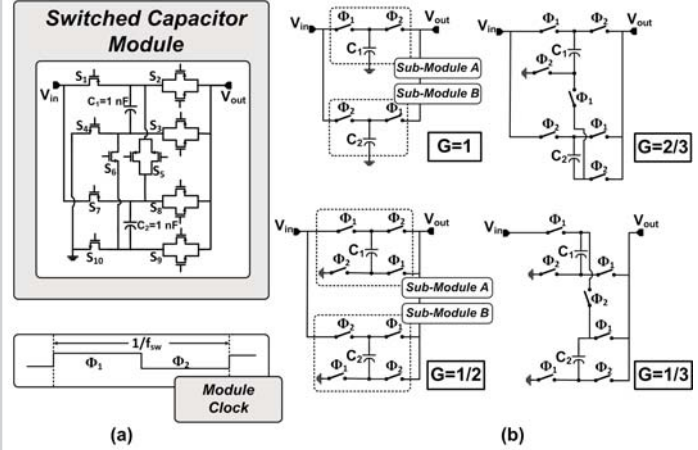Figure 21.7.1: Top level architecture of the Power Management IC (PMIC).

Figure 21.7.2: (a) Transistor level implementation of a single module of the switched capacitor (SC) DC-DC converter (b) Reconfiguration of the SC module for various gain settings (1,2/3,1/2,1/3).
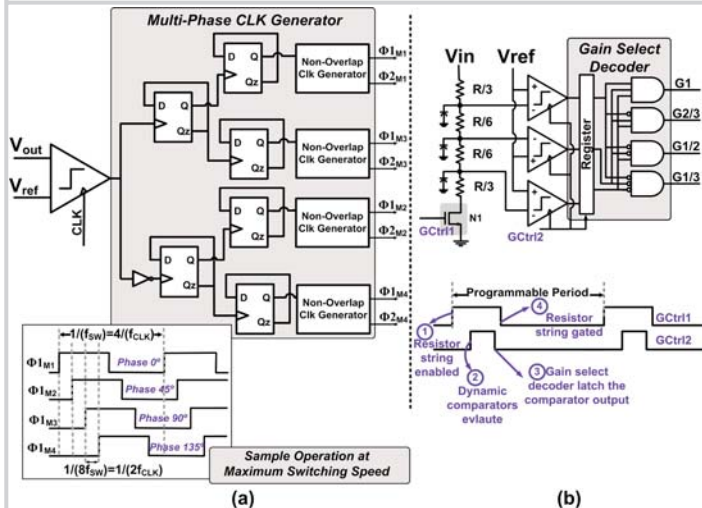

Figure 21.7.3: (a) Pulse Frequency Modulation (PFM) control logic for output voltage regulation of the multi-phased converter (b) Gain select block architecture and timing diagram.
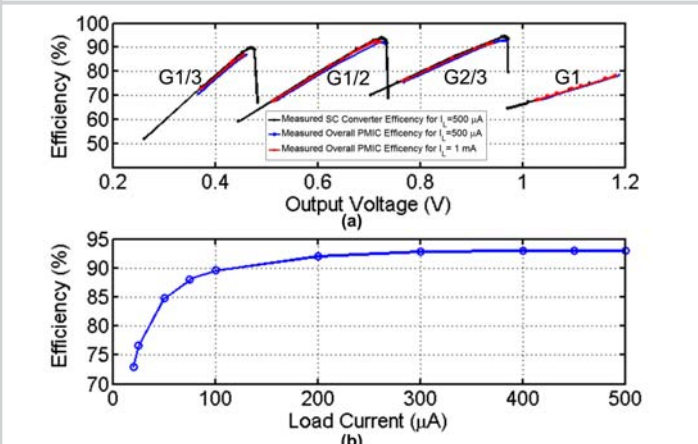

Figure 21.7.4: (a) Measured overall efficiency of the Power management IC (PMIC) while delivering 500µA and 1mA and measured efficiency of the switched-capacitor DC-DC converter alone while delivering 500µA. (b) Measured efficiency the PMIC versus load current while supplying an output voltage of 0.96V at a comparator clock of 8.2MHz.
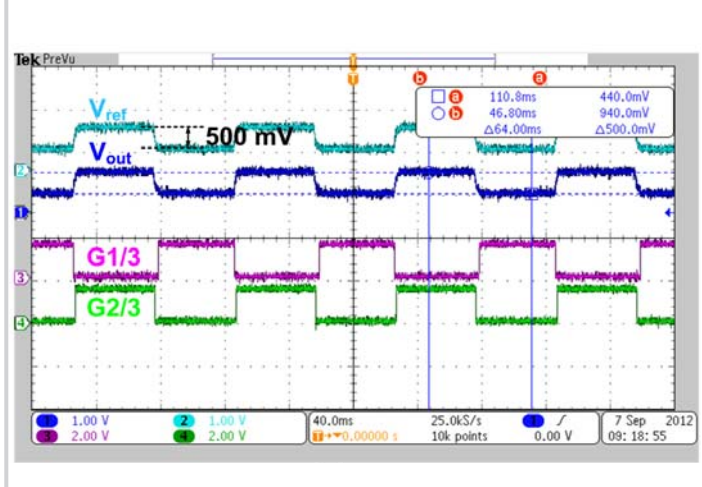

Figure 21.7.5: Measured load transient performance of the PMIC with a step in the reference voltage from 0.95 V to 0.45 V while showing the gain hopping from 2/3 to 1/3.

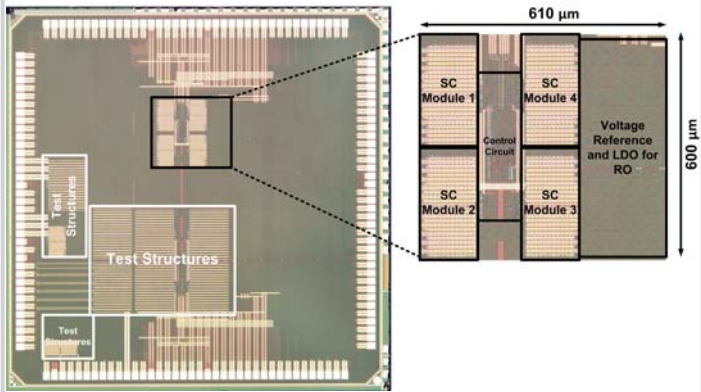| Design	G. Piqué ISSCC 2012 [3]	Y. Ramadass ISSCC 2010 [8]	L.Chang VLSI 2010 [5]	T. Breussegem VLSI 2009 [7]	This Work
Technology	90nm CMOS	45nm CMOS	45nm SOI	130nm CMOS	130nm CMOS
Chip Area	0.25 mm²	0.16 mm²	0.0012mm²	2.25 mm²	0.366mm²
Capacitor Type	Thin-gate MOS + fringe metal capacitors	Gate oxide	Deep trench cap	MIM	Ferroelectric
Vin	1.2-2 V	1.8 V	2 V	1.2-1 V	1.5 V
Vout	0.7 V	0.8-1 V	0.95 V	2.1- 1.8 V	0.4-1.1 V
Conversion Ratios	Step down 2/3-1/2	Step down 2/3	Step down 1/2	Step up 1:2	Step down 1-2/3-1/2-1/3
Output Current	8 mA	8mA	2.8mA	150µA to 2.2mA	20 µA to 1mA
Quoted Efficiency	81 %	69 %	90 %	82 %	93%

Figure 21.7.6: Performance summary and comparison.

Figure 21.7.7: Chip micrograph.