Electrical Study of Molybdenum in Silicon and Fluorinated SiO_2 for Interlayer Dielectrics

by

Jean Cagas

Submitted to the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degree of

Bachelor of Science

at the

Massachusetts Institute of Technology

June 1999

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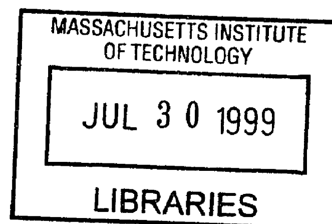
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ABSTRACT

Molybdenum is unintentionally introduced into silicon at various points in semiconductor processing. This introduction is a concern because molybdenum introduces a deep level state into the forbidden gap of silicon, degrading minority carrier lifetime. In this project, DLTS was used to measure the concentration of electrically active molybdenum. Temperature dependence was investigated by varying annealing temperature and keeping annealing time constant, and time dependence was studied by performing rapid thermal anneals at 750°C and varying annealing time. DLTS spectra were generated and isothermal depth profiles of trap concentration were found using additional data from C-V measurements. For a rate window of 35 ms, the molybdenum peak occurred at 165K. The energy level of molybdenum was 0.3eV and the capture cross section was $5.5 \times 10^{-16} cm^2$. At high temperatures, the diffusion behavior of molybdenum exhibited a Gaussian profile. At low temperatures, however, the profiles exhibited an initial kick-out mechanism followed by normal diffusion.

Fluorinated SiO_2 is becoming an extremely important material for intermetal dielectrics. As integrated circuits are scaling down in size, the RC constant is becoming the bottleneck to faster circuit speeds. The addition of fluorine decreases the dielectric constant of SiO_2 by decreasing the ionic and electronic polarizability of the entire structure. The addition of fluorine still has some detrimental effects, however, such as lower hardness and increased water adsorption. For this project, eight oxide films with varying fluorine content were studied. The dielectric constant K of each film was calculated with the saturation capacitance from C-V measurements, oxide thickness, and diameter. While all the observed values of K were lower than known values for pure SiO_2, they did not exhibit a decreasing trend. Possibly, processing conditions might have had more of a dominant effect for such small differences in fluorine content. From changing C-V profiles and fluctuating saturation capacitance, it is suggested that there was movement of charge in the oxide layers. However, this was not consistent for all the films.

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1 Introduction

The ability to control electrical properties of materials has been a necessity to the success of the semiconductor industry. The widespread use of silicon has been due to the abilities to control these properties through processing. In general, electrical properties of semiconductors can be altered either by the addition of shallow-level dopants or by the introduction of deep-level defects or impurities. In either case, the bonding structure of the native material is disturbed by the presence of the dopant or impurity resulting in a defect state in the forbidden gap of the energy band, as shown in Figure 1. (1) Therefore, it is desirable to be able to monitor the presence of dopants and impurities so that the altered electrical properties of the material can be known. One way in which this can be done is through junction capacitance measurements.

This project uses deep level transient spectroscopy (DLTS) along with current-voltage (I-V) and capacitance-voltage (C-V) measurements to study the diffusive behavior of ion-implanted molybdenum in silicon. I-V and C-V measurements are also used to examine the capacitance of MOS capacitors with silicon dioxide films of varying fluorine content. The motivation for these studies is described in later sections.

1.1 Junction Capacitance Measurements

Capacitance describes the ability of a material to store separated charge. The electric field that arises from the separation of charge exactly balances the electric field from the applied voltage. Although the capacitance of a material is often characterized in terms of its dielectric constant, actual capacitance will vary with dopant concentration, trap

concentration, and geometry of the capacitor. In order to carry out junction capacitance measurements, the sample studied must be some kind of junction with a space charge region. This can be a MOS capacitor, a Schottky diode, or an asymmetrically doped p-n junction. In addition, the capacitance measurement can be taken in the steady state or in the transient.

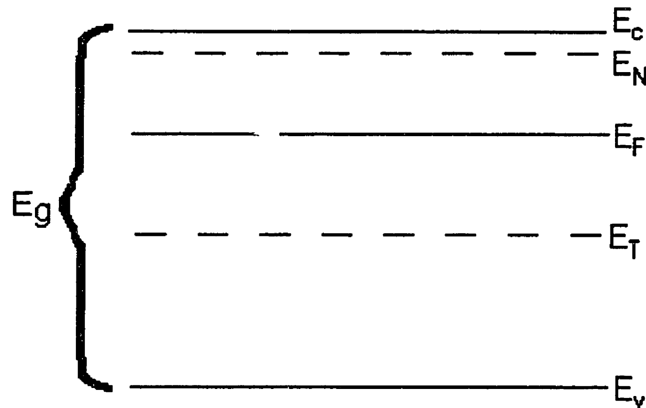


Figure 1: Band diagram of an n-type semiconductor. Note: the energy state of shallow-level dopants is closer to the conduction band than the deep-level traps.

1.1.1 Steady-state Capacitance

The parallel plate model, in which charge is stored on the surface of two plates and is separated by a distance filled with air or some dielectric, can be applied to the capacitance of semiconductors. In the case of a MOS capacitor, this distance would be the oxide thickness. In the case of a Schottky diode, which is illustrated in Figure 2, it would be the depletion width. However, the parallel plate model assumes that no conduction occurs between the plates. This condition is not always met in semiconductor structures, although there should be no significant current in either a MOS capacitor or a Schottky diode. I-V measurements can act as a preliminary check of the quality of the structure, ensuring a certain level of adherence to the assumptions of the model.

Given a parallel plate model, capacitance is given by the relation:

$$C = \frac{Q}{V} = \frac{K\varepsilon_0 A}{d} \qquad \text{(Eq. 1)}$$

where C is the measured capacitance, Q is the stored charge, V is the applied voltage, K is the dielectric constant, d is the width of the space charge region, and A is the area of the junction.

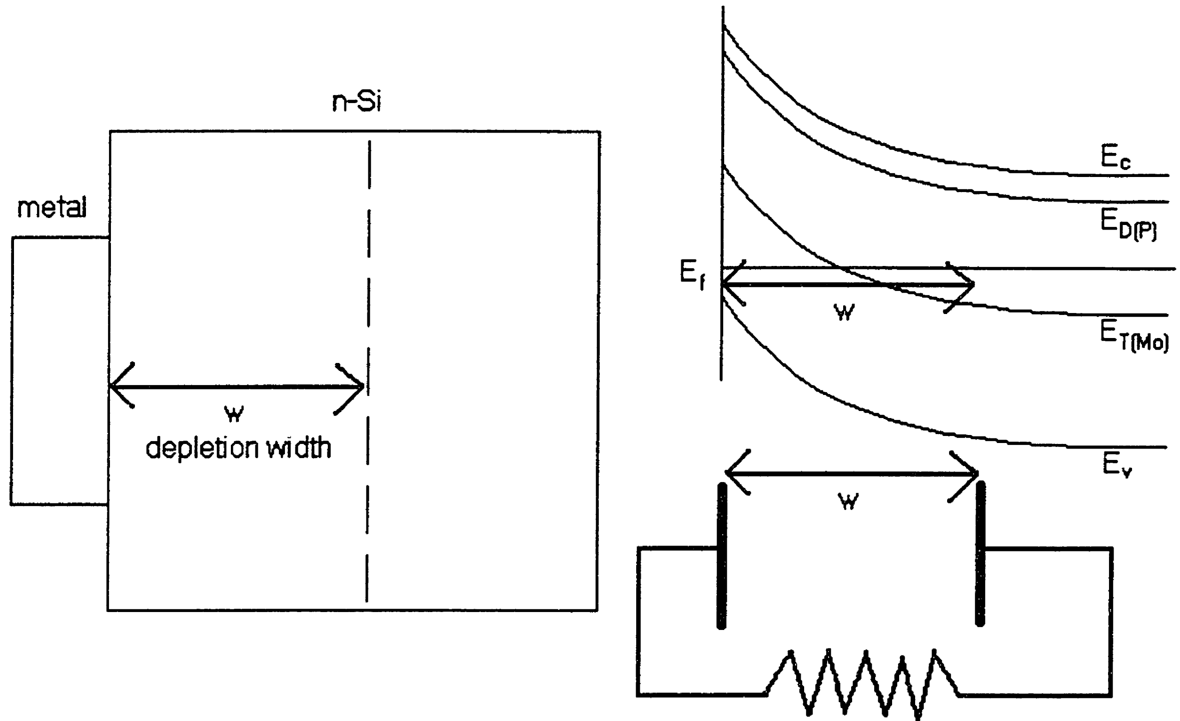


Figure 2: Schottky diode (left) with some depletion width w. Band diagram of Schottky diode (upper right) and parallel plate model (lower right).

In Schottky diodes and p-n junctions, the depletion width d is not constant and varies according to the equation:

$$d = \sqrt{\frac{2K\varepsilon_0 (V_b + V_0)}{qN}} \qquad \text{(Eq. 2)}$$

where V_b is the reverse bias voltage, V_0 is the built-in voltage, q is the charge of the electron, and N is the dopant concentration. (1) With Equations 1 and 2, the value of N can be extracted from the slope of a $1/C^2$ versus V graph, assuming that N is uniform.

If N is not uniform, then more complicated equations must be performed in order to extract N from a C-V measurement. Note in Equation 2 that as the bias voltage increases, the depletion width must also increase. This increase in depletion width must uncover enough additional charge to cancel out the increase in electric field. N can then be found as a function of depletion width and a junction profile of N can be obtained from the equation:

$$N(x) = -\frac{(C/A)^3}{q\varepsilon_0 K}\frac{\partial V}{\partial C} \tag{3}$$

It should be noted, however, that there is a natural limitation on the resolution of this profiling method which is given by the local Debye length. (1)

1.1.2 Transient Capacitance

As stated earlier, the addition of dopants or deep level impurities disturb the bonding structure of the native semiconductor, so the impurity introduces a defect state into the forbidden gap of the energy band. As shown in Figure 1, shallow level defect states are close to their related energy band while deep level states are farther away from their related energy band. Since the difference between the related energy band and the shallow level is small, there is enough thermal energy at room temperature to excite carriers at the shallow level to the energy band. There is not enough thermal energy to excite carriers from the deeper levels. Therefore, dopants are usually ionized and do not

contain carriers at normal temperatures while deeper levels act as carrier traps and recombination centers. Shown in Figure 3, traps are those levels that capture more of one type of carrier (either holes or electrons) while recombination centers capture both types of carriers.

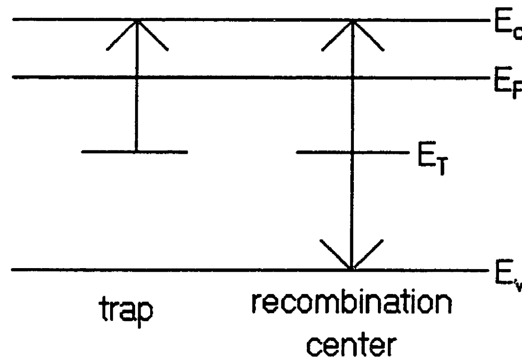


Figure 3: Electron trap and recombination center. Traps interact with one type of carrier while recombination centers interact with both types of carriers.

These traps are responsible for the transient capacitance response. Through transient capacitance measurements, deep level transient spectroscopy (DLTS) observes the emission processes of these traps, which can only be detected by forcing the introduction of carriers to be captured. First, a reverse bias is applied to the junction in order to establish dominant space charge conditions. A slight forward bias pulse collapses the depletion width; making carriers available for capture by traps. The duration of the pulse is long enough for the traps to become filled. When the pulse is released, the concentration of carriers held by traps in the depletion region thermally decays. This decay is observed as the transient capacitance response and DLTS measures this response in terms of a difference in capacitance at some time interval. This is illustrated in Figure 4.

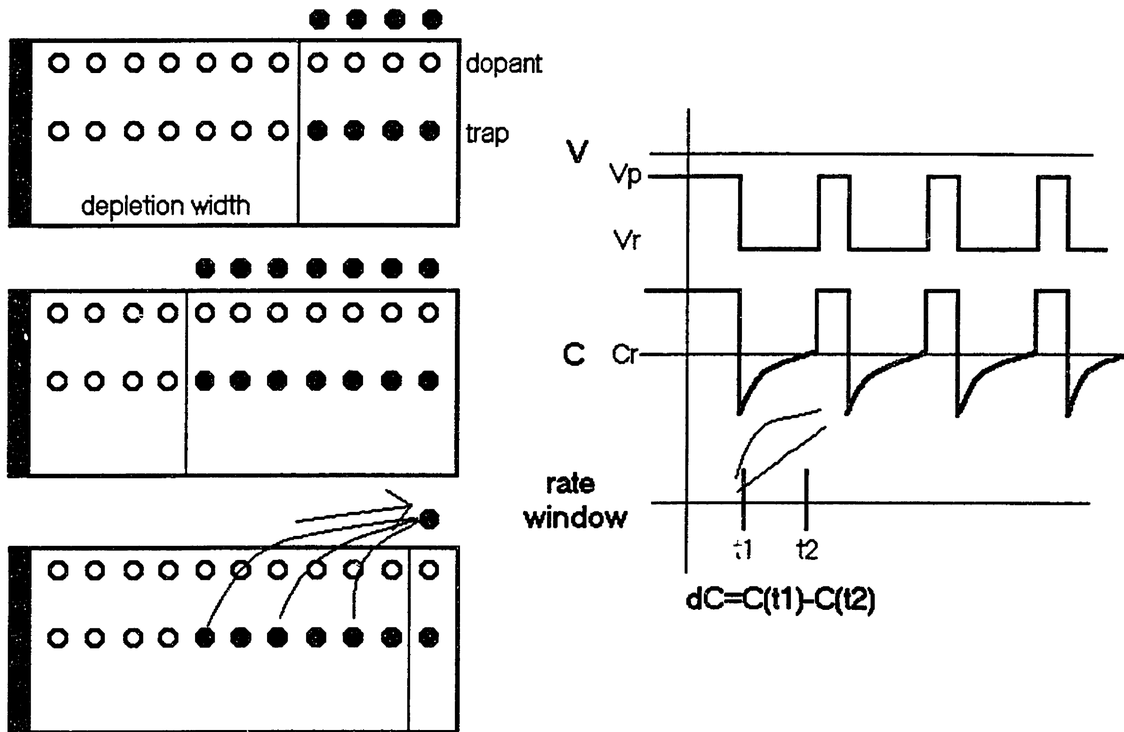


Figure 4: Left: Semiconductor junction during DLTS pulsing. When the bias is pulsed, carriers fill the previously depleted region. When the pulse is removed, the carriers are thermally emitted. Right: (top) Voltage and capacitance during DLTS pulsing. Note the exponential decay between pulses. (bottom) The rate window is determined by t1 and t2.

Since carrier emission is a thermal process, the emission rate will vary with temperature and reach some maximum for a given time interval (or rate window). This rate window technique generates a spectrum, from which the capture cross section and the activation energy can be extracted. (1, p. 417) The emission of electrons, for example, from a trap would vary according to the relation:

$$e_n = \sigma_n \langle v_n \rangle N_c \exp\left(\Delta E / kT\right) \qquad \text{(Eq. 4)}$$

where e_n is the emission rate, σ_n is the trap's capture cross section, $\langle v_n \rangle$ is the average thermal velocity of electrons, N_c is the effective density of states in the conduction band, and ΔE is the activation energy of the defect state. If an Arrhenius plot of log e versus 1/T

is constructed, the activation energy can be extracted from the slope and the capture cross section can be extracted from extrapolation to where 1/T=0. (1) This is shown if Figure 5.

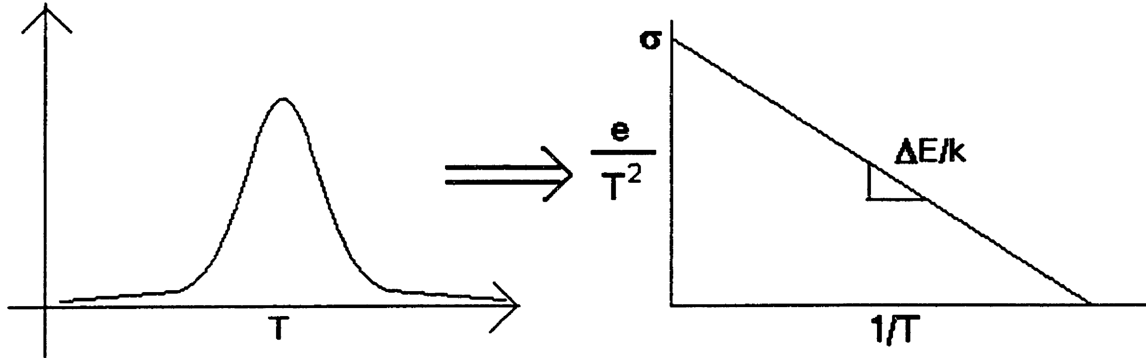


Figure 5: Left: DLTS spectrum. Right: Arrhenius plot constructed from DLTS spectrum.

It should also be noted that the reverse bias determines the depth of detection, and the pulse height determines the detection volume, as shown in Figure 6. This concept, coupled with C-V measurements, can be made the basis for depth profiling of trap concentrations at the peak temperature. Isothermal profiling can be performed by keeping reverse bias constant and varying pulse voltage, keeping pulse voltage constant and varying reverse bias, or by just keeping pulse height constant. These methods result in incremental changes in capacitance, which are related to the trap concentration by the equation:

$$\delta\left(\Delta C/C\right)=\left(\frac{\varepsilon_0 K}{qd^2N^+}\right)\frac{N_T(x)}{N^+(x)}\delta V \qquad \text{(Eq. 5)}$$

where $\delta(\Delta C/C)$ is the incremental change in relative capacitance, d is the depletion layer width, $N_T(x)$ is the trap concentration and N^+ is the dopant concentration at the edge of the depletion layer. (1)

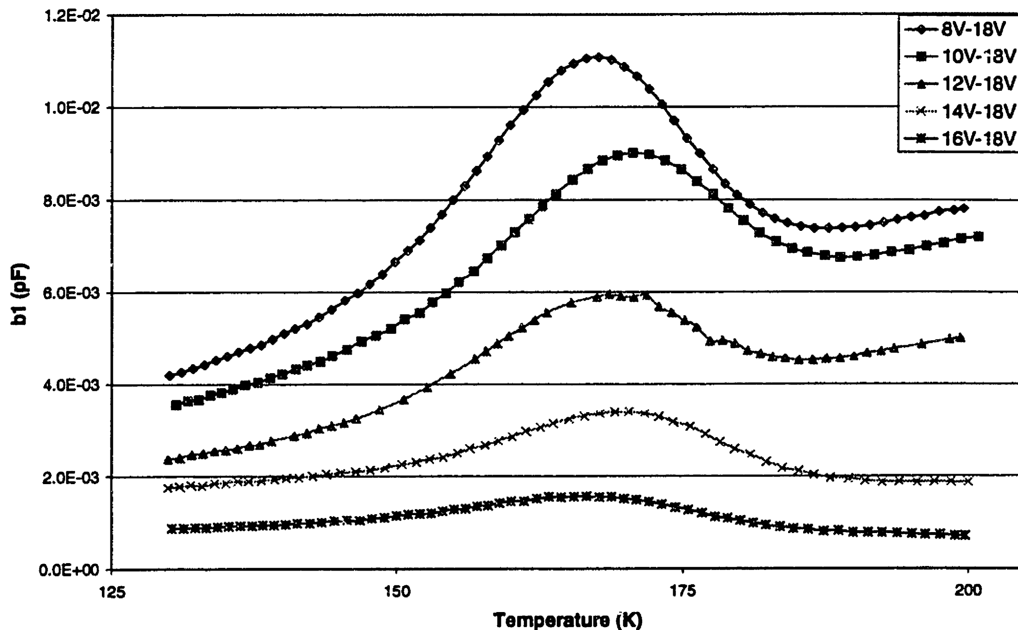


Figure 6: DLTS Spectra with constant reverse bias and decreasing pulse height. As pulse height decreases, the detection volume (and therefore the magnitude of the signal) decreases.

The primary advantage of DLTS is that it has extremely sensitive detection limits. However, because trap concentration is detected as a fraction of the dopant concentration, these limits will be less sensitive for heavily doped materials. (1) One disadvantage of DLTS is that there is no distinction between positive and negative charges in the signal, so the effect on majority carriers cannot be distinguished from the effect on minority carriers in p-n junctions. In Schottky diodes, however, injection of minority carriers into the semiconductor does not occur, so the effect on majority carriers can be isolated. (2)

2 Molybdenum in Silicon

2.1 Background

Molybdenum is unintentionally introduced into silicon at various points in semiconductor processing. For example, during ion implantation of BF_2, the mass analyzer magnet cannot distinguish between the ions $^{11}B^{19}F_2^{+}$ and $^{98}Mo^{2+}$. Because both species have the same charge-to-mass ratio, both ions are implanted. Molybdenum is also thought to be introduced during CVD, since it is a component in stainless steel CVD susceptors. (3, 4) Furthermore, molybdenum is used in industry as a high temperature component in crystal growth and heat treating equipment, and it is used as an interconnect material and as a gate electrode in devices. Molybdenum contamination is a concern in semiconductors because it introduces a deep level impurity into the energy band, thereby decreasing carrier lifetime in the bulk. It is a concern for any application in which carrier lifetime is important such as p-n junctions, and in fact, molybdenum has been shown to degrade the performance of solar cells. (4-6) More study is required in this area because little is known at this point about the diffusive behavior of molybdenum, except that its diffusion may depend on the presence of defects. In addition, it has been documented that molybdenum has a temperature-independent hole capture cross section. (3)

2.2 Experimental Procedure

P-type samples of float-zone (FZ) silicon were ion implanted with $1.3 \times 10^{11}/cm^2$ molybdenum at 50keV. The samples were supplied by Bell Labs. Two types of anneals were performed on the samples. One anneal was for 30 minutes at 750°C, 850°C, and

950°C. The other type was a rapid thermal anneal at 750°C for 10 seconds, 160 seconds, and 640 seconds. After the samples had undergone an organic clean and an oxide etch, circular titanium contacts were deposited onto the samples to form Schottky diodes. I-V measurements were performed at room temperature to check the quality of the diodes, and DLTS spectra were found for each sample. Suitable diodes had leakage currents below 10 microamps. I-V and C-V measurements were then taken at the peak temperature, and isothermal profiling was performed keeping reverse bias constant and changing the pulse voltage. DLTS measurements were performed on a Bio-Rad 8000 using a period width of 35 milliseconds. Depth profiles were compared to data simulated on Trim software.

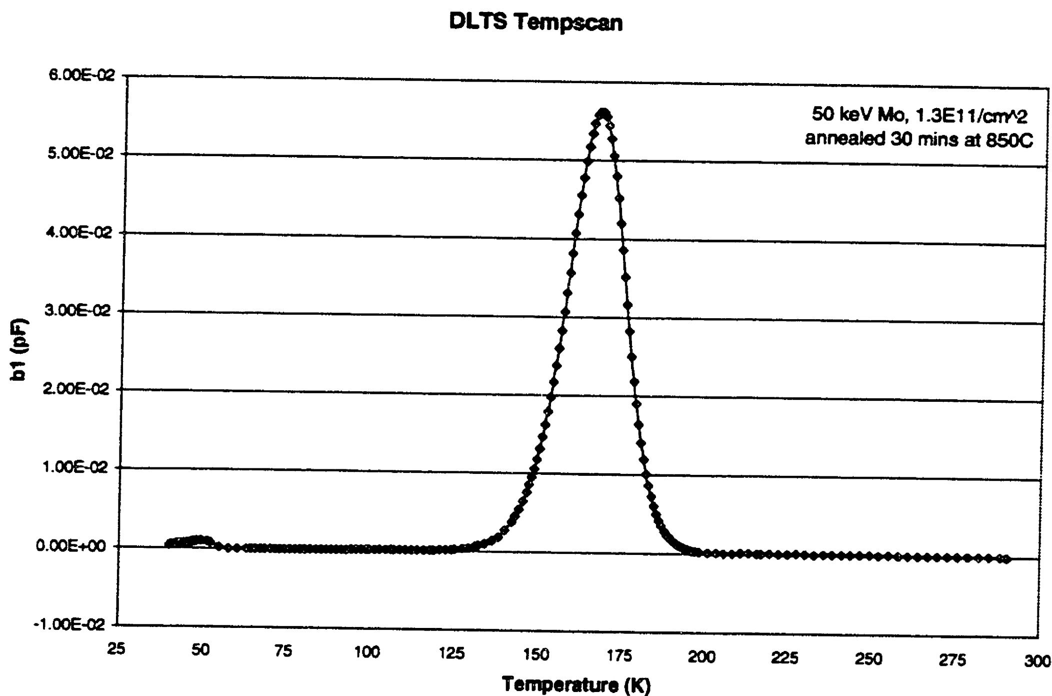


Figure 7: Representative DLTS spectra: sample annealed at 850°C for 30 minutes

2.3 Results

The DLTS spectra show that for a period width of 35 ms, molybdenum peak occurs around 165K. Isothermal depth profiling of trap concentration was calculated by Equation 5. A representative DLTS spectrum is shown in Figure 7. The depth trap profiles are shown in Figure 8. Figure 9 shows simulated trap profiles for normal (Gaussian) diffusion and the kick-out mechanism. The capture cross section of molybdenum was found to be $5.5x10^{-16}cm^2$ and its activation energy was found to be 0.3 eV.

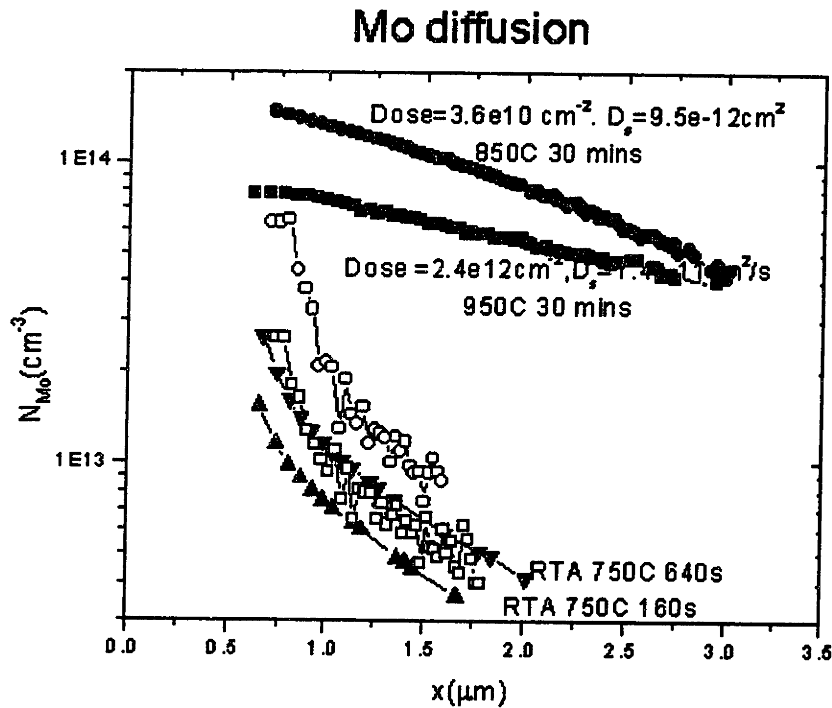


Figure 8: Depth profiles of molybdenum traps for samples annealed for 30 minutes at 850°C and 950°C, and RTA at 750°C for 160 seconds and 640 seconds.

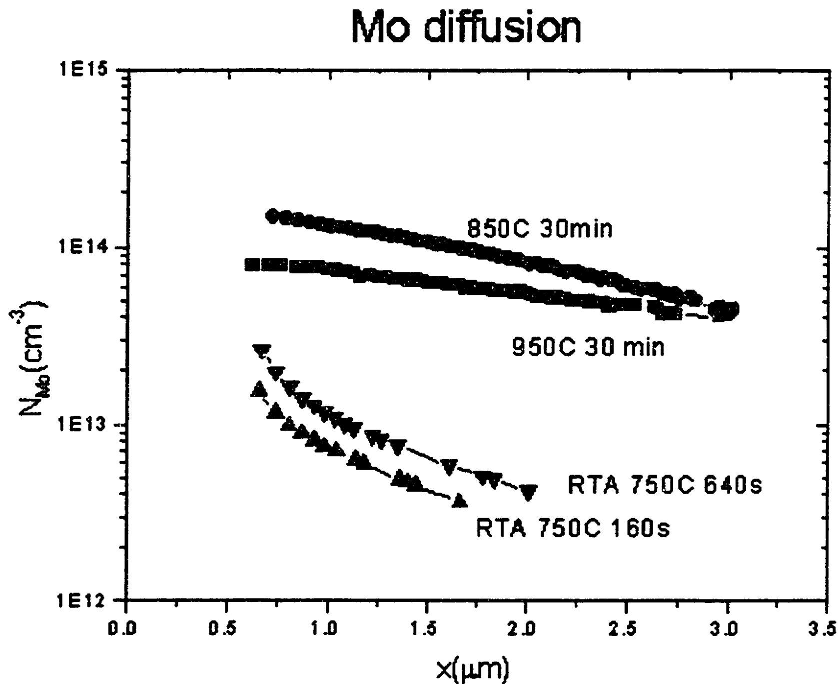
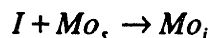


Figure 9: Simulated diffusion profiles of molybdenum in silicon 30 minute anneals at 850°C and 950°C, and RTA at 750°C for 160 seconds and 640 seconds

2.4 Discussion

Small differences in the actual peak temperatures of the DLTS spectra are attributed to temperature gradients existing within the Bio-Rad chamber. At 850°C and 950°C, the diffusion profiles appeared Gaussian. The diffusion constant D was $9.5x10^{-12}cm^2/s$ at 850°C and $1.4x10^{-11}cm^2/s$ at 950°C. Either substitutional or interstitial-substitutional exchange mechanisms could have been responsible for Gaussian profiles. At 750°C, the diffusion profiles of ion-implanted silicon suggest an initial kick-out mechanism. In this case, interstitial silicon kicks out substitutional molybdenum into the interstitial site:



$$I + Mo_s \rightarrow Mo_i$$

This interstitial molybdenum then diffuses fast. The self-interstitials were generated by the molybdenum ion implantation. Once these self-interstitials were gone, normal diffusion is observed.

2.5 Conclusion

Deep level molybdenum traps were studied in this experiment in order to observe its diffusive behavior. For a period width of 35 ms, the spectrum peak was observed to occur around 165K. Slight differences in this peak temperature are most likely due to temperature gradients existing within the Bio-Rad chamber. The capture cross section and energy level of molybdenum were found, and depth profiling of the trap was performed. These profiles show that when annealed at higher temperatures (850°C and 950°C), molybdenum diffusion followed a Gaussian distribution (from which diffusion constants were calculated). For samples annealed at lower temperature (750°C), the profiles showed an initial kick-out mechanism followed by normal diffusion.

3 Fluorinated SiO_2 for Interlayer Dielectrics

3.1 Background

Scaling down of circuits has resulted in increased circuit speed and faster switching times. However, the RC product is becoming the bottleneck to further increases in speed. (7) Going back to the parallel-plate model, the RC time constant is the time required for the plates to charge and discharge. In circuits, it describes the signal propagation delay time. (8) Decreasing interconnect dimensions increases signal delay time, power consumption, and cross talk. Two ways to combat the increase in RC are either to choose metals with a lower resistivity, such as copper, or to decrease the capacitance of the dielectric material. One material currently being studied for this latter purpose is fluorinated SiO_2. (7) Of all the dielectrics being studied, fluorinated SiO_2 or fluorosilicate glass (FSG) is probably the most easily used since it can be deposited with existing CVD techniques. (9)

The addition of fluorine decreases the dielectric constant of SiO_2 because it reduces the ionic and electronic polarizability of the material. The high electronegativity of fluorine causes a shift of electrons toward fluorine. The effect on Si-O bonds is a decrease in bond length and a weakening of bond strength. As a result, the Si-O bond angles change, and the complete structure is less polarizable. In addition, the fluorine acts as a network modifier, as shown in Figure 10. This leads to a lower density, which further decreases the capacitance of the film, but density will depend also on processing conditions. (7)

The addition of fluorine to SiO_2 also has some undesirable effects. Because fluorine breaks up the Si-O network, the resulting film often has a lower hardness. Fluorine also

acts as an adsorption site for water. This degrades device performance for two reasons. First, water has an extremely high dielectric constant of about 83. Second, it is highly reactive with fluorine at high temperatures. This reaction can cause loss of fluorine, making the device less stable. (7)

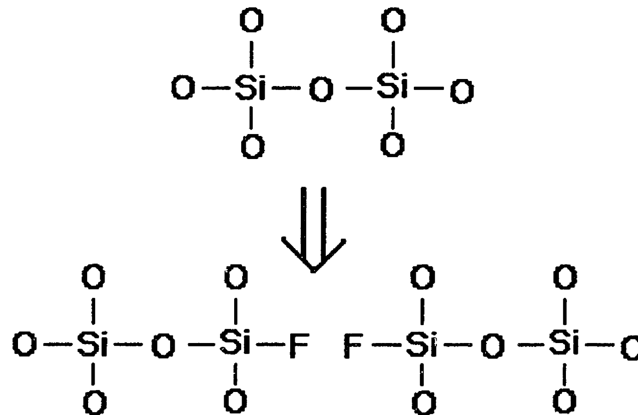


Figure 10: Addition of fluorine to SiO_2. Fluorine breaks up the Si-O network by substituting for oxygen. (Two fluorine atoms substitute for one oxygen atom.)

The capacitance-voltage curves of MOS capacitors are studied in this experiment and have three regimes, which are shown in Figure 11. In the accumulation region, majority carriers are accumulated in the semiconductor in order to balance out the applied voltage. The capacitance in this region is determined by the thickness of the oxide. In the depletion region, the capacitance decreases as the depletion layer forms and widens. In the inversion region, the portion of semiconductor near the oxide interface is inverted. In p-type silicon, this would mean that a channel of n-type silicon forms. Capacitance is then determined by both the oxide capacitance and the capacitance associated with the depletion layer. The exact shape of the C-V curve depends on the measurement frequency, the number of interface charges, and the presence of mobile or fixed charges in the oxide. (2)

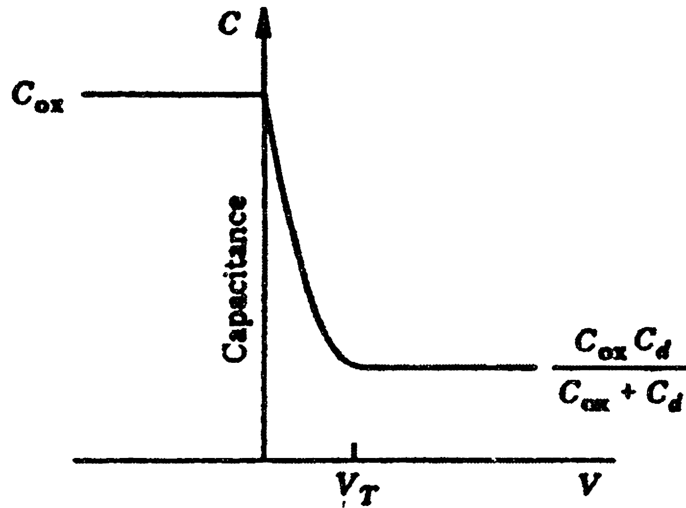


Figure 11: C-V profile of an MOS structure. At the accumulation region (left), capacitance is determined by the capacitance of the oxide layer. Capacitance decreases in the depletion region (middle). In the inversion region (right), capacitance is determined by both the oxide capacitance and the capacitance associated with the depletion layer. Figure taken from Mayer & Lau, (2).

3.2 Experimental Procedure

Experiments were performed on wafer samples with eight different films of varying fluorine content. Thickness measurements were taken at nine points on each wafer. The wafers were supplied by Applied Materials. Nine samples were cut from each wafer (corresponding to the positions of the nine thickness measurements). Circular aluminum contacts were evaporated onto the samples to form MOS structures. I-V measurements were performed to check the structure quality. (Again, suitable samples had leakage currents less than 10 µA.) C-V measurements were performed on two structures of each sample, and the diameter of each contact was then measured.

The dielectric constants K of the films were calculated by rearranging equation 1:

$$K = \frac{Cd}{\varepsilon_0 A} \qquad (1)$$

where C was the saturation capacitance taken from the accumulation region, d is the thickness of the oxide, and A was the area of the contact calculated from the diameter measurements.

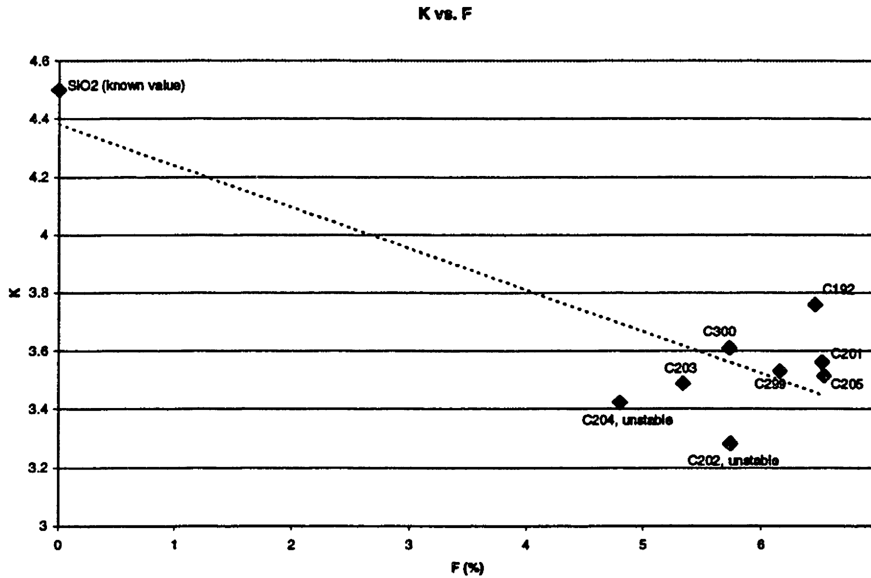


Figure 12: Observed K values for oxide films with varying fluorine content. Data points are labeled with their wafer ID.

3.3 Results

The dielectric constants of the films were lower than known values for SiO_2. The values of K ranged from 3.3 to 3.8 and are shown in Figure 12. The electrical stability of the films also varied slightly in that some films exhibited fluctuation capacitance values. Specifically, the T192 film was the most stable (exhibited the least fluctuation) while the C202 film was the least stable (exhibited the most fluctuation). However, the C202 film also had the lowest K, 3.3. The lowest K for the stable films was 3.5. In addition, it was

observed that the C-V behavior of the films changed after exposure to high voltages. An example of this is shown in Figure 13.

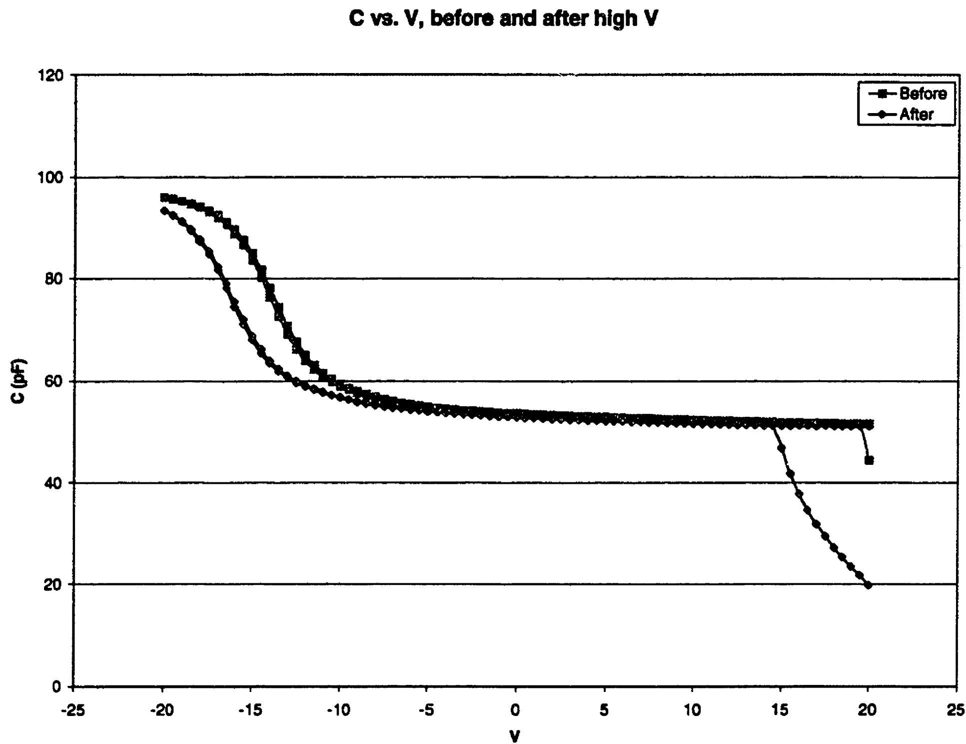


Figure 13: C-V behavior of a MOS structure using film T192. Note that there is a shift in the threshold voltage after exposure to high voltages.

3.4 Discussion

The fluorinated oxide films had a lower dielectric constant K than pure SiO_2, but there did not appear to be a decreasing trend among the observed values. The differences in fluorine content were very small, however, and at such small differences processing factors might have had more dominant effects. The changes in C-V behavior after exposure to

high voltage probably was caused by the (permanent) movement of charged species within the oxide. Instability of the films was most likely due to oscillation of charges in the oxide.

3.5 Conclusion

The C-V profiles of fluorinated SiO_2 films were studied in this experiment. While the observed values of K were smaller than known values for pure SiO_2, they did not exhibit a decreasing trend. Considering that the differences in fluorine content were so small, processing factors most likely had a more dominant effect on K than the fluorine content. The movement of charged species was also observed in the oxide films in the fluctuation of capacitance and the more permanent change in C-V behavior after exposure to high voltages.

4 Summary

Molybdenum is unintentionally introduced into silicon at various points in semiconductor processing. This introduction is a concern because molybdenum introduces a deep level state into the forbidden gap of silicon, degrading minority carrier lifetime. In this project, DLTS was used to measure the concentration of electrically active molybdenum. Temperature dependence was investigated by varying annealing temperature and keeping annealing time constant, and time dependence was studied by performing rapid thermal anneals at 750°C and varying annealing time. DLTS spectra were generated and isothermal depth profiles of trap concentration were found using additional data from C-V measurements. For a rate window of 35 ms, the molybdenum peak occurred at 165K. The energy level of molybdenum was.3eV and the capture cross section was $5.5x10^{-16}cm^2$. At high temperatures, the diffusion behavior of molybdenum exhibited a Gaussian profile. At low temperatures, however, the profiles exhibited an initial kick-out mechanism followed by normal diffusion.

Fluorinated SiO_2 is becoming an extremely important material for intermetal dielectrics. As integrated circuits are scaling down in size, the RC constant is becoming the bottleneck to faster circuit speeds. The addition of fluorine decreases the dielectric constant of SiO_2 by decreasing the ionic and electronic polarizability of the entire structure. The addition of fluorine still has some detrimental effects, however, such as lower hardness and increased water adsorption. For this project, eight oxide films with varying fluorine content were studied. The dielectric constant K of each film was calculated with the saturation capacitance from C-V measurements, oxide thickness, and diameter. While all the

observed values of K were lower than known values for pure SiO_2, they did not exhibit a decreasing trend. Possibly, processing conditions might have had more of a dominant effect for such small differences in fluorine content. From changing C-V profiles and fluctuating saturation capacitance, it is suggested that there was movement of charge in the oxide layers. However, this was not consistent for all the films. Future work in this area may involve correlating processing parameters with the observed K values and the electronic stability of the films.

5 Acknowledgments

I would like to acknowledge Mr. Sang Ahn for his contributions and guidance throughout this project and Professor Lionel Kimerling for allowing me the opportunity to work on this project. I would also like to thank Janet Benton at Bell Labs and Dr. Hichem Ma'saad at Applied Materials for their collaboration and for supplying the samples which were used in this project.

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