Graphene for Radio Frequency Electronics and Infrared Thermal Imaging

by

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Abstract

The aim of this thesis is two-fold: The first is to develop a reliable processing technology for CVD graphene devices for applications in graphene circuits, i.e. mixers, frequency multipliers and phase key shifters. The performance of current graphene circuits has been limited to below 1.5 GHz due to issues with contact resistances and materials quality. Through improved processing techniques and studies about interface preparation between graphene and metal contacts - we demonstrate improved graphene-metal interactions to allow for CVD-graphene based circuits operating at >10 GHz. The second part of this thesis involves exploring graphene as a new infrared photoactive and thermally sensitive material for sensors in the IR spectrum (80 meV $< E_{ph} <$ 250 meV), which have applications ranging from thermography and night vision systems to nanoscale chemical spectroscopy. In this thesis, we will focus on graphene's intrinsic detection mechanisms at much lower photon energies ($\sim$ 125 meV) and resolve experimentally the dominant infrared detection mechanism in graphene. We find in the infrared that graphene's electronically tunable Seebeck Coefficient ($\sim$50-100 μV/K) dominates at very low photon energies making graphene suitable as a nanoscale thermal detector. Utilizing this design concept, we discuss graphene's suitability for infrared imaging, as well as, other thermal applications such as low cost transparent temperature sensors.

Thesis Supervisor: Tomás Palacios
Title: Associate Professor

Thesis Supervisor: Jing Kong
Title: Associate Professor

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While the journey at the end of the Ph.D. is a solitary one, the process is far from it. From family, friends, and colleagues, my Ph.D. has been the culmination of help from everyone around me and I'd like to take this opportunity to thank everyone.

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Chapter 1

Introduction

Layered materials such as graphite, molybdenum disulfide, hexagonal boron nitride, are common materials that can be found in our everyday lives ranging from cosmetics to dry lubricants [19, 20]. While much experimental, as well as, theoretical work has been done on these materials in the past in their bulk phase [21–26], it has been their recent single layer isolation [27] and their new-found electrical properties at the single atomic layer scale that has rejuvenated research interest in these and many other layered materials. The material that has triggered this exploration of two-dimensional (2D) materials by many research groups around the world, as well as in this thesis, has been that of monolayer graphite or graphene, which garnered the Nobel Prize in 2010 [28]. As a single atomic layer of material, graphene has demonstrated amazing material properties: ultra-high carrier mobility ($>$200,000 $cm^2V^{-1}s^{-1}$) [29], large mechanical strength (55 N/m) [30], room temperature quantum hall effect [31], long range ballistic transport [32], and tunable optical absorption [33]. In addition, due to its unique band structure, analogues between condensed matter physics and relativistic physics can be studied in a single material. With all of these amazing properties, graphene has inspired both engineers and physicists alike to imagine new applications for such a unique material. Technologically, graphene's allotrope of the carbon nanotube has been around for decades with many of its own amazing properties [34–41]; however, the planar configuration of graphene has greatly simplified both the patterning and placement of this material such that conventional planar fabrication processes

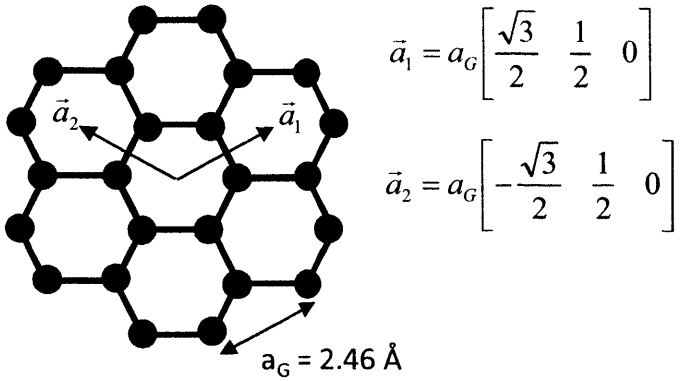

Figure 1-1: Lattice Structure of Graphene

can be made compatible. This thesis aims to show contributions to the field by developing the technology of graphene from both a materials, as well as, a processing perspective with aims towards large area applications. Utilizing this technology, we aim to explore some unique applications for graphene for both high speed electronics as well as infrared/thermal imaging applications.

1.1 Graphene Theory

1.1.1 Band Structure

Graphene, as mentioned earlier, is a two-dimensional material composed of a hexagonal arrangement of sp^2 bonded carbon atoms as shown in Figure 1-1, where $\vec{a_1}$ and $\vec{a_2}$ compose the basis vectors of the Bravais lattice. Following Wallace [21] using a standard tight binding approach and using a linear combination of atomic orbitals (LCAO), we can derive graphene's electronic bandstructure. Following from Schrödinger's Equation for a single electron model(Eq. 1.1),

$$\left[-\frac{\hbar^2\nabla^2}{2m_0} + V(\vec{r})\right]\psi(\vec{r}) = E\psi(\vec{r}) \tag{1.1}$$

where E is the energy of the electron, m_0 is the mass of an electron, $\hbar$ is Planck's constant, ψ is the wavefunction of the electron, $\vec{r}$ is position, and V is the spatial potential. Since we are sitting inside of a crystal, as a first approximation (using an LCAO approach), we make an estimate that the wavefunction of the electron inside the crystal is composed of a superposition of atomic orbitals centered at each lattice site (Eq. 1.2).

$$\psi(\vec{r}) = \sum_{\vec{R}} \sum_{i=1}^{m} c_i[\vec{R}]\phi_i(\vec{r}+\vec{R}) \tag{1.2}$$

where ϕ is the atomic orbital at each lattice site, and $\vec{R} = n_1\vec{a_1} + n_2\vec{a_2}$ where n_1 and n_2 are integers, and c_i is a scalar weighting factor for each atomic orbital. If we assume that the potential takes the form $V(\vec{r}) = V_0(\vec{r}) + \sum_{\vec{R}\neq 0} V_0(\vec{r}+\vec{R})$, where V_0 is the potential associated with the atomic orbital, we can rewrite Schrödinger's Equation (Eq. 1.3) as:

$$[H_0 + \Delta V] \sum_{\vec{R}} \sum_{i=1}^{m} c_{il}[\vec{R}]\phi_i(\vec{r}+\vec{R}) = E_l \sum_{\vec{R}} \sum_{i=1}^{m} c_{il}[\vec{R}]\phi_i(\vec{r}+\vec{R}) \tag{1.3}$$

where we have defined $H_0 = -\frac{\hbar^2\nabla^2}{2m_0} + V_0(\vec{r})$ as the atomic orbital Hamiltonian and $\Delta V = \sum_{\vec{R}\neq 0} V_0(\vec{r}+\vec{R})$ as a perturbation to the original atomic orbital's Hamiltonian due to the interaction with all of the neighboring lattice sites. Utilizing orthogonality between basis wavefunctions, we can write an expression for all the weighting coefficients (Eq. 1.4)

$$\sum_{\vec{R}} \sum_{i=1}^{m} \langle \phi_j(\vec{r}) | H_0 + \Delta V | \phi_i(\vec{r}+\vec{R}) \rangle c_{il}[\vec{R}] = E_l \sum_{\vec{R}} \sum_{i=1}^{m} c_{il}[\vec{R}] \langle \phi_j(\vec{r}) | \phi_i(\vec{r}+\vec{R}) \rangle \tag{1.4}$$

Due to the periodicity of the crystal, we can assume that the probability of finding an electron on each lattice site is equal; however, their weighting coefficients may only differ in phase (Eq. 1.5), where we introduce $\vec{k}$ as the crystal momentum vector.

$$c_{il}[\vec{R}] = c_{il} e^{i\vec{k}\cdot\vec{R}} \tag{1.5}$$

Combining Equation 1.4 and 1.5, we have a general expression for computing the eigenstates for a single electron in graphene's crystal lattice (Eq. 1.6).

$$\sum_{\vec{R}}\sum_{i=1}^{m}\langle\phi_j(\vec{r})|H_0+\Delta V|\phi_i(\vec{r}+\vec{R})\rangle c_{il}e^{i\vec{k}\cdot\vec{R}} = E_l\sum_{\vec{R}}\sum_{i=1}^{m}c_{il}e^{i\vec{k}\cdot\vec{R}}\langle\phi_j(\vec{r})|\phi_i(\vec{r}+\vec{R})\rangle \quad (1.6)$$

To illustrate more clearly how to compute the actual energies, we write this in a matrix form (Eq 1.7)

$$\begin{bmatrix} H_{1,1} & \cdots & H_{1,m} \\ \vdots & \ddots & \vdots \\ H_{m,1} & \cdots & H_{m,m} \end{bmatrix} \times \begin{bmatrix} c_1 \\ \vdots \\ c_m \end{bmatrix} = E \begin{bmatrix} N_{1,1} & \cdots & N_{1,m} \\ \vdots & \ddots & \vdots \\ N_{m,1} & \cdots & N_{m,m} \end{bmatrix} \times \begin{bmatrix} c_1 \\ \vdots \\ c_m \end{bmatrix} \quad (1.7)$$

where $H_{i,j} = \sum_{\vec{R}}\langle\phi_i(\vec{r})|H_0+\Delta V|\phi_j(\vec{r}+\vec{R})\rangle e^{i\vec{k}\cdot\vec{R}}$ and $N_{i,j} = \sum_{\vec{R}}\langle\phi_i(\vec{r})|\phi_j(\vec{r}+\vec{R})\rangle e^{i\vec{k}\cdot\vec{R}}$. If we assume a two atom basis of carbon p_z orbitals and only nearest neighbor interactions, Equation 1.7 reduces to a much simpler form (Eq. 1.8)

$$\begin{bmatrix} E_z - E & V_{pzpz}\left(1+e^{i\vec{k}\cdot\vec{R_1}}+e^{i\vec{k}\cdot\vec{R_2}}\right) \\ V_{pzpz}\left(1+e^{i\vec{k}\cdot-\vec{R_1}}+e^{i\vec{k}\cdot-\vec{R_2}}\right) & E_z - E \end{bmatrix} \times \begin{bmatrix} c_A \\ c_B \end{bmatrix} = 0 \quad (1.8)$$

where $\vec{R_1} = -\vec{a_1}$ and $\vec{R_2} = -\vec{a_1}+\vec{a_2}$ are the two nearest neighbors and $V_{pzpz} = \langle\phi_A(\vec{r})|\Delta V|\phi_A(\vec{r}+\vec{R_1})\rangle = \langle\phi_A(\vec{r})|\Delta V|\phi_A(\vec{r}+\vec{R_2})\rangle$ is the overlap integral, which according to many experimental works is approximately 2.5-3.0 eV [42]. The solution to equation 1.8 yields the energy (E) versus crystal momentum ($\vec{k}$) relationship (Eq. 1.9), which is plotted in Figure 1.2 (a), where $E_z = 0$.

$$E = E_z \pm V_{pzpz}|1+e^{i\vec{k}\cdot\vec{R_1}}+e^{i\vec{k}\cdot\vec{R_2}}| \quad (1.9)$$

Because of this hexagonal arrangement of atoms and the symmetric two atom carbon p_z basis, there exists crystal momentum wave vectors ($\vec{k}$) where the conduction and valence band of graphene are degenerate with respect to energy, which we denote as the $\vec{K} = \frac{1}{a_G}\left(\frac{2\pi}{3}, \frac{2\pi}{3\sqrt{3}}\right)$ and $\vec{K'} = \frac{1}{a_G}\left(\frac{2\pi}{3}, -\frac{2\pi}{3\sqrt{3}}\right)$ or Dirac points [43]. At low energies

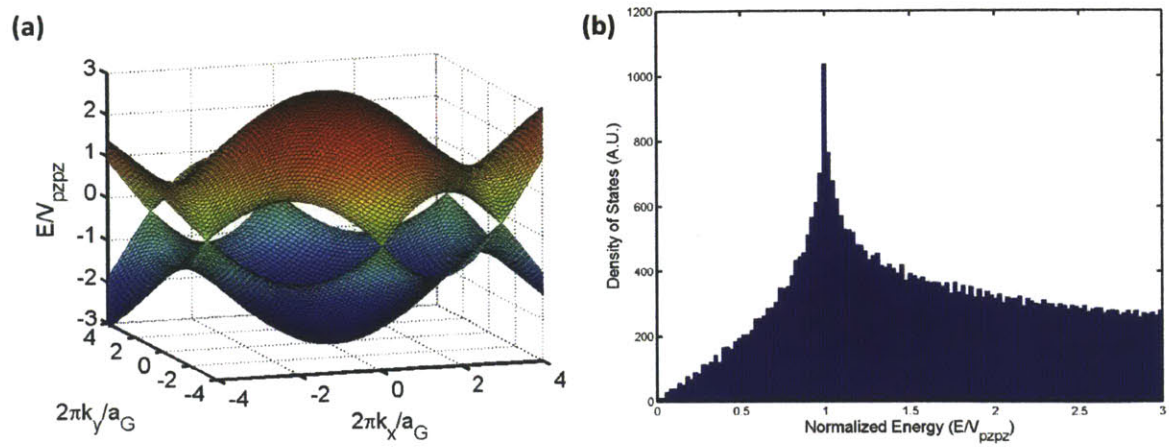

Figure 1-2: (a) Band Structure (E vs. $\vec{k}$) for Monolayer Graphene plotted from Eq. 1.9. (b) Density of States (g(E)) of graphene as a function of energy computed numerically from part (a)

($E << V_{pzpz}$) near the Dirac points, one can expand the bandstructure for graphene by expressing $\vec{k}$ relative to the Dirac points $\vec{K}$ and $\vec{K'}$ in terms of $\vec{q}$ (Eq. 1.10):

$$\vec{k} = \vec{K} + \vec{q} \tag{1.10}$$

The resulting new low energy Hamiltonian (H_q^{eff}) written in terms of $\vec{q}$ has a much simpler form (Eq. 1.11)

$$H_q^{eff} = \pm\hbar v_f(q_x\sigma^x \pm q_y\sigma^y) = \pm v_f\vec{\sigma}\cdot\vec{p} \tag{1.11}$$

where $v_f = (3|V_{pzpz}|a_G)/(2\hbar)$ is the Fermi velocity 1×10^6 m/s, $\sigma^x = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$, and $\sigma^y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}$. The corresponding eigenvectors of the system are represented by a two component spinor (Eq. 1.12):

$$\psi_{\vec{q}}^{\pm} = \frac{1}{\sqrt{2}} \begin{pmatrix} e^{-i\theta_q/2} \\ \pm e^{i\theta_q/2} \end{pmatrix} \tag{1.12}$$

where $\theta_q = tan^{-1}(q_x/q_y)$. Utilizing this low energy approximation yields the traditional energy versus momentum dispersion relationship (Eq. 1.13) that has drawn so many analogues with relativistic mechanics.

$$E_{\pm}(\vec{q}) = \pm\hbar v_f|\vec{q}| \tag{1.13}$$

As we will see over and over again, a unique property of graphene is the large tunability of the Fermi Energy (E_f) as a function of charge carrier concentration (n_s). Given equation 1.13, we can derive the relation between E_f and n_s (Eq. 1.14) as well as the density of states (g(E)) (Eq. 1.16) at 0 K:

$$n_s = \frac{d_{spin}d_{valley}}{4\pi}\frac{|E_f|^2}{(\hbar v_f)^2} = \frac{1}{\pi}\frac{|E_f|^2}{(\hbar v_f)^2} \tag{1.14}$$

$$E_f = \sqrt{(\hbar v_f)^2\pi n_s} \tag{1.15}$$

where we have taken into account the degeneracy of both Dirac Cones ($d_{valley} = 2$) within the Brillion Zone, as well as, both spin orientations ($d_{spin} = 2$).

$$g(E) = \frac{dn}{dE} = \frac{d_{spin}d_{valley}}{2\pi}\frac{|E|}{(\hbar v_f)^2} = \frac{2}{\pi}\frac{|E|}{(\hbar v_f)^2} \tag{1.16}$$

Figure 1-2 (b) shows the calculated density of states, which shows the expected linear relationship between density of states and energy for low energies ($E << V_{pzpz}$). Figure 1.3 shows the plot of E_f vs. n_s in Eq. 1.14 showing the square-root dependence between carrier concentration (n_s) and the Fermi Energy (E_f) Level. This plot will have greater significance when we discuss the optical properties of graphene in 1.1.2.

1.1.2 Optical Properties

Since we explore the opto-electronic applications of graphene in this thesis, the first materials property of interest is the optical absorption of a monolayer of graphene. Utilizing, Fermi's Golden Rule, we can directly compute the optical absorption ($\alpha = W_a/W_i$), which is the ratio of the absorbed power (W_a) relative to the incident power

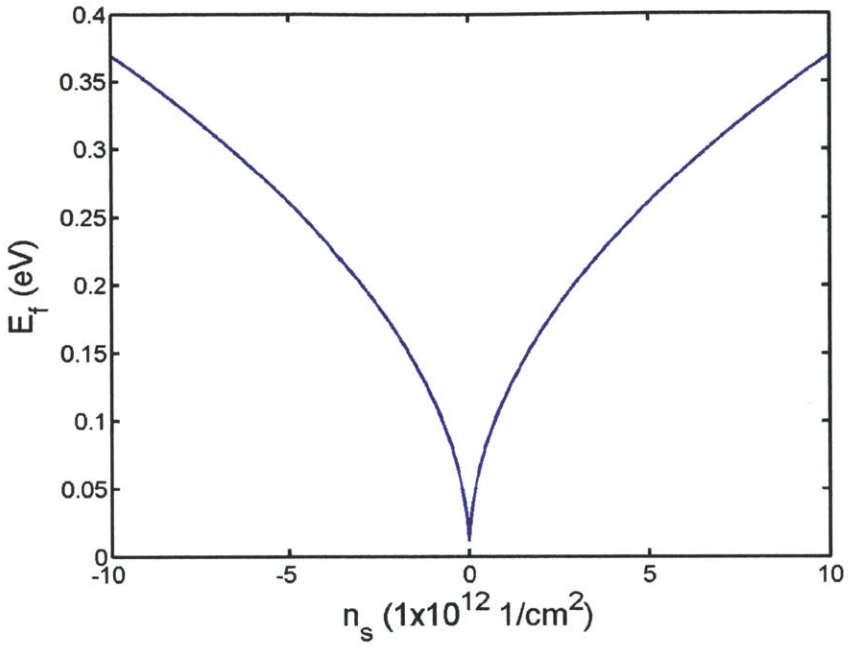

Figure 1-3: Variation of the Fermi Energy Level as a function of carrier density

(W_i):

$$W_i = \frac{1}{2} n_r c \epsilon_0 E_0^2 = \frac{1}{2} n_r c \epsilon_0 \omega^2 A_0^2 \tag{1.17}$$

where n_r is the relative refractive index, c is the speed of light, ϵ_0 is vacuum permittivity of free space, E_0 is the incident electric field strength, ω is the frequency of light in radians, and A_0 is the vector potential of the incident electromagnetic field.

In our calculation of absorbed power (W_a), we assume only vertical transitions between the conduction and valence band states (Eq. 1.18).

$$W_a = \frac{d_{spin} d_{valley}}{V} \hbar\omega \sum_{\vec{q_i}} \sum_{\vec{q_f}} \frac{2\pi}{\hbar} |\langle f | H_{int} | i \rangle|^2 \delta(2\hbar v_f |\vec{q}| - \hbar\omega) \tag{1.18}$$

where, i and f are the initial and final states, respectively, near the Dirac point, and H_{int} is the interaction Hamiltonian due to light-matter interactions. To compute H_{int}, we follow the traditional convention for light matter interactions and we replace

momentum ($\vec{p}$) in Eq. 1.11 by ($\vec{p} - e\vec{A}$), where e is the charge of an electron, and

$$H_q^{eff} = v_f \vec{\sigma} \cdot (\vec{p} - e\vec{A}) \tag{1.19}$$

$$\vec{A}(t) = \frac{1}{2}\vec{A}e^{-i\omega t} + \frac{1}{2}\vec{A}e^{+i\omega t} \tag{1.20}$$

Following standard light-matter interactions of a classical particle in an electromagnetic field, we can rewrite H_{int} in Eq. refch1eq:Wa for only absorption processes; therefore, we only use one of the two complex sinusoids in the vector potential (Eq. 1.21)

$$H_{int} = -v_f \vec{\sigma} \cdot \frac{1}{2} e\vec{A} = -\frac{ev_f}{2}\vec{\sigma} \cdot \vec{A} \tag{1.21}$$

Utilizing our eigenstates from Equation 1.12, we can compute the interaction term $\langle f|H_{int}|i\rangle$.

$$\langle f|H_{int}|i\rangle = -\frac{ev_f}{2}[\langle f|\sigma_x A_x|i\rangle + \langle f|\sigma_y A_y|i\rangle] = -i\frac{ev_f}{2}[A_x sin(\theta_{\vec{q}}) - A_y cos(\theta_{\vec{q}})] \tag{1.22}$$

$$|\langle f|H_{int}|i\rangle|^2 = \left(\frac{ev_f}{2}\right)^2 [A_x^2 sin^2(\theta_{\vec{q}}) + A_y^2 cos^2(\theta_{\vec{q}}) - 2A_x A_y sin(\theta_{\vec{q}})cos(\theta_{\vec{q}})] \tag{1.23}$$

where $\vec{q} = \vec{q_i} = \vec{q_f}$. Combining Eq. 1.23 and Eq. 1.18, we can integrate over all possible transitions (Eq. 1.24) to obtain

$$W_a = e^2 A_0^2 \frac{\omega^2}{8\hbar} \tag{1.24}$$

Finally, combining Eq. 1.24 for W_a with Eq. 1.17 for W_i, we can compute the fraction of optically absorbed power (Eq. 1.25),

$$\alpha = \frac{W_a}{W_i} = \frac{e^2}{4\epsilon_0 c\hbar} = 2.29\% \tag{1.25}$$

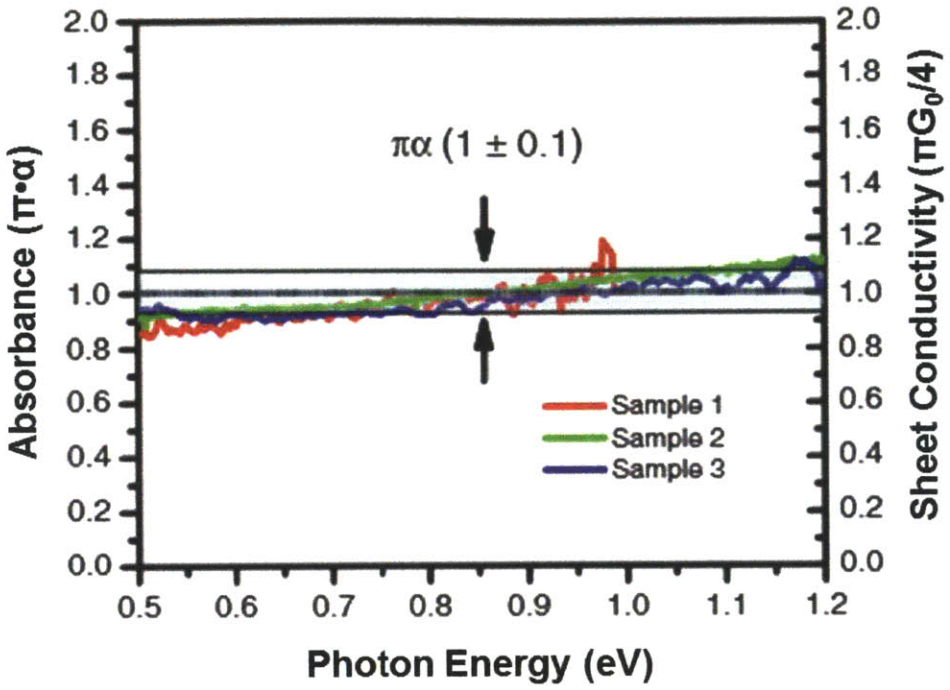

Figure 1-4: Broadband Optical Absorption of Graphene in units of the fine structure constant ($\alpha = \frac{e^2}{4\pi\epsilon_0\hbar c}$) [1]

in which interesting enough, the dependence on the photon energies disappears, resulting in an optical absorption dependent only on fundamental constants equal to 2.3%. This relation was confirmed experimentally by Mak, et al. and reproduced in Figure 1-4 [1, 44]. This analysis is valid as long as we are at low enough energies ($E << V_{pzpz}$) so that Equation 1.11 is valid.

However, in our previous calculations, we have assumed that $E_f = 0$, when the Fermi energy level is located between the conduction and valence bands. Unfortunately, the Fermi energy level can be modulated very easily by doping or electrostatic gating which can lead to Pauli Blocking. Equation 1.26 takes into account both the location of the Fermi Energy Level as well as the finite temperature due to Fermi Dirac Statistics.

$$\alpha_{inter}(\omega, T) = \alpha \left[tanh\left(\frac{\hbar\omega + 2E_f}{4k_BT}\right) + tanh\left(\frac{\hbar\omega - 2E_f}{4k_BT}\right)\right] \tag{1.26}$$

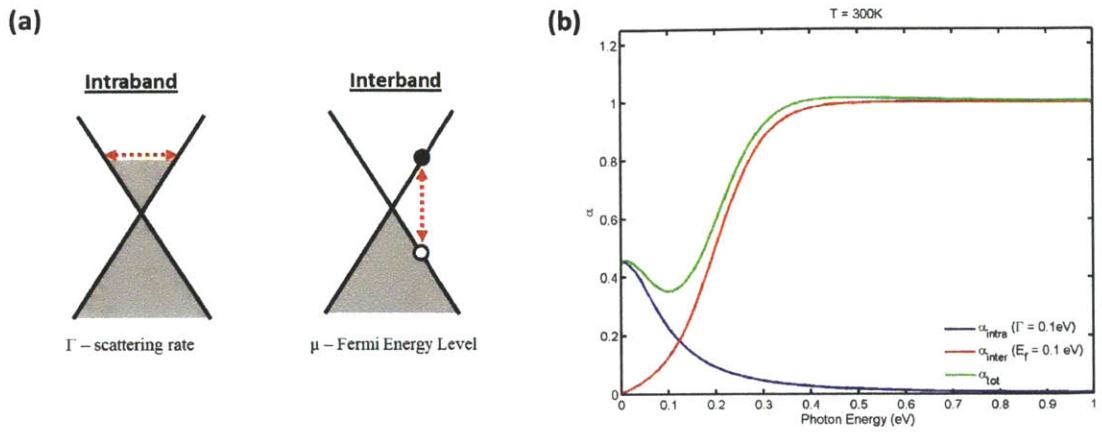

Figure 1-5: Interband and Intraband Optical Absorption (a) Intraband absorption process caused by free carrier absorption and Interband absorption processes caused by vertical transitions between the valence and conduction band. (b) Simulated optical absorption processes in graphene following Eq. 1.26 and 1.27, assuming $E_f = 0.1$ eV and $\Gamma = 0.1$ eV.

In addition, we can also model the free carrier absorption (α_{intra}) with a Drude-like model with a phenomological scattering (Γ) or dampening term (Eq. 1.27).

$$\alpha_{intra}(\omega, T) = \alpha \frac{16ln(2)}{\pi} \left[\frac{\hbar\Gamma k_B T}{(\hbar\omega)^2 + (\hbar\Gamma)^2} \right] \tag{1.27}$$

Therefore, the total optical absorption of graphene is just the summation of both the intraband and interband processes (Fig. 1-5). While the 2.3% absorption per layer has made graphene a viable candidate for transparent optical applications, this value of 2.3% is actually quite high considering this is only a single layer of material.

1.1.3 Electronic Properties

In addition to optical properties of graphene, this thesis will also explore the electronic transport properties of graphene. To begin, we start with the general expression (Eq. 1.28) for the electrical conductivity (σ), derived from the Boltzmann Transport Equation assuming the relaxation time approximation [45]:

$$\sigma = \frac{e^2 v_f^2}{2} \int g(E)\tau(E) \frac{\partial f(E, E_f)}{\partial E} dE \tag{1.28}$$

where $\tau(E)$ is an assumed scattering rate and $f(E, E_f)$ is the Fermi Dirac distribution function which depends on the Fermi energy level. For simplicity, we assume low enough temperatures ($E_f >> k_B T$) such that the derivative of the Fermi Dirac distribution can be approximated by $\delta(E - E_f)$. Therefore, in Equation 1.29, we can express the electrical conductivity in terms of an assumed scattering or relaxation lifetime:

$$\sigma = \frac{e^2 v_f^2}{2} g(E_f)\tau(E_f) = q n_s \mu \tag{1.29}$$

$$\mu = \frac{e^2 v_f^2}{|E_f|}\tau(E_f) \tag{1.30}$$

In graphene there are two dominant scattering mechanisms that we choose to consider: (1) Point defect or short range scattering (τ_{defect}) and (2) charged impurity or Coulombic scattering (τ_{imp}) [46] .

We begin again by following Fermi's Golden Rule in order to estimate the dependence of the scattering rate on the carrier concentration:

$$\frac{1}{\tau_{defect}(E_{\vec{q}})} = \frac{2\pi}{\hbar} n_{defect} \frac{|V_0|^2}{(2\pi^2)^2} \frac{1}{\hbar v_f} \int_0^{2\pi} [1 - cos(\theta_{\vec{q},\vec{k'}})] d\theta \int_0^{\infty} \delta(|\vec{q}| - |\vec{k'}|) |\vec{k'}| d|\vec{k'}| \tag{1.31}$$

$$\frac{1}{\tau_{defect}(E_{\vec{q}})} = n_{defect} |V_0'|^2 \sqrt{n_s} \tag{1.32}$$

Where n_{defect} is the density of defects or point scatters, V_0 is the Fourier Transform of the potential due to a point scatterer which can be approximated in real space by a delta function, resulting in a constant potential in Fourier space. However in equation 1.31, the scattering time due to point defects is inversely proportional to the energy, which results in equation 1.32, where we have lumped together all of the proportionality constants into the new term V_0'.

The situation is more complex when we take into account slowly varying potential functions due to a Coulomb scattering potential from charged impurities, as now the Fourier transform of the potential (V_1) has a momentum dependence. A more detailed

derivation can be found in Ref. [46], while in equation 1.33, we show only the result.

$$\frac{1}{\tau_{imp}(E_{\vec{q}})} = \frac{n_{imp}|V_1'|^2}{\sqrt{n_s}} \tag{1.33}$$

where n_{imp} is the density of charged scatterers, V_1' is the Fourier Transform of the Coulomb potential. Unlike the case for point defects, the scattering time for charged impurity scattering is proportional to the square-root of the carrier concentration in the case of graphene.

Since the scattering time or mobility of graphene is due to both types of scatterers, we can use Matthiessen's Rule to write the total mobility (μ)

$$\frac{1}{\mu} = \frac{|E_f|}{qv_f^2}\left[\frac{1}{\tau_{defect}} + \frac{1}{\tau_{defect}}\right] = \frac{1}{\mu_{imp}} + \frac{1}{\mu_{defects}} \tag{1.34}$$

where we have defined $\mu_{imp} = K_{imp}/n_{imp}$ and $\mu_{defect} = K_{defect}/(n_{defect}n_s)$ and we have assumed a constant of proportionality, K_{imp} and K_{defect} respectively. To illustrate the importance of this, we have plotted in Figure 1-6 the mobility for various graphene samples from the literature, as well as values measured here at MIT, to show how the carrier concentration strongly affects the measured mobility of graphene. These data will be discussed in more depth in Chapter 2 on materials growth, but it strongly suggests that there are limitations to the ultra-high carrier mobility of graphene at high charge carrier densities.

Looking at Eq. 1.34, we see that at relatively low carrier concentrations near the charge neutrality or Dirac point, the mobility of graphene can be considered to be independent of carrier concentration. Moreover, Eq. 1.29 also suggests that at low carrier concentrations, the conductivity of the film should go to zero; however, this is traditionally not the case [47]. Instead, we model graphene's conductivity near the Dirac point as a finite minimum carrier concentration (n_0), such that by using a square root model, we can write the total carrier concentration (n_{tot}) as [48].

$$n_{tot} = \sqrt{n_s^2 + n_0^2} \tag{1.35}$$

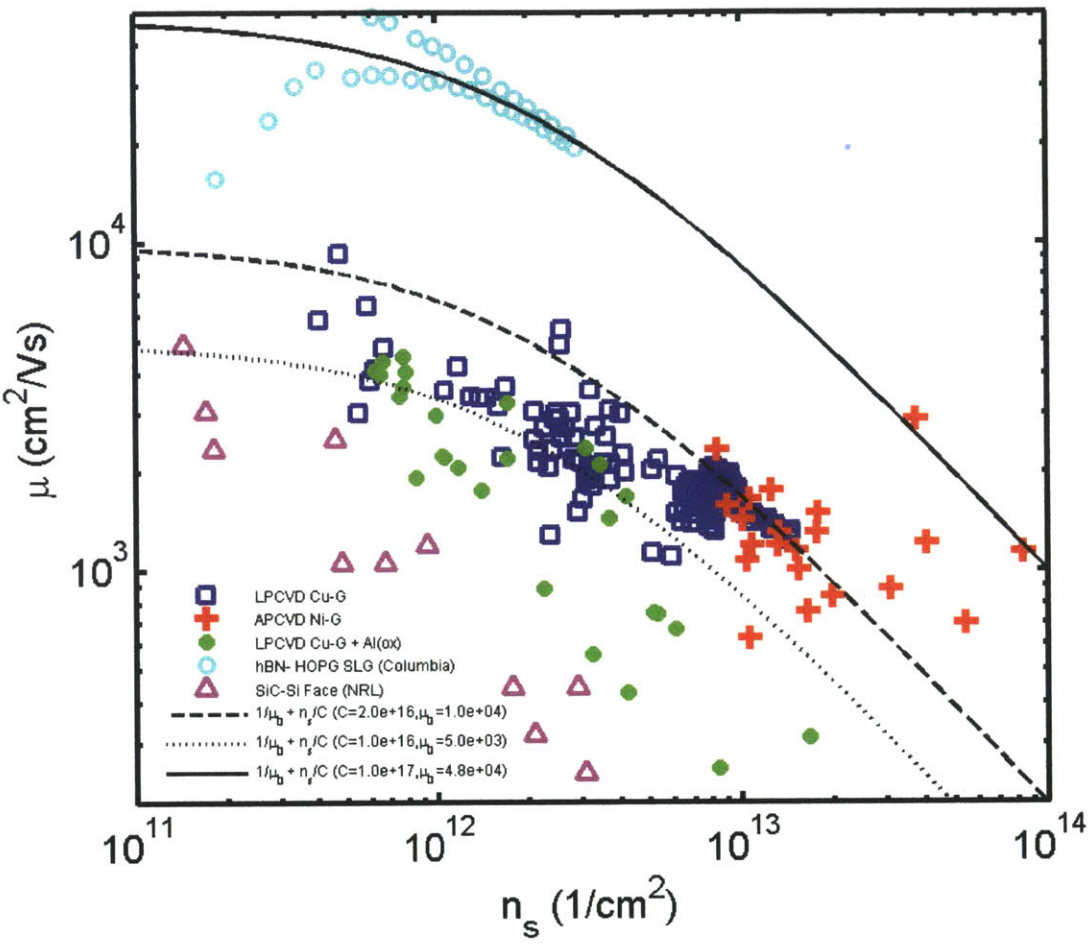

Figure 1-6: Mobility versus carrier concentration for a variety of graphene samples. Blue squares denote low pressure chemical vapor deposition (LPCVD) graphene on copper, red crosses denote ambient pressure (AP)CVD graphene grown on thin film nickel, magenta triangles denote epitaxial graphene grown on SiC-Si face, open circles denote exfoliated highly-oriented pyrolytic graphite on h-BN, green closed circles denote LPCVD Cu-G + thin oxidized aluminium, the continuous solid and dotted lines are fitting lines utilizing Eq. 1.34

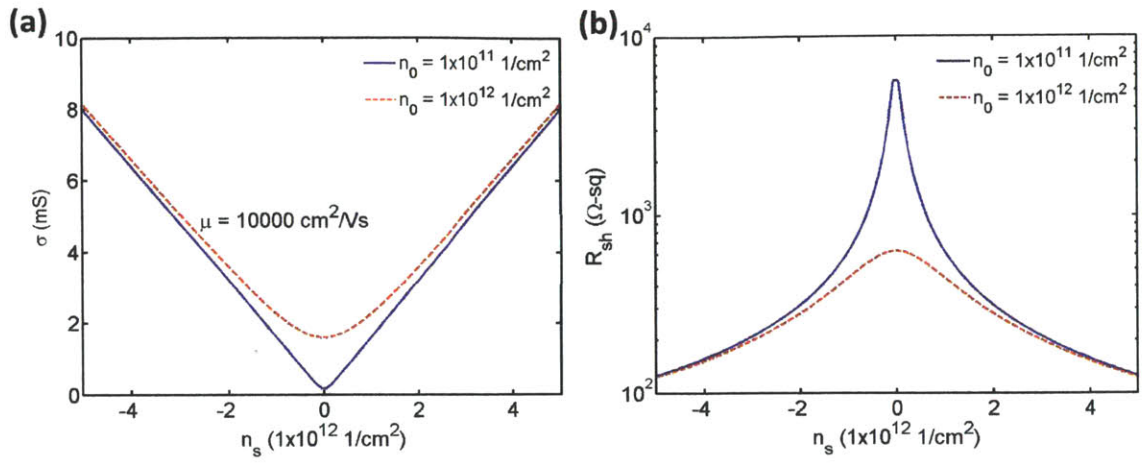

Figure 1-7: Electrical Properties of Graphene. The carrier concentration dependence of the (a) electrical conductivity (σ) and (b) sheet resistance (R_{sh}) taking into account non-idealities such as finite carrier concentration $n_0 = 1 \times 10^{11}$ (blue line) and 1×10^{12} $1/\text{cm}^2$ (dotted-red line), assuming a constant value of $\mu = 10,000$ cm^2 V^{-1}s^{-1}.

where $n_s = 0$ corresponds to the Dirac point. Therefore, the conductivity of graphene is now written as Eq. 1.36

$$\sigma = q n_{tot} \mu \tag{1.36}$$

To show the impact of the finite carrier concentration that is actually observed in real samples at the Dirac point, we plot in Figure 1-7, σ, as well as $R_{sh} = 1/\sigma$, to show the impact that these parameters have on the conductivity that is actually achievable in real graphene samples assuming two different levels of non-ideal behaviors.

1.2 Graphene Synthesis

While only recently has the physics of these layered compounds been revisited, the thin film growth of these materials has been an ongoing research topic for the past 30-40 years [49–51]. Recent developments have been focusing mainly on achieving atomic layer control, as well as, large single crystalline sizes over large areas. In addition, as we have shown earlier, the electrical conductivity of graphene is sensitive to both its surrounding environment due to charged impurities as well as intrinsic

defects. Both of these factors are strongly dependent on the graphene production or synthesis method. Therefore, we will review three of the most common synthesis techniques for graphene films for electronic applications: (1) Mechanical Exfoliation (2) Epitaxial Synthesis and (3) Chemical Vapor Deposition (CVD).

1.2.1 Mechanical Exfoliation

Mechanical exfoliation by cleaving bulk layered compounds is the most straightforward method to obtain a high quality single crystalline monolayer of graphene. By applying a sufficient force perpendicular to the plane direction such that the weak van der Waals forces between sheets can be overcome and then repeating this process over and over again, eventually a single atomic layer can be isolated and deposited onto a substrate for characterization [27, 52]. Novoselov et al. used an adhesive tape to peel off graphene layers [27]. They first prepared square highly oriented pryolytic graphite (HOPG) mesas with 20 μm to 2 mm in length and then attached such samples to photoresist. Using the adhesive tape, graphite sheets were peeled off from the photoresist, still leaving single to few-layered graphene. These layers were finally brought onto a Si substrate by releasing the photoresist from the tape by an acetone treatment. This method is highly remarkable since not only was the graphene one atomic layer and micron sized, but also it opened up a simple strategy for preparing other 2-D mono-atomic layers, such as hexagonal BN and MoS_2. This technique in its simplicity has proven very effective for many research groups around the world and has enabled the wide-spread availability of these materials today. What is most remarkable has been the ease of visual identification of monolayer sheets. Due to the optical interference of visible light between graphene and the underlying 300 nm SiO_2 substrate [2], graphene can be easily found using a standard optical microscope.

Figure 1-8 shows a picture of an exfoliated graphene flake. Typically, the flakes are in-homogeneous in thickness, as indicated by the highly reflective or white regions in Figure 1-8; however, the faintest colors can eventually be identified and confirmed by Raman spectroscopy and electrical transport measurements as monolayer graphene. The quality of this type of graphene for electronic measurements can be quite good

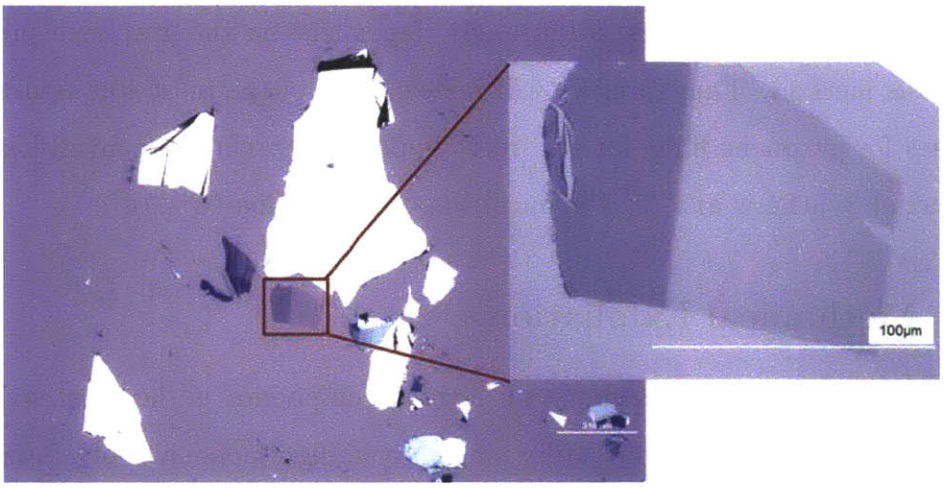

Figure 1-8: Picture of Exfoliated Graphene on top of 300 nm silicon dioxide [2,3]

in terms of number of defects; however, the carrier transport properties are degraded due to the surrounding environment for the graphene sample and due to its transfer onto silicon dioxide (SiO_2). Therefore, more recently, work on transferring these flakes onto other exfoliated flakes of h-BN have shown values of $\mu > 50{,}000$ $cm^2V^{-1}s^{-1}$ due to the flat and passivated surface structure of h-BN [53].

While exfoliated monolayer graphene has been used primarily for physics experiments, from Figure 1-8, one can see from the in-homogeneity in flake thickness, as well as, from the small flake size that other techniques are needed to generate a large-area scalable process for monolayer graphene. Currently there are two predominate methods for synthesizing large area graphene: (a) Epitaxial graphene grown on SiC and (b) chemical vapor deposition (CVD) of graphene on metal catalysts. Each of these methods has their own advantages and disadvantages depending on the final application.

1.2.2 Epitaxial Graphene

A route towards wafer scale graphene synthesis is the large area, epitaxial growth of graphene on single crystalline SiC. Since the graphene is directly prepared on this wide bandgap semiconductor material, it is ideally compatible with industrial

semiconductor processes. A number of different polymorphs of SiC, either 6H-SiC with AB-stacking or 4H-SiC with ABC-stacking can be used for this type of epitaxial graphene growth. Both of these hexagonal forms of SiC have two different topmost layers along the c-axis, Si-face SiC and C-face SiC, which affect the morphology and quality of the resulting graphene [54, 55].

Van Bommel et al. first developed this method of graphene synthesis through the high temperature-annealing of SiC [56]. They found thin graphite layers formed after heating SiC between 1000 and 1500 °C in ultrahigh vacuum (UHV) below 10^{-10} Torr. The synthesis process involves three steps [54,57–59] the desorption of Si atoms from the SiC surface at high temperatures, subsequent surface reconstruction to a C-rich surface, and the formation of a conformal graphene layer initiated from islands at step edges. The critical step in the synthesis process is controlling the desorption rate of Si from the SiC surface. A single crystalline graphite layer is typically observed on the Si-face SiC, while in contrast, the C-face SiC shows a poly-crystalline graphite layer with various in-plane orientations with respect to the lattice underneath. This difference between the two faces also results in changes in the electrical performance of the graphene [60]. While the C-face yields typically multiple graphene layers, the measured mobility of the graphene appears to be nearly intrinsic, limited by electron-phonon scattering rather than by defects and extrinsic factors. Si-face epitaxial graphene, on the other hand, can be only 1 to 2 layers, but due to the interfacial buffer layer, Si-face epitaxial graphene has lower mobilities than for the C-face, with mobility values similar to those of HOPG on silicon dioxide.

Epitaxial graphene growth on top of SiC has advantages in electronics applications by directly preparing high quality graphene on a semiconductor material at a wafer scale. In spite of this merit and high compatibility with the present Si-based process, there are some obstacles for industrializing this technique for graphene production. First, in terms of production cost, this process is expensive. Not only is the price of a single crystalline SiC wafer quite expensive, but also only specific versions of SiC, 4H-SiC (0001) or 6H-SiC (0001), are suitable for graphene growth [61–64]. To address this problems, much work has been done on growing graphene on thin films of

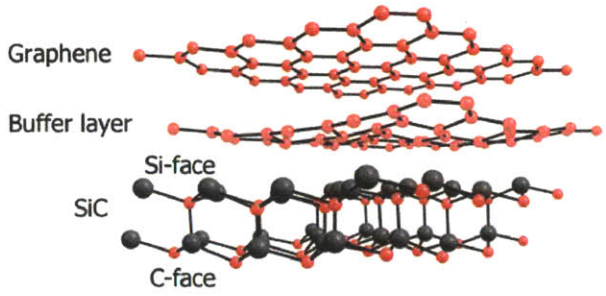

Figure 1-9: Surface Reconstruction of Epitaxial Graphene on a SiC surface.

SiC deposited on top of Si substrates as a cheaper alternative [65–71]. Furthermore, the epitaxial process usually requires either UHV or a very high process temperature (>1000 °C) which are not suitable for back-end integration. Furthermore, the formation of a buffer layer inbetween graphene and the SiC can have detrimental effects on the mobility of graphene, typically leading to relatively low mobilities $\sim$ 1000 $cm^2V^{-1}s^{-1}$; however, recent research on the hydrogen intercalation [72, 73] of graphene has shown that the buffer layer formed is actually a single monolayer of graphene that can be decoupled from the substrate resulting in both higher mobility and higher quality epitaxial graphene (Fig. 1-9).

1.2.3 Chemical Vapor Deposition of Graphene

Another method for large area growth is the CVD method using transition metal surfaces like Cu or Ni foils. These transition metals have traditionally been used as a catalyst to mediate the formation of sp^2 bonded carbon, such as graphite or carbon nanotubes (CNT) [23, 74–78]. The chemical structure of the metals contain partially filled d-orbitals which lower the activation energy for the formation of carbonaceous species [79–82]. The general process to synthesize CVD graphene includes four steps: (1) hydrogen annealing, (2) introduction of a carbon source (i.e. CH_4), (3) carbon surface reconstruction or dissolution of C into the metal, and (4) cooling. The hydrogen annealing step aims to increase the metal grain size and to remove any native oxides. Subsequently, during the growth step at 800-1000°C, a graphene layer forms

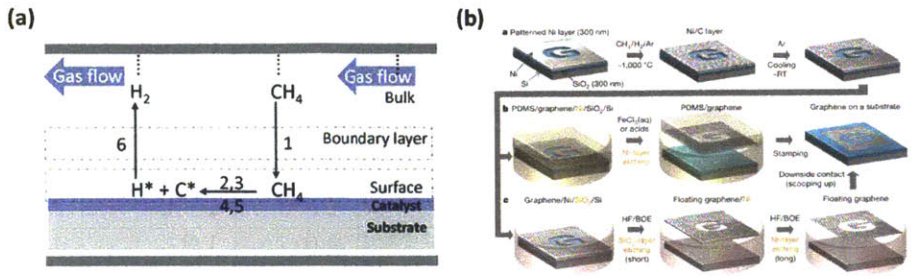

Figure 1-10: CVD Graphene Growth and Transfer (a) Growth Kinetics of CVD graphene growth [4](b) Synthesis, etching and transfer process for CVD Graphene [5]

on the metal surface. The mechanism of formation depends strongly on the carbon solubility of the metal catalyst. When synthesizing graphene using high carbon solubility substrates, such as nickel, the nickel becomes saturated with carbon, which naturally precipitates out upon cooling as a thin graphene layer [83]. Conversely, utilizing a low carbon soluble metal, such as copper, leads to a surface-limited growth producing highly uniform monolayers [84]. Finally, after graphene is synthesized on the metal substrate, the graphene can then be transferred onto any target substrate by selectively etching away the metal catalyst.

Figure 1-10 shows a rough outline of the growth and transfer process. Due to the simplicity of this technique and the relative ease of integration with any arbitrary substrate, it is this type of graphene that is the focus of this thesis. More in depth details about the material synthesis, material quality, and transfer optimization will be discussed in Chapter 2. While the CVD process is much simpler than that of epitaxial graphene and has similar material quality to that of HOPG, the mobility of CVD graphene suffers not as much from the material synthesis as it does from the transfer process - the optimization of which will also be discussed later in Chapter 2.

	Si	AlGaAs/ InGaAs	InAlAs/ InGaAs	SiC	AlGaN/ GaN	Graphene
E_{gap} (eV)	1.1	1.42	1.35	3.26	3.49	0 (MLG) 0.25 (BLG)
μ ($cm^2V^{-1}s^{-1}$)	1500	8500	5400	700	1500	>100,000
v_{sat} ($\times 10^7$ cm/s)	1.0	1.3	1.0	2.0	1.3	4
$E_{breakdown}$ (MV/cm)	0.3	0.4	0.5	3.0	3.0	-
κ_{th} ($Wcm^{-1}K^{-1}$)	1.5	0.5	0.7	4.5	>1.5	1.6-20

Table 1.1: Electronic Properties of Typical Semiconductors, E_{gap} is the electronic band gap,v_{sat} is the saturation velocity, $E_{breakdown}$ is the breakdown electric field, κ_{th} is the thermal conductivity

1.3 Graphene Applications

1.3.1 Radio-Frequency Applications

As we have mentioned earlier, the extremely high mobility of graphene, while enabling long length ballistic transport at room temperatures [32], has attracted a lot of attention by device engineers looking towards new channel materials for the next generation of electronics. Table 1.1 shows a comparison between the electronic properties of graphene relative to other standard semiconductors. While much attention has been focused on graphene as a replacement material for silicon, the lack of a band gap prevents graphene from being used for digital switching applications. However, that does not preclude the use of graphene for other electronic applications such as radio frequency (RF) or analog electronics applications, where signal amplification does not require a clear off state. In addition, the large hole and electron mobility is also unique since in the case of many materials (such as InSb or GaAs), due to k-p coupling or band repulsion, the effective mass of electrons is typically smaller than the effective mass of holes due to the large density of states from the heavy and light hole bands.

As opposed to digital applications, where we examine the large signal analysis, for

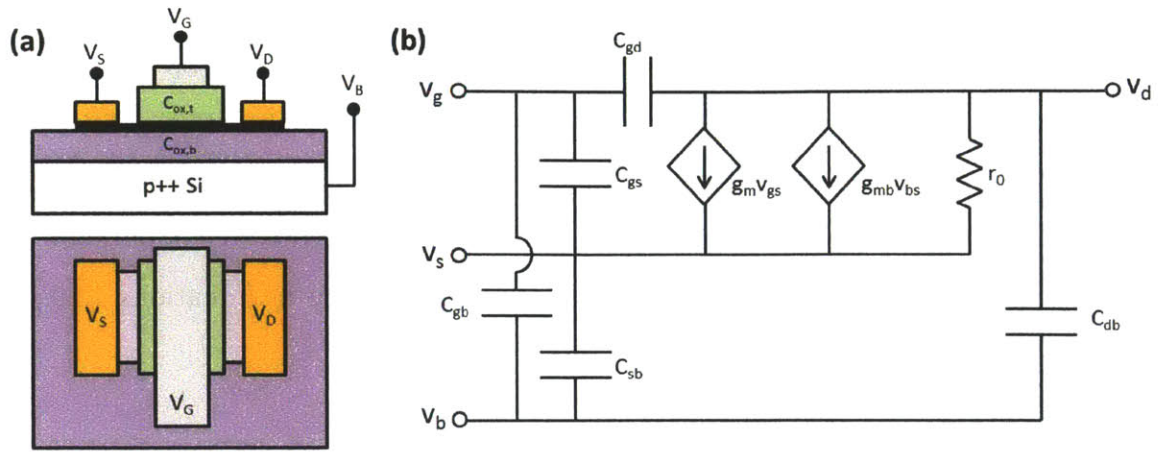

Figure 1-11: (a) Basic Schematic of Graphene Field Effect Transistor (G-FET) (b) Small Signal Model for G-FET including parasitic capacitances.

utilizing graphene for high frequency RF applications, we first look at creating a small signal model for a graphene-based field effect transistor (FET). Utilizing Eq. 1.36 for the electrical conductivity in combination with the effect of electrostatic gates, we can express the drain-source current through the Graphene FET as

$$I_{DS} = q\frac{W}{L}\mu\sqrt{n_s^2 + n_0^2}V_{DS} \tag{1.37}$$

$$n_s = \left|\frac{C_{ox,t}}{q}V_{GS} - n_{Dirac} - \frac{C_{ox,b}}{q}V_{BS}\right| \tag{1.38}$$

where V_{DS} is the voltage between the drain and the source, I_{DS} is the current between drain and source, $C_{ox,t}$ is the capacitance of the top gate oxide, $C_{ox,b}$ is the back gate oxide capacitance, and V_{GS} and V_{BS} are the voltages between the gate and source and backgate and source respectively. The expression in Eq. 1.37 is assumed to be in the triode regime of operation, as is common for graphene. Due to the lack of a band gap, a high field region of depleted charge is difficult to form at the drain contact (V_{DS}). Using Eq. 1.37, we can derive a small signal model for a G-FET to analyze its use for high frequency applications.

Figure 1-11 shows the basic wiring for a graphene field effect transistor including

voltage terminals. V_D and V_S are the drain and source voltages. The V_G and V_B are the top gate and back gate voltages, while $C_{ox,t}$ and $C_{ox,b}$ are the top and bottom oxide capacitances. Typically, for RF devices, V_B is usually tied to V_S, such that we can ignore both the backgate transconductance g_{mb}, and the capacitances associated with C_{sb}. Therefore, the two main device small signal parameters to compute are the transconductance (g_m) and the output resistance (r_0) shown in Equations 1.39 and 1.40.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = q\mu \frac{W}{L} V_{DS} \frac{C_{ox,t}}{q} \frac{n_s}{\sqrt{n_s^2 + n_0^2}} \tag{1.39}$$

$$\frac{1}{r_0} = \frac{\partial I_{DS}}{\partial V_{DS}} = q\mu \frac{W}{L} \sqrt{n_s^2 + n_0^2} \tag{1.40}$$

Therefore, if we look at a figure of merit such as the intrinsic short circuit current gain (f_T), where we short the drain to source and bulk, we find that the maximum frequency that this device can operate at is written in Equation 1.41

$$f_T = \frac{g_m}{2\pi C_{tot}} = \frac{W}{L} \frac{C_{ox,t}}{C_{tot}} \mu V_{DS} \frac{n_s}{\sqrt{n_s^2 + n_0^2}} \approx \frac{W}{L} \frac{C_{ox,t}}{C_{tot}} \mu V_{DS} \tag{1.41}$$

where $C_{tot} = C_{gs} + C_{gd} + C_{gb}$ is the total summation of gate to source, gate to drain, and gate to backgate capacitances. We also see that for large mobility materials for which high f_T can be achieved, since the frequency is directly proportional to the mobility of the channel material for long channel devices. As we scale the gate length of these devices to shorter dimensions, the speed of the device eventually becomes limited by the saturation velocity (v_{sat}), which for graphene is much higher than other conventional semiconducting materials.

The first GFET [27] was fabricated on a SiO_2/Si substrate. The 300-nm-thick SiO_2 was used as a gate dielectric, and its thickness was chosen for imaging single- and few-layer graphene. At the same time, the heavily doped Si substrate underneath served as a back-gate to modulate the conductivity of the graphene channel. This structure is the most commonly used in physics experiments due to its simplicity,

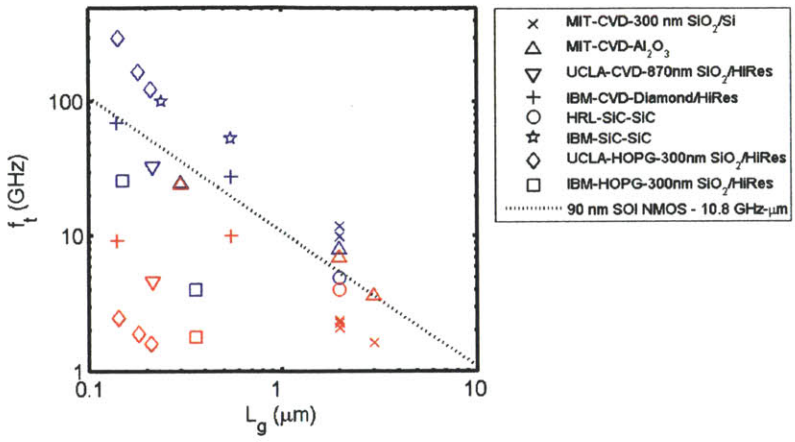

Figure 1-12: The blue data represent frequency performance after de-embedding pad capacitances, while the red data denotes the extrinsically measured f_T plotted as a function of gate length for various reports including values from this thesis.

but it is certainly not ideal for RF applications because of the thick gate dielectric and large parasitic capacitances introduced by the conductive substrate (C_{gb}). The first GFET with a top-gate was fabricated by Lemme [85] in 2007, and Meric [86] demonstrated the first GFETs with high frequency current-gain and 1/f dependence on frequency in 2008, basically starting the field of graphene RF devices. Since then, the performance of RF GFETs has quickly improved. IBM [15] demonstrated the first RF GFET with sub-micrometer gate length in late 2008. With an L_G of 150 nm, the device achieves an $f_T = 26$ GHz after de-embedding the co-planar waveguide (CPW) parasitics. HRL reported RF GFET with an $f_T = 4.4$ GHz with a gate length of 2 μm using graphene grown on SiC in 2009 [16]. In 2010, researchers in IBM reported f_T of 100 GHz using graphene on SiC with a gate length of 240 nm [11], and in the same year, a UCLA group fabricated a GFET using a nanowire gate that gave an f_T of 300 GHz [12]. These results are summarized in Figure 1.12 showing work including our own as we will discuss later on in Chapter 3.

1.3.2 Opto-electronic Applications

While work on graphene initially explored electronic applications, other applications, such as opto-electronic applications, have also begun to appear. Probably the most

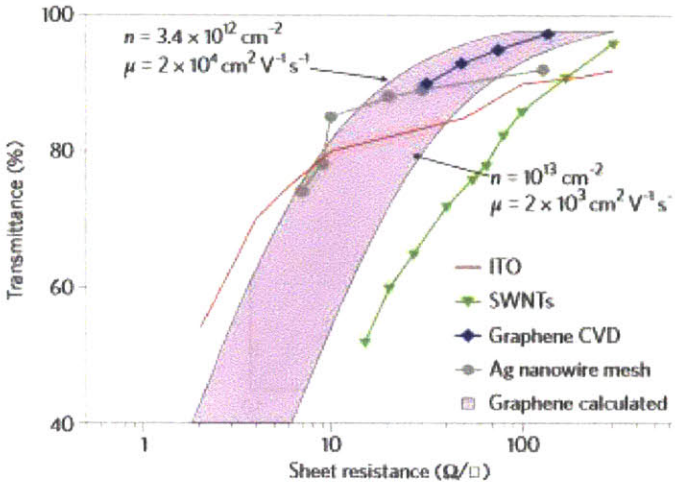

Figure 1-13: Comparison of optical transmission of graphene and other transparent conductive materials versus sheet resistance [6]

significant impact has been that of graphene for transparent conductive electrode applications as a replacement for indium tin oxide (ITO).

Transparent Conductive Electrodes

Given our analysis previously, monolayer graphene absorbs a constant 2.3 % of incident light spanning the visible and infrared spectrum.

Therefore, stacking various layers of monolayer graphene can achieve relatively transparent films with a high conductivity (Fig. 1-13). Sheet resistance ranges of 10-100 Ω-sq are shown in Fig. 1-13 and are expected to have a superior performance relative to other technologies, such as ITO or silver nanowire meshes. In addition, graphene's flexible nature, relative earth-abundance, and low cost are attractive reasons for pursuing graphene as a future replacement for ITO.

Photodetectors [6, 7, 87–91]

While graphene is considered to be relatively transparent compared to other materials, graphene is a material that can absorb 2.3% of the incident light across only a thickness of 0.35 nm, the actual optical absorption corresponds to an extremely high value of $\sim 33.7 \times 10^4$ cm^{-1} [92]. Coupled with its ultra-high carrier mobility

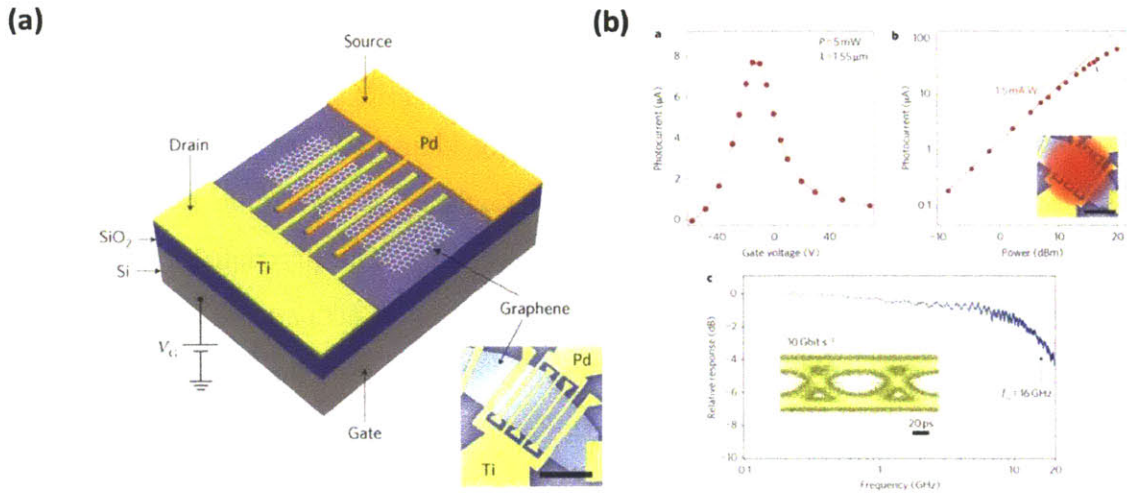

Figure 1-14: Graphene Photodetector utilizing asymmetric metal combinations demonstrating detection at 10 GBit/s (a) Schematic of Device (b) Measured Response - more details can be found in Ref. [7]

and broad band optical absorption, there has been a lot of interest in using graphene as a photodetector. Recently, by utilizing asymmetric metal contacts, to create a metal-graphene-metal Schottky junction, graphene has been demonstrated to have an internal quantum efficiency of 15%. Using the built-in field created by the metal junctions, IBM has demonstrated >10GBit/s data transmission utilizing >16 GHz detection at $\lambda = 1.55\mu$m shown in Figure 1-14. While most work has focused on the visible, it is the longer wavelengths (i.e. the mid-IR), where less is presently understood, that is the topic of Chapters 4 and 5 of this thesis. However, while graphene's built-in field has been the source of charge separation, more recent work has also suggested that in addition to photo-voltaic effects, thermo-electric effects may also be occurring in graphene [90, 91]. This source of ambiguity plays a critical role for evaluating the performance of graphene as a photodetector in the infrared and will be clarified in more depth in the physical detection mechanism in Chapter 4 of this thesis.

1.4 Thesis Overview

While there are numerous applications already identified and many new ideas for graphene, in this thesis, we will mainly be focusing on electronic RF applications and IR detection utilizing graphene-based detectors. The first half of this thesis is dedicated towards the development of the graphene itself and related technologies to provide a robust toolbox for graphene applications. In Chapter 2, we will focus mainly on the material quality and on the metrology of our starting graphene. The motivation and goal of this thesis is to develop a stable and robust fabrication technology, which after many trials and tribulations is only possible through careful material metrology of the starting material. Furthermore, we introduce device structures utilizing large area CVD h-BN, including again material characterization of h-BN as well as its integration with large area CVD graphene. Chapter 3 explores the device processing side of graphene with an emphasis of graphene field effect transistors for RF frequency applications. We will discuss some of the fundamental issues of processing graphene and our contributions related to contact resistance as well as an in-depth analysis of graphene-metal interactions. The second half of this thesis is devoted towards developing graphene as an infrared detector for thermal imaging applications. Chapter 4 discusses the fundamental physics and background of infrared detection presenting experimental work on clarifying the fundamental detection mechanisms in the infrared (IR) at $\lambda = 10.6\mu$m. We discover that in the mid-infrared, thermoelectric effects are the dominant detection mechanisms making graphene a unique temperature sensor. Therefore, Chapter 5 is dedicated to estimating the performance of graphene based IR sensors and demonstrating improved sensitivities through thermal engineering of the device. In addition to improving the overall sensitivity of our detectors, we also demonstrate in Chapter 5 the development of a focal plane array of monolithography integrated graphene detectors onto a complementary metal oxide semiconductor (CMOS) chip and we discuss the fabrication and integration issues related to this back end of the line process. Finally, Chapter 6 briefly discusses future work as well as other exciting applications areas utilizing graphene for infrared

imaging and thermal sensing applications that are beyond the scope of this thesis.

Chapter 2

CVD Graphene - Large Area Materials Development

While graphene's predominance amongst the scientific community is closely correlated with the simple sample preparation by exfoliation, the technological interest in graphene has really stemmed from the development of large area synthesis techniques. As mentioned earlier, two techniques have been developed for electronic applications: (1) Epitaxial graphene on SiC and (2) Chemical Vapor Deposition (CVD) graphene on metallic catalyst surfaces. While we have mentioned in Chapter 1 the advantages and disadvantages of both techniques, for this thesis, we focused primarily on CVD graphene for its ease of integration with a variety of substrates that will become more clear in the following sections and chapters. However, because the preparation of CVD graphene was still in its relatively nascent stages at the start of this thesis, a large amount of time was spent better characterizing and bench marking the large area CVD graphene before being able to develop a robust processing platform for device applications. This includes work, not only optimizing growth and synthesis of these films, but also controlling the Fermi energy level within graphene and minimizing external charged impurities.

Therefore, this chapter will cover various metrology techniques including scanning electron microscopy, Raman spectroscopy, and Hall effect measurements of our CVD graphene to better characterize our starting material. At the end of this chapter, we

will also discuss the materials development of large area hexagonal boron nitride with our CVD graphene as a platform for high-carrier mobility substrates.

2.1 Graphene Synthesis

The graphene grown in this thesis primarily stems from graphene grown by chemical vapor deposition on copper foils following from X. Li, et al [93]. While previously, CVD graphene was grown utilizing thin films of Ni as a catalyst material [5, 83], the lower solubility of carbon within Cu leads to a surface limited growth unlike Ni, where carbon and Ni form a solid-solid super-saturated solution that precipitates carbon or graphene upon cooling. Figure 2-1(a) shows a basic schematic of our low pressure growth chamber (<1 Torr). Graphene growth normally consists of 3 stages (Figure 2-1(b)): typically during the first stage, the metallic foil is pre-annealed at 1000 °C with H_2 to reduce any native oxides on the copper surface. After the pre-annealing stage, methane is introduced into the system to initiate the graphene growth process. Finally after the graphene growth reaches steady state conditions, the sample is then cooled down back to room temperature and the copper foil is removed and ready for transfer off of the copper surface.

2.1.1 Scanning Electron Microscopy (SEM)

In order to rapidly identify the material quality before transfer of the film, scanning electron microscopy (SEM) was utilized to directly image the graphene on the surface of the Cu foil. This allowed for direct examination of the graphene nucleation density and verification that the graphene films had grown to full completion.

Figure 2-2 shows the growth and nucleation of graphene flakes on the copper surface after different durations of time. The graphene samples are grown for a specific amount of time inside of the furnace and then are rapidly cooled to suspend the growth process, thereby freezing the graphene structure in place. This is done traditionally when evaluating a new growth condition to determine roughly the domain size of the graphene (5-8 μm), as well as, the necessary time to grow a sample to completion

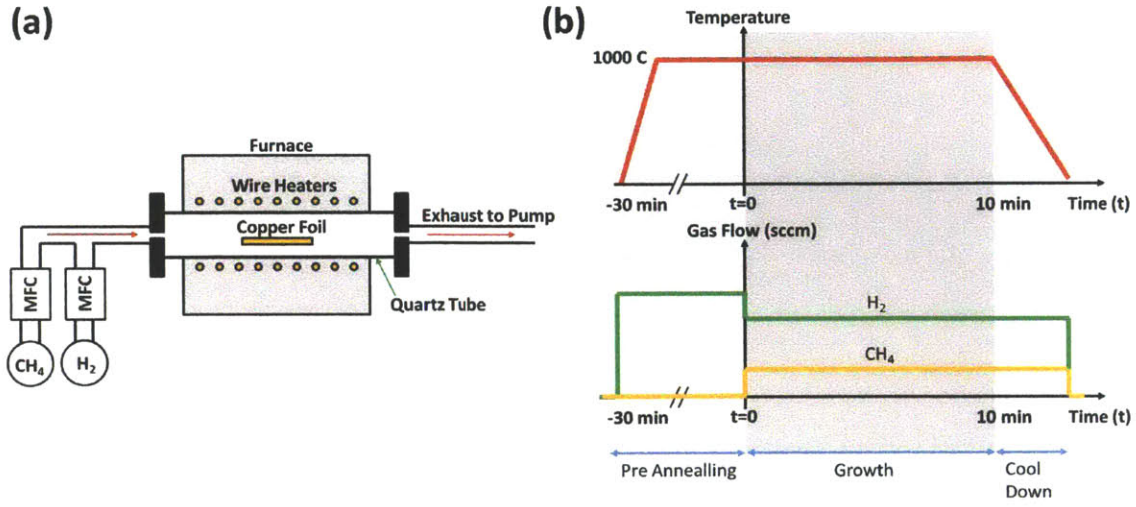

Figure 2-1: (a) Basic Schematic of the CVD Growth Chamber, where mass flow controllers (MFC) for methane (CH_4) and hydrogen (H_2) gas regulate the flow rates to control the total pressure within the quartz tube as the gas is being exhausted to a dry scroll pump. (b) Typical diagram of the graphene growth conditions. (1) Pre-Annealing occurs at 1000 °C under a hydrogen environment to remove any surface oxides, (2) Growth occurs when methane, introduced as the carbon source, decomposes to form atomic carbon on the copper surface. (3) After growth reaches steady state conditions, the sample is then rapidly cooled and taken out of the furnace for transfer.

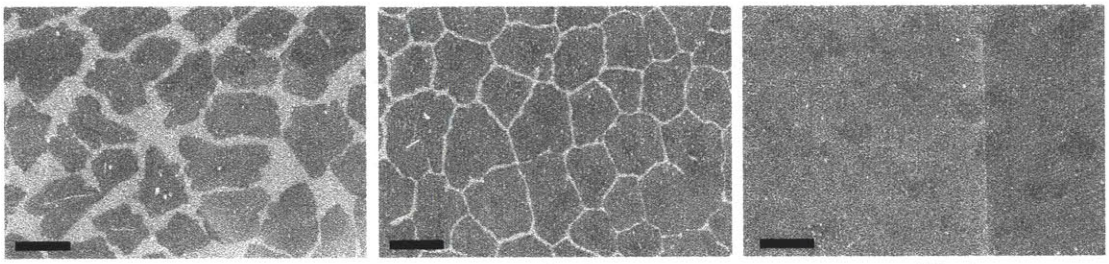

Figure 2-2: Scanning Electron Microscopy of Graphene Growth on Cu Foil as a function of Time (t_0): 1 min, 5 min, and 30 minutes, the black scale bar in the lower left hand corner is equal to 4 μm. After 1 minute, the light gray background is the copper surface, while the gray flakes are graphene. The center of the graphene flake does show the formation of a bilayer in the center - represented by the darker center of the flake. After completed growth for 30 minutes, and cooling, wrinkles formed by the coefficient of thermal expansion mismatch between graphene and the copper begin to appear.

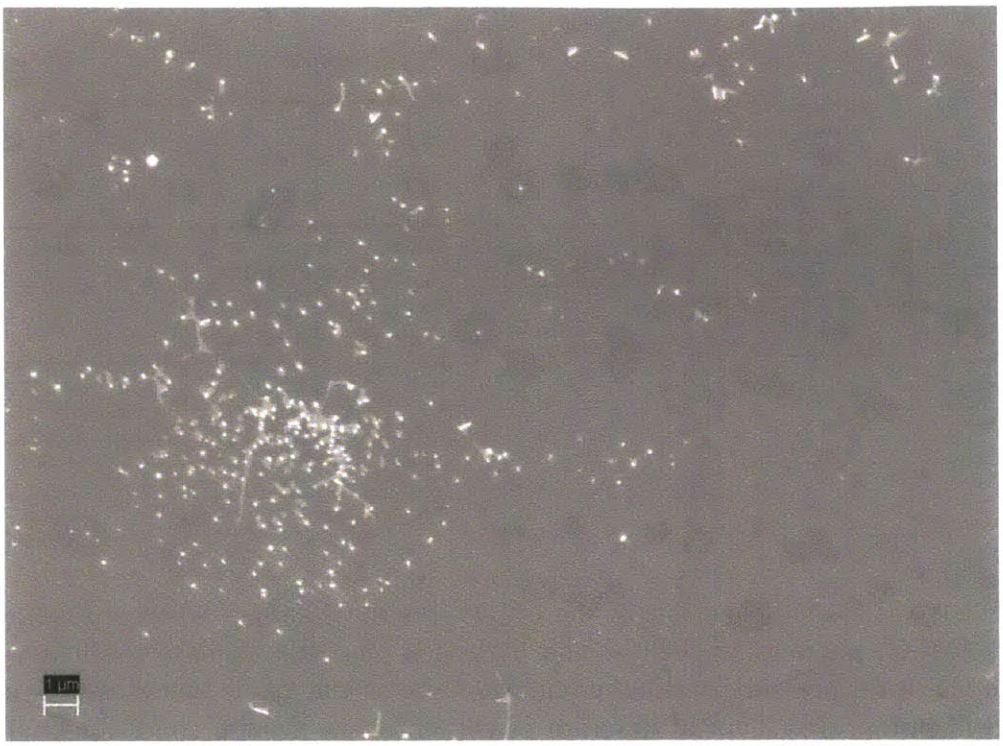

Figure 2-3: SEM image of continuous graphene after growth, showing how surface particles can prevent the proper completion of the graphene film, leaving behind gaps in the graphene film. Scale bar here represents 1 μm.

(10-20 minutes). While we mentioned that carbon has a low solubility within Cu, yielding a surface dominated growth regime, there are still many nucleation sites that can actually yield bilayer graphene domains which are represented by the darker spots located in the center of the monolayer domain. Other sources of non-idealities during growth that can occur include the formation of wrinkles due to the coefficient of thermal expansion mismatch between graphene and the copper [93].

In addition to the previously mentioned imperfections, a lack of complete growth or discontinuous graphene was another common issue that often led to inconsistent material quality. As we will discuss in the next chapter on device fabrication, the graphene on the surface is often exposed to dilute bases commonly found in many photoresist developers, which can etch away the underlying substrate through any small defects or holes in the graphene thereby causing the film to delaminate. While normally etching $<$1 nm of the substrate material does not impede standard device

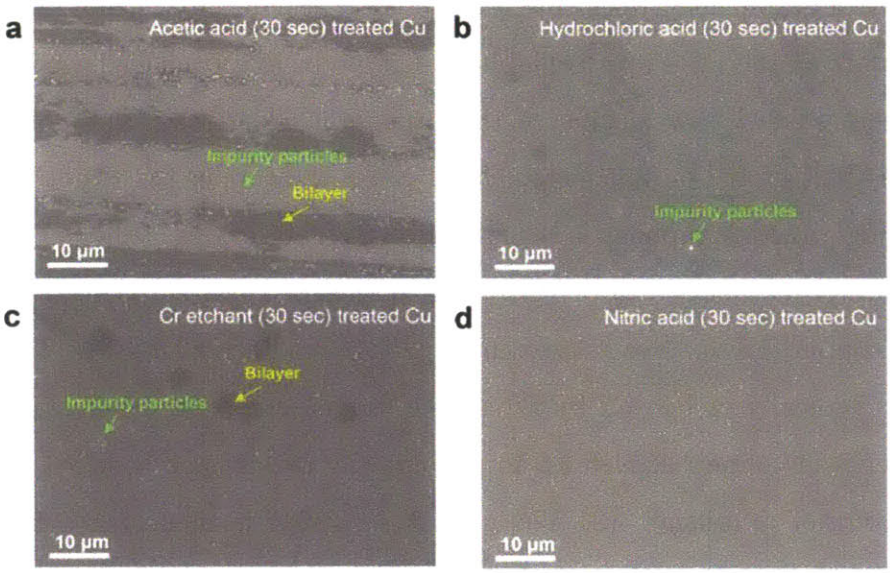

Figure 2-4: Variety of surface pre-treatments (30s each) to the copper foil to improve the uniformity of graphene growth on copper. (a) Acetic Acid (b) Hydrochloric Acid (c) Cr etchant (d) Nitric Acid

processing, for only van der Waals bonded materials, any substrate etching can automatically release the film causing it to peel off. Figure 2-3 shows an SEM image of some of these discontinuous regions where a collection of particles on the surface - possibly surface contaminates - appeared to agglomerate near the boundaries of the graphene growth front, resulting in an incomplete growth. To discover if these impurities were due to the copper or to the growth system, we implemented a series of copper pre-treatments on the copper foil prior to the growth of graphene to get rid of any surface contamination that might be present during the manufacturing of the copper foil, which was purchased from Alfa-Aesar (Fig. 2-4).

2.2 Graphene Transfer

As we have mentioned before, perhaps one of the greatest strengths of CVD graphene is its ability to be transferred onto any arbitrary substrate. However, this ability is also CVD graphene's greatest weakness. As we have shown earlier in Chapter 1,

the mobility of graphene (μ) is strongly affected by the density of charged impurities (n_{imp}). Unfortunately, the most reliable and reproducible transfer process has been that of wet transfer. An outline of the process is illustrated in Figure 2-5. (1) Graphene is first grown on flat copper foils. Since the copper foil is not sitting on a carrier during growth, graphene is actually grown on both sides of the flat copper foil. (2) poly(methyl methacrylate) or PMMA is spun (thickness $\sim$ 300-500 nm) on one side of the copper foil to serve as a mechanical support during transfer. The backside graphene is typically etched off by a reactive oxygen etcher to ensure rapid etching of the underlying copper, as well as, to prevent any re-adhesion between the bottom and top layers of graphene. (3) The copper substrate is then etched off in a wet chemical process using copper etchant typically composed of $FeCl_3$; however, due to residual Fe nano-particles left over, the samples are then etched additionally in HCl to remove any residual metal particles. (4) Finally the graphene is then transferred onto a separate bath of Di:H_2O to rinse away any residual ions and acids before being scooped and transferred onto the target substrate, which for testing/visualization purposes is 300 nm of thermally grown silicon dioxide [2]. (6) Finally, the PMMA support layer is removed through a solvent clean, as well as, a high temperature (300-350 °C) annealing under forming gas (Ar/H_2) - (400/700 sccm) to remove any residual sp^3 bonded carbon.

However, while the graphene basal plane is relatively inert and stable in this transfer process, the use of acids and ions can leave behind some amount of residual doping in the graphene sample due to adsorbed molecules. Therefore, chemical doping is often the root cause of non-intentional doping of the graphene sample, which can not only introduce a large number of n_{imp}, but also can affect the minimum carrier concentration or n_0. These effects will become more critical when we discuss the performance of electronic and opto-electronic devices in the following chapters. In this section, we will discuss a variety of transfer treatments and their impact onto residual doping of the graphene. For these experiments, we utilize Raman spectroscopy as a fast non-contact method for characterizing our graphene samples before device fabrication.

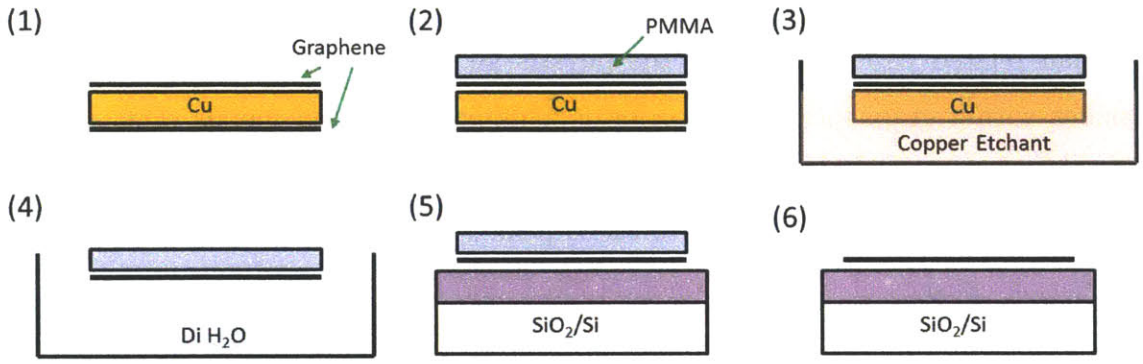

Figure 2-5: Wet Chemical Transfer Process for graphene (1) CVD graphene grown on copper grows on both sides of the foil. (2) A single side of graphene is protected using PMMA as a mechanical support layer. The backside graphene is often exposed to a reactive oxygen plasma to prevent the graphene on the backside from adhering to the PMMA protected graphene during removal of the Cu substrate. (3) The copper is etched away utilizing Transene Cu etchant and diluted with HCl:DIH_2O leaving behind a graphene/PMMA stack floating on top of DI water. (5) This G/PMMA film is scooped out of water by the final target substrate and nitrogen dried to remove any excess water between the graphene and the substrate. The PMMA is heated to its glass transition temperature (150 °C) to ensure the proper bonding and relaxation of the graphene/PMMA film and to smooth out any imperfections or surface features in the copper foil during transfer. (6) Finally the PMMA is removed by acetone and IPA and if necessary can be thermally annealed in H_2/Ar (400/700 sccm) at 350 °C to induce thermal decomposition of the PMMA into volatile carbon fragments. The final sample is a graphene layer on a SiO_2/Si substrate.

2.2.1 Raman Spectroscopy

Raman Spectroscopy is a nonlinear optical process where excited electron-hole pairs undergo scattering with phonons and recombine, resulting in a frequency shift (Raman shift) of the emitted light. This nonlinear optical process has proven to be a valuable tool for analyzing various materials, but especially important for carbon based nanomaterials such as carbon nanotubes or graphene [94]. While there are numerous Raman related papers exploring the physics and identification of various phonons modes within graphene, the three most commonly analyzed modes (D,G, and 2D shown in Figure 2-6) have become a gold standard for characterizing graphene quality. The Raman process associated with the D peak is shown in Figure 2-6 (a), where the transition consists of both a phonon (1350 1/cm) and a defect in order to conserve momentum and energy. Therefore, the intensity of the D peak is often associated with point like defects (n_{defect}) such as lattice defects or grain boundaries [95]. Another relevant peak for graphene metrology is that of the G peak. This process is associated with the Γ optical phonon ($E_{ph} = 200meV$) which exhibits a Raman shift of $\sim$ 1580-1600 cm^{-1}. This vibrational mode is extremely useful for quantifying the chemical doping within graphene as shown in Figure 2.7. Excess carriers within graphene can cause stiffening or softening of the carbon-carbon bond resulting in a shift of the peak position of the G peak. Finally, the 2D peak results from a double resonant process between the 2 Dirac Cones (K and K') within the Brillioun zone of graphene. For metrology purposes, the width or lineshape of the 2D peak can be used as a characterization tool for the differentiation between monolayer and Bernal-stacked bilayer graphene, as well as, another metric for identifying the doping level within graphene [96,97]. A typical Raman spectrum for graphene is shown in Figure 2-6(d) with the corresponding peaks (D,G, and 2D) labeled. While our interest is mainly in a rapid quality assessment of our graphene after transfer, we primarily investigate the G peak position as a metric of the doping level within graphene. The G peak position for undoped graphene is typically 1585 cm^{-1} [8].

As we have mentioned previously, there are a variety of factors that can dope

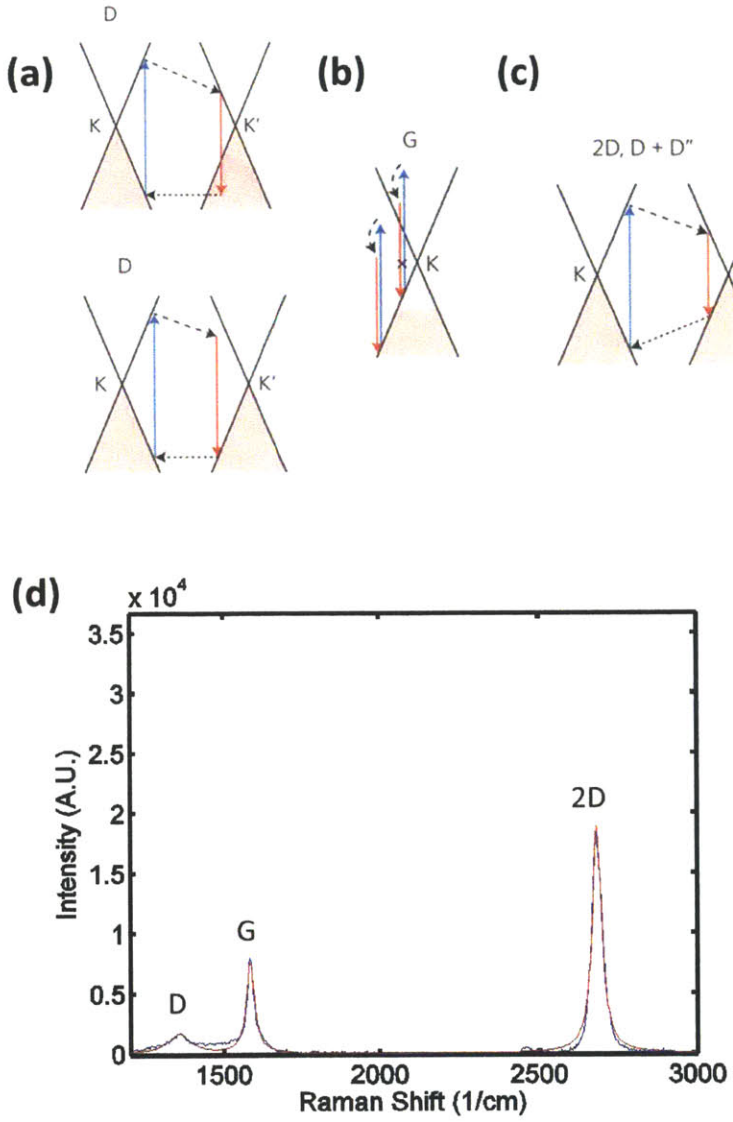

Figure 2-6: Dominant Raman Scattering Processes in Graphene: (a) D peak (b) G peak (c) 2D peak. The blue arrow signifies the incoming optical photon, the red is the photon shifted after scattering or interacting with a phonon within the material. Various transition can occur not only within a single Dirac cone, but can also occur between Dirac cones, such as the D and 2D peaks. The shift of the exciting light is dependent on certain phonon modes of graphene and lead to discrete peaks in the Raman spectra.[6] (d) Raman Spectra of graphene after background removal. Blue shows the measured data, and the red line shows the automatic Lorentzian fitting to the peaks.

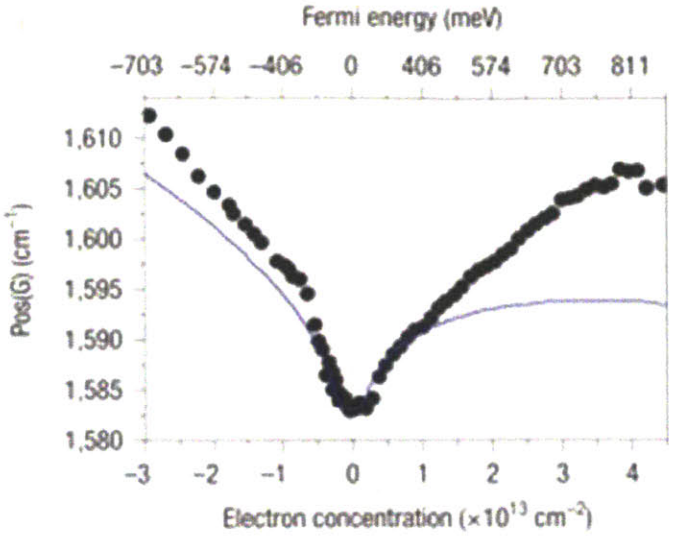

Figure 2-7: Electrochemical gating of graphene and the resulting shift of the G peak position as a function of doping. The solid blue line is from theory, while the dots are experimentally measured values. [8]

graphene during transfer: the acid or etchant to remove copper, any substrate pre-treatments, and the removal process for the PMMA. Any excess doping from these steps can dramatically impact our electrostatic control of the graphene channel. Therefore, to address these issues, we ran a series of experiments listed in Figure 2-8 looking at the average G peak position as well as the variation in the G peak position for a variety of transfer conditions.

As shown in figure 2-8, utilizing polycrystalline graphene (PCG) with a domain size typically of 5-10 μm, we tried a series of experiments focusing on three main parameters: (1) Substrate Treatment of the SiO_2 (Bare, Asher (TRL-Asher 800 W for 1 Hour), OTS (octadecyltrichlorosilane) (dip coating), Pirahna/RCA (H_2SO_4:H_2O_2 1:3 for 10 minutes), (2) Type of Copper Etchant ($FeCl_3$, ammonium persulfate (APS)), (3) PMMA removal process (Acetone or Annealing in H_2/Ar environment for 2 hours). All Raman data was taken under ambient conditions utilizing a 532 nm excitation laser for 100 randomly chosen points across the sample. After all of these experiments, we find that the G peak position for almost all of the process conditions results in graphene relatively heavily doped (G pos $\sim$ 1600 1/cm $= 1 \times 10^{13}$ 1/cm^2) except

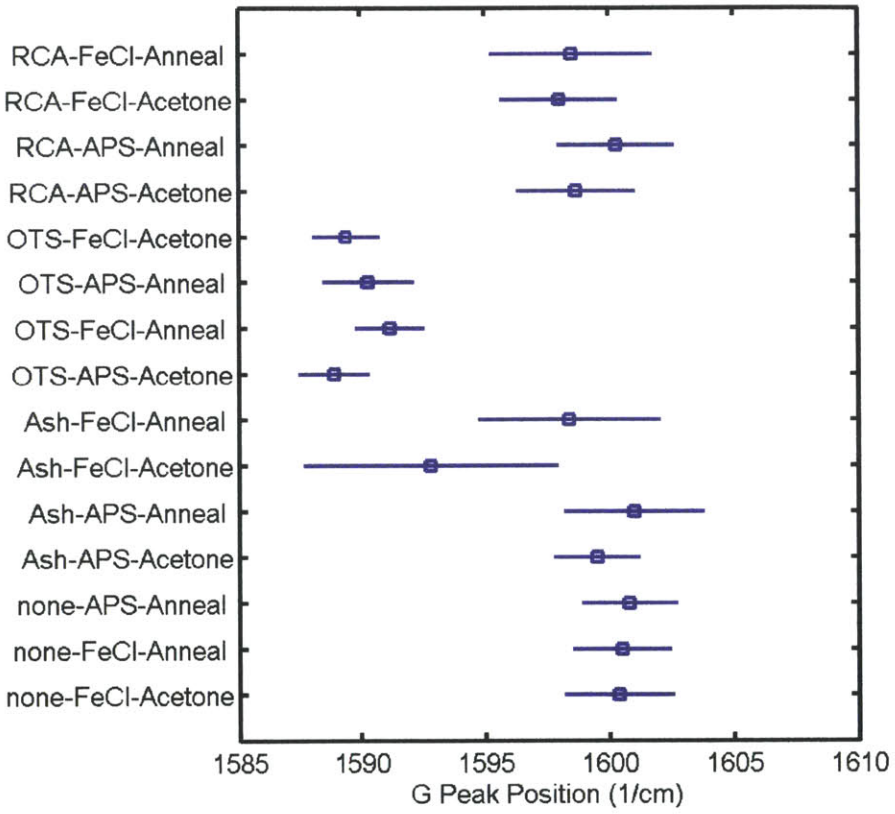

Figure 2-8: All Samples were polycrystalline graphene (PCG), APS = ammonium persulfate, OTS = octa-decyltri-chloro-silane, RCA = H_2O_2:H_2SO_4 1:3, FeCl = Iron Chloride ($FeCl_3$), Ash = Oxygen Plasma 800W for 1 Hr. The square is the average G peak position, while the line is the variation in G peak position over 100 data points.

for the OTS treated substrate (G pos $\sim$ 1590 1/cm = 5×10^{12} 1/cm^2). The main difference between the OTS treated substrate and the others is the increased hydrophobicity of the SiO_2 [98]. Traditionally, treatments such as Pirahna and reactive ion etching (Asher) are known to make silicon dioxide much more hydrophilic. While hydrophilic substrates are often much easier to transfer onto, the hydrophobicity of the substrate appears to be the dominant contribution to the extrinsic doping of the graphene.

This strongly suggests that the water during transfer may contain some residual ions or adsorbed material that might be trapped during transfer. Because of this possibility, we optimized our graphene transfer by increasing the rinse time of our samples in DI:H_2O water to help wash away any chemical residues during step 4 of our transfer process (see Fig. 2-5). While Raman spectroscopy is an extremely useful tool for rapid characterization, in order to fully quantify our material quality, electrical characterization and device fabrication are still necessary.

2.2.2 Hall Effect

In addition to optical techniques, we also developed a rapid characterization process for electrically quantifying the graphene doping and mobility. Figure 2-9 shows the device process flow. (1) Utilizing pre-patterned Ti/Pt electrodes fabricated by photolithography, we can create an entire wafer of ohmic pads for contacting graphene. (2) While in the second step, we transfer graphene onto these electrodes. By utilizing a four point probe geometry, issues such as contact resistance can become nullified, since the probes injecting the current are no longer used to measure the voltage drop. (3) After graphene transfer, a combination of methyl-methacrylate (MMA) and photoresist (Fujifilm OCG-825) are utilized as an etch mask since the electron beam resists appear to leave behind less residues on the graphene surface than optical photoresists. (4) The photoresist (OCG) is patterned by photolithograhpy on top of MMA/graphene stack. This serves as an etch mask as both the MMA/graphene are then etched by reactive oxygen etching. (5) The MMA/OCG stack is then removed by solvents (acetone and isoproponal). The greek-cross structure shown in the top-

down profile in Figure 2-9 was chosen due to its scalability for smaller geometries as opposed to the standard square geometry which can often result in large errors due to ohmic alignment with the graphene mesa [99, 100].

The sheet resistance (R_{sh}) of these devices is measured utilizing the van der Pauw (vdP) method [101,102], while the Hall voltage (V_{hall}) is measured under a fixed magnetic field (B). Equation 2.1 and 2.2 show how from these two measurements both carrier concentration (n_s) and carrier mobility (μ_{hall}) can be extracted. Graphene devices were measured in ambient conditions on a custom built Hall-effect probe station with a permanent Neodynium Magnet ~0.3 T (shown in Figure 2-10). The injected current (I) was set to 0.1 mA and typical device dimensions ranged from 5-100 μm in size. Hall characterization has an advantage over field effect characterization due to the ability to measure both the carrier concentration and Hall mobility simultaneously. In addition, field effect characterization requires good electrostatic control of the Dirac point, which is often limited by the breakdown electric field of the dielectric (solid gate dielectrics limit the maximum measurable doping to $\sim 6 \times 10^{12}$ 1/cm^2). However, as we have shown with our Raman spectroscopy estimates, values for doping can easily exceed 1×10^{13} 1/cm^2:

$$V_{hall} = \frac{IB}{qn_s} \tag{2.1}$$

$$R_{sh} = \frac{1}{qn_s\mu_{hall}} \tag{2.2}$$

To double check and confirm our Raman measurements, we fabricated devices based upon our previous Raman treatments (Fig. 2-11). As expected, only the OTS (self-assembled monolayer) treated substrates are able to achieve low doping ($1-2\times 10^{12}$ 1/cm^2). As a comparison, we also measured Hall devices fabricated from single crystalline domains (SCG) of graphene. Our polycrystalline domain size was only 5-10 microns and the device placement was completely random, whereas, large single domain graphene was grown following reference [103] to increase the domain size of the graphene to >100 μm. SCG was chosen to ensure that each device was fabricated within a single domain of graphene, thereby avoiding any grain boundaries.

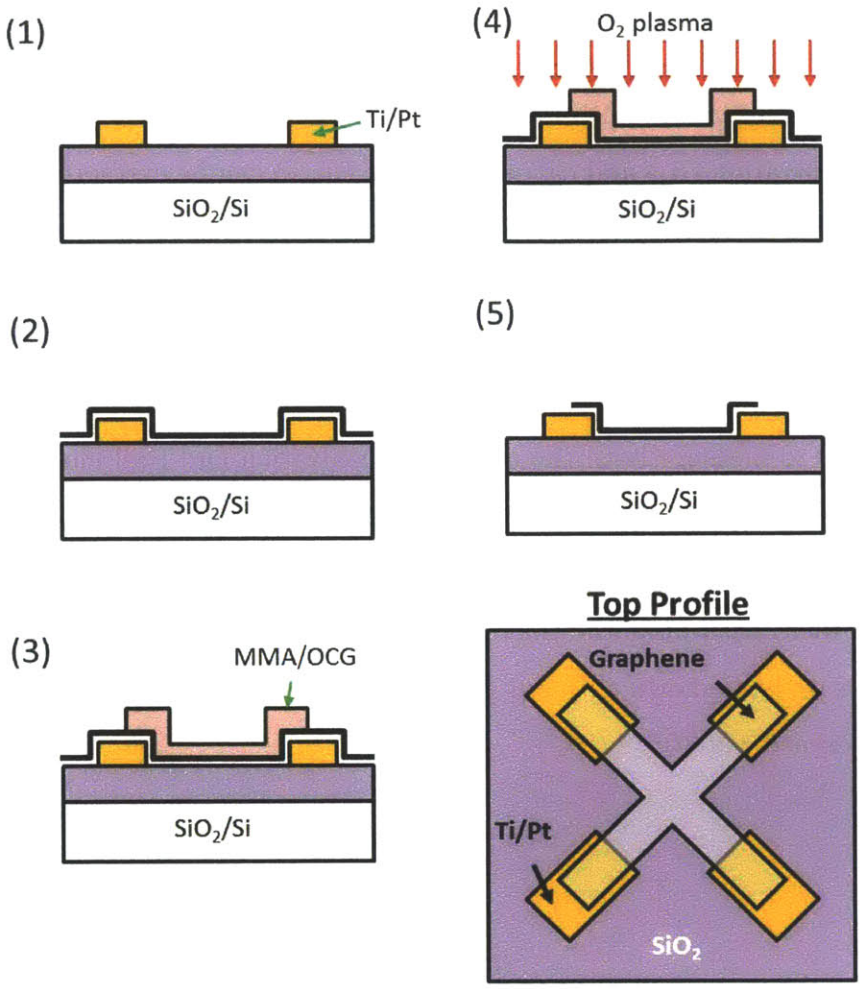

Figure 2-9: Hall Device Process Flow. (1) Ti/Pt (10 nm/20 nm) are deposited onto a thermally grown silicon dioxide substrate. (2) Graphene is then transferred ontop of these electrodes. (3) an MMA/OCG positive mask is spun on and then patterned by photolithography. (4) Reactive oxygen etching is performed to electrically isolate the graphene devices. (5) Solvent cleaning is used to remove the MMA/OCG mask. The figure in the bottom right hand corner shows a top-down diagram of the complete graphene device.

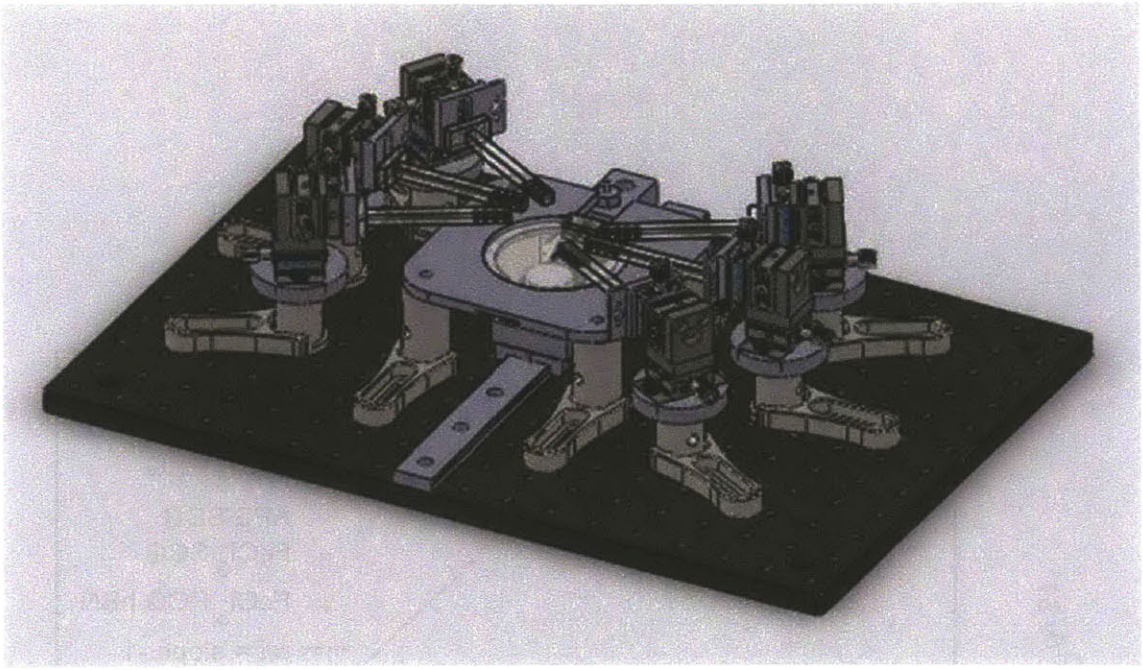

Figure 2-10: Solidworks Rendering of the home built Hall Effect Probe Station, utilizing a 0.3-0.4 T permanent magnetic. The fabricated Hall probe station allows for both +/- magnetic fields by easily flipping the magnet upside down.

However in the end, we did not find any correlation between the types of graphene (PCG or SCG) and doping level.

Previously in Chapter 1, we mentioned that for various types of dopants (defects vs. charge impurity scattering) the mobility of graphene can depend on the carrier concentration. Looking holistically at all of our devices that were tested and fabricated, we can fit equation 1.34 to our data plotted in Figure 2-12 (μ vs n_s) for various graphene samples including ambient pressure CVD graphene from Nickel [83], epitaxial Graphene Si-Face [60], HOPG on h-BN [53], LPCVD Cu Graphene + Al(ox) [10, 48], monolayer graphene on silicon dioxide [104] (Table 2.1). Unfortunately, due to the inhomogeneity in samples from CVD graphene grown from nickel, we were unable to fit equation 1.34 to this data set.

Figure 2-12 shows that our graphene quality is quite good as compared to epitaxial graphene from the Si-face; however, at high carrier concentration ($n_s > n_{imp}/n_{defects}$) we begin to see a predicted roll off in the carrier mobility. This roll off at high doping

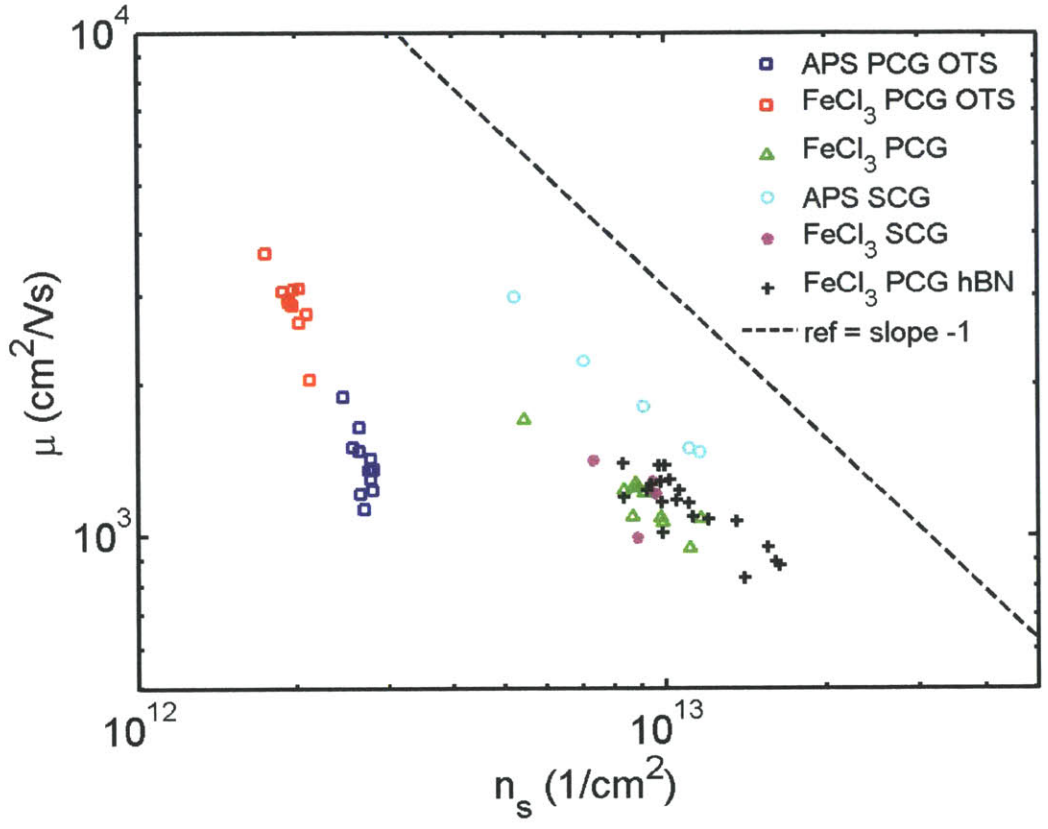

Figure 2-11: Hall Mobility versus Carrier Concentration for various sample treatments. PCG = polycrystalline graphene, SCG = single crystalline graphene, APS = ammonium persulfate, OTS = octa-decyltri-chloro-silane, hBN utilized in this experiment is monolayer hBN grown on copper by CVD [9]. The black dotted line denotes a slope of -1 which corresponds to $\mu \propto 1/n_s$

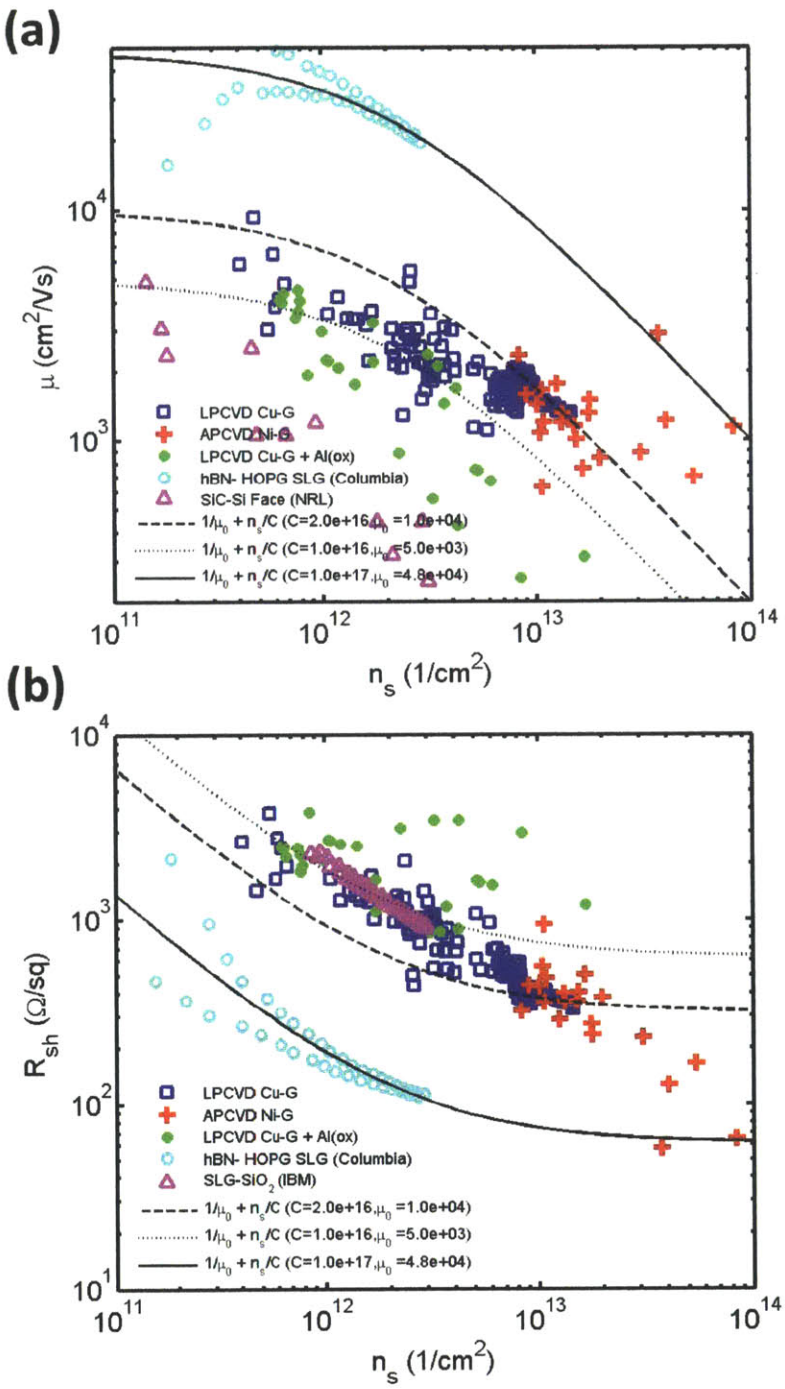

Figure 2-12: (a) Mobility versus carrier concentration for variety of graphene samples. Blue squares are LPCVD-Cu graphene, red crosses are APCVD-Ni graphene, magenta triangles are SiC-Si face, open circles are HOPG on h-BN, closed green circles are LPCVD Cu-G + Al(ox). (b) Sheet resistance as a function of carrier concentration - however the magenta triangle is monolayer graphene on thermally grown silicon dioxide. The continuous black lines represent the fitting from Eq. 1.34.

Material	μ_{imp} ($cm^2V^{-1}s^{-1}$)	n_{imp}/n_{defect}	R_{lim} (Ω-sq)
LP-CVD CuG	5000-10000	2-4	313-625
LP-CVD CuG + Al(ox)	4962	0.9	1449
HOPG-hBN	48000	2	62.5
SiC - Si Face	44828	0.02	-
APCVD NiG	-	-	-

Table 2.1: Fitting Parameters for Figure 2-12. Mobility due to impurity scattering μ_{imp}, the ratio of n_{imp}/n_{defect}, and the sheet resistance (R_{lim}) assuming only defect scattering as the carrier concentration (n_s) goes to ∞.

levels is perhaps better shown when plotting the R_{sh} vs. n_s of the samples. As we dope the sample more heavily, graphene's ultimate sheet resistance begins to saturate due to the short range scatterers caused by $n_{defects}$. This has great implications for applications requiring graphene for transparent conductive electrodes. While we can dope graphene very heavily, we eventually will be unable to lower R_{sh} indefinitely due to short range scattering events to which R_{lim} is sensitive.

However, after comparing our CVD graphene samples from copper to those of HOPG [104] and epitaxial graphene, we find that the carrier mobility of CVD graphene is quite comparable to that of HOPG. However, what does appear to make a large difference is the introduction of a thick hexagonal boron nitride layer [53]. Therefore, in addition to improving the intrinsic graphene itself and associated transfer techniques, work done in collaboration with Dr. Ki Kang Kim was carried out to find ways to integrate large areas of hexagonal boron nitride with our large area CVD graphene.

2.3 Hexagonal Boron Nitride

Since the initial demonstrations of hexagonal boron nitride as an ideal substrate for two-dimensional materials such as graphene [53], there has been a lot of interest in developing new synthesis techniques for large area hexagonal-boron nitride. Hexagonal boron nitride (h-BN) has a very similar crystal structure to that of graphene, except that instead of having a 2 atom carbon basis, the basis set now consists of a B and a N atom [105]. The strong dipole or ionic bond between B and N leads to

the formation of a wide band gap material ($E_{gap} \sim 5.78$ eV). This material has many similar properties to graphene - amazingly high thermal conductivity and mechanical strength. In addition, due to its 2D nature and fully passivated surface, this insulator serves as a remarkable substrate for 2D materials [53], enabling higher quality carrier transport by providing an extremely flat and uniform surface, thus reducing any effects due to ripples or wrinkles in the graphene.

While high quality graphite or HOPG is readily available, the same cannot be said of boron nitride. Motivated by the direct wide band gap properties of h-BN, work done by Watanabe, et al. have explored various routes for synthesizing this material [106]. Initial work focused on utilizing high temperatures >1500 °C and 5.5 GPa to achieve the synthesis of cubic BN, as well as, recrystallized h-BN from h-BN powders utilizing barium [106]. However, continuing upon their work at high temperatures and pressures, they also found that nickel could serve to dissolve h-BN, leading to the formation of recrystallized h-BN [107]. Synthesizing high quality crystals at both high temperatures and pressures is obviously very difficult; therefore, work done by Kubota et al. [108], thus demonstrated a slightly more accessible process for the formation of high quality h-BN by adding molybdenum to the metal solvent (Ni) to increase its nitrogen solubility, thus allowing ambient pressure synthesis. Consequently they were able to recrystallize and precipitate h-BN domains typically hundreds of microns in size [108]. It is currently this sole method that has provided the h-BN for many reports in the literature [53].

Since then much work has been done to produce similar quality crystals over larger areas similar to graphene [109–111]. Shi et al, demonstrated a low temperature synthesis route utilizing ambient pressure conditions using a gas precursor borazine ($B_3N_3H_6$), a similar precursor to benzene, to form polyborazylene, which upon annealing up to 1000 °C recrystallizes into h-BN on nickel thin films and then is transferred to a target substrate. Other chemical vapor deposition techniques have also been attempted, for example, utilizing ammonia borane (NH_3-BH_3) on copper results in the thermal catalytic decomposition of ammonia borane onto a copper surface forming h-BN thin films [110].

Figure 2-13: Scanning Electron Microscopy of Large Area hexagonal boron nitride synthesized on Iron foils from Dr. Ki Kang Kim.

2.3.1 h-BN Characterization

Recently, work still under investigation here at MIT has shown that high quality large area h-BN can be synthesized by CVD methods on iron foils. Utilizing a similar growth system as shown in Figure 2-1(a), and increasing the growth temperature up to 1100 °C, borazine ($B_3N_3H_6$) is introduced with the iron foil at low pressures ($\sim$1 Torr). The striking feature is that after synthesis relatively large domains (>10 μm) in triangular crystals are observable on the surface that completely cover the entire foil as shown in Figure 2-13 of an SEM image taken directly after synthesis of the h-BN, suggesting relatively thick hBN (>15 nm) which is advantageous as a substrate for graphene.

To better quantify the quality of our h-BN, we performed basic materials characterization of these h-BN films. h-BN has a Raman active mode that coincidentally sits very close to that of graphene's D peak (1350 cm^{-1}) caused by an in-plane optical phonon mode (1370 cm^{-1}) [24]. Therefore, similar to our graphene samples, we can

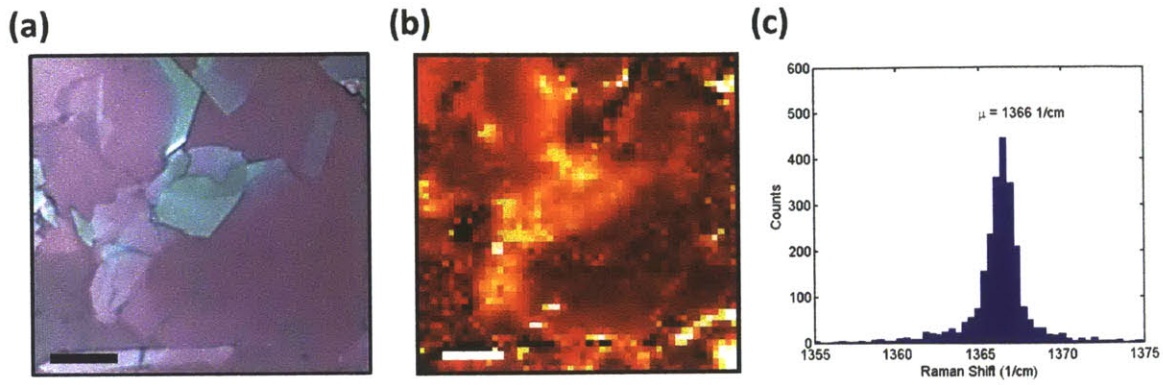

Figure 2-14: Raman Spectroscopy of Large Area CVD Hexagonal Boron Nitride (a) Optical Micrograph of CVD h-BN, (b) Raman Map of Peak Intensity of the h-BN peak. (c) Histogram of the h-BN Raman Peak Position. Scale Bar Indicates 10 μm for both (a) and (b).

also examine the Raman active mode of our h-BN substrate as a first confirmation of its material quality.

Figure 2-14 (a) shows the optical micrograph of the h-BN transferred onto silicon dioxide substrates. For the transfer of h-BN off of the iron foil, we followed similar transfer procedures as for graphene. PMMA was used as a supporting material and the underlying Iron was etched off utilizing HNO_3. The h-BN in Figure 2-14 (a) shows that there is some thickness inhomogeneity in our h-BN films. After performing a Raman scan over the same area, we automatically fit a Lorentzian peak to the Raman data and we plot the peak height in Figure 2-14 (b). The thicker regions show a much stronger Raman intensity, as to be expected. We can also plot the peak position of the Raman peak. If we look at the distribution of the data over the mapped region, we find that the average peak position for the in-plane Raman mode is 1366 cm^{-1}, which agrees quite well with the bulk values of 1370 cm^{-1}. The small discrepancy between our measured values and the bulk value in the literature could be attributed to strain due to the relatively thin films of h-BN. Unfortunately, unlike the D peak of graphene, the in-plane mode of h-BN does not provide us with much information about the defect density of the h-BN sample.

In order to quantify the quality of the large area h-BN, more sophisticated tech-

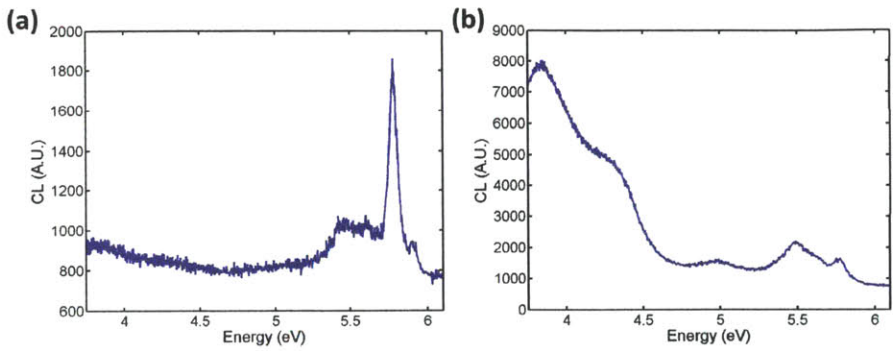

Figure 2-15: Cathodeluminescence of CVD h-BN taken at 5K using an Attolight integrated SEM + CL option. (a) Local CL data from the h-BN sample showing some high quality regions emitting light at an energy of 5.777 eV or 214.6 nm (b) Potentially some color centers exist within the hBN suggesting some trap states located at 3.837 eV, 4.262 eV, 4.981 eV, and 5.489 eV.

niques are necessary. Therefore, utilizing a modified scanning electron microscope for cathodeluminescence (CL) measurements, we can excite electron-hole pairs in large band gap materials by directly injecting electrons into the material and collecting the emitted light. For these experiments, we worked with a commercial CL-SEM tool from Attolight. Measurements were carried under vacuum conditions ($< 10^{-5}$ mbar) at both 5K and 300K utilizing a 5 keV electron beam with an emission current of approximately 120 μA. Figure 2-15 (a) shows a localized CL (cathodeluminescence) spectrum measured from one of our CVD h-BN samples transferred onto silicon dioxide. Figure 2-15 (a) shows that high quality h-BN is achievable using this method as we see a relatively sharp peaks at 5.78 eV (or 214.6 nm) which agrees well with values in literature [106, 108]. However, we do find that in certain regions of the sample a much larger intensity and broader CL emission background is often measured. The peak positions are listed in Table 2.2. The emission peaks located near 4 eV have traditionally been associated with impurities and structural defects, perhaps due to nitrogen vacancies or carbon impurities [112]. As for the peaks near 5.5 eV associated with defects, the origin of these peaks is debatable. Due to the strong in-plane binding energy in two dimensional materials, the peaks at both 5.78 and 5.5 eV are often attributed to excitonic peaks in hexagonal boron nitride, suggesting an even larger

Peak Number	Energy (eV)	Wavelength (nm)
1	3.837	323.1
2	4.262	290.9
3	4.981	248.9
4	5.489	225.9
5	5.773	214.7

Table 2.2: Peak Positions from Figure 2-15 (b).

direct band gap energy than that measured by CL [106, 108, 112].

After basic confirmation by Raman and CL characterization of the material quality, our actual interest in the h-BN material is still for its electronic properties. Therefore, in order to evaluate the electrical performance of CVD h-BN synthesized by Fe, we first measure the vertical (normal to the planar direction) electrical transport properties of this material (1) relative dielectric constant (ϵ_r) and (2) Breakdown Electric Field (E_{MAX}). These properties not only provide further material characterization of the synthesized h-BN, but are also important for many groups that are interested in utilizing CVD h-BN not only as a substrate material for graphene, but also as a two-dimensional tunneling barrier or integrated gate dielectric for 2D layered materials [9, 53, 113–115]. To measure the electrical performance of our material, we fabricated Metal-Insulator-Metal (MIM) capacitors. Figure 2-16 (a) shows a schematic of the device we used. First non-oxidizing metal electrodes (10 nm Ti/ 20 nm Pt) were patterned by lift-off using electron-beam lithography onto a 1 μm thick thermally grown silicon dioxide wafer. Then CVD h-BN was transferred on-top as the gate dielectric through by protecting the CVD h-BN with PMMA and etching away the iron substrate using commercial iron etchants. The second metal electrode (50 nm Pd) is deposited on-top forming a cross-bar structure. 50 nm of Pd was chosen as the top electrode as a low stress metal to avoid delamination of the underlying h-BN. Furthermore, the thick 1 μm thermally grown SiO_2 wafer was chosen to help minimize the parasitic capacitance between the pads and the silicon substrate underneath.

Figure 2-16 (c) shows the current density (J) versus applied electric field (E_{DS}). Devices were measured at room temperature under vacuum conditions in a Lakeshore VPX Cryoprobe station utilizing an Agilent Semiconductor Parameter Analyzer (4155C).

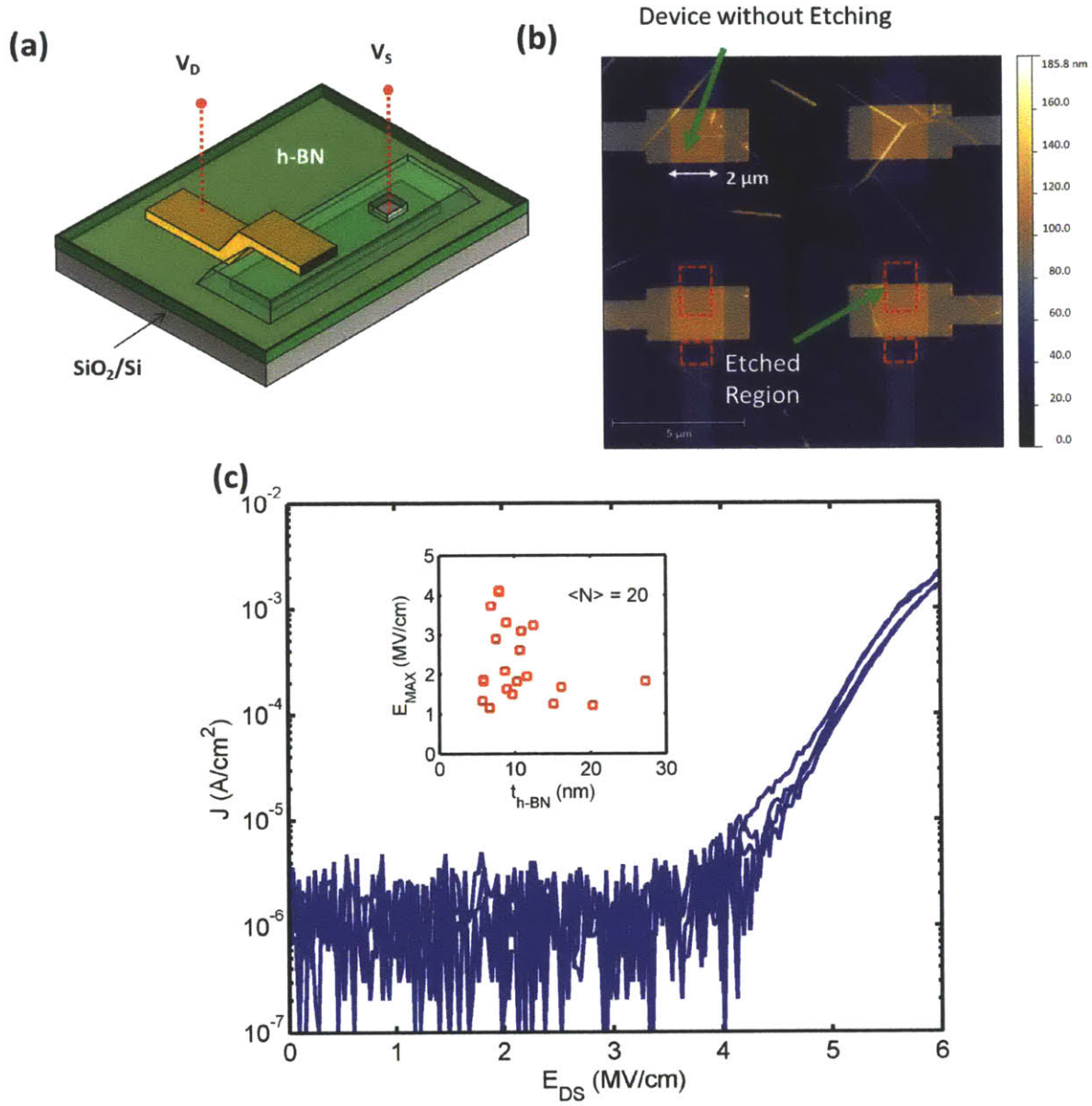

Figure 2-16: h-BN Electrical Characterization (a) Schematic of Metal-h-BN-Metal Capacitor and Electrical Breakdown Measurements. (b) AFM of fabricated Devices showing etched regions used to determine the thickness of the h-BN. (c) J versus E_{DS} for the measured devices. Inset shows the E_{MAX} as a function of various thicknesses of h-BN.

The electric field was computed by measuring the thickness (t_{h-BN}) of the h-BN for each device. The thickness was determined by atomic force microscopy (AFM) after patterning and etching the h-BN under a standard CF_4/O_2 (40 sccm/4 sccm) at 198.8 W at 10 mtorr in a reactive ion etcher (NEXX-RIE). The lower Ti/Pt electrode served as a natural etch stop for the plasma etching. All devices measured for electrical breakdown consisted of a 1 μm $\times$ 1 μm overlap of electrodes. We defined a breakdown current at $\sim 10^{-5}$ A/cm^2, which corresponds to a raw current of 0.1 pA, this current is seen in Figure 2-16 (c) as just being above the noise floor of our measurement system. In total, 20 devices were measured for breakdown. The inset in Figure2-16 (c) shows the E_{MAX} for varying thickness of the device. The typical thickness that we were able to achieve was ~8-15 nm of h-BN with a $E_{MAX} \sim$ 2-4 MV/cm. This value is within reasonable measurements for h-BN [116]. The lower breakdown value, as we will discuss later, we believe to be due to the wrinkles and defects in the h-BN after transfer.

Utilizing similar devices except for a larger 2 μm $\times$ 2 μm overlap (A_{device}), we also measured the capacitance of the devices and utilized similar techniques for measuring the thickness (t_{h-BN}) to convert the measured capacitance into a relative dielectric constant (ϵ_r). Utilizing, an Agilent Impedance Analyzer (4294A), we measured the small signal capacitance (C_{meas}) as a function of input frequency (100 Hz to 100 kHz) utilizing a 50 mV input signal with zero DC applied bias (Fig. 2-17). For most devices, we found that the capacitance was relatively constant as a function of input frequency and for the data shown in Fig. 2-18, we chose to look at C_{meas} only at a fixed input frequency of 1 kHz. After measuring many devices (N=61), we actually compensated for parasitic capacitances (C_{par}) by looking at the capacitance as a function of h-BN thickness. Following equation 2.3, where ϵ_0 is the vacuum dielectric permittivity, we obtained

$$C_{meas} = \frac{\epsilon_r \epsilon_0 A_{device}}{t_{h-BN}} + C_{par} \tag{2.3}$$

Therefore, looking at many of the relatively thick devices, we actually extracted

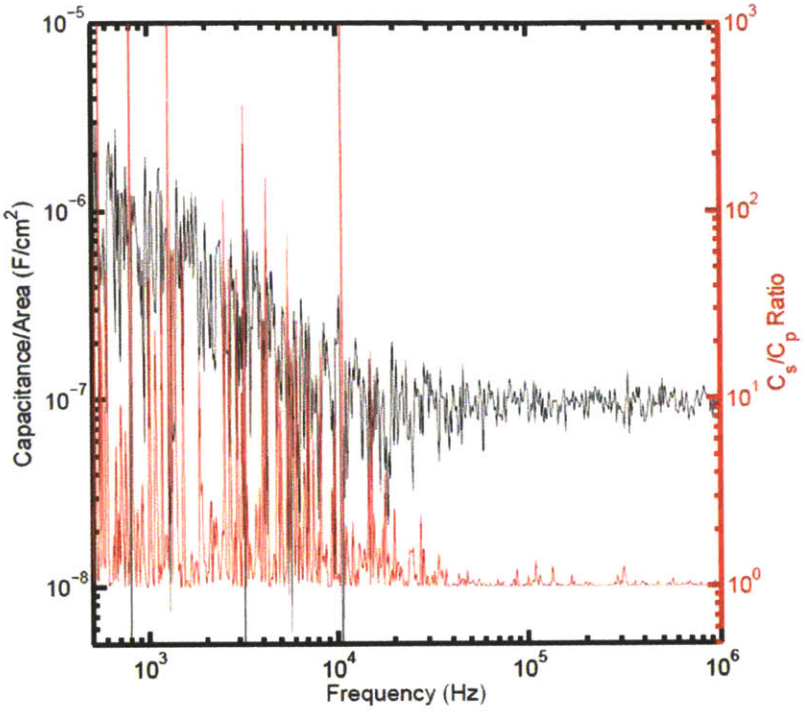

Figure 2-17: Capacitance as a function of Excitation Frequency. Left axis the is extracted capacitance per unit area, while the right axis is the ratio between a modeled series capacitance (C_s) and the measured parallel capacitance (C_p). Low values of the ratio C_s / C_p imply a low current leakage in the devices.

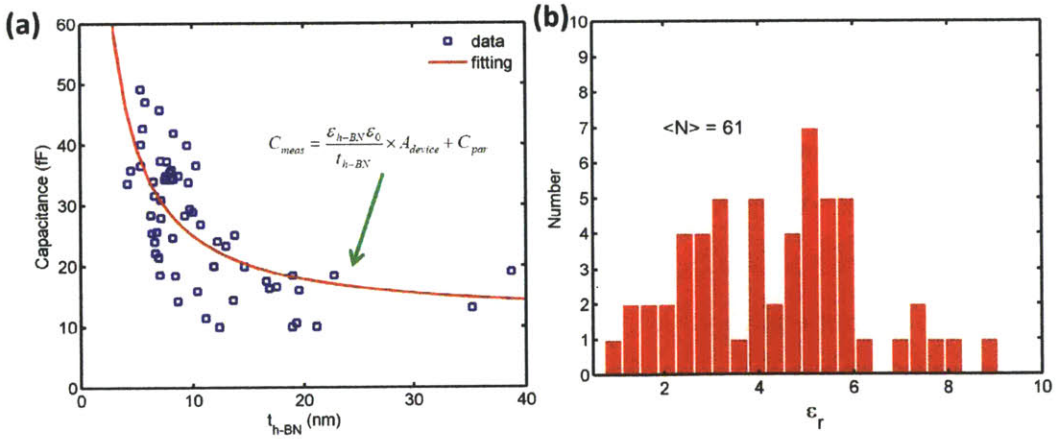

Figure 2-18: h-BN Electrical Characterization (a) Capacitance as a function of the h-BN thickness (t_{h-BN}) (b) Histogram of the dielectric constant for the 61 samples.

a typical $C_{par} \sim 15$ fF. Since most of this parasitic capacitance is in parallel with our device, we subtracted this parasitic value from our data set before computing the relative dielectric constant. The extracted dielectric constant for 61 devices is shown in Figure 2-18 (b). The average range of relative dielectric constants range from 2-6, which is consistent with expected values [9]. The large range or distribution, we also believe is due to the varying thickness of hBN. This was seen previously in Figure 2-16 (b), which shows an AFM image of the capacitor, where wrinkles are clearly observable within the device. From the above electrical characterization (Capacitance and Breakdown Electrical Field), the CVD h-BN is sufficient for utilization as a gate dielectric material and has good vertical electrostatic integrity.

2.3.2 h-BN + Graphene Integration

However, a major application for h-BN is as a passivated surface for use in conjunction with graphene and other 2D materials. Recently, exfoliated h-BN [29] has resulted in high performance devices but only has a limited spatial coverage; therefore, we also measured the performance of large area CVD graphene integrated with our large area CVD h-BN over mm length scales. For this study, large area CVD h-BN was transferred onto standard 300 nm thermally grown silicon dioxide wafers. After transfer, large area single crystalline graphene (SCG) was grown with a typical domain size $>$ 100 μm. As a control reference, the same CVD graphene was also transferred onto a reference SiO_2 wafer. Multi-terminal devices were then fabricated from each sample to avoid any contact resistance artifacts in the measurements. Optical micrographs of the completed device are shown in Figure 2-19(a). The typical channel width (W) and length (L) are 1.5 μm and 2 μm, respectively. The inset shown in Figure 2-19 (a) is an AFM scan of the device after fabrication. The rough topology is believed to be due to the multiple transfer of films as has been seen for work done for multiple transfers of graphene used for transparent conductive electrodes. Utilizing a 4 terminal measurement of the devices, with a $V_{DS} \sim$100 mV, we measured the conductance (σ) of our channel as a function of applied backgate (V_{BG}) to the conductive silicon at 300 K. Representative σ vs V_{BG} plots are shown in Figure 2-19 (b). The CVD

Substrate	n_{dirac} ($\times 10^{12}$1/cm^2)	μ_p (cm^{2}V^{-1}s^{-1})	μ_n (cm^{2}V^{-1}s^{-1})	Number of Devices
SiO_2	1.31±0.41	6091±1252	5494±1256	18
CVD h-BN/SiO_2	0.71±1.27	7490±4773	4407±3230	44

Table 2.3: Table of Graphene Doping and Mobility comparing two substrates SiO_2 and CVD hBN/SiO_2

graphene on CVD h-BN shows a much sharper Dirac cone than for the CVD graphene samples on SiO_2, which indicates a more uniform graphene sample with regards to charged impurities in the substrate. The hole and electron mobility (μ_p and μ_n) was extracted from the peak slope following the equation 2.4:

$$\mu_{n,p} \cong \frac{1}{C_{ox}} \frac{d\sigma}{dV_{BG}} \tag{2.4}$$

where C_{ox} is assumed to be capacitance per unit area of the underlying substrate (300 nm SiO_2). Due to the increased thickness of the substrate gate dielectric due to thin layers of h-BN, these extracted values are actually underestimates of the actual mobility values.

In addition, we also extracted the backgate charge neutrality point (V_{CNP}) or the Dirac point for the device and converted it into a charge carrier concentration (Eq. 2.5) as a measurement of the intrinsic doping of the samples. The extracted hole mobility (μ_p) and n_{dirac} for both of the substrates (CVD h-BN and SiO_2) are plotted in Figure 2-19 (c). A summary of the device performance is included in Table 2.3.

$$n_{dirac} = \frac{C_{ox}}{qV_{CNP}} \tag{2.5}$$

Consistently, on average the doping of the CVD graphene on CVD h-BN is lower than the reference SiO_2 sample, which we believe is due to the low number of dangling bonds found on the CVD h-BN surface. This lower number of dangling bonds also appears to translate over to the mobility measurements (μ_n and μ_p) of CVD graphene. While there is a large variance of CVD graphene quality, we are still able to find many devices with mobility $>$ 10,000 cm^{2}V^{-1}s^{-1}, with potentally a peak value of $\sim$ 24,000 cm^{2}V^{-1}s^{-1}. Due to the large variation in devices on h-BN, the average electron

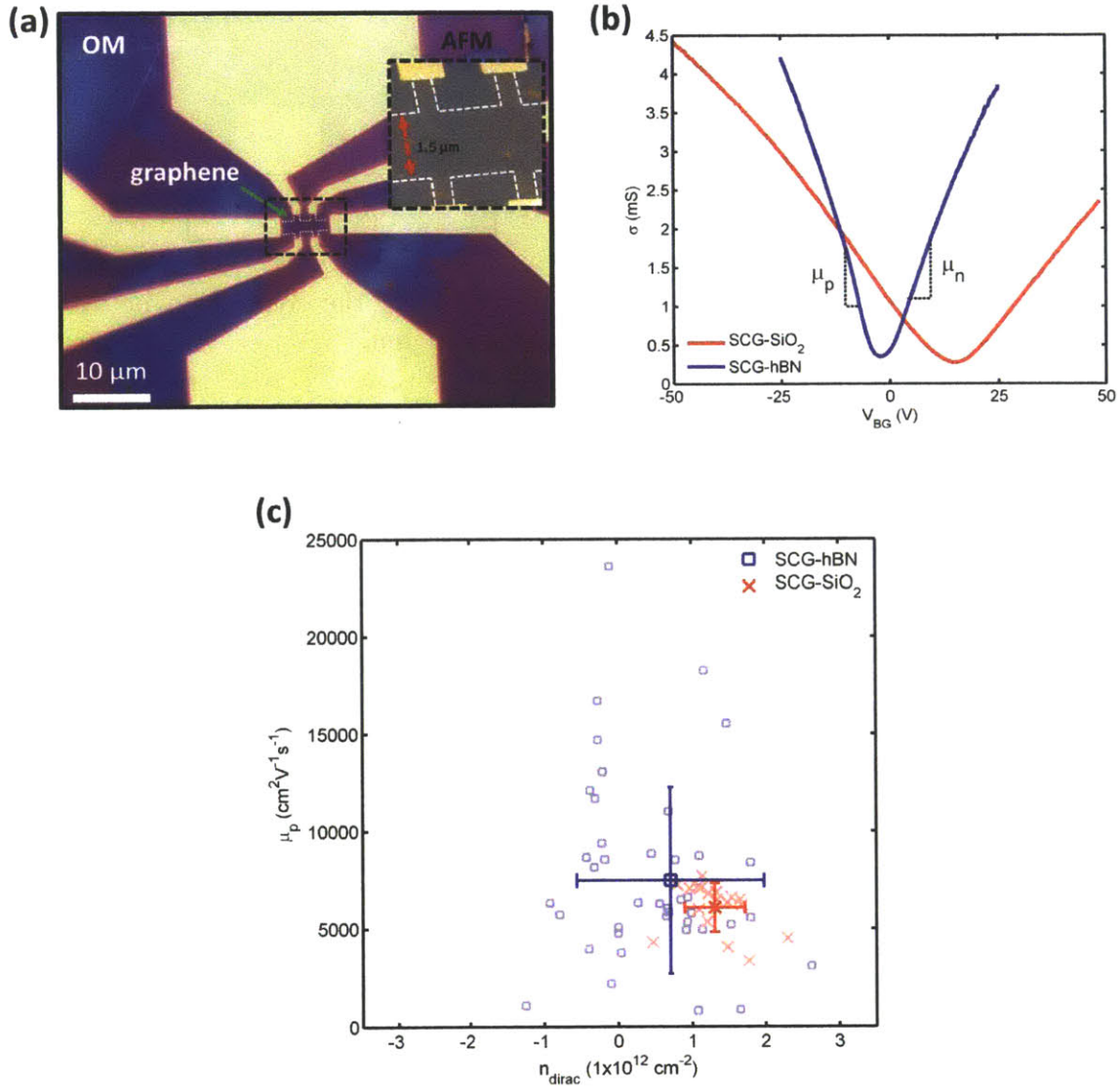

Figure 2-19: Graphene and h-BN Integrated Devices (a) Optical Micrograph of CVD Graphene integrated on top of CVD h-BN (b) Conductance as a function of backgate voltage (V_{BG}). (c) Extracted Hole Mobility as a function of Shift of Dirac Peak (n_{dirac})

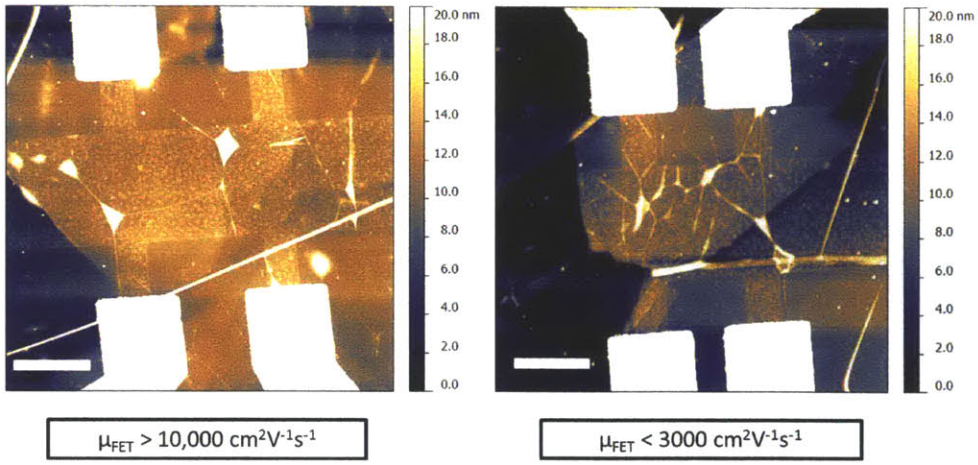

Figure 2-20: AFM images of various devices showing the connection between the mobility and the uniformity. Scale bar is equal to 1 μm.

mobility (μ_n) of graphene on h-BN is actually lower than graphene on silicon dioxide; however, the achievable peak mobility value still remains higher on graphene on h-BN than SiO_2. It is expected that the large distribution in values is related more to the quality of graphene transfer rather than the variations in the material quality of the h-BN. We investigated many of the high performance and low performance devices and find that large bubbles and non-homogeneity during transfer appear to smear out the conductance curves resulting in a lower extracted mobility (Figure 2-20). With improved transfer techniques in the future, we believe higher and more consistent mobility values can be achieved; however, the current h-BN is indeed already useful as a large area substrate for graphene electronics.

As an additional comparison, we also measured devices utilizing different transfer conditions (annealing vs. acetone), substrates (OTS vs. h-BN vs. SiO_2) and various types of graphene (PCG vs. SCG), to see if there was any measurable effect. Figure 2-21 shows the extracted field effect hole mobility for a variety of devices as function of n_{dirac}. Similar to before, we see that the OTS treated substrates serve a similar role in reduction of doping; however, we do find that the doping after device fabrication and measured under vacuum at room temperature in a Lakeshore cryoprobe station show a significantly lower doping than our ambient measured Hall devices. Table 2.4

Type	Substrate	Transfer	n_{dirac} ($\times 10^{12}$1/cm^2)	μ_p (cm^{2}V^{-1}s^{-1})	μ_n (cm^{2}V^{-1}s^{-1})	N
PCG	SiO_2	Anneal	1.68±0.28	3690±1448	3102±1369	30
SCG	SiO_2	Anneal	1.31±0.41	6091±1252	5494±1256	18
SCG	CVD h-BN/SiO_2	Anneal	0.71±1.27	7490±4773	4407±3230	44
PCG	SiO_2	Acetone	1.50±0.13	4259±1816	3666±1660	30
SCG	SiO_2	Acetone	1.62±0.46	6397±1095	5301±1312	24
SCG	CVD h-BN/SiO_2	Acetone	1.07±1.30	7076±3647	4042±2849	36
SCG	OTS/SiO_2	Anneal	0.60±0.19	7627±2490	4775±1822	16

Table 2.4: Table of Doping and Mobility comparing SiO_2 and CVD hBN/SiO_2 substrates for graphene devices. All graphene samples were etched using $FeCl_3$

shows the full compiled data set on extracted device parameters.

In conclusion, we have investigated many aspects of graphene synthesis and transfer. We have confirmed the trends we have seen from Raman spectroscopy with actual device transport data. The key factors appear to be related to the hydrophobicity of the substrate, as well as, the passivation of the silicon dioxide utilizing hexagonal boron nitride. The average achievable carrier mobility from copper grown CVD graphene ranges from 1000-6000 cm^{2}V^{-1}s^{-1} on SiO_2, with potential improvements through the improvement of uniformity of devices transferred onto CVD h-BN. In chapter 3, we will discuss the fabrication of transistors made from the graphene optimized in this chapter.

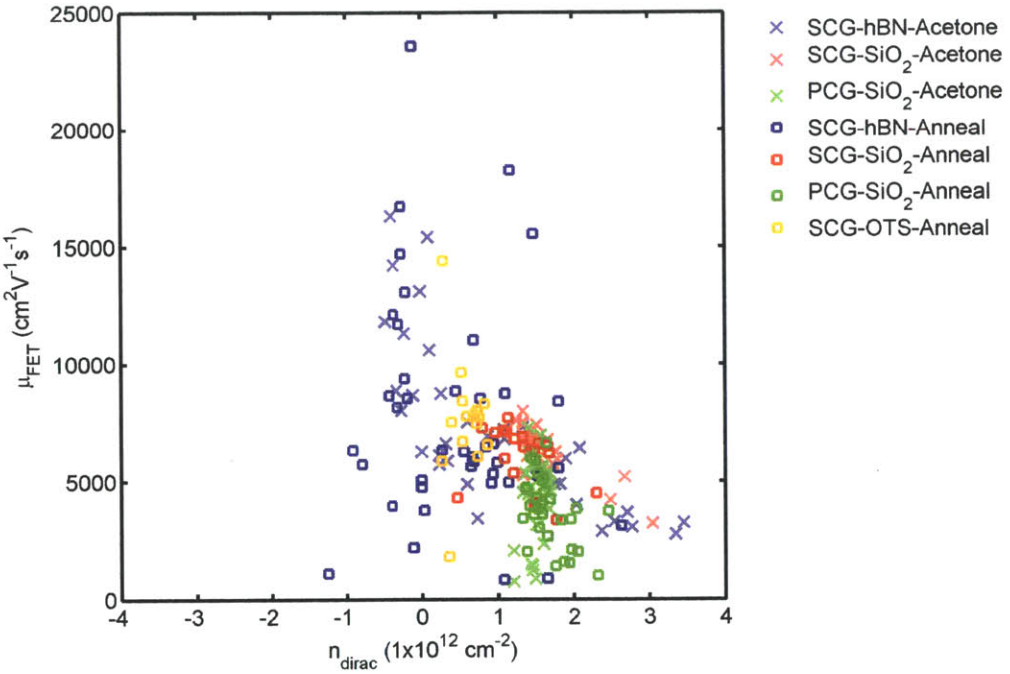

Figure 2-21: Field Effect Hole Mobilities (μ_{FET}) from back-gated devices

Chapter 3

Process Optimization

Much of the appeal behind 2D materials over other low dimensional structures, such as nanotubes, is their compatibility with conventional planar processing technologies. In Chapter 2, we have already discussed some of the issues related to the doping of graphene, as well as, the impact of substrate interactions (h-BN and OTS treated SiO_2) on the mobility and carrier transport within graphene. In this chapter, we will focus on the primary technological issues for device integration, as well as, challenges for fabrication and control of these materials: (1) Contact Resistances and (2) Gate Dielectrics. With regards to contact resistances, this section will go more indepth on the fundamental interactions between graphene and metals by exploring the structural, chemical, and electronic modifications between these two materials when they are in contact. Finally, while our earlier experiments have involved the use of field effect devices - most of these devices were meant as test structures for materials characterization, as opposed to utilization as fully optimized radio frequency (RF) devices. When going from a test structure to a real device for high frequency operation, a variety of factors, such as contact resistance, can no longer be neglected. In addition, parastic capacitances can also no longer be ignored. Therefore, the last part of this chapter will focus primarily on high-frequency devices optimized for graphene-specific circuits.

3.1 Contact Resistance

Graphene devices show amazing promise for high speed applications due to their intrinsic ultra-high mobility; however, while their intrinsic materials properties are exciting, for many engineers looking at graphene for device applications, scalability is just as important as a material's intrinsic properties. One of the main issues with all device technologies is that of contact resistance. While the channel dimension and gate length of a transistor can continue to shrink in size, the transfer length (L_T) associated with the contact resistance (R_C) is a fixed quantity that determines the size of the contact region and thus the density of transistors. Currently in graphene devices, contact resistances range anywhere from 200-2000 $\Omega - \mu m$ [10, 117–123]. Unfortunately, these values are still an order of magnitude higher than what is typically found in silicon $\approx$ 20-50 $\Omega - \mu m$ [124]. This excess source and drain resistance (R_s & R_d) can also greatly decrease the maximum unity current gain frequency (f_T) in a transistor shown in Eq. 3.1 [125]:

$$f_T = \frac{g_m/(2\pi)}{[C_{gs} + C_{gd}] \cdot [1 + (R_s + R_d)/R_{ds})] + g_m C_{gd}(R_s + R_d)} \tag{3.1}$$

where g_m is the transconductance, C_{gs} and C_{gd} are the gate to source and gate to drain capacitances, respectively, R_s and R_d are the parasitic source and drain resistances, and R_{ds} is the output resistance (r_0) of the device.

Figure 3-1 illustrates the various factors that can influence R_c: (1) the interface quality (ρ_{int}), (2) the sheet resistance of the material underneath the metal (R_{sh}), and (3) the work function mismatch between the channel underneath the metal and the channel itself (R_{dep}) [126]. Typically R_{dep} makes a much smaller contribution to R_c due to the lack of a band gap in graphene and is ignored in the following calculations [127]. Utilizing a distributed resistance network or a transmission line, we can separate the components of the contact resistance into two separate components: (1) a differential interface resistance R_{int} and (2) a differential sheet resistance underneath the contact $\Delta R_{G/M}$ as shown in Equation 3.2 and 3.3:

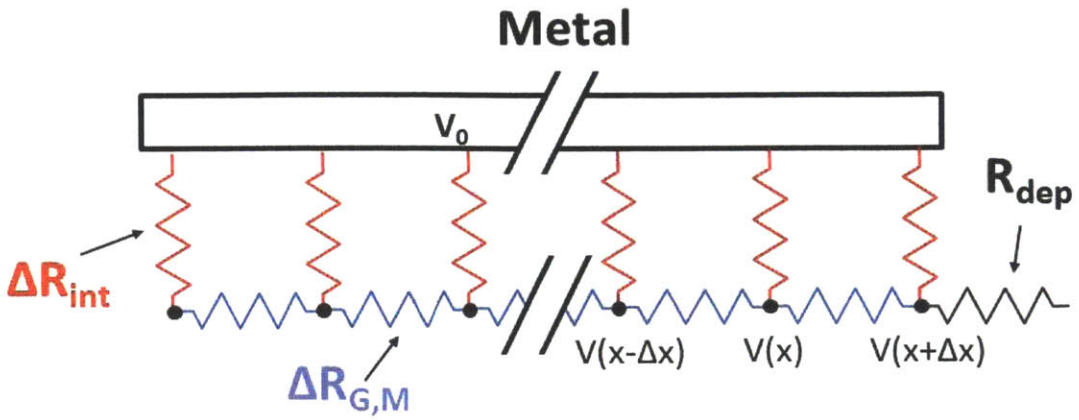

Figure 3-1: Diagram of the Distributed Resistance of the Metal/Graphene Contact Resistance

$$\Delta R_{int} = \frac{\rho_{int}}{W}\frac{h_{int}}{\Delta x} = \frac{\rho_c}{W\Delta x} \tag{3.2}$$

$$\Delta R_{G/M} = R_{sh}\frac{\Delta x}{W} \tag{3.3}$$

where h_{int} is the vertical distance travelled, W is the width of the contact, δx is a incremental distance. Due to the uncertainty in h_{int}, often it is better to express the product of ρ_{int} and h_{int} as a specific contact resistance (ρ_c) [128]. Equations 3.4 and 3.5 are the constitutive coupled differential equations for computing the voltage (V(x)) or current (I(x)) in the graphene underneath the metal. By solving equation 3.6, we can calculate the voltage distribution underneath the metal contact:

$$\frac{dI(x)}{dx} = \frac{W}{\rho_c}[V_0 - V(x)] \tag{3.4}$$

$$\frac{dV(x)}{dx} = \frac{R_{sh}}{W}I(x) \tag{3.5}$$

$$\frac{d^2V(x)}{d^2x} = \frac{R_{sh}}{\rho_c}[V_0 - V(x)]. \tag{3.6}$$

where, V_0 is the applied voltage at the contact metal. The second order differential

equation in Eq. 3.6 has a homogenous solution (second order polynomial) and a particular solution (hyperbolic sine and cosine). By matching boundary conditions such that V(0) = 0 and V(L) = V_0, we can express the contact resistance (R_C) in equation 3.7 as

$$R_C = \frac{\sqrt{R_{sh}\rho_c}}{W} \times \frac{1}{tanh(L/L_T)} \tag{3.7}$$

where, L is the length of the entire metal contact, and we define a characteristic length as the transfer length ($L_T = \sqrt{\rho_c/R_{sh}}$). Therefore, typically L » L_T to ensure negligible additional contact resistance; however, as devices shrink, L_T must also scale appropriately in order to ensure that while the gate of a device can become very small, if the contacts are physically large, then the device density is impeded. However, it is clear that to reduce the parasitic contact resistance, the quality of the graphene underneath the metal (R_{sh}) is of critical importance, as well as, the transport resistivity vertically (ρ_c). Unfortunately, little is known about the interaction between 2D materials and metals. Recently, theoretical and experimental work done by IBM has looked at the limit of graphene-metal junctions and the origins of this contact resistance [129]. They examined the anomalous temperature dependence of the contact resistances and noticed a 35 % reduction in contact resistance from 300 K to 6 K, which is the opposite trend to expect, assuming that the contact resistance is mainly dependent on the thermionic emission over a potential barrier. According to their analysis, they attribute this effect mainly due to a shift in transport from diffusive transport at room temperature (300 K) to ballistic transport at low temperatures (6 K) of the graphene underneath the contacts. This further suggests that the quality of the material underneath the metal may be crucial for lowering contact resistances. In addition, there are many other factors for achieving low contact resistances: metal wetting, graphene doping, interface quality, etc. Therefore in this section of the thesis, we will focus on addressing our understanding of graphene/metal interactions: first beginning with the optimization of graphene/metal processing for ohmic contacts and then finally discussing, in more microscopic detail, the interfacial

physics between graphene and various transition metals.

3.1.1 Ohmic Device Processing

Due to our primary interest in utilizing graphene potentially for high speed radio frequency electronic applications, the first problem in working with graphene is how to process materials such as graphene utilizing standard organic photoresists to ensure a low contact resistance. Organic residues, due to the use of photoresist or e-beam polymers, often are hard to remove due to van der Waals forces; furthermore, the selective removal of the sp^3 bonded carbon without damaging the 2D material is very difficult to integrate into a process flow [10, 121]. Generally, high temperature processing steps are usually used to further improve metal contacts [121], although the interaction of the graphene and the substrate at high temperatures may degrade the transport properties. Following standard lift-off processes, we typically measure $R_C W \approx 2500\ \Omega - \mu$m (using Ti/Pd/Au and Ti/Au), from transmission line measurements on our CVD graphene. Due to the strong interaction between the photoresist and the graphene, we investigated the addition of an inorganic buffer layer placed between the graphene and the photoresist. By providing a separate layer in between the photoresist and the graphene, we can use wet chemical etching to restore a high selectivity between the developer of the photoresist and the inorganic buffer layer. For the interfacial buffer layer chosen, we utilized Al for 4 reasons: (1) Al oxidizes very strongly on a graphene surface [48]. (2)Al is already used in graphene technology as a seed layer for gate dielectric deposition [48]. (3) Thin layers of Al oxidize readily which can also serve as a gate dielectric without the need for additional atomic layer deposition. (4) Al can be selectively etched in tetra-methyl ammonium hydroxide (TMAH), which is found in many developers [130].

Figure 3-2 shows the resulting X-ray photoemission spectra (XPS) of 2.5 nm of Al electron beam evaporated onto the surface of graphene and onto the surface of SiO_2. As intended, we find that the Al oxidizes more readily when deposited onto graphene then when deposited onto SiO_2. As we will discuss later in this section, due to the low free surface energy of graphene, many metals do not appear to be wetting the

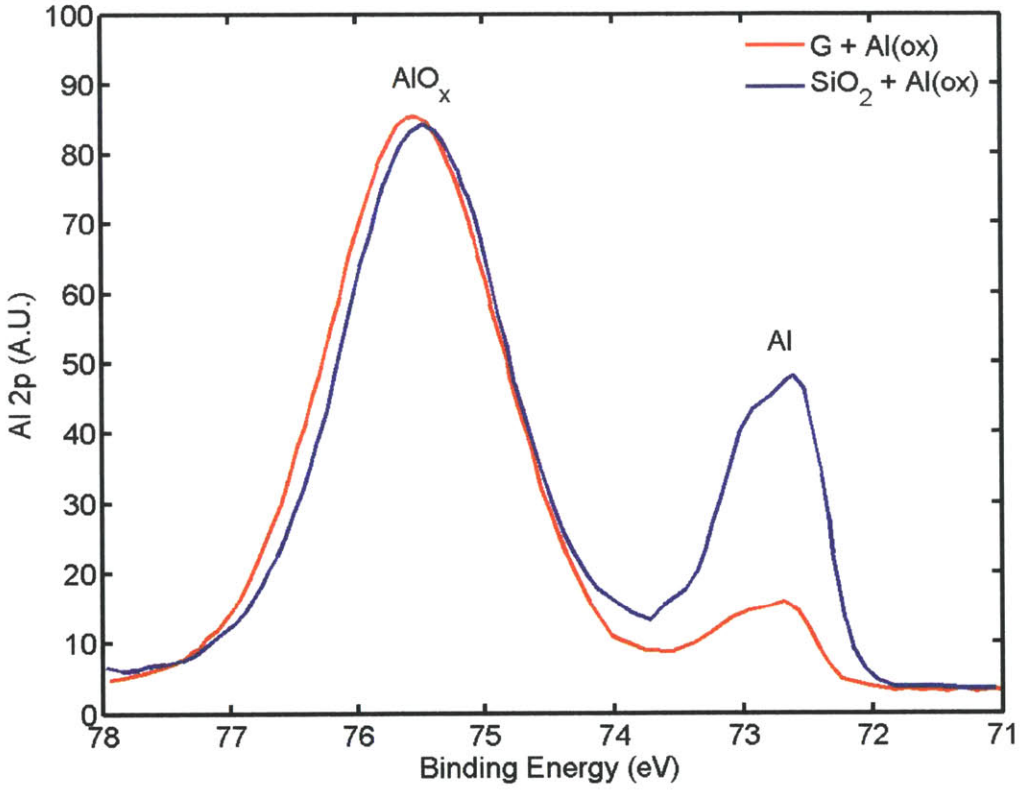

Figure 3-2: XPS Spectrum of 2.5 nm of Al deposited onto Graphene (red) and SiO_2 (blue). The XPS spectrum shows one peak corresponding to oxidized aluminum (E_B = 75.53 eV). The metallic Al peak is located at (E_B = 72.68 eV).

graphene surface, resulting in their island-like deposition on top of graphene. This porous configuration thus enhances the oxidation of Al at the Al/Graphene interface, as compared to the Al/SiO_2 interface. Therefore, we set out to evaluate the effect of introducing this inorganic buffer layer into our ohmic device processing.

The graphene films used in this work were also grown by CVD on copper substrates as described in the previous chapter. Films were then transferred using poly(methyl methacrylate) (PMMA) onto polished Si wafers with 300 nm of thermally-grown SiO_2 on their surface. PMMA was removed with a forming gas anneal (H_2/Ar) at 500 °C for 1 hour. Two samples were fabricated as shown in Figure 3-3. Sample #1 had a 5 nm Al cap layer deposited by electron-beam evaporation and oxidized under ambient conditions after transfer to the Si wafer (2.5 nm deposited/oxidized twice), while Sample #2 had no Al cap layer. Device fabrication starts with the patterning of the ohmic contacts. A 1.5 nm Ti/ 45 nm Pd/ 15 nm Au metal stack is deposited by e-beam evaporation and patterned by lift-off with AZ5214E photoresist and AZ422 developer. In Sample #1, the Al cap layer is etched simultaneously during the development of the Al(ox) by the AZ422 developer, which contains dilute tetramethyl ammonium hydroxide (TMAH). Device isolation is achieved by wet etching the Al(ox) and etching the graphene with an O_2 plasma for 30 seconds. Devices were measured in a Lakeshore Cryogenic Probe Station under vacuum (1.4×10^{-4} Torr).

To confirm the presence of interfacial polymer residues at the surface, atomic force microscopy images of the ohmic lift-off regions immediately before metal deposition are shown for Sample #2 and Sample #1 in Fig. 3-4(a) and 3-4(b), respectively. Following standard lift-off processing procedures, Sample #2 results in a surface arithmetic mean roughness (R_a) and root mean square roughness (R_q) of 1.26 and 1.00 nm, respectively (Fig. 3-4(a)). However, in Sample #1, the photoresist residue is significantly reduced as 2-3 nm wrinkles (due to thermal expansion mismatches from growth and transfer) are clearly seen in Fig. 3-4(b), and $R_a = 0.23$ nm and $R_q = 0.20$ nm in this case. As a reference, CVD graphene on thermally grown SiO_2 immediately after transfer has R_a=0.25 nm and $R_q = 0.2$ nm. The increased surface roughness in Sample #2 is due to photoresist residue leftover after development. Similar poly-

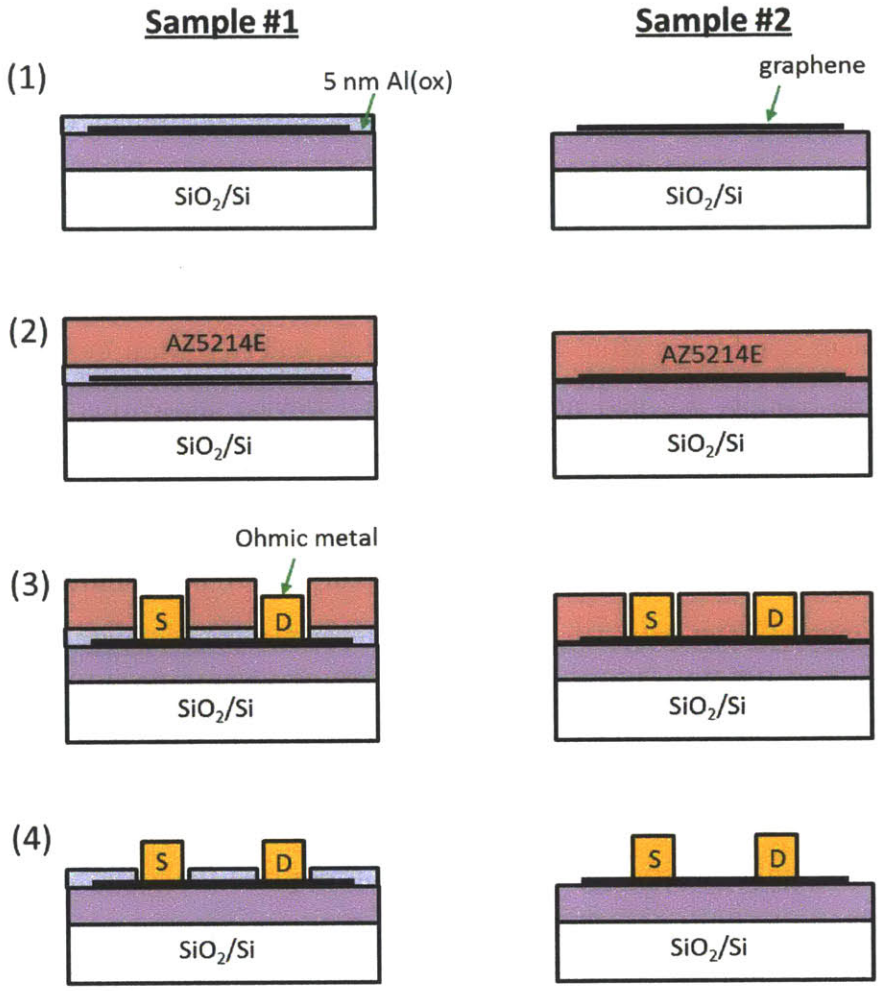

Figure 3-3: Schematic Diagram of Ohmic Process. (1) Starting Graphene Samples - Sample #1 - 5 nm Al e-beam evaporated and oxidized. Sample #2 is as transferred CVD graphene. (2) Photoresist (AZ5214E) deposited, (3) Develop photoresist using AZ422, (4) Evaporate ohmic metal and lift-off.

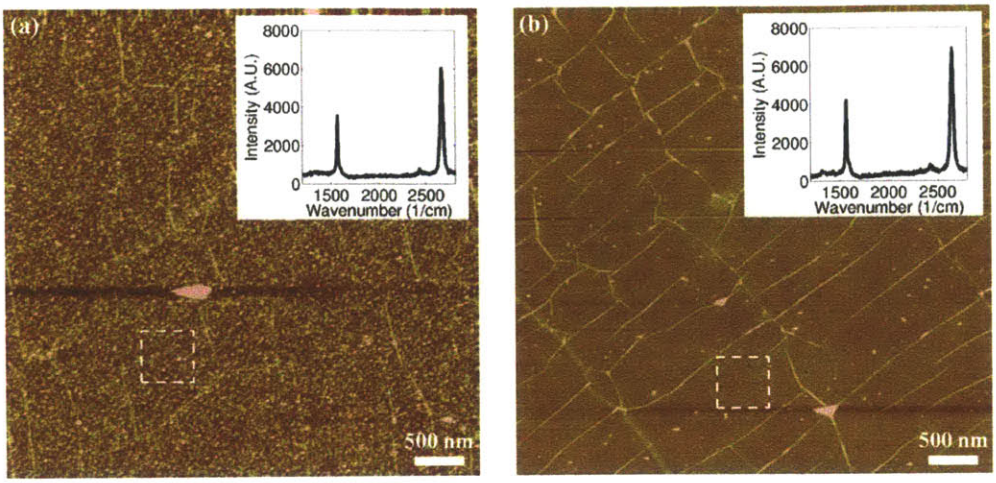

Figure 3-4: AFM of the Graphene Surface After Processing: (a) AFM image (5 μm $\times$ 5 μm) of the graphene surface after standard processing (Sample #2). (R_a,R_q) = (1.26,1.00) nm area shown in the dotted square. As reference, CVD graphene before processing on a SiO_2 surface is (R_a,R_q) = (0.25,0.20) nm. (b) AFM of the graphene surface of Sample #1 is (R_a,R_q) = (0.23,0.20) nm shown in dotted square. Raman data is shown in the inset for (a) and (b).

mer residues are observed using e-beam resists, such as PMMA during the transfer of CVD graphene. In conventional semiconductor processing, oxygen plasma is commonly used to remove these organic residues; however, there is only a weak selectivity between graphene and other organic compounds; furthermore, CVD graphene contains defects and wrinkles due to its growth and transfer, which make it more reactive than mechanically exfoliated graphene. A common procedure for removing organic residues is a forming gas anneal. Unfortunately, forming gas annealing at >200 °C is incompatible with lift-off technology due to photoresist reflow. Therefore, utilizing an Al(ox) buffer layer serves as a low temperature and low damage method of protecting the graphene surface. To ensure that this Al capping process does not damage the graphene, Raman characterization (inset Fig. 3-4(a) and 3-4(b)) shows no difference in the graphene quality between Samples #1 and #2 after Al etching.

Before deposition of any top gate contacts (but after the deposition of the Al_2O_3 gate dielectric), 23 devices from each of the two types of samples were characterized using a doped silicon backgate at room temperature. As shown in Fig. 3-5(a), there

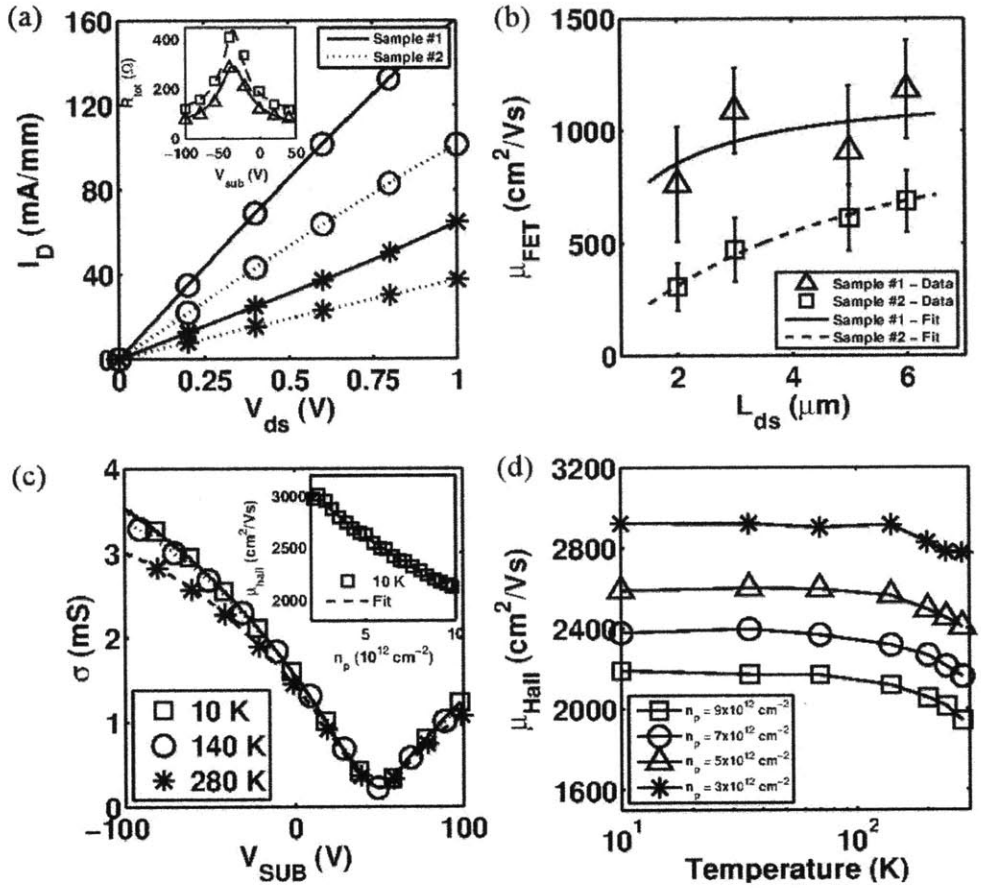

Figure 3-5: Electrical Characterization of Devices (a) I_D vs. V_{DS} for Samples #1 and #2. $L_{DS} = 6\ \mu m$. Dirac point (symbol: *) and $n_p = 6 \times 10^{12}$ cm^{-2} (symbol: ○). The inset shows R_{tot} for the two samples including the fitting from equation 3.9. (b) μ_{FET} vs. L_{DS} , solid and dotted lines are fits from equation 3.8, (fit parameters, $\mu_{Hall} = 1200 cm^2V^{-1}s^{-1}$, $R_C^{\#2}/R_C^{\#1} = 5.2$). (c) Conductance as a function of back-gate voltage for three values of temperature measured using a van der Pauw (VdP) geometry. The inset shows mobility fitting for data at 10 K. The fit estimates mobility values due to Coulomb impurities (μ_{imp} = 3,500 $cm^2V^{-1}s^{-1}$) and short range scatterers ($\mu_{sr} = 5.434 \times 10^{16}/n_p$) (d) μ_{Hall} vs. temperature for various hole carrier densities in the range of 3 to 9 $\times$ 10^{12} cm^{-2} (I= 0.1 mA, B = 0.3 T) for Sample #1

-	$R_C W$ $(\Omega - \mu m)$	n_{imp} $\times 10^{12}$ cm^{-2}
Sample #1	132-573	1-1.2
Sample #2	1955-2440	0.9-1.0

Table 3.1: Extracted Contact Resistance ($R_C W$) and Charged Impurity concentration (n_{imp}) using Eq. 3.9 for Sample #1 and #2. Fitting parameters for n_{imp} are obtained from Eq. 3.9; $\mu_{Hall} = 1,200$ (cm^{2}V^{-1}s^{-1})

is a clear reduction in total resistance (R_{tot}) and in the drain-source current (I_D) of Sample #1 due to the cleaner interface. Two-probe peak field effect mobilities (μ_{FET}) are shown for both samples in Fig. 3-5(b) when varying drain source separations (L_{DS}) at hole concentrations (n_p) $\approx 3.0 \times 10^{12}$ cm^{-2}. As the source-to-drain distance is reduced, the two-probe μ_{FET} is likewise reduced due to the larger effect of the contact resistance. This effect of the contact resistances on μ_{FET} can be seen in equations 3.8 and 3.9, where the variables are defined as drain/source width (W), the drain/source voltage (V_{DS}), gate voltage (V_G), charge neutrality point (V_{dirac}), gate capacitance (C_{ox}), transconductance (g_m), charged impurity concentration (n_{imp}), and sheet resistance (R_{sh}):

$$\mu_{FET} = \frac{g_m(V_G)}{V_{DS}C_{ox}}\frac{L_{DS}}{W} = \frac{\mu_{Hall}(V_G)}{\left(\frac{2R_C}{R_{sh}(V_G)}\frac{W}{L_{DS}} + 1\right)^2} \tag{3.8}$$

$$R_{tot} = \frac{V_{DS}}{I_D} = 2R_C + \frac{1}{q\mu_{Hall}\sqrt{n_{imp}^2 + C_{ox}/q(V_G - V_{dirac})}}\frac{L}{W} \tag{3.9}$$

The Hall mobility (μ_{Hall}) in both of the samples was measured between 1,800-3,000 cm^{2}V^{-1}s^{-1} depending on the carrier concentration at 300 K (Fig. 3-5(c)- 3-5(d), for Sample #1). The improved contact resistance in Sample #1 allowed a better agreement between μ_{FET} and μ_{Hall} than in Sample #2. The contact resistance is estimated from fitting (R_C, μ_{Hall}, n_{imp}) the experimental R_{tot} (inset of Fig. 3-5(a)) with equation 3.9 [48]. The extracted parameters are listed in table 3.1. Contact resistances are reduced from 2000-2500 $\Omega - \mu$m in Sample #2 to 200-500 $\Omega - \mu$m in Sample #1 due to the cleaner graphene surface before ohmic metallization. The estimated contact resistance values for Sample #2 agree well with Transmission Line

Measurements (TLM); however, inhomogenities in CVD graphene limit the accuracy of this technique.

The effect of the Al(ox) on the carrier mobility of graphene is also studied through van der Pauw measurements in Fig. 3-5 (c) and 3-5 (d) at various temperatures. The weak temperature dependence in the mobility data indicates that charge impurity scattering limits the mobility at T $<$ 100 K [46]. At low temperatures (10K), we assume the mobility is dominated by Coulomb impurities ($\mu_{imp} \approx 20qh^{-1}n_{imp}^{-1}$) and short range scatterers ($\mu_{sr} \approx C/n_p$). Following Matthiessen's rule, we can express $\mu_{Hall}^{-1} = \mu_{imp}^{-1} + \mu_{sr}^{-1}$. By fitting μ_{Hall} (Fig. 3-5(c) inset) as a function of n_p, we can differentiate between Coulomb and short range scatters. Therefore, we estimate $\mu_{imp} = 3500$ ($cm^2V^{-1}s^{-1}$) corresponding to n_{imp} $\approx$1.2-1.4$\times10^{12}$ cm^{-2} [46], which agrees well with the fitted estimates in table 3.1 for Sample #1. Short range scatters due to intrinsic defects or dislocations in the CVD graphene are the cause for the decreased mobility at high n_s, thereby limiting the mobility to the range of 1,000-2,000 ($cm^2V^{-1}s^{-1}$). These carrier mobility values, while not ideal, are still sufficiently high enough for electronic applications.

Impact of Sample Variability on Transmission Line Methods

As an aside, while transmission line measurements (TLM) are the standard for characterizing the contact resistance in thin film devices, we have often found that material inhomogeneity can make this extraction method very prone to errors especially for low contact resistance samples. In typical Transmission Line Measurements (TLM), various channel length (L) devices are measured and their total resistance (R_{tot}) is plotted as a function of L according to (Eq. 3.10):.

$$R_{tot} = \frac{1}{qn_s\mu}\frac{L}{W} + 2R_C. \tag{3.10}$$

Typically n_s and μ are assumed to be constant; therefore, measuring the slope and the y-intercept of the data (R_{tot} vs L) provides both the sheet resistance as well as the contact resistance for this technology. However for standard semiconductors

(Si, GaN, etc) where the variability ($\Delta\mu$,Δn_s) is quite small, this is a valid method; however, when there are large variations in μ and n_s from one sample to another, this type of linear extraction becomes much more problematic. This can be seen by inserting the effect of variability on mobility and carrier concentration in equation 3.10.

$$R_{tot} = \frac{1}{q(n_s \pm \Delta n)(\mu \pm \Delta\mu)} \frac{L}{W} + 2R_C \tag{3.11}$$

$$R_{tot} = R_{sh}(1 + \Delta_{var})\frac{L}{W} + 2R_C \tag{3.12}$$

where $\Delta_{var} = \sqrt{(\frac{\Delta\mu}{\mu})^2 + \frac{\Delta n_s}{n_s})^2}$. Unfortunately in Eq. 3.11 and 3.12, we see that the variability is actually multiplied by L in this problem such that longer devices will actually have a larger error in R_{tot} than that of shorter devices. While typically we use multiple sizes of devices, we analyze in equation 3.13 and 3.14 the simplest case where we only have two devices. So let us then look at the two data points where we have L_{min} and L_{max}:

$$R_{tot}^{min} = R_{sh}(1 + \Delta_{var})\frac{L_{min}}{W} + 2R_C \tag{3.13}$$

$$R_{tot}^{max} = R_{sh}(1 + \Delta_{var})\frac{L_{max}}{W} + 2R_C \tag{3.14}$$

In this simple case, the extracted y-intercept when L=0, results in equation 3.15:

$$R_{c,extracted} = \frac{R_{tot}^{min}L_{max} - R_{tot}^{max}L_{min}}{L_{max} - L_{min}} = 2R_C \pm \frac{L_{min}R_{sh}}{W(1 - L_{min}/L_{max})} \times 2\Delta_{var} \tag{3.15}$$

Therefore the error in the extracted contact resistance actually depends on both the size and the material properties of the device. However, it does point out that in order to use TLM measurements given the material variations found in the various samples used, one should choose a very large W, and a very small L for the TLM pattern. However, Δ_{var} in some regards is also a function of W. As we increase

the width of our devices, we integrate over more wrinkles, ripples, charge variations, defects, grain boundaries, etc., all of which can introduce larger variations in the measurement. Therefore, while explicitly extracting the contact resistance is useful, using the actual measured transconductance g_m is perhaps a more relevant parameter that takes into account any effects of the contact resistance especially in the case of constructing high frequency (>1 GHz) devices. While initially we have focused more on the processing side of the contact resistance problem, in the following section we further investigated the fundamental interactions between graphene and various contact metals (Au, Ni, Pd and Ti) to understand the physics of the interface between graphene and the metal.

3.2 Graphene-Metal Interactions

Since graphene is a two-dimensional (2D) material living in a three-dimensional world, graphene's interaction with various materials and surfaces is of paramount importance for new electronic device technologies. The most common interface to graphene is that of a metal, and in some cases - such as graphene nano-electronics - this interface rather than the intrinsic material properties themselves often limits the overall device performance [118, 119, 122]. Previously, in-situ angle resolved photoemission spectroscopy (ARPES) experimental measurements have revealed that drastic changes in graphene's linear band structure can occur when epitaxial graphene is synthesized directly on a single crystal transition metal substrate (Ni, Ir, Ru) [131–136], while Raman spectroscopy has shown that graphene's work function can be tuned by evaporating various metals (Au, Ni, Co, etc.) [137, 138]. However, there is still much unknown about both the structure and the impact on carrier transport that various metals can have on graphene.

While previous reports have investigated much about the direct synthesis of graphene on various metallic single crystals, for technological reasons, we study electron-beam deposited metals onto graphene due to the added availability of metals to choose from, as well as, the compatibility of electron-beam deposition with ohmic contact process-

ing. Therefore, we focus most of our work on common contact metals to graphene, specifically titanium and palladium. Various metrology techniques were utilized to explore the structural interaction (atomic force microscopy (AFM) and transmission electron microscopy (TEM) as well as chemical interaction (Raman Spectroscopy and X-ray Photo-emission spectroscopy (XPS)). Utilizing, density functional theory (DFT), we find that the titanium appears to result in a unique p-d orbital hybridization between the metal and graphene. Therefore, we also investigated any electronic modification between titanium and graphene through angle-resolved photo-emission spectroscopy (ARPES).

3.2.1 Graphene-Metal Structure

In order to explore the interaction between the metal and graphene, we start with examining the interface quality between the two. Using atomic force microscopy (AFM), we can measure the metal wettability through the surface roughness of the films, while selected area electron diffraction (SAED) can confirm the crystal orientation between graphene and the metal. Chemical vapor deposited (CVD) graphene from a copper foil was synthesized following previously mentioned methods in Chapter 1. Annealing was performed at 350 °C in an H_2/Ar ambient pressure environment to ensure a clean surface after transfer. Ti and Pd were then deposited separately onto the samples through e-beam evaporation at a base pressure of 1×10^{-6} Torr at 1 Å/s to ensure proper control of the film thickness.

Atomic Force Microscopy - Interface Wettability

Shown in Figure 3-6 (a) and (b) are the atomic force microscopy scans taken over a 5 μm x 5 μm scan region. The mean average surface roughness (R_a) of the titanium deposited onto graphene is almost indistinguishable from that of intrinsic graphene ($R_a \sim$ 0.18-0.25 nm), whereas the Pd deposited sample shows a much larger surface roughness ($R_a \sim$ 0.63 nm), indicating a strong clustering and a Volmer-Weber growth mode. The low surface roughness of Ti is maintained for films with a thickness $<$ 10

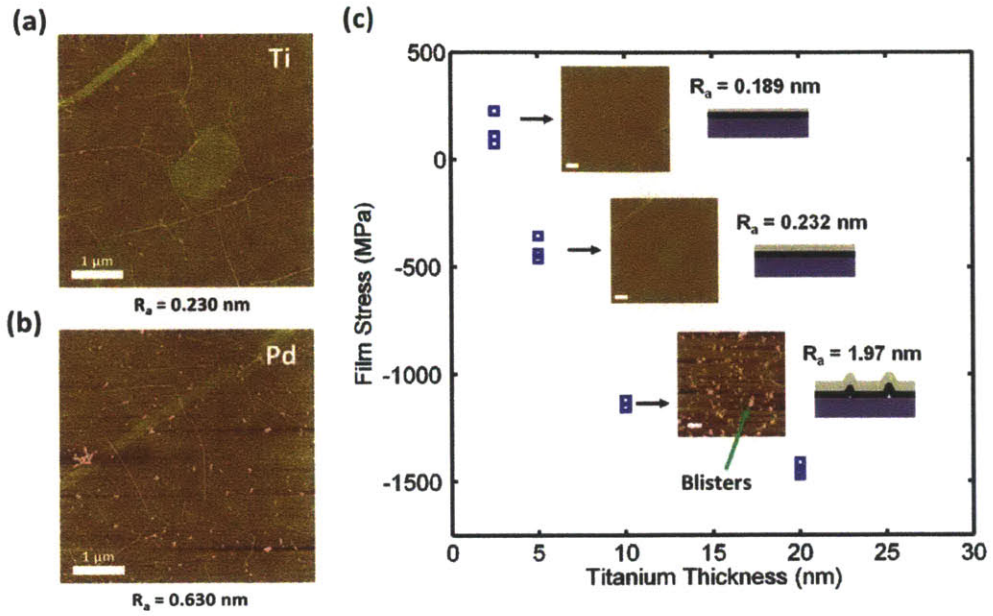

Figure 3-6: Investigating graphene wettability using Atomic Force Microscopy (AFM). Images taken over a 5μm x 5μm scan area: (a) 25 Å of Titanium evaporated on top of Graphene, (b) 2.5 nm of Palladium evaporated on top of Graphene (c) Film Stress (MPa) versus thickness of Titanium. Inset shows AFM of titanium at various thickness of Titanium (2.5, 5.0, and 10.0 nm). Large hillocks or blisters (>30 nm) are observed after 10.0 nm of deposited Titanium.

nm. At films thicker than 10 nm, large hillocks begin to appear (>50 nm), as shown in Figure 3-6(c). The stresses of the titanium film cause a buckling or delamination of the film from the substrate. This delamination is attributed to the weak adhesion energy between the transferred CVD graphene and the SiO_2 substrate [139]. The deposition of thick Pd (< 50 nm), on the other hand, shows an overall much lower intrinsic stress (<500 MPa).

Transmission Microscopy - Orientation Dependence

To further identify the crystal orientation and structure between the metal and the graphene, we utilize selected area electron diffraction (SAED). Using now suspended graphene membranes and identical deposition conditions, we evaporate Ti and Pd onto TEM grids and record the selected area diffraction patterns from both the graphene and the metal. The total sampling area from SAED is approximately 100

nm in diameter. Agreeing well with our AFM data, we find that there is a drastic wettability difference between the two deposited films. Figure 3-7 (a) shows the electron diffraction pattern for graphene (red) and titanium (white). The diffuse diffraction spots correspond to a hexagonal closely packed (hcp) Ti lattice with a lattice constant ratio $a_{Ti}/a_G = 1.19$ (Ideal = 1.199). The titanium lattice shows a distinct epitaxial ordering or alignment to the underlying graphene surface across the entire TEM sample. The palladium diffraction pattern in Figure 3-7(b), on the other hand, shows a much more disordered or random orientation of Pd clusters on the graphene surface. Surprisingly, the deposited orientation of the Pd is the [011] orientation of the face-centered-cubic (fcc) lattice as determined by the ratio of the diffraction rings. The lattice constant ratio between the palladium and graphene is $a_{Pd}/a_G = 1.61$ (Ideal = 1.59). This lattice orientation is slightly unexpected as most simulations predict a [111] orientation between many fcc lattices such as palladium and graphene. [27] This same orientation is also seen for Au and Ni on graphene (Fig 3-8).

In both cases the underlying graphene lattice is still completely observable suggesting that the graphene has not been destroyed or severely damaged by the deposition. Figure 3-7 (c) and (d) are diagrams of the expected orientation of the deposited metal films relative to the graphene crystal lattice. The titanium domains are mainly oriented 30° relative to the graphene with a finite angular dispersion of $\pm < 5°$. While in Figure 3-7 (d), the small crystalline domains of Pd are randomly rotated around their [011] zone axis. These structural morphologies agree well with the AFM morphologies of the two deposited films. The epitaxial orientation of the titanium suggests that the metal atoms wet the surface much more smoothly unlike palladium which appears to be depositing in small clusters (4-5 nm) on the graphene surface. This is further confirmed by plan-view TEM of the samples shown in Figure 3-9.

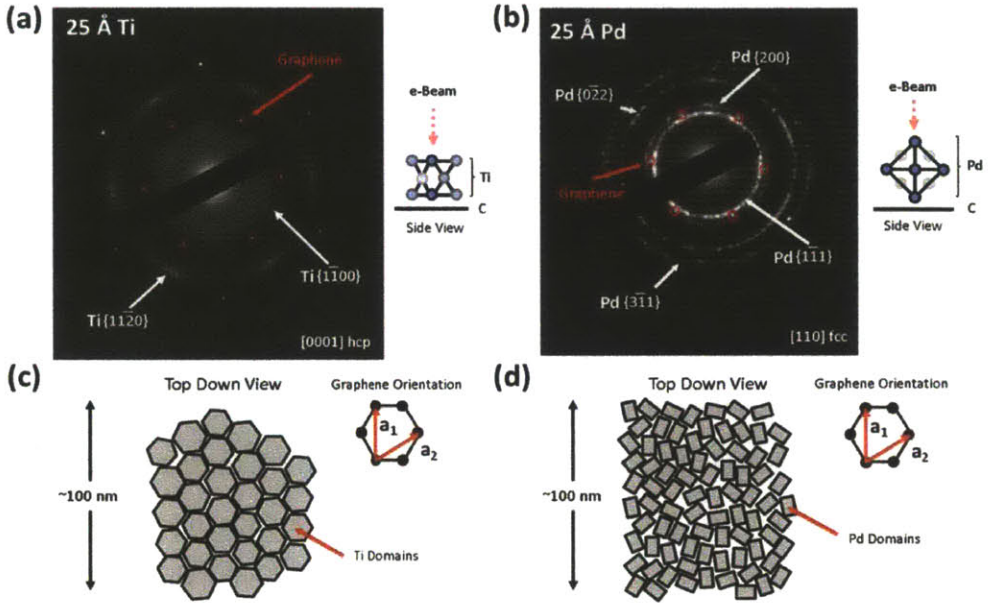

Figure 3-7: Selected Area Diffraction Patterns using Transmission Electron Microscopy (TEM) (a) Graphene/Ti (25 Å) showing a measured lattice constant ratio between $a_{Ti}/a_G = 1.19$. Red circles indicate graphene's first order diffraction spots. The white arrows indicate Titanium's diffraction spots. The zone axis of the electron beam [0001] and crystal orientation (hcp) is labeled in the lower right hand corner. (b) Graphene/Pd (25 Å) showing a measured lattice constant ratio between a_{Pd}/a_G is 1.61. Unlike Titanium where distinct diffraction spots can be identified, the random orientation of the palladium domains results in diffraction rings which are also labeled by white arrows. Diagrams of the electron beam orientation relative to the crystal orientation of the metal are included alongside (a) and (b). (c) Diagram of a schematic of the orientation between Titanium domains (domain shown schematically as a hexagon). A finite angular dispersion is included in the diagram due to the broadening of the diffraction spots in (a). The titanium domains are mainly oriented 30° relative to the graphene with a finite angular dispersion of $\pm < 5°$. In contrast, (d) shows the formation of small nano-domains of randomly distribution Pd rotated around the [011] zone axis (domain shown schematically as a rectangle). Note that the domain sizes ($\approx$ 4-5 nm) are not drawn to scale.

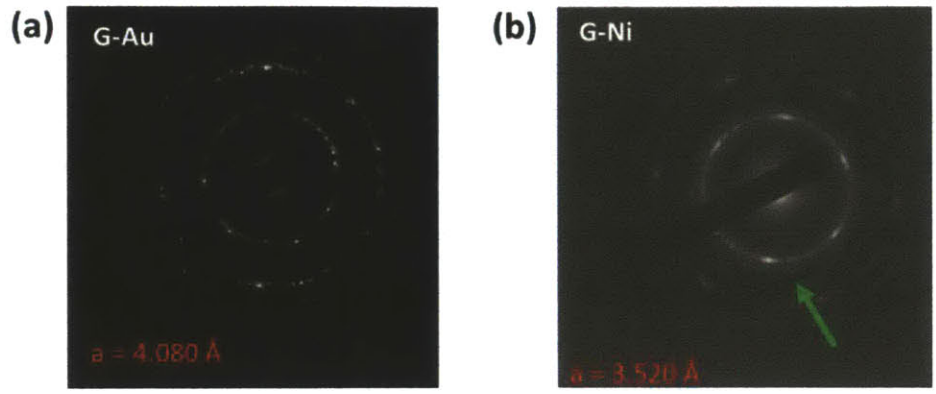

Figure 3-8: TEM data of metals deposited on top of graphene. Selected Area Diffraction Pattern of (a) 25 Å of Au and (b) 25 Å of Ni. The green arrow indicated unidentified diffraction ring. There is an undefined diffraction ring located between the [200] and the [022] rings that we have not yet attributed to any particular [k l m] values.

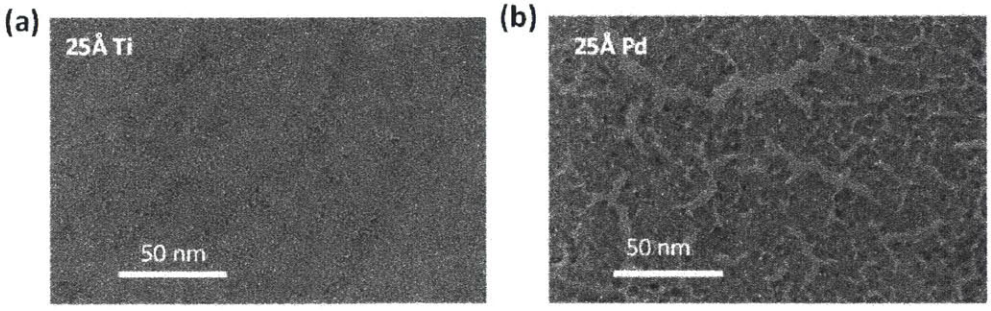

Figure 3-9: TEM taken of suspended graphene samples transferred by direct a transfer method after deposition of (a) 25 Å of Ti and (b) 25 Å of Pd.

3.2.2 Graphene-Metal Chemical Modification

Raman Spectroscopy

Optical techniques, such as Raman spectroscopy, provide a unique opportunity to probe selectively the electronic properties of graphene in contact with a metal [138]. For Raman spectroscopy, we deposit an optically thin layer (25 Å) of different metals (Ti, Pd, Au, or Ni) onto separate CVD graphene samples (1 Å/s), using a shadow mask to create a thickness profile. After deposition, the samples are measured ex-situ in a Raman microscope with a 532 nm laser light source. Figure 3-10 shows the resulting Raman spectra for the various graphene-metal combinations, as well as, the experimental schematic of the measurement Fig. 3-10 (b). The data for most of the metals (Au, Ni, and Pd) agrees well with previous reports in the literature [48, 137, 138]. However, what has not been reported before is the drastic quenching of the D and 2D peaks and the strong down shift of the G peak to $\sim$ 1560-1570 cm^{-1} after titanium deposition. Furthermore, while the 2D peak is completely absent in our sample, other Raman features such as the silicon substrate or G peak of the graphene are still observable, discounting electromagnetic shielding effects by the metal films. Some previous reports have shown an increased D peak due to titanium [140], but our spectra for titanium on graphene shows no experimentally identifiable D peak. The data across various regions, and thus across various film thicknesses, shows a ratio of the 2D peak position/G peak position of $\sim$ 2 (black line Fig. 3-10 (c)). This indicates strained graphene [141]. For the titanium sample, there is no 2D peak to be found, thus the random distribution of points along the y-axis is the result of the noise in the peak value of the background signal. The data along the x-axis shows a clustering of the G peak position around 1570 cm^{-1}, which is much lower than other metals, which might be partially caused by electron doping from the titanium to the graphene.

Assuming this effect originates through the interaction between graphene and metallic titanium, we ran further experiments to rule out artificial effects caused by (1) (hydro)-carbon residues from transfer (2) oxidized titanium and (3) destruction

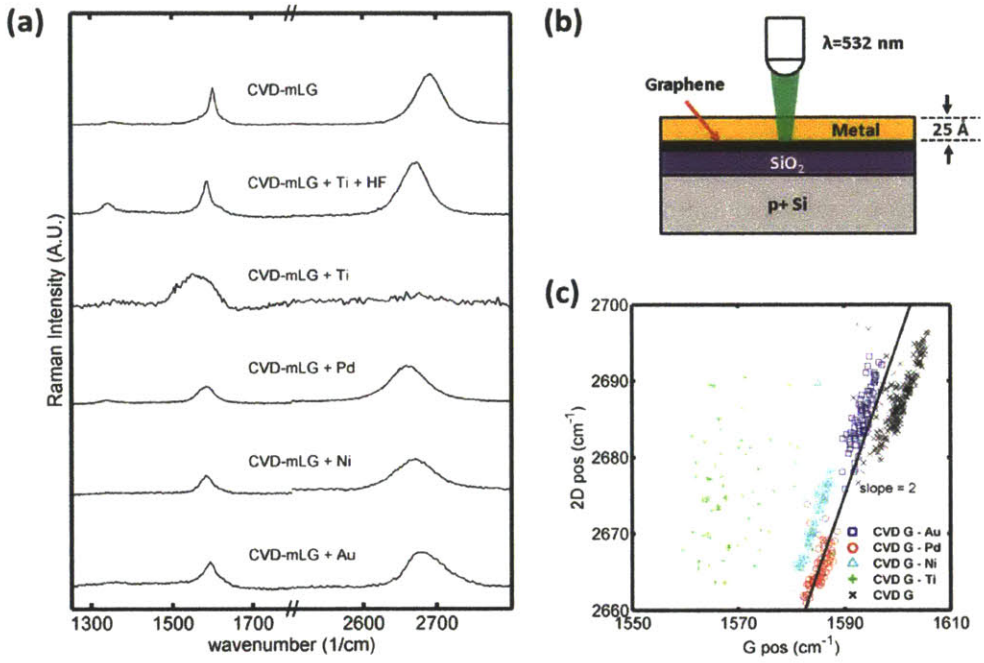

Figure 3-10: Raman Spectroscopy of graphene underneath evaporated metal: (a) Raman spectra of graphene before and after various metals (25 Å of Au, Ni, Ti, or Pd) are evaporated on top. (b) A schematic of the sample during measurement. Raman laser excitation is done at λ= 532 nm, (c) a plot of the fitted 2D peak position versus G position for the various metals deposited. Due to the absent 2D peak in the titanium data, the 2D peak position is simply represented by the peak intensity position found in the background noise of the spectra. The black solid line represents a slope of 2 for the expected strain effect on the 2D peak position versus the G position.

of the intrinsic graphene lattice. To address possible carbon residues after transfer, we repeated our Raman experiment utilizing other transfer techniques, such as mechanical exfoliation of highly oriented pyrolytic graphene (HOPG), as well as, direct synthesis of quasi-free standing monolayer graphene on a SiC surface (sample prepared by intercalating the buffer layer on a 6H-SiC(0001) surface with ultra-pure molecular hydrogen using the same process in the same experimental setup as was previously published by Speck et al. [73]). All samples showed the same drastic quenching of the 2D peak when Titanium was deposited (Fig. 3-11). Figure 3-11 (b) shows AFM of the surface before and after Titanium deposition. [1]

In addition, we also found (Fig. 3-12 (a)) that this effect could be purposely inhibited by introducing carbon residues at the surface (i.e. residues resulting from the exposure and development of a photoresist [10]). After discounting any effects due to carbon contamination, we next turned our attention to any possible titanium-oxygen effects at the interface. Since titanium naturally oxidizes upon exposure to air, we examined the Raman spectra of 5 Å of titanium (fully oxidized) on top of graphene and also found no observed quenching of the 2D peak (Fig. 3-12 (b)). Consequently, this Raman effect is not the product of oxidized titanium at the graphene interface, supporting our assumption that upon ex-situ Raman and oxidation of the titanium film, that the titanium in contact with the graphene is still metallic. Finally, to ensure that the graphene is still intact after deposition, we also measured the Raman spectra after the removal of the titanium by hydrofluoric acid (HF) in Figure 3-10(a). The resulting spectra clearly shows that the G and 2D line shapes can be recovered after HF acid treatment, thus suggesting the Titanium is not covalently bound to the graphene. There is, however, a small D peak present after etching which could be due to damage either through the delamination of the graphene from the underlying SiO_2 or possibly some direct etching of graphene at defects or grain boundaries. In either case, the graphene's lattice has not been completely destroyed by the titanium deposition, indicating that the surface interaction between the two

[1] We traditionally see less blistering of the titanium when deposited onto epitaxial graphene than CVD graphene. We believe this is the result of a stronger substrate adhesion between epitaxial graphene directly synthesized on SiC as opposed to transferred CVD graphene on SiO_2.

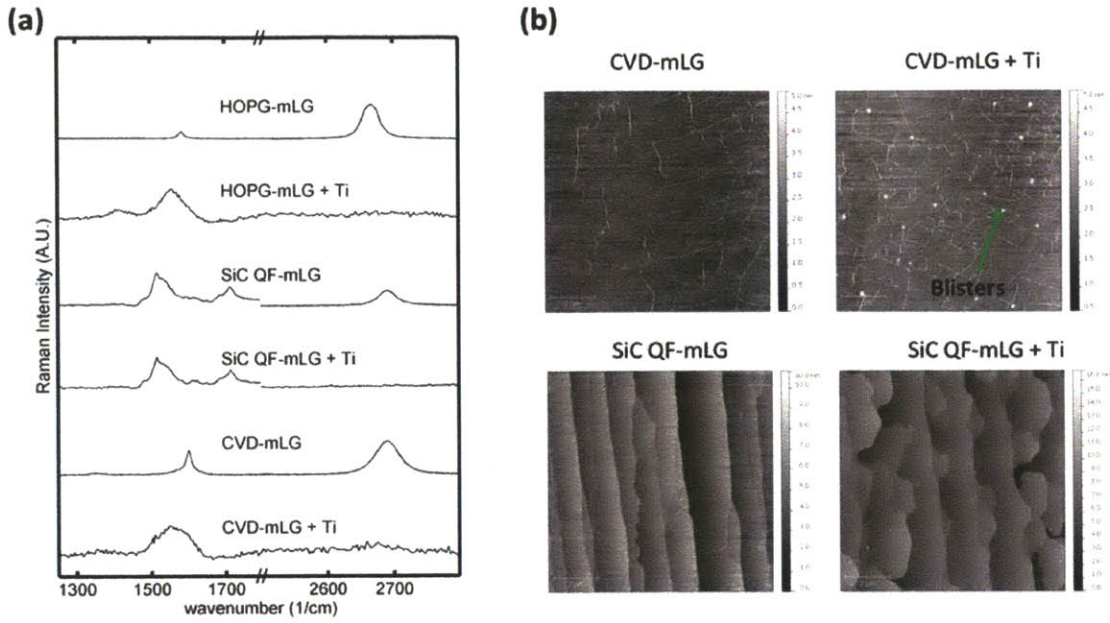

Figure 3-11: Raman Ti effect on various other material sources HOPG, CVD graphene, Epitaxial graphene (a) Raman of 5 nm of Ti evaporated on various graphene sources as labeled, (b) AFM after Ti deposition on CVD graphene and SiC quasi-free standing monolayer graphene (QF-mLG). CVD graphene adhesion affects the puckering of the film due to the strain of CVD graphene, which is not as evident on QF-mLG.

materials interferes with the double resonant Raman process. The explanation for this effect will be described in further detail in Section 3.2.4.

X-ray Photo-emission Spectroscopy

To further investigate the chemical interaction between these metals and graphene, we performed in-situ deposition of titanium or palladium, with parallel acquisition of x-ray photo-emission spectra (XPS) on epitaxial quasi-free standing monolayer graphene (QFMLG) grown on SiC. This graphene substrate was chosen to ensure an in-situ clean graphene surface by avoiding any transfer processes [72]. Contaminations from the ex-situ transfer of the samples to the XPS chamber were removed by annealing the sample at 300°C in a chamber with a base pressure better than 1×10^{-10} torr for 5 minutes. The C1s peak of the pristine sample is plotted in Figure 3-13 (a). The XPS spectrum shows two distinct carbon chemistries: (1) the sp^2 bonded carbon

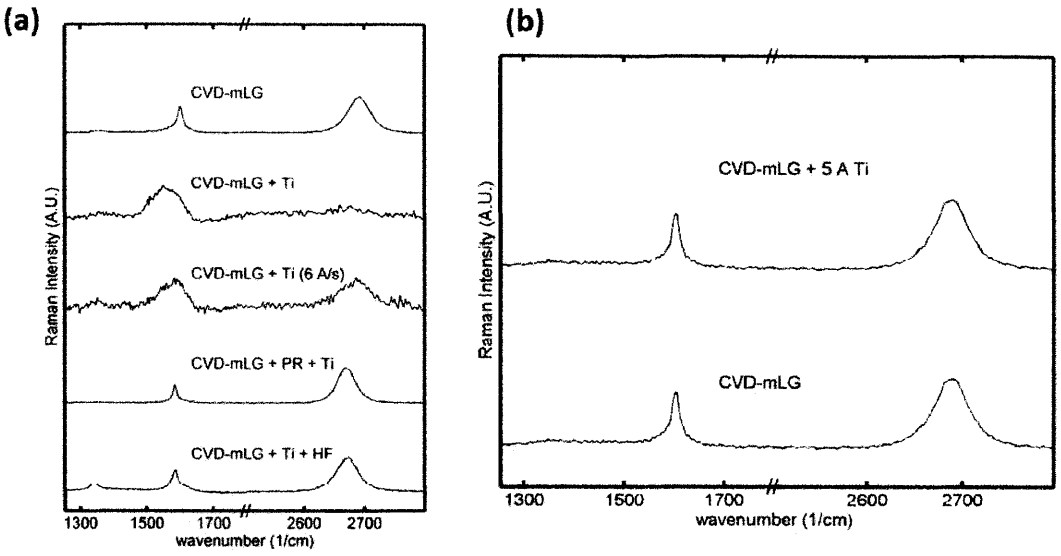

Figure 3-12: Raman spectrum of Titanium (50 Å) deposited on top of graphene for various conditions. Deposition conditions of (6 Å/s) of Ti as compared to Titanium deposited when photoresist (PR) residue is in between the graphene and titanium. (b) Raman spectra comparison of pristine graphene and pristine graphene with an ultra thin layer of titanium (5 Å) after exposure to ambient conditions.

from the graphene (E_B = 284.3 eV, fitted using a Doniach-Sunjic lineshape) and (2) the chemistry of the SiC substrate (E_B = 282.6 eV, fitted using a Voigt lineshape). As reported by Riedl et al. [72] and Speck et al. [73] no interface layer contribution is observed in the C1s core level confirming we have only a monolayer of graphene. After the deposition of two monolayers (ML) of metal (Ti or Pd) (deposition was performed inside an ultrahigh vacuum (UHV) chamber using electron-beam evaporation from a rod at a deposition rate of 0.1 Å/min for Ti and 0.85 Å/min for Pd. The pressure during evaporation was kept below 2×10^{-10} Torr.), we find that titanium causes a chemical modification to the C1s (Fig 3-13 (a)) peak unlike Pd (Fig 3-13 (b)). The graphene peak after Ti deposition (3-13) is now split into two contributions; 54 % of the graphene peak is now shifted to a binding energy (E_B) of 285.2 eV. Furthermore, this new contribution is substantially broadened (FWHM $\sim$ 0.8 eV). Moreover, we observe a very small amount of TiC (E_B = 282.2 eV) during the evaporation. This TiC component increases with evaporated titanium thickness, whereas the modified graphene component is attenuated with the same rate as the graphene and silicon

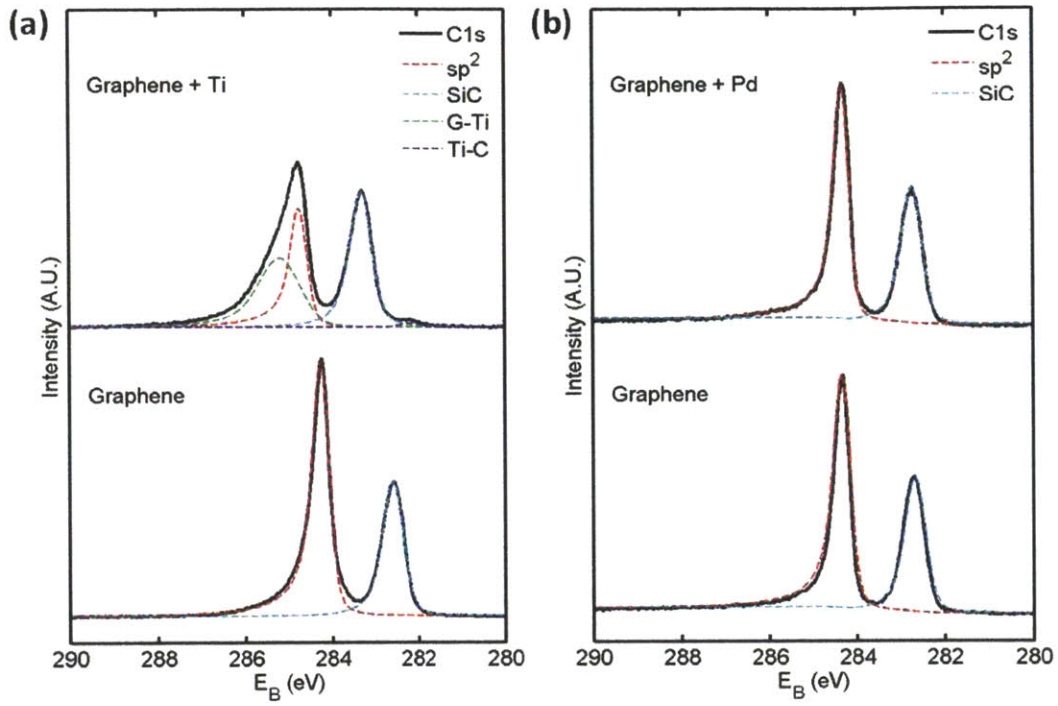

Figure 3-13: In-situ synchrotron X-ray Photoemission Spectroscopy (XPS) spectra for the C1s core level taken at a photon energy of 600 eV: (a) Pristine quasi-freestanding graphene (QF-mLG) on SiC(0001) (bottom), the carbon chemistry is divided into two peaks (1) sp^2 bonded carbon due to graphene (red) and the carbon bonded to Silicon (light blue) from the substrate and in-situ XPS of 2 ML of Ti evaporated on QF-mLG. The carbon bonded in graphene undergoes a chemical modification shown by the arrow which is labeled in green (G-Ti). A small Ti-C peak at ~282 eV also appears in purple, while the intensity of the SiC substrate peak does not change. (b) in-situ XPS spectra of pristine graphene (bottom) and after 1.2 ML of Pd evaporated on QF-mLG (top).

carbide contributions during evaporation. Therefore, in contrast to other reports in literature such as Gong et al. [142], we can attribute the TiC to contamination of titanium from residual gas during and after the evaporation. Furthermore, the oxygen content within the film is also quite low as compared to a completely oxidized Titanium film on graphene (Fig 3-14 (b)). After complete oxidation of the titanium film (600L O_2, 2×10^{-6} torr, at 400°C for 5 minutes) the XPS spectrum of the C1s almost returns to its pristine shape (Fig 3-14 (a)) suggesting a decoupling of the titanium from the graphene, which is consistent with our Raman experiments.

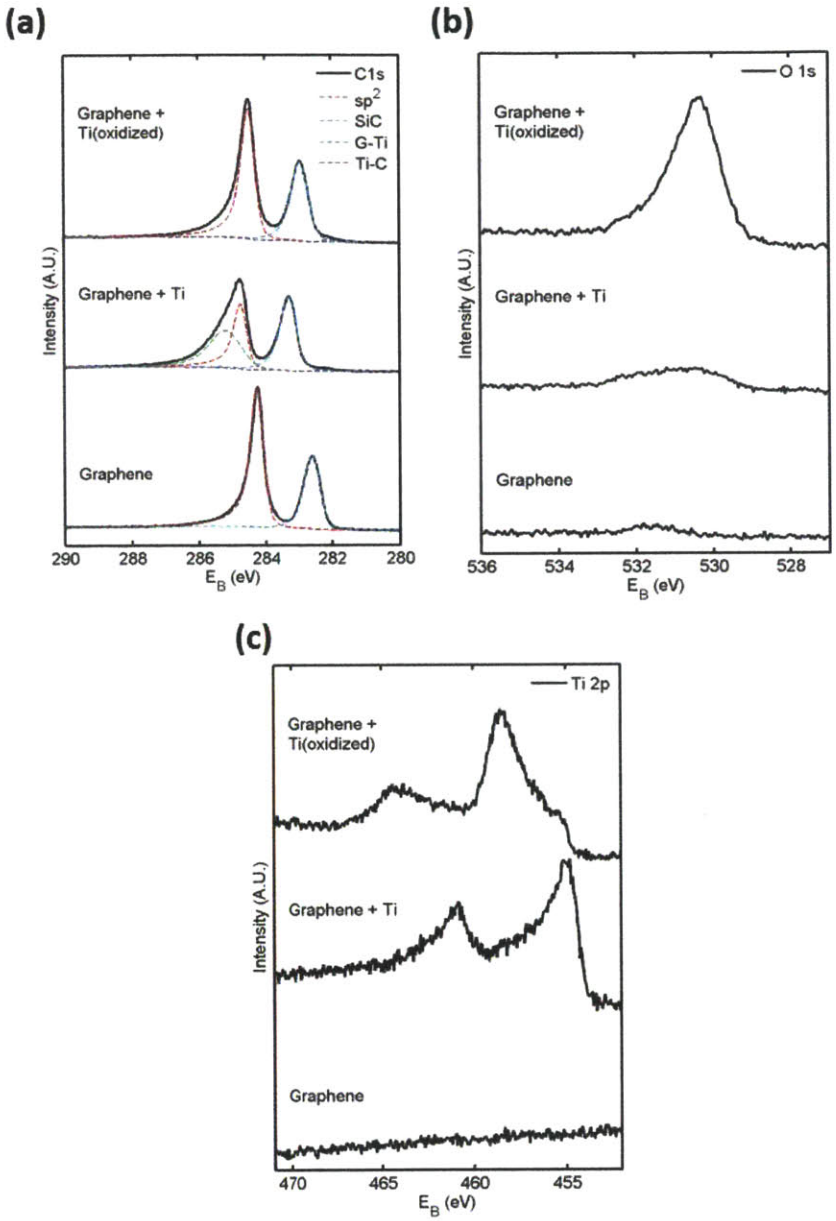

Figure 3-14: In-situ XPS spectra of (a) C1s (b) O1s and (c) Ti 2p energies of titanium on QF-mLG after deposition as well as after oxidation . Oxidation of the titanium was achieved by in-situ exposing the sample to 600L oxygen at a pressure of 2×10^{-6} torr and subsequent annealing at 400°C for 5 minutes. Note the binding energies of the metallic titanium (c) are much lower than that of the oxidized titanium, thus supporting our assumption that the titanium deposited in-situ is in-fact mostly metallic Ti.

3.2.3 Density Functional Theory

We performed density functional theory (DFT) simulations with Perdew-Burke- Ernzerhof (PBE) semi-local exchange and correlation [143] to understand the interaction of titanium and palladium atoms deposited on graphene (simulations conducted by Mitchell Ong and Professor Evan Reed) [143, 144]. TEM images from experiments indicate that titanium crystals deposit in a [0001] orientation on graphene (Fig. 3-7). Based on these results, we construct a supercell arrangement of Ti atoms on graphene, shown in Figure 3-15 (a), that is consistent with the orientation from the TEM experiments. Six metal atom layers are used, corresponding to a ~1.2 nm thick slab of metal on graphene. A similar arrangement of Pd atoms, in Figure 3-15 (b), is also considered, which corresponds to the Pd(111) surface with cubic symmetry ABCABC stacking as opposed to hexagonal symmetry ABABAB stacking for Ti(0001). We calculate the adsorption energies (E_{ads}) for the two structures in Figure 3-15 (a) and (b) by using the expression:

$$E_{ads} = E_{graph+metal} - E_{graph} - E_{metal} \tag{3.16}$$

Here, $E_{graph+metal}$ is the total energy for the graphene-metal complex, E_{graph} is the total energy of graphene and E_{metal} is the total energy of the metal slab. These energies correspond to optimized lattice parameters for each structure which minimize the stress. As shown in Table 3.2, the adsorption energy between Ti(0001) and the graphene lattice is negative, while E_{ads} for Pd(111) on graphene is near zero. These results indicate that titanium binds more favorably to graphene than palladium in this orientation. This result is consistent with the observation that the layers of Ti atoms are much closer to graphene than Pd, as shown in Figure 3-15 and Table 3.2. The observed trends in the adsorption energies and graphene-metal distance (h) are in agreement with trends of previous DFT calculations performed using the local-density approximation (LDA) exchange correlation functional [145, 146].

While the hexagonal symmetry of the Pd(111) surface on hexagonal graphene may be expected to result in the highest adsorption energy, our TEM measurements

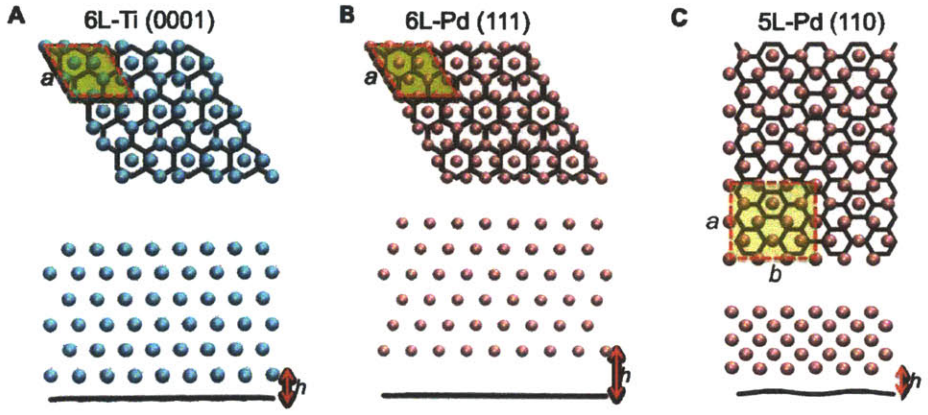

Figure 3-15: Density functional theory simulation of optimized equilibrium geometries. Top-down and side views of (a) 6-layer Ti(0001) on graphene, (b) 6-layer Pd(111) and (c) 5-layer Pd(110) on graphene. The primitive cell in each figure is highlighted in yellow. The equilibrium separation distance between the metals and graphene is represented by h. The dimensions of the unit cell are represented by a and b. For Ti(0001) and Pd(111), a = b, unlike the rectangular unit cell of Pd(110).

	E_{ads}	h (Å)	% Strain a_{lat} (Graphene)	% Strain a_{lat} (Metal)	% Strain b_{lat} (Graphene)	% Strain b_{lat} (Graphene)
6L-Ti(0001)	-0.258	2.08	2.00	-0.55	-	-
6L-Pd(111)	0.014	4.04	-1.05	1.20	-	-
5L-Pd(110)	-0.003	2.50	-0.24	2.31	0.62	-3.88

Table 3.2: Calculated Adsorption energies (E_{ads}), height above graphene surface (h), and % strain on metal and graphene for 6L-Ti(0001), 6L-Pd(111), and 5L-Pd(110) on graphene (a_{lat}, b_{lat}).

suggest that Pd binds to graphene on the (110) surface. We have constructed a Pd(110) orientation surface shown in Figure 3-15 (c), which consists of five layers. A supercell of Pd[110] on graphene was created by recognizing that a 3x2 supercell created from an orthorhombic unit cell for Pd[110] had very similar lattice matching to a 2x3 supercell created from an orthorhombic unit cell of graphene. This Pd-graphene complex consists of 5 layers, containing 24 carbon atoms and 30 Pd atoms, and was optimized such that no stress acted on the cell. From the adsorption energies calculated in Table 3.2, we can see that the Pd(110) case is 0.02 eV per C atom lower in energy than the (111) case. The lower adsorption energy of Pd(110) is consistent with TEM observations, which also observe a preference for the deposition of Pd(110) rather than Pd(111).

These adsorption energies also contain information about the wetting properties of Ti and Pd on graphene. Since the adsorption energy of Ti on graphene is negative for the (0001) configuration, it is energetically favorable for Ti atoms to completely wet the surface of graphene in a uniform fashion, consistent with experimental results [147]. For Pd, the adsorption energies in both orientations are near zero suggesting a very weak driving force for forming an ordered system. However, the energy resolution of our calculations may not be high enough to confidently predict the nature of Pd on the surface. The side profile of Pd(110) on graphene in Figure 3-15 (c), shows that the graphene sheet exhibits an out of plane curvature. While simulations for computationally tractability assumed a periodic supercell, the level of strain is sufficiently large so that this configuration is unlikely to exist over many unit cells of graphene; this conclusion is perhaps related to our observations from TEM that many small Pd clusters are observed in the diffraction pattern. Larger scale structure search calculations assuming metal clusters could shed light on this possibility in the future. These results may also be influenced by the use of the generalized gradient approximation (GGA)/PBE exchange correlation functional. Van der Waals functional (vdW-DF) studies and RPA-based studies of metal adsorption on graphene have been performed that suggest the GGA/PBE approach underestimates the binding energy of physisorbed metals by up to several tens of meV [148–150]. Therefore, the relative

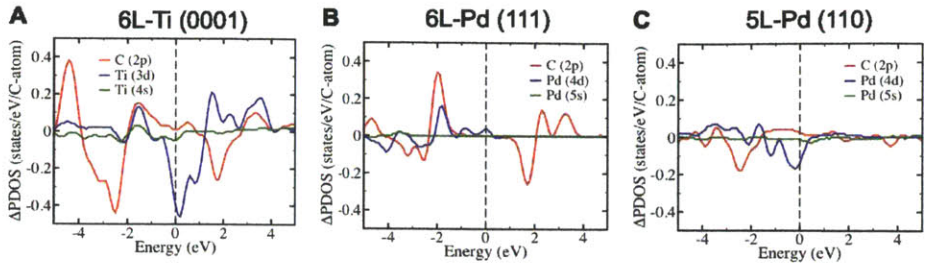

Figure 3-16: Difference between the projected density of states (PDOS) of interacting and isolated configurations indicating the contributions of individual p and d atomic orbitals near the Fermi level for (a) 6-layer Ti(0001), (b) 6-layer Pd(111), and 5-layer Pd(110) on graphene. Atomic orbital contributions from the metal are computed only for the metal layer adjacent to graphene.

energies of the Pd(111) and Pd(110) surface binding may be sensitive to the choice of the exchange and correlation approach used in the calculation. We also performed LDA calcultions and included van der Waals corrections (DFT-D) for dispersion interactions and found that Ti is still predicted to bind more favorably to graphene than Pd(111).

In Figure 3-16, we show the calculated change in the projected density of states (ΔPDOS) with respect to the individual metal and graphene layers for all three structures given in Figure 3-15. Here, we consider only the metal atoms in the first layer and the graphene sheet in the calculation of ΔPDOS. We observe in the chemical bonding a small increase in the p character from the graphene and a large decrease in the d character from the metal near the Fermi energy (between -1 to 1 eV) for 6L-Ti(0001). This suggests that the p orbital of graphene and the d orbital of the metal hybridize, thereby providing evidence that the metal covalently interacts with graphene. This p-d hybridization is believed to be the observed chemical modification as seen in Ti by XPS measurements in Figure 3-13 (a). For the 5L-Pd(110) and the 6L-Pd(111), there is not as large an effect as seen with 6L-Ti(0001). Even inclusion of van der Waals corrections or using LDA for 6L-Pd(111) still show little p-d hybridization. For 6L-Pd(111) the metal and graphene might simply sit too far away for there to be any sizeable hybridization, while the 5L-Pd(110) case suggests some small hybridization assuming a complete sheet. However, the large levels of strain

should reduce the effective contact area with the graphene and likewise should reduce this hybridization effect on the macro-scale, consistent with our XPS measurements.

3.2.4 Raman Analysis

Our XPS experiments and the DFT simulations suggest that a strong p-d hybridization occurs between the titanium and graphene interface. Moreover, the intimate and epitaxial nature of the graphene-titanium film appears to be the cause for the drastic changes in the Raman spectra. Due to the Lorentzian nature of graphene's Raman features, the intensity of the 2D peak is also directly proportional to the lifetime of the 2D peak (γ_{2D}), which can be separated into two components: (1) the intrinsic electron phonon lifetime (γ_{e-ph}) and (2) the electron-defect lifetime (γ_{defect}) shown in Eq. 3.17:

$$\gamma_{2D} = \gamma_{e-ph} + \gamma_{defect} \tag{3.17}$$

Traditionally, most Raman papers studying this intensity have investigated how γ_{e-ph} is affected by doping. Recent work, however, from Mauri et al. investigates the theory of the double-resonant Raman spectra in graphene by incorporating additional lifetime broadening effects (γ_{defect}) due to defects including charged impurity, on-site, and hopping defects [97]. At small defect concentrations, the intrinsic electron-phonon matrix element dominates the electronic broadening of the 2D peak, and the intensity of the D peak is linearly dependent on the defect concentration. However for large defect densities ($N_{defect} > 10^{12}$ cm^{-2}) eventually the intensity of the D and 2D peak becomes inversely proportional with respect to defect density, explaining in part the lack of both a clearly defined D and 2D peak in the Raman spectra of amorphous carbon as well as in our sample [95,151,152]. When $\gamma_{defect} > \gamma_{e-ph}$, this implies that the mean free path for an electron or hole is less than the mean free path due to only optical phonon scattering. From XPS measurements, we have shown that the fraction of chemically hybridized carbon is $> 50\%$, which strongly suggests that we are well within the regime of large defect densities. Therefore, we believe that the chemical

modification due to p-d hybridization serves as a "defect-like" perturbation to the graphene lattice, resulting in a new scattering mechanism. However, we point out that this "defect-like" perturbation is not caused by the destruction of the underlying graphene lattice and is a strong function of the interface as seen by the recovery of the Raman intensity of the 2D peak after removal of the Titanium.

3.2.5 Graphene-Metal Electrical Modification

Angle Resolved Photo-emission Spectroscopy

In addition to the unique structural and chemical properties of graphene and titanium, we are explored any modification of graphene's electronic band structure due to the titanium. Therefore, working again with our collaborators, Roland Koch and Professer Thomas Seyller, we also measured the electronic band structure of graphene after titanium deposition, utilizing Angle Resolved Photoemission Spectroscopy (ARPES). Our samples are measured in the identical chamber as utilized for our previous XPS measurements (3.2.2); however, our samples were now cooled down to 150K to prevent thermal broadening of the ARPES data. Before any deposition, ARPES spectra are taken for the pristine sample. Figure 3-17 (a) shows the ARPES data of the pristine sample, where the wave vector component k_x at the x-axis is perpendicular to the Γ-K direction of the surface Brillouin zone (SBZ) and cuts through the Γ-K direction at the K-Point (see red line in Figure 3-17). Neglecting many body effects, this figure shows the linear band structure of graphene around the K-Point of the SBZ with a Fermi-energy (E_f) level of 0.28 eV below the Dirac point corresponding to a Fermi radius of 0.042 1/Å. On this surface we evaporate titanium while continuously monitoring the graphene bands. After deposition of 0.05 ML of titanium in Figure 3-17(b), we begin to find a strong electron doping as well as a distinct lack of electronic states near the Fermi energy level attributed to the formation of a band gap (E_g). In Figure 3-17(c), the top of the graphene valence band is now located 400 meV below the Fermi level.

In Figure 3-18 (a), the energy distribution curves (EDC) taken at the K-Point of

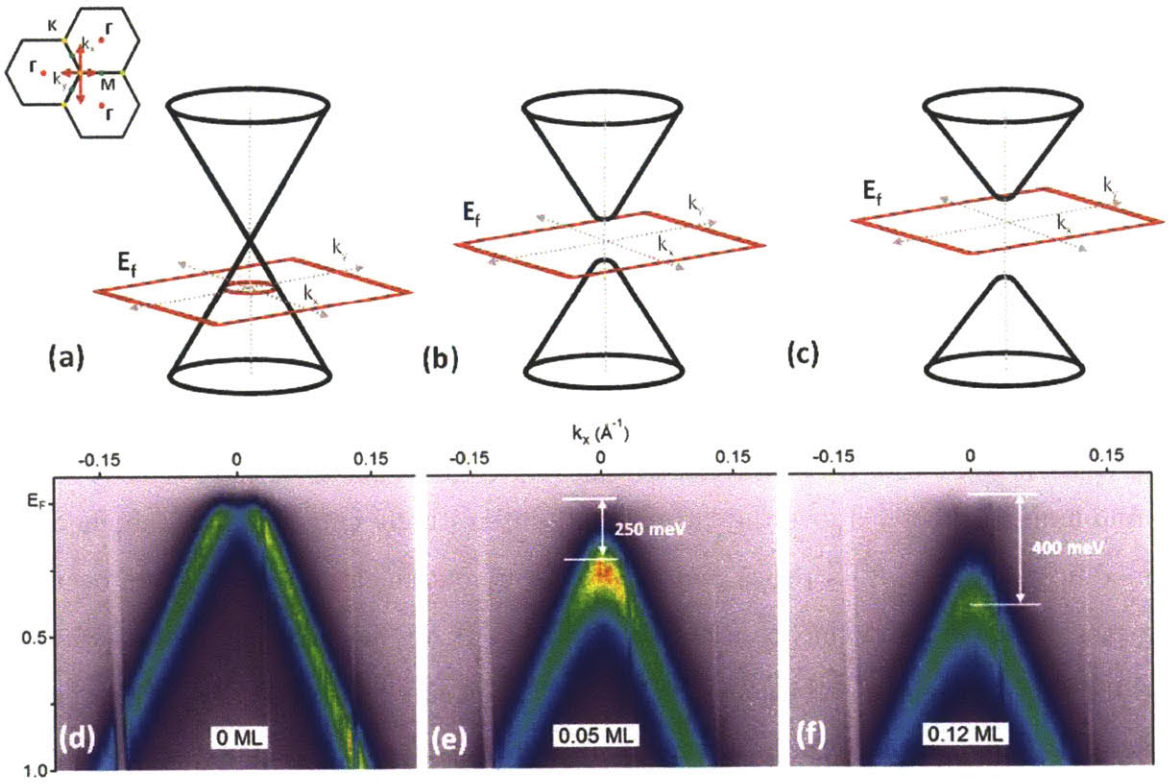

Figure 3-17: Photoelectron intensity maps of graphene during titanium deposition onto quasi-free standing monolayer graphene (QFMLG) at 150 K (d) 0 ML of Ti, (e) 0.05 ML of Ti, (f) 0.12 ML of Ti. The diagrams (a),(b), and (c) are to show the Dirac cone that we are probing during the ARPES measurement as well as the expected modification to graphene's band structure during the deposition. The diagram in the upper left hand corner shows the surface Brillouin zone (SBZ) and the coordinate axis for k_x and k_y

the surface Brillouin zone (SBZ) are shown as a function of the titanium deposition. Before the titanium deposition, the Dirac point is 0.28 eV above the Fermi level (p type $\sim 5 \times 10^{12}$ cm^{-2}). When the evaporation starts, we see the valence band maximum begin to appear below the Fermi energy level. At a titanium film thickness of about 0.25 ML, the effect saturates and the valence band maximum stays at the same binding energy (E_B). Upon further deposition of titanium, up to 1.5 ML, the bands become broader and finally disappear due to elastic/inelastic scattering of photoelectrons by the titanium layer [153]. As verification of our results from before (3.2.2), we also simultaneously monitor the XPS spectra as a function of titanium thickness. Figures 3-18 (b) and (c) show the binding energy of the Ti2p and C1s peaks. The graphene C1s core level shifts from 284.25 eV to 284.76 eV, which indicates an n-type doping of 0.50 eV (Figure 3-18 (a)) (n type $\sim 5 \times 10^{12}$ 1/cm^2). Assuming a symmetric band gap opening, this would give us an undistorted Dirac point position of 0.2 eV below the Fermi level and a band gap of 0.5 eV. This indicates that the conduction band minimum is directly above the Fermi level. Interestingly enough, both the chemical modification of the C1s peaks and the electronic modification of graphene occur at a particular titanium thickness. In Figure 3-18 (d), we fit our C1s spectra assuming three main carbon contributions: (1) SiC (2) Graphene (3) Graphene + Ti during the deposition, to further illustrate this saturation effect on the graphene as a function of titanium thickness. The saturation of all observed effects (ARPES and XPS) at low titanium coverage (0.25 ML) suggests a limited availability of adsorption sites for titanium on the graphene sheet.

While investigations and experiments are still on going to explain this electronic modification to the epitaxial graphene, we did explore through DFT calculations a possible explanation for the modification to the electronic structure. Due to the low Titanium coverage observed in our previous experiments, some educated guesses had to be made with regards to the possible crystal structure of this hybrid system. Therefore, comparing the lattice mismatch between titanium (a=2.95 Å) and graphene (a=2.46 Å), it is very unlikely that titanium is depositing with a commensurate crystal structure over the entire SiC sample. This is confirmed by low

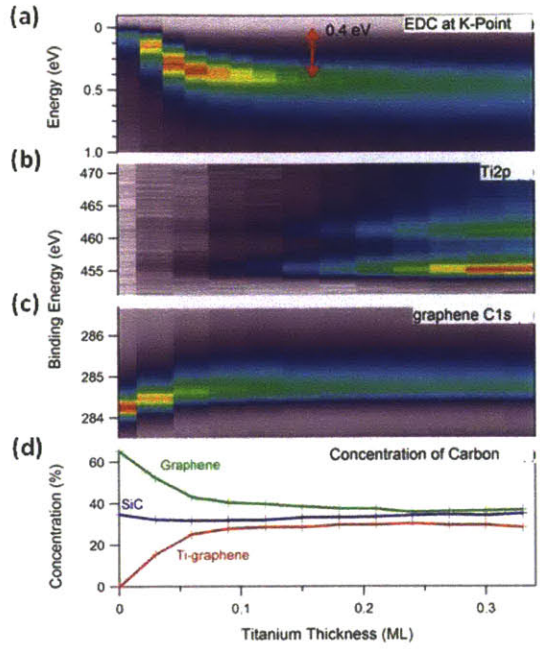

Figure 3-18: ARPES and XPS during Titanium Deposition (a) Energy Distribution Curves taken at the K-point of the BZ (b) XPS of Ti2p peak (c) C1s peak (d) Fitted Carbon Distribution: Graphene, SiC, Ti-graphene

energy electron diffraction (LEED) which does not show a clear diffraction pattern contributed from the titanium. However, from our previous TEM results, we do know that there is a strong epitaxy associated with the titanium to the underlying graphene lattice. Therefore, given the potential epitaxy between graphene and titanium, we investigated various theoretical structures that have been predicted for other alkali metals [154–156] to induce a band gap in graphene. Specifically the symmetry of $(\sqrt{3} \times \sqrt{3})$R30° as well as (3×3) can induce band gaps in graphene. Initial single titanium atom simulations sitting on a graphene surface show a preferential binding energy to the interstitial hollow sites in graphene (E_{bind} = -1.683 eV). Therefore, if we assume a mostly hollow site configuration, the closest relaxed structure would be the $(\sqrt{3} \times \sqrt{3})$R30° structure, which could locally induce a Kekule distortion [157] breaking the sublattice symmetry. Figure 3-19 (a) shows the simulated structure as well as the resulting band structures as computed by DFT. Due to the change in the unit-cell due to the titanium, the K-point of graphene is now mapped to the Γ point

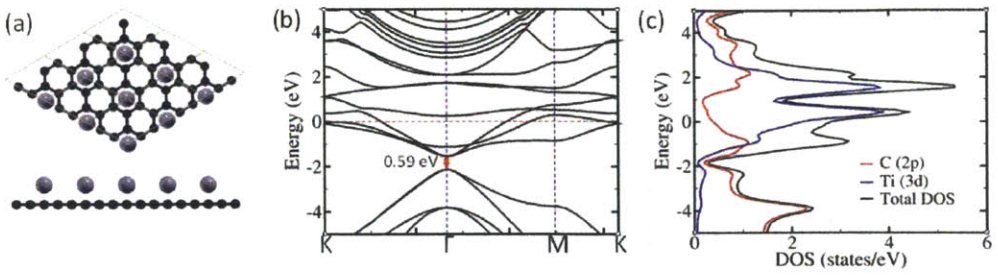

Figure 3-19: DFT Calculations of Ti $(\sqrt{3} \times \sqrt{3})$R30° adatom configuration on top of graphene surface (a) schematic of configuration (b) Energy versus crystal momentum - due to the supercell the Dirac point is now located at the Γ point. (c) Density of States as a function of energy - decomposed into the C(2p) and Ti(3d) orbitals.

(Fig. 3-19 (b)), which shows pretty good agreement between the simulated band gap ($E_g = 0.59$ eV) and our experimentally measured value ($E_g = 0.5$ eV) Furthermore, unlike other previous reports of induced band gap such as hydrogen, while it is agreed that the introduction of hydrogen on top of graphene induces an insulating state, the same cannot be said of the introduction of titanium. Further work through other DFT simulations and experiments are still on going to verify this effect; however, it does pose an interesting question of the possibility of chemically modifying the bandstructure of graphene.

3.3 Gate Dielectrics

To complete our graphene technology, we also require the ability to deposit materials and top gate dielectrics on top of graphene. However, directly depositing a high quality gate dielectric on 2D materials, especially graphene, is much more challenging than silicon. Unlike silicon, which has a native oxide, 2D materials have no bulk to contribute to an oxide layer. Therefore thermally grown or oxidized surfaces are not a viable solution. However as we have shown from our metal evaporation experiments, the low free surface energy and lack of available binding sites limits the types and quality of gate dielectrics available on graphene, as well as other two dimensional materials. For example, a standard technique of creating thin gate dielectrics is

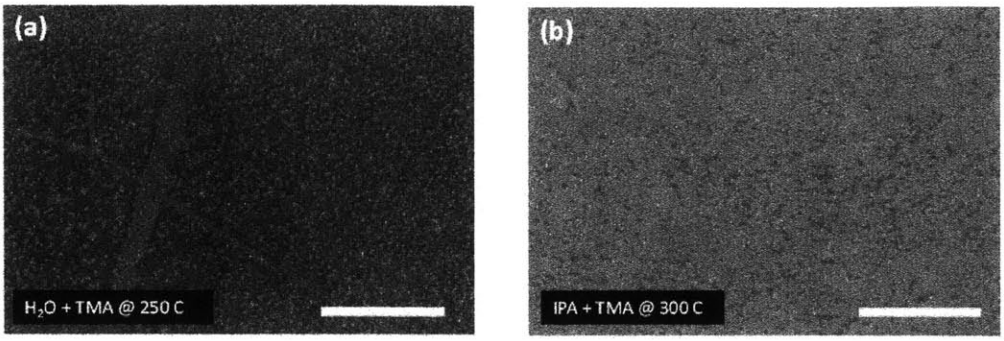

Figure 3-20: ALD of Al_2O_3 on CVD graphene (a) using H_20 as the oxidizer at 250 °C and (b) using isoproponal (IPA) as the oxidizer at 300 °C.

that of atomic layer deposition (ALD). This method utilizes alternating pulses of an oxidizing agent and a metallic-organic precursor to create a thin metal oxide film. Generally the chosen oxidizing agent is that of water. Unfortunately, graphene has a very low free surface energy leading to a hydrophobic surface [158]; water, when absorbed onto the surface of these materials, nucleates like droplets at either defects, wrinkles, or any chemically active region. The resulting deposition thus yields a very non-uniform coverage as shown in Fig. 3-20 (a) when depositing Al_2O_3 on graphene. To address this issue, a variety of seed layers have been implemented: self-assembled organic monolayers, spin coated polymer buffer layers, oxidized thin films, gas phase functionalization, etc. [15,48,159,160]. In our own work, we have examined modifying the free surface energy of the oxidizer by utilizing isopropanol which contains extra hydrocarbons for better surface adhesion to graphene than water. As shown in Figure 3-20 (b), proper control of the surface energy of the oxidizer does play a critical role; however at high temperatures for ALD, the films appear to always nucleate in an island-like growth formation. ALD on other 2D materials such as h-BN and MoS_2 have shown that physical adsorption for these materials dominates nucleation rather than a chemical adsorption, due to the lack of chemically active bonds on the surface [161]. Therefore to avoid these nucleation related issues on graphene, we attempted three alternatives: (1) direct transfer of h-BN, (2) embedded gates, and (3) Al(ox).

3.3.1 Direct Transfer of h-BN

The main effort in this section is to evaluate the use of h-BN films as a dielectric layer for graphene field effect transistors (FET). The h-BN films in this case are synthesized by the deposition of borazine on top of copper substrates [9]. These films were chosen mainly for their improved uniformity and our ability to control the thickness. In order to evaluate the dielectric quality of these h-BN films, we perform similar vertical electrostatic experiments, as shown previously in Chapter 2. We fabricated metal-h-BN-metal capacitor structures to evaluate the dielectric constant (ϵ_r) and breakdown electric field (E_{MAX}) of these materials. The bottom Ti/Pt (2 nm/20 nm) "M1" electrodes (Fig. 3-21 (a) inset) were patterned using standard photolithography and a lift-off process. Large area h-BN films (typically 15-19 nm thick) were then transferred onto pre-patterned substrates following our standard PMMA transfer process. Finally, top electrodes (5 nm Ti/90 nm Au) "M2" were again patterned using photolithography and lift-off. Capacitance was measured from 50-450 kHz using an Agilent 4294A impedance analyzer. The typical device size measured was 150 μm. The extracted average dielectric constant (ϵ_r) was 2$\sim$4 with a breakdown electric field of 1.5-2.5 MV/cm, as shown in Fig. 3-21(b). The lower breakdown field ($\sim$8 MV/cm for single crystalline h-BN [116]) is most likely due to the polycrystalline nature of the h-BN films synthesized on copper, providing a leakage pathway through grain boundaries.

In addition, we fabricated top-gated graphene FETs with transferred h-BN as a top-gate dielectric on top of CVD grown graphene transferred from copper substrates (inset of Fig. 3-21 (c)). To study the impact of h-BN on the transport of graphene, we fabricated van der Pauw structures to measure the Hall mobility before and after transfer of the h-BN. Using a magnetic field of B=0.30 T, I = 1 mA, and an area of graphene of 100 μm x 100 μm, we measured a room temperature Hall hole mobility before integrating the h-BN of 2455 $cm^2V^{-1}s^{-1}$ with $n_s = 3.60 \times 10^{12}$ cm^{-2} and after integrating the h-BN of 2141 $cm^2V^{-1}s^{-1}$, with $n_s = 4.81 \times 10^{12}$ cm^{-2} for the same device. Five other devices also showed similar Hall hole mobility values before and

Parameter	Unit	Back gate (BG) before h-BN integration	Top gate (TG) after h-BN integration
R_C	$\Omega - \mu$m	7338	12130
μ_{Hall}	$cm^2V^{-1}s^{-1}$	1338	1404
n_{imp}	$1/cm^2$	8.08×10^{11}	9.23×10^{11}
n_{Dirac}	$1/cm^2$	3.25×10^{12}	5.90×10^{12}
C_{BG}	nF/cm^2	11.5	-
C_{TG}/C_{BG}	-	-	11.5
W	μm	5	5
L_G	μm	6	3
L_{DS}	μm	6	6

Table 3.3: Fitting parameters for the top and back gated h-BN/graphene devices shown in Fig. 3-21 (d)

after the integration of h-BN. The increase in charge doping is most likely due to the wet transfer process that might trap water at the h-BN/CVD graphene interface. Figure 3-21 (c) shows the measured I_{DS} (drain-to-source current) vs. normalized electrostatically gated carrier concentration ($n_G - n_{Dirac}$) of one of the transistors before and after h-BN integration. The fabrication technology for the graphene transistors is similar to the one used in our metal-h-BN-metal capacitors, except that the bottom electrode in Fig. 3-21 (c) is replaced with graphene. To extract the carrier mobility from the transfer curves, we used a simplified model to fit the device data including the effects of parasitic resistances as done previously in Chapter 2 and Equation 3.9. Here the gate dielectric capacitance for the bottom gate (C_{BG}) can be calculated based on the SiO_2 thickness (11.5 nF/cm^2), and for the top gate, C_{TG} is obtained by comparing by the ratio of the Dirac voltage between the bottom and top gate measurements (115-184 nF/cm^2), which agrees well with our estimated dielectric constant as measured before.

The related extracted device parameters are presented in Table 3.3. Back-gated measurements before h-BN integration and top-gated measurements after h-BN integration are included. The reduced on-state current in the top gated devices is mostly attributed to increased access resistances due to the un-gated graphene regions. This can be easily explained due to the device geometry of our transistor. During back

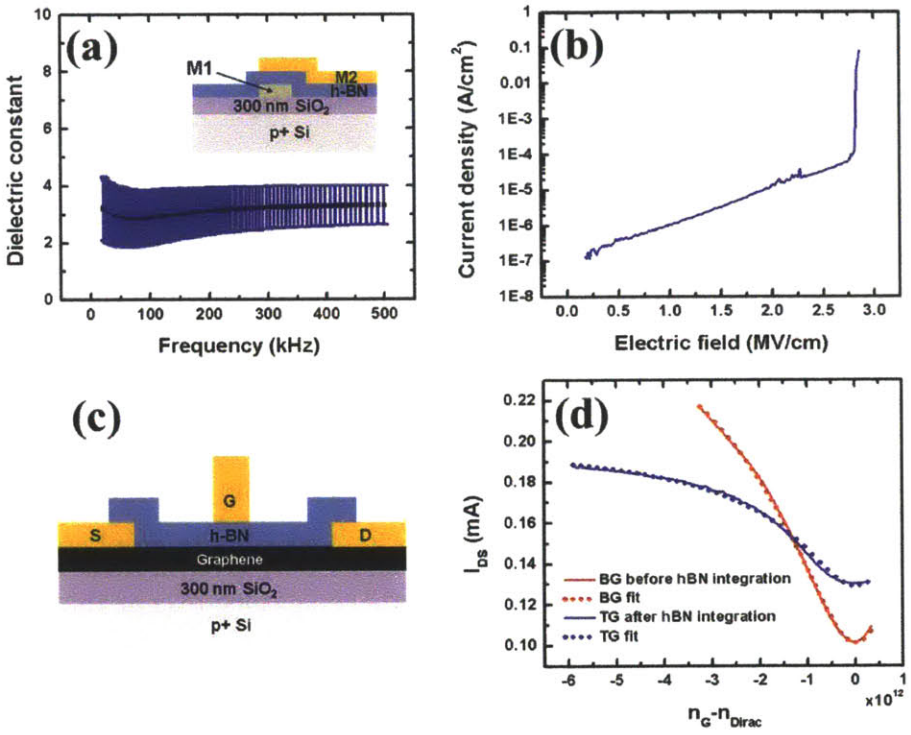

Figure 3-21: h-BN dielectric constant and graphene devices. (a) Average dielectric constant of an h-BN film depending on frequency, (b) Representative breakdown voltage measurement, (c) Schematic diagram of graphene device after h-BN integration. (d) I-V characterization of Bottom-gated (BG) and top-gated (TG) graphene device before and after h-BN integration. The dotted and solid lines indicate the experimental data and fitted data, respectively. V_{DS} for all measurements is 1 volt.

gate measurements, the entire channel is modulated (L = 6 μm , W = 5 μm), while during top gate measurements only a fraction (L = 3 μm) of our channel is modulated. The more pronounced sub-linear dependence of I_D with respect to V_G in the top-gated case is encompassed within the model as a contact resistance term including any parasitic resistances such as access resistances and any additional resistances due to any Schottky or p-n junctions. The field effect transistors also show a slightly increased p-type doping, agreeing well with Hall measurements. The discrepancy between the Hall hole mobility and the field effect hole mobility is due to the sample and transfer variations since different samples were used for Hall measurements and field effect mobility measurements. While, we have explored transferred dielectrics as a possibility, due to transfer related complications, we continued to explore other avenues for top gate dielectric integration.

3.3.2 Embedded Gates

Another alternative for forming a gate contact is to deposit graphene onto pre-patterned gate electrodes/gate oxide [162]. While deposition of materials onto graphene requires careful control of the free surface energy, as well as a limited range of operating temperatures, transferring graphene onto pre-patterned local substrate gates similar to the global back gate of silicon can leverage CVD graphene's easy integration with any arbitrary substrate. This greatly simplifies the device processing while enabling standard lithography and techniques that are CMOS compatible with only a final stage of graphene integration. While we introduce the concept here, this integration issue will be addressed in more detail in Chapter 5 where we show high levels of CMOS/Graphene integration utilizing this strategy, as well as MEMS based devices. This strategy avoids the issues of stress management of deposited films that might otherwise delaminate the underlying graphene. While this is an attractive structure, unfortunately, for RF devices, this process flow requires a high accuracy of alignment between the ohmic metal and graphene to avoid any parasitic overlap capacitance. Therefore, deposition techniques on top of graphene are still necessary for self-aligned structures or processes.

3.3.3 Oxidized Aluminum

Other methods to circumvent issues related with ALD is to utilize physical vapor deposition techniques, such as ebeam-evaporation of metal oxides or PECVD deposition of SiN [163]. However, with many of these methods, the impact on carrier transport and mobility degradation is still assumed to be present, since many of these amorphous materials are not fully passivated at the surface. The impact of these seed layers is generally charge mobility degradation and doping, as discussed in Chapters 1 and 2. In our earlier work in Chapter 2, Figure 2-12 and Figure 3-5, we show the effect of PVD Al deposited on top of graphene, which has shown a decrease in p-type doping; however, accompanied by a small decrease in mobility [48, 164]. This method so far has yielded, in terms of process reliability and reproducibility, our most consistent gate dielectric. This is seen in our top-gated high frequency devices utilizing Al(ox) as our gate dielectric in Figure 3-22, with 7.5 nm of Al_2O_3 is deposited by e-beam (all films deposited in 2.5 nm increments) [48]. The top gate contact is patterned using photolithography and a gate stack of 120 nm Al/ 10 nm Ni/ 7.5 nm Au is deposited by e-beam deposition. Top-gate DC performance for these transistors are shown in Fig. 3-22 for gate length (L_G) equals 2 μm at 300K. Ohmic contacts for these devices and all devices discussed in this chapter utilize our clean ohmic processing discussed at the beginning of this chapter. The measured DC top-gate capacitance (C_{TG}) is 279 nF/cm^2, which corresponds to a top gate p-type μ_{FET} (V_{DS}=0.85 V) = 1,307 cm^{2}V^{-1}s^{-1}. A maximum transconductance (g_m) of 200 mS/mm at V_{DS} = 2 V is achieved without substrate bias corresponding to μ_{FET} = 717 cm^{2}V^{-1}s^{-1}. To note, these values are close to the actual operating values for the transistor. Unlike standard measurements, for evaluating material quality as in Chapter 2, the large V_{DS} bias is actually close to the bias necessary for measuring high frequency RF devices. This high electric field might be the cause for the lower reported mobility values.

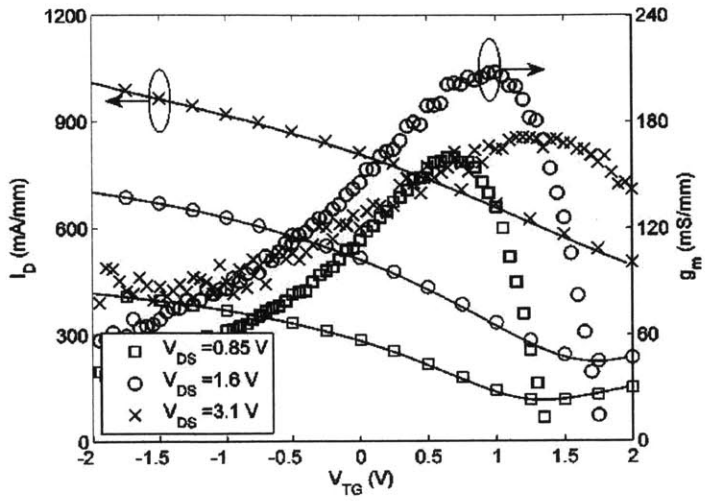

Figure 3-22: I_D vs V_{TG} (Top Gate Voltage) at various V_{DS} (0.85, 1.6, 3.1 V). The right axis shows the DC g_m ($g_{m,max} \sim 205$ mS/mm). Device dimensions are $L_{DS} = 2\mu$m, W = 10 μm [10].

3.4 Radio Frequency Device Technology and Characterization

Given the tremendous interest in the high carrier mobility of graphene, the motivation for our process technology was to develop a robust platform for RF devices. For our graphene based devices, utilizing photolithography, our most robust platform for device fabrication consisted of our Ohmic Device Processing (Al(ox)) in conjunction with Al(ox) gate dielectric and metal gate. This work led to the first demonstration of RF graphene devices constructed from Chemical Vapor Deposition graphene. However, much work has been done on graphene on thermally grown silicon dioxide wafers, which is where most of our own device processing started from. The thermally grown SiO_2 wafers enabled not only optical identification of graphene, but also served as an initial test gate structure due to the conductive silicon backgate for process debugging and optimization. However, utilizing a conductive silicon backgate structure has limitations due to parasitic pad capacitances. The extrinsic RF device performance for our devices on SiO_2 are shown in Fig. 3-23 at 300K. Using Short-Open calibration structures, we de-embed the pad capacitance resulting in an extrinsic f_T

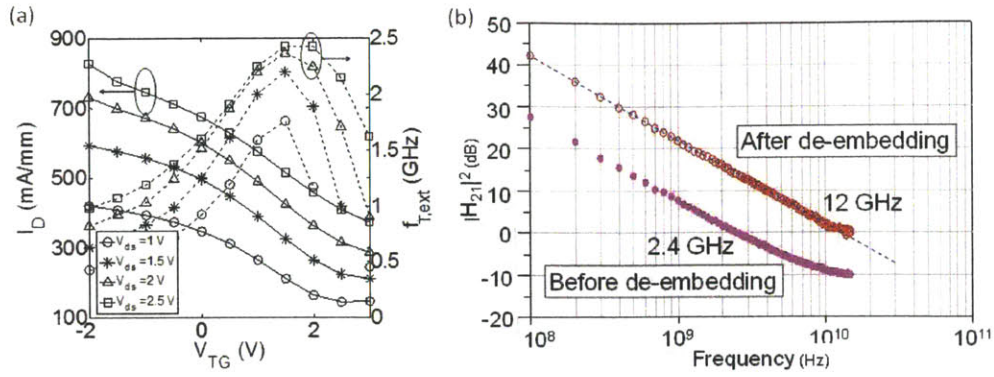

Figure 3-23: RF Measurements on SiO_2 (a) I_D vs V_{TG} at various V_{DS} (1, 1.5, 2, 2.5 V). Measured $f_{T,ext}$ is plotted simultaneously on the right, (b) $|H_{21}|^2$ vs frequency before and after pad de-embedding. The bias conditions are (V_{DS}, V_{TG})= (2,1.5) V. Dimensions are W = 25 μm, $L_{DS} = L_G = 2\mu m$ with a mis-alignment error of 0.5 μm.

of 2.4 and 12 GHz before and after de-embedding [165]. The main reason for the large difference between $f_{T,ext}$ and $f_{T,de-embed}$ is the use of a conductive silicon substrate. The estimated geometric parasitic pad capacitance is 4.56 pF, whereas the geometric capacitance of our gate to channel is only 270 fF. These large parasitic capacitances are currently the main limitation in our extrinsic device performance. However, our $f_{T,de-embed}L_G$ product (24 GHz-μm) is similar to the best devices reported on SiC (using similar de-embedding techniques) [11].

3.4.1 RF GFETs on Sapphire

Therefore, to reduce the coplanar waveguide (CPW) capacitances that limit the directly measurable f_T of the device, we fabricate RF GFETs on a sapphire wafer (500 μm thick), with a resistivity above $10^{16}\ \Omega - cm$. For comparison, the resistivity of conductive Si is less than $1\ \Omega - cm$ and about $10^3\ \Omega - cm$ in high-resistivity Si. This highly resistive substrate can help eliminate most of the capacitances due to the coupling between the CPW metals and the charge carriers in the substrate. CVD graphene films grown by Cu were then transferred to both 300 nm thermally grown SiO_2 and sapphire substrates. The SiO_2 sample is used as a reference sample for device fabrication due to the poor optical contrast of the graphene on sapphire. Ambient

carrier mobilities were in the range of 2234 ± 95 $cm^2V^{-1}s^{-1}$ ($n_s = 6 \pm 0.4 \times 10^{12}$ cm^{-2}) as measured through van der Pauw structures (B = 0.3 T, I = 0.1 mA). As reference, values of graphene transferred on to 300 nm silicon dioxide are typically 2220 ± 174 $cm^2V^{-1}s^{-1}$ ($n_s = 5.5 \pm 0.6 \times 10^{12}$ cm^{-2}). To fabricate graphene transistors, the ohmic contacts of the GFETs are first formed by depositing a 2.5 nm Ti/45 nm Pd/15 nm Au metal stack by e-beam evaporation using a pre-Ohmic aluminium capping process discussed at the beginning of this Chapter. Device isolation is achieved by O_2 plasma etching. The gate dielectric of 13 nm Al_2O_3 is then formed by naturally oxidizing e-beam evaporated Al. The top gate is a 20 nm Ni/200 nm Au/10nm Ni metal stack deposited by e-beam evaporation.

Figure 3-24(a) shows the schematic of the fabricated device, which has a gate length L_G=2 μm, and Figure 3-24(b) shows its transfer characteristic. The minimum conduction point is at 1.8 V. The peak transconductance for holes and electrons is 200 mS/mm and 150 mS/mm, respectively. Fig. 3-24(c) shows the RF characteristics of the same device. For a gate length of L_G=2 μm, the current-gain cut-off frequency, f_T, is 7 GHz before de-embedding the CPW effects and 8 GHz after de-embedding, giving a de-embedding ratio of only 1.14. The de-embedding procedure follows the well-established standard open-short method [11, 12, 166]. The layouts of these open and short structures are strictly identical to that of the active device except in the graphene channel. Figure 3-24(c) also shows the S-parameters before and after de-embedding the CPW effects. It is clear that the de-embedding process only introduces small changes to the S-parameters, which is consistent with the low de-embedding ratio in the f_T and confirms that the CPW capacitance is at a minimum in these devices. Furthermore, we see that the RF performance of these devices already surpasses our previous devices in Figure 3-23.

To increase the device frequency performance, we scale the device gate length to the sub-micrometer range. Figure 3-25 (a) and 3-25 (b) show the scanning electron microscopy (SEM) images of a device with L_G=300 nm and L_{DS}=1.5 μm. Figure 3-25 (c) shows its transfer characteristic, which has a minimum conduction point at 1.3 V. The peak transconductance for holes and electrons is 160 mS/mm and

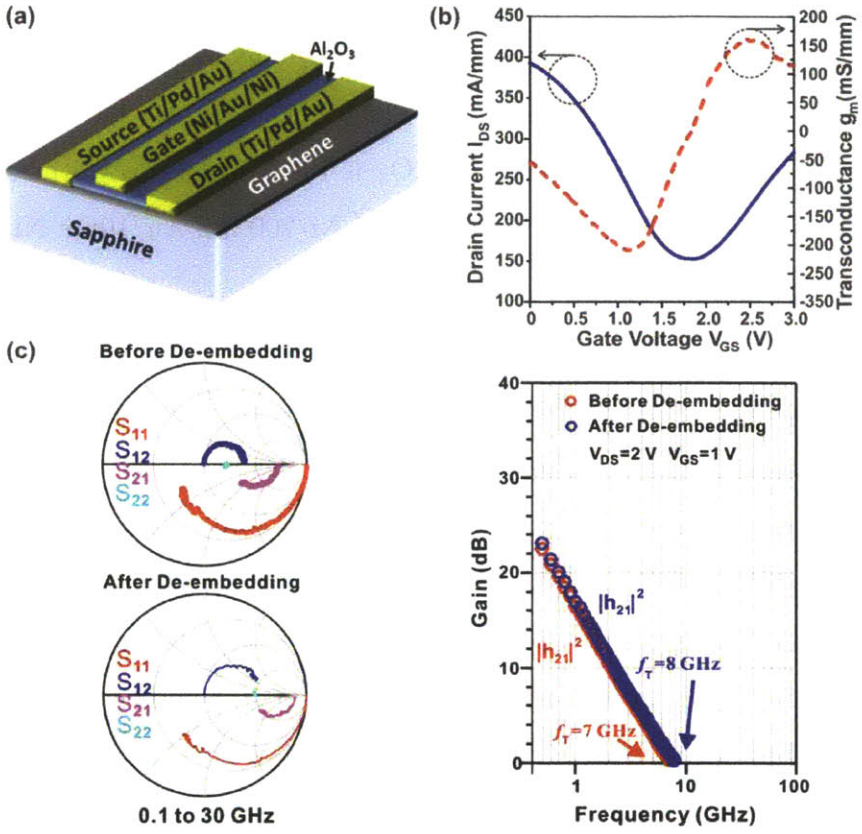

Figure 3-24: RF Device Characterization of Graphene Devices on Sapphire. (a) Structure of the fabricated devices. Ohmic metal: 2.5 nm Ti/45 nm Pd/15 nm Au; Gate dielectric: 13 nm Al_2O_3 (naturally oxidized Al deposited by e-beam evaporation); Gate Metal: 20 nm Ni/200 nm Au/10 nm Ni; Channel Width W=2×25 μm. (b) DC characteristics of a GFET with $L_G = 2\mu$m and $L_{DS} = 2\mu$m for V_{DS}=2 V. The hole conduction mode has a slightly higher transconductance than the electron conduction mode. (c) RF characteristics of the same device. DC bias: V_{DS}= 2 V and V_{GS}=1 V. S-parameters before and after de-embedding CPW capacitances are also shown.

140 mS/mm respectively. Figure 3-25 (d) shows the V_{DS}-V_{GS} characteristic of the device. The V_{DS}-V_{GS} characteristic is measured by driving a constant current density of 250 mA/mm through the device using a current source, and then measuring the drain voltage as a function of the gate voltage. Figure 3-25(d) shows that the device has a signal voltage gain of about 0.2 for low-frequency voltage swings around the minimum conduction point. In this device, the current-gain cut-off frequency, f_T, is 24 GHz before de-embedding and 28 GHz after de-embedding (Figure 3-25(e)). The de-embedding ratio is about 1.2. Comparing the electron and hole branches, the peak current gain cut-off frequency without de-embedding CPW effects is $f_{T,hole}$=24 GHz for hole conduction and $f_{T,electron}$=20 GHz for electron conduction (Figure 3-25(f)).

As a frame of reference for these devices, Figure 3-26 compares the f_T value before and after de-embedding for the state-of-the-art graphene transistors published in the literature [11–16], as well as the 90 nm silicon-on-insulator (SOI) CMOS technology [17]. Firstly, the device with L_G=300 nm fabricated in this work shows the highest before-de-embedding f_T values ever reported. In addition, the devices on sapphire substrate show a very low de-embedding ratio compared to other devices in the literature, mainly due to a highly insulating sapphire substrate that eliminates most of the CPW capacitances. The variations in de-embedding ratios amongst various groups is highly dependent on CPW layout and substrate parameters. The ultimate motivation for targeting the extrinsic f_T, is primarily for circuit applications. While de-embedding performance allows us to understand the channel material, the actual circuit application of these devices requires proper optimization of the extrinsic frequency performance, which we demonstrate in Figure 3-27.

Figure 3-27 (a) illustrates the basic test circuit for our RF graphene devices as a frequency doubler [167]. Under the test conditions, the gate of the GFET is biased at its minimum conduction point. As a sinusoidal signal is superimposed to the DC bias at the gate electrode, it modulates the conductivity in the channel. Due to the inductor in the bias-tee, the current through the device remains stable while the drain voltage swings in response to the change in channel conductivity. Due to the ambipolar behavior of the transistor, the output signal as measured from the drain

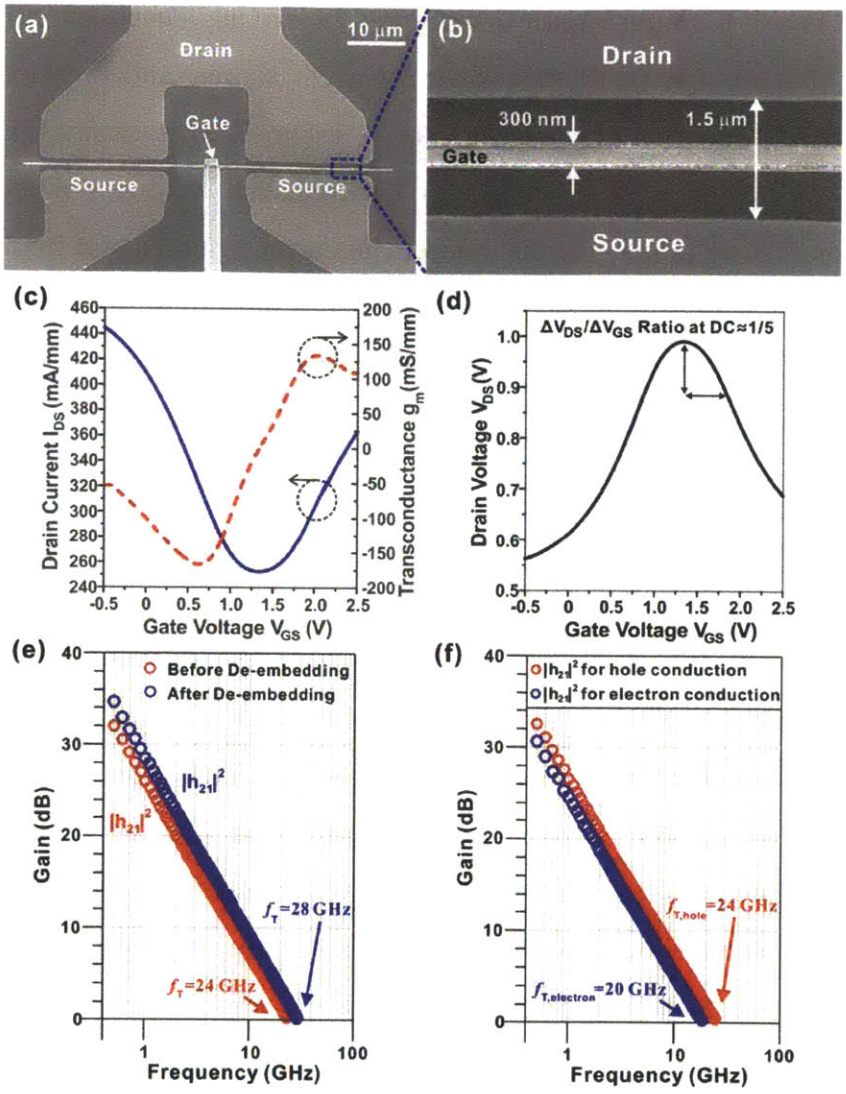

Figure 3-25: RF Device Characterization of Graphene Devices on Sapphire with sub-micron gates (a) and (b) SEM images of a device with L_G=300 nm and L_{DS}=1.5 μm. This device is used for the frequency multiplier demonstration. (c) Transfer characteristics (I_{DS} vs. V_{GS}) of the device. (d) V_{DS}-V_{GS} characteristic of the device measured by keeping I_{DS} at a constant value of 250 mA/mm. (e) Peak current gain cut-off frequency f_T of the device before (f_T=24 GHz) and after (f_T=28 GHz) de-embedding the CPW capacitances. V_{DS}=2 V. V_{GS}=0.5 V. (f) Peak current gain cut-off frequency f_T (before de-embedding the CPW capacitances) for both the electron and hole branches of the device. For the electron branch, $f_{T,electron}$=20 GHz; and for the hole branch, $f_{T,hole}$=24 GHz. The lower of $f_{T,electron}$ and $f_{T,hole}$ limits the frequency doubling performance of the device.

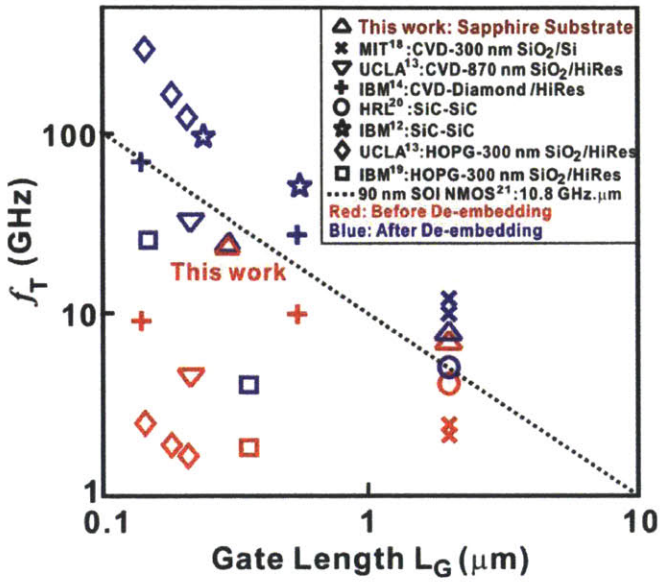

Figure 3-26: Comparison of current gain cut-off frequency f_T before and after de-embedding CPW capacitances for the devices fabricated in this work and other devices reported in the literature [11–17]

and source current is always read in the positive direction, which performs a similar analog function as the absolute value of $V_G(t) - V_{Dirac}$, resulting in a rectified output signal (Figure 3-27 (b)). Figure 3-27 (c) shows the power spectral density, where a larger fraction of RF power is actually present at the output at the doubled frequency (6 GHz) as opposed to the input frequency (3 GHz), showing the improved conversion efficiency of this non-linear operation. Figure 3-27 (d) shows the power conversion efficiency; however, because of the low measured voltage gain of our device, the overall power gain is still negative. This device performance, due to the improved $f_{T,ext}$ of our devices, actually operates up until ~17 GHz, where performance of the circuit is actually limited by the external cabling in the system (Fig. 3-28). However, while many interesting nonlinear operations can leverage graphene's ambipolar transport (binary phase shift keying or modulators), the issue of power gain or signal gain inside of these devices is still a problem. The reason for this is due to the low output resistance of the graphene based devices. Due to the lack of a band gap inside a graphene channel, the graphene transistor operates in the linear or triode

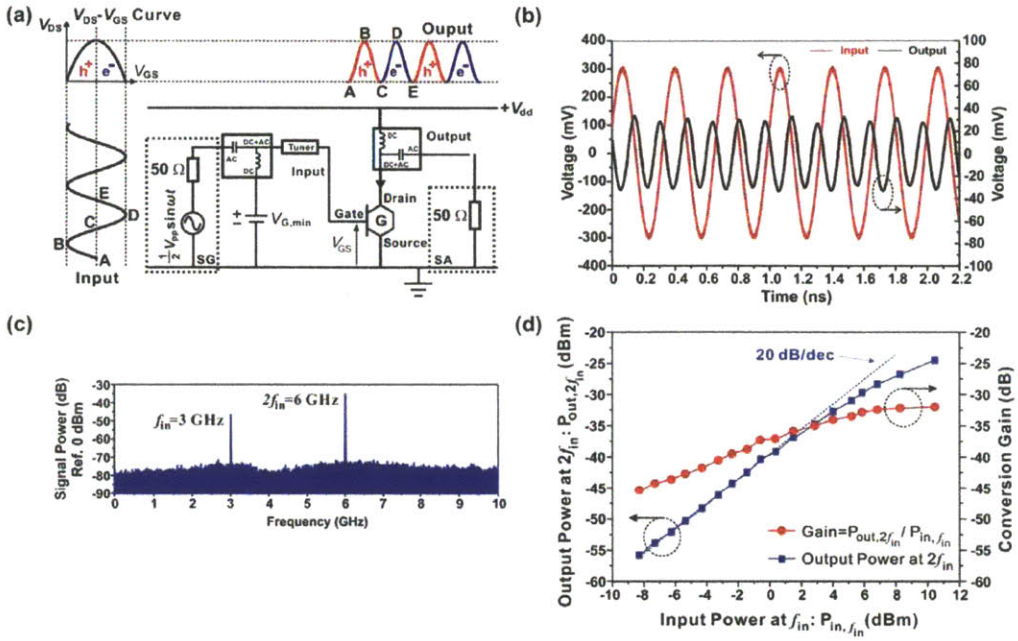

Figure 3-27: Graphene Circuit (a) Principles of ambipolar frequency doubling and schematic of the measurement circuit for the demonstration of graphene frequency multipliers. The inductor in the bias-tee at the drain isolates the DC power supply $+V_S$ from the RF power at the drain by keeping the supply current relatively constant. The capacitor in the bias-tee blocks the DC voltage component at the drain and only allows RF power to be transmitted to the measurement equipment, which is either an oscilloscope or a spectrum analyzer. (b) Experimental demonstration of frequency doubling measured by an Agilent DSA90604A oscilloscope. The input is at 3 GHz. The output fundamental frequency is 6 GHz. DC bias: V_{DS}=2 V. The gate is biased at V_{GS}=1.25 V, slightly below the minimum conduction point (1.3 V), to compensate for the small asymmetry in the transfer characteristics and, hence, to improve the symmetry between the electron and hole conduction at the output. (c) Power spectrum of the output signal from the graphene frequency multipliers measured by an Agilent N9010A spectrum analyzer. The input is at 3 GHz. Frequency doubling is clearly visible. The signal power at frequency component $f_{out} = 2f_{in}$=6 GHz is about 10 dB higher than the signal power at frequency component $f_{out} = f_{in}$=3 GHz without any filtering. (d) Output power at the doubled frequency component $f_{out} = 2f_{in}$ is plotted against the input power that has a frequency of f_{in}. The output power at $2f_{in}$ increases with the input power with a slope of 2 when plotted on a logarithmic scale. Conversion Gain=$P_{out,2f_{in}}/P_{in,f_{in}}$ increases with input power up to 2 dBm.

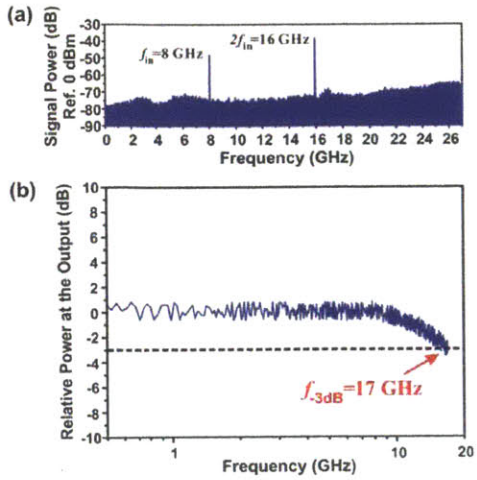

Figure 3-28: Frequency Performance of Graphene-based Multiplier(a) Power spectrum of the output signal from the graphene frequency multiplier when an 8 GHz input signal is applied to the gate of the device. The signal power at $f_{out} = 2f_{in}$=16 GHz is about 11 dB higher than the signal power at $f_{out} = f_{in}$=8 GHz without filtering. More than 93% of the total RF power in the output signal is at 16 GHz. (b) Frequency dependence of gain. The -3dB cut-off point is at 17 GHz. Bandwidth is not limited by the carrier transit time, but mainly by the RC constant of the device and the measurement setup.

regime. This unfortunately, leads to a very small output resistance ($\mathrm{d}V_{DS}/\mathrm{d}I_{DS}$) since the transistor still operates as a resistor as opposed to a current source, when the transistor saturates. This small output resistance thus shunts the internal current gain and reducing the measured signal. Therefore, the demonstration of current saturation in graphene based transistors is still an area of ongoing work [168–170]; however, as we have shown earlier, perhaps inducing an electronic band gap by chemical modification such as titanium might be a future route for improving the power gain from these devices.

3.5 Summary

Therefore, in this chapter we have investigated many of the process-related and fundamental issues for graphene based RF devices. We developed improved processing techniques for making ohmic contact to graphene based devices, which enabled us to

demonstrate high-speed transistors for RF applications. However, we have also investigated the fundamental interactions between graphene and various metals specifically titanium. Unlike contacting a standard 2D electron gas, the entire channel material is self-contained within the graphene itself. By observing both the structural nature of Ti and Pd on top of graphene, as well as the chemical modification to graphene by these metals, one can gain more insight into optimizing graphene contacts. On one hand, titanium forms an intimate conformal contact to graphene. On the other hand, the titanium-graphene p-d hybridization also appears to interfere with carrier transport as seen from Raman spectroscopy. Conversely, palladium and even other metals (i.e. gold and nickel) due to poor wetting, form a far worse interface to graphene, but the graphene properties underneath the metal appear intact. While many external factors play a role in ohmic contacts to graphene, including the fabrication process, stresses, and delamination, the microscopic interface between these metals and graphene appears to be far from ideal, shedding new light towards improving ohmic technology for carbon electronics. Leveraging this chemical modification to titanium, we also investigated the electronic modification to graphene's bandstructure due to titanium, which suggests the formation of a small band-gap. These findings may have a lot of significance for our RF devices; as we have mentioned, the lack of a band-gap in graphene also prevents graphene devices from demonstrating current saturation, which limits the voltage gain of these devices. Potentially, chemical modification by titanium at the drain side of the transistor may enable high voltage gain transistors. Finally, while the graphene technology was developed for RF transistors, this knowledge and understanding will be recycled in the following chapters, when we discuss optical devices made of graphene for thermal sensing applications.

Chapter 4

Infrared Graphene Detection Mechanisms

While in the previous chapters, we have been focusing on the device processing technology and its implications on the electronic properties of graphene, in the next half of this thesis, we would like to discuss graphene's optical properties specifically focusing on the electromagnetic spectrum in the mid-infrared (5-15 μm = 0.248 - 0.0826 eV), a range of energies below the detection capabilities of the human eye. This relatively low energy range corresponds with many low energy vibrational modes found in molecules and covalent bonds, which makes this range especially attractive for chemical detection applications. Furthermore, this range overlaps with the emitted blackbody radiation of objects at 300K, which makes it an interesting range for thermography or active night vision systems. While emission and detection technologies in the visible (390-700 nm or 3.17-1.77 eV) and near-infrared (1.55 μm = 0.8 eV) are commercially mature technologies for imaging and communications, detector technologies in the mid-infrared still span a wide gamut of physical detection mechanisms, such that no one technology, as of yet, is able to provide the trifecta of an ideal detector: (1) high speed, (2) high sensitivity, and (3) low cost. Therefore, due to the already large optical absorption demonstrated within graphene as discussed in Chapter 1, for this thesis, we explore the potential applications of graphene as another option as a thermal imaging technology. However, before discussing potential applications

of graphene's for infrared detection, we first review some background and theory of blackbody radiation and infrared detectors.

4.1 Theory - Blackbody Emission

While there are many interesting spectroscopic applications in the infrared, our main interest for this thesis is specifically in active thermal imaging applications of roughly room temperature blackbodies. Following standard blackbody theory, we can express Planck's blackbody radiation law for the spectral radiant emittance (W_λ) in equation 4.1 [171]:

$$W_\lambda(\lambda, T) = \frac{\partial}{\partial\lambda}\frac{\partial^2 U}{\partial A \partial t} = \frac{2\pi hc^2}{\lambda^5}\frac{1}{e^{\frac{hc}{\lambda k_B T}} - 1} \tag{4.1}$$

where, U is the radiant energy, A is the surface area, t is time, λ is the wavelength of light, c is the speed of light and k_B is Boltzmann's constant, and T is the temperature. This distribution of energy for a given temperature of a blackbody is plotted in Figure 4-1, which near room temperature is mainly centered around 10 μm.

If we integrate the spectral radiant emittance over λ, we arrive at the total emitted power ($W_0(T)$), which results in the Stefan-Boltzmann law assuming an emissivity of one (Eq. 4.2):

$$W_0(T) = \int_0^\infty W_\lambda(\lambda, T)d\lambda = \frac{2\pi^5 k_B^4}{15h^3c^2}T^4 = \sigma T^4 \tag{4.2}$$

where σ is the Stefan-Boltzmann constant. Therefore, infrared detectors designed for active thermal imaging must span a relatively wide range of photon energies ~4-20 μm as shown in Fig. 4-1.

4.2 Comparison of Infrared Detectors

Unlike the visible range, where we traditionally think of visible detectors operating as solely photon detectors, many variety of detection schemes are possible in the

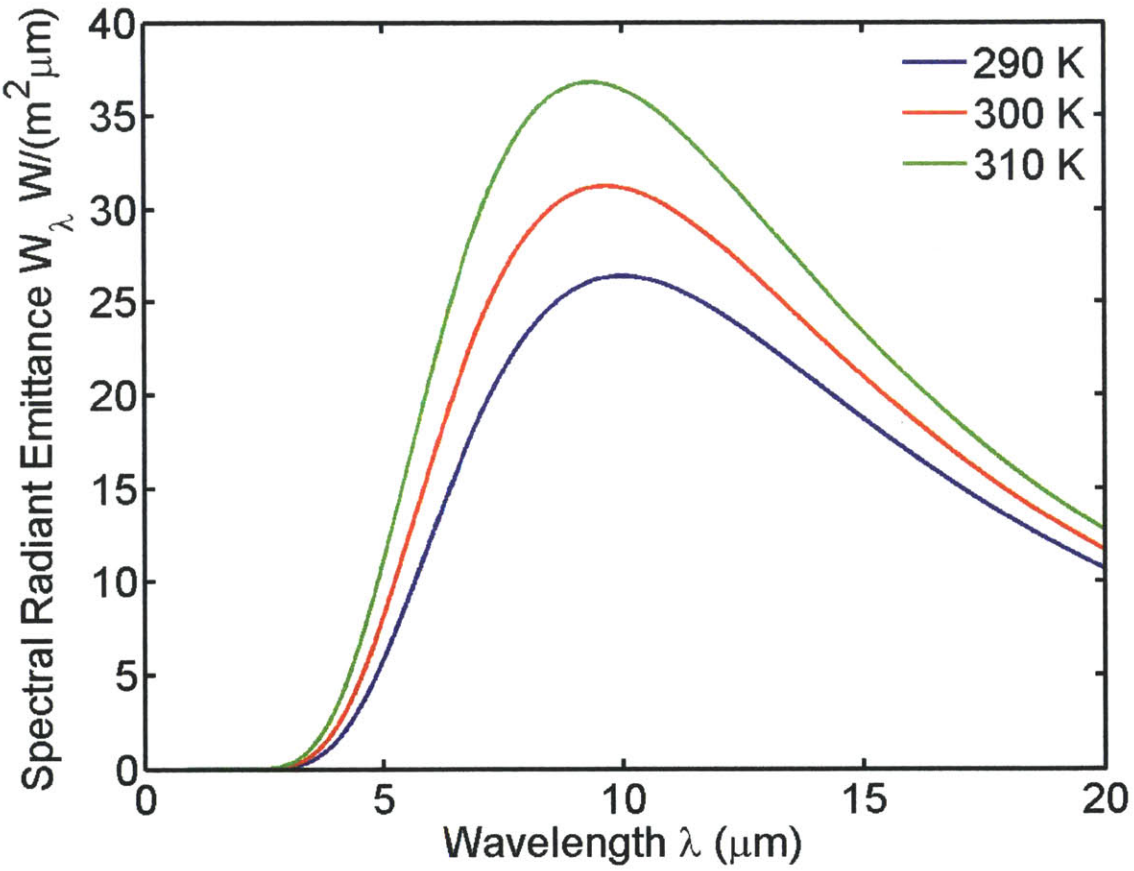

Figure 4-1: Spectral Radiant Emittance for Room Temperature blackbodies at 290 K, 300 K, and 310 K.

infrared. At longer wavelengths, this range is traditionally associated with radiative heat transfer as well as optical photons. This strange mix between thermal engineering and optical engineering leads to a wide variety of infrared detectors.

4.2.1 Figure of Merit - D*

Before discussing the actual detection mechanisms, it is useful to define a figure of merit for infrared detectors: Detectivity (D*). This figure of merit is useful for not only understanding the fundamental limitations of these detectors, but also as a point of comparison to discuss the performance of various infrared sensing technologies. Detectivity ($\mathrm{cmHz^{1/2}/W}$) can often be thought of as the equivalent of a normalized version of signal to noise:

$$D*(\lambda) = \frac{R(\lambda)}{V_N}\sqrt{a_0 b_0 \Delta f} \tag{4.3}$$

where R is the responsivity (V/W), while V_N is the total voltage noise source present in the detector within the frequency band Δf, and a_0 and b_0 are the lateral dimensions of the detector element. Thus a higher D* implies a higher intrinsic signal to noise ratio for the detector. D* is useful for evaluating the intrinsic sensitivity of a detector material, while being independent of the physical imaging system. Table 4.1 and Figure 4-2 compare a variety of infrared detector technologies in terms of operating temperature and detectivities. Later in chapter 5, we will introduce factors dependent on the imaging system and discuss another type of figure of merit, that of the Noise Equivalent Temperature Difference (NETD). While there are many different detectors to choose from, the various available detectors can often be classified by the method of detection they employ: (1) Thermal or (2) Optical.

4.2.2 Thermal Detectors

Thermal detectors are perhaps the oldest form of infrared detector. While we typically think of light as being composed of photons and directly detecting those photons in the visible, the infrared spectrum is traditionally associated with heat. As we have

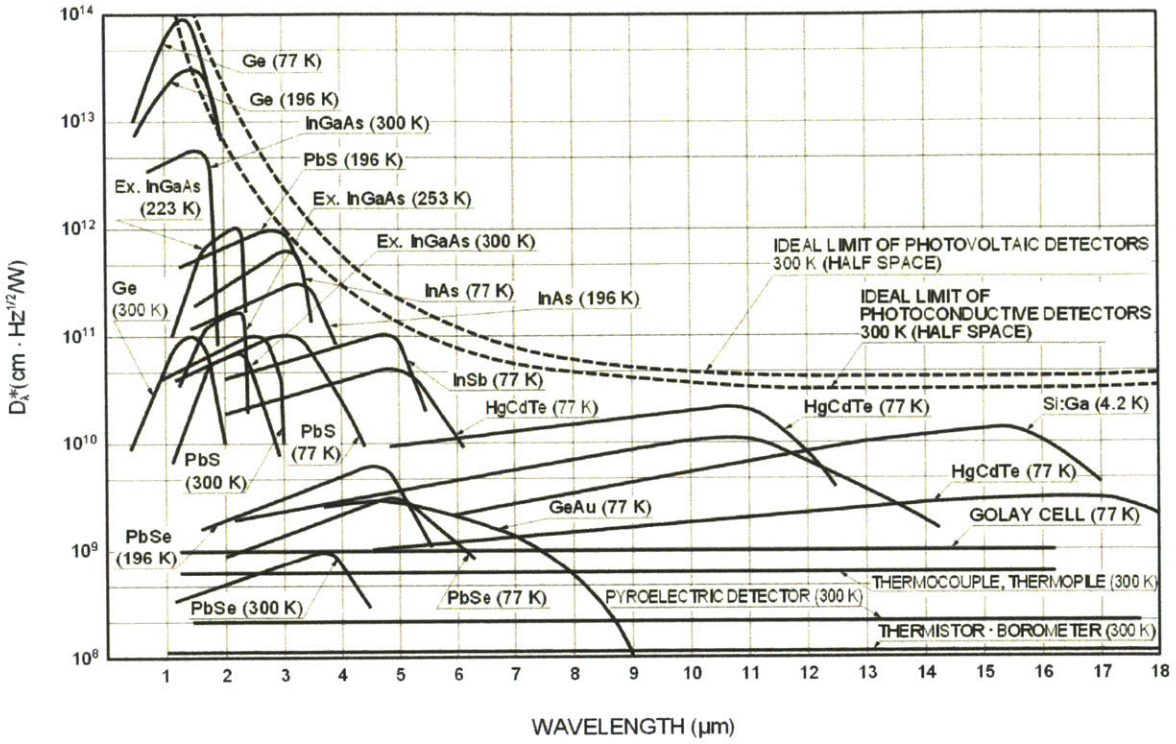

Figure 4-2: Various Infrared Detection Technologies [18]

Type	Detector	Spectra Response (μm)	Operating Temperature (K)	D* (cmHz$^{1/2}$/W)
Thermal	Thermocouple-thermopile	Window	300	6×10^8
Thermal	Bolometer	Window	300	1×10^8
Thermal	Golay cell, condenser-microphone	Window	300	1×10^9
Thermal	PZT, TGS, $LiTaO_3$	Window	300	2×10^8
Photoconductor	PbS	1-3.6	300	1×10^9
Photoconductor	PbSe	1.5-5.8	300	1×10^8
Photoconductor	InSb	2-6	213	2×10^9
Photoconductor	HgCdTe	2-16	77	2×10^{10}
Photovoltaic	Ge	0.8-1.8	300	1×10^{11}
Photovoltaic	InGaAs	0.7-1.7	300	5×10^{12}
Photovoltaic	Ex. InGaAs	1.2-2.55	253	2×10^{11}
Photovoltaic	InAs	1-3.1	77	1×10^{10}
Photovoltaic	InSb	1-5.5	77	2×10^{10}
Photovoltaic	HgCdTe	2-16	77	1×10^{10}

Table 4.1: Comparison of D* for various infrared detection technologies [18]. The spectral response of thermal detectors is determined by the window material (ZnSe, Si, Ge, etc.)

mentioned before, hot blackbodies emit incoherent infrared radiation corresponding to their temperature. Therefore by properly designing a thermal system and isolation for the system, infrared detection can be thought of as a radiative heat detector, where incident infrared photons are absorbed and transformed into a temperature gradient. The temperature increase is proportional to the incident power and the amount of thermal isolation (R_{th}), which can then be read off utilizing a number of transduction mechanisms. However, since this type of detector is a thermal device, the time constant of the device is limited mainly by the thermal time constant rather than the electronic time constant, which places a trade-off with regard to speed and sensitivity. The general form of D* for thermal devices follows from equation 4.4, where we assume a signal transduction mechanism K_{conv} (V/K), that converts optical power into temperature:

$$D^* = \frac{\epsilon K_{conv} R_{th}}{\sqrt{1+\omega^2\tau_{th}^2}} \frac{\sqrt{a_0 b_0 \Delta f}}{\sqrt{V_j^2 + V_{th}^2 + V_{1/f}^2}} \tag{4.4}$$

$$V_j^2 = 4k_B T R_e \Delta f \tag{4.5}$$

$$V_{th}^2 = \frac{4k_B T^2 \Delta f}{1+\omega^2\tau_{th}^2} K_{conv}^2 R_{th} \tag{4.6}$$

$$V_{1/f}^2 = k_{1/f} \frac{I^\delta}{f^\beta} \Delta f \tag{4.7}$$

in which ϵ is the emissivity, τ_{th} is the thermal time constant, ω is the modulation frequency, R_{th} is the thermal resistance, V_j is the Johnson thermal noise, V_{th} are the thermal fluctuations noise, and $V_{1/f}$ is the flicker noise in the system, R_e is the electrical resistance of the material, $k_{1/f}$ and I^δ are phenomological fits for the flicker noise. While Eq. 4.4 is a general expression for thermal detectors, what differs amongst the various technologies is the contributions of these various noise sources, as well as the method of transduction from temperature to an electrical signal. There are three main technologies for the direct conversion of temperature into a measurable

electrical signal: (1) Bolometers (2) Thermoelectrics and (3) Pyroelectrics.

Bolometers

These detectors utilize the temperature dependent change in resistivity which can be expressed as

$$V_{total} = I_{meas} R_0 (1 + \alpha_{TCR}) \Delta T) \tag{4.8}$$

$$K_{conv} = \frac{\Delta V}{\Delta T} = \alpha_{TCR} I_{meas} R_0 \tag{4.9}$$

where α_{TCR} is the temperature dependent change in resistivity (TCR) of a material. Since a bolometer is a passive resistor (R_0), the detection mechanism requires inputting a current or voltage to measure the actual change in temperature. Therefore the measured voltage out from the device is simply the measurement current (I_{meas}) multiplied by R_0 and α_{TCR}, which can be increased by increasing the measurement current. Obviously, in this approach, there are always issues with self-heating effects that limit the largest I_{meas} one can achieve. The current state of the art, in terms of materials with a large TCR, are amorphous silicon with 2.5 %/K and vanadium oxide with >4%/K [172]. Typically these devices can have responsivities of well over 10,000 V/W; however, due to the need for biasing these devices, in order to measure the resistance change, they often can have additional noise due to 1/f noise.

Thermopiles

Thermopile detectors operate on a different transduction mechanism, where as opposed to a passive system, a thermopile detector operates on the thermo-electric effect, where temperature gradients (ΔT) can induce a voltage through the Seebeck effect (S) and

$$V = S \Delta T \tag{4.10}$$

$$K_{conv} = \frac{\Delta V}{\Delta T} = S. \tag{4.11}$$

A Thermopile is similar to thermo-electric power generation where by introducing a temperature gradient, power can be generated; however, in the case of a detector, we are not concerned with power generation but rather with the signal to noise ratio. The advantages with thermopiles are their large dynamic range and linearity of these detectors, which is why they are often used for astronomical applications [173–175]. Furthermore, since they are self-powered without the need for an input bias, they are traditionally only Johnson or thermal noise limited. Unfortunately, while in bolometers the signal can be amplified by a larger input current, the signal from these devices is limited by the magnitude of the Seebeck coefficient (S $\sim$ 10-100 μV/K), which requires the need to place many thermo-couples in series in order to increase the total measured voltage. This unfortunately places a larger constraint on the thermal isolation of these devices. A wide variety of materials (metals and semiconductors) can be chosen for thermo-electric detectors. However, in order to create a large thermal voltage, two materials of different carrier type (p-type or n-type) are required.

Pyro-electrics

Unlike the previous two devices which can operate under DC conditions, pyro-electric detectors are inherently AC detectors. Because of this requirement, the input radiation must be modulated, not only to decrease 1/f noise, but also to ensure a time dependent change in temperature rather than a static change in temperature. Two modes of operation are possible with a pyro-electric detector: (1) A rapid change of temperature disrupts the spontaneous polarization of a material and this effect depends on the pyro-electric coefficient (p) or (2) the change in temperature alters the dielectric constant of a material, thereby changing the amount of stored charge on a capacitor. However, in both cases the device still requires a modulated input source (optical chopping). Equation 4.10 shows the signal response due to a temperature change; however, traditionally for pyroelectric detectors, the output signal is treated

as a current signal (i_p) due to the capacitive nature of the device [172, 176, 177]:

$$i_p = Ap\frac{dT}{dt} = Ap\omega\Delta T \tag{4.12}$$

$$K_{conv} = Ap\omega \tag{4.13}$$

4.2.3 Optical Detectors

Optical detectors, on the other hand, operate by the direct conversion of incident photons into excited charged carriers, which either generate a measureable photovoltage or generate a change in conductivity. However, in order for this to occur, the material's electronic structure must allow for direct optical transitions between the conduction and valence band in the mid-infrared. Therefore, materials that have an appropriate band gap (0.024-0.3 eV) are traditionally part of the InSb or HgCdTe family [178–181]. In addition, instead of an interband processes, also intraband quantum well infrared photodetectors (QWIPS) can be used, where electrons can be excited between intersubband quantum well transitions [182–184]. However, because carriers require excitation by low energy photons, thermal energy from the ambient environment can lead to excess carriers within the sample; therefore, while unlike thermal detectors which operate at room temperature, photon-based detectors are often chilled to liquid nitrogen temperature (77K) in order to suppress the thermal generation of carriers that are not induced by incoming photons. This is expressed by the figure of merit D* for optical detectors in equation 4.14.

$$D^*_{pc} = 0.31\frac{\lambda}{hc}\sqrt{\frac{\alpha_{opt}}{G}} \tag{4.14}$$

where, α_{opt} is the optical absorption, $G = G_{opt} + G_{th}$ is the total carrier generation rate which is composed of noise sources due to the optical excitation of carriers from environmental blackbody radiation (G_{opt}), and thermally generated carriers (G_{th}).

4.2.4 Comparison between Thermal versus Optical Detectors

Each type of detector has various advantages and disadvantages for different applications. To illustrate these differences, we look at the fundamental sensitivity of these two detection approaches, where we assume that the noise is always limited by the noise due to heat transfer between the detector and the surrounding environment. However, even though one can try to eliminate heat transfer due to conduction and convection, radiative heat transfer is always present, which sets the fundamental lower bound for thermal-based detectors shown in Equation 4.15:

$$D^*_{th} = \left(\frac{R_t h \epsilon^2 A_0}{4 k_B T^2}\right)^{1/2} = \left(\frac{\epsilon}{8 k_B \sigma (T_d^5 + T_b^5)}\right)^{1/2} \tag{4.15}$$

Therefore, assuming a room temperature thermal detector viewing a room temperature background, the figure of merit D^*_{th} is limited to around 1.98×10^{10} cmHz$^{1/2}$/W, even upon cryogenic cooling. However, in the case for photon-based detectors, a similar fundamental limit also applies. While unlike thermal detectors which can be operated at room temperature, photon-based detectors are noisy due to thermally generated carriers, which is why these detectors must always be cooled down to cryogenic temperatures. However, even under cryogenic temperature operation there is always noise due to background blackbody photons emitted from the surrounding environment (Eq. 4.16) [185]:

$$D^*_{BL} \approx \left[sin^2\theta_0 \frac{4\pi (k_B T)^5}{c^2 \hbar^3} x_c^2 (x_c^2 + 2x_c + 2) e^{x_c}\right]^{-1/2} \tag{4.16}$$

where ω_c is the lower cutoff frequency, and θ_0 is the cutoff viewing angle of the detector. This fundamental limit is plotted in Figure 4-2 for both photovoltaic and photoconductive devices assuming materials with various wavelength cutoffs and a viewing angle of $\theta_0 = \pi/2$. In addition, thermal detectors are limited by the thermal time constant of the detector, whereas photon-based detectors are limited in speed by carrier transport, such as the drift or diffusion velocity within a sample.

4.3 Graphene for Infrared Detection

While we have discussed the inherent differences between photon versus thermal-based detection, we return to the original problem of applying graphene for the detection of infrared radiation. In atomically thin monolayer graphene (MLG), broad band photodetectors and optical modulators have been demonstrated in the near-infrared range (E_{ph} =0.8-1.6eV), and have been shown to be capable of ultra-fast response times (>10GHz) [89,186]. However, these experiments focused on photon energies that are much larger than the intrinsic energies of the system, such as the optical phonon energy (E_{op} = 0.2eV) or the electrostatically controllable Fermi Energy of MLG (E_f 0.5eV) [89–91,187]. For MLG photo-excited in the MIR, very recent work has shown active modulation due to Pauli blocking [33, 188] as well as interesting plasmonic effects [189–191]. Many experiments have begun to explore MLG's unique optoelectronic properties while attempting to make use of its unusual broadband optical absorption from the far-infrared all the way to the visible [6,192–196]. However, more recently, experiments in the visible on graphene have begun to show that not only are optical effects possible within graphene, but thermal effects as well [90, 91, 187]. Therefore, distinguishing the dominant physical photo-detection mechanisms at low energies is critical for illuminating MLG's potential role as a MIR photodetector.

Unlike photovoltaic detectors where only photons absorbed by the active material (MLG) can generate a signal, here we find that MLG acts as the key element in a novel hybrid ambipolar infrared thermocouple, converting a temperature gradient into a voltage signal at the thermocouple junction. We experimentally identify the energy conversion mechanism of the electrostatically controlled device and the key parameters for engineering the MIR (E_{ph} = 0.117 eV) photo-response. We measure the photovoltage response of these devices as a function of carrier density (n_s), carrier density difference (Δn_s), substrate material, and temperature, and find that MIR detection is well described within a thermoelectric framework. Of key importance, extrinsic properties of the surrounding environment must be included to fully understand the photovoltage response. To locally photo-excite MLG at low photon

energies below 0.2 eV, we constructed a CO_2 ($\lambda = 10.6$ μm, $E_{ph} = 0.117$ eV) scanning laser microscope capable of measuring the spatial photo-response of our devices as a function of temperature and gate bias (Figure 4-3(a)). All measurements (optical and electrical) were done using an AC lock-in technique.

4.3.1 Infrared Scanning Photovoltage System

The light source was a temperature stabilized 1W CO_2 laser (Access Laser Company) providing a collimated light source at a wavelength (λ) of 10.6 μm. After mechanical chopping, the laser power on the sample was typically 8 mW as determined by a reference thermal power meter (Thor labs). A beam combiner optic (ULO optics) was used to add a collinear laser(632 nm laser diode) for alignment (not shown in Figure 4-3(a)). A set of galvanometer controlled mirrors produces angular deflections centered at the focal point of lens 1 (L1 in Figure 4-3(a)). These deflections were then mapped through a relay of confocal optics (L1 and L2) onto the back focal plane of the objective. The confocal optics directs the beam to strike the objective (L3) at the same position, but at a variable angle set by the galvanometer mirrors, producing distortion free scanning over a large ($>1\text{mm}^2$) area. The beam was then passed through a ZnSe anti-reflection coated window into an optical cryostat (Janis) allowing measurements to be done under vacuum and at low temperatures (77K$<$ T $<$300K). To reduce the noise in our measurements, the laser is modulated with an optical chopper wheel operating at 368Hz before it is sent to the galvo mirrors. A lock-in amplifier operating in a differential voltage mode is connected across the two contacts of the device (M1 and M2) and synced to the output reference from the chopper wheel. The surface reflectance image of the chip was simultaneously recorded as a function of laser position by the reference thermal power meter. The metallic bond pads (M1 and M2) provide high contrast features on the chip to orient our device and to align our laser spot to the junction signal. The reflected signal also provides feedback on the stability of the laser power and alignment during scanning. Laser power attenuation was achieved by utilizing a Brewster window attenuator (ULO optics) and by feeding the input beam through a series of cross polarizers. We also

measured the response of the device purely as a function of laser polarization and saw no change in the signal, ensuring that we measured the effect of only the power dependence using the attenuator.

4.3.2 Device Fabrication and Characterization

Figure 4-3(a) shows the structure of the ambipolar graphene infrared thermocouple, composed of a large area MLG p-n junction device supported on top of an aluminum oxide (Al_2O_3) gate dielectric. The underlying substrate consisted of 300nm of thermally grown oxide on heavily doped p+ silicon. Two independent titanium-platinum gate electrodes (V_{G1} and V_{G2}) were then patterned by electron beam-lithography and encapsulated by the gate dielectric (60nm ALD Al_2O_3). The gap between the gate electrodes was designed to be 300-500 nm (sub-wavelength across all photon energies used). MLG grown on copper foils, using a chemical vapor deposition (CVD) technique, was then transferred on top using poly(methyl methacrylate) (PMMA) [84]. Atomic force microscopy (AFM) confirmed that the sample was a uniform monolayer while Raman spectroscopy confirmed that there was minimal sample doping due to the high 2D-band (ω_{2D} 2680 cm^{-1}) to G-band (ω_G 1580 cm^{-1}) intensity ratio (I_{2D}/I_G =8.5) and a low concentration of defects by the low D-band to G-band intensity ($I_D/I_G \approx 0$). Finally, electron beam lithography and reactive oxygen etching defined the titanium-gold ohmic contacts (M1 and M2) and the graphene channel, respectively (Figure 4-3(b)).

We first characterize the ambipolar graphene infrared thermocouple by measuring the gate voltage dependent resistance (R) and the photovoltage (V_{PH}). We measured R (shown in Figure 4-3(c)) by applying 25μV between M1 and M2 while simultaneously measuring the current. The voltage V_{G1} and V_{G2} were kept equal during the resistance sweep ($V_{G1} = V_{G2}$). The maximum transconductance (g_m) calculated from Figure 4-3(c), allows us to estimate the hole carrier mobility (μ_p) of our MLG to be 800± 100 $cm^2V^{-1}s^{-1}$. To form an ambipolar thermocouple in our device, the gates were then biased oppositely (V_{G1} = 10V, V_{G2} = -10V) to create a p-n junction. Figure 4-3(d) shows the photovoltage V_{PH} measured between M1 and M2 while the laser is

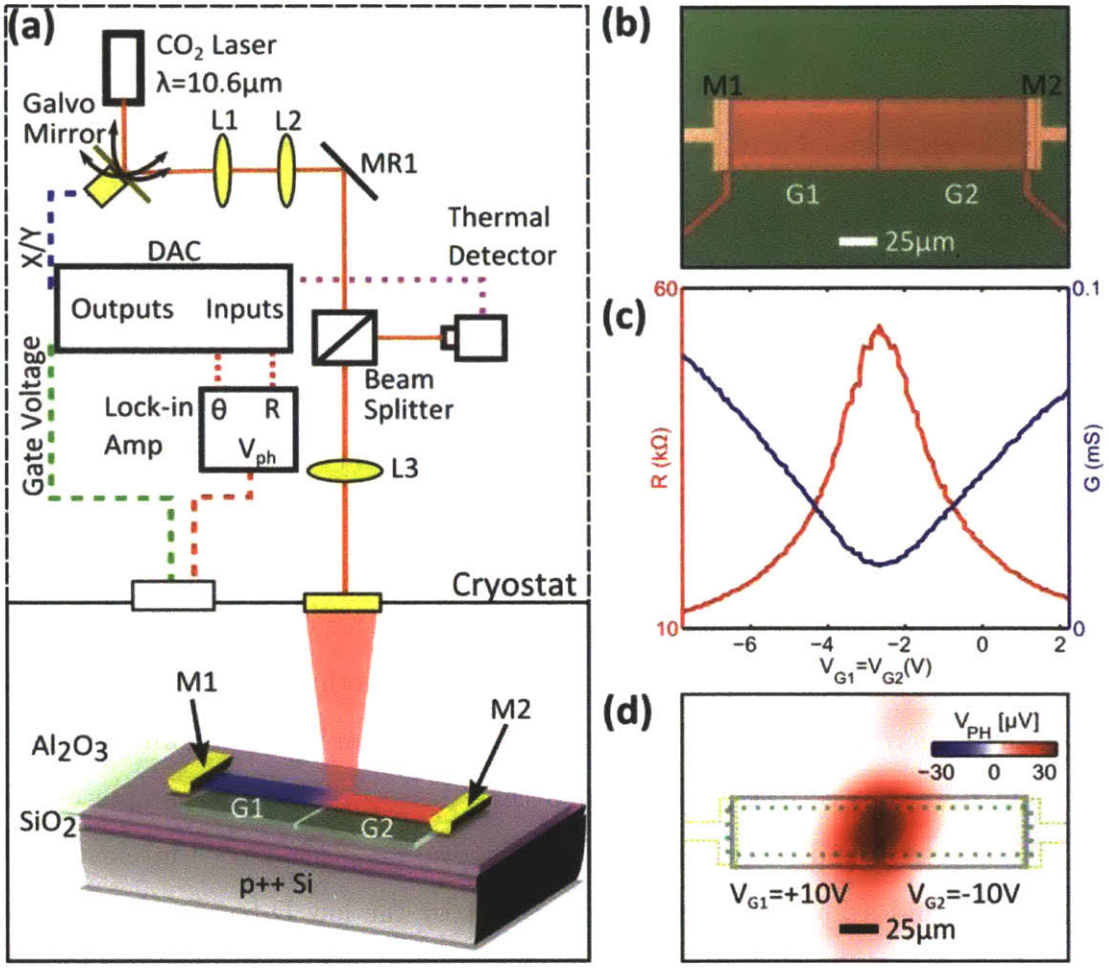

Figure 4-3: IR Confocal Microscopy (a) Schematic of the scanning mid infrared laser microscope. The CO_2 laser beam is scanned across the sample using a galvo-mirror and the beam is fed into a cryostat through lens L1 to L3. A schematic of the ambipolar graphene infrared thermocouple is shown in the lower left hand corner. (b) Optical layout of the fabricated device. M1 and M2 are the ohmic contacts to the MLG; G1 and G2 are the local electrostatic gates. (c) Resistance-Gate Voltage measurements of the device, where $V_{G1} = V_{G2}$, are shown in red. Shown in blue is the conductance versus gate voltage using the right axis. (d) Spatial map of the photovoltage response from the device. The MLG is outlined by a dotted green line, while the local electrostatic gates are outlined in grey. The contacts are outlined by a dotted gold line. The gate voltages are biased to form a p-n junction (V_{G1} = +10 V and V_{G2} = -10 V).

scanned over the device. Due to the diameter of our laser spot ($\approx 20\mu$m), we chose the dimensions of our device ($L = 200\mu$m, $W = 30\mu$m) to allow us to spatially resolve the photoresponse. Figure 4-3(d) shows that the photoexcitation in the region near the p-n junction results in a large, positive photovoltage, while the contacts contribute negligible signal.

The photovoltage mechanism can be identified by measuring the response as a function of charge carrier density (n_s) and carrier density difference (Δn_s) at the p-n junction. Figure 4-4 (a) shows the dual gate resistance map of our devices. The red cross shape in Figure 4-4 (a) indicates that the two gates are independent and can electrostatically control each half of the MLG channel. The peak or maximum resistance occurs when both gates are biased at the charge neutrality point (V_D) at approximately V_{G1} = -3V, V_{G2} = -3V, while the resistance of the device decreases as the number of charge carriers increases due to electrostatic doping. Due to the long geometry of our device and small lateral gap between gates, the resistance of the p-n junction itself is negligible compared to the bulk resistance of the MLG channel [197–199]. Figure 4-4(b) shows V_{PH} when we fix the laser spot at the p-n junction and sweep over the same gate voltages as in Figure 4-4(a). The four distinct charge carrier configurations in each half of the device are labeled in Figure 4-4(b): p-n, n-n', n-p, p-p'. A distinctive 6-fold pattern of alternating photovoltage polarity is observed due to the sign change when V_{G1} or V_{G2} crosses either a charge neutrality point or the diagonal where $\Delta n_s = 0$ [90, 187].

We can use the inherent symmetry of the photovoltage gate map to extract line cuts of the data set that contains the most relevant information. While previously in Figure 4-3(c), we plotted the line cut where $V_{G1} = V_{G2}$, which corresponds to $\Delta n_s = 0$, in Figure 4-4(c) we plot the line cut $V_{G1} = -V_{G2}$ cutting through the charge neutrality point in both the resistance map and the photovoltage map. This line cut corresponds to fixing the junction's carrier density at the charge neutrality point, while the MLG to the left and the right is doped so that Δn_s varies from negative to positive. As mentioned before, the resistance line cut (shown in red in Figure 4-4(c)) looks quite similar to our previous line cut in Figure 4-3(c), thus confirming

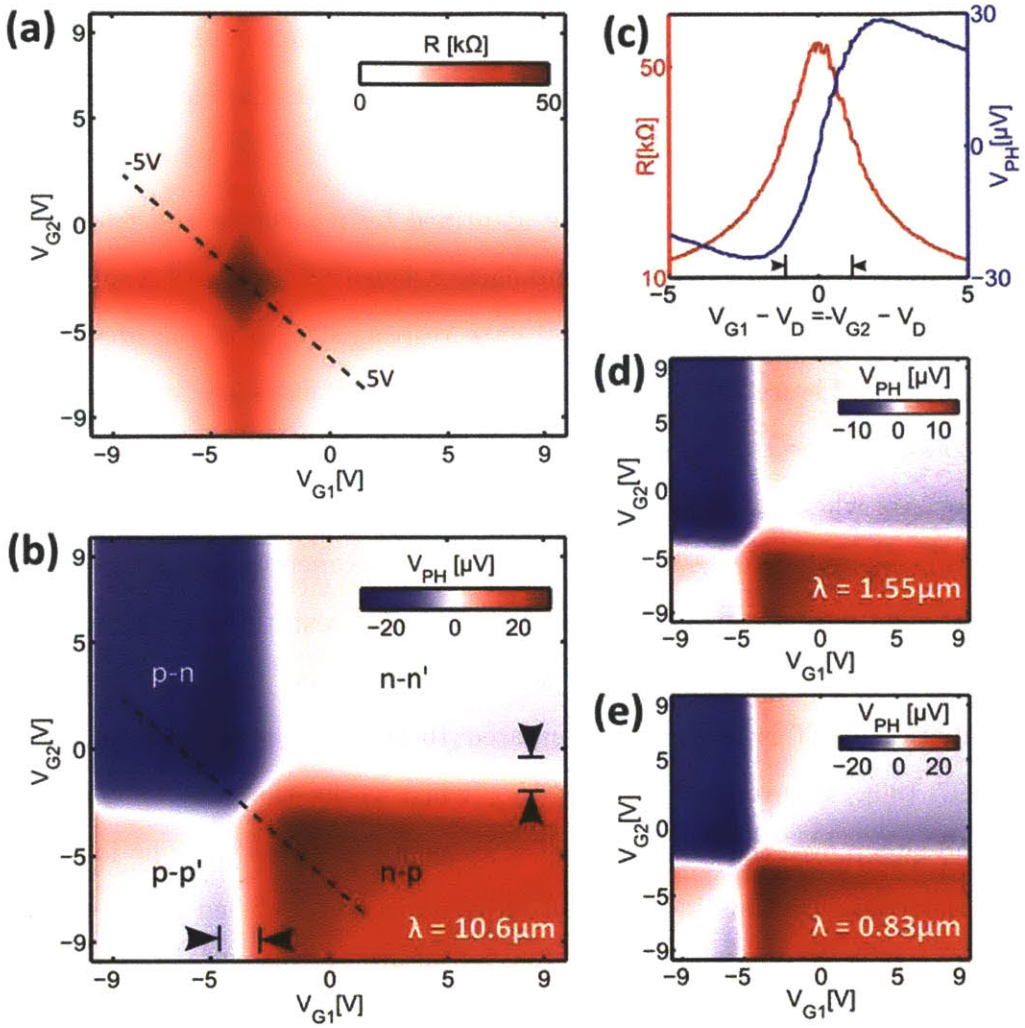

Figure 4-4: Photovoltage and I-V maps of Graphene Devices (a) Dual gate resistance map of the ambipolar graphene infrared thermocouple. The dashed line indicates the position of the line cut shown in (c) that corresponds to increasing Δn_s. (b) Dual gate photovoltage map of the ambipolar graphene infrared thermocouple with $\lambda = 10.6\mu$m photoexcitation. The gate voltage range between the arrows is where transitions are not Pauli blocked. The four carrier quadrants are labeled p-n, n-n', p-p', n-p. (c) Line cuts through the resistance and photovoltage maps in the positions indicated by the dashed line in (a) and (b). (d) and (e) Dual gate photovoltage maps of the ambipolar graphene infrared thermocouple with a $\lambda = 1.55\mu$m and 0.83μm excitation. The photovoltage at 1.55 μm is smaller due to lower power transmitted to the sample. All measurements taken at 300 K.

that the p-n junction makes only a small contribution to the resistance of our devices. Furthermore, the line cut (shown in blue in Figure 4-4(c)) through the photovoltage map shows a roll off at large Δn_s and a positive and negative maximum located near the charge neutrality point. Also in Figure 4-4(c), under MIR photoexcitation of the p-n junction, we observe no noticeable transition between the Pauli allowed (high absorption $E_f < 1/2E_{ph}$) and the Pauli blocked (suppressed absorption $E_f > 1/2E_{ph}$) regime. The threshold gate voltages where Pauli-allowed transitions can occur at 10.6μm (0.117eV) are indicated in Figure4-4(b) and(c). While these experiments were done to probe very low photon energies, we also took the same device and repeated the experiments (photovoltage maps) at $\lambda = 1.55$ μm (E_{ph}=0.8 eV) and at $\lambda = 0.83$ μm (E_{ph}=1.49 eV) shown in Figures 4-4(d) and 4-4(e), respectively. The data sets at both higher photon energies also show the distinctive 6 fold pattern that indicates a thermoelectric mechanism.

4.3.3 Device Model

In the ambipolar graphene infrared thermocouple, the incident radiation is absorbed near the p-n junction and increases the local temperature (T_{hot}) relative to the contacts (T_{cold}). The thermal gradient is established across both the MLG and within the infrared absorber (Al_2O_3). Photons are absorbed optically and are converted into a thermal bath composed of both phonons and electrons. The thermal gradient ($\Delta T = T_{hot} - T_{cold}$) between the p-n junction and the contacts results in holes and electrons near the Fermi energy level diffusing away from the junction, thereby establishing a photo-induced voltage via the thermoelectric effect (Figure 4-5 (a)) [200]. The difference between MLG's Seebeck coefficients (S_1 and S_2) on each side of the junction results in the six fold symmetry observed in previous work [90, 187]. The gate dependence of the photovoltage signal can be written as:

$$V_{ph}[V_{G1}, V_{G2}] = [S_1(V_{G1}) - S_2(V_{G2})]\Delta T \tag{4.17}$$

The gate tunable Seebeck Coefficient ($S(V_G)$) of the MLG follows from Mott's

relation [200, 201], and exhibits a sign change as V_{Gi} crosses the charge neutrality point (embedded in the term dR/dV_G) in the following equation:

$$S_{i1}(V_{Gi}) = \frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{1}{R_i}\frac{dR_i}{dV_{Gi}}\frac{dV_{Gi}}{dE}\bigg|_{E_f} \tag{4.18}$$

Here, k_B is the Boltzmann constant, T is the temperature, q is electron charge, E_f is Fermi energy and V_{Gi} (i=1,2) is the bias on the left and right gate embedded in the infrared absorber. The magnitude of the Seebeck coefficient can be increased by decreasing the disorder near the charge neutrality point, leading to a larger derivative term. Optical absorption deposits power in the device and creates a thermal gradient, which we can write as:

$$\Delta T = \frac{1}{\kappa_{eff}} P_{in}\left[1 - e^{-\alpha t}\right]. \tag{4.19}$$

Here P_{in} is the incident laser power, κ_{eff} is the effective thermal conductance between the p-n junction and the contacts, taking into account the parallel thermal paths, t is the thickness of the material at the device junction, and α is the optical absorption of the material. As evidenced by the absence of Pauli blocking, optical absorption through the formation of electron-hole pairs is not the dominant mechanism for establishing a temperature gradient ΔT. We note that the length of our devices (L=200 μm) is much longer than the estimated electronic cooling length ($\approx 2\mu$m), allowing us to neglect hot-carrier mechanisms that have been reported previously [90]. Based on this physical understanding, we can make several predictions to validate our model and engineer improved sensitivity.

We first compute the expected gate-dependent Seebeck coefficient (S_1 and S_2) purely from the resistance map using equation 4.18. Independently, we also extract the two Seebeck coefficients from our photo-voltage map using a Fourier transform (FT) of equation 4.17 with respect to V_{G1} and V_{G2} [90]. This is possible since the two Seebeck coefficients in equation 4.17 are assumed to be linearly independent with respect to gate bias (V_{G1} and V_{G2}). Filtering the data along the x and y axis in Fourier space and then inverting the FT, we can find the experimentally measured Seebeck

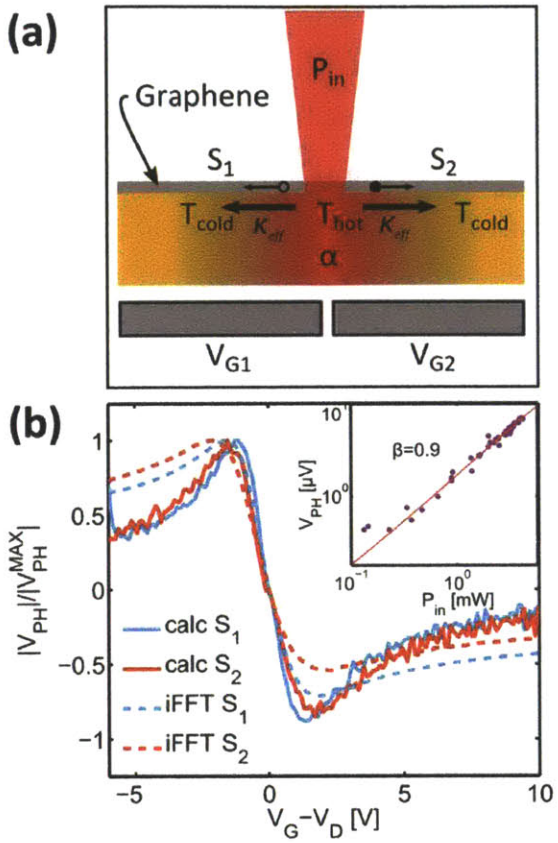

Figure 4-5: Model of Graphene IR detection mechanism (a) Schematic of our thermoelectric device. Hot carriers at the junction (solid circle represents electrons, empty circle represents holes) diffuse away from the local heat spot generated by the laser. The temperature difference between the junction temperature (T_{hot}) and the ambient temperature (T_{cold}) is controlled by the optical absorption (α) and thermal conductance (κ_{eff}) of the substrate. (b) Seebeck coefficients calculated from the resistance map in Figure 4-4(a) using Mott's relation (solid lines) and independently extracted from the photo-voltage map in Figure 4-4(b) using a Fourier transformation analysis technique (dashed lines). The inset shows the photo-voltage as a function of incident optical power (P_{in}) at $\lambda = 10.6$ μm. The fit line is $log(V_{PH}) = \beta log(P_{in}) + c$ with a coefficient (β) of 0.9.

coefficients from Figure 4-4(b) (shown in the main panel of Figure 4-5(b) as dotted lines). The agreement between extracted and calculated coefficients further supports our thermoelectric model since these coefficients are responsible for the multiple sign reversals (6 fold pattern) observed in our map, as opposed to single sign reversal expected from photovoltaic effects [201]. Furthermore, the inset of Figure 4-5 (b) shows the photovoltage response as a function of incident power (P_{in}). The linear power dependence that we observe in the slope of this plot (β=0.9) is consistent with Fourier's law (equation 4.19) in this range of optical power levels.

4.3.4 Substrate Interactions

Given its limited thickness, the MLG is an excellent thermal conductor as well as a broad band absorber [202–204]; however, the infrared absorber material has an absolute bulk thermal conductance and optical absorption that can be equally important, depending on the geometries involved. Within our model, the thermal conductance (κ_{eff}) and the optical absorption (α) are central to the photo-response mechanism of our devices. However, two questions naturally arise: (1) does the laser primarily heat up the MLG (optical free carrier absorption) or instead the infrared absorber around the MLG (substrate optical absorption, etc.), and (2) which thermal conductance dominates our device (the MLG's or the infrared absorber's thermal conductance)?

Our model predicts that increasing the optical absorption in our devices should lead to an increased photovoltage signal. To test this prediction, we fabricated identical devices as previously shown in Figure 4-3(b); however, we replaced the Al_2O_3 infrared absorber with SiN, which has a larger optical absorption ($\alpha = 1.3\mu m^{-1}$) than Al_2O_3 ($\alpha = 0.34\mu m^{-1}$) at $\lambda = 10.6$ μm [205]. Figure 4-6(a) shows the transport behavior ($V_{G1} = -V_{G2}$) of the SiN devices compared to the previously discussed Al_2O_3 devices, taken at temperatures ranging from 100K to 300K. The resistance curves of both devices exhibit a weak temperature dependence and the calculated Seebeck coefficients (equation 4.18) are similar in magnitude for both devices (Figure 4-6 (b)).

In contrast, the measured photovoltage signal is twice as large at room temperature for the ambipolar graphene infrared thermocouple supported on SiN (with larger

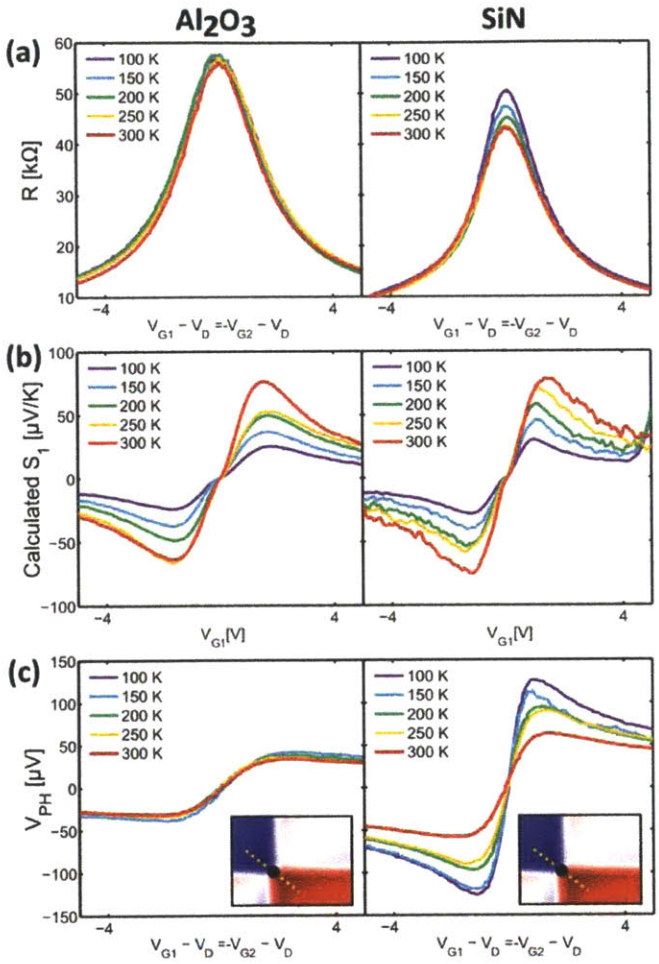

Figure 4-6: Substrate and Temperature Dependence (a) Resistance-Gate Voltage measurements of the ambipolar graphene infrared thermocouple utilizing different infrared absorbers (ALD Al_2O_3 on the left and PECVD SiN on the right) at various temperatures (100 K-300 K) (b) The Seebeck coefficients computed from the transport data in (a); for simplicity, we plot the dependence on one gate only, due to the symmetric behavior of the resistance maps. (c) The measured photo-voltage response for 5 values of temperature for each infrared absorber. The insets on the lower right corner show schematically where the line cuts were taken in the complete dual gate response at 300K.

MIR absorption), compared to Al_2O_3 (Figure 4-6(c)), even though the transport behavior is highly similar in both devices. From this result, we conclude that the optical absorption mainly occurs in the infrared absorber ($\alpha \approx \alpha_{SUB}$).

As heat is deposited and diffuses away, the magnitude of the temperature gradient (equation 4.19) will be determined primarily by the highest thermal conductance. To study this effect we measure the temperature dependence of both devices, and find distinct trends for each infrared absorber material. Our model (equations 4.17, 4.18,4.19) states that the temperature dependence follows $V_{ph} \propto T/\kappa(T)$, where $\kappa(T)$ is the temperature dependent thermal conductance and α is temperature independent (no thermo-optic effect). In Figure 4-7, we plot comparatively the normalized maximum photovoltage (V_{PH}^{MAX}) and the quantity $< \kappa_{eff} > \propto T/V_{PH}^{MAX}$ (normalized effective conductance) as a function of temperature for both Al_2O_3 and SiN. As a function of temperature, the photovoltage increases with decreasing temperature, but at a much larger rate for devices with an SiN infrared absorber. Within that temperature range (100-250 K), the quantity $< \kappa_{eff} >$ exhibits a decreasing trend with distinct slopes for Al_2O_3 vs. SiN, regardless of the illumination wavelength in the designated range. Fitting this data to a power law $< \kappa_{eff} > \propto T^{\gamma}$, we find that $\gamma \approx 1$ for Al_2O_3 ($T^{1.14}$ at 0.83 μm and $T^{0.99}$ at 10.6 μm) and $\gamma \approx 1.5$ for SiN ($T^{1.41}$ at 0.83 μm and $T^{1.55}$ at 10.6 μm). These values show excellent agreement with thermal conductivity measurements for amorphous dielectric solids in the regime where strong phonon scattering limits thermal conductance [206, 207].

By integrating the electrostatically controlled MLG with carefully chosen infrared absorbers, we construct a highly sensitive ambipolar graphene infrared thermocouple. The device sensitivity can be engineered by choosing substrate materials with a high MIR absorption and low thermal conductance. A thermoelectric description captures important aspects of the device response for a wide variety of conditions: temperatures (100-300K), photon energies (0.117-1.49eV), and substrate materials. While the MLG can exhibit a Seebeck coefficient ($\pm$ 50μV/K) similar to a variety of other standard thermoelectric detectors, such as poly Si, Sb, and Bi [172], the MLG embedded into a hybrid thermal device has one major advantage: an atomic layer of graphene

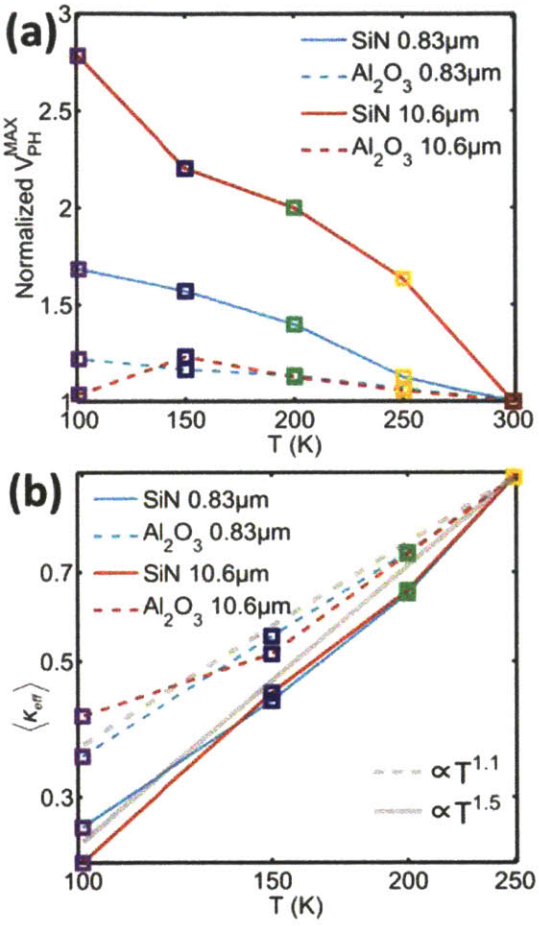

Figure 4-7: Extracted Thermal Conductivity Data (a) The maximum V_{PH} normalized with respect to the maximum V_{PH} taken at 300 K as a function of temperature under 4 conditions. The solid lines represent measurements taken for SiN while the dotted lines represent the data for Al_2O_3. The color indicates the excitation source for the measurements (red is λ=10.6 μm, while blue is λ=0.83 μm). (b) Temperature dependence of the normalized effective thermal conductance $< \kappa_{eff} >$ for both the SiN and Al_2O_3 substrates plotted on a log-log scale. The grey lines show the power law (T^{γ}) fitting to the data: γ is 1.1 and 1.5 for SiN and Al_2O_3 respectively.

adds a negligible thermal mass, yet generates a significant MIR photovoltage signal. This work provides a significant step forward towards engineering MLG devices that extract energy from thermal gradients, a technology that may have applications in human positioning detectors, passive sensors, such as nanoscale monitors of chemical reactions, as well as transparent and flexible thermal sensors and energy harvesting devices. Therefore given this insight, in the following chapter, we further explore the potential application of graphene as a thermal based imaging technology.

Chapter 5

Graphene-based Infrared Thermal Detectors

In this chapter, we examine and demonstrate some potential applications, as well as technology based upon graphene infrared thermal detectors. We will begin by examining the fundamental sensitivities of graphene-based thermopiles and examine the effect of a tunable Seebeck coefficient on D*. Based upon these estimates, we integrate graphene into micro-electro-mechanical system to provide improved thermal isolation. Finally, as we look towards the future, we will conclude this chapter by investigating some technology development of a monolithic process to integrate graphene with standard silicon CMOS for potential applications for graphene based infrared cameras.

5.1 Performance Analysis

While initially, graphene's broadband optical absorption was an interesting property for infrared detecion, the previous chapter suggests that the more dominant detection mechanism at infrared energies is actually thermo-electric in nature. Given this understanding of the infrared detection mechanisms in graphene, we can now better evaluate the potential applications and performance of this graphene-based technology. Starting with the transduction method that we modeled in Chapter 4, we rewrite

here the expression for Mott's relation:

$$S_{i1}(V_{Gi}) = \frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{1}{R_i}\frac{dR_i}{dV_{Gi}}\frac{dV_{Gi}}{dE}\bigg|_{E_f}. \tag{5.1}$$

In addition, in Chapter 1, we also constructed a square root charge model to take into account charge puddles near the Dirac point, also employing

$$R_{sh} = \frac{1}{q\mu\sqrt{n_s^2 + n_0^2}} \tag{5.2}$$

where $n_s = \frac{C_{ox}}{q}(V - V_D)$. If we combine equations 5.1 and 5.2, we can derive an explicit relationship for the Seebeck coefficient in terms of n_s:

$$S = \frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{2}{\hbar v_f\sqrt{\pi}}\frac{-n_s^{3/2}}{n_s^2 + n_0^2} \tag{5.3}$$

As we have shown before, the Seebeck coefficient is a tunable value; however, S has a maximum and minimum value located at $n_{SMAX} = \pm\sqrt{3}n_0$. When computing the maximum Seebeck coefficient (S_{MAX}) in equation 5.4, we find that interestingly enough, this quantity does not depend on the mobility of the graphene, but only on the density of charged puddles (n_0) within the sample:

$$S_{MAX} = \pm\frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{2}{\hbar v_f\sqrt{\pi}}\frac{3^{3/4}}{4}\frac{1}{\sqrt{n_0}}. \tag{5.4}$$

Equation 5.4 is plotted in Figure 5.1 as a function of charge puddle density (n_0), which as discussed in Chapter 1 and 2 and is primarily dependent on the graphene transfer and substrate interaction.

However, while in our analysis of graphene's Seebeck coefficient, we find that the maximum Seebeck coefficient is independent of mobility, the mobility is still an important factor when looking at the main figure of merit, which is the detectivity (D*). If we return back to our general expression for the detectivity for thermal detectors (Eq. 4.4), and include thermo-electric mechanisms (signal generation and noise sources), we can rewrite the previous expression (Eq. 5.5)

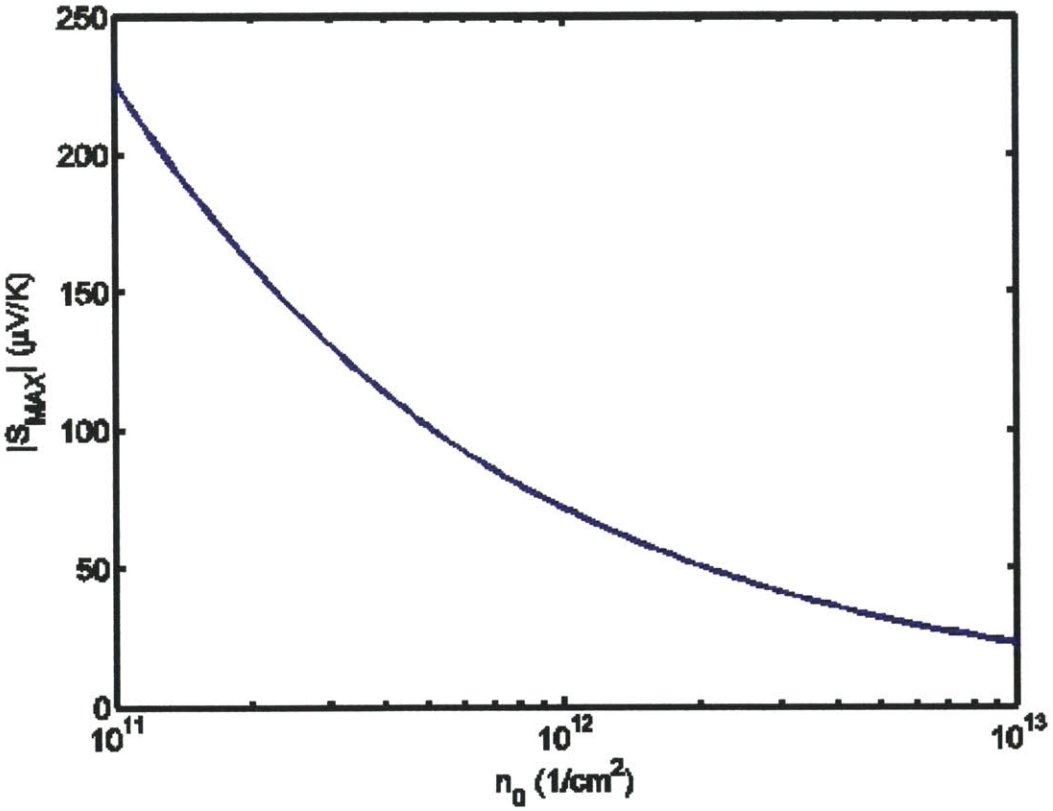

Figure 5-1: S_{MAX} as a function of n_0

$$D^*_{thermopile} = \frac{\epsilon S R_{th}}{\sqrt{1+\omega^2\tau_{th}^2}} \frac{\sqrt{N a_0 b_0}}{\sqrt{4 k_B T R_e \Delta f}}. \tag{5.5}$$

Unlike other types of detectors such as bolometers which require active biasing and thus contain 1/f noise, thermo-electric based detectors are often noise limited by Johnson noise. Due to the low voltage response of a single junction ($\sim \mu$V), typically many thermopile detectors are often placed in series to create a large array of thermopiles, which increase the signal by N; however, due to the limitation of Johnson noise, this also increases the amount of noise in the signal; however, for graphene the decrease in signal is only by $N^{1/2}$. Therefore overall, there is an increase in the net D* by only $\sqrt{N}$. Therefore, we express the electrical resistance (R_e) and Seebeck coefficient (S) as only one branch of a thermocouple. However, assuming similar geometries and thermal isolation of the devices, the only material dependent component of Equation 5.5 is just the Seebeck coefficient (S) and the resistivity (ρ_{sh}). Therefore, in figure 5-2, we plot the Seebeck coefficient versus resistivity for a variety of common thermo-electric materials.

Graphene, for a given resistivity (ρ_{sh}), has some potential advantages over other thermoelectric materials. Furthermore, in Figure 5-2, we plot both the positive and negative values of graphene's Seebeck coefficient to highlight the unique tunable dynamic range. This will be important later on in this chapter and when we will leverage some of graphene's other unique physical properties for some new applications. However, Figure 5-2 does show that while improvements in mobility do not make a large change in the overall Seebeck coefficient, they do have an important role in the conductivity or resistivity of graphene. Therefore, given these calculated values of Seebeck coefficient and sheet resistance, we can actually make some estimates for the achievable ranges of D*.

In order to estimate values for D*, we have to make some assumptions about the geometry of our detector (Figure 5-3). In an idealized thermal detector, we can assume a detector absorber area similar to before with a respective length and width of a_0 and b_0. Assuming perhaps applications for focal plane arrays, we assume the

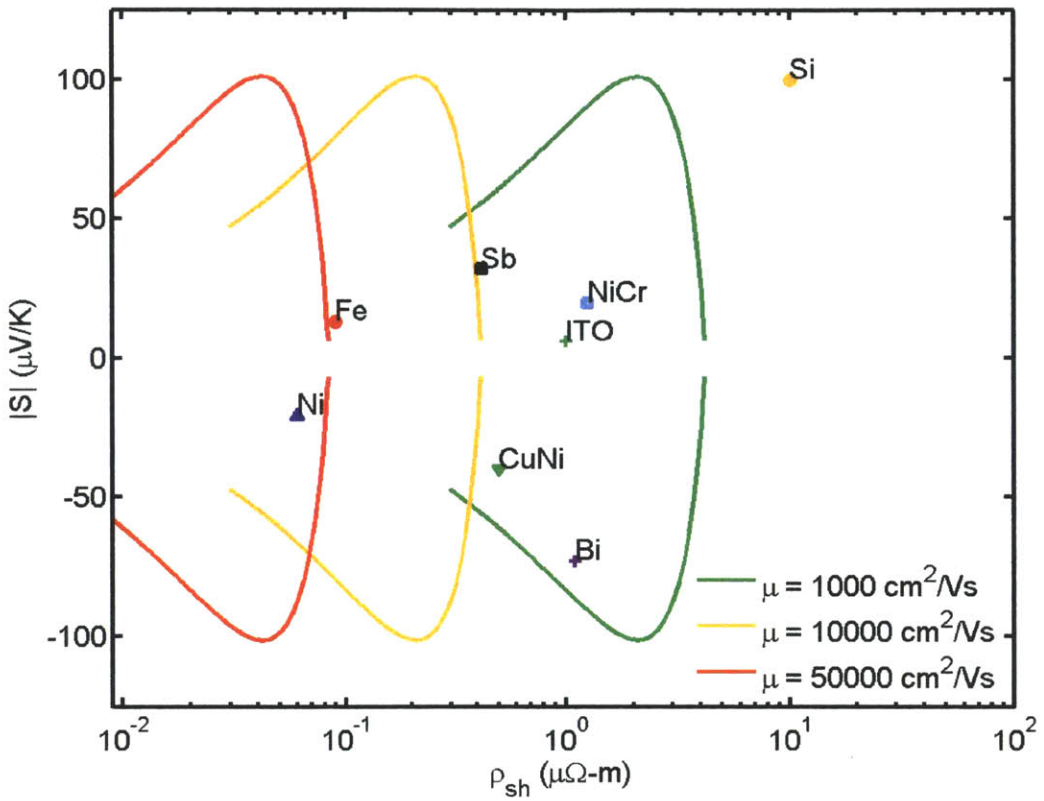

Figure 5-2: Comparison of Seebeck Coefficient of Various Thermoelectric Materials compared to Resistivity. The model assumed for graphene $n_0 = 5 \times 10^{-11}$ 1/cm^2

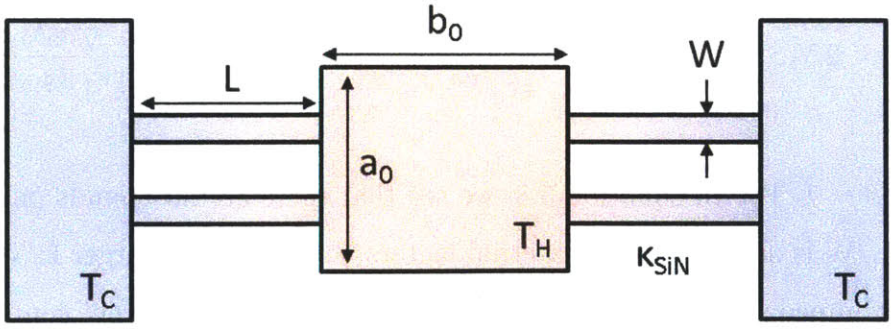

Figure 5-3: Schematic of ideal thermal detector

absorber geometry is an infrared pixel approximately 100 μm x 100 μm in length and width. We also assume that thermal the conduction is the dominant term in the thermal resistance (R_{th}):

$$R_{th} = \frac{L}{t_{SiN}\kappa_{SiN}W} \tag{5.6}$$

where L and W are the length and width of the thermal isolation legs, t_{SiN} is the thickness of the silicon nitride bridge, and κ_{SiN} is the thermal conductivity of the SiN. In addition, since electrical signals have to be wired on and off of the absorber region, we also assume that the electrical resistance of the device is dominated by the aspect ratio of the thermal isolation leads. In addition, we assume that we are able to lower the sheet resistance of the detector by increasing the number of layers of graphene (N_{layers}):

$$R_{sh} = \frac{1}{qn_s\mu}\frac{1}{N_{layers}}, \tag{5.7}$$

so we assume ω=0 in Equation 5.5. For a thermoelectric device, because the device requires a branch to go back and forth between the hot and cold zone, which affects the total thermal insulation, there need to be 2 leads for each electrical and thermal connection. We define N_j as the total number of junctions in the device and assume an emissivity of 1, so that the figure of merit of the thermopile is given by.

$$D^*_{thermopile} = 2N_jS\frac{L}{2N_j\kappa_{th}t_{SiN}W}\frac{\sqrt{a_0b_0}}{\sqrt{4k_BT2N_j\frac{R_{sh}}{N_{layers}}\frac{L}{W}}} = \frac{S(n_s)}{\sqrt{R_{sh}(n_s)}}\frac{\sqrt{a_0b_0}}{\kappa_{th}t_{SiN}}\sqrt{\frac{N_{layers}\beta}{8k_BTN_j}} \tag{5.8}$$

where $\beta = L/W$. In equation 5.8, we see that there are no bounds on L/W, and therefore L/W is determined by external factors; for example, a larger L/W increases the output impedance of the device such that it does not effectively couple into the input stage of an amplifier or L/W is limited by mechanical issues or by the layout area of the device. We have also assumed that one is able to dope multiple sheets of graphene to help reduce the overall sheet resistance. Finally, we also make the

Parameter	Value
κ_{th} ($Wm^{-1}K^{-1}$)	8-12
N_j	1
t_{SiN} (nm)	250
N_{layers}	1
a_0 (μm)	100
b_0 (μm)	100
β	5
c_{SiN} ($Jg^{-1}K^{-1}$)	0.17
ρ_{SiN} (kg/m^3)	2500

Table 5.1: Estimated parameters for D*.

approximation that $t_{SiN}/\kappa_{th} \gg N_{layers}t_G/\kappa_{G,th}$ such that we do not have to consider the thermo-electric material thermally shorting the device. The parameters that we used for calculating D* are presented in Table 5.1 where we utilize SiN as our supporting material layer.

Utilizing our calculations from Figure 5-2 and Equation 5.8, we plot our calculated D* as a function of carrier concentration (Fig. 5-4). Interestingly enough, even though the sheet resistance and the Seebeck coefficient are both functions of carrier concentration, the product of $S/\sqrt{R_{sh}}$ actually results in a constant value determined only by mobility (Eq. 5.10)

$$\frac{S}{\sqrt{R_{sh}}} = \frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{2}{\hbar v_f \sqrt{\pi}}\frac{-n_s^{3/2}}{n_s^2 + n_0^2} \times \left[q\mu\sqrt{n_s^2 + n_0^2}\right]^{1/2} \tag{5.9}$$

$$\frac{S}{\sqrt{R_{sh}}} = \frac{\pi^2}{3}\frac{k_B^2 T}{q}\frac{2\sqrt{q\mu}}{\hbar v_f \sqrt{\pi}}, n_s >> n_0. \tag{5.10}$$

In addition to calculating D*, we also calculated the thermal capacitance (C_{th}) in Equation 5.11.

$$C_{th} = c_{SiN}\rho_{SiN}a_0 b_0 t_{SiN} \tag{5.11}$$

where c_{SiN} is the specific heat of silicon nitride, and C_{th} is calculated from the values from Table 5.1 yielding $C_{th} = 2.656 \times 10^{-10}$ (J/K) and a corresponding $\tau_{th} = 1.06$ ms.

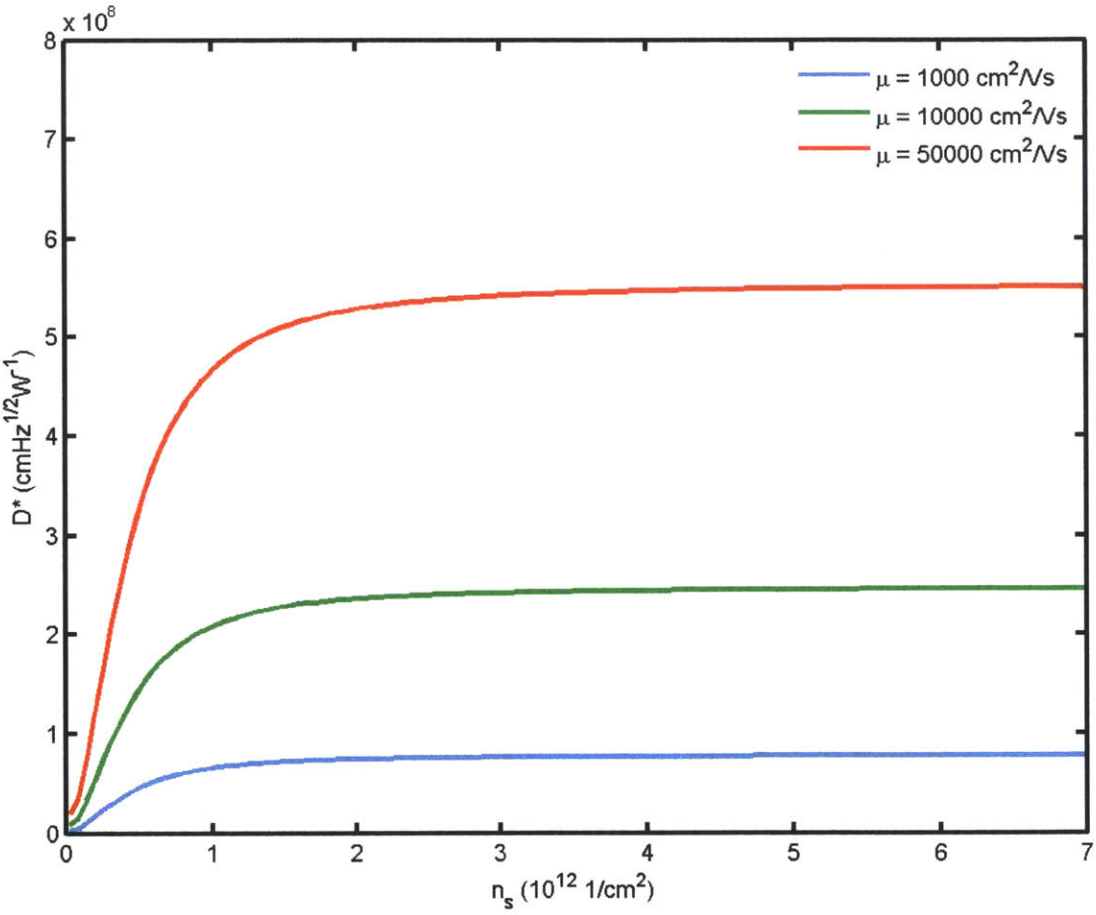

Figure 5-4: D* as a function of n_s assuming various mobilities

Figure 5-4 shows that for graphene, detection levels similar to other thermopile materials and even standard bolometer structures can be achieved when only a single sheet of graphene and appropriate thermal isolation are utilized. While this device may not, as of yet, be at the same performance level as conventional micro-bolometers (a-Si and VOx), the self-powered signal from thermopile sensors has intrinsic advantages for radiometry and other consumer and industrial applications where passive sensors or calibrated sensors are required [174, 208]. The simplicity of the device and fabrication may also tend to make it an attractive low-cost thermopile based material for large area applications, where scanning many large arrays of bolometers may not be as efficient as a self-powered thermo-electric. Furthermore, the integration aspects of CVD graphene and compatibility with roll to roll process may suggest a low cost stamping method for creating thermally isolated devices. Therefore motivated by these performance metrics, the following section mainly explores the potential applications for graphene-based thermal sensors. The first demonstration is the development of a graphene integrated microelectronic electrical mechanical system (MEMS).

5.2 Micro-electrical-mechanical Graphene Thermopile

Understanding that graphene-based infrared detection relies on thermal effects, we re-examine our original device structure in Chapter 4. In the previous experiments, the silicon substrate that the device is sitting on acts as a heat sink, which drastically reduces the T_{hot} at the junction since most of the heat generated by the laser is transported to the substrate. This heat loss mechanism is the predominate reason that the measured responsivities were only ($\sim$ mV/W). Therefore, to alleviate this problem, the process flow for the original device structure was modified to include additional etch release steps in order to construct a thermally suspended bridge structure. Figure 5-5 shows the new process flow for fabrication.

(1) Starting with a bare silicon wafer, we deposit a dielectric stack by high frequency plasma-enhanced (PE) CVD of 80 nm SiO_2/ 500 nm SiN/80 nm SiO_2. This serves as our starting substrate with the SiO_2 chosen as a protective cap for the SiN

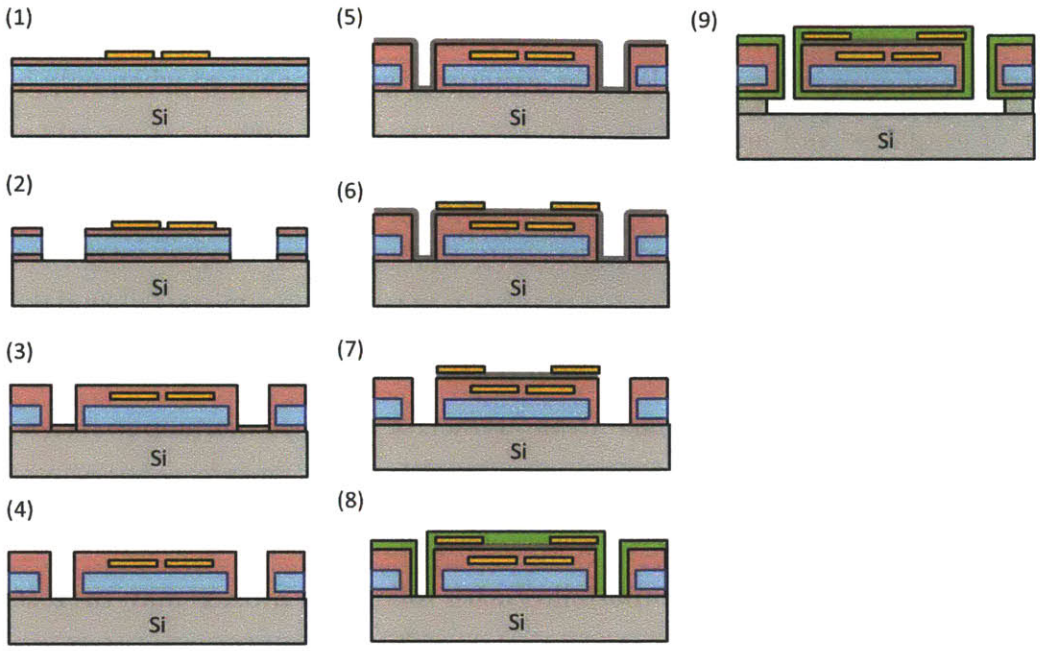

Figure 5-5: MEMS Device Process Flow, blue - represents the SiN, red is silicon dioxide, orange are ohmic pads, gray - graphene sheet, green is XeF_2 passivation.

to protect it during our XeF_2 silicon release process (Step 9). The SiN deposited by PE-CVD is not fully densified, which is both good and bad. The lack of densification leaves the SiN chemically reactive with XeF_2; however, this also implies a lower thermal conductivity. Gate electrodes are also patterned by ebeam-lithography. (2) Release vias are cut through the entire dielectric stack exposing the underlying silicon substrate. To reduce plasma etching time on the structure, the etch vias are exposed to a short buffered oxide etch (BOE) to help thin down the membrane structure. This process was chosen to deliver more flexibility due to poor photoresist selectivity in our dielectric plasma etch recipe. (3) The entire structure is then recoated with another layer of PE-CVD SiO_2 $\sim$80 nm thick, that serves as a gate dielectric as well as a sidewall coating for the SiN. (4) An additional etch is performed to selectively etch away the underlying silicon to re-expose the silicon underneath. (5) Graphene is then transferred onto the chips. Due to the rough topology, some regions of the graphene can delaminate; however, most of the graphene that tears is located near the exposed silicon regions. (6) Ohmic metals are patterned by ebeam-lithography (1 nm Ti/ 30

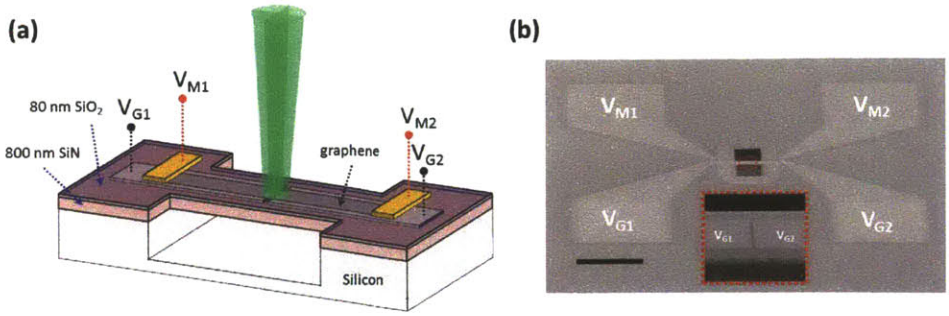

Figure 5-6: MEMS Diagram of Completed Membrane Structure. (a) Diagram and electrical schematic of device (b) SEM of device structure. Scale bar is 100 μm, inset shows a zoomed in region of the membrane

nm Au). (7) Reactive oxygen etching and a PMMA hard mask are used for electrical isolation. (8) As a passivation layer to protect the graphene from the XeF_2, PMMA is spun onto the sample and then rexposed for the etch vias for suspension. This PMMA slightly dopes the graphene, but it does not appear to significantly degrade the electrical properties. (9) Finally the chip is exposed to XeF_2 for 2 cycles for 30s each to undercut the membrane bridge.

Figure 5-6(a) shows the schematic of the device structure and Figure 5-6 (b) shows an SEM image of the completed device after suspension. The inset in Figure 5-6 (b) shows a zoomed-in image of the suspended bridge structure and the two embedded electro-static gates.

We characterized our devices in a similar fashion, as described previously in Chapter 4, measuring both the resistance of the device (Fig. 5-7 (a)) as well as the photovoltage response of the device (Fig. 5-7 (b)). However, unlike previous measurements, the measured responsivity is now $\sim$ 1 V/W as compared to our original responsivity of $\sim$ mV/W. Therefore simply by thermally engineering the substrate, we are indeed able to enhance the responsivity of this device by almost 3 orders of magnitude. Using our measured responsivity at 10.6 μm, we can estimate the potential D* of this device in Equation 5.12:

$$D^*_{thermopile} = \frac{R\sqrt{a_0 b_0 \Delta f}}{\sqrt{4k_B T R_e \Delta f}} = \frac{R\sqrt{a_0 b_0}}{4k_B T R_e} \tag{5.12}$$

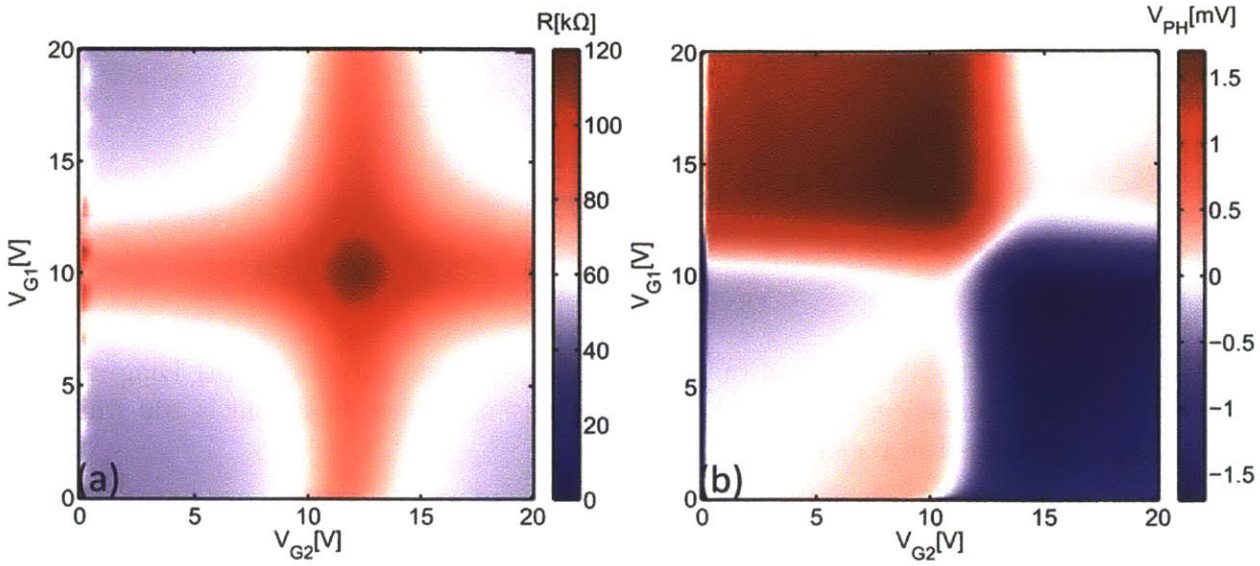

Figure 5-7: Electrical and Optical Characterization of MEMS device (a) IV measurement utilizing $V_{M1-M2} = 25\mu V$ (b) measured photovoltage response. Input laser power was 1.6 mW. All measurements taken at 300 K

so that the responsivity (R) is approximately 1 V/W at 10.6 μm. The area of the device is 16 μm by 30 μm in size. The resistance (R_e) of our device is approximately 50 kΩ. This results in a calculated $D^* = 7.6 \times 10^4$ cmHz$^{1/2}$W^{-1}, whereas the ideal calculated from Equation 5.8 is $D^* = 1.32 \times 10^6$ cmHz$^{1/2}$W^{-1}. The lower value of D* is due to a couple of factors. The largest effect in our device is the fact that the incident power on the device is not fully absorbed. This can be seen from the device structure. For electrostatic gating of our graphene device, the location of the incident absorbed power is mainly in the PE-CVD SiO_2 gate dielectric. To quantify this, we measured the infrared optical transmission spectra through various layers of material. The measured transmission through 10 nm Ti/20 nm Pt is essentially zero across the entire infrared spectrum. Therefore, this implies that some of the incident light is absorbed by the metal gates; however, most of the incident light is actually reflected back through the SiO_2 gate dielectric. To estimate the fraction of absorbed light in the Ti/Pt electrode, we can compute the complex reflectivity of Pt at 10.6 μm. The real (n_R) and imaginary (n_I) part of the refractive index of Pt is 11.13154 and 39.670, respectively [205]. Utilizing Equation 5.13, we can compute the magnitude of

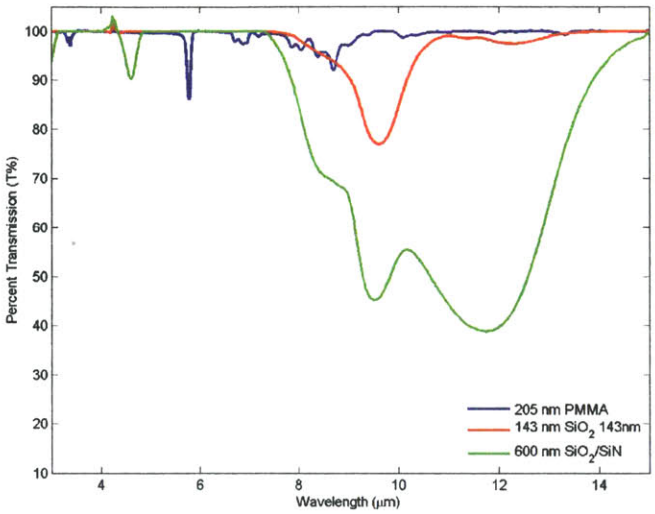

Figure 5-8: IR transmission of various device materials: PMMA, PE-CVD SiO_2, Substrate Material (PE-CVD SiO_2/SiN/SiO_2).

Layers	Percent Absorption
10 nm Ti/ 20 nm Pt	2.6 %
143 nm SiO_2	2.5 %
205 nm PMMA	0.23 %
Total	5.33 %

Table 5.2: Optical Absorption at $\lambda = 10.6$ μm

the reflectivity of the gate electrodes.

$$R = \frac{(1 - n_R)^2 + n_I^2}{(1 + n_R)^2 + n_I^2} = 97.4 \tag{5.13}$$

Therefore, only 2.6% of the incident laser light is absorbed by the metal. The rest must be reflected and then absorbed by the SiO_2 and PMMA coating on top. Therefore, we measured, using a Fourier Transform Infrared Spectrometer (FTIR), the percent transmission of infrared light for various thickness of materials including the PMMA coating, the PE-CVD SiO_2 and the substrate PE-CVD SiO_2/SiN/SiO_2 (Fig. 5-8).

Table 5.2 shows the measured optical absorption for each of the different layers. At λ=10.6 μm, we are only absorbing approximately 5% of the incident light in our MEMS device, suggesting that potentially, much larger responsivities are achievable

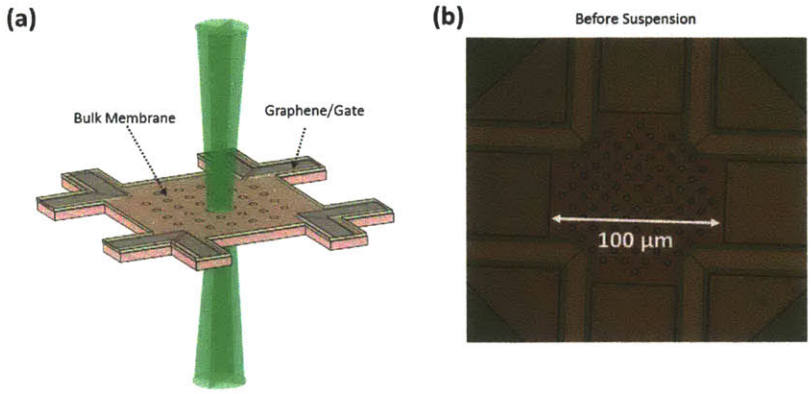

Figure 5-9: MEMS Graphene Thermopile before suspension(a) Schematic of MEMS device version 2 (b)Optical Micrograph of fabricated device before suspension

with proper optical absorption. Therefore, while we have addressed the fundamental issue of thermal isolation, there is still much to be done to improve the optical absorption of our devices. This could be accomplished through the inclusion of carbon nanotubes, carbon black, optical cavities, etc. For simplicity, we chose to redesign the device structure in order to utilize the inherent substrate underneath, which has a much larger and broader infrared absorption (Fig. 5-8).

5.2.1 MEMS Graphene Thermopile version 2

Therefore, we modified the device layout of the MEMS device, as shown in Figure 5-9 (a). The gates are placed at the periphery, leaving the center of the substrate SiN open as a passive absorber. In addition, this structure can be combined with other approaches, such as (1) deposition of amorphous carbon or (2) utilizing a back optical cavity between the SiN and the substrate. With only a change in layout, MEMS devices were fabricated identical to the process flow listed in Figure 5-5. Figure 5-9 (b) shows the device structure before suspension. The center absorber area in Fig. 5-9(b) is 100 μm by 100 μm. Figure 5-10 shows optical microscope and SEM images of the device after suspension.

Unfortunately, due to the larger dimensions and sizes of these structures, the device is more sensitive to internal process-induced stresses than before. Figure 5-11

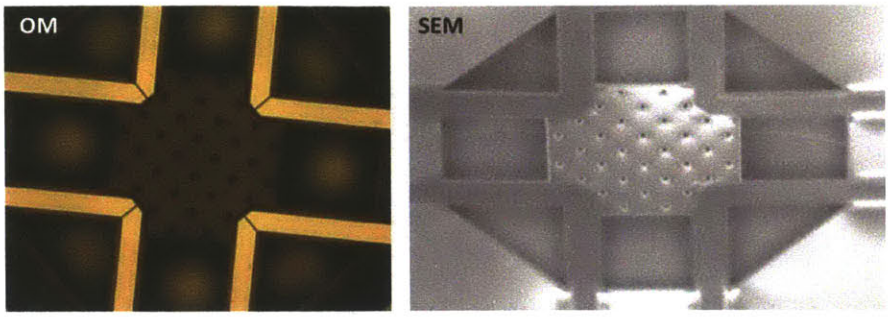

Figure 5-10: MEMS Graphene Thermopile after suspension (a) Optical Micrograph of fabricated device after suspension (b) SEM of completely suspended device

shows an SEM of the devices and failure mechanisms due to the excessive tensile strain. Utilizing the KLA-Filmetrics to measure stress on the starting wafers, we quantify the amount of tensile stress in our SiN at 605 MPa Tensile Stress. This stress we found to be too great resulting in a large fraction of post release failures. Therefore, we reduced the total amount of stress in the film by utilizing a mixed frequency (HF + LF) PE-CVD deposition RF to reduce the total intrinsic stress down to 29.61 MPa, which we found to greatly improve our yield after release.

Figure 5-12 shows measured data from these new batches of devices including varying the optical chopping frequency to measure the time constant of this device, which is approximately 47 ms. Further device characterization is still underway with our collaborators from the Army Research Labs for a more detailed characterization of D*. However, as measurements for D* are still ongoing, estimations can still be made about graphene-based thermopiles for standoff thermal imaging. A new figure of merit is necessary in order to take into account the entire imaging system (Figure 5-13): noise equivalent temperature difference (NETD), which represents the smallest detectable change in far-field blackbody temperature that one can measure.

5.2.2 NETD Estimation

Figure 5-13 shows an array of detectors (left); each imaging the far field through an imaging lens with an area of A_0 and the object of interest has a temperature of T_B. To derive the NETD value, we first compute the difference in emitted optical power as a

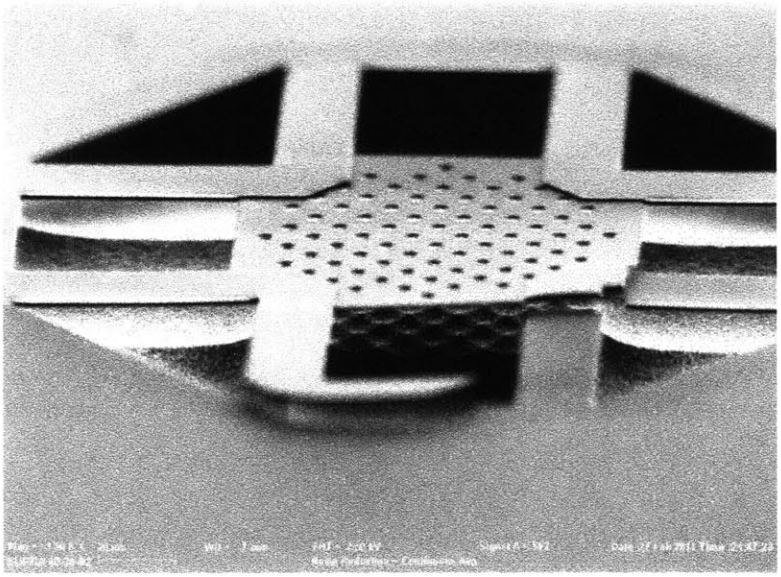

Figure 5-11: MEMS Graphene Thermopile - SEM of failed devices due to stress and cracking

blackbody emitter changes temperature, which comes from differentiating Equation 4.1

$$\frac{dW(\lambda,T)}{dT} = W(\lambda,T)\frac{c_2 e^{\frac{c_2}{\lambda T}}}{\lambda T^2\left(e^{\frac{c_2}{\lambda T}}-1\right)} \cong \frac{c_2}{\lambda T^2}W(\lambda,T) \tag{5.14}$$

This change in blackbody emitted power (dW) is due to a small change in blackbody temperature (dT). The quantity in Eq. 5.14 c_2 is equal to 1.4388×10^4 (μm °K). Therefore, given the sensitivity of the device to small changes in power, we can express NETD in equation 5.15.

$$NETD = \frac{\pi f^2\sqrt{a_0 b_0 \Delta f}}{A_0 a_0 b_0}\frac{1}{\int_0^\infty D^*(\lambda)\tau_0(\lambda)\frac{\partial W_\lambda(\lambda,T)}{\lambda T}d\lambda} \tag{5.15}$$

where A_0 is the size of the lens, f is the focal distance of the lens, τ_0 is the transmission coefficient of the optics and system. This figure of merit thus becomes more important when quantifying the entire system, as opposed to quantifying only the intrinsic detectivity.

So previously, we estimated D*; however, this was measured at a specific wave-

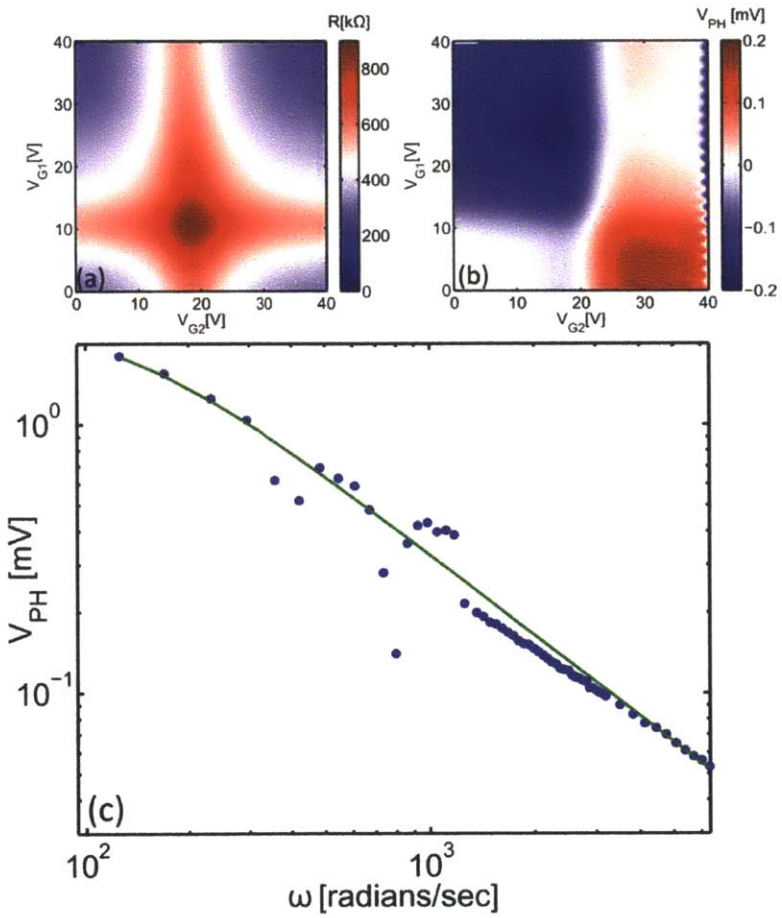

Figure 5-12: MEMS Graphene Thermopile - (a) resistance measurement as a function of V_{G1} and V_{G2} with 25μV excitation. (b) Responsivity Map of the device in (a) utilizing $P_{in} = 0.28$ mW. (c)Response of device in (a,b) as a function of modulation frequency (ω - radians/sec)

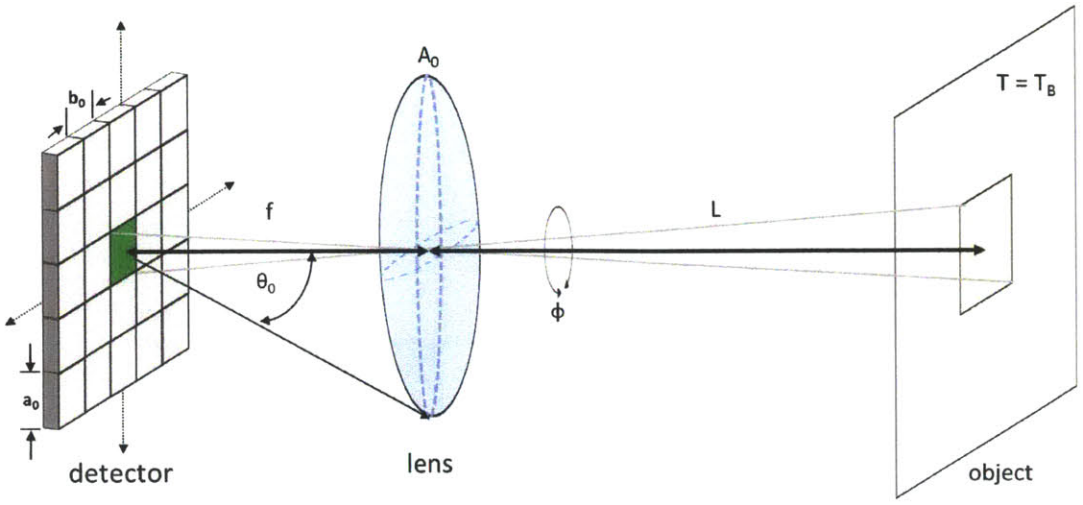

Figure 5-13: Diagram of Basic Thermal Imaging System

length 10.6 μm, for a device which only absorbed 5.33 % of the incident light. Therefore, to avoid any double counting of the optical absorption, we computed D* assuming 100% absorption, which is equal to 2.6×10^7 cmHz$^{1/2}$W^{-1}. Therefore, in our expression for NETD, we take into account optical absorption through τ_0. At the same time, we could define D* as a function of wavelength initially and then take τ_0 as the transmission only through the optics, as opposed to taking into account the absorption of the material. Utilizing this definition of NETD and Equation 5.15, we compute the NETD assuming various optical substrates as well as graphene quality. Table 5.4 shows the computed NETD for (1) PE-CVD SiO_2 and Ti/Pt (2) PE-CVD SiO_2/SiN/SiO_2 (3) Carbon black. In addition, we have also computed NETD assuming the ideal calculated D* (1.0×10^8 cmHz$^{1/2}$W^{-1}) from Figure 5-4 assuming approximately μ =1000-5000 cm^{2}V^{-1}s^{-1}. In conclusion, even with our existing structures, it appears promising that these MEMS-based devices can be used for standoff thermal imaging. Experiments are currently underway to demonstrate this with a single MEMS-based pixel.

Focal Length (f)	25.4 mm
Lens Diameter (d_0)	25.4 mm
Detector Width (a_0)	100 μm
Detector Length (a_0)	100 μm
Bandwidth (Δf)	60 Hz

Table 5.3: Assumed Optical and System Imaging Parameters for the device in Fig. 5-13

NETD (K)	PECVD SiO_2/TiPt	PECVD SiO_2/SiN/SiO_2	Carbon Black or 100 % absorption
D* = 2.6×10^7 cmHz$^{1/2}$W^{-1}	6.88	1.00	0.21
D* = 1.0×10^8 cmHz$^{1/2}$W^{-1}	1.79	0.26	0.055

Table 5.4: Computed NETD due to various optically absorptive substrates. In addition, we have also computed NETD assuming the ideal calculated D* from Figure 5-4 assuming approximately μ =1000-5000 cm^{2}V^{-1}s^{-1}.

5.3 Graphene-CMOS Monolithic Integration

Given the growing development of graphene-based electronic and opto-electronic devices, these materials provide new materials capabilities to our existing toolbox of electronic devices; however, due to the overwhelming technology and history with silicon, we believe graphene-based sensors may serve better as a complementary technology. Unfortunately, due to the weak adhesion between CVD graphene and the underlying substrate, as seen in Chapter 3, we believe that a front end of the line process may not be the best way to integrate graphene since the graphene would then be a mechanical weak spot. In addition, graphene's amazing transport properties require special encapsulation to properly preserve its high quality transport. Therefore, we developed a back end of the line (BEOL) process, integrating our graphene thermal sensors with a commercially available CMOS chip fabricated by TSMC. The chip design/ testing was done in collaboration with Sung Jae Ha. The device processing is discussed in this section.

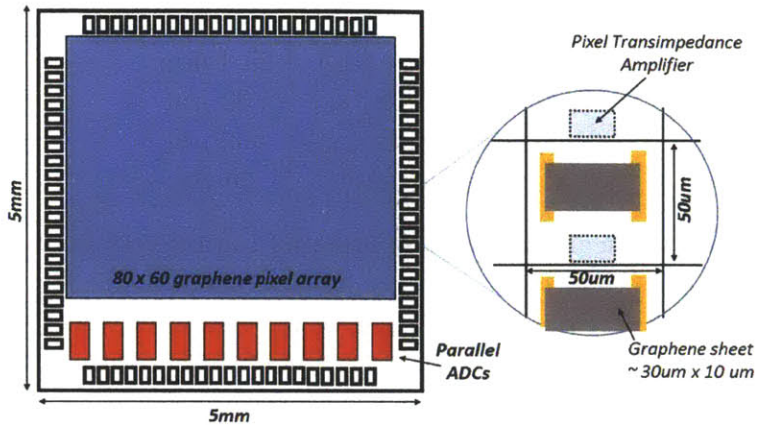

Figure 5-14: Diagram of CMOS chip and graphene devices

5.3.1 Device Concept

As a test for thermal signatures, we designed a read-out chip fabricated from TSMC's 180nm process line, with a 60 $\times$ 80 graphene device array monolithically integrated onto a TSMC chip (Fig. 5-14). Each pixel is read through a series of multiplexors (MUX) where each row (Row Select - RS) and column (Column Select - CS) are chosen and then transmitted to an Successive Approximation Register (SAR) analog-to-digital converter (ADC) for readout from the chip (Fig. 5-15). An optical micrograph of the chip is shown in Fig. 5-15. The graphene-based device structure for the first iteration of processing was identical to the MEMS device (Fig. 5-6) excluding the substrate release step. This was chosen to simplify device processing to a bare minimum for process development purposes.

5.3.2 Device Processing

The graphene device area is shown in Figure 5-16 after a blanket passivation removal by CF_4 plasma to expose the top metal (M6) layer. Due to design rules imposed by TSMC, dummy metal structures are included. Unfortunately, the chip, as received, was not planarized as shown in Figure 5-16 (b), which corresponds to an AFM scan across one of the Ohmic Vias (white dotted line in Figure 5-16 (a)). Therefore, the total peak to valley roughness is approximately 1.25 μm. This lack of planarization,

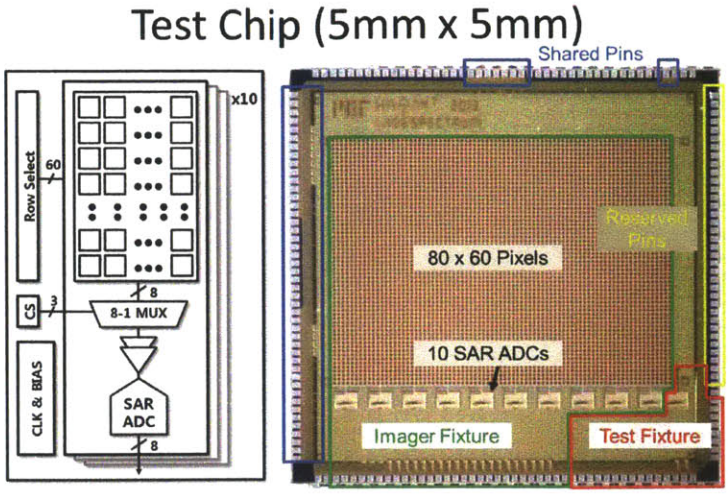

Figure 5-15: Block level diagram (right) of the read out chip including the pixel select blocks (Row Select and Column Select (CS)) for multiplexing signals (MUX) to the SAR ADC. Clock (CLK) and Bias signals are also shown. Optical micrograph of chip (left) and circuit placement

unfortunately, complicates our integration process, as we will discuss later in this section; many issues related to photoresist, metallization, and graphene transfer are complicated by this non-planar topology. In addition, the chips, as received, were only 5 mm x 5 mm in size. Due to the small size, conventional planarization techniques such as chemical mechanical planarization (CMP) were difficult to utilize on such a small piece. Attempts were made to utilizing a standard TEM sample prep from Southbay Technologies - however the equipment, made available at MIT, did not have the proper wedge compensation to allow for perfectly planar polishing. Also due to the small size of the chip, polymer planarization techniques utilizing polyimide (PI) proved to be potentially hazardous to the chip, due to the required high temperature mechanical curing of the polymer ($T_{cure} > 300$ °C) for 1-2 Hours. The thermal budget for the chip was also not clearly presented by TSMC; therefore, we choose to limit our processing mainly to low temperatures (<250 °C).

The final process flow that appeared to satisfy all of these constraints is shown in Figure 5-17. The process flow starts with a (1-2) blanket passivation etch to remove the top passivation to expose the ohmic vias underneath. (3) This is followed

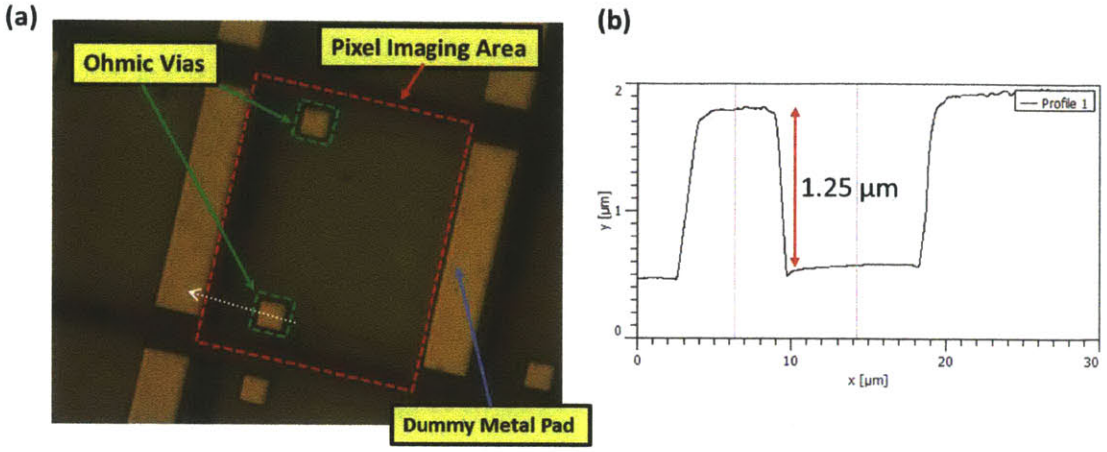

Figure 5-16: Graphene Pixel Area (a) Optical micrograph of pixel area. Red dotted line represents the area for the graphene device, dummy metal represents dummy metal fill imposed by TSMC, ohmic vias connect directly to the underlying trans-impedance amplifier (b) AFM of dotted white line in (a) to show that the ohmic vias stick out of plane

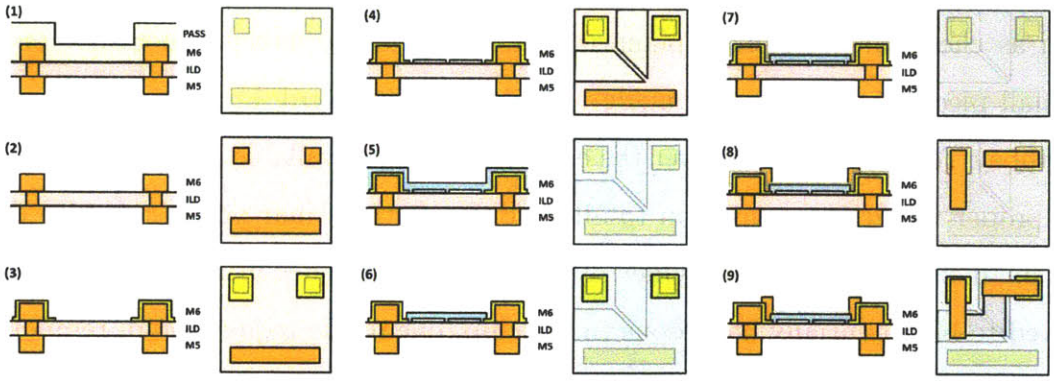

Figure 5-17: Process Flow for Graphene Integration. PASS = passivation, ILD = interlayer dielectric, M6 = Metal 6 (Cu), M5 = Metal 5 (Cu), blue = PECVD SiO_2, grey line is graphene. The left and right images are the side and top view of the pixel area, respectively

by an ohmic metallization to contact the metal on the flat regions of the pixel for eventual graphene contact. (4) Ti/Pt electrodes are then deposited by electron beam evaporation. (5) This is then covered by a 70 nm layer of PE-CVD SiO_2, which serves as our gate dielectric. (6) Etch vias into the gate dielectric are then patterned to expose the underlying metal pads and (7) graphene is then transferred on top of the chip. (8) Ohmic connections to the graphene are defined by e-beam lithography and (9) graphene is then electrically isolated by mesa isolation utilizing Reactive Oxygen Etching.

While the final process flow appears relatively straight-forward, there were a couple of issues that required some further investigation: (1) Resist Uniformity (2) Ohmic Metallization and (3) Graphene Transfer.

Resist Non-uniformity

Due to the small chip size and non planar features, we were also limited to electon-beam lithography for all of our processing steps. However, due to the rough topology of the surface, much thicker ebeam resists were necessary, as shown in Figure 5-18. The PMMA resist is almost 63% thinner on top of the metal structures than in the graphene pixel region. Therefore, depending on the processing steps (Lift-off versus Etching), layout of the structures differed depending on whether the pattern was on top of a protrusion or in the flatter region.

Ohmic Metallization

Due to the non-planar substrate, ohmic metallization was also more difficult than in previous devices. Standard lift-off requires utilizing a directional metal evaporation, which forms a discontinuous metal film across large step heights (>200 nm), to enable solvent to "lift-off" the polymer/metal stack. The discontinuity in the metal films is due to the shadowing effects caused by the directional electron-beam evaporation. Therefore, instead of electron-beam evaporation, we focused on sputtered ohmic metal films, which, due to the higher pressure of deposition, are usually conformal. Unfortunately, while we desire conformal metal depositions to enable good step coverage,

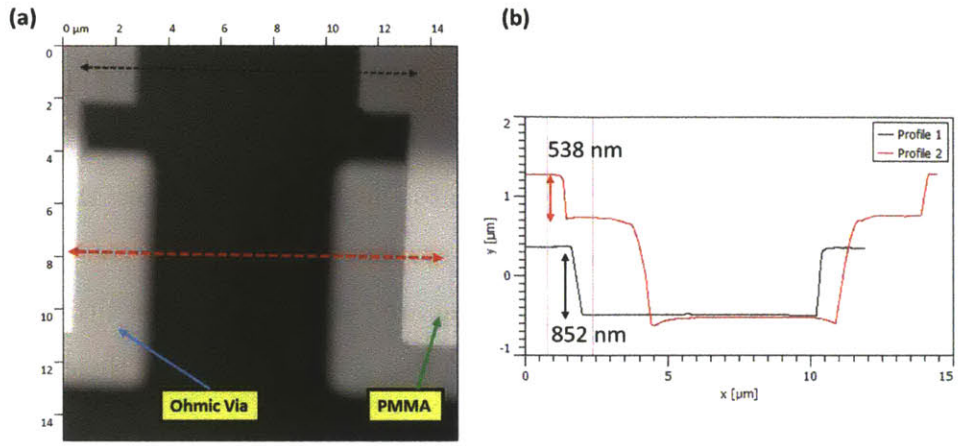

Figure 5-18: Resist Non-uniformity of PMMA when spinning and exposing PMMA on the surface. (a) AFM scan region of 15 μm x 15 μm (b) Line Cuts of AFM scan red line cut corresponds to across the metal layer, while the black line cut is in the flat region of the pixel.

this also complicated matters when performing lift-off. Therefore, initially we tried to directly sputter a conformal layer of metal onto the entire chip surface and then dry etch the metal using maN-2403 e-beam resist as an etch mask (see Fig. 5-19).

The top metal contact metal (Ti/Au) was chosen to avoid issues such as oxidation after deposition. Unfortunately, there are only a few plasma etch technologies that are capable of etching Ti/Au. The most common one is direct ion milling using Argon, which has been proven to be highly selective between photoresist and gold. Work on ion milling was done in collaboration with Matt Chin at Army Research Labs (ARL) with the assistance of their 4wave ion mill. After ion milling, the method appears to work; however, as mentioned before, the thickness variation of the resist after spinning led to a thinning of the resist mask at the top of the ohmic vias and dummy metals, causing metal erosion (Figure 5-20). In addition, after ion milling, the photoresist left behind was very difficult to completely remove. Even after long exposure to oxygen plasma (>2 Hr), residue on top of the metal remained. Due to the ion bombardment and thermal management, there were some issues of bubbling of the maN-2043 resist that led to pinhole defects and rough metal surfaces after processing.

Therefore, we began searching for another alternative and investigating a sput-

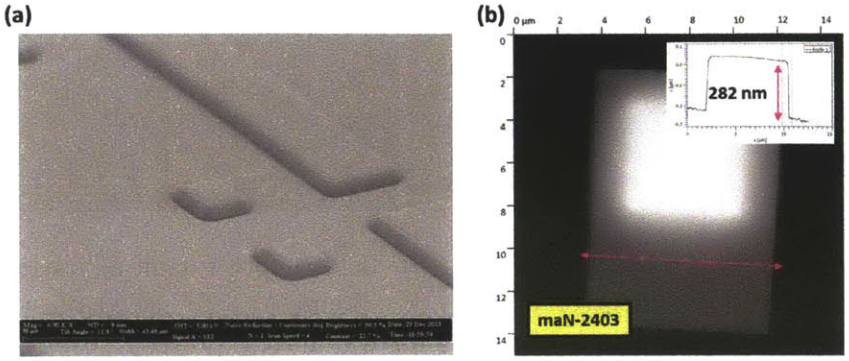

Figure 5-19: Direct Sputtering of Metal (a) SEM of the structures after metal sputtering (b) AFM of the maN-2403 resist after exposure and development.

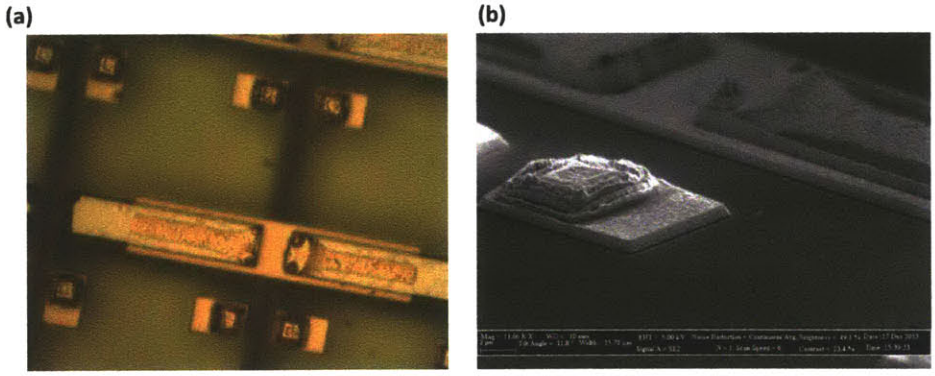

Figure 5-20: Ion Milling (a) Optical micrographs of the Ti/Au after ion milling. (b) SEM of the structures in (a) after ion milling. Notice that the metal layers on top appear to have been etched through due to poor step coverage of the resist.

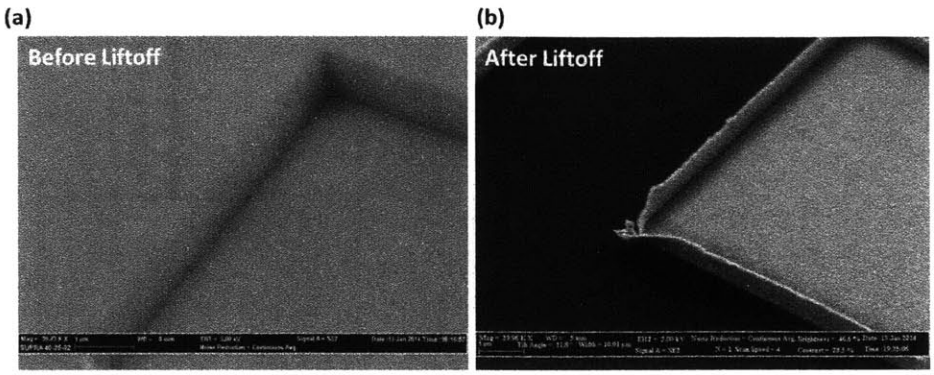

Figure 5-21: Sputtered Liftoff - PMMA (a) SEM before lift-off of patterned e-beam resist and sputtered metal layer (10 nm Ti/ 30nm Au) (b) SEM of structure after performing lift-off (ultrasonic in Acetone for 2 minutes, power = 6). Note the fence structure surrounding the feature caused by the conformal deposition of metal along the side walls of the lift-off resist.

tered lift-off process. The sputtering process, due to the higher base pressures, is a conformal process, as shown in Figure 5-21. As expected, the metal deposition from sputtering is too conformal to do a direct liftoff from a single layer of resist, as seen by the fence structures in Figure 5-21 (b). To adjust for this, we utilized a bilayer resist process of MMA and PMMA to ensure a very deep undercut (<1 μm). Utilizing a deep undercut provided by the bilayer process, we are able to form a discontinuity in the deposited metal as shown in Figure 5-22 (a). Unfortunately, this does mean that the patterns that we constructed have a much larger profile then as originally defined by the lithography (approximately 1.5 μm larger on both sides), but at least this provides us with a conformal metal coverage for thin metal stacks $\sim$ 100-200 nm of metal. Therefore, this sputtered lift-off process was the final process that we used in step (3) of our process flow (Fig 5-17).

Graphene Transfer

The last integration issue, with this non-planar chip, was the graphene itself (done with the assistance of Yong Cheol Shin). Unfortunately, due to the density of features (dummy metals and ohmic vias), tenting of the transferred graphene films can often occur as it is suspended above the surface. However, if the graphene did not make

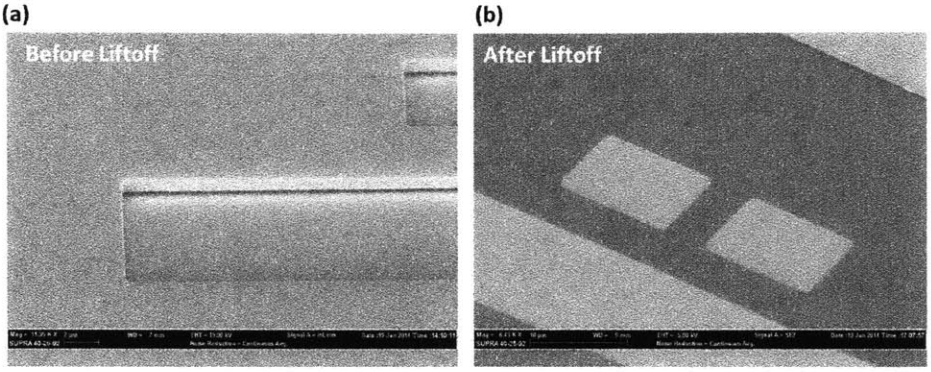

Figure 5-22: Sputtered Liftoff - MMA/PMMA (a) SEM before lift-off of patterned MMA/PMMA e-beam resist after sputtered metal layer (10 nm Ti/ 30 nm Au) (b) SEM of structure after performing liftoff (ultrasonic in Acetone for 2 minutes, power = 6). Note there is a small plateau effect that changes the patterned geometry slightly due to sputtered material underneath the undercut.

contact with the underlying substrate before solvent treatment, the graphene did not adhere correctly (Fig 5-23 (a)). Therefore, we found that softening and re-flowing of the PMMA is a necessary step to ensure proper adhesion between the graphene and the substrate (Fig 5-23 (b)). Traditionally, we think of graphene as being extremely flexible; however, given the support layer of PMMA (~200-400 nm), graphene is mechanically confined by the PMMA. Therefore, we added in a PMMA reflow step (T > 130 °C) since the glass transition temperature (T_{glass}) of PMMA is around 120-130 °C. This reflow step allows the graphene/PMMA stack to relax and adhere to the underlying substrate. Unfortunately, even with this step, there is still a small amount of tenting near closely spaced protrusions (Fig. 5-23 (b)); however, a sufficient coverage of graphene is transferred onto the chip for device processing. While other techniques, such as thermal decomposition of PMMA under a forming gas environment are possible for both removal and relaxation of the PMMA, we wanted to avoid any high-temperature processing so as to ensure compatibility with the underlying silicon chip. In the current scheme, the entire transfer process only undergoes a maximum temperature of 150°C and exposure to acetone.

Therefore after resolving the issues outlined above, we were able to monolithically integrate our graphene devices with the foundry fabricated CMOS chip. Figure 5-24

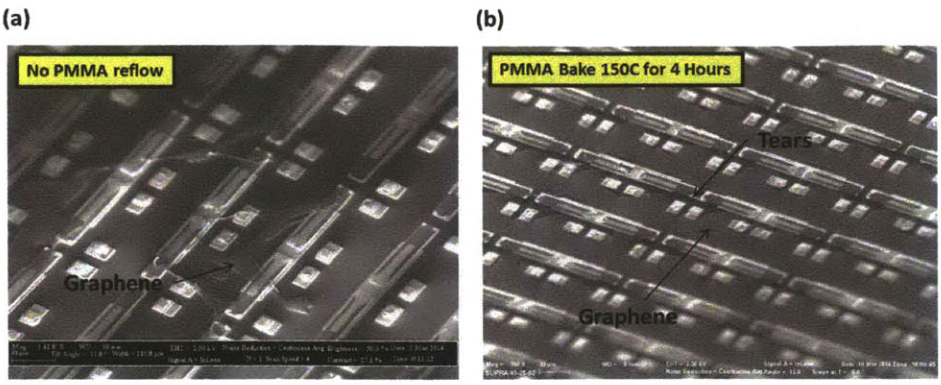

Figure 5-23: Graphene Transfer onto CMOS chip (a) SEM of Graphene transferred onto the chip with only blow drying and no thermal reflow step (b)SEM of Graphene transferred onto the chip after PMMA softening at 150 °C for 4 hours.

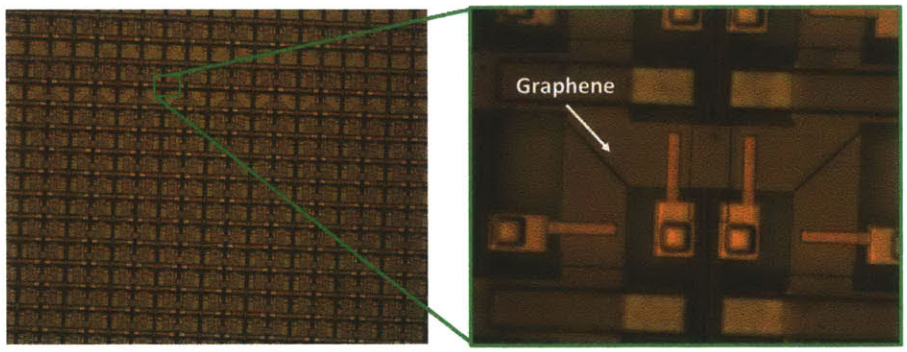

Figure 5-24: Optical Micrgraphs of completed graphene-CMOS integration.

shows the completed process, including graphene ohmic contacts and mesa integration.

5.3.3 SPICE Modelling

Currently, device testing after processing is still ongoing; however simultaneously, we have also begun developing a basic SPICE (Simulation Program with Integrated Circuit Emphasis) model for the graphene thermocouple element utilizing the basic equations that we have shown earlier in this chapter for circuit level simulations. Figure 5-25 shows the basic circuit level model for the graphene based thermocouple. We model the input temperature (DT) as an input voltage (1V = 1K) through an RC

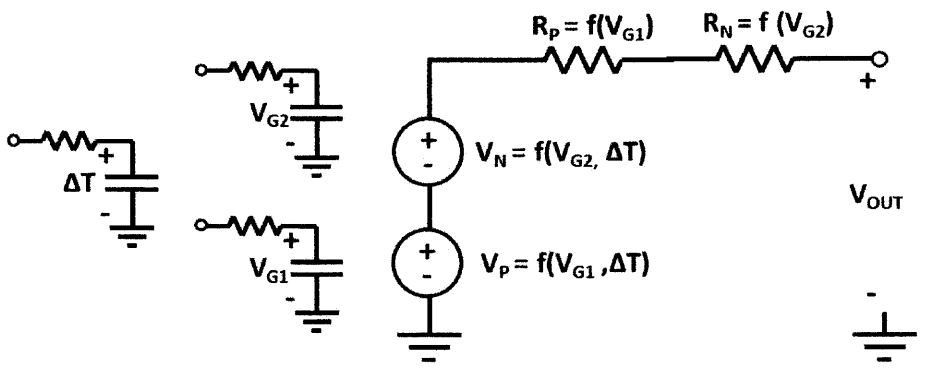

Figure 5-25: Spice Model for graphene based thermocouple

filter to take into account the thermal time constant of the device. Further voltage inputs taken into the gates of the device (VG1 and VG2) are also inputted into RC filters to take into account capacitive effects of gating graphene. The carrier concentration ($n_{s1} = C_{ox}V_{G1}/q$ and $n_{s2} = C_{ox}V_{G2}/q$) are then computed from the input gate voltages. The carrier concentrations and equation 5.3 are used to compute the Seebeck coefficient of each side of the thermocouple. Each branch of the thermocouple computes a voltage, as represented by a voltage source (V_N and V_P), by utilizing the relation $V = S\Delta T$. The voltages are then summed in series to take into account the total measured thermo-voltage. Finally, these computed carrier concentrations and equation 5.7 are used to compute the series resistance of the thermocouple (R_P and R_N). These parameters and inputs are summarized in Table 5.5.

In this chapter, we have looked at the performance estimates for graphene-based thermo-couple devices and we find that there are some advantages and unique aspects of this technology. Therefore, we have demonstrated a method for integrating graphene-based devices with thermal isolation in a MEMS structure. This modification has enabled an improvement of detection close to 7 V/W at DC at $\lambda = 10.6$ μm. Current device characterization is still on-going to better quantify the ultimate detection limit of these devices. In addition, we have also demonstrated a useful technology to directly integrate our graphene temperature sensors as a back-end of the line process with a foundry processed CMOS chip. This high-level integration should prove useful to complement our graphene technology with present state-of-the-art sil-

PARAMETERS	Name	Units	Value
Width	W	cm	10e-4
Length	L	cm	15e-4
Mobility	muG	$cm^{-2}V^{-1}s^{-1}$	1000
Impurity Charge	n0	$1/cm^2$	1e12
Oxide Capacitance	Cox	F/cm^2	5.75e-8
Temperature	T	K	300
Thermal Resistance	Rth	K/W	0.1
Thermal Capacitance	Cth	J/K	0
INPUTS			
Temperature Diff.	DT	K (1V = 1K)	-
Gate 1	VG1	V	-
Gate 2	VG2	V	-

Table 5.5: Table of SPICE parameters and inputs

icon technology, which can extend beyond infrared sensors, but also to chemical as well as optical sensors for graphene and other two-dimensional materials.

Chapter 6

Outlook and Future Work

6.1 Thesis Contributions

The contributions of this thesis span three main topic areas: (1) Graphene Materials and Transfer development; (2) Device Processing ranging from development of h-BN, ohmic contacts, titanium-metal interactions, RF devices and circuits; and (3) Graphene-based Thermal Detectors for infrared applications. The following lists papers that have contributed to each of these different areas.

Graphene Synthesis and Transfer

- S. M. Kim, A. Hsu, Y.-H. Lee, M. Dresselhaus, T. Palacios, K. K. Kim, and J. Kong, "The effect of copper pre-cleaning on graphene synthesis," *Nanotechnology*, vol. 24, p. 365602, Sept. 2013

- K. K. Kim, A. Hsu, et al, "Charge neutralization of CVD Graphene on various substrates," In Preparation, 2014.

Device Processing

- A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "High frequency performance of graphene transistors grown by chemical vapor deposition for mixed

signal applications," *Japanese Journal of Applied Physics*, vol. 50, p. 070114, July 2011

- A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, "Impact of graphene interface quality on contact resistance and RF device performance," *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1008–1010, 2011

- A. L. Hsu, R. J. Koch, M. T. Ong, W. Fang, M. Hofmann, K. K. Kim, T. Seyller, M. S. Dresselhaus, E. J. Reed, J. Kong, and T. Palacios, "Surface-induced hybridization between graphene and titanium," *ACS Nano*, July 2014

- K. K. Kim, A. Hsu, X. Jia, S. M. Kim, Y. Shi, M. Hofmann, D. Nezich, J. F. Rodriguez-Nieva, M. Dresselhaus, T. Palacios, and J. Kong, "Synthesis of monolayer hexagonal boron nitride on cu foil using chemical vapor deposition," *Nano Letters*, vol. 12, pp. 161–166, Jan. 2012

- K. K. Kim, A. Hsu, X. Jia, S. M. Kim, Y. Shi, M. Dresselhaus, T. Palacios, and J. Kong, "Synthesis and characterization of hexagonal boron nitride film as a dielectric layer for graphene devices," *ACS Nano*, Sept. 2012

- H. Wang, A. Hsu, D. S. Lee, K. K. Kim, J. Kong, and T. Palacios, "Delay analysis of graphene field-effect transistors," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 324–326, 2012

- H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Letters*, vol. 31, pp. 906–908, Sept. 2010

- S. M. Kim, A. Hsu, et al, "Synthesis of High Quality Large Area h-BN for Device Applications," In Preparation, 2014.

- R. J. Kock, A. Hsu, et al, "Titanium-induced symmetry breaking in Graphene," In Preparation, 2014.

Graphene-based Thermal Detectors

- P. K. Herring, A. L. Hsu, N. M. Gabor, Y. C. Shin, J. Kong, T. Palacios, and P. Jarillo-Herrero, "Photoresponse of an electrically tunable ambipolar graphene infrared thermocouple," *Nano Letters*, vol. 14, pp. 901–907, Feb. 2014

- A. Hsu, P. K. Herring, et al. "Graphene-based MEMS IR Thermopile," In Preparation, 2014.

- A. Hsu, P. K. Herring, et al. "Transparent-Flexible Graphene based Thermocouple," In Preparation, 2014.

6.2 Future Work

While in chapter 5, we have investigated the utilization of graphene as a thermal detector for primarily stand-off thermal imaging, in the following sections, we examine some future/ongoing work along four different directions: (1) Graphene Optical Choppers, (2) Graphene Plasmonic Absorption, (3) Graphene Surface Charge Sensors, and (4) Transparent Flexible Thermal Sensors.

6.2.1 Graphene Optical Choppers

As we have mentioned in Chapter 1, graphene's band structure is capable of direct inter-band optical absorption across the entire far-infrared and infrared spectra. This, coupled with the large tunability of the Fermi-energy level with respect to gate bias, also means that low energy states can become Pauli-blocked through the application of an applied electric field. Essentially, this means that we can create a tunable optical filter, which absorbs all energies above a specific value, as determined by the electrostatic gate bias. Unfortunately, a single layer of graphene can only absorb 2.3 % of the incident light. Therefore, in order to function as a more effective absorber, many layers of monolayer graphene are required (Eq. 6.1), so that the relation between the absorption and transmission through many layers becomes

$$T = [1 - \alpha_{graphene}]^{N_{layers}} \tag{6.1}$$

where, T is the optical transmission, $\alpha_{graphene}$ is the optical absorption through a single layer of graphene including both intra-band and inter-band processes, and N_{layers} is the total number of layers in the absorber. Therefore, to achieve approximately >90% optical absorption, requires a minimum of 99 layers of monolayer graphene. While 99 layers is achievable by direct transfer, this method is obviously extremely taxing and time consuming. Possible folding options with graphene could be considered which due to the exponential rate of film thickness by folding would only require a single layer of graphene and only 7 folds. However, while the film thickness also increases exponentially, the total film area is halved, which implies that if the final filter is to be 1 cm x 1 cm in size, the original starting material would have to be 12 cm x 12 cm. In addition, folding could causing tearing and damage while handling the film. Therefore, perhaps a more scalable process for generating such a structure is to directly create such a structure through direct synthesis of monolayer graphene as shown in Figure 6-1. Due to the graphene growth process occurring at low pressures, by altering the geometry at which we grow, we can in parallel grow 100's of sheets of graphene in a relatively small volume. Typically graphene is grown on copper foils around 25 μm thick. If we assume that we are able to space copper foils approximately 25 μm apart, then to grow 100's of sheets of graphene simultaneously would only consume a total width of 2.5 mm since we grow graphene on two surfaces per sheet of copper foil. This copper fin structure could be constructed in a variety of different ways: (1) manually holding 50 foils in parallel, (2) constructed using massively parallel techniques such as photolithography, (3) rapid prototyping techniques using metal sintering, or (4) massive hot wire saw structures. In addition, in this fin geometry, all of the copper could be etched in parallel while encasing the graphene in a rigid matrix - ideally some IR transparent polymer material. However, the second issue with all of these structures is how to electro-statically gate each of these layers. In the proposed geometry, one could utilize a common connection, such

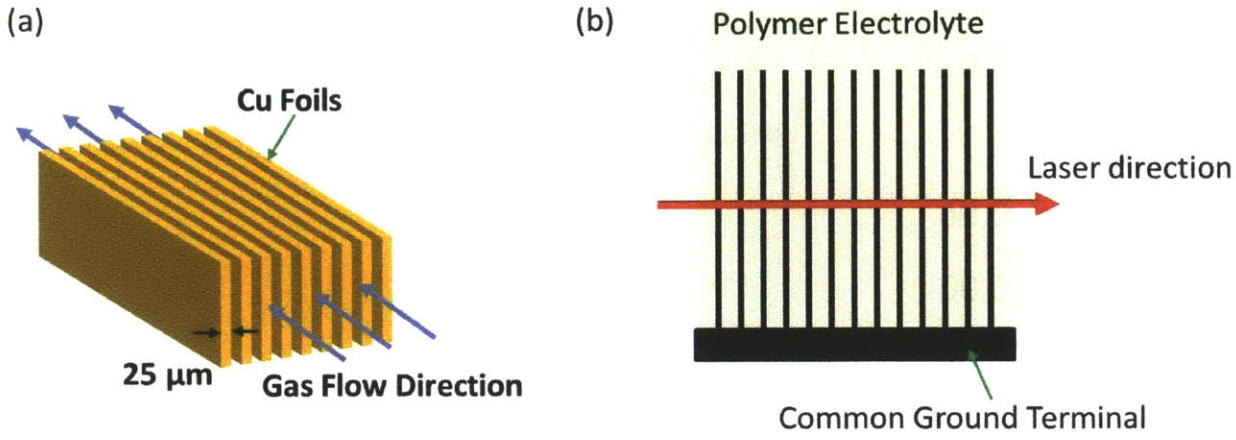

Figure 6-1: Graphene Optical Choppers (a) Multiple Layer Growth of Graphene Layers (b) Final Structure

that all of the graphene sheets are shorted together as one extremely large graphene sheet. Then with the addition, of a polymer electrolyte, one could actually fill the gaps in between the graphene layers, and the polymer electrolyte gate would form a double layer capacitance all along the surface of the graphene fins. One type of polymer electrolyte gate is that of PEO (poly(ethylene) oxide) for which we have measured the IR transmittance in the FTIR (Figure 6-2) [216].

From Figure 6-2, one sees that there are indeed various transmission bands within this polymer across the infrared, such that it could be used over a specific range of photon energies. In addition, through proper surface coating of the graphene, the PEO could also be made very thin to try to minimize any unwanted optical absorption through the PEO, since only the double layer capacitance near the interface of graphene is necessary for gating. Another added advantage of using polymer electrolyte gating is that the amount of induced charged density is extremely high $\sim 1 \times 10^{14}$ $1/\text{cm}^2$, which would correspond to approximately to an $E_f = 1.167$ eV (assuming no trigonal warping effects and higher level corrections to graphene's linear band structure). This would correspond to being able to Pauli block up to 2.334 eV photons, which corresponds to $\lambda = 531$ nm. This is advantageous mainly because we need to consider intra-band absorption effects, which will not be greatly modified by

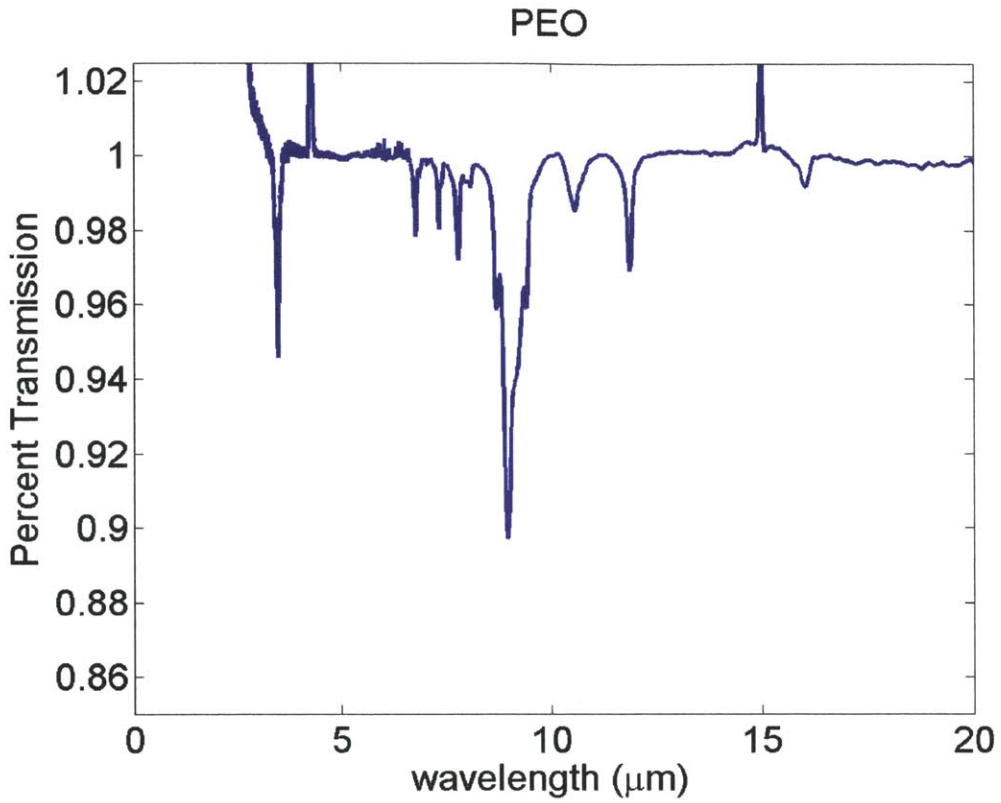

Figure 6-2: IR transmission of PEO (poly(ethylene) oxide).

adjusting the Fermi-energy level. These large carrier effects or Drude like optical absorption pathways will dominate mainly at longer wavelengths (>5 μm), which would serve to reduce the extinction ratio of this filter. Therefore this electrically controlled absorber may be better suited for $\lambda = 500$ to 5000 nm.

6.2.2 Graphene Plasmonic Absorption

In addition to graphene's potential for inter-band optical absorption, there has been a lot of interest in graphene for plasmonic absorption. Shown recently, [217, 218], plasmonic structures made of patterned graphene can potentially yield large (~100%) optical absorption. Utilizing periodic arrays of nano-patterned graphene (~60 nm) sized disks sitting in between two dielectric environments, it has been calculated that close to 100 percent optical absorption can be achieved with heavily doped graphene (0.4 eV $\sim 1 - 3 \times 10^{13}$ $1/\text{cm}^2$). This large optical absorption is due to the high carrier

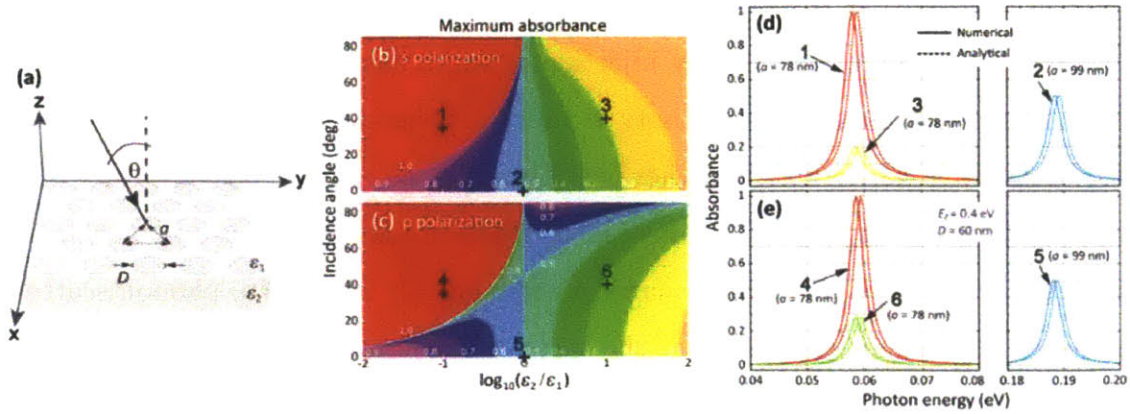

Figure 6-3: Plasmonic Absorption in nano-patterned graphene (a) Diagram of Plasmonic Absorber (b), (c) Colormap of maximum optical absorption as a function of the ratio of the dielectric constants above and below the graphene as well as angle of incidence for s and p polarized light. (d) and (e) absorbance as a function of photon energy for various points (1-6) labelled in (b) and (c).

density within graphene that leads to the coherent oscillation of electrons within the graphene sheets generating a resonant optical absorption [191]. This effect could be quite useful for our previously demonstrated graphene IR thermal detectors. We mentioned earlier that we can utilize materials such as carbon black for optical absorption; however, utilizing a single atomic monolayer of material might be more amenable as an optical absorber, since the device could still be optically transparent, but infrared active. Therefore, these plasmon resonance structures would be an interesting way to allow for ultra-thin thermal detectors, as well as, dual wavelength (vertically stacked) imaging structures. Furthermore, spatially patterned optical absorbers can also be created such that one can create directly integrated IR absorbers on the surface of a MEMS structure or thermopile.

6.2.3 Graphene Surface Charge Sensors

While our studies in infrared stand-off thermal imaging have primarily focused on the applications of graphene as a thermo-couple material, there are some intrinsic limitations of such a detection mechanism in terms of achievable response. As we have mentioned before, thermo-couple based sensing requires a large number of junc-

tions to increase the responsivity of these detectors, whereas bolometers can always increase their signal response by injecting a larger measurement current. However, the temperature change of resistivity at room temperature is usually around 4-6 %/K for vanadium oxide (VOx). Another possible approach is to leverage graphene's ultra-high carrier mobility or transconductance. While graphene itself is a poor bolometric material since graphene's charge carriers are relatively immune to phonon scattering, graphene is extremely sensitive to the surrounding charged environment, specifically the location of the charge neutrality point using (Eq. 6.2):

$$R_{graphene} = \frac{L}{W}\frac{1}{q\mu\sqrt{(n_s - n_{dirac})^2 + n_0^2}} \tag{6.2}$$

so assuming all factors are relatively constant with respect to temperature, except for n_{dirac}, we can compute the resistance change in graphene as a function of temperature (Eq. 6.3)

$$\frac{dR_{graphene}}{dT} = \frac{dR_{graphene}}{dn_{dirac}}\frac{dn_{dirac}}{dT} = \frac{L}{q\mu W}\frac{n_{dirac}}{((n_s - n_{dirac})^2 + n_0^2)^{3/2}}\frac{dn_{dirac}}{dT} \tag{6.3}$$

and we can rewrite Eq. 6.3 in terms of the temperature coefficient of resistance (TCR) of graphene (Eq. 6.4 and 6.5).

$$R_{tot} = R_{graphene} + \frac{dR}{dT}\Delta T = R_{graphene}\left(1 + \frac{1}{R_{graphene}}\frac{dR}{dT}\Delta T\right) \tag{6.4}$$

$$TCR = \frac{1}{R_0}\frac{dR}{dT} = \frac{n_{dirac}}{(n_s - n_{dirac})^2 + n_0^2}\frac{dn_{dirac}}{dT} \approx \frac{1}{n_{dirac}}\frac{dn_{dirac}}{dT} \tag{6.5}$$

The reason we assume that only n_{dirac} is a function of temperature, is that as we discussed earlier, many pyroelectric materials change their surface charge density as a function of temperature. As an example, we consider lead zirconium titanate (PZT) which has a pyro-electric 0.042 μC/(cm^{2}K) [219], thereby corresponding to a surface charge density of 2.625×10^{11} 1/(cm^{2}K). Assuming $n_0 = 1 \times 10^{11}$ 1/cm^2, n_s=0, so if we assume the starting value of $n_{dirac} >> n_0$ and $n_{dirac} \sim 5 \times 10^{12}$ 1/cm^2,

then the corresponding TCR = 5.25 %/K, assuming $n_{dirac} = 3 \times 10^{12}$ 1/cm^2, and we can achieve a TCR of 8.75 %/K. Therefore, assuming proper control of the starting n_{dirac} point, we can construct a very sensitive bolometer by coupling the surface charge generated by pyro-electric materials as a surface sensitive gating. If proper doping can be controlled, relatively large TCR's can potentially be engineered out of graphene.

6.2.4 Transparent Flexible Thermal Sensors

While previous work in this chapter has focused on graphene for infrared optical applications, we return back to graphene for thermal applications. While ultra-sensitive temperature sensors can be used for stand-off imaging by utilizing radiative heat transfer, other forms of heat transfer can also be used with a graphene sensor such as heat conduction. Therefore, graphene can serve as a general temperature sensor; however, when we compare graphene to many of the materials that can be used as a thermo-couple, we find that graphene has some unique properties: (1) it is extremely mechanically flexible, (2) it is also optically transparent, and (3) it is cheap to produce. While transparent conductive metals such as ITO can be doped to form various thermocouples, the values achievable by ITO as well as the flexibility for various electronic applications are still far off [220]. Furthermore, due to the optical transparency, graphene might serve as a unique opportunity for invisible electronic applications, where devices envisioned in the future can provide sensing opportunities without any visual indicator of the sensor. Therefore, revisiting our existing graphene-based thermal sensor, we investigate strategies and methodologies to make the structure transparent.

As we have discussed previously, graphene itself is already 2.3% transparent; however, the only thing that is not transparent in our present device, is the gate electrode. The gate electrode can be simply replaced with another layer of graphene such that one layer of CVD graphene can gate another layer of graphene electrostatically (Fig. 6-4 (a)). The only issue with this structure is the need to form a high quality, pin-hole free gate dielectric at the interface of graphene. This may be more difficult over large

areas of graphene due to issues pertaining to surface roughness, pin hole defects, and various particles, which make uniform gate dielectrics over large areas $>$ mm or $>$ cm a very daunting challenge. However, as a reminder, the need for an electrostatic gate is to simply modify the Fermi energy level of the graphene. This can also be achieved by other means such as chemical doping. While we have spent a lot of time studying doping of graphene in chapter 2, we can leverage these studies to chemically dope graphene both p and n type. This simplifies the device fabrication and allows for a more robust detector without the worry of mechanical deformation shorting the detector. For p-type dopants of graphene, there are many to choose from; $AuCl_3$, various charged ions, etc. can serve this purpose [221–224]. However, the choice for n-type dopants is more limiting. Much work has been spent on achieving sufficient n-type doping in graphene including synthesis of N-type graphene utilizing nitrogen dopants [225–228]; however, traditionally in our experiments, we find that our original Al(ox) often compensates the intrinsic doping of the material from p-type to n-type. Therefore we fabricated the structure shown in Figure 6-4 (b). Finally, the lateral geometry or layout of this device can be made quite large ($\sim$ mm), such that fabrication can be accomplished using shadow masking rather than more complicated micro-fabrication techniques.

We have begun process development and basic device fabrication of these device structures. Device testing to confirm the degree of n-type doping as well as a measurement regarding sensitivity and mechanically flexibility are scheduled for the near term future.

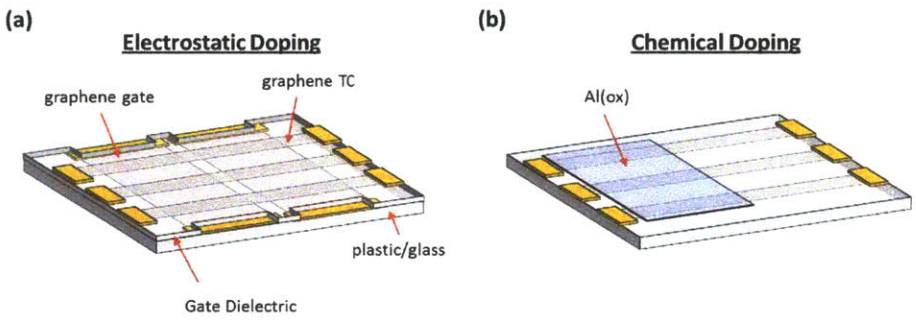

Figure 6-4: Transparent Flexible Thermal Sensors (a) Schematic of Electrostatically Controlled Thermal Sensor Devices (b) Chemically doped graphene-based thermocouples.

Appendix A

Process Flow

A.1 MEMS Device Process Flow

A.1.1 Starting Substrate Preparation

1. Start with Blank 4" Si Wafer (purchased from MTL)

2. Asher-TRL - 800W for 1 hour

3. TRL STS-CVD HFSiO_DP Recipe for 1 minute - Target Thickness = 75 nm [1]

   Deposition Temperature = 300 ° C

   Deposition Rate = 8.0 - 8.5 (nm/min)

   Approximate Stress = -443.917 MPa

4. TRL STS-CVD MFSiN_AH Recipe for 8 minute (9.5s HF/0.5s LF) - Target Thickness = 450 nm

   Deposition Temperature = 300 °

   Deposition Rate = 56.48 nm/min

   Approximate Stress = 174.3 MPa

[1] Run Etchback.rcp for 15-20 minutes and run HFSiO_DP recipe on dummy silicon to calibrate deposition rates before run - use Filmetrics to confirm deposition rate.

5. TRL STS-CVD HFSiO_DP Recipe for 1 minute - Target Thickness = 75 nm [2]

A.1.2 Gate Electrodes

1. TRL Coater (TRL PMMA Spinner)

   PMMA A4 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - bake at 175 °C for 7 minutes

2. Elionix 125 [3]

   Beam Current = 30 nA

   Dwell Time = 0.06 us

   Dose = 1800 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. Asher-TRL - 800W for 5 minutes

5. Ebeam-FP

   10 nm Ti - No Rotation, Dep. Rate = 0.1 nm/s

   20 nm Pt - No Rotation, Dep. Rate = 0.1 nm/s

6. Liftoff

   Acetone/IPA/N_2 and check under microscope [4]

[2]Total Stress of Wafer after deposition should be 29 MPa, and target total thickness $\sim$ 601.82 nm

[3]Depending on the gap between the gate electrodes ($<$ 500 nm) may require a multi beam current exposure.

[4]Ultrasonication may be necessary to ensure clean substrate - PWR = 5-6 for 2 minutes for all solvents should be sufficient.

7. Asher-TRL

   Descum - Asher 800W for 1 hour

A.1.3 Pad Electrodes

1. HMDS Oven - Recipe 5

2. TRL Coater

   AZ5214E (750 rpm for 2s, 3000 rpm for 60s)

   TRL Hotplate 2 - Bake at 80 °C for 5 minutes

3. MA-6

   9.8s vacuum contact mode (Pad Electrode Mask)

   TRL Hotplate 2 - Bake 105 °C for 1 minute

   97.8s flood exposure

4. Develop

   AZ422 - 2 minutes

   DiH_2O - 60s and N_2 - inspect after done

5. Asher-TRL - 800 W for 5 minutes

6. Ebeam-FP

   10 nm Ti - No Rotation, Dep. Rate = 0.1 nm/s .

   20 nm Pt - No Rotation, Dep. Rate = 0.1 nm/s

7. Liftoff

   Acetone/IPA/N_2 and check under microscope (ultrasonic might be necessary)

8. Asher-TRL

   Descum - Asher 800W for 1 hour

A.1.4 XeF_2 Vias

1. HMDS Oven - Recipe 3
2. TRL Coater

   SPR-7000 (750 rpm for 2s, 3000 rpm for 60s)

   TRL Hotplate 2 - Bake at 80 °C for 5 minutes
3. MA-6 - 14s vacuum contact mode (XeF_2 Vias)
4. Develop

   CD-26 - 90s

   DiH_2O - 60s and N_2 - inspect after done
5. Asher-TRL - 800 W for 5 minutes
6. Plasmaquest [5]

   CF4H2_AH.rcp (234-240 V - DC bias)

   Run for 10 minutes, 10 minutes, 3 minutes (Total Time = 23 minutes)

   chiller at 15 °C - Substrate at 21 °C [6]
7. Solvent Clean

   Acetone/IPA/N_2 with ultrasonics
8. Asher-TRL - 800W 1.5 Hours

A.1.5 Gate Dielectric/Pad Vias

1. TRL STS-CVD HFSiO_DP Recipe for 1 minute - Target Thickness = 75 nm [7]

[5] use a clean silicon wafer and condition with ETCHCLN.rcp and CF4H2_AH.rcp for 10 minutes before running real sample

[6] calibrated etch on dummy reference substrate samples with photolithography test - check with Dektak and also can check with XeF_2 etcher to see if suspension occurs. Etched regions should like silicon or have a slightly pinkish hue

[7] Run Etchback.rcp for 15-20 minutes and run HFSiO_DP recipe on dummy silicon to calibrate deposition rates before run - use Filmetrics to confirm deposition rate.

Deposition Temperature = 300 ° C

Deposition Rate = 8.0 - 8.5 (nm/min)

Approximate Stress = -443.917 MPa

2. HMDS Oven - Recipe 3

3. TRL Coater

   SPR-7000 (750 rpm for 2s, 3000 rpm for 60s)

   TRL Hotplate 2 - Bake at 80 °C for 5 minutes

4. MA-6 14s vacuum contact mode (Pad Vias Mask)

5. Develop

   CD-26 - 90s

   DiH_2O - 60s and N_2 - inspect after done

6. Asher-TRL - 800 W for 5 minutes

7. Plasmaquest [8]

   CF4H2_AH.rcp (234-240 V - DC bias)

   Run for 3 minutes and 30 s.)

   chiller at 15 °C - Substrate at 21 °C

8. Solvent Clean

   Acetone/IPA/N_2 with ultrasonics

9. Asher-TRL - 800 W for 1.5 hours.

[8] use a clean silicon wafer and condition with ETCHCLN.rcp and CF4H2_AH.rcp for 10 minutes before running real sample

A.1.6 Graphene Transfer

1. Graphene Transfer Done by Yi Song and Yong Cheol Shin
2. Check with Optical Microscopy and SEM to ensure continuous graphene
3. Make sure thermal reflow step is done and no drying by spinning.
4. Check Graphene Quality on Copper by SEM before transfer on to the rough substrate.
5. If Graphene Transfer is bad use NSL plasmatherm (90s of testp3.prc to remove graphene OR short Pirahna 45s and Asher-TRL to clean surface before retransfer)

A.1.7 Graphene Ohmics

1. TRL Coater (TRL PMMA Spinner)

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes

2. Elionix 125

   Beam Current = 30 nA

   Dwell Time = 0.08 us

   Dose = 2400 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. Ebeam-FP

   1 nm Ti - No Rotation, Dep. Rate = 0.1 nm/s

   30 nm Au - No Rotation, Dep. Rate = 0.1 nm/s

5. Liftoff

   Acetone/IPA/N_2 and check under microscope. Only Pipette should be necessary as long as PMMA is thick enough. Only leave in acetone for 2-3 hours before trying liftoff

A.1.8 Graphene Mesa

1. TRL Coater (TRL PMMA Spinner)

   PMMA A4 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes

2. Elionix 125 (Ohmic Mask)

   Beam Current = 30 nA

   Dwell Time = 0.06 us

   Dose = 1800 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. NSL-Plasmatherm

   testp3.prc for 15 s (48 V/ 128 W)

5. Asher-TRL - 800W for 5 minutes

6. Solvent clean

   Acetone/IPA/N_2 and check under microscope. Let sit in Acetone for 90 minutes

A.1.9 Device Suspension

1. TRL Coater (TRL PMMA Spinner)

   PMMA A4 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes

2. Elionix 125 (XeF2 Mask)

   Beam Current = 30 nA

   Dwell Time = 0.06 us

   Dose = 1800 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. Cleave chip into various dies

5. Plasmaquest

   CF4_AH.rcp 15 s (209.48 W/ 22 W/ 308.64 V)

6. XeF_2

   Cycles 2-3

   Etch Time 30 s

   Pressure (5000/5000/2200 mtorr)

   Check with microscope if undercut is sufficient; if not then place chip in for another cycle.

A.2 CMOS Device Process Flow

To handle chip, utilize Aluminium carrier disks from First Cut.

A.2.1 Sample Preparation

1. Solvent Clean

   Acetone/IPA/N2 with ultrasonics in teflon beakers (PWR = 5-6)

A.2.2 Via Etching

1. TRL Coater (TRL PMMA Spinner)

   MMA 8.5 EL 11.5 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes/ Cool for 3 minutes

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

2. TRL Hotplate 2 - Bake at 175 °C for 7 minutes/ Cool for 3 minutes

3. Elionix 125 (Via Etching)

   Beam Current = 30 nA

   Dwell Time = 0.08 us

   Dose = 2400 uC/cm^2

4. Develop Bilayer Resist (slight agitation)

   MIBK:IPA 1:3 for 90s

   METH:IPA 2:1 for 20s

   IPA for 60s

   N_2 and check in microscope

5. Plasmaquest

   CF4_AH.rcp (208 W/ 21 W/ 315 V - chiller at 15 °C - Substrate at 21 °C)

   Etch for 2 minutes/ Cool down for 3 minutes

   Etch for 2 minutes/ Cool down for 3 minutes

   Etch for 1 minutes/ Take out and inspect sample

6. Solvent Clean

   Acetone/IPA/N_2 with ultrasonics in teflon beakers (PWR = 5-6)

7. Asher-TRL

   30-45 minutes [9]

8. Plasmaquest

   CF4_AH.rcp (208 W/ 21 W/ 315 V - chiller at 15 °C - Substrate at 21 °C) for 3 minutes/ cool for 2 minutes

   Repeat approximately 7-9 times. After 6th or 7th etch take sample out and inspect under the microscope. Copper borders should begin to appear the metal pads.

   SEM/AFM plug structures to ensure that all of the top passivation has been removed and to measure the step height from the top of the passivation to the area in between metal structures

A.2.3 Ohmic Plugs

1. TRL Coater (TRL PMMA Spinner)

   MMA 8.5 EL 11.5 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake 175 °C for 7 minutes/ Cool for 3 minutes.

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake 175 °C for 7 minutes/ Cool for 3 minutes.

2. Elionix 125 (Ohmic Plug Pattern)

   Beam Current = 30 nA

   Dwell Time = 0.08 us

   Dose = 2400 uC/cm^2

[9] This time might influence the blanket passivation etch time

3. Develop Bilayer Resist (slight agitation)

   MIBK:IPA 1:3 for 90s

   METH:IPA 2:1 for 20s

   IPA for 60s

   N_2 and check in microscope - make sure one sees a deep undercut in the bilayer resist

4. Sputter (Harvard or EML - depending on process restrictions)

   Presputter Bias (RF) 45 W for 5 minutes at 3 mtorr

   Ti - Thickness 10 nm / 3 mtorr / ROT ON

   Au - Thickness 100 nm / 3 mtorr / ROT ON [10]

5. Liftoff

   Place Sample in Acetone (Teflon beaker) for 2 minutes, ultrasonic PWR 5.

   Place Sample in Acetone (Quartz beaker) for a couple of seconds

   Place Sample in IPA (Teflon beaker) for 2 minutes, ultrasonic PWR 3

   N_2 and check with optical microscope the metal structures

   Check Ohmic Interconnects in DC probe station on test dummy structures to make sure an Ohmic connection is achieved.

6. Asher-TRL - 800W for 30 minutes

A.2.4 Gate Electrodes

1. TRL Coater (TRL PMMA Spinner)

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - bake at 175 °C for 7 minutes

[10] Ti - 60 W/306 V/193 mA 0.3-0.4 Angstroms/s (8/13/2014), Au 30 W/ 518 V/ 56 mA 1 Angstroms/s - this strongly depends on the target used - fresh gold target should have conditions approximately 59 W/ 376 V/ 159 mA at 3 mtorr - check all targets before using real sample

2. Elionix 125

   Beam Current = 10/30 nA (fine/large features)

   Dwell Time = Depending on Dose

   Dose = 2200 - 2400 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. Asher-TRL - 800W for 5 minutes

5. Ebeam-FP

   10 nm Ti - No Rotation, Dep. Rate = 0.1 nm/s

   20 nm Pt - No Rotation, Dep. Rate = 0.1 nm/s

6. Liftoff

   Acetone/IPA/N_2 and check under microscope [11]

7. Asher-TRL

   Descum - Asher 800W for 1 hour

8. DC Probe Station

   Test Connection of Ti/Pt electrodes.

A.2.5 Gate Dielectric

1. TRL STS-CVD HFSiO_LT Recipe for 1 minute - Target Thickness = 75 nm [12]

   Deposition Temperature = 250 ° C

[11] Ultrasonication may be necessary to ensure clean substrate - PWR = 5-6 for 2 minutes for all solvents should be sufficient.

[12] Run Etchback.rcp for 15-20 minutes and run HFSiO_LT recipe on dummy silicon to calibrate deposition rates before run - use Filmetrics to confirm deposition rate.

Deposition Rate = 73.85 (nm/min)

A.2.6 Gate Vias

1. TRL Coater (TRL PMMA Spinner)

   MMA 8.5 EL 11.5 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes/ Cool for 3 minutes

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

2. TRL Hotplate 2 - Bake at 175 °C for 7 minutes/ Cool for 3 minutes

3. Elionix 125 (Via Etching)

   Beam Current = 30 nA

   Dwell Time = 0.08 us

   Dose = 2400 uC/cm^2

4. Develop Bilayer Resist (slight agitation)

   MIBK:IPA 1:3 for 90s

   METH:IPA 2:1 for 20s

   IPA for 60s

   N_2 and check in microscope

5. Asher-TRL

   Descum - Asher 800W for 5 minutes

6. Plasmaquest

   CF4_AH.rcp (208 W/ 21 W/ 354 V - chiller at 15 °C - Substrate at 21 °C)

   Etch for 2 minutes/ Cool down for 3 minutes

7. Solvent Clean

   Acetone/IPA/N_2 with ultrasonics in teflon beakers (PWR = 5-6)

8. Asher-TRL

   1 Hour

9. Metrology

   Inspect using AFM and SEM that the ohmic vias are exposed.

A.2.7 Graphene Transfer

1. Graphene Transfer Done by Marek Hempel and Yong Cheol Shin
2. Check with Optical Microscopy and SEM to ensure continuous graphene
3. Make sure thermal reflow step is done and no drying by spinning.
4. Check Graphene Quality on Copper by SEM before transfer on to the rough substrate.
5. If Graphene Transfer is bad use NSL plasmatherm (90s of testp3.prc to remove graphene OR short Pirahna 45s and Asher-TRL to clean surface before retransfer)
6. Ensure that the PMMA is thin enough to conform to the entire surface
7. Image in SEM at 2.5 keV for graphene contrast using inlens detector.

A.2.8 Graphene Ohmics

1. TRL Coater (TRL PMMA Spinner)

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes

2. Elionix 125 (Graphene Ohmic Mask)

   Beam Current =25 nA

   Dwell Time = 0.08 us

   Dose = 2000 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. Ebeam-FP

   1 nm Ti - No Rotation, Dep. Rate = 0.1 nm/s

   30 nm Au - No Rotation, Dep. Rate = 0.1 nm/s

5. Liftoff

   Acetone/IPA/N_2 and check under microscope. Only Pipette should be necessary as long as PMMA is thick enough. Left in acetone overnight - but do not let the samples flip over or scratch the surface.

A.2.9 Graphene Mesa

1. TRL Coater (TRL PMMA Spinner)

   PMMA A8 (750 rpm for 2s, 4000 rpm for 60s)

   TRL Hotplate 2 - Bake at 175 °C for 7 minutes

2. Elionix 125 (Graphene Mesa Mask)

   Beam Current = 25 nA

   Dwell Time = 0.08 us

   Dose = 2000 uC/cm^2

3. Develop PMMA

   MIBK:IPA 1:3 for 90s

   IPA for 60s

   N_2 and check in microscope

4. NSL-Plasmatherm

   testp3.prc for 75 s (48 V/ 128 W)

5. Asher-TRL - 800W for 5 minutes

6. Solvent clean

   Acetone/IPA/N_2 and check under microscope. Let sit in Acetone for a couple of hours.

7. Chip ready for packaging by Sungjae Ha.

A.2.10 FIB Cutting

In case of issues during packaging, the FIB can be used to remove or destroy shorts on the chip. Using the continuous SEM option on the FIB in CMSE to monitor the etch, a beam current of 0.28 - 0.93 nA, with an approximate dose of 2-5 nC/um^2, was sufficient to cut most metal lines. Note that there is some re-sputtering of the removed material on the sidewalls of the sample.

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