Processing Technology for High Quality AlGaN/GaN MOSHEMT Interfaces

by

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Submitted to the Department of Electrical Engineering and Computer Science
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ABSTRACT

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) are very promising for applications requiring high power and high operating frequencies due to its intrinsic material properties like the high electron mobility, large critical electric field and large carrier concentration. For power switching applications, it is necessary to lower gate leakage by introducing a gate insulator between the gate metal and the AlGaN barrier. This thesis focuses on studying the impact of processing conditions on the quality of the gate stack of AlGaN/GaN based MISHEMTs. First, the role of mobile ions like sodium in impacting the threshold voltage of AlGaN/GaN MIS-HEMTs was studied. Characterization techniques like bias temperature stress (BTS) that were traditionally used for characterizing mobile ions in SiO_2/Si capacitors were adapted for AlGaN/GaN MISHEMTs. Next, the impact of fabricating Al_2O_3/AlGaN/GaN MISHEMTs by using a CMOS compatible gate first process flow vs an Au-contact based, liftoff oriented process flow was evaluated. The differences between capacitors and transistors fabricated by different process flows were evaluated by a combination of high bias capacitance-voltage (CV) and transient current-voltage (IV) measurements. Organic contamination from the ohmic first process flow was attributed as being the key cause of the superior interface for the AlGaN/GaN MISHEMT processed using a gate first process flow. Finally, the gate first process flow was used to fabricate additional AlGaN/GaN MISHEMTS in order to look at the impact of atomic layer deposition (ALD) nucleation layers, the AlN interlayer, annealing conditions and AlGaN oxidation on the quality of the gate stack.

Thesis Supervisor: Tomás Palacios
Title: Associate Professor of Electrical Engineering

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Lastly, all thanks are due to God.

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Chapter 1 Introduction

Gallium Nitride (GaN) and associated nitride-based semiconductors have been of great interest for their electrical and materials properties. GaN first attracted attention because its large direct bandgap (3.4 eV) made it promising for making blue LEDs. Herbert Maruska of RCA Laboratories reported single crystal Gallium Nitride for the first time in 1969 [1]. Maruska et al. were able to identify Mg has a promising acceptor for obtaining p-type GaN necessary for making LEDs [2]. However, the low electrical conductivity coupled with financial difficulties made it difficult to continue work in GaN and worldwide, work on GaN based diodes stopped for more than a decade. Interest in GaN resurged after Amano et al. discovered that irradiating Mg doped GaN with electrons made it conductive enough to make a PN diode [3]. S. Nakamura then developed the first commercial GaN LEDs in the early 1990s and the market for GaN LEDs took off [4].

The growing interest in GaN led to the realization that the unique combination of wide bandgap, high electron mobility and large breakdown voltage made it very promising for electronics applications as well. M.A. Khan et al. reported the formation of a two dimensional electron gas at AlGaN/GaN heterojunction in 1991 [5] and after sufficient material improvement was achieved, the first GaN metal semiconductor FET (MESFET) and high electron mobility transistor (HEMT) were demonstrated in 1993 [6], [7]. Since then, GaN based transistors have attracted a lot of attention for microwave applications [8] and more recently for power applications as well.

Initial AlGaN/GaN HEMTs used Schottky gates given that microwave applications are more forgiving of gate leakage. However, power electronics applications require low gate leakage and therefore early on, the need for incorporating a gate oxide between AlGaN barrier and the gate metal was identified [9], [10]. The first reported dielectrics were silicon nitride (SiN) and silicon dioxide (SiO_2) and as expected, incorporating these films resulted in the expected reduction in gate leakage and increase in breakdown voltage [11].

The first use of Al_2O_3 as an insulating layer on AlGaN/GaN was reported in 2003 by T. Hashizume et al. [12]. The increasing interest in atomic layer deposition (ALD) as a viable gate dielectric technology led to the first demonstration of ALD deposited Al_2O_3 has a gate insulator for AlGaN/GaN HEMTs by P.D. Ye et al. in 2005 [13]. Since then, HfO_2 based devices deposited by reactive sputtering and ALD have been reported [14],[15] as well.

Introducing gate dielectrics in GaN based transistors pose additional challenges as well. The gate breakdown voltage must be large enough to withstand high voltage spikes that the gate routinely sees in high voltage switching. Hysteresis and trapping must be reduced or even eliminated. To study these, the characterization techniques used to study the AlGaN/oxide interfaces have gotten more sophisticated over the years. Earlier studies were limited to assessing the impact of introducing gate insulators on gate leakage, current collapse and change in maximum current [12],[13]. Later work involved attempts to calculate D_{it} by using the conductance method and by using an adapted version of the Terman method [16]. Swenson et al. detailed how deep level traps can only be probed by the use of ultraviolet light [17].

However, the earlier work did not emphasize the importance of applying positive biases in order to look at the AlGaN/oxide interface. Applying positive biases large enough for carriers to leave the 2-DEG and go into the AlGaN is very important for probing the oxide/AlGaN interface. Mizue et al. published one of the first systematic studies of charging defects by applying large positive biases [18]. Lagger et al. studied the impact of positive gate pulses on the threshold voltage of AlGaN/GaN MIS-HEMTs [19].

Simultaneously, the fabrication technology for power devices has evolved away from Au bearing contacts and liftoff based processing to silicon compatible processing. Many commercially available power devices offered by companies like International Rectifier and Efficient Power Conversion (EPC)

Corporation are being fabricated in silicon foundries [20]. IMEC has led a visible research program on developing gate stacks for devices processed in a CMOS compatible process flow [21],[22] . Wang et al. asserted that process flows that use alloyed Au-based ohmic contacts cause surface degradation which in turn causes current collapse [23]. Given these reports and given that companies are moving towards manufacturing GaN in Si compatible foundries, it would be very valuable to perform a direct comparison of GaN devices fabricated with a CMOS compatible process flow with devices fabricated with a process flow utilizing liftoff and Au based ohmic contacts in order to understand the impact of CMOS compatible process flows on the performance of GaN based devices. However, to the best of this author's knowledge, there has not been a direct comparison of GaN devices fabricated in a CMOS environment with a CMOS-friendly process flow with devices fabricated with a traditional Au-based, liftoff-oriented process. This might be due to the fact that institutions with CMOS fabrication facilities can't allow a liftoff-based process while fabs where Au processes are allowed typically do not have the facilities or the knowhow to process using a CMOS compatible process flow. The presence of a CMOS compatible lab like the Integrated Circuits Laboratory (ICL) at MIT together with a III-V compatible fab like the Technology Research Laboratory (TRL) allow for performing a direct comparison of the two kinds of process flows.

Scope of Thesis

There are three key themes of this thesis. First, this thesis aims to study the impact of processing conditions and process flows on AlGaN/GaN MISHEMTs. By directly comparing CMOS style gate first processes to a traditional Au-based liftoff process flow, it allows for directly accessing the impact of using a CMOS style gate first process flow. Second, this thesis aims to highlight a combination of characterization techniques that can be used to study the AlGaN/oxide interface. Finally, this thesis aims to look at the impact of processing conditions on the AlGaN/oxide interface and on the robustness of the gate stack.

Outline of Thesis

Chapter 2 deals with the impact of mobile ion contamination on AlGaN/GaN MIS-HEMTs. Species like Na+ and K+ can easily drift though gate oxide materials like SiO_2 and identifying mobile ions as a source of threshold voltage instability was key for commercializing Si based MOS devices in the 1960s. This chapter adapts the characterization techniques used for identifying mobile ion contamination in Si based MOS devices to AlGaN/GaN MISHEMTs with ALD deposited oxides like Al_2O_3.

Chapter 3 motivates the need to develop a gate first process. First, the compatibility of GaN with CMOS front end tools like atomic layer deposition (ALD) is studied by performing TXRF based contamination studies. Then, the formation of low temperature ohmic contacts necessary for a robust gate first process is studied.

Chapter 4 directly compares capacitors fabricated by using a gate first process with capacitors fabricated by a standard ohmic first process with ohmic contacts formed at 800°C. The interface is characterized by performing high bias capacitance-voltage (CV) measurements. The difference in surface cleaning is identified as the key difference between the gate first process and the ohmic first process.

Chapter 5 describes transient current voltage measurements that are used to further study AlGaN/oxide interfaces. These measurements are performed on the gate first and ohmic first samples that were compared in Chapter 4. These transient measurements give insight into the recovery mechanism of transistors after traps are occupied due to the application of a positive bias.

Chapter 6 describes process optimization performed with the gate first process flow that was validated in Chapters 4 and 5. First, the impact of nucleation layers on the oxide AlGaN interface is studied. Second, the impact of the AlN interlayer on CV measurements is studied. Third, the impact of

annealing gasses on transistor properties is investigated. Finally, a gate first process flow is used to demonstrate a SiO_2 based gate stack that relies on oxidizing deposited polysilicon.

Chapter 7 includes conclusions and a discussion of future work that can be carried out to expand the scope of this thesis.

Chapter 2 Mobile Ion Contamination

This chapter will first describe how to adapt electrical characterization techniques used to identify mobile ion contamination in SiO_2/Si MOS for GaN based MIS-HEMTs and MOS devices. Then, sources of mobile ion contamination will be studied and finally the impact of mobile ion contamination on AlGaN/GaN MOS-HEMTs will be studied.

Importance of studying mobile ion contamination

The first SiO_2/Si MOS device was demonstrated by Dawon Kahng and M.M. Atalla of Bell Telephone Laboratories in 1960 [24],[25]. MOS devices were very promising for low power applications due to the absence of the base leakage current that is intrinsic to bipolar transistors and due to the ability to design circuits with complementary PMOS and NMOS transistors, as first demonstrated by Frank Wanlass and C.T. Sah of Fairchild R&D Lab in 1963 [26]. However, early MOS devices exhibited threshold voltage instability both in operation and in fabrication which precluded their commercialization. Ionic contaminants like sodium and potassium were conclusively identified as culprits of this threshold voltage instability. Sodium and potassium ions can drift through SiO_2 at relatively low temperatures (200°C) and thus can easily cause the V_{th} of MOS devices to change. Once mobile ion contamination was identified conclusively by Edgar Snow of Fairchild in 1965 as the cause of threshold voltage instability, steps were taken towards eliminating this contamination in order to allow for commercializing MOS devices [24], [27]. Mobile ion contamination was eliminated by using semiconductor grade materials and by implementing strict cleanroom protocols which helped reduce contamination from human bodies [28].

Characterizing Mobile Ion Contamination in GaN

Power GaN switches require the introduction of a gate dielectric in order to reduce gate leakage. It is appropriate to assess if mobile ion contamination is an issue for AlGaN/GaN MOSHEMTs

given that mobile ion contamination caused problems for commercializing MOS devices in the 1960sas discussed in this chapter.

Mobile ion contamination has been studied with various techniques. A key technique is called bias temperature stress (BTS) [29]. First, a high frequency CV measurement is done in order to measure the initial channel charge. Then, the capacitor is heated to 200°C and a positive or negative bias is applied. A positive bias causes mobile ions to shift away from the gate metal (where they are shielded) and towards the gate oxide where they cause the threshold voltage to shift as schematically shown in Figure 2-1. Then, the capacitor is cooled down while keeping the capacitor under bias in order to prevent the mobile ions from diffusing apart. This requires that the probes are adjusted when cooling down in order to prevent any shorting due to the probes moving due to thermal contraction. Once the capacitor is at room temperature, another high frequency CV measurement is done in order to remeasure the channel charge. The change in threshold voltage is a result of the mobile ions moving from the gate metal towards the oxide as illustrated in Figure. Finally, the process can be reversed by applying a negative bias in order to move the mobile ions back towards the gate metal.

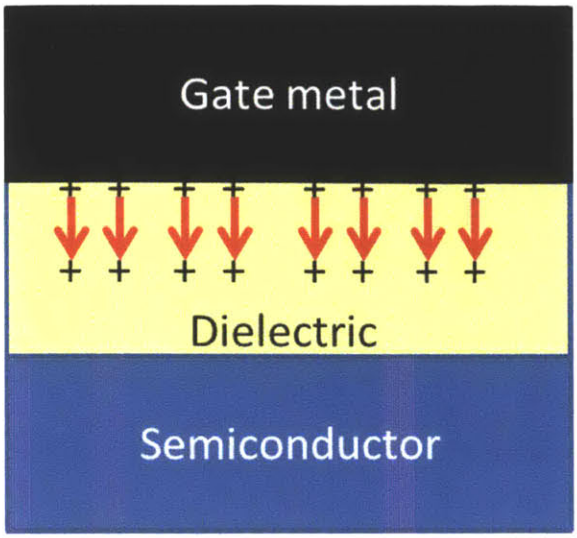


Figure 2-1: Under Bias Temperature Stress (BTS) measurements, the threshold voltage shifts due to mobile ions drifting from the gate metal (where they are screened) into the oxide. The positively charged mobile ions move into the gate oxide when a positive bias is applied at the gate at high temperature (200°C)

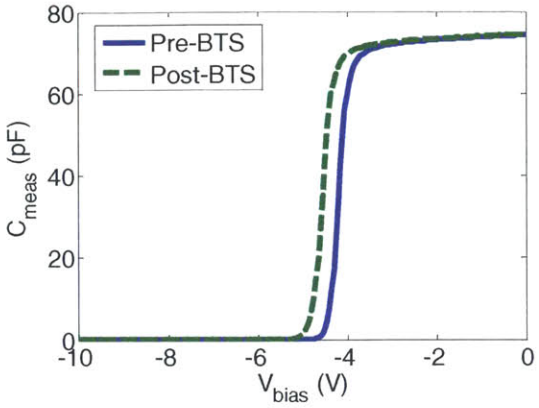


Figure 2-2: Change in threshold voltage in HfO_2/AlGaN/GaN CV measurements due to mobile ion drift

However, there are several key considerations that need to be taken into account when adapting bias temperature stress measurements to AlGaN/GaN based MIS-HEMTs. One consideration is the impact of the gate oxide material on the measurement. For example, silicon nitride and silicon oxynitride films have been reported to be barriers to sodium movement in gate stacks and thus a bias temperature stress measurement would not work as a means for detecting the total amount of mobile ions present [30],[31].

In order to evaluate the impact of gate oxide material on the ability to use bias temperature stress, AlGaN/GaN MIS-HEMTs with 20 nm of SiO_2, 20 nm of Al_2O_3 or 20 nm of HfO_2 were fabricated. First, Ti/Al/Ni/Au (200Å/1000Å/250Å/500Å) ohmic contacts were patterned by doing liftoff. Then, the samples were annealed at 800°C for 30s in order to form ohmic contacts. Following the ohmic contact formation, the devices were isolated by a BCl_3/Cl_2 based mesa isolation etch. Then, the samples were cleaned by a UV ozone treatment for 2 min and then a NH_4OH:DI (1:1) dip for 2 min before the samples

were loaded into the ALD for the oxide depositions. The SiO_2 deposition was performed using the process described by D. Hausmann et al. [32]. Following the oxide depositions, Ni/Au/Ni gates were patterned by liftoff and finally, the stack was annealed at 400°C in order to densify the gate stack.

As expected, the MIS-HEMT with SiO_2shows an expected shift in V_{th} of -1V after performing a BTS stress with positive gate voltage. However, the MIS-HEMT with Al_2O_3 (Figure 2-5), shows a V_{th} shift of + 0.5V which is indicative of electron injection as opposed to mobile ion drift. Al_2O_3 has been reported as a block for mobile ions and historically, diffusion tubes were coated by alumina in order to prevent mobile ions from leaching out of furnaces [28].

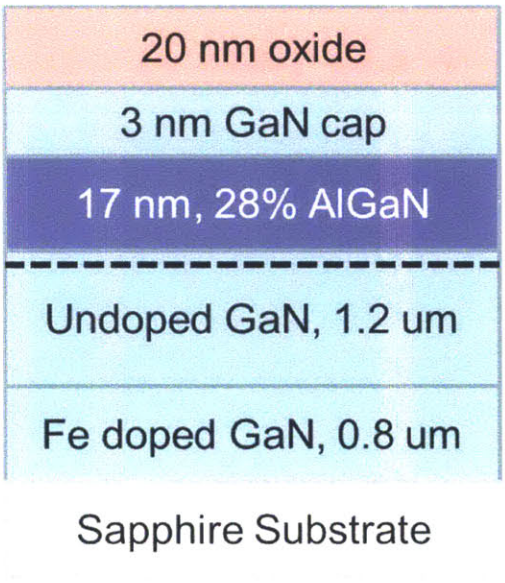


Figure 2-3: Schematic of MIS-HEMT structures used for studying the impact of dielectric on BTS results.

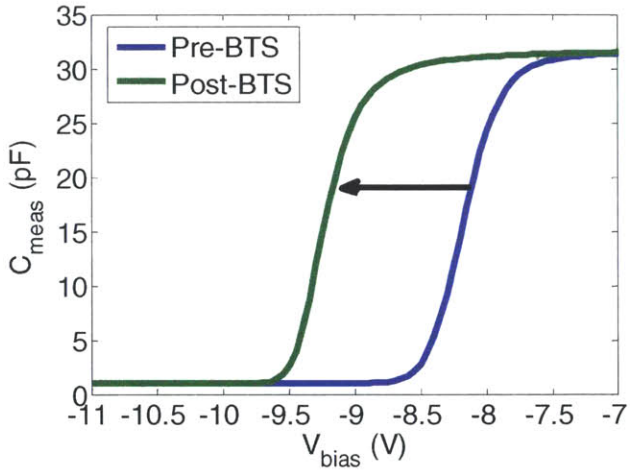


Figure 2-4: BTS results for 20 nm SiO_2/AlGaN/GaN MIS-HEMT. Note that change in V_{th} is negative due to mobile ion drift resulting from the positive gate stress

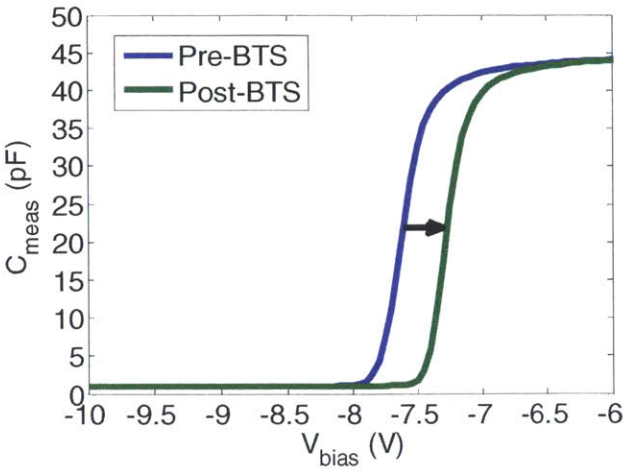


Figure 2-5: BTS results for 20 nm Al_2O_3/AlGaN/GaN MIS-HEMT. Al_2O_3 is said to be a barrier for sodium transport. Therefore, mobile ions do not shift much and thus the change in V_{th} is due to electron injection into the AlGaN/oxide interface

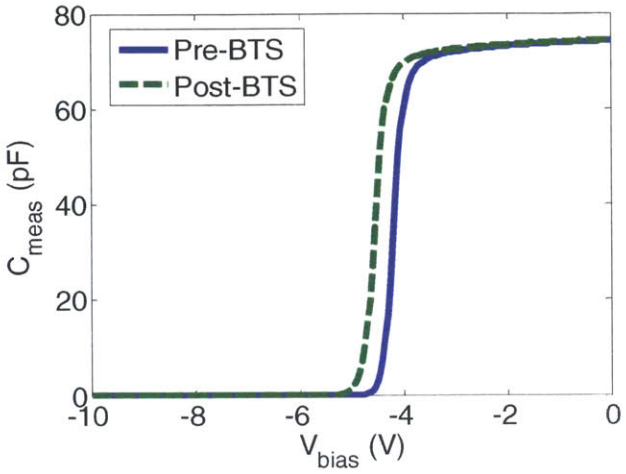


Figure 2-6: BTS results for 20 nm HfO_2/AlGaN/GaN MIS-HEMTs. Based on V_{th} shift, HfO_2 allows for sodium drift.

The second consideration is the impact of the bias level on BTS measurements. Typically, a bias level equivalent to 1 MV/cm has been used when characterizing SiO_2/Si capacitors [29]. However, when using structures like AlGaN/GaN MISHEMTs, applying a large positive bias can cause electrons to leave the 2-D electron gas (2-DEG) and get injected into the AlGaN/dielectric interface as shown in Figure 2-7 and Figure 2-8, which in turn will counteract the impact of the mobile ion drift. Therefore, the bias level needs to be large enough to move the mobile ions but small enough to ensure that there is not excessive electron injection into the AlGaN and AlGaN/dielectric interface. Of course, the voltage shift due to electron injection depends on the quality of the interface, the quality of the AlGaN and the number of bulk traps present in the gate oxide and so all factors must be taken into consideration before selecting a bias level.

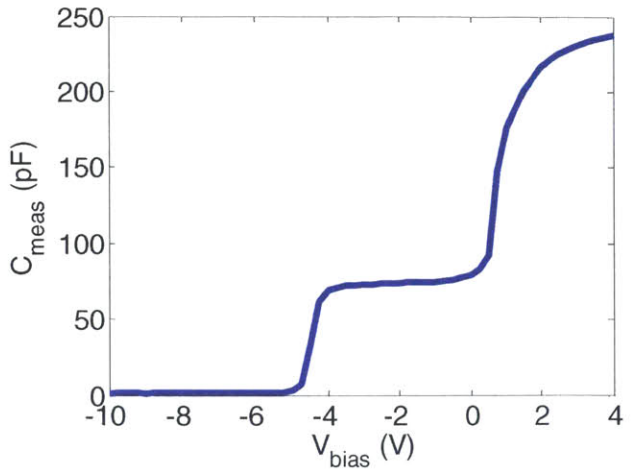


Figure 2-7: Quasi-static CV measurement of HfO_2/AlGaN/GaN capacitor. When the bias exceeds 0V, electrons leave the 2-DEG and go towards AlGaN/oxide interface. As a result, the measured capacitance increases.

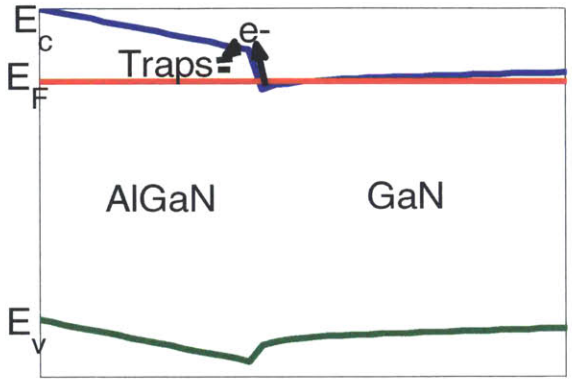


Figure 2-8: Schematic of band diagram showing that under positive bias, electrons can leave 2-DEG at AlGaN/GaN interface and get injected into AlGaN and AlGaN/dielectric interface

Therefore, in order to assess the impact of bias level on BTS results, HfO_2/AlGaN/GaN capacitors were stressed at 200°C with a bias of 1 V and 4 V given that 4 V corresponds to a field of 1 MV/cm. However, as seen in Figure 2-7, electrons have populated the AlGaN/dielectric interface at a bias of 4V. As seen in Figure 2-10, the BTS measurement with a bias level of 4V actually results in the threshold voltage shifting positive. On the other hand, when BTS measurements are done with a bias of 1 V, the change in threshold voltage due to the mobile ions is greater than due to electron injection and thus mobile ions can be detected (Figure 2-9).

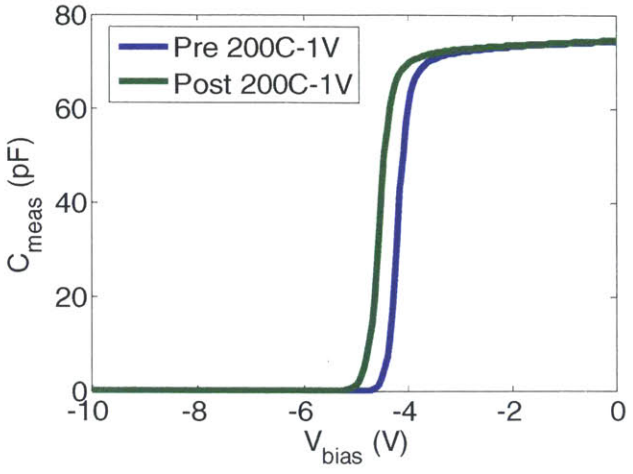


Figure 2-9: BTS measurement with bias of 1V. Negative shift in V_{th} due to mobile ions is more pronounced than any positive shift in V_{th} due to electron injection

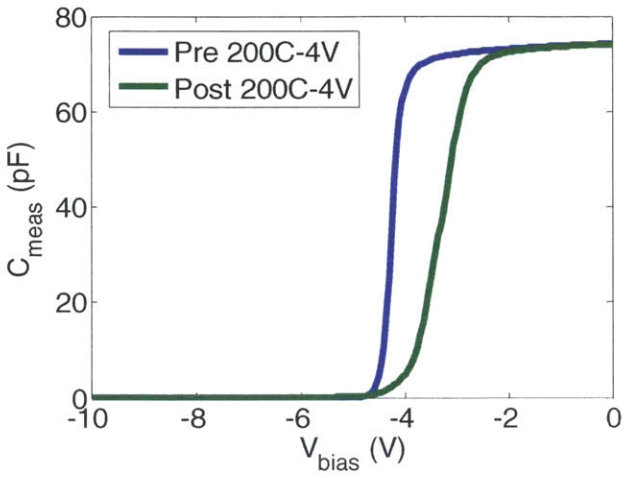


Figure 2-10: BTS measurement with a bias of 4V. Electron injection swamps any negative shift in V_{th} due to mobile ions. As a result, it's not possible to detect presence of sodium ions with this bias level

Finally, the device structure also plays a role in the bias temperature stress measurements. In addition to HEMT structures, capacitors fabricated on top of doped GaN were also fabricated. One drawback of MIS-HEMT structures is the presence of AlGaN, since it serves as a layer where electrons can get trapped. However, by depositing oxides on top of a Si doped GaN layer, the electric field only drops across the oxide and there is no semi-insulating layer in the middle where electrons can be trapped. This allows for applying a larger electric field without worrying about trapped electrons. As can be seen by the difference between Figure 2-11 and Figure 2-12, the MOS sample that was processed together with the MIS-HEMT sample shows much greater differences in charge due to bias temperature stress measurements.

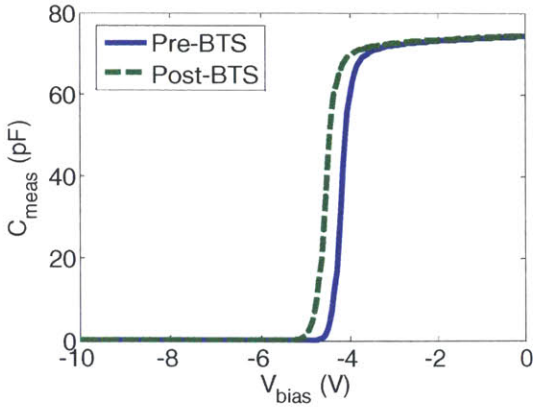


Figure 2-11: HfO_2/AlGaN/GaN MIS-HEMT capacitor processed with HfO_2/nGaN/GaN MIS capacitor shown in Figure 2-12.

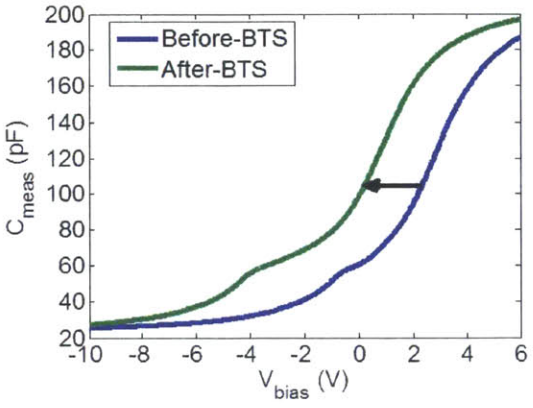


Figure 2-12: HfO_2/nGaN/GaN MIS capacitor processed together with MIS-HEMT described in Figure 2-11. Given that there is no AlGaN layer for charges to get trapped in, the change in threshold voltage due to mobile ion drift is fully manifested.

Glassware as Sodium Contamination Source

One key source of contamination is the glassware that is used for wet processing. Much of the glassware that was used in the fabrication process was made with borosilicate glass (Pyrex®). Borosilicate glass contains 3.8% Na_2O by weight [33] and Na_2O can be etched in commonly used acids like HCl and H_2SO_4 [34],[35]. In order to confirm that the use of borosilicate glass is a source of sodium, two sets of devices were fabricated. For one set of devices (both a HfO_2/n-GaN MOS structure and HfO_2/AlGaN/GaN MIS-HEMT), only borosilicate glass beakers were used while for the other set of devices, Teflon and semiconductor grade quartz beakers were used. Materials like semiconductor grade quartz and PFA and PTFE Teflon® are commonly used in CMOS processing and due to their material purity do not have alkaline and heavy metal contaminants.

For both sets of devices, first Ti/Al/Ni/Au (200Å/1000Å/250Å/500Å) ohmic contacts were patterned by doing liftoff. Then, the samples were annealed at 800°C for 30s in order to form ohmic contacts. Following the ohmic contact formation, the devices were isolated by a BCl_3/Cl_2 based mesa

isolation etch. Then, the samples were cleaned by a UV ozone treatment for 2 min and then a NH_4OH:DI (1:1) dip for 2 min before the samples were loaded into the ALD for HfO_2 and Al_2O_3 depositions. Following that, a Ni/Au/Ni gate stack was patterned by liftoff.

Bias temperature stress measurements were done on the HfO_2/n-GaN capacitors in order to directly compare the impact of using semiconductor grade glassware on the concentration of mobile ion contamination. As can be seen, the sample that was processed in Pyrex beakers showed a change 1×10^{13} cm^{-2} change in carrier concentration after the BTS measurement while the change in carrier concentration for a capacitor that was fabricated in semiconductor grade quartz was less than 5×10^{11} cm^{-2}. These results show that with proper cleaning and the use of appropriate glassware, it is possible to greatly reduce mobile ion contamination even in a university cleanroom setup.

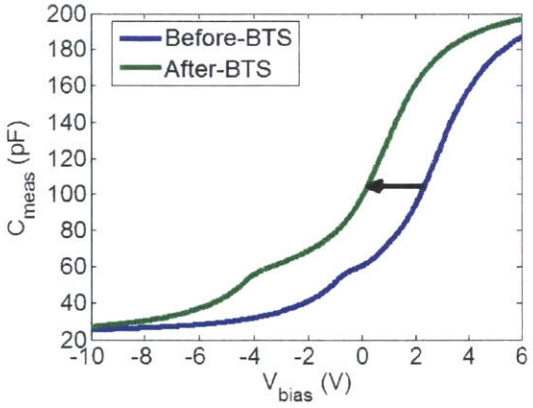


Figure 2-13: BTS results for HfO_2/n-GaN MOS capacitor processed in Pyrex beakers. The change in carrier concentration after the BTS stress is 1×10^{13} cm^{-2}.

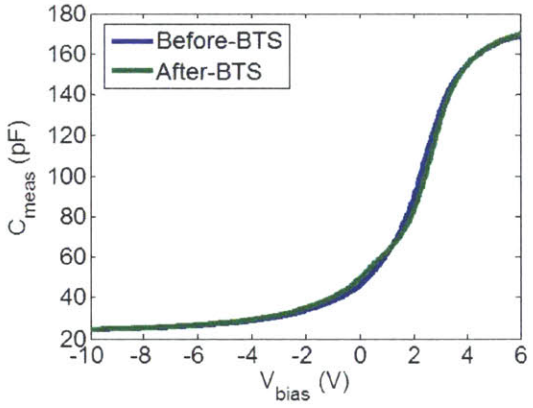


Figure 2-14: BTS results for HfO_2/n-GaN MOS capacitor processed in clean PTFE and quartz beakers. The change in carrier concentration after BTS stress is less than 5×10^{11} cm^{-2}

Impact of Mobile Ions on HEMT device performance

Depositing gate oxides on AlGaN/GaN HEMTs has been reported to have an impact on the carrier concentration [36]. In particular, Al_2O_3 has been reported to have positive charges at the interface which in turn induces additional carriers in the 2-DEG in order to compensate for the positive charges [37],[38],[39]. However, as seen with BTS measurements, if mobile ions are present, they can distort the measured carrier concentration. In order to illustrate this, a HfO_2 capacitor with mobile ion

contamination was subjected to both a positive and negative BTS stress in order to see how much the channel charge changed due to mobile ions contamination. As seen in Figure 2-16, the carrier concentration can vary anywhere from 5.1×10^{12} to 8.2×10^{12} cm^{-2}. Given that hall measurements on a fresh sample indicated that the carrier concentration was 6.5×10^{12} cm^{-2}, this highlights how mobile ion contamination can obscure whether an oxide is positive or negatively charged.

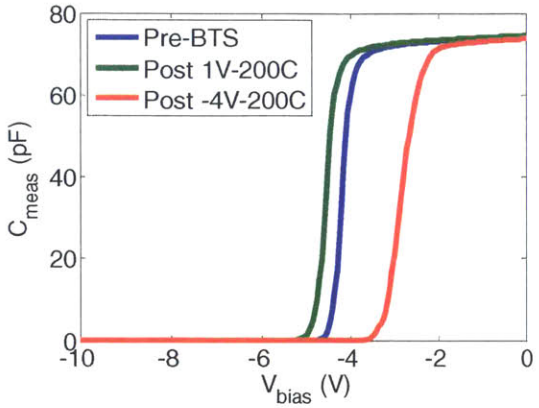


Figure 2-15: Capacitance-Voltage plots of HfO_2/AlGaN/GaN capacitor after BTS measurements at +1V and -4V. The drastic change in V_{th} and the corresponding channel charge highlight the extent to which mobile ion contamination can mask the impact of gate oxide on channel charges

Condition	Charge
Pre-BTS	7.5×10^{12} cm^{-2}
Post 1V BTS	8.2×10^{12} cm^{-2}
Post -4V BTS	5.1×10^{12} cm^{-2}
Hall Measurement on fresh sample	6.5×10^{12} cm^{-2}

Figure 2-16: Charges as determined by integrating the CV curves in Figure 2-15 from V_{th} to 0V. Based on the Hall measurements of the fresh sample, it illustrates how HfO_2 based oxides can be incorrectly thought to have positive charges in the oxide.

If mobile ions drift during device operation or testing, this results in dynamic changes in the threshold voltage. AlGaN/GaN on sapphire substrates can easily achieve junction temperatures that exceed 150°C, which allows for mobile ions to drift [40],[41]. Therefore, during device operation with a large V_{ds}, it is possible for the V_{th} to change during device operation, which would in turn cause the drain current to change as well. In order to illustrate this, sampling measurements were performed where the gate was pulsed at a high bias (V_{gs} > 0V) for 5s before looking at the recovery for 25 s at V_{gs} = 0V as depicted in Figure 2-17. The V_{ds} value was set to either V_{ds} = 1V or V_{ds} = 10V such that the channel temperature would be different. The high bias injects electrons but also allows for mobile ions to move if the channel temperature is hot enough.

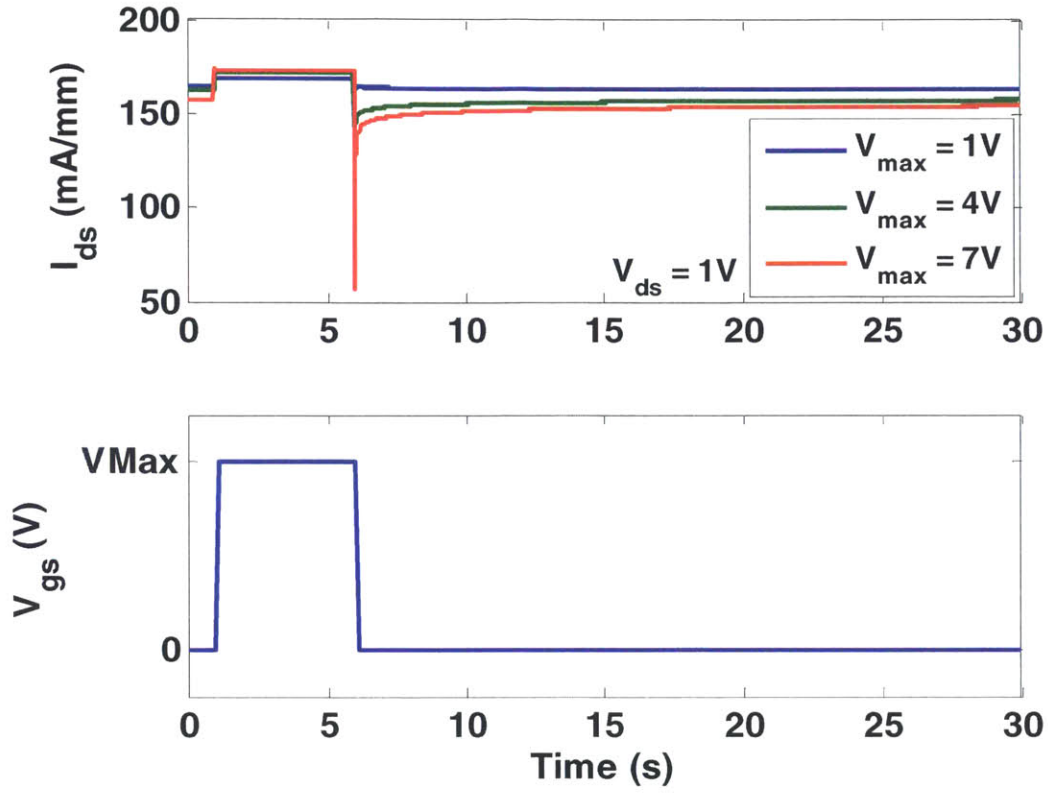


Figure 2-17: Illustration of sampling measurements. $V_{gs} = V_{max}$ for 5 s after 1 s has passed. The measured device has an Al_2O_3 gate dielectric and therefore mobile ions do not drift.

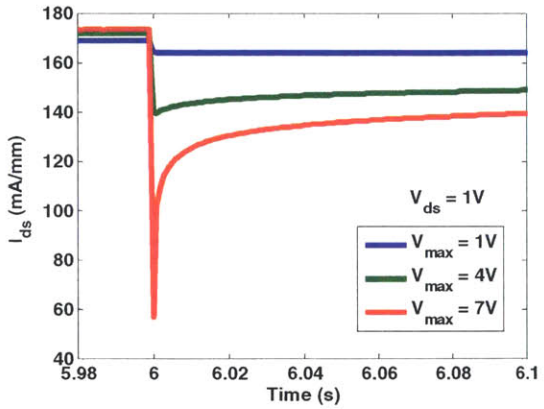


Figure 2-18: Sampling measurement immediately after transition from $V_{gs} = V_{max}$ to $V_{gs} = 0V$ for Al_2O_3 device with $V_{ds} = 1V$. As expected, when device is subjected to higher V_{max}, the current at $V_{gs} = 0V$ is lower due to electron trapping.

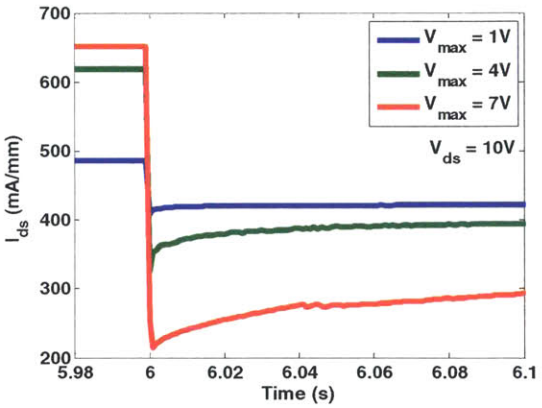


Figure 2-19: Sampling measurement immediately after transition from $V_{gs} = V_{max}$ to $V_{gs} = 0V$ for Al_2O_3 device with $V_{ds} = 10V$. Despite the higher temperature in the channel caused by the larger power dissipation at $V_{ds} = 10V$, mobile ions do not drift in Al_2O_3 and therefore the current drops with larger V_{max} values.

Figure 2-18 and Figure 2-19 show the evolution in current seen in transistors with an Al_2O_3 gate dielectric after applying positive gate biases ranging from 1V to 7V for a drain bias of 1V and 10V

respectively. The power dissipation when a drain bias of 10V is applied is greater than when a drain bias of 1V is applied and as a result, the channel temperature is greater with the increase in drain bias. As seen in Figure 2-18 and Figure 2-19, applying a higher V_{max} bias on the gate results in greater electron injection, which in turn causes the current to drop. This drop in current is independent of the drain bias.

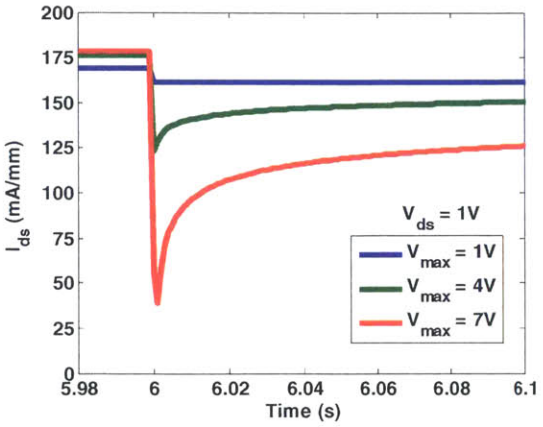


Figure 2-20: Sampling measurement immediately after transition from $V_{gs} = V_{max}$ to $V_{gs} = 0V$ for HfO_2 device with $V_{ds} = 1V$. As expected, when device is subjected to higher V_{max}, the current at $V_{gs} = 0V$ is lower due to electron trapping. Even though this sample has mobile ion contamination, the dissipated heat is low enough to not have a rise in current.

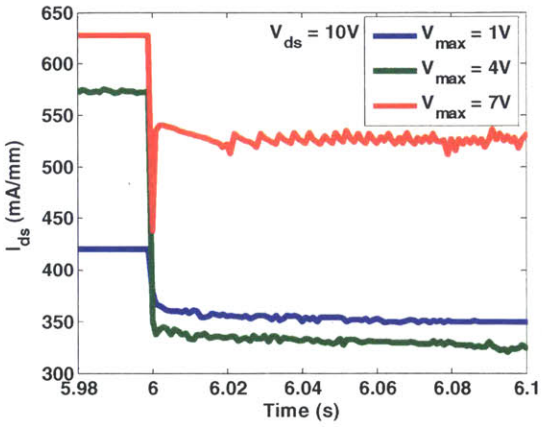


Figure 2-21: Sampling measurement immediately after transition from $V_{gs} = V_{max}$ to $V_{gs} = 0V$ for HfO_2 device with $V_{ds} = 10V$. This sample is contaminated with mobile ions and therefore when $V_{max} = 7V$, the electric field causes the mobile ions to drift away from gate. This causes an increase in current in contrast to Figure 2-20 where the current drops with increasing V_{max}.

However, with transistors with a HfO_2-based gate stack contaminated with mobile ions, the transient behavior as a function of drain bias is different. When the drain voltage is equal to 1V, the change in current as a function of the maximum gate voltage follows the same trend as the Al_2O_3 device as seen in Figure 2-20. When the drain bias is equal to 10V, the channel temperature gets large enough to cause mobile ions to move. The resulting movement of mobile ions away from the gate metal induces more carriers in the 2-DEG which in turn causes the current to *increase* when a gate voltage of 7V is applied as seen in Figure 2-21.

Summary

In summary, mobile ion contamination has been identified as a source of threshold voltage instability and charge distortion in GaN based MIS-HEMTs and MIS devices. Bias temperature stress measurements can be used with MOS devices that use gate dielectrics like $SiO_2$and HfO_2 which allow mobile ions to drift. Pyrex-based glassware was identified as a culprit for contamination and by using semiconductor grade glassware for processing devices, mobile ion contamination was almost eliminated.

Chapter 3 Developing a Gate First Process

This chapter is focused on looking at the feasibility of processing GaN based devices using a CMOS compatible process. First, the possibility of metallic contamination from GaN was studied by performing TXRF measurements. Then, once GaN wafers were deemed to be acceptable for the CMOS ALD tool, a low temperature ohmic contact process was developed to allow for a gate first process.

GaN contamination study

There are two ALD systems at MIT. The Oxford Instruments Flex-AL is dedicated for CMOS processing while the Cambridge Nanotech Savannah 200 system is used for processing samples that may have been Au contaminated. While the Cambridge Nanotech ALD is more than adequate for many applications, there are several key advantages for using the Oxford Flex-AL ALD tool [42]. First, due to the fact that it is a CMOS front end tool, all samples that are processed are required to either be RCA cleaned [43],[44] or cleaned by piranha. These requirements decrease the likelihood of mobile ion contamination in the tool. Second, the Oxford Flex-AL has a load lock and a lower base pressure (5×10^{-6} Torr for the Oxford ALD vs. 1×10^{-4} Torr for the Cambridge Nanotech) which again reduces the likelihood of contamination from atmosphere. Third, the Oxford Flex-AL has a plasma source which allows for the deposition of higher quality metal nitride films and for plasma pretreatments.

CMOS processing requires strict contamination controls. In addition to mobile ion contamination, heavy metals like Au and Fe serve as deep level traps and can cause the carrier lifetime in silicon to degrade readily. Fe is particularly bad for CMOS devices because it lowers the carrier lifetime, it diffuses very quickly in Si wafers and can also cause premature SiO_2 gate oxide breakdown [45]. Ga is a p-type dopant for Si and thus Ga contamination from GaN must also be monitored and controlled [21].

However, these contaminants are commonly found in compound semiconductor processing unless special care is taken to avoid them. For example, Au is commonly used in ohmic contacts for AlGaN/GaN HEMTs [46],[47]. Fe is used in growing semi insulating GaN in order to reduce buffer leakage and given that Fe growth has a memory effect where, it's very easy to end up with Fe on the surface [48],[49]. Therefore, when introducing GaN into tools intended for CMOS processing, it is important to ensure that the GaN substrate does not end up contaminating CMOS tools. One way to combat this is to grow least 1 µm of GaN after the growth of intentionally Fe doped GaN stops as seen in a GaN wafer with intentional Fe doping (Figure 3-1). The wafer that was used for these experiments had a 3 µm thick GaN buffer as seen in Figure 3-2. As a result, the Fe concentration in the wafer in the top 3 µm of epitaxy is below the TXRF detection limit of 10^{15} atoms/cm^3 as seen in Figure 3-3.

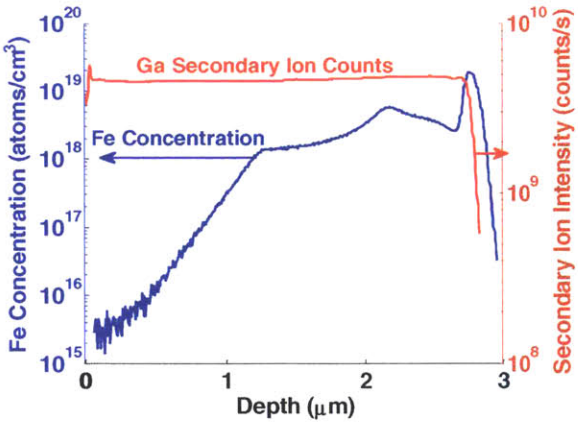


Figure 3-1: Fe concentration vs. Depth for AlGaN/GaN/sapphire wafer from another source. Fe doping was stopped at 1.1 µm and it took 1.1 µm for Fe concentration to go down to around 10^{15} cm^{-3}. Gallium secondary ion counts help indicate where the GaN epitaxy begins as a function of depth.

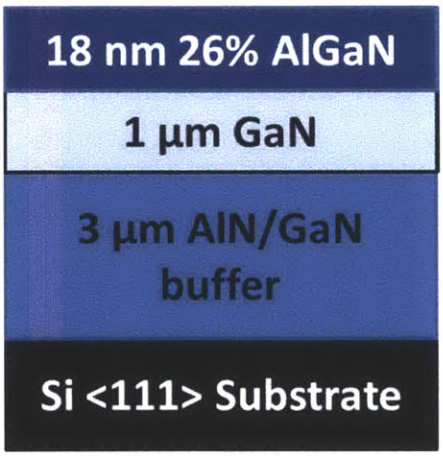


Figure 3-2: Schematic showing wafer structure used for TXRF contamination study.

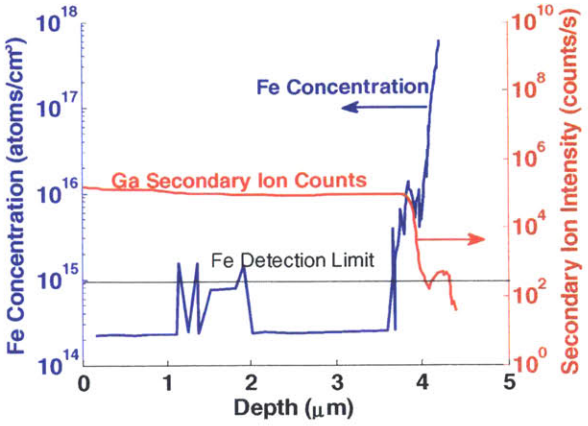


Figure 3-3: Fe concentration vs. Depth for AlGaN/GaN wafer used in TXRF contamination study. Gallium secondary ion counts are used to indicate the depth of the GaN epi layer. Fe concentration peaks at the nucleation layer between 3.5 and 4.2 μm

These contaminants have been monitored by a variety of techniques. One common method is to measure the lifetime of carriers in Si capacitors [50]. Metals like Fe and Au induce deep level traps which cause the lifetime of minority carriers to get greatly reduced. However, fabricating capacitors exposes the wafer to multiple tools and thus the source of contamination can get obscured.

A more direct method is to perform Total X-Ray Reflection Fluorescence (TXRF) measurements on bare Si wafers. TXRF is a very sensitive technique that can be used to detect contaminants on the order of 10^{10} cm^{-2} on the top surface. This also allows for simply loading monitor Si wafers into a tool before and after a potentially contaminating wafer or process has been run. Any different in contamination levels between the Si wafers loaded before and after the potential source of contamination can be directly attributed to the contamination source.

In order to assess the possibility of GaN contaminating the Oxford FlexAl ALD, an experiment was conducted where first an RCA cleaned p-Si wafer [43] was loaded into the ALD and was kept at 350°C for 30 min. Then, an AlGaN/GaN on Si wafer (with schematic shown in Figure 3-2 and Fe doping

profile shown in Figure 3-3) was cleaned with piranha and HCl:DI before loading into the ALD tool. Then, the wafer was subjected to a 100W, 15 mTorr, N_2 plasma for 1 min before letting the wafer sit at 350°C for 30 min. Finally, a third RCA cleaned p-Si wafer was loaded into the ALD and allowed to bake for 30 min to allow for time for any released contaminants to settle on the wafer surface.

Table 1. TXRF Results for W source measurements (units of 10^{10} atoms/cm^2).

C0DJA225	S	Cl	K	Ca	Ti	Cr	Mn	Fe	Ni	Cu	Zn
Wafer #1 ALD CONTROL											
Center	260±18	1460±90	<5	<5	<1.0	<0.5	<0.3	0.9±0.2	<0.3	6.4±0.5	126±8
30,-30	270±19	1300±80	<5	<5	<1.0	<0.5	<0.4*	0.9±0.2	0.7±0.2	9.3±0.6	147±9
-30,30	260±18	1270±80	<5	<5	<1.0	<0.5	0.4±0.2	0.8±0.2	0.6±0.2	9±0.6	165±10
Wafer #2 ALD TEST											
Center	410±30	1260±80	<5	<5	<1.5	<0.5	<0.4	0.7±0.2	<0.3	<0.3*	3.7±0.3
30,-30	470±30	1100±70	<5	<5	<1.0	<0.5	<0.4	0.5±0.2	<0.3	0.5±0.2	4.1±0.3
-30,30	490±30	1060±60	<5	<5	<1.0	<0.5	<0.4	0.5±0.2	<0.3	0.5±0.1	5.6±0.4

* may be present near the detection limit

Table 2. TXRF Results for Mo source measurements (units of 10^{10} atoms/cm^2).

C0DJA225	As	Br	Ta	W	Ga	Ge	Sr	Y	Pt	Au	Pb
Wafer #2 ALD TEST											
Center	<3	8±1.6	<2	<2	<4	<3	<2	<3	<1.4	<1.4	<1.2
30,-30	<4	13±2	<3	<3	<5	<4	<3	<3	<1.8	<1.8	<1.5
-30,30	<3	10.5±1.8	<3	<2	<4	<4	<3	<3	<1.7	<1.6	<1.4

Table 1: TXRF results for Si wafers before and after the GaN wafer was loaded into the ALD tool. The Si wafer loaded before the GaN wafer is referred to as "Wafer# 1 ALD CONTROL" while the Si wafer loaded after the GaN wafer is referred to as "Wafer #2 ALD TEST". TXRF report was written by Evans Analytical Group.

As can be seen above in Table 1, there was no meaningful change in contaminants such as Fe and Au between the wafer loaded before the GaN wafer (referred to "Wafer #1 ALD CONTROL") and the wafer loaded after the GaN wafer (referred to "Wafer #2 ALD TEST") . For example, the measured Fe concentration on the wafer that was loaded before the GaN wafer was around 8×10^9 to 9×10^9 cm^{-2} and the measured Fe concentration on the post GaN wafer was from 5×10^9 to 7×10^9 cm^{-2}. In addition, the level of Ga contamination on the wafer after the GaN wafer had been loaded was in the 10^{10} range, which has been deemed an acceptable level of contamination [21]. Based on these results, these GaN wafers were permitted to be introduced into the CMOS Oxford ALD tool.

Developing Low Temperature Ohmic contacts

Metalized wafers are not allowed in CMOS front end tools like oxidation furnaces or ALD tools. Therefore, a gate first process is the only process that can be run through the Oxford ALD tool. However, this means that the gate stack will be subjected to the ohmic anneal process. While a high temperature gate first process has been demonstrated in the past, it does cause some degradation in the gate stack. Therefore, ideally, the ohmic anneal should be limited to 600°C or below.

There are several aspects that need to be optimized in order to successfully form ohmic contacts in a reproducible manner. First, the annealing temperature and time needs to be carefully selected. Second, many low temperature ohmic contact schemes involve recessing the AlGaN layer and the recess depth needs to be optimized [51],[21]. Nonuniform recessing can cause unexpectedly high contact resistances. Third, given that the Ti/Al ohmic metals are sputtered, it is possible to perform an Ar clean on the etched GaN surface in-situ before the Ti/Al is deposited. The impact of this Ar clean on contact resistances needs to be studied. Fourth, the ratio of Ti/Al needs to be optimized for getting reproducible ohmic contacts. A low temperature ohmic contact flow is illustrated below in Figure 3-4. A SiO_2 interlayer dielectric (ILD) layer is first deposited and patterned. Then, the AlGaN barrier is recessed through completely in regions where the ohmic contacts will be deposited. Ti/Al metal is sputtered everywhere and then is etched by using a Cl_2 based etch recipe. The SiO_2 ILD layer is important for protecting the AlGaN/GaN heterostructure during this etch step. Finally, the sample is annealed in order to form an ohmic contact.

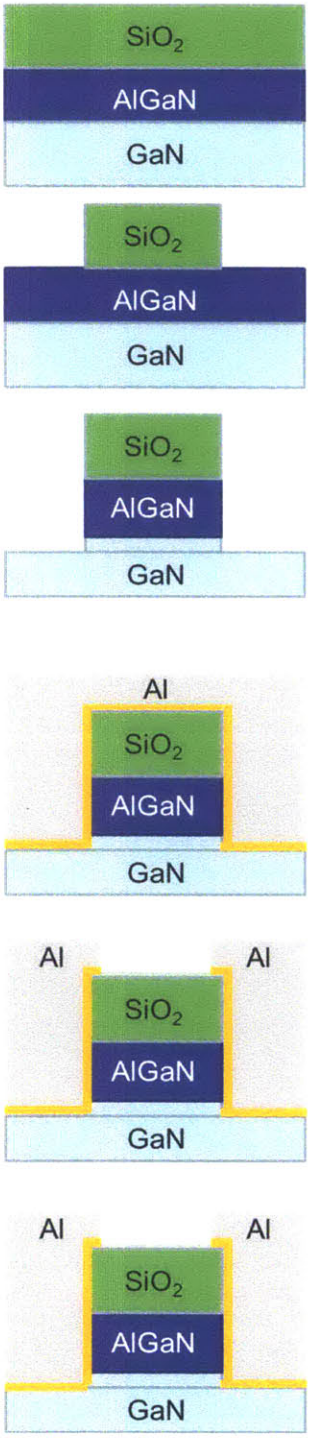


Figure 3-4: Process flow for fabricating low temperature ohmic contacts.

It has been widely reported that it is necessary to form nitrogen vacancies in order to form ohmic contacts [52]. Nitrogen vacancies serve as electron donors which dope the underlying

semiconductor. One method to induce nitrogen vacancies has been to damage the GaN surface with a plasma and the resulting nitrogen vacancies dope the semiconductor enough to allow for ohmic contacts to form without alloying the metal [52],[53],[54]. However, this is a very sensitive process and inducing too much damage can prevent ohmic contacts from forming [52]. An easier way is to alloy a reactive metal on top of GaN. For example, Ti reacts with the underlying GaN in order to form TiN and the resulting leaching of N from the GaN to form TiN has been attributed as the key source of nitrogen vacancies. The enthalpy of formation for TiN is -336 kJ/g as opposed to -110 kJ/g for GaN and thus TiN formation is thermodynamically favored [52]. At the same time, Ti and Al form intermetallic compounds and thus there is a trade off with the thickness of the Ti layer. Depositing a Ti layer that is too thin causes all the Ti to be consumed by the Al in the ohmic metal stack and thus prevents the formation of the TiN intermetallic layer. Having a Ti layer that is too thick poses separate issues since the Ti aggressively reacts with the underlying GaN.

The first experiment involved studying the impact of annealing temperature on the contact resistance. For this experiment, the targeted recess depth was 30 nm in order to remove all the AlGaN. The recess was done by using a $SiCl_4$ based inductively coupled plasma (ICP) etch [55]. Following the recess, 20 nm Ti and 500 nm of Al were deposited by sputtering. The ohmic metals were patterned by using a BCl_3/Cl_2 dry etch where the SiO_2 ILD was key for protecting the underlying device from the Cl_2 based plasma. Finally, the samples were annealed anywhere from 500°C to 600°C for 5 min. Figure 3-5 shows that an anneal temperature range between 500°C and 550°C is optimal for forming ohmic contacts with Ti/Al metallurgies.

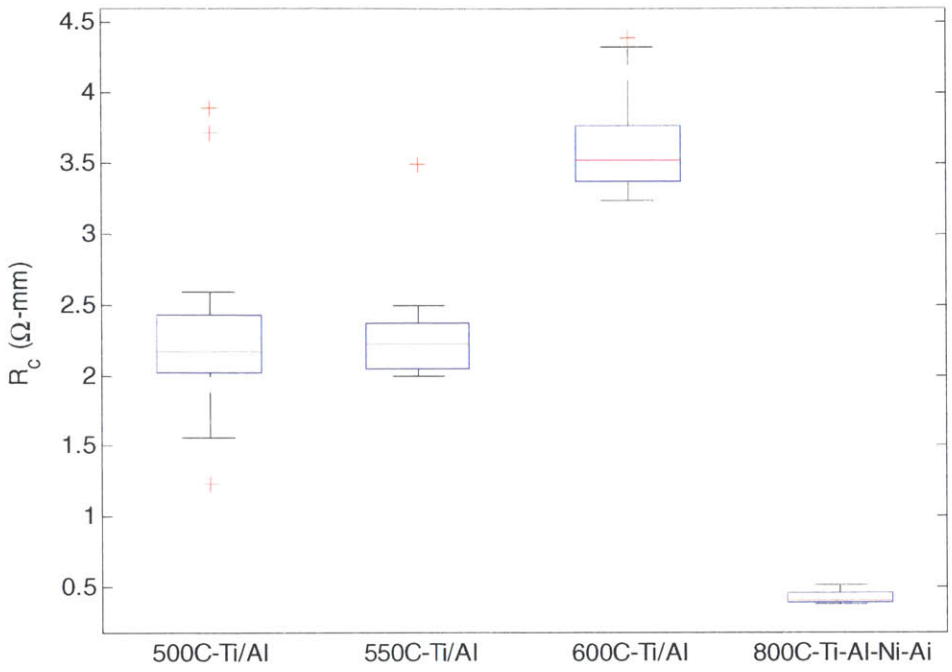


Figure 3-5: Comparison of ohmic anneal temperature on the R_c of Ti/Al ohmic contacts. As a reference, the contact resistance of a conventional Ti/Al/Ni/Au ohmic contact is also included. While the Ti/Al based contact resistances are high, they are ohmic contacts and are sufficient for testing capacitors and long gate transistors. 10-15 TLM structures were measured per sample in order to extract trends.

Given that the AlGaN layer needs to be recessed through, it is important to have information about the uniformity of the ohmic recess etch. In order to measure the thickness of the AlGaN layer across the wafer in an efficient manner, a bare sample was processed and AlGaN/GaN Schottky diodes were fabricated. CV measurements were done in order to measure the thickness of the AlGaN layer. Anywhere from 100-150 capacitors were measured per sample, which have an area of around 3.2-3.5 cm^2, in order to measure the spatial variation across each sample. First, a sample without any recessing was fabricated in order to serve as a reference. Figure 3-6 shows the variation in measured capacitance across the unrecessed sample. This sample from the edge of the wafer and therefore, the bottom 5 mm was excluded when determining the etch rates (Figure 3-7).

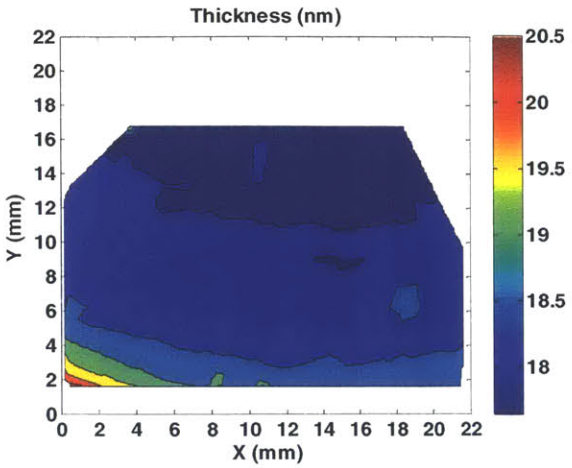


Figure 3-6: Contour Map of unrecessed AlGaN/GaN sample. The bottom 5 mm of the same is from the edge and thus is thicker.

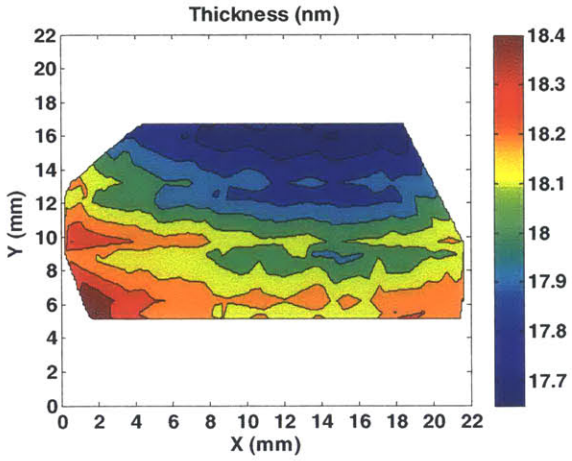


Figure 3-7: Contour map of unrecessed AlGaN/GaN sample with the edge excluded. The mean thickness of the sample is 18.1 nm

Then, samples were processed where the AlGaN/GaN heterostructure was recessed in order to study the uniformity of different recess conditions. Given that recessing AlGaN causes a reduction in carrier concentration, it is important to ensure that the access region of the capacitors is not recessed as well. Therefore, as shown in Figure 3-8, there was a 3 µm offset between the edge of the Schottky metal and the recessed region. When extracting the depth of the etched region, the capacitance of the unetched ring was taken into account as shown in Figure 3-9. The measured capacitance was then converted to the remaining AlGaN thickness for different etch conditions as shown in Figure 3-10.

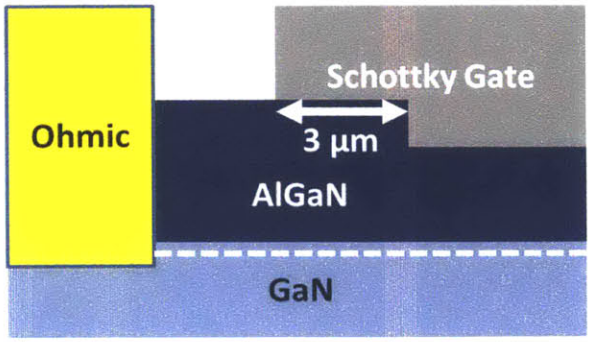


Figure 3-8: Schematic of recessed Schottky Diode structures. In order to prevent the access region from getting resistive, the recessed region is offset by 3 µm from the gate metal edge. Schottky diode size was 100 µm X 100 µm while recessed region was 94 µm X 94 µm

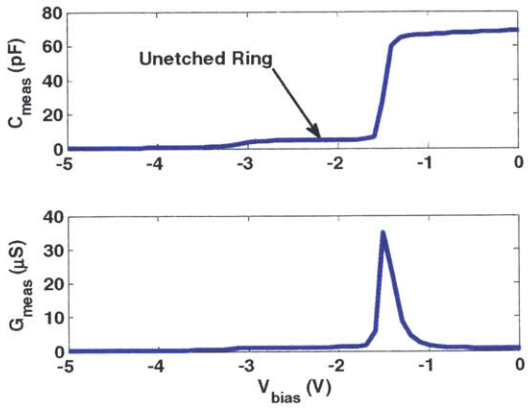


Figure 3-9: CV and GV measurement for recessed AlGaN/GaN Schottky diode. The unetched ring has a V_{th} of around -3.25V and so the measured CV curve shows a first step between -3.2V and -1.7V where only the unetched ring is on. Then, the etched region goes into accumulation and the measured capacitance reflects the capacitance of both the etched and unetched region.

Etch Condition	Etch Time	Median Thickness	Etch Rate (nm/min)
No etch (no edge)		18.0 nm	
ICP-50W,RF-20W	420s	12.9 nm	0.73
ICP-50W,RF-50W	70s	10.8 nm	6.17
ICP-75W,RF-35W	90s	14.0 nm	2.67

Table 2: Summary of different etch conditions and calculated etch rates

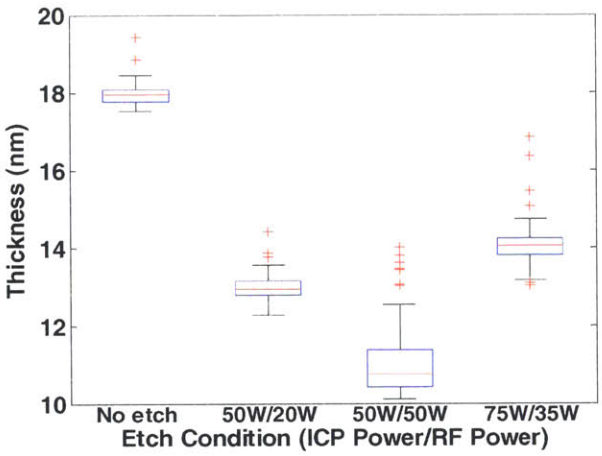


Figure 3-10: Thickness of AlGaN after different etch conditions. Higher etch rates generally resulted in more non-uniformities

Figure 3-11 is a spatial map of the sample that had been etched using the ICP-50W, RF-20W power setting. The edges of the sample were etched faster than the center. This "bullseye" effect is a common issue in plasma etching [56] and has been attributed to a greater concentration of etch species at the edge of the sample [57],[58].

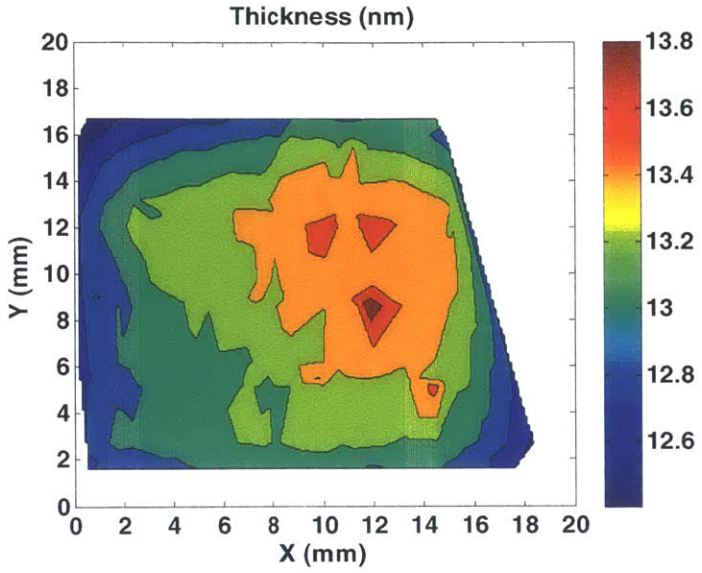


Figure 3-11: Contour plot showing etching nonuniformities across the sample for the ICP-50W, RF-20W etching condition. The edges etch faster than the center of the sample.

If the purpose of this recess etch was to perform a gate recess, the nonuniformity seen would pose a technical challenge since non-uniformity in the AlGaN thickness results in threshold voltage variation. However, given that the objective of this etch step is to recess the AlGaN completely, this level of nonuniformity should not pose a problem as long as there is some overetching done to ensure that all the AlGaN is recessed.

The next set of experiments dealt with the impact of Ar plasma precleans on the ohmic contact formation. Ar based plasma has been used for etching through native oxide in silicon devices [59], [60]. Sputtering tools typically allow for performing a plasma preclean and given that some damage has been reported to facilitate the formation of ohmic contacts, it is reasonable to expect some improvement. In addition, an Ar clean might help etch some native oxide that would have formed between the time when wet HCl:DI dip is completed and the AlGaN/GaN sample is loaded into the load lock. Therefore, two samples were fabricated where the AlGaN/GaN stack was recessed 30 nm. Then, one sample had a 5 min, 1.5 mTorr, 35W Ar plasma clean while the other sample did not have a plasma clean. As seen in

Figure 3-12, the contacts that had been precleaned with the Ar plasma exhibit Schottky characteristics while the non-precleaned samples are ohmic.

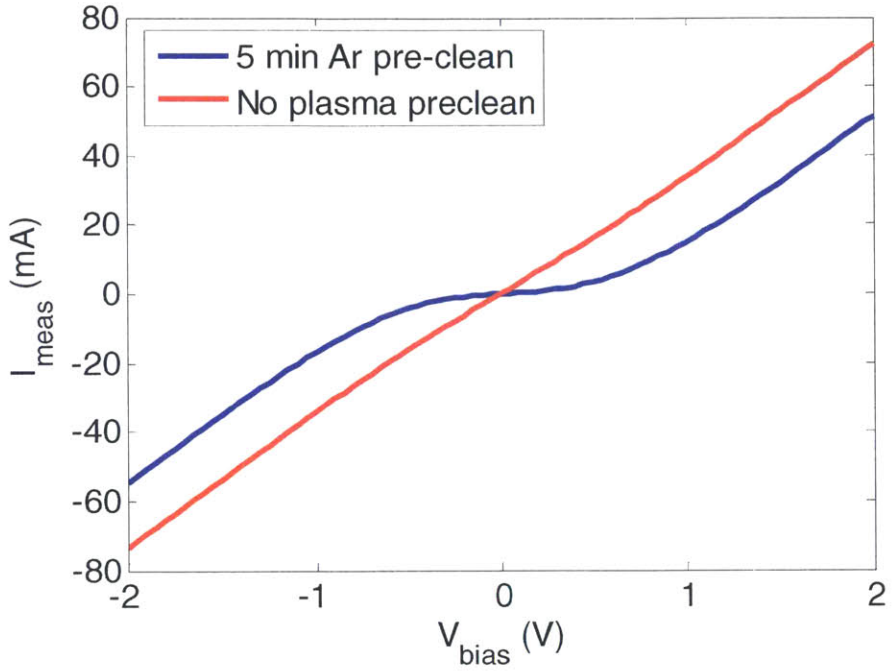


Figure 3-12: Differences in I_{ds} vs. V_{bias} for circular TLM structures with a gap of 30 µm. Both samples were annealed at 600°C for 5 min and were recessed for 30 min with a target depth of 30 nm

In order to study the origin of the degradation in ohmic contacts, XPS studies of AlGaN/GaN samples were conducted where the samples were either just acid cleaned, acid cleaned and recessed with the $SiCl_4$ plasma used for ohmic recessing and finally acid cleaned, recessed and subjected to a 5 min Ar plasma clean in the sputtering tool . The objective is to see the change in material composition as a function of these processes. It would be ideal to calculate the Ga ratio to N ratio from XPS measurements. However, when using an Al Kα X-ray source, the presence of the resulting Ga LLM Auger line in the proximity of the N1s peak makes it difficult to deconvolve the two signals [61]. Therefore, it is difficult to accurately determine the N concentration in GaN without careful calibration. However, any reduction in nitrogen concentration will result in an increase in oxygen concentration since dangling Ga bonds will bond with ambient oxygen in the air [53].

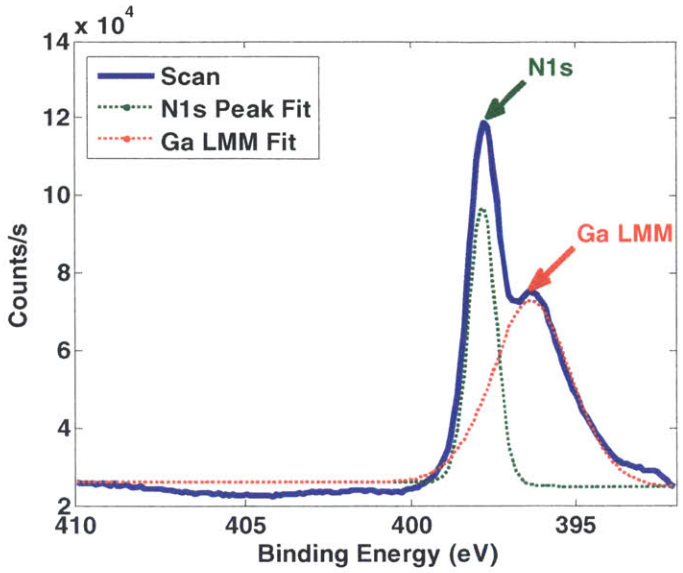


Figure 3-13: N1s scan for unrecessed sample. The presence of the Ga LMM line makes it difficult to determine the contribution of the N1s line to the measured signal which in turn adds to the ambiguity of the measurement.

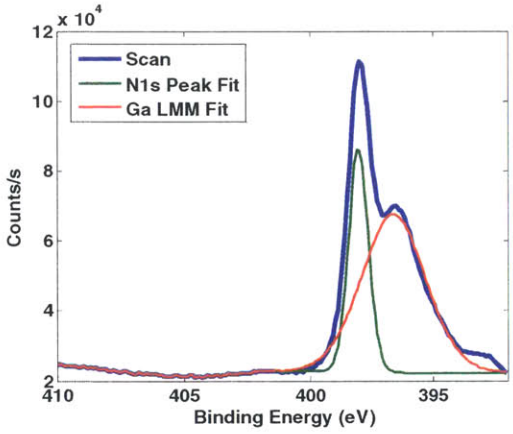


Figure 3-14: N1s scan for recessed sample. N1s peak is more pronounced before the Ar clean.

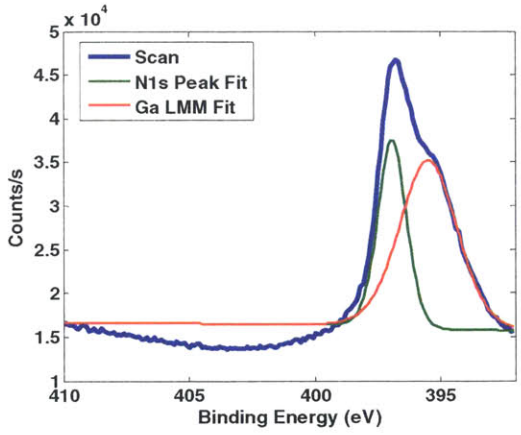


Figure 3-15: N1s scan for recessed sample with 5 min Ar clean. N1s peak is less pronounced after the Ar clean. This is indicative of a reduction in nitrogen on the GaN surface.

Figure 3-13 and Figure 3-14 show that the N1s scans of the unrecessed and recessed samples without the Ar clean are very similar. However, as seen in the contrast between Figure 3-13 and Figure 3-15, performing an Ar sputter clean causes the N1s peak to get smaller. When the sample is bombarded with Ar plasma, it is easier for the liberated N atoms from GaN to form N_2 and to get pumped away. In contrast, the remaining Ga atoms are much heavier and thus they remain on the

surface. When the sample is then unloaded for performing XPS measurements, the dangling Ga atoms oxidize and thus the oxygen content increases on the surface.

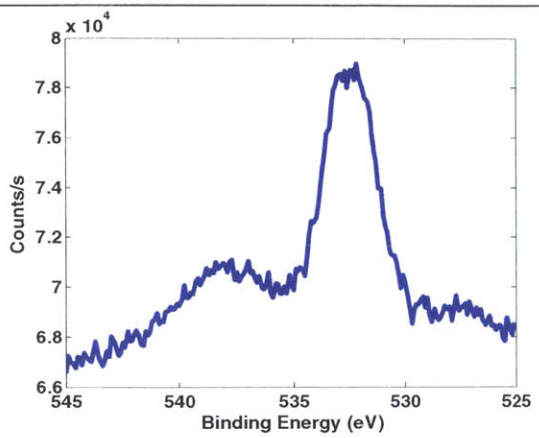


Figure 3-16: O1s peak for unrecessed sample

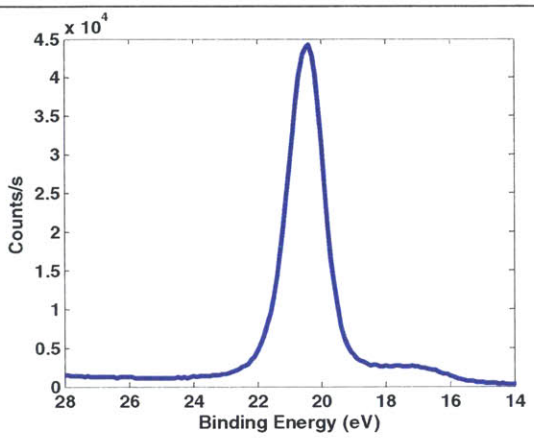


Figure 3-17: Ga3d peak for unrecessed sample

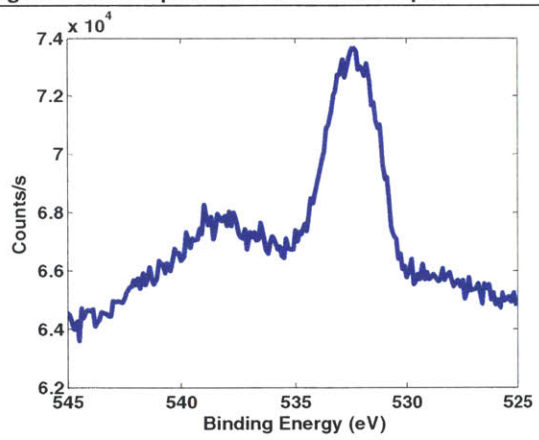


Figure 3-18: O1s peak for recessed sample

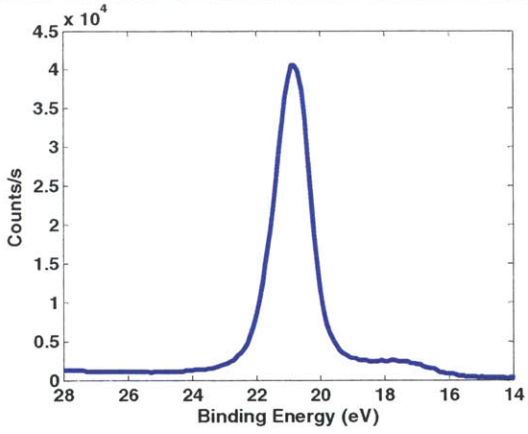


Figure 3-19: Ga3d for recessed sample

Both the recessed and unrecessed samples have similar Ga3d and O1s scans in terms of counts and also in terms of the chemical bond states as seen in Figure 3-16 to Figure 3-19. On the other hand, the sample exposed to Ar plasma in the sputtering tool looks very different. First of all, there is no secondary peak at around a binding energy of 540 eV. Secondly, the O1s peak is a lot more prominent in the samples that had been exposed to the Ar plasma (Figure 3-20).

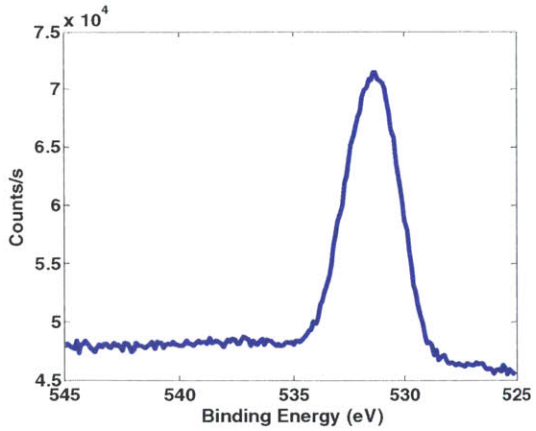


Figure 3-20: O1s for recessed + Ar cleaned sample. Note that the O1s peak is a lot more prominent than the O1s peaks for the samples that had not been exposed to the Ar plasma.

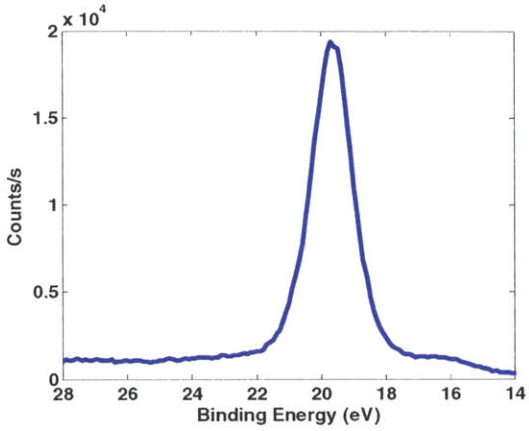


Figure 3-21: Ga3d for recessed + Ar cleaned sample

By calculating the areas of the peaks and normalizing with respect to the relative sensitivity factors, it is possible to look at the ratio of Ga to O. The sample that has been subjected to the Ar plasma has the lowest Ga:O ratio of 1.08 while the other two samples have a Ga:O peak ratio of greater than 6.5. This is indicative of a very significant oxidation of the sample that had been exposed to the Ar plasma

Sample	Ga Raw Area	RSF	O Raw area	RSF	Ga:O ratio
Unrecessed	63248.1	1.09	25446.0	2.93	6.68
Recessed	57560.8	1.09	23465.8	2.93	6.59
Recessed + Ar Plasma	31553.2	1.09	78661.7	2.93	1.08

Table 3: XPS Summary of Ga:O ratios for different sputtering conditions

Summary

In summary, TXRF contamination studies showed that processing GaN wafers through the CMOS compatible ALD tool did not contaminate the tool as evidenced by the absence of contaminants such as iron and gallium found on silicon wafers processed after the GaN wafer. Then, in order to facilitate a gate first process, Ti/Al based low temperature ohmic contacts were developed for the AlGaN/GaN

HEMT. While the optimized ohmic contact resistance is relatively high, it is low enough for performing CV measurements and for characterizing long gate length annular FETs.

Chapter 4 Gate First Process vs. Ohmic First Process

In this chapter, the difference between gate first and ohmic first processing is explored. First, the process flows will be described. Then, the two samples will be compared with respect to high bias CV measurements. Following that, the role of cleaning in explaining the difference between the gate first and the ohmic first samples will be studied.

Process Flows

Both gate first and ohmic first samples were processed using AlGaN/GaN/sapphire HEMT samples grown by Dr. Richard Molnar of MIT Lincoln Laboratories. The mask was designed so that device isolation was not necessary. This necessitated the use of circular TLM structures, annular FETs and ring capacitors. The basic schematics of the process flow used to fabricate the gate first samples can be found in Figure 4-3

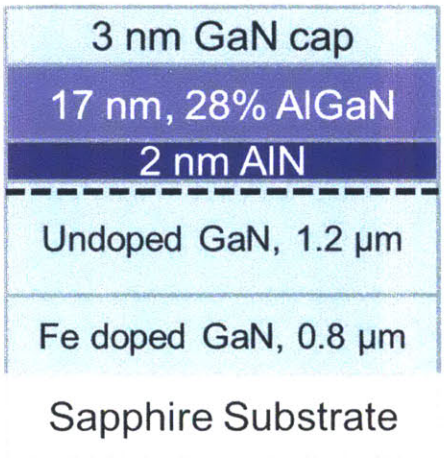
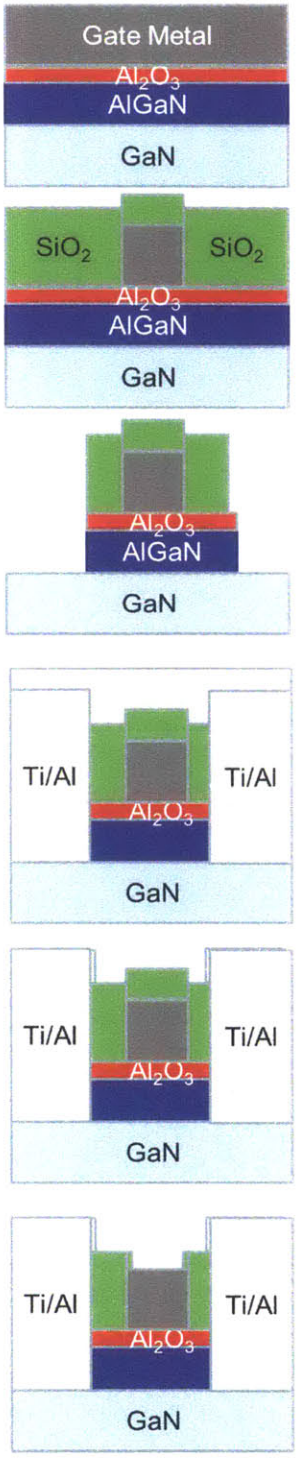


Figure 4-1: HEMT structure used for processing gate first and ohmic first samples

Figure 4-2: (a) Annular FET structure with L_g = 50 µm. (b) 100 X 100 µm capacitor structures used for CV measurements



1) After wet cleaning, deposit 20 nm Al_2O_3 by ALD. Sputter Mo gate metal

2) Pattern Mo with SF_6 dry etch. Selective etch to Al_2O_3 Deposit 200 nm thick SiO_2 interlayer dielectric (ILD) layer.

3) Open ILD layer. Recess through AlGaN. Low temperature ohmics require recessing

4) Sputter 20 nm Ti/500 nm Al ohmic metals. Sputtering key to get conformal coverage for sidewalls

5) Etch Ti/Al ohmic metals with BCl_3/Cl_2 dry etch. SiO_2 ILD layer protects underlying device from metal etch. Anneal ohmic metal to form ohmic contacts.

6) Etch ILD on top of gate contact in order to land probes on gate for electrical testing.

Figure 4-3: Gate First Process flow

The starting substrate for the gate first process is shown in Figure 4-1. After the pieces were cleaved, the samples were dipped in H_2SO_4:H_2O_2 (3:1) (piranha mixture) for 10 min. This clean helps clean organic contamination and some metallic contamination. It has also been reported to yield good

results for Al_2O_3/nGaN capacitors due to the resulting reduction in surface roughness [62]. Then, after the sample was rinsed in DI water for 2 min, the sample was dipped in HCl:DI (1:3) for 1 min. The purpose of this clean is to etch any surface oxide that might have grown after the piranha clean [63]. It is also intended to remove any sodium ion contamination that might be present on the sample [35].

Following the clean, the samples were loaded into the Cambridge Nanotech ALD tool with the chuck temperature set to 250°C. Before the samples were loaded and cleaned, a piranha cleaned new p-Si wafer was loaded into the chuck of the ALD chamber and 20 nm of Al_2O_3 was deposited in the chamber. The Al_2O_3 helps blocks any mobile ions that might be present in the tool while using a new piranha cleaned wafer as the piece holder also helps ensure that the chamber is clean. Then, once the sample is loaded into the chamber, the sample is heated up to 300°C and held at 300°C for 10 min in order to desorb any water that might be present and to stabilize the chuck temperature. After the temperature stabilization, the sample is subjected to 3 min of O_3 and then the ALD deposition starts. The role of ozone in preparing the sample will be discussed later. The two precursors for the deposition was trimethylaluminum (TMA) and DI water and the deposition was DI first. The deposition conditions are detailed in Table 4

Chuck Temperature	300°C
N2 Flow	20 sccm
DI Pulse	0.02s
Purge	10s
TMA Pulse	0.02s
Purge	10s
Repeat	180 cycles-Target thickness is 20 nm

Table 4: Al_2O_3 Deposition Recipe

Following the ALD deposition, the sample was loaded immediately in the sputtering tool in order to sputter Mo. The gate was sputtered instead of patterned by liftoff since exposing Al_2O_3 to TMAH containing developers causes Al_2O_3 to etch. This was verified experimentally by dipping Al_2O_3 in AZ422

and OCG 834, the TMAH containing developers used for developing positive and negative photoresists used in TRL, as shown in Figure 4-4 . Mo was chosen as a gate metal for the following reasons

- Like tungsten (W) and unlike nickel, molybdenum etches readily in an SF_6 plasma. Using an SF_6 plasma is desirable since it is very selective to Al_2O_3 [64].
- Molybdenum etches much slower than tungsten in nanostrip, a sulfuric acid based cleaning solution that is used to clean organic contamination. The etch rate of molybdenum is slow enough to allow for using a nanostrip clean. This is key for ensuring cleanliness on the sample after lithography steps.
- Like nickel, molybdenum has a relatively large work function of 5 eV [65].

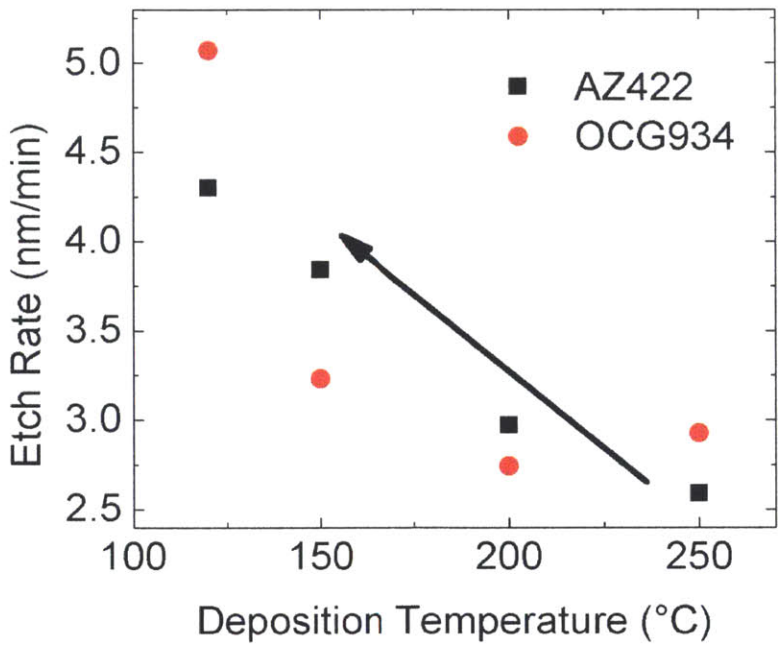


Figure 4-4: Etch rates of Al_2O_3 deposited by ALD at deposition temperatures ranging from 100°C to 250°C. Both developers contain TMAH and etch Al_2O_3.

100 nm of Mo was sputtered using an AJA International ATC-1800 (referred to as the AJA-TRL) tool. The deposition conditions for the Mo deposition are listed below in Table 5.

Ar flow	35 sccm
Deposition Power	200 W
Deposition Pressure	1.5 mTorr
Deposition Rate	1.8 A/s
Time	10 min

Table 5: Deposition conditions for sputtered Mo

Then, gates were patterned by performing photolithography and by etching in an SF_6 based plasma. Following the gate patterning, a 200 nm thick SiO_2 interlayer dielectric (ILD) layer was deposited by PECVD. The purpose of the ILD layer was to protect the core device from subsequent etching steps. The ILD layer was etched by a BOE 7:1 wet etch in the contact regions and then the AlGaN layer was recessed using the $SiCl_4$ ICP etch described in Table 2. Given that the $SiCl_4$ ICP etch has been reported to leave behind some SiO_2 residual films [66], the sample was dipped in 50:1 DI:HF for 30s, rinsed in DI for 2 min, dipped in HCl:DI (1:3) for 1 min and rinsed in DI for 2 min. The dilute HF dip was intended to remove residual SiO_2 layer without etching the SiO_2 ILD layer [64]. Then, 20 nm Ti/500 nm Al ohmic contacts were sputtered and then patterned by using a BCl_3/Cl_2 dry etch. After the ohmic patterns were etched and the photoresist was stripped with a combination of a solvent clean and two minute nanostrip® dip, the sample was annealed at 550°C for 5 min given that this annealing condition was identified as being optimal (Figure 3-5). Finally, the ILD layer was etched open by using buffered oxide etch (BOE 7:1) on top of the gate contact in order to be able to probe it.

The ohmic first process flow was simpler because the ohmic metals were lifted off as opposed to sputtered and etched. This eliminated the need for an ILD layer. In addition, given that the ohmic anneal was performed at 800°C, it was not necessary to perform an ohmic recess. Figure 4-5 shows a schematic of the ohmic first process flow.

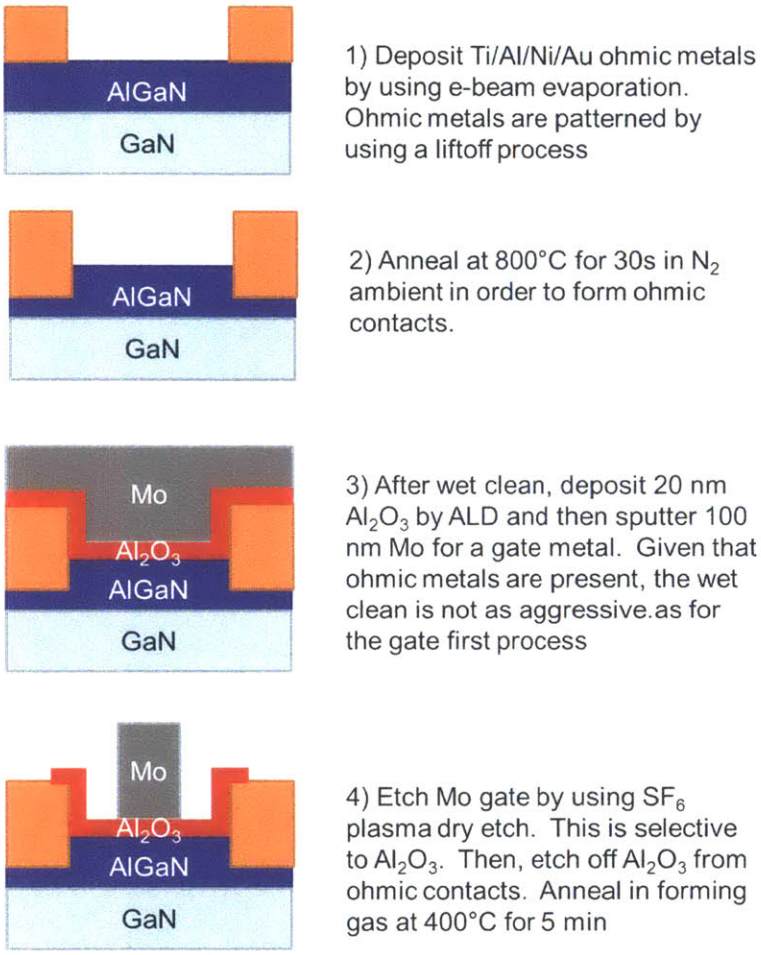


Figure 4-5: Ohmic first process flow

The same wafer, as described in Figure 4-1, that was used for the gate first process flow was also used for the ohmic first process flow. After the sample was cleaved, it was cleaned by dipping in piranha for 10 min, rinsing in DI for 2 min, dipping in HCl:DI (1:3) for 1 min and rinsing again in DI for 2 min. Then, photolithography was done for doing ohmic metal liftoff and following a 5 min O2 ashing step and a 1 min DI:HCl dip, Ti(200 Å)-Al(1000 Å)-Ni(250 Å)-Au(500 Å) ohmic metals were deposited by e-beam evaporation. After the ohmic metals were lifted off, the sample was cleaned by performing a standard solvent clean consisting of sonication in acetone, methanol and isopropanol. However, the solvent clean is not enough to fully remove the residue as shown by the atomic force microscopy (AFM) scans of

a GaN substrate with photoresist that was stripped by a standard solvent clean (Figure 4-6 and Figure 4-7).

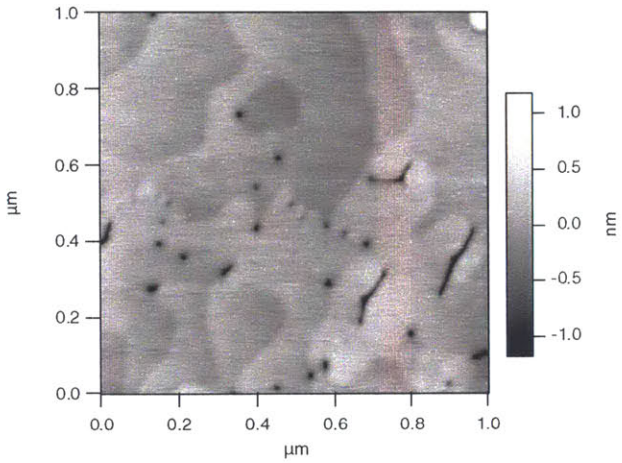


Figure 4-6: Bare AlGaN/GaN substrate before photoresist. AFM image courtesy of Dr. Yiqun Liu of Harvard University.

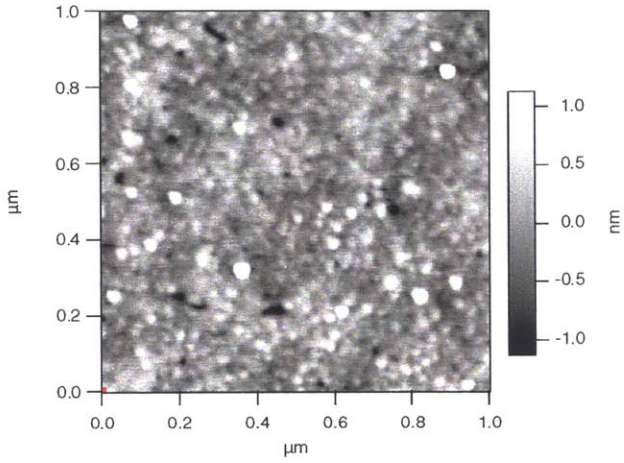


Figure 4-7: AFM scan of AlGaN/GaN surface after AZ422 image reversal resist was spun on, baked at 80°C to harden the resist as per standard processing protocol and then stripped by an acetone, methanol and isopropanol solvent clean. There is still a substantial amount of residue left behind. AFM image courtesy of Dr. Yiqun Liu of Harvard University.

In order to remove some of the remaining resist residue, the sample was dipped in nanostrip for 2 min. Given that nanostrip slowly etches Ni, the length of the nanostrip clean step was limited to 2 min. The sample was annealed at 800°C for 30s in an N_2 ambient in order to form ohmic contacts. Then, pre-ALD cleans were performed. Given that ohmic metals were already present on the sample, the pre-ALD cleans that are performed on the ohmic first sample were more limited in cleaning effectiveness. For example, it was not possible to perform a piranha clean on these samples. Therefore, the sample was dipped in nanostrip for 2 min, rinsed in DI for 2 min, dipped in HCl:DI (1:3) for 1 min and finally rinsed in DI for 2 min before loading into the ALD. Again, the nanostrip was intended to help remove organic contamination while the HCl:DI dip was intended to remove any mobile ion contamination and etch any remaining surface oxide. 20 nm of Al_2O_3 was deposited on the ohmic first

sample at the same time as the gate first sample and details of the ALD deposition conditions can be found in Table 4. Following the oxide deposition, the sample was loaded into the AJA-TRL sputtering tool in order to sputter 100 nm Mo. Deposition details are given in Table 5. The Mo gates were patterned by etching in an SF_6 plasma and then after the photoresist was stripped by a combination of a solvent clean and 2 minute nanostrip clean, the sample was annealed for 5 min at 400°C in a forming gas ambient.

High Bias CV Characterization

Capacitance voltage measurements were used in order to characterize the AlGaN/ Al_2O_3 interface for both the gate first and ohmic first samples. It is necessary to apply a large enough bias to inject carriers from the 2-DEG into the oxide-AlGaN interface [18],[67]. By varying the measurement frequency, it is possible to probe different trap levels and therefore, the frequency dispersion in high bias CV measurements is correlated to trapping. The emission time constant of electrons from interface state states is given by (1)[18]. τ is the emission time constant, v_{th} is the thermal velocity of electrons, σ_{th} is the capture cross section of electrons and N_c is the effective density of states in the conduction band.

$$\tau = \frac{1}{(v_{th}\sigma_{th}N_c)}\exp\left(\frac{E_T}{kT}\right), v_{th} = \sqrt{\left(\frac{8kT}{\pi m^*}\right)}, \sigma_{th} = 1\times10^{-14}cm^2, N_c = 4.3\times10^{14}T^{\frac{3}{2}}\,cm^{-3} \quad (1)$$

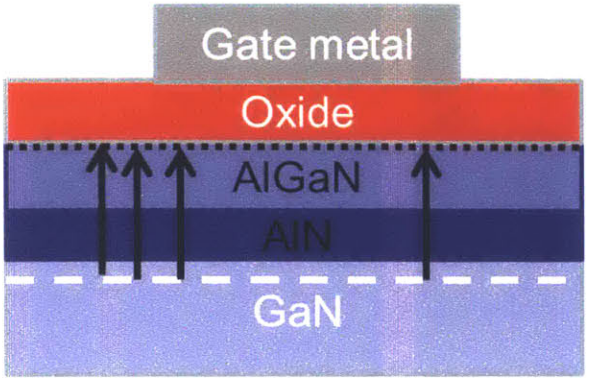


Figure 4-8: Schematic illustrating charge injection from 2-DEG into AlGaN/oxide interface

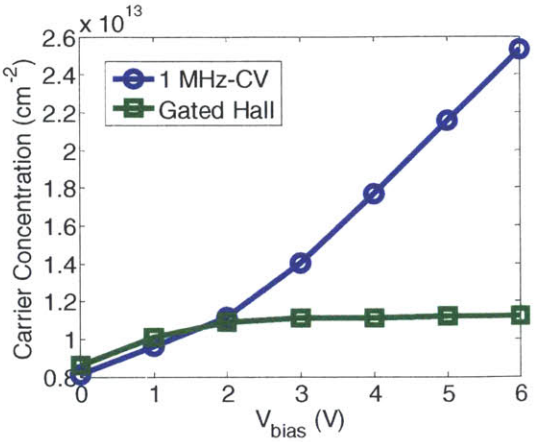


Figure 4-9: A comparison of the carrier concentration measured by Hall measurements vs. CV measurements. Hall measurements only capture carriers in 2-DEG while the measurements from CV measurements capture both carriers in 2-DEG and carriers injected into the AlGaN region

Figure 4-10 shows the expected trap energies necessary for traps to interact with a given measurement frequency at 25°C. Figure 4-11 shows an example of a capacitor with interface traps and the resulting frequency dispersion in the forward bias region.

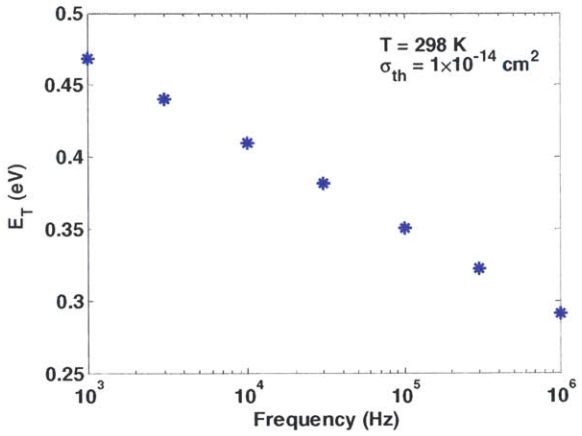


Figure 4-10: Calculated trap energies that correspond to particular measurement frequencies if assuming SRH statistic for T = 298K and $\sigma_{th} = 1\times10^{-14}$ cm^2

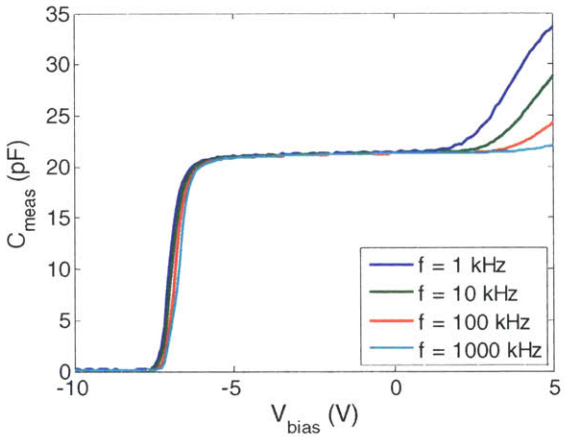


Figure 4-11: An example of an Al_2O_3/AlGaN/GaN capacitor with dispersion in the forward bias region.

CV measurements were performed by using the capacitance measurement unit on the Agilent B1505A, which has a frequency range from 1 kHz to 5 MHz. Probing deeper traps required alternative techniques and there were several options for probing deeper trap levels. One option was to use a

combination of a lock-in amplifier coupled with a function generator to apply a small AC signal and a current amplifier to convert the current into a voltage that a lockin amplifier can measure. Such a setup was evaluated as a possibility to measure low frequency CV measurements. However, while the absolute magnitude of the impedance was measured correctly for a range of frequency from 10 Hz to 1 kHz, the phase measurements were not accurate. For example, as seen in Figure 4-12, the phase at a bias voltage of 0 V was measured to be around 35° as opposed to something closer to 90°. As a result, the extracted capacitance was underestimated (10.5 pF vs an actual value of 22 pF) as seen in Figure 4-13 and the extracted conductance looks like what a CV measurement would look like (Figure 4-14)

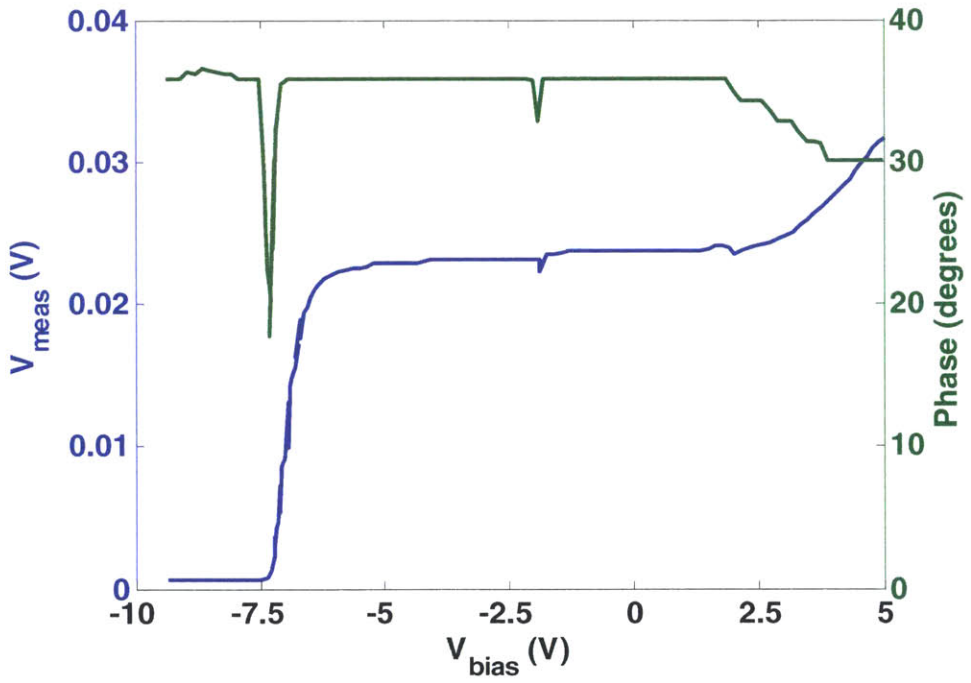


Figure 4-12: Measured voltage and phase. Note that the measured phase is 36 degrees at a bias of 0V, which suggests that the impedance is more real than imaginary. The measurement frequency is 1 kHz for this measurement

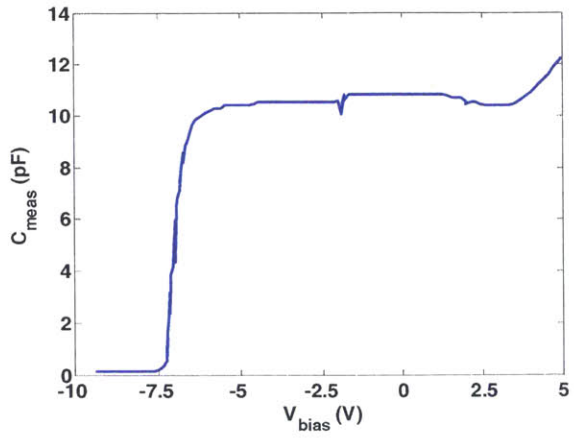


Figure 4-13: Extracted capacitance from lock-in measurement. The measured capacitance is roughly a factor of 2 lower than what the actual value should be.

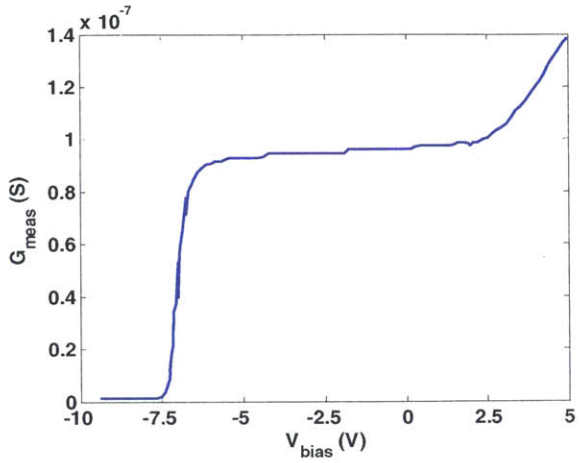


Figure 4-14: Extracted Conductance from lock-in measurement. Given that the shape of this conductance sweep looks like the CV measurement, it's clear that the phase is incorrect.

Therefore, a more promising solution is to perform quasi-static CV measurements. Quasi-static CV measurements are based on the principle that $I_{meas} = C\frac{dV}{dt}$. M. Kuhn first demonstrated this technique by applying a linear ramp on a capacitor and measuring the displacement current [68]. However, leakage current can distort the quasi-static CV measurement. There are several approaches to account for the leakage current. One approach is to simply perform voltage ramps in both directions and to subtract the difference between the positive sweep and the negative sweep as reported by Monderer et al. [69]. A second approach, which has been implemented by Hewlett Packard/Agilent in the 4155/4156 semiconductor parameter analyzer, is to sample leakage current after a small sweep and to subtract the leakage current in order to get the capacitance value [70].

The Agilent B2902A SMU unit that was used for the QS-CV measurements did not have a built-in QS-CV measurement function and therefore, a custom QS-CV program to control the unit was written in Matlab®. For the purpose of this study, a hybrid approach where the voltage was swept in a positive and negative direction for small 250 mV steps was used. The timing of the voltage sweep and an example of the resulting measured current is detailed below in Figure 4-15. There are two key benefits

of using the hybrid approach. First, the hybrid measurement allows for compensating for the leakage either by subtracting the difference between positive and negative sweeps or by subtracting the measured leakage current from the current during the sweep since all the necessary data points for implementing either approach were recorded. Second, the positive-negative sweep compensation resulted in less noisy QS-CV measurements at low ramp rates. Both the positive-negative differential compensation scheme and the leakage compensation scheme result in similar QS-CV measurements at a fast QS-CV rate of 5 V/s as seen in Figure 4-16. At lower sweep rates (1 V/s and slower) though, the positive-negative differential compensation scheme yield QS-CV measurements that are significantly less noisy than the QS-CV measurements with leakage compensation as seen in Figure 4-17. The origin of the noise in the leakage compensation scheme is believed to be due to noise in the leakage measurements. The leakage currents for these capacitors were in the pA range which was close to noise floor of the combined probe station + SMU and therefore are more susceptible to noise. On the other hand, the measured currents when the voltage was being swept was around 120 pA even for the slow 0.75 V/s sweep and therefore above the noise floor.

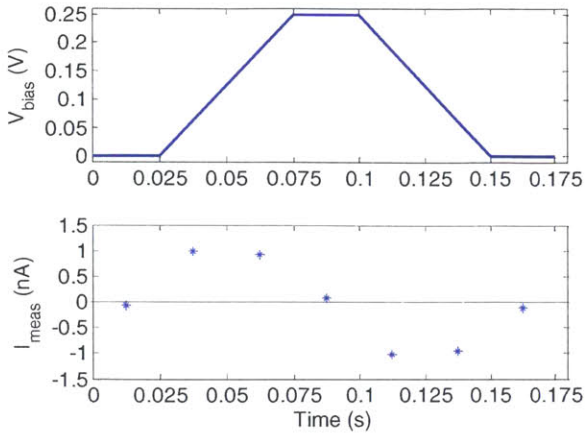


Figure 4-15: Quasi-Static measurement scheme utilized for this work. By sweeping positive and negative and by having hold steps, it is possible to compensate for leakage current by either subtracting the negative sweep from the positive sweep or by subtracting the measured current from current measured . This sweep has a rate equal to 5 V/s.

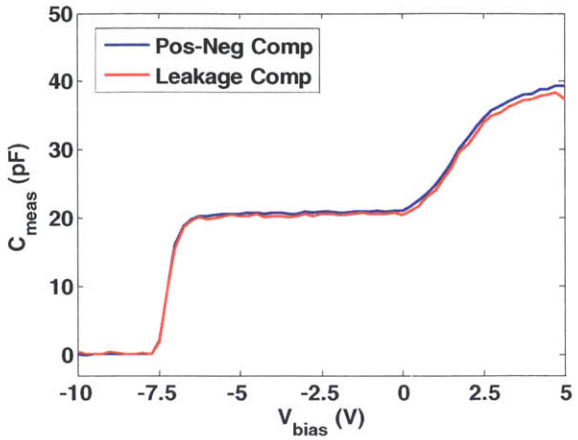


Figure 4-16: Quasi-Static CV measurement for a gate first capacitor with two different compensation schemes. Both the positive - negative differential sweep leakage compensation and the leakage compensation show very similar results when the QS-CV sweep rate is set to 5 V/s.

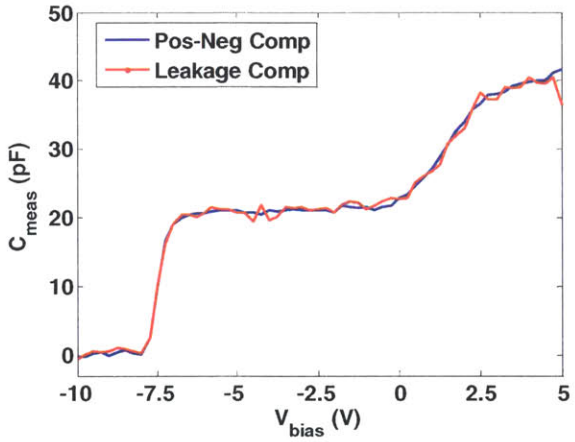


Figure 4-17: When the QS-CV sweep rate is lowered to 0.75 V/s, the QS-CV measurement using leakage compensation shows significantly show more noise than the QS-CV measurement using positive-negative sweep compensation. This is the same capacitor measured in Figure 4-16. In order to reduce the measurement noise, the positive-negative sweep compensation was used to account for gate leakage in these measurements.

CV measurements for capacitors from both the ohmic first sample and the gate first sample are plotted in Figure 4-18 and Figure 4-19.

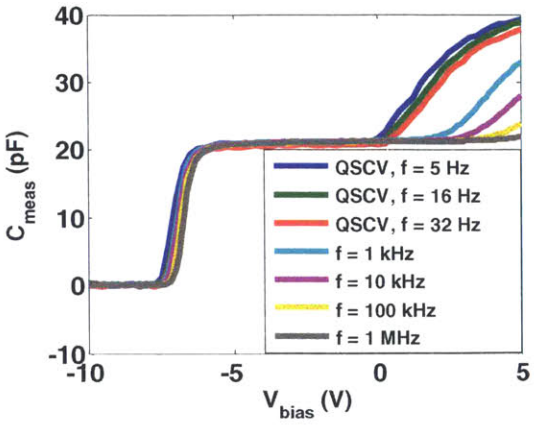


Figure 4-18: Ohmic first transistor that shows the best forward bias dispersion behavior. Note the extensive dispersion between the 1 MHz signal and the slowest QS-CV measurement curve

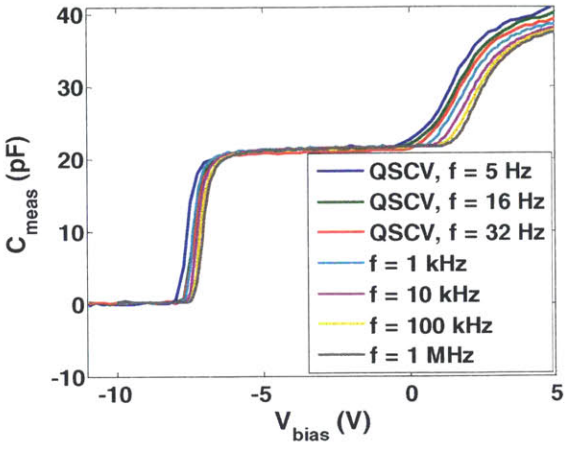


Figure 4-19: Representative gate first transistor shows significantly less dispersion behavior than the ohmic first transistor shown in Figure 4-18

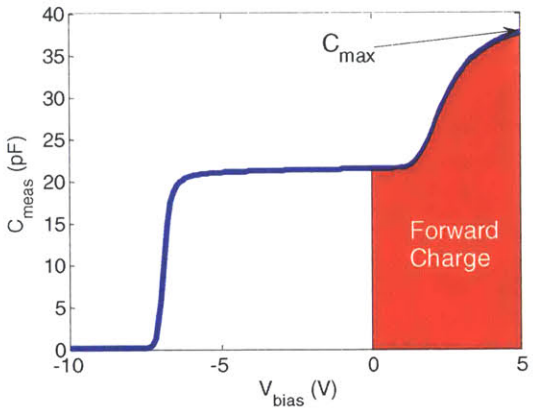


Figure 4-20: Forward Charge is used to quantify the amount of measured charge at forward biases. Looking at the evolution of forward charge as a function of frequency gives an indication of the dispersion behavior.

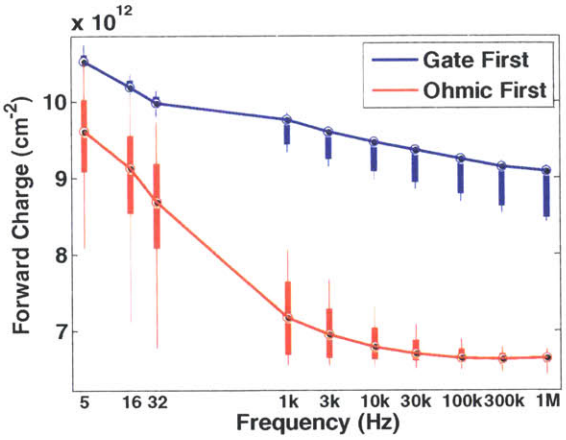


Figure 4-21: Forward Charge, as defined in Figure 4-20, vs frequency for gate first and ohmic first capacitors. Note that gate first capacitors show significantly less dispersion than ohmic first capacitors. Also note that the variation across the sample for the ohmic first sample is much larger than the gate first sample.

In order to quantify the amount of frequency dispersion seen in CV measurements, the measured CV curve was integrated from 0V to the maximum bias, which was set to 5 V for these measurements (Figure 4-20). The QS-CV measurement sweeps were translated into an associated frequency by the following expression: $f_{osc} = \frac{SweepRate}{2\pi V_{osc}}$ [28]. As seen in the error bars shown in Figure 4-21, the ohmic first sample has more extensive variation across the sample than the gate first sample.

As shown in Figure 4-22, there is particular spatial pattern where the center of the ohmic first sample shows less dispersion than the edges of the sample. As will be explained later, the origin of the spatial variations in the ohmic first sample is believed to be due to organic contamination. When photoresist was spun on this sample for lithography, the resist on the edges was slightly thicker and thus contributed to the spatial variations.

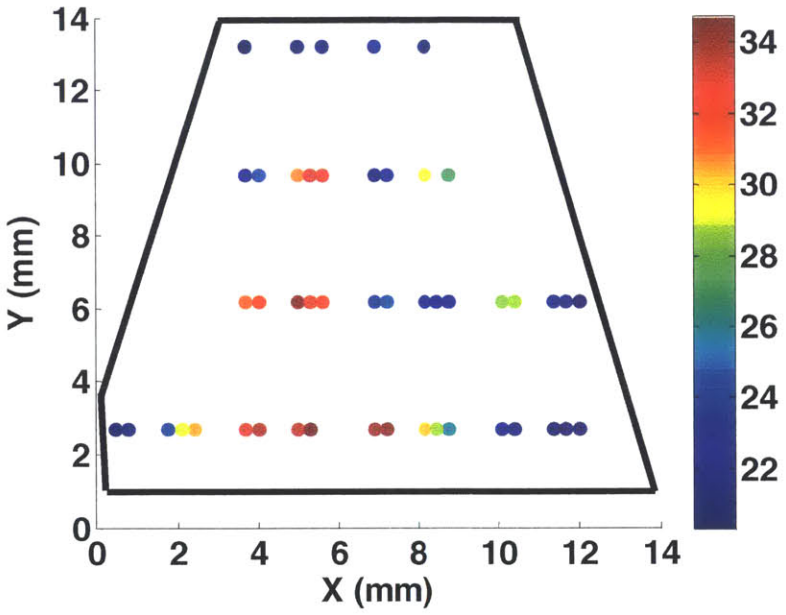


Figure 4-22: Scatter Map of C_{max} as measured at f=1 kHz and T = 25°C. Capacitors on edge show much more dispersion than in the center as evidenced by lower measured capacitance.

A key challenge with interpreting the CV dispersion data is that the series resistance due to the AlGaN layer can help distort the measured value of capacitance. As the measurement frequency increases, the relative ratio of impedance of the capacitive component to the impedance of the series resistance drops. Since the impedance analyzer models the impedance as a two component circuit with a real component and an imaginary component, the measured capacitance drops to compensate for the increase in the real component.

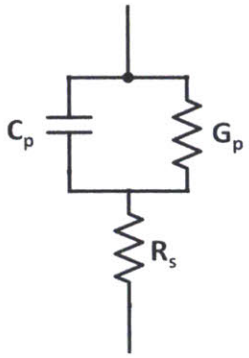


Figure 4-23: Schematic of Circuit Diagram with series resistance due to AlGaN.

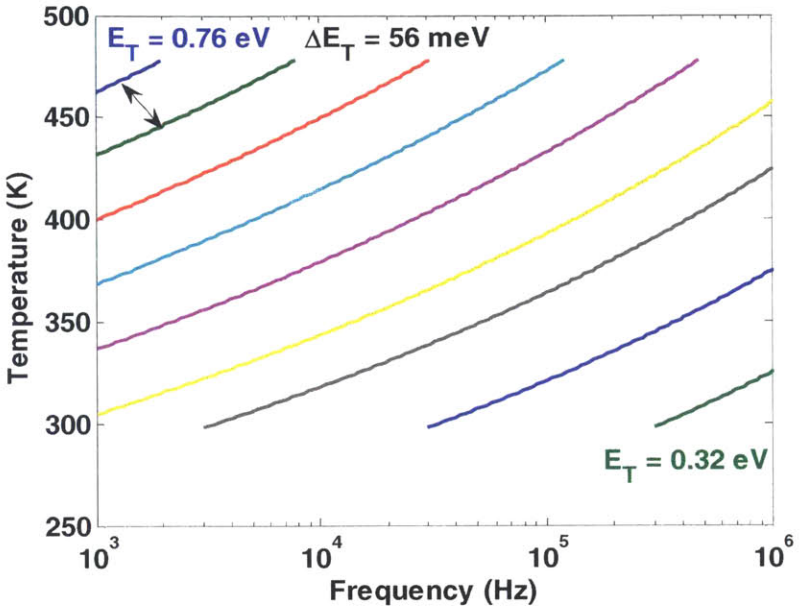


Figure 4-24: Contour plot showing how the time response of a trap changes as a function of temperature and measurement frequency. Lines indicate equidistant trap levels. This is calculated for $\sigma_{th} = 10^{-14}$ cm^{-2} using the expression in (1).

Performing CV measurements at elevated temperatures yields additional information for the following reasons. First, increasing the temperature allows for probing traps that are further away from the conduction band. At the same time, varying the temperature can allow for measuring the same trap energy by using different CV measurement frequencies. The relevant trap energies can be correlated to both CV measurement frequency and measurement temperature by the expression in Eq(1). As seen in Figure 4-24, a trap that interacts with a 1 kHz at 300 K will also interact with a 1 MHz AC signal if the temperature is 450 K. Therefore, if the AlGaN series resistance shown schematically in Figure 4-23 is negligible, then the forward charge measured at 1 kHz at 300 K will be equal to the forward charge measured at 1 MHz at 450K. On the other hand, if the AlGaN series resistance is dominant, then the measured forward charge measured at 1 MHz at 450K will be lower than the measured forward charge

at 1 kHz at 300K since the measured capacitance at 1 MHz will be smaller. Therefore, performing CV measurements with a combination of different frequencies and temperatures can help identify the contribution of series resistance on the measured forward charge. Both the gate first and ohmic first samples were measured at 25°C, 85°C, 145°C and 205°C with measurement frequencies ranging from 1 kHz to 1 MHz.

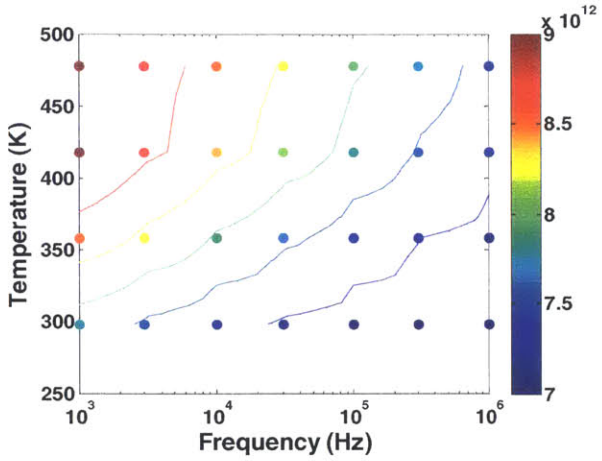


Figure 4-25: Forward Charge as a function of Temperature and Measurement Frequency for ohmic first capacitor.

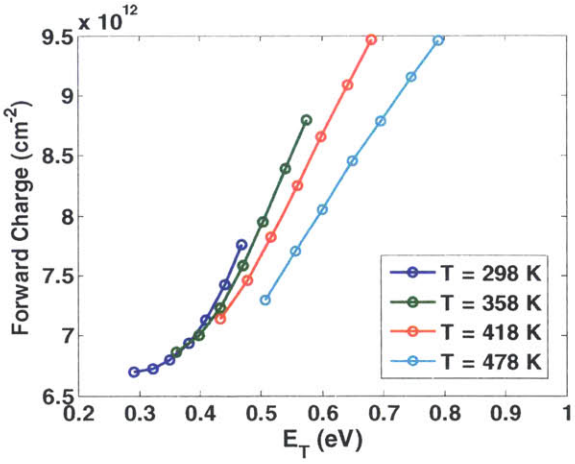


Figure 4-26: Forward Charge vs calculated trap energy for representative ohmic first capacitor. CV measurement frequency ranged from 1 kHz to 1 MHz. Measurement temperature ranged from 25°C to 205°C

Figure 4-25 shows the evolution of the measured forward charge as a function of frequency and measurement temperature for a representative ohmic first capacitor. Series resistance is still playing a role given that the forward charge measured at 1 kHz at 300K is greater than the forward charge measured at 1 MHz at 478K despite the latter corresponding to deeper traps. If series resistance were not playing a role, then the plot of E_T vs forward charge shown in Figure 4-26 for different measurement temperatures would overlap with each other completely.

A contour plot of forward charge vs frequency and measurement temperature is shown for a representative gate first capacitor in Figure 4-27. The role of series resistance is even more pronounced than for the ohmic first sample as seen by the contours. The forward charge only shows a pronounced frequency dependence and minimal temperature dependence. As seen by the E_T vs forward charge plot

in Figure 4-28, the maximum forward charge did not change appreciably by increasing the temperature. In contrast, for the ohmic first capacitor, the forward charge increased as a function of temperature, meaning that there was greater interaction with deeper traps by increasing the temperature. Therefore, it is apparent that the frequency dispersion seen in the gate first samples are more a function of series resistance as opposed to trapping.

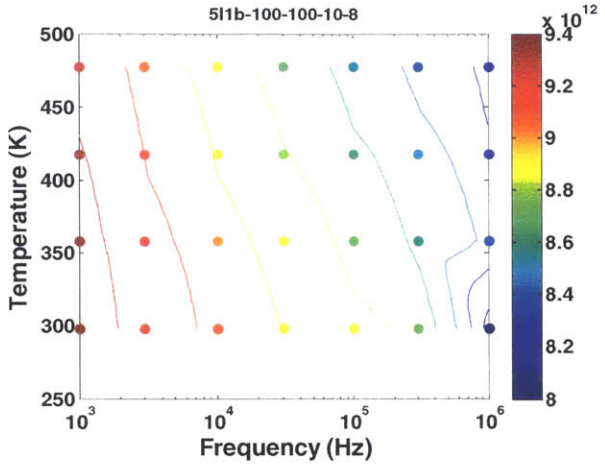


Figure 4-27: Measured forward charge for different frequencies and temperatures. Unlike the ohmic first capacitor, the forward charge is only dependent on the measurement frequency.

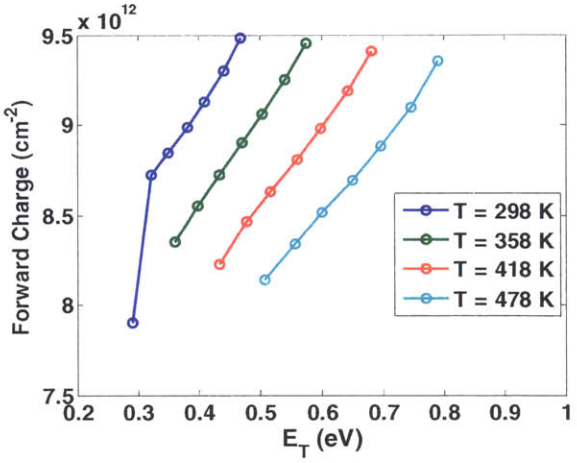


Figure 4-28: Plot of forward charge vs calculated trap energy. Note that the forward charge is overwhelmingly dependent on the measurement frequency

Identifying origin of difference between gate and ohmic first processes

There are three key differences between the gate first and the ohmic first samples. The first difference is that the ohmic first sample was subjected to an 800°C anneal while the maximum temperature that the gate first sample was subjected to was a 550°C, 5 min anneal. The second key difference is that the ohmic first sample was not subjected to a piranha clean given that ohmic metals were present while the gate first samples were subjected to a piranha clean. Finally, the ohmic first sample had a surface that was exposed to photoresist before performing an ohmic anneal. In order to study the impact of annealing temperature, gate first samples were fabricated where before starting the rest of the process, the bare sample was annealed at 800°C for 30s. Then, the rest of the gate first processing was performed.

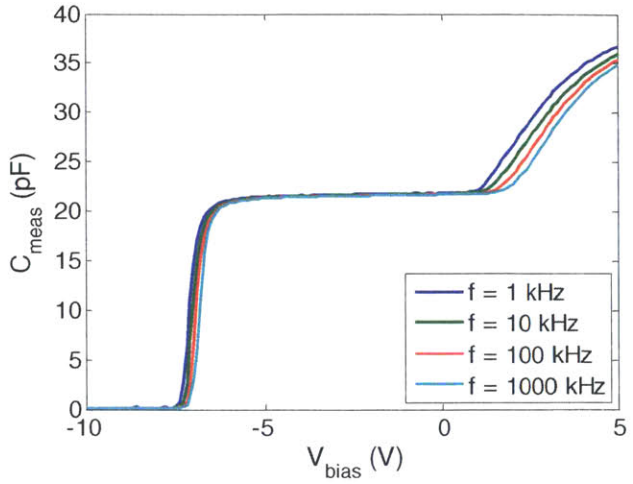


Figure 4-29: Representative gate first capacitor that had been annealed at 800°C before starting a gate first process

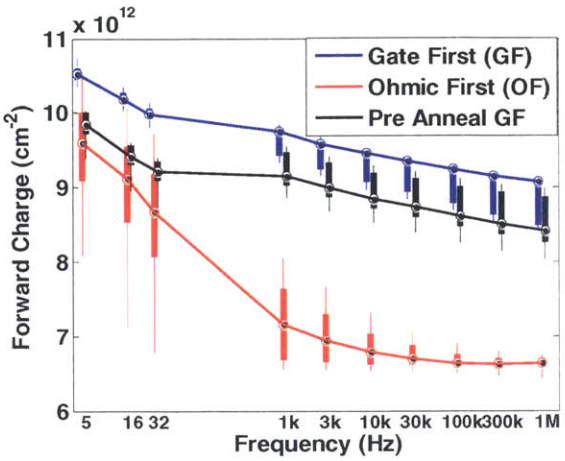


Figure 4-30: The gate first capacitor that had been annealed shows similar forward bias dispersion behavior to the gate first capacitor that was not pre-annealed.

CV measurements for a representative gate first capacitor that had been pre-annealed (Figure 4-29) display low frequency dispersion at positive biases just like the gate first capacitors that were not pre-annealed as shown earlier in Figure 4-19. The change in forward charge as a function of frequency shows that the gate first samples, regardless of whether they were pre-annealed or not, have much lower frequency dispersion than the ohmic first sample (Figure 4-30). These results seem to rule out high temperature processing as a key cause of the CV frequency dispersion seen in the ohmic first samples.

The difference in surface cleaning between the gate first sample and the gate last sample was another potential cause for the ohmic first samples' CV frequency dispersion. However, in order to perform wet piranha wet cleans before depositing the gate dielectric, the ohmic metals needed to be covered by a protective layer. Standard plasma enhanced chemical vapor deposition (PECVD) SiO_2 and SiN deposited by the STS-CVD tool were found to have too many pinholes to adequately protect the ohmic metals from a piranha clean. However, Tetraethyl orthosilicate (TEOS) SiO_2 deposited by the Oxford-100 tool was found to be conformal and also allowed for performing piranha cleans given the lack of pinholes in the oxide.

As stated earlier, the ohmic first sample was exposed to photoresist before performing the ohmic anneal. This discrepancy can be resolved by fabricating samples with a protective insulating layer before starting any processing [71]. In order to account for both the surface protection aspect and the difference in pre-ALD cleans for the gate first and ohmic first samples, four different samples were fabricated. Two of the samples had a protective SiO_2 layer deposited before the ohmic metals were pattered with liftoff. After the ohmic anneal was done, one sample with the pre-metallization oxide and one sample without the pre-metallization oxide had 250 nm thick TEOS SiO_2 layer deposited on top of the ohmic metal in order to allow for a pre-ALD piranha clean. The other two samples did not have this protective oxide layer on top of the ohmic metals and thus were were cleaned by using nanostrip for 2 min as part of the pre-ALD clean. A process flow for the four samples is illustrated in Figure 4-31

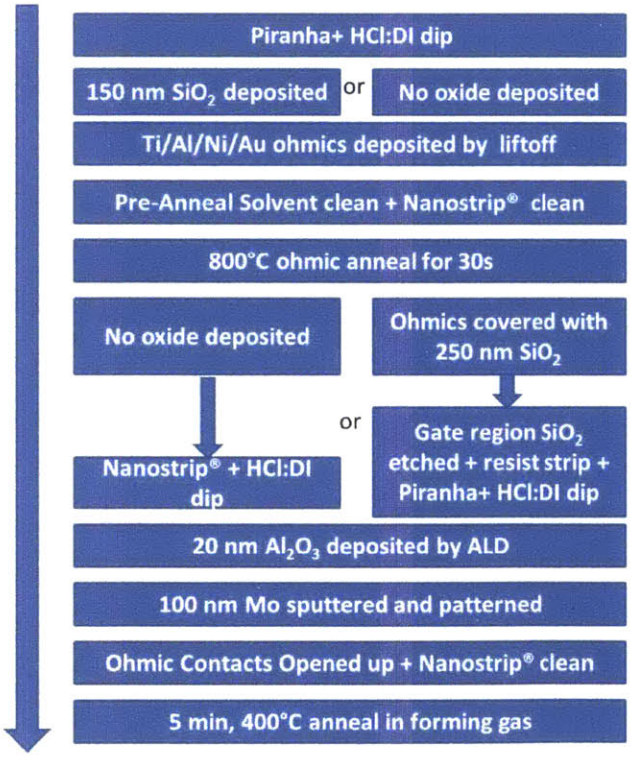


Figure 4-31: Process flow for ohmic first samples with different combinations of a pre-anneal oxide and post anneal oxide

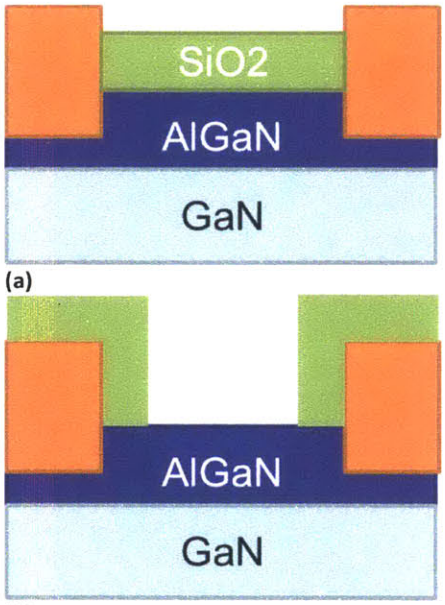


Figure 4-32: (a) This is a schematic showing a SiO_2 surface protection layer deposited before ohmic metals are deposited. (b). This schematic shows a SiO_2 layer that is deposited after the ohmic anneal and then patterned in order to remove the oxide from the gate region

Sample Name	TEOS SiO_2 Deposition		Process Attributes	
	Before ohmic metallization	After ohmic anneal	Surface exposed to photoresist before 800°C anneal	Surface cleaned by piranha before ALD
Ohmic First (OF)			X	
PreOxide OF	X			
PostOxide OF		X	X	X
Pre-Post Oxide OF	X	X		X

Table 6: All four Ohmic First samples fabricated with different combinations of TEOS SiO_2 and resulting process attributes

As shown in Figure 4-33, performing a piranha clean on a sample that had been exposed to photoresist before annealing can cause a drastic improvement in the interface as determined by forward bias CV measurements. As seen by the lower frequency dispersion for the two samples with surface protection layers (Figure 4-34) than the Post-Oxide sample that was cleaned with piranha before ALD deposition, it is more effective to protect the surface with an oxide layer than to clean it afterwards with a piranha clean

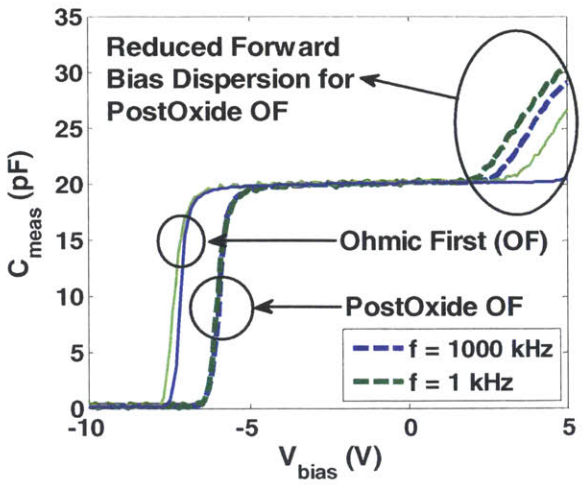


Figure 4-33: Comparison of an ohmic first capacitor with a PostOxide ohmic first capacitor. Both samples were exposed to photoresist before the 800°C ohmic anneal. The PostOxide OF capacitor shows a superior interface due to use of piranha mixture to get a more aggressive pre-ALD clean than the ohmic first sample.

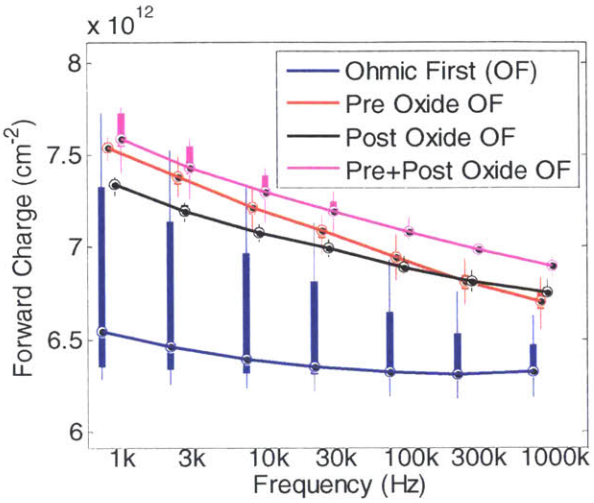


Figure 4-34: Forward Charge vs Frequency for all ohmic first capacitors. Samples that had a protective oxide layer before ohmic annealing exhibit signs of a slightly better interface. All samples with either a pre-anneal protective oxide layer or a pre-ALD piranha clean show drastically better frequency dispersion behavior and uniformity than the ohmic first sample.

Summary

To summarize, forward bias CV measurements were performed in order to compare capacitors fabricated using a gate process with capacitors fabricated with an ohmic first process where the Au based ohmic contacts were pattered by liftoff and annealed at 800°C in order to form ohmic contacts. Gate first capacitors exhibited a superior interface than the ohmic first capacitors as determined by the much lower frequency dispersion for the gate first capacitors. Given that capacitors that were processed using the gate first process were neither exposed to an 800°C anneal or were exposed to photoresist before depositing the oxide, additional experiments were performed in order to identify the key source of the difference between the gate first and ohmic first capacitors. First, gate first capacitors that had been annealed at 800°C before starting the gate first process were fabricated. Forward bias CV measurements showed that these capacitors had dispersion behavior that was similar to the gate first sample that had not been annealed which indicated that the high temperature anneal was not a cause of the degradation of the interface. Additional ohmic first samples with various combinations of protective SiO_2 layers that were deposited before and/or after the ohmic metals were deposited.

Samples with protective layers deposited before any other processing had an interface that was not exposed to photoresist while samples with ohmic contacts that were encapsulated by a protective SiO_2 layer were cleaned by a piranha clean before performing ALD. Both kinds of aforementioned samples showed a superior interface than the samples processed by a standard ohmic first process. These results indicate that organic contamination due to photoresist is a key culprit for the interface degradation seen for the standard ohmic first samples.

Chapter 5 Transient Current-Voltage Transistor Characterization

Capacitance voltage measurements are very useful for studying interfaces but in order to get a complete picture, it is necessary to look at the transistor behavior as well. Samples using the gate first process will be compared with samples processed with an ohmic first process in order to see how a poor interface translates into transistor performance. Transistors in this section will be characterized by the following techniques.

- Drain Lag Pulsed IV measurements. These measurements involve performing pulsed IV measurements where the evolution in I_D-V_{DS} measurements is seen as a result of applying large drain biases while the device is pinched off. These bias conditions occupy traps in the drain access region which are the cause of the current collapse phenomenon.
- Positive Gate Transient current measurements. These measurements involve applying positive gate pulses and looking at the recovery in drain current as populated traps detrap.
- Positive Gate Pulsed IV measurements. These measurements involve performing pulsed-IV measurements where the evolution in I_D-V_{ds} and I_D-V_{gs} measurements is seen as a result of applying positive gate pulses. These measurements help build upon information gleaned from positive gate transient current measurements.

Drain Lag Pulsed IV Measurements

Current collapse in GaN based devices is a well-known phenomenon where the drain current measured under DC conditions is much larger than the drain current measured under switching conditions [72]. Current collapse in GaN based devices has been attributed to trapping that occurs in the drain access region when large fields are applied at the drain [72]. It has been a major reliability concern and has been partially addressed by depositing passivation layers like SiN and Al_2O_3 in order to passivate surface states that are present on the AlGaN surface [73],[12].

In order to characterize current collapse, an Auriga AU4750 measurement system was used in order to perform drain lag measurements where the gate was pinched off and successively larger drain voltages were applied. The current was measured 200 ns after transitioning from a stress step where the gate is pinched off and a large drain voltage is applied as illustrated schematically in Figure 5-1. As the drain voltage during the stress step increases, an additional number of traps in the drain access region get occupied and the drain access resistance increases. This results in an increase in the saturation voltage and an increase in R_{on} as shown in Figure 5-2. As can be seen in Figure 5-3, the gate first transistor shows minimal current collapse in comparison to the ohmic first transistor which indicates that the surface of the gate first transistor is better passivated than the ohmic first transistor. This is consistent with the superior interface was seen from CV measurements.

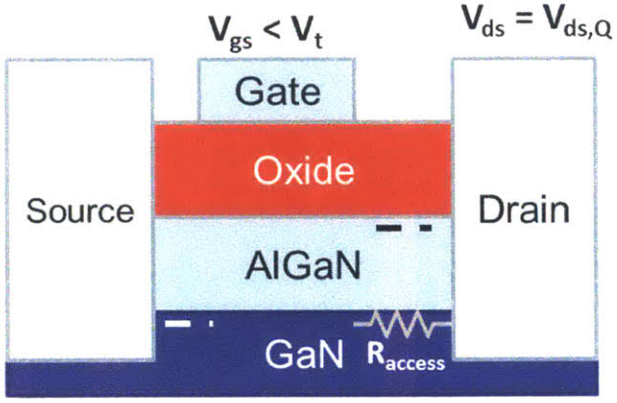


Figure 5-1: Schematic explaining origin of current collapse in drain lag measurements. When the gate is pinched off and large V_{ds} is applied, electrons are injected into the drain access region. This in turn causes the 2-DEG in the drain access region to get partially depleted. The increase in R_{access} means that a larger V_{ds} needs to be applied for the intrinsic transistor to go into saturation.

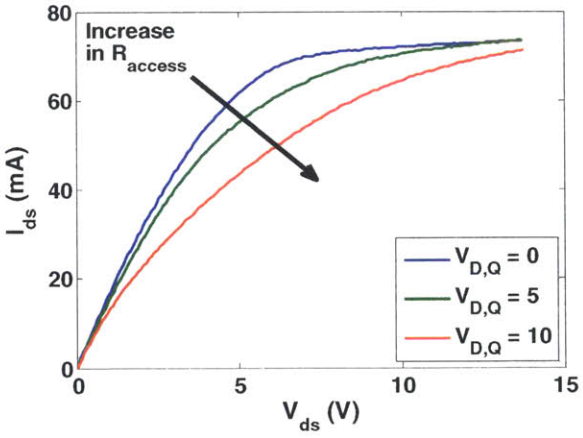


Figure 5-2: An example of drain lag, pulsed IV measurements on an ohmic first transistor. As the quiescent drain bias increases, R_{access} increases and therefore, R_{on} increases and the saturation voltage for the transistor increases as well.

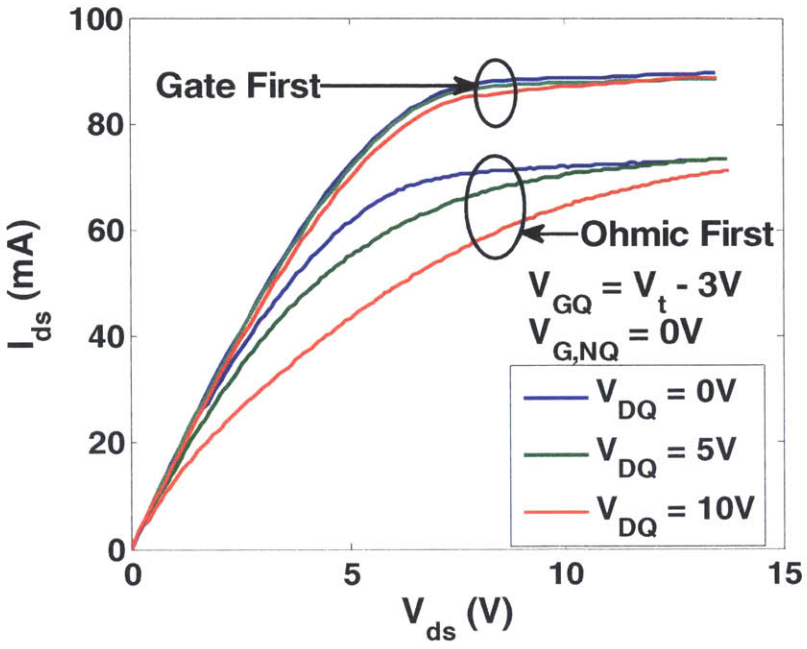


Figure 5-3: Comparison of gate first and ohmic first transistors.

Transient Current Measurements

As seen earlier, forward bias CV measurements give an indication for the quality of the interface. However, due to the impact of series resistance, it is difficult to determine the impact of series resistance which can lead to an overestimate of the total number of traps present. Therefore, a technique which allows for directly charging traps and measuring their impact by looking at the decay in current allows for direct confirmation of both the number of relevant traps and their time constants. Such a measurement technique is very similar to negative bias temperature instability (NBTI) measurements that are performed on PMOS Si devices in order to study threshold voltage instability [74]. In order to capture short term transients, a measurement setup that allows for both short term, high speed sampling and long term sampling is desired for NBTI measurements. Similar high speed transient measurements have been performed on GaN based devices as well. Lansbergen et al. studied the change in V_{th} in D-Mode AlGaN/GaN MISHEMTs by applying a square wave in order to switch the device on and off and by looking at the different in V_{th} [75].

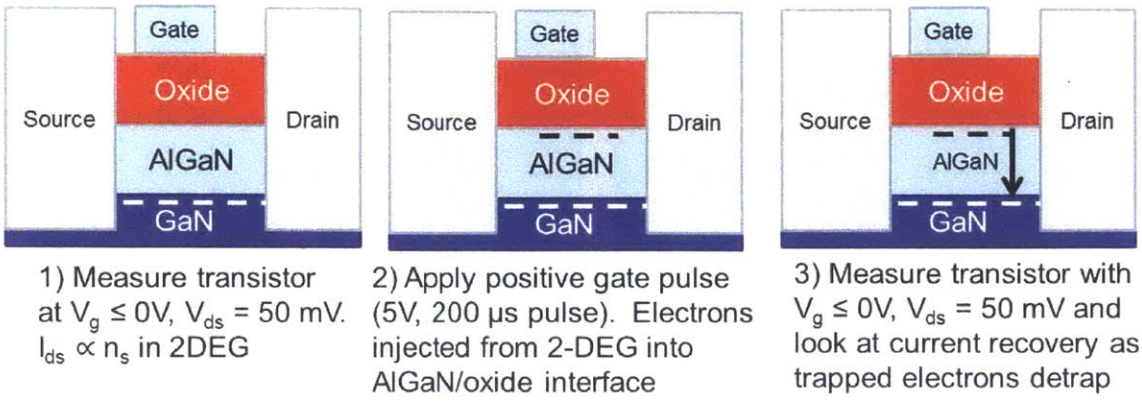


Figure 5-4: Schematic of the measurement sequence for transient IV measurements. The transistor is biased with V_{ds} = 50 mV in order to ensure low lateral fields and to avoid detrapping due to transistor self-heating.

In order to capture fast dynamics, it is not enough to use a conventional source measurement unit since the fastest sampling time with reasonable accuracy is still 200 µs. As suggested by Lagger et al., it is necessary to use an oscilloscope in order to capture fast transients in GaN based MIS-HEMTs on the order of 1 µs [76]. Therefore, as sketched out below in Figure 5-5, a combination of an oscilloscope and a semiconductor parameter analyzer allowed for both fast sampling immediately after the pulse and low noise, long term sampling. A Stanford Research System SR 570 current amplifier was used in order to convert the source current to a voltage that was in turn measured by both the oscilloscope and by a channel of the Agilent B2902A SMU. The drain bias was set to 50 mV for several reasons. First, the low V_{ds} value ensured that the lateral field between the source and drain was uniform in comparison to the vertical field. Second, the low V_{ds} and the resulting low power dissipation ensured that the device temperature was controlled by the chuck. Finally, the current amplifier was limited to a current of 1 mA, which also necessitated the low V_{ds}.

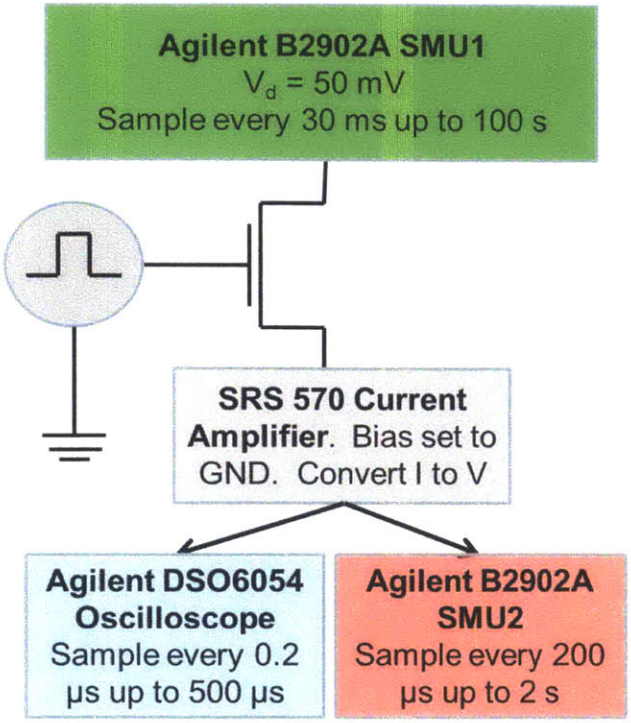


Figure 5-5: Schematic for transient current measurements

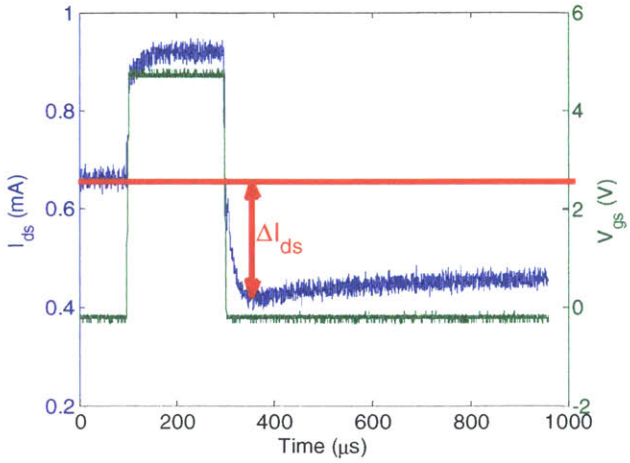


Figure 5-6: I_{ds} and V_{gs} as captured by the oscilloscope. The V_{gate} at the pulse was 5V while the base voltage was 0V in this measurement.

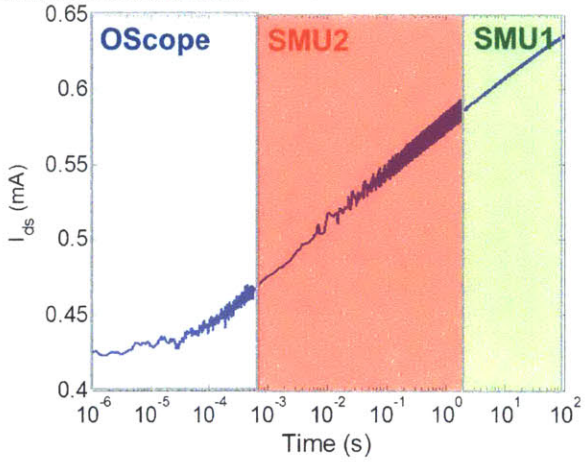


Figure 5-7: Timing Schematic for Transient current measurements. Time refers to the time after the 5V pulse seen in Figure 5-6. By using a combination of an oscilloscope and two different SMUs sampling at different rates, it's possible to capture transient behavior across eight or more orders of magnitude.

After applying a 200 µs pulse, the current drop, as defined in Figure 5-6, resulted from charging traps. As shown by Figure 5-7, the transient behavior after the high voltage pulse can be capture across timescales ranging from 1 µs to 100 s. In order to see the impact of electric field on the recovery, V_{base}

ranged from -6V to 0V. In addition, the samples were measured at four temperature points ranging from 25°C to 205°C in order to study the thermionic nature of the trapping. As seen in Figure 5-8, the absolute value of the current drops as a function of temperature due to the decrease in mobility. Therefore, in order to ensure that the impact of temperature is taken into account, the drop in current needs to be normalized with respect to the drain current at V_{gs} = 0V before any pulses. Therefore, the percentage change in current, as plotted in Figure 5-9, is proportional to the number of carriers in the 2-DEG that are depleted by the trapped electrons.

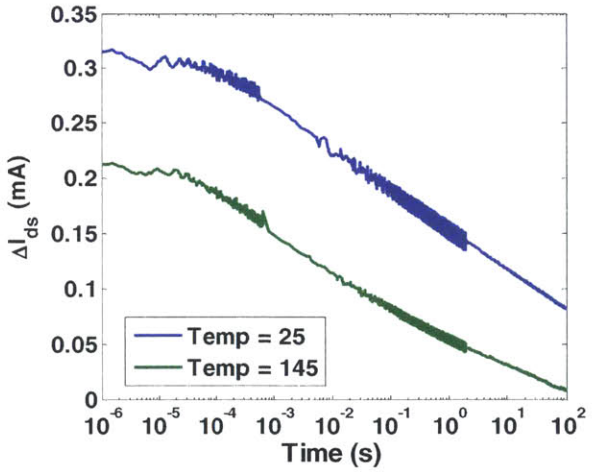


Figure 5-8: Change in current vs. Time for T = 25°C and T=145°C for an ohmic first sample. The absolute value of the change in current drops because of the drop in electron mobility. Therefore, the change in current needs to be normalized with respect to the absolute value

There are two components of the current recovery mechanism after the positive gate pulse is applied. As seen in Figure 5-9, the ohmic first sample exhibits a clear temperature dependence on the recovery. By increasing the temperature, the slope of the recovery increases. This is consistent with the temperature dependence on the CV measurements seen for the ohmic first sample. In contrast, the gate first sample does not exhibit a strong temperature dependence on the slope of the recovery. This is consistent with a tunneling based recovery mechanism [77] given that tunneling based recovery mechanisms show relatively low temperature independence [78]. This is also consistent with the relative temperature independence of the CV measurements of the gate first sample.

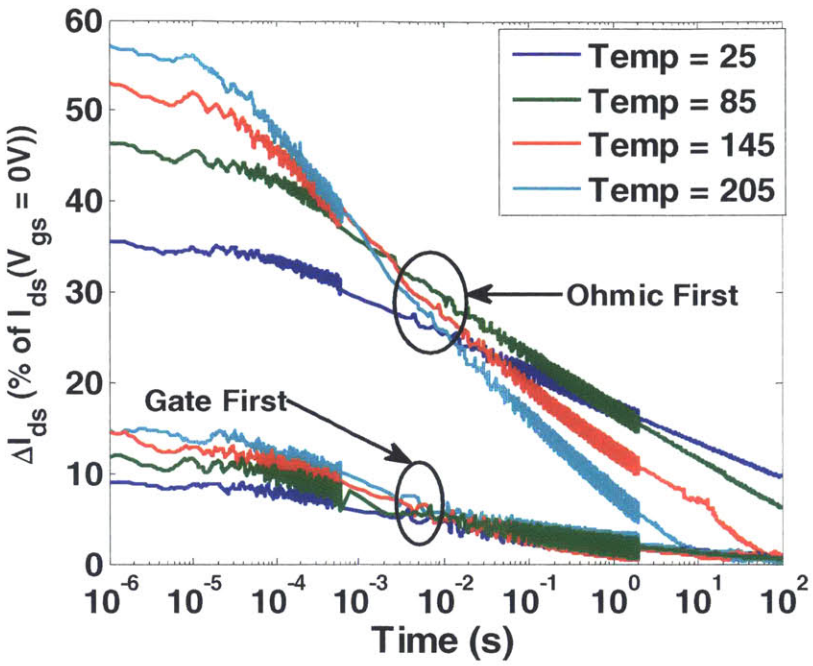


Figure 5-9: Change in normalized current vs. time after +5V gate pulse for both ohmic first and gate first HEMTs at temperatures from 25°C to 205°C. The slope of the recovery for the ohmic first transistor shows much stronger temperature dependence than that of the gate first transistor. The small temperature dependence of the gate first transistor's recovery is suggestive of a tunneling based mechanism.

In order to quantify the temperature dependence of the transient measurements, the method of fitted time constants was utilized [77]. The transient behavior is fitted to a sum of exponentials with different characteristic time constants, where τ_n corresponds to individual time constants and where x_n are the weights for each of the time constants τ_n.

$$b(t) = \sum x_n e^{-\frac{t}{\tau_n}}$$

In order to solve this problem in a computationally efficient manner, the fitting function was setup as a convex function and the convex solver CVX was then used [79],[80]. The coefficients were limited to being positive only given that during the recovery step, traps are not assumed to get reoccupied. In order to prevent over fitting, an additional term, $\eta|x|$, was added where η is an arbitrary variable that

helps prioritize the amount of variation. Larger values of η cause peaks to smear out while smaller values of η cause peaks to get amplified as seen in Figure 5-10.

$$\min(|Ax-b|+\eta*|x|), where\ A=\begin{bmatrix} e^{-\frac{t_1}{\tau_1}} & \cdots & e^{-\frac{t_1}{\tau_n}} \\ \vdots & \ddots & \vdots \\ e^{-\frac{t_n}{\tau_1}} & \cdots & e^{-\frac{t_n}{\tau_n}} \end{bmatrix}, x_n \geq 0$$

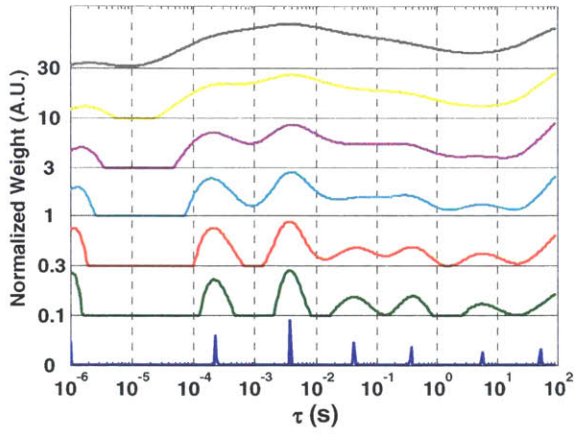


Figure 5-10: Transient current data is fitted by η values ranging from 0 to 30. By increasing η value, the shape of the weights gets broader as expected. Weights are normalized in order to capture change in shape

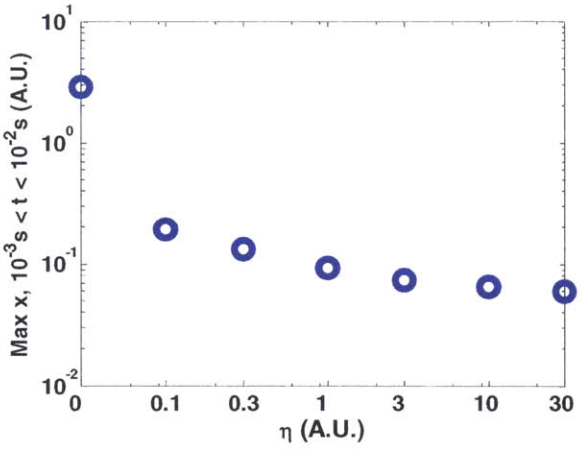


Figure 5-11: As the η values increased, the absolute value of the amplitudes decreased. This is a plot of the maximum amplitudes for tau values between 10^{-3} and 10^{-2} s.

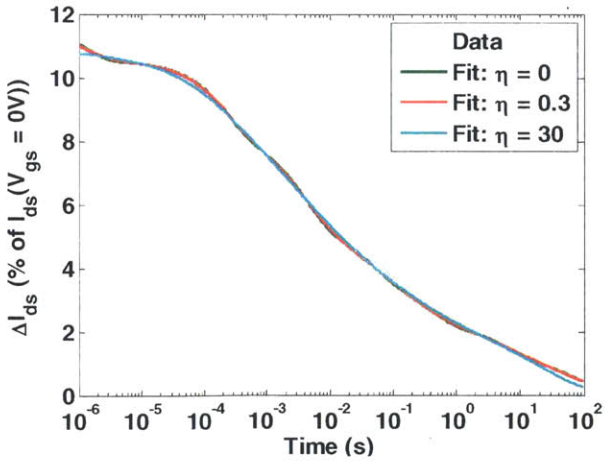


Figure 5-12: Data and fits with different η values. All η values capture essence of dynamics but larger η values cause increasing inaccuracy for t < 10^{-5} s and t > 10s

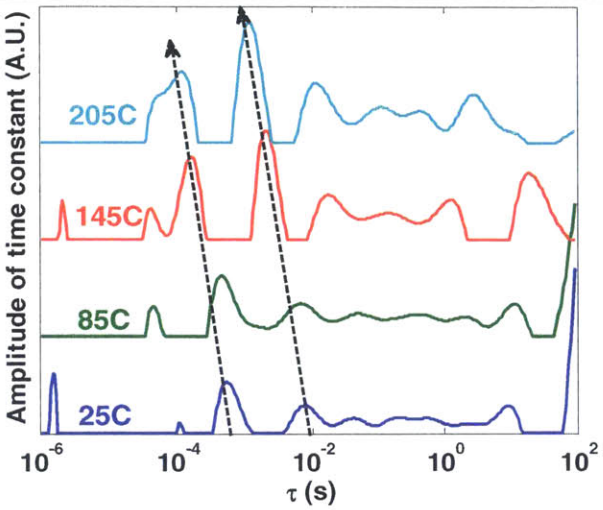


Figure 5-13: Fitted time constants for ohmic first sample as shown in Figure 5-9. There is a clear temperature dependence on the time constants. η = 0.3 for these fits

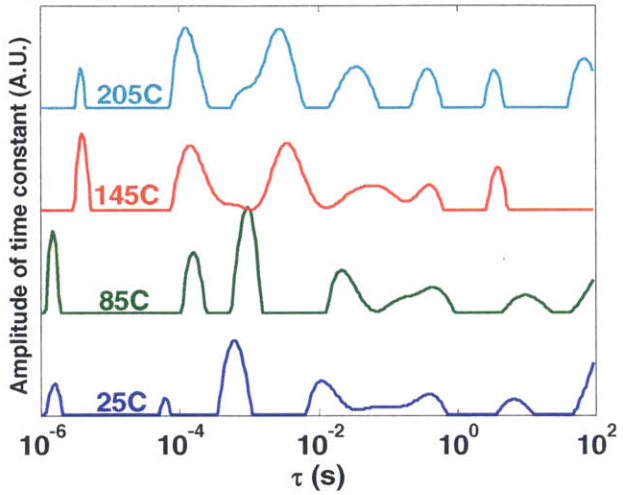


Figure 5-14: Fitted time constants for gate first sample as shown in Figure 5-9. The temperature dependence on the time constants is less clear. η = 0.3 for these fits

Figure 5-13 shows the fitted time constants at varying temperatures for the ohmic first device plotted in Figure 5-9. Several peaks move towards shorter time constants as the temperature increases which is consistent with the faster recovery seen by increasing the temperature. Figure 5-14 shows the equivalent time constants for the gate first device plotted in Figure 5-9. There is no clear temperature dependence on the peaks seen which is reflected by the lack of temperature dependence seen in the recovery current for the gate first device plotted in Figure 5-9.

In addition to fitting time constants, it is useful to look at the rate in recovery per time decade as shown in Figure 5-16. Plotting the recovery rate per decade helps visualize the time period where the fastest recovery is taking place. For example, the current recovers 2.3% between 10^{-3} and 10^{-2} s for the device in Figure 5-16.

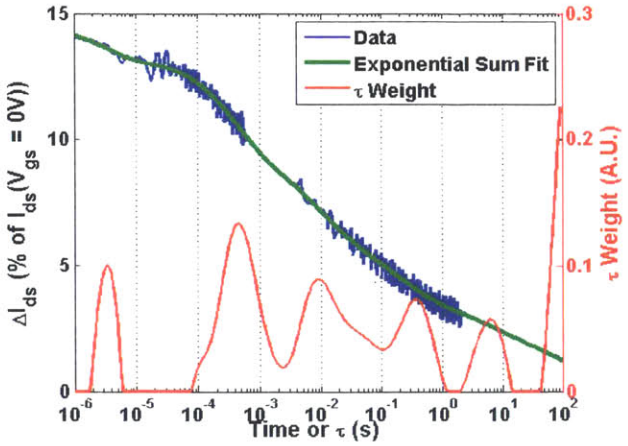


Figure 5-15: Example of Fitted exponential sum. Gate First sample with V_{Base} = -4V.

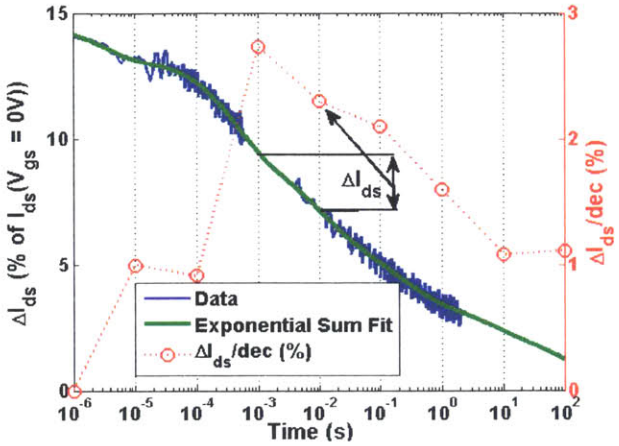


Figure 5-16: This is the same transistor measured in Figure 5-15. It can be clearer to look at the change in recovery as a function of decade of time as described in [74]. In the plot above, the quantity ΔI_{ds}/dec is defined by the change in current recovery per decade. For example, the current recovers 2.3% between 10^{-3} and 10^{-2} s

The gate voltage during the recovery step also plays a role in the recovery speed. The gate voltage during the recovery step varied from -6V to 0V. By varying the gate voltage, the recovery rate and relevant time constants changed. As seen in Figure 5-17, a more negative V_{Base} accelerates the rate of recovery. For V_{Base} = 0V, the greatest amount of recovery per time decade takes place between 10^{-3} and 10^{-2} s while for V_{Base} = -4V, the greatest amount of recovery per time decade takes place between 10^{-4} and 10^{-3} s. The dependence on reverse bias on the recovery suggests that Fowler-Nordheim tunneling is involved in the post positive gate pulse recovery process. Fowler-Nordheim tunneling is based on the narrowing of the barrier [81]and by applying a more negative V_{Base}, the effective barrier width of the AlN interlayer is reduced.

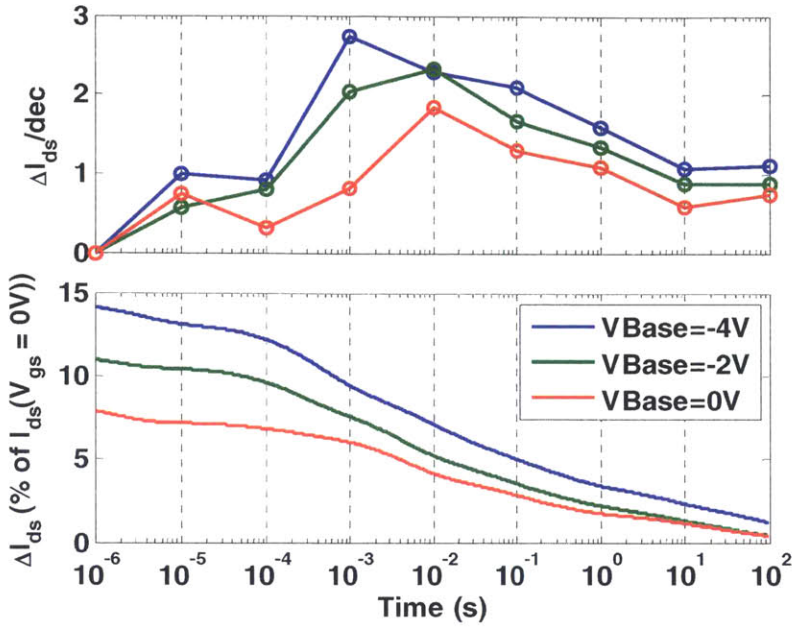


Figure 5-17: Bottom plot shows fitted ΔI_{ds} vs Time for representative gate first sample. Top plot shows current recovery as a function of time as defined in Figure 5-16. Lowering the base voltage causes a faster recovery.

The impact of the pulse voltage was looked at by applying successively larger gate pulses ranging from 2 V to 6V. As can be seen in Figure 5-19, applying a larger pulse voltage greater than 2 V caused a uniformly large degradation in the transient behavior in the ohmic first sample.

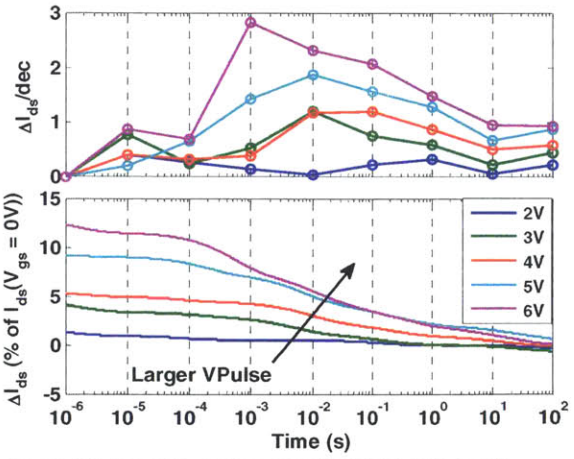


Figure 5-18: Representative gate first transistor with successively larger values of VPulse applied during the 200 us pulse. For all VPulse values, the recovery starts at around 10^{-4} s. Vbase = 0V for this measurement.

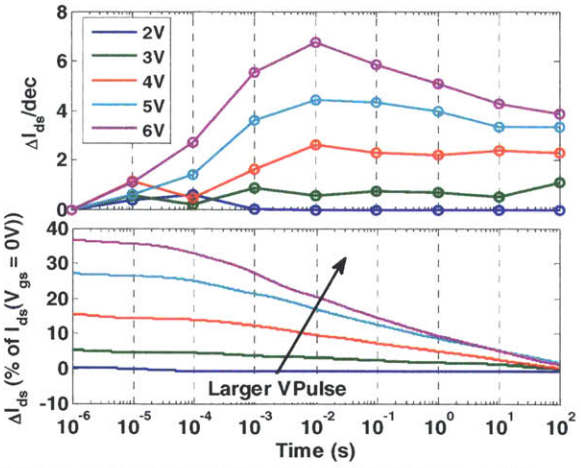


Figure 5-19: Representative ohmic first transistor with successively larger values of V_{Pulse} applied during the 200 us pulse. For all V_{Pulse} values, the recovery starts at around 10^{-4} s. V_{base} = 0V for this measurement.

Finally, pulses of different lengths ranging from 10 µs to 1 ms were applied to both samples to see the impact of pulse time and to see the interaction between pulse time and recovery time as seen in

Figure 5-20 and Figure 5-21 for representative gate first and ohmic first transistors respectively. For both samples, the initial degradation is proportional to the log of the pulse width. For example, for the ohmic first transistor in Figure 5-21, after a 10 µs, 100 µs and 1 ms 5V pulses, the initial drops in current are 18.1%, 21% and 24% respectively. The shapes of the recovery curves also do not vary as a function of the pulse width. For example, for all pulse widths, the gate first transistor shows the fastest recovery between 10^{-4} and 10^{-2} s while the ohmic first transistor shows recovery rate that is linear to the log of time after 10^{-4} s regardless of the pulse width.

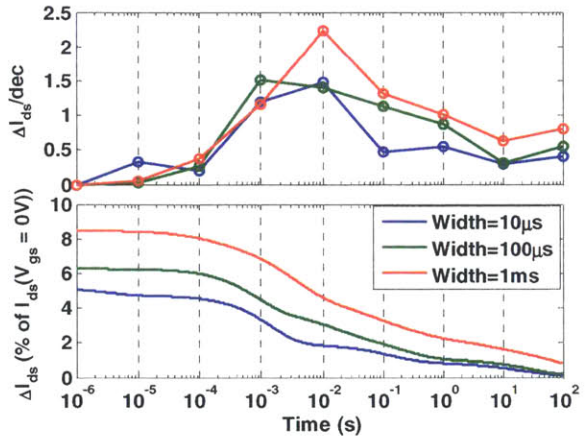


Figure 5-20: Dependence on the pulse width on the transient behavior of a gate first transistor. The initial degradation varies linearly as a function of the log of pulse width. For all three pulse times, the fastest recovery/decade of time takes place between 10^{-4} s and 10^{-2} s

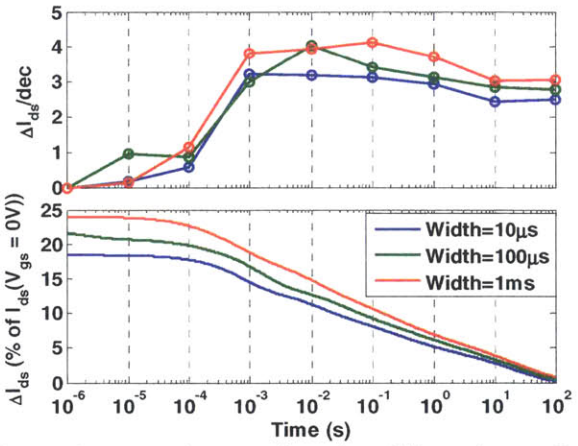


Figure 5-21: Dependence on the pulse width on the transient behavior for an ohmic first transistor. Note that the initial degradation varies linearly as a function of the log of the pulse width. Also note that the recovery slope is flat as a function of the log of time after 100 µs. This is different from the gate first transistor (Figure 5-20) which has a large decrease from 10^{-4} s and 10^{-2} s

The log(t) dependence seen in the ohmic first transistor in Figure 5-21 is indicative of multiple trap states that have uniformly distributed time constants [19]. In order to demonstrate this, Figure 5-22 shows a plot of the sum $y = \sum a_n e^{-\frac{t}{\tau_n}}$, where $a_n = A, \tau_n = 10^{-4} \ldots 10s$. A sum of multiple exponentials with time constants spaced out in log time will give a resulting function that is proportional to the log(t) as seen in Figure 5-22. On the other hand, if there is a dominant time constant as shown in Figure 5-23, the resulting sum will have a kink and a time decade where the change per decade is the

largest. The gate first transistors shown in Figure 5-20 have a similar behavior where certain time constants are more dominant than others.

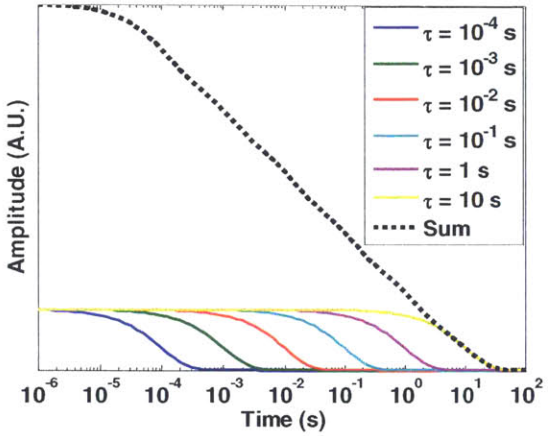


Figure 5-22: Plot of sum of equally weighted exponentials with different τ values. Note that the sum is proportional to log(t).

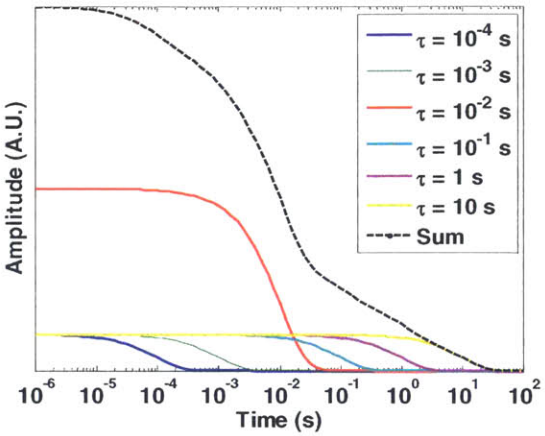


Figure 5-23: Example of sum where exponential with $\tau = 10^{-2}$ s is weighted 5 times more than the rest of the τ values. There is an appreciable kink as a result.

Transient current Recovery

The transient current measurements involved a sequence of multiple +5V pulses and varying base voltages that were applied for 100s after the +5V pulse. In order to look at the cumulative impact of the +5V pulses, a number of experiments were performed both on the gate first sample and the ohmic first sample. First, the change in current was measured after 100 cycles of 5V pulses with a base voltage of 0V. Then, the change in current was measured after a combination of a stress cycle with the same +5V pulse and 0V base voltage and a recovery cycle where a negative stress bias of -6V was applied for 100s. Finally, a third recovery experiment was performed where the recovery cycle involved turning the microscope light on while applying a negative bias. The probe station microscope light was limited to visible light only due to filtering from the microscope objective and optics.

Recovery Experiment	Stress Cycle	Recovery Cycle
Stress Cycle Only	200 µs 5V pulse + 100 s recovery at Vg = 0V	None
Stress + Negative Recovery	200 µs 5V pulse + 100 s recovery at Vg = 0V	Vg = -6V for 100s after each stress cycle with microscope light off
Stress + Negative Illuminated Recovery	200 µs 5V pulse + 100 s recovery at Vg = 0V	Vg = -6V for 100s after each stress cycle with microscope light on

Table 7: Different conditions for long term recovery measurements

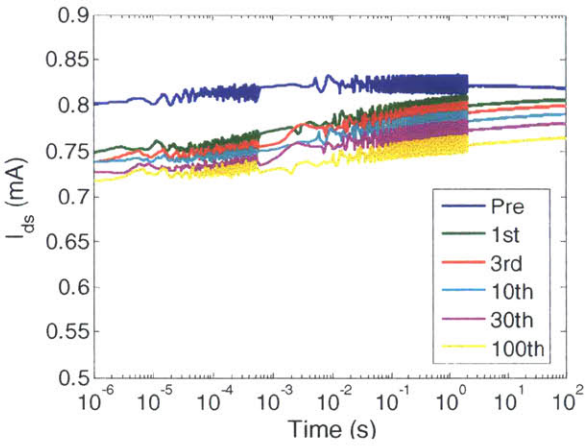


Figure 5-24: Transient Ids as a function of different numbers of pulses for the gate first sample

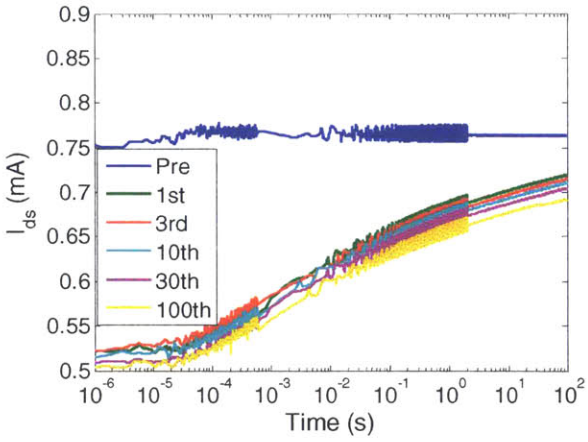


Figure 5-25: Transient Ids as a function of different numbers of pulses for the ohmic first sample.

Figure 5-24 and Figure 5-25 show the measured current for gate first and ohmic first transistors after varying numbers of gate pulses. For both the gate first and ohmic first transistors, the first gate pulse causes the largest drop in current. For example, for the gate first transistor shown in Figure 5-24, the current drops from 0.8 mA to 0.75 mA after the first gate pulse and then after the 100th pulse, the current is 0.7 mA. The change in current is logarithmically dependent on the number of pulses which is consistent with the variable pulse time measurements which showed that the degradation was logarithmically dependent on the pulse width (Figure 5-20 and Figure 5-21). However, after that, while there was some cumulative decay in current, the dynamic behavior did not change over time. This is consistent with the cumulative impact of 100 ns positive gate pulses as reported by Lagger et al. [76].

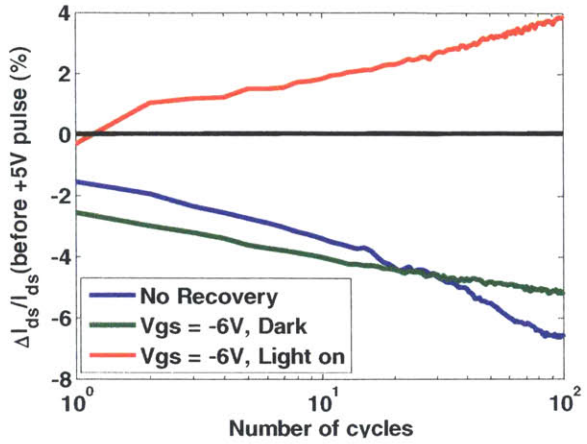


Figure 5-26: Change in I_{ds} @ 100s as a function of number of cycles for gate first sample. Note that applying light during the recovery step causes the current to *increase*

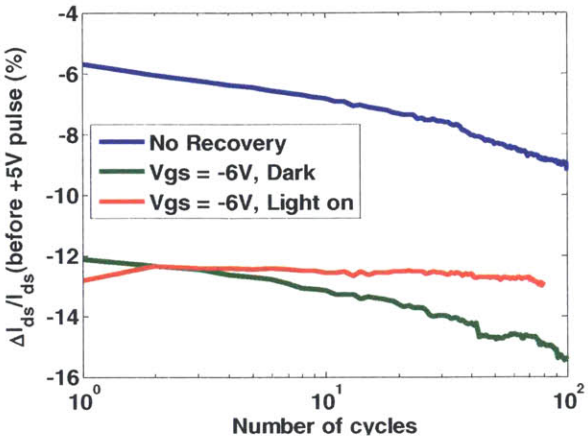


Figure 5-27: Change in I_{ds} @ 100s as a function of number of cycles for ohmic first sample. Applying light causes the change in current as a function of time to stabilize.

Figure 5-26 and Figure 5-27 show the evolution in measured I_{ds} 100s after the 5V pulse for measurements cycles without any recovery, dark negative bias recovery and illuminated negative bias recovery for the gate first and ohmic first samples respectively. For both the gate first and ohmic first samples, the dark negative bias recovery was not enough to prevent long term degradation of the drain current. However, for the gate first sample, applying a negative bias while illuminating the sample with white light caused an increase in current over time while for the ohmic first sample, it allowed the current to stabilize.

However, the transient behavior, as opposed to the absolute change in current, does not show dependence on the number of pulses as seen in Figure 5-28 and Figure 5-30 for both a gate first transistor and an ohmic first transistor. Rather, it stabilizes after the first pulse. The fitted time constants also confirm this behavior in that there is no long term change in the dominant time constants as a function of the number of pulses as shown in Figure 5-29 and Figure 5-31 for the gate first and ohmic first transistors respectively.

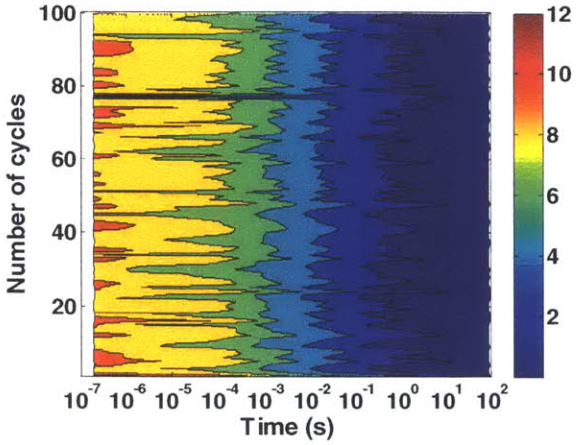


Figure 5-28: Contour plot showing relative change in current after +5V pulse as a function of time after pulse for all 100 cycles. This highlights the lack of a long term trend as a function of the number of pulses in terms of recovery.

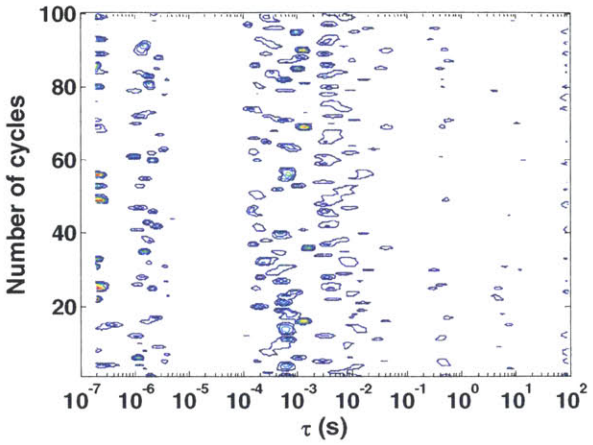


Figure 5-29: Contour plot showing evolution in fitted time constant tau as a function of the number of pulses. This is the same transistor from the gate first sample shown in Figure 5-28. The fitting parameter η = 0.3.

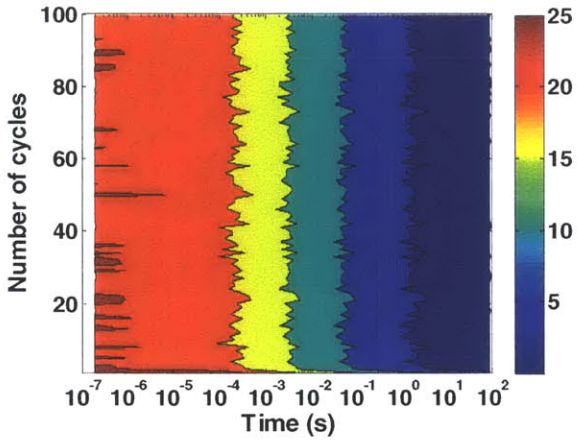


Figure 5-30: Contour plot showing relative change in current after +5V for ohmic first sample. Note that the transient behavior does not show any dependence on the number of pulses.

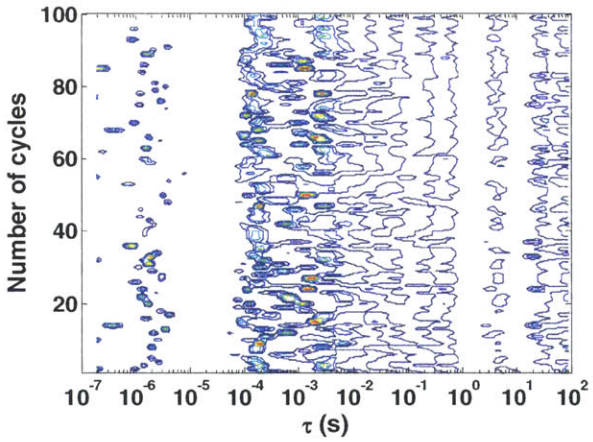


Figure 5-31: Contour plot showing evolution in fitted time constant τ as a function of the number of pulses. This is the same transistor shown in Figure 5-30.

There are several reasons why illuminating samples with light might cause an increase in current. Persistent photoconductivity was observed in AlGaN/GaN HEMTs when illuminated by light smaller than the bandgap of GaN [82]. This photoconductivity was attributed to defect levels commonly associated with yellow luminescence [83],[84], [85]. Reddy et al. showed that GaN samples without yellow luminescence do not show persistent photoconductivity [85]. At the same time, the photoconductivity related to illumination at light energies below the GaN bandgap shows a much

slower time response than illumination at the GaN bandgap [84]. Therefore, this photoconductivity does not involve creating electron hole pairs but rather it involves slowly increasing the carrier concentration by exciting electrons that are found in traps associated with yellow luminescence. An alternate theory is that shining light helps detrap trapped electrons at the interface and that these traps are emptied out, the threshold voltage shifts negative [18].

In order to look at the impact of light illumination and bias on the resulting change in current, a set of experiments was conducted where first the sample was illuminated by microscope light while a bias ranging from 0V to -10V was applied at the gate. Then, the illumination was turned off and the change in current was measured as a function of time with the gate voltage set to -6V. The measurement sequence is illustrated in Figure 5-32. Figure 5-33 and Figure 5-34 show the measured current for representative transistors from the gate first and ohmic first transistors. For both transistors, the more negative the gate bias was during the first 100s when the light was illuminated, the greater the current was in the second 100s step when the light was off and the gate bias was set to -6V. In order to help see the trends more clearly, Figure 5-35 and Figure 5-37 show the percentage increase in current at different gate biases normalized with respect to the drain current at V_{gs} = 0V for the gate first and ohmic first transistors respectively. The current was normalized with respect to I_{ds} at V_{gs} = 0V in order to help see how much the increase in carriers compares to the total number of carriers in the 2-DEG electron gas. The gate first transistor exhibits a greater change in current than the ohmic first transistor (up to 22% for the gate first sample vs 7 % for the ohmic first sample) but for both samples the more negative the gate bias, the greater the increase in current. After the microscope light was turned off, the current for the gate first sample had an increase in current equivalent to 32% of I_{ds} @ V_{gs} = 0V while the current for the ohmic first sample had an increase in current equal to 21% of I_{ds} @ V_{gs} = 0V (Figure 5-36 and Figure 5-38).

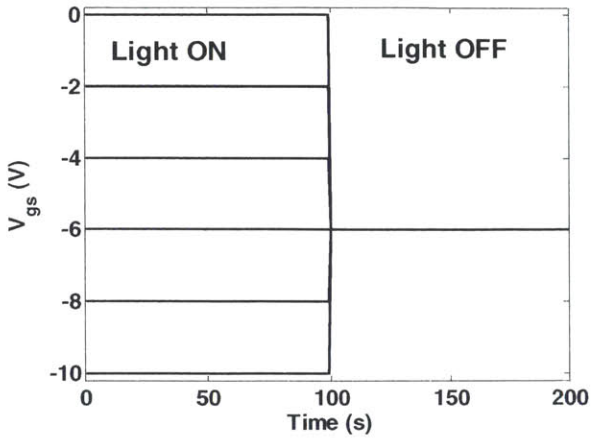


Figure 5-32: Schematic of the timing of the bias and lighting. The light was on for the first 100s while the transistor gate was biased at anywhere from 0V to -10V. Then, with the light

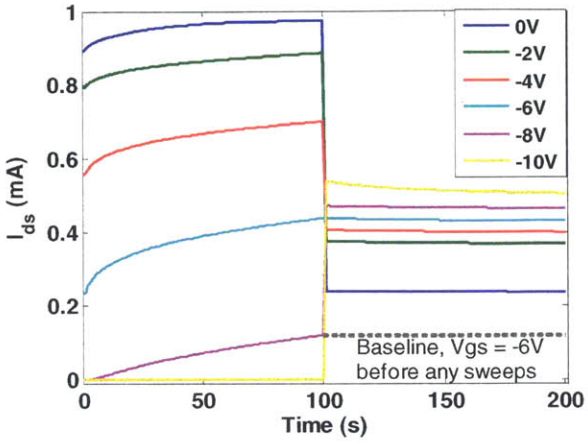


Figure 5-33: Example of Ids vs Time for gate first sample with the biasing/illumination scheme shown in Figure 5-32.

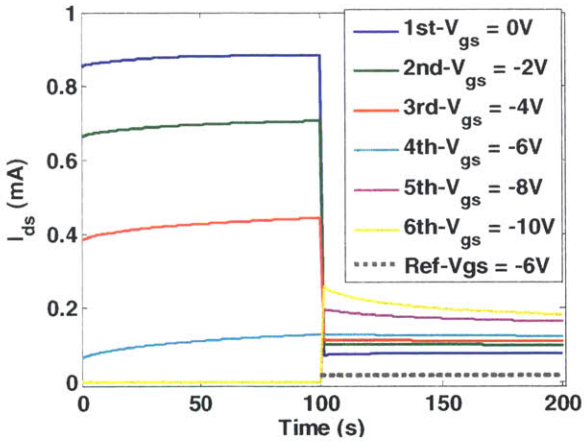


Figure 5-34: Example of Ids vs time for ohmic first sample with the biasing/illumination scheme shown in Figure 5-32. Note that change in current is smaller than the gate first sample

When the applied bias gets more negative, the electric field in the AlGaN is larger. Therefore, any electrons that are detrapped by the light are more likely to end up in the 2DEG. As a result, applying a more negative bias causes more electrons to detrap and for the current to increase.

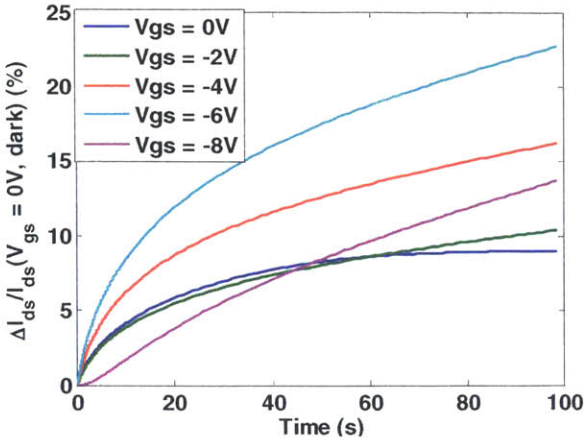


Figure 5-35: Gate first sample: Plot of increase in current during 100s of microscope light illumination as shown in Figure 5-33. Change in current is normalized with respect to current in the dark at Vg = 0V to get idea of relative change in Ns due to illumination. Note that gate first sample has larger increase in current than the ohmic first sample.

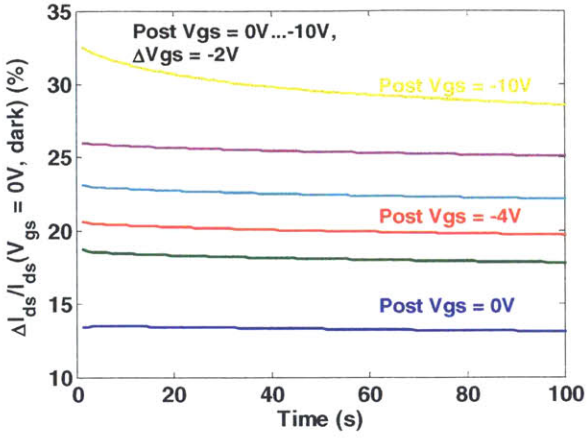


Figure 5-36: Gate first sample. Plot of relative change in current after 100s of illumination. As described in (), the gate bias is equal to -6V. The change in current is normalized with respect to Ids(Vg = 0V, dark).

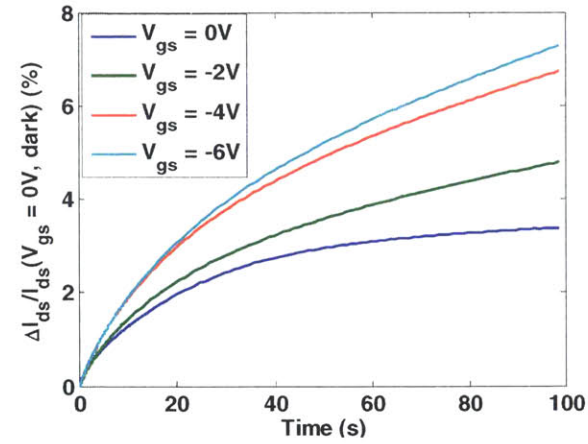


Figure 5-37: Ohmic First sample. Plot of normalized increase in current during 100s of microscope light illumination shown in Figure 5-34. Note that change in current is much smaller than for gate first sample

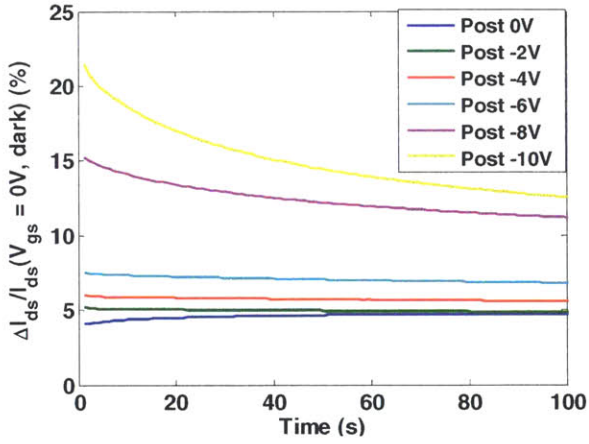


Figure 5-38: Ohmic first sample. Plot of relative change in current after 100s of illumination with a gate bias of -6V. The change in current is normalized with respect to I_{ds} (V_{gs} = 0V, dark). Note that the relative change in current is significantly smaller than the gate first transistor.

The larger increase in current for the gate first transistor than the ohmic first transistor (Figure 5-36 vs Figure 5-38) after illuminating with light during negative bias can explain why the gate first transistor showed an increase in current because of the negative gate voltage + microscope light recovery test.

Positive Gate Pulsed IV measurements

Having seen the impact and recovery behavior of transistors after a single positive gate pulse, pulsed-IV measurements were conducted where the evolution in I_D- V_{ds} and I_D-V_{gs} measurements as a function of the quiescent gate bias was measured.

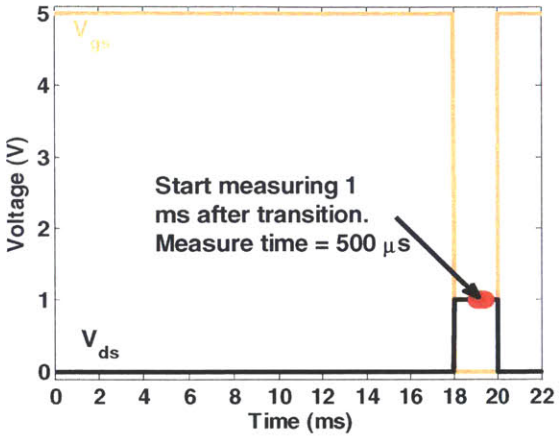


Figure 5-39: Timing schematic for positive gate pulse PIV measurements. The $V_{G,Q}$ value (the V_{gs} value for t < 18 ms), would vary from 0V to 5V while the $V_{D,Q}$ value was set at 0V.

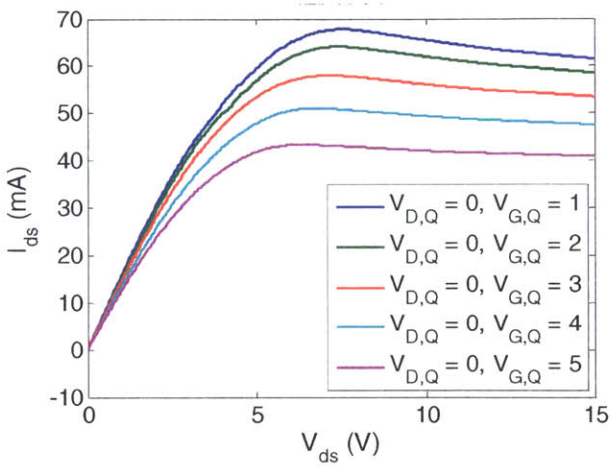


Figure 5-40: Example of Pulsed I_D-V_{gs} measurements as a function of increasing $V_{G,Q}$ values. As the $V_{G,Q}$ value increased, more electrons were trapped which manifested itself as a larger shift in threshold voltage.

The evolution in the I_D- V_{ds} characteristics is consistent with a change in V_{th} as seen in Figure 5-40. Unlike drain lag measurements, the drain access resistance does not change. Therefore, the reduction in current is due to charge depletion below the gate as opposed to a change in access resistance.

Below are representative I_D-V_{gs} plots and g_m plots for gate first and ohmic first devices. There is a decrease in gm with an increase in $V_{G,Q}$. Given that for devices biased in the low field linear region, this is indicative of mobility degradation. More importantly, even though there is a voltage shift with the $V_{G,Q}$ = 0V sweep after the 5 V sweep, the g_m does not show signs of degradation.

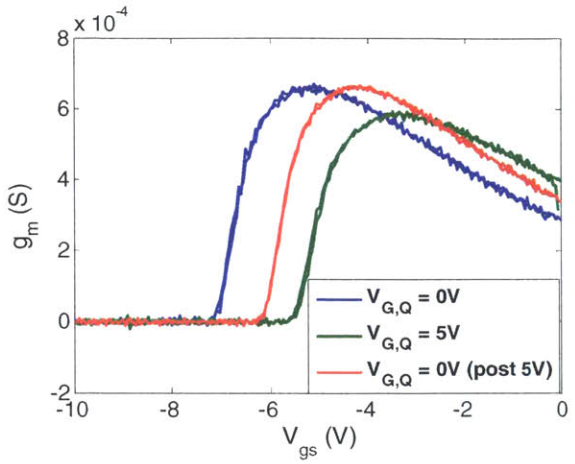


Figure 5-41: g_m vs. V_{gs} for representative gate first transistor as a function of $V_{G,Q}$. Note that there is a drop in gm for the $V_{G,Q}$ = 5V sweep

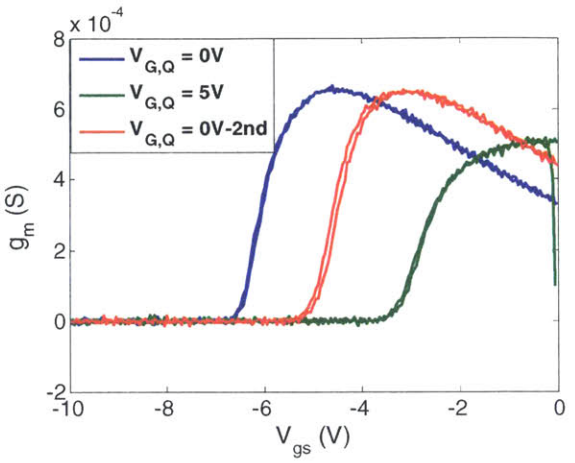


Figure 5-42: g_m vs V_{gs} for representative ohmic first transistor as a function of $V_{G,Q}$. Note that there is a similar drop in gm as what is seen in Figure 5-41.

In order to quantify the change in mobility, first simultaneous CV and IV measurements were performed. The drain bias was set to 50 mV in order to ensure that the device was in the low field limit [86]. For circular transistors, the relation between I_{ds} and V_{ds} is given as [87],[88] the following relationship holds between I_d and V_{gs} and V_{ds}. The geometric identities are defined in Figure 5-43.

$$I_D = f\mu_e C_{ox}(V_{GS} - V_T)V_D, f = 2\pi/(\ln\left(\frac{R_2}{R_1}\right)$$

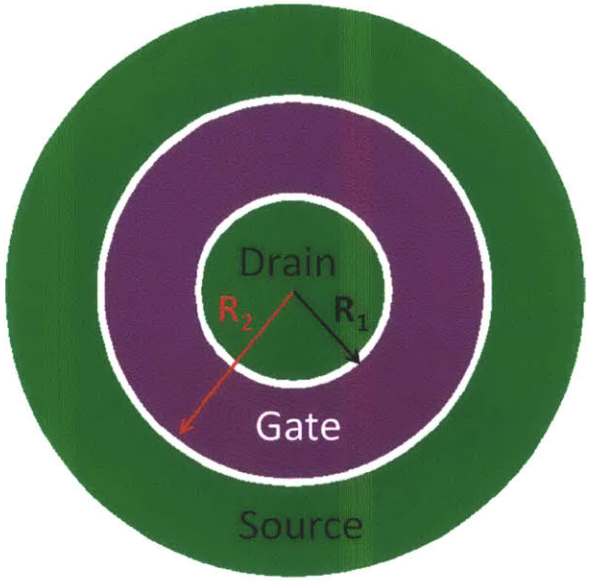


Figure 5-43: Schematic of circular transistor used for measurements. Rd, the radius of the drain, is 50 µm. L_{dg}, the distance between the gate and drain, is 5 µm. The gate length L_g is 50 µm. R1 = R_{dg} + Rd = 55 µm. R2 = L_g + R_{dg} + Rd = 105 µm

Therefore, the mobility is calculated by the following expression

$$\mu_e = \frac{I_d}{(QV_{ds}f)}, Q(V_{gs}) = \int_{V_t}^{V_{gs}} C(V_{gs} - V_t)dV_{gs}$$

In order to perform simultaneous CV-IV measurements, the signal path for the AC signal used for the impedance measurement must not get shorted by the SMU used to measure the DC current. In order to decouple the DC ground from the AC low, the source and drain of the transistor were connected to two different Picosecond Pulselab 5575A Bias-Ts as illustrated in Figure 5-44. The AC signal was blocked from the DC SMU and therefore only went to the LO channel of the impedance analyzer. At the same time, the DC current was blocked from the impedance analyzer and only went to the SMU. The low cutoff frequency for the 5575A Bias-T was 10 kHz for the currents in use and thus was low enough to use a measurement frequency ranging from 200 kHz to 1 MHz without any signal decay due to the low cutoff frequency limit. An Agilent B2902A SMU was used for sourcing the DC currents while CMU unit on the Agilent B1505A or the Boonton 7200 CV meter were used for measuring capacitance. Figure 5-45 shows a resulting simultaneous CV and I_d-V_{gs} measurement from this setup.

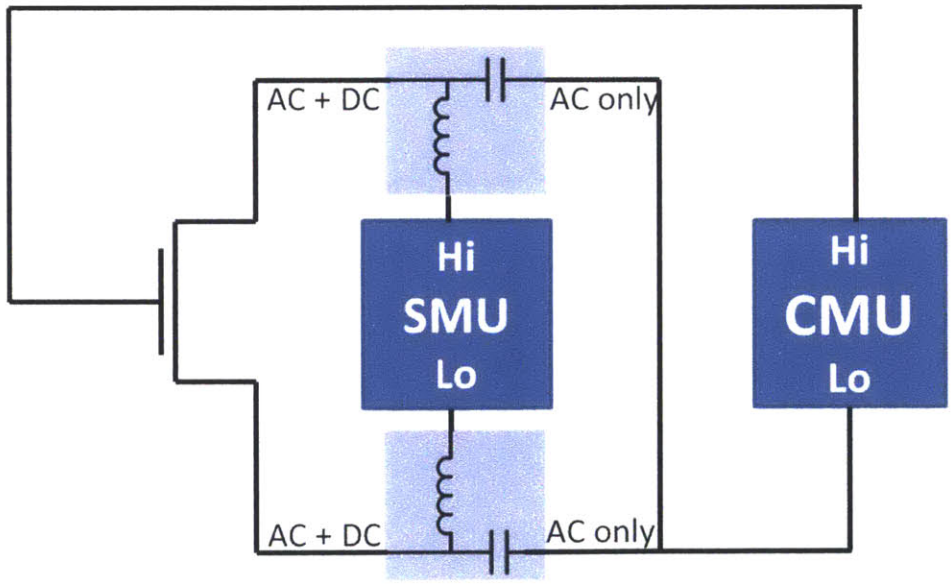


Figure 5-44: Measurement setup for performing simultaneous CV-IV measurements in order to calculate mobility. The Bias-Ts(highlighted in blue) allow for decoupling the AC signal used to measure capacitance from the DC current source from the SMU

The access regions were 5 μm on both the drain side and the source side. Given that the gate length of the device was 50 μm, the drain voltage drop across the contacts and access regions can get appreciable and if the drain voltage drop is not taken into account, the drain voltage across the intrinsic transistor will be overestimated [89]. The contact resistance and sheet resistance was determined by performing transmission line measurements (TLM). Using the methodology discussed by Marlow et al. to extract contact resistances for circular TLM structures, the access resistances were determined to be equal to the following [90]:

$$R_{access} = \frac{R_{sh}}{2\pi}\left(\ln\left(\frac{R_d + L_{gd}}{R_d}\right) + \ln\left(\frac{R_d + L_g + L_{gs} + L_{gd}}{R_d + L_g + L_{gd}}\right) + \frac{R_c}{R_{sh}}\left(\frac{1}{R_d} + \frac{1}{R_d + L_g + L_{gd} + L_{gs}}\right)\right)$$

The access resistance expression above takes both the sheet resistance of the drain side, the source side and the contact resistance of both the drain and source side. Given the circular geometry, the drain side access region and contact resistances were larger than the source side access region and contact resistances. By taking the R_{access} and R_{cable} (measured to be around 4 ohms) into account when calculating the mobility, mobility curves were calculated for a representative gate first transistor. TLM structures were measured across the wafer and in order to illustrate the impact of variation on the TLM measurements, the mobility was calculated for the 25th, 50th and 75th percentiles of the R_{access} distribution shown in Figure 5-46.

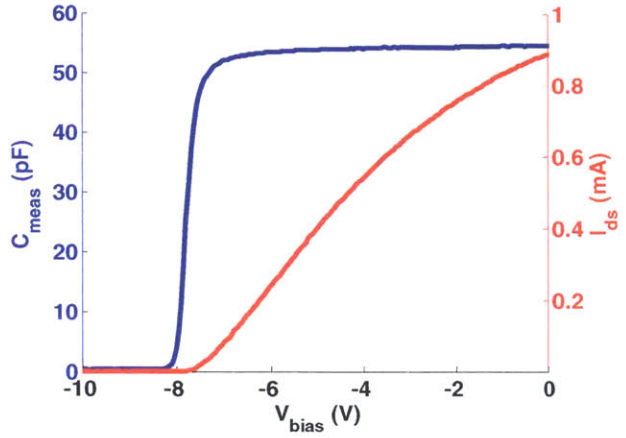


Figure 5-45: Simultaneous CV and Id-Vgs measurement of a gate first transistor that is used to calculate mobility. V_{ds} = 50 mV for this measurement

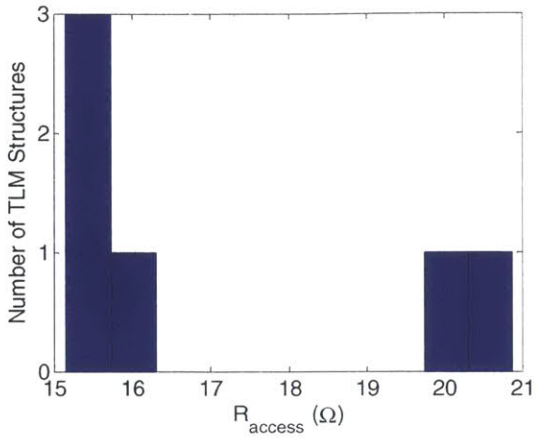


Figure 5-46: Distribution of calculated access resistances based on different TLM structures on the gate first sample. Given this variation, it is important to look at how this impacts the calculated mobility.

Figure 5-47 shows the calculated mobility for the gate first transistor plotted in Figure 5-45. By taking the median TLM access resistance and cable resistance into account, the peak measured mobility increases from 1400 $cm^2/V/s$ to 1800 $cm^2/V/s$. The access resistance correction is validated because the access resistance corrected mobility value is consistent with Hall mobility values that range from 1800 – 2000 $cm^2/V/s$.

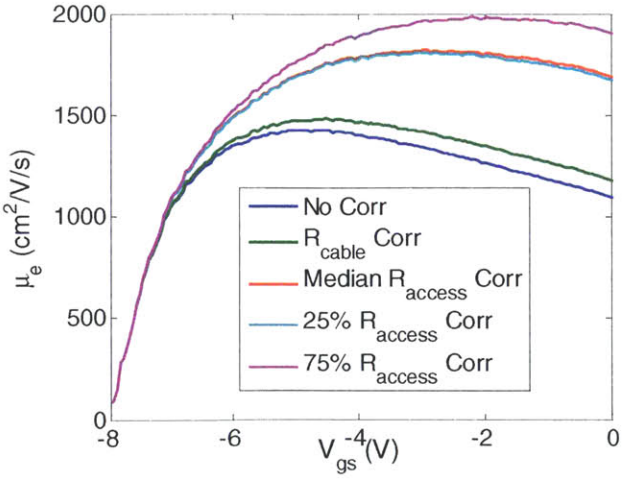


Figure 5-47: Calculated electron mobility vs Vgs for the gate first device plotted in Figure 5-45. Accounting for the access resistance (Figure 5-46) and the 4 ohm cable resistance makes a great difference in the calculated mobility.

In order to calculate the change in mobility, first the CV-IV measurement were performed on selected transistors from both samples. Then, pulsed I_D-V_{gs} measurements were done and the data from the two experiments was used together in order to estimate the mobility. In order to account for the change in threshold voltage, the current from the CV-IV measurements was used as a reference to determine the change in threshold voltage. Then, the CV curves were translated by that amount and then the mobility curves were calculated from the pulsed I_D-V_{gs} current and the translated CV curve as shown in Figure 5-48 and Figure 5-49.

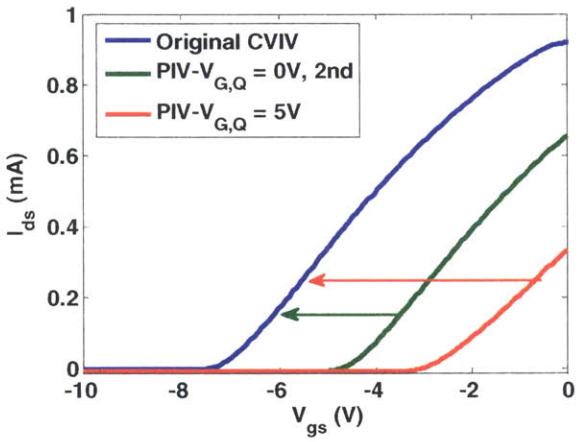


Figure 5-48: Ohmic First Transistor. This is a I_D-V_{gs} plot of the original IV-CV measurement, the pulsed-IV measurement with a $V_{G,Q}$ = 0V (after the 5V sweep) and the pulsed-IV measurement with a $V_{G,Q}$ = 5V.

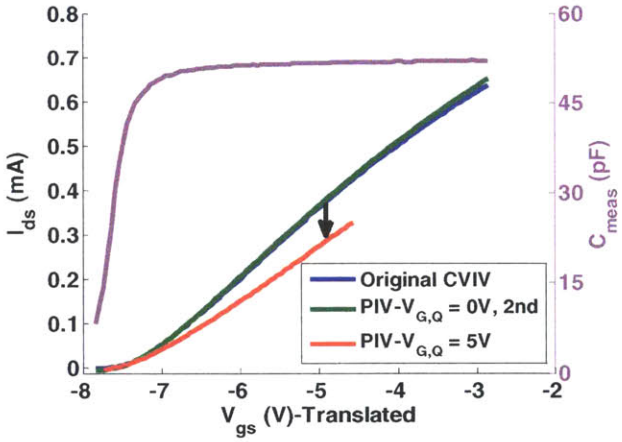


Figure 5-49: This is the same ID-V_{gs} measurements shown in Figure 5-48 except the different ID-V_{gs} curves have been translated. Note that the $V_{G,Q}$ = 5V curve has a lower I_{ds} than the other two curves even after the translation. This is attributed to a reduction in electron mobility.

Once the I_D-V_{gs} curves were translated such that the threshold voltages were aligned as shown in Figure 5-49, the electron mobility were calculated from the pulsed ID-VGS measurements for different devices and different $V_{G,Q}$ bias points. For a given carrier concentration, the drop in mobility during the $V_{G,Q}$ = 5V I_D-V_{gs} sweep for the gate first transistor is up to 230 $cm^2/V/s$ (Figure 5-50) while for the ohmic first transistor, the mobility drops by up to 500 $cm^2/V/s$ (Figure 5-51).

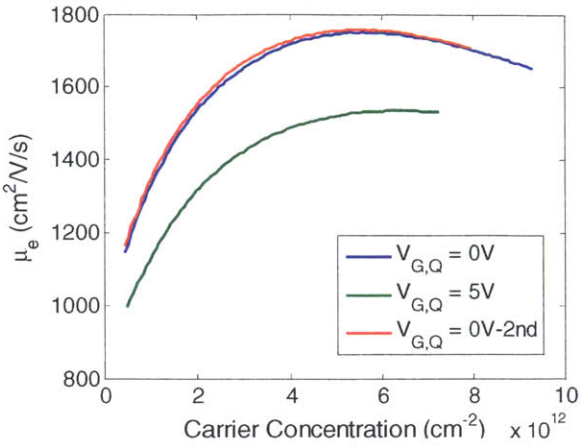


Figure 5-50: Calculated mobility curves from pulsed I_D-V_{gs} measurements of same transistor in Figure 5-41. Increasing $V_{G,Q}$ causes a degradation in mobility

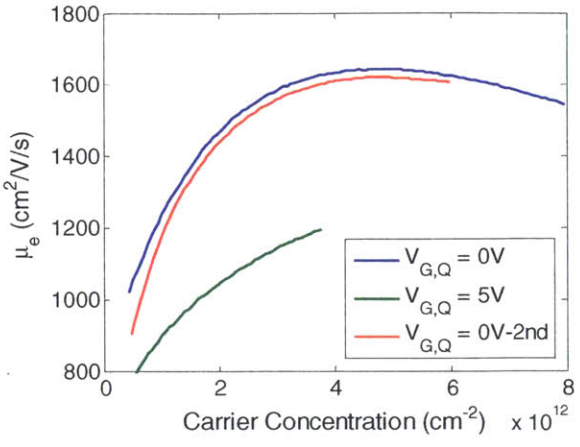


Figure 5-51: Calculated mobility curve from pulsed I_D-V_{gs} measurements of ohmic first transistor shown in Figure 5-42.

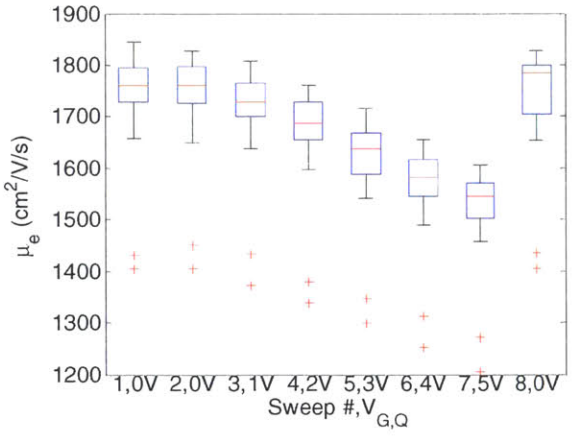


Figure 5-52: Calculated maximum electron mobility as a function of the number of sweeps and $V_{G,Q}$ for the gate first sample. Note that during the eighth sweep when $V_{G,Q}$ = 0V, the mobility has recovered completely. This suggests that the mobility degradation might be related to the charge recovery process as opposed to being related to an absolute change in threshold voltage.

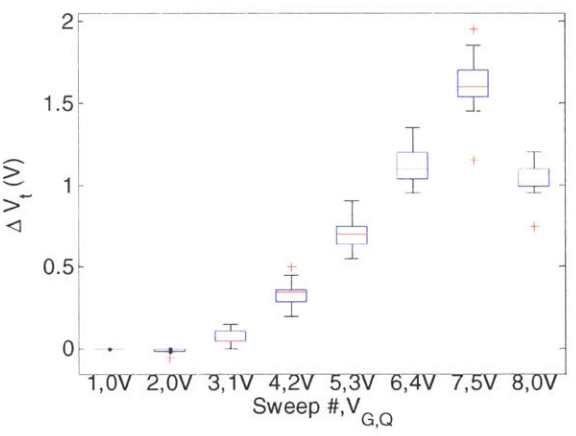


Figure 5-53: The change in threshold voltage with respect to the first sweep with $V_{G,Q}$ = 0V for the gate first sample. Note that the 8th sweep with $V_{G,Q}$ = 0V has a V_{th} shift of 1V with respect to the original.

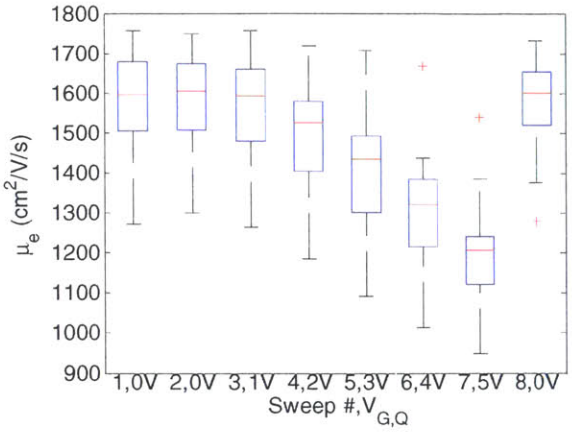


Figure 5-54: Calculated maximum electron mobility as a function of the number of sweeps and $V_{G,Q}$ for the ohmic first sample. In comparison to the gate first sample, there is more substantial mobility degradation. However, just like the gate first sample, the mobility for the eighth sweep is as high as the initial sweeps before any positive gate pulses.

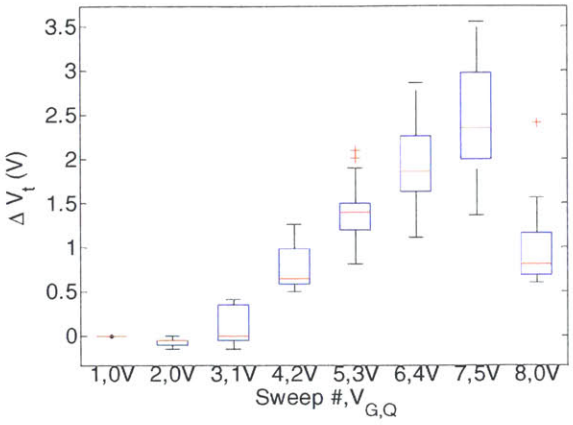


Figure 5-55: The change in threshold voltage with respect to the first sweep with $V_{G,Q}$ = 0V for the ohmic first sample.

For the gate first and ohmic first samples, the change in V_{th} on the eight sweep ($V_{G,Q}$ = 0V sweep after the $V_{G,Q}$ = 5V sweep) was equal to the change in V_{th} during the $V_{G,Q}$ = 4V and $V_{G,Q}$ = 2V sweeps respectively as shown in Figure 5-53 and Figure 5-55. However, despite having the same V_{th}, the mobility for the gate first sample drops from 1780 cm^2/V/s to 1580 cm^2/V/s as shown in Figure 5-52. This indicates that the drop in mobility is not due to the absolute change in N_s but rather is due to an additional source of coulomb scattering. For example, charged defects caused by irradiation of AlGaN/GaN samples has been cited as a cause of drop in electron mobility [91],[92]. One possibility is that as charges detrap from the Al_2O_3/AlGaN interface, they pile up at the AlGaN/AlN interface and cause Coulomb scattering as illustrated in Figure 5-56. The physical distance then of these electrons is small enough to cause Coulomb scattering. Until these carriers tunnel through the AlN barrier, they cause Coulomb scattering and deplete the 2-DEG. The proposed current recovery mechanism involving tunneling through the AlN interlayer is consistent with the fact that for gate first transistors with a good interface, the recovery was not dependent on temperature.

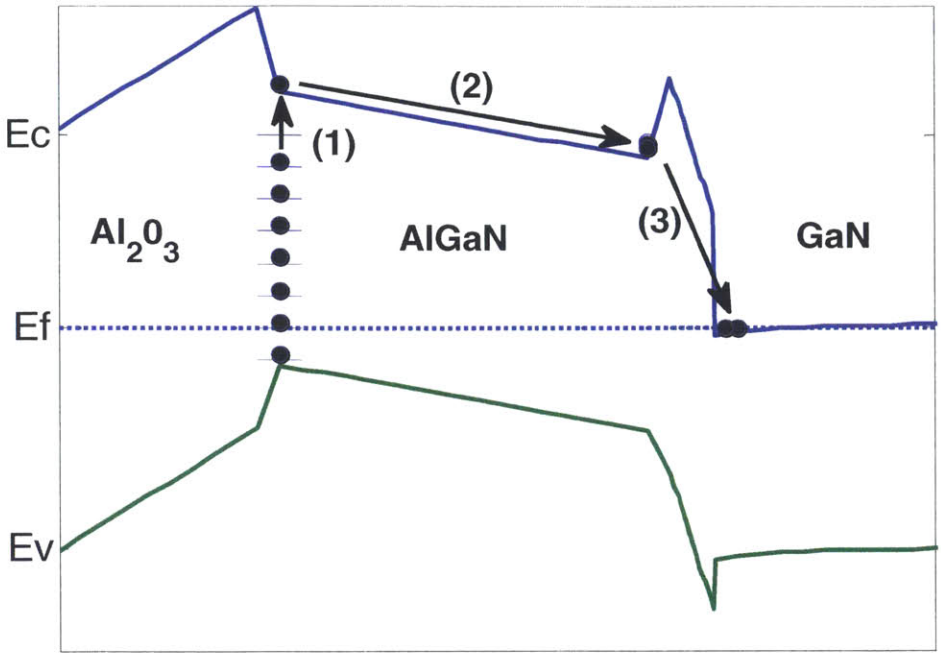


Figure 5-56: Schematic showing electron detrapping process. 1) First trapped electrons at Al_2O_3/AlGaN interface detrap and get injected into Ec. 2) Electrons roll down to the AlGaN/AlN interface where they pileup because of the ΔE_c between AlGaN and AlN. These trapped electrons are close enough to 2-DEG electron gas in order to cause Coulomb scattering. 3) Trapped electrons tunnel into 2-DEG as final stage of recovery

Both the change in carrier concentration and the change in mobility contribute to the change in the output conductivity g_o given the following relationship between g_o, μ_e and N_s.

$$g_o(V_{gs}) \propto \mu_e N_s(V_{gs})$$

However, a convenient assumption to make is that the mobility degradation can be neglected when looking at the change in current due to traps getting charged at the AlGaN/oxide interface after positive gate pulses [19]. Lagger et al. noted that this can be justified by the fact that the Al_2O_3/AlGaN interface is up to 20 nm away from the channel [76]. However, in order to illustrate this, the product of μ_e*Ns is plotted as a function of gate bias for $V_{G,Q}$ = 0V, $V_{G,Q}$ = 5V and a third hybrid which consists of $\mu_e(V_{G,Q} = 0V)*N_s(V_{G,Q} = 5V)$. The difference between the μ_e*N_s for $V_{G,Q}$ = 5V and $\mu_e(V_{G,Q} = 0V)*N_s(V_{G,Q} = 5V)$ curves indicates the role of mobility degradation in the drop in current. As shown in Figure 5-57 and Figure 5-58, while the majority of reduction on output conductance is due to charge depletion, mobility

degradation can account for up to around 20% of the reduction in current for the gate first and ohmic first transistors. Therefore, the change in current can still be used as a proxy for the number of carriers being trapped but there will be some inaccuracy due to mobility degradation.

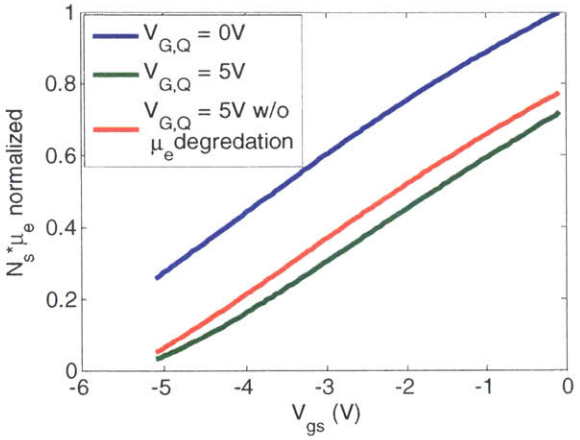


Figure 5-57: Gate first sample. The blue and green lines are the products of $N_s*\mu_e$ for the $V_{G,Q}$ = 0V and $V_{G,Q}$ = 5V cases. The red line shows what the degradation would look like if the mobility were equal to the $V_{G,Q}$ = 0V case but the carrier concentration was equal to the $V_{G,Q}$ = 5V. As can be seen by the red line, at least 80% of the degradation in current can be attributed to the change in V_{th} while the rest is because of the change in electron mobility.

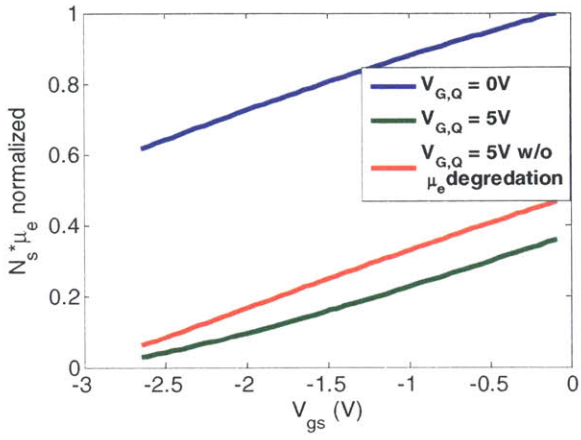


Figure 5-58: Ohmic First sample. Equivalent plot as Figure 5-57. Note that an even greater percentage of the drop in current can be attributed to the change in V_{th}.

Summary

To summarize, the following findings have been made through transient current measurements:

- Transistors with a poor interface display a combination of thermally activated trapping together with tunneling. This is shown by the temperature dependence on the recovery where elevating the temperature causes faster recovery for the ohmic first samples.
- When transistors have a good Al_2O_3/AlGaN interface, the recovery is believed to be limited by tunneling. The following trends confirm tunneling. First, the recovery for the gate first sample was shown to be temperature independent. Second, the recovery was shown to be dependent on the base voltage which again is consistent with a tunneling based recovery.

- Both samples show evidence of some very slow trapping as evidenced by the long term trends. However, these long term traps do not impact the transient behavior within the first 100s after the gate pulse.
- Pulsed I_D-V_{gs} measurements coupled with CV-IV measurements indicate that up to 20% of the current drop seen may be attributed to degradation in mobility as opposed to a change in carrier concentration.

Chapter 6 Optimizing Gate First Processes

As shown in Chapter 4 and Chapter 5, the gate first process yields a good AlGaN/oxide interface with electrical properties that are not skewed by organic contamination at the interface. Therefore, the samples fabricated using a gate first process can be used to study other factors that can impact the oxide. These factors include the following which will be studied in this chapter:

- The impact of initial nucleation layers on the interface
- The impact of an AlN interlayer
- The impact of annealing conditions on electrical performance
- The impact of oxidation on breakdown voltage performance

Impact of nucleation layer

The initial surface condition of a semiconductor greatly impacts the ability for initial dielectric layers to form when deposited by atomic layer deposition. For example, hydrogen terminated Si caused incomplete surface coverage by HfO_2 in comparison to oxidized Si surfaces [93]. Also, oxidized GaN is also shown to facilitate more uniform Al_2O_3 growth [94]. Incomplete growth initialization causes islanding to occur, which in turn results in greater roughness at the semiconductor/insulator interface. Initial surface roughness has been shown to be linked to greater hysteresis in Al_2O_3/GaN capacitors [62] and greater leakage in SiO_2/Si capacitors [95],[96].

In order to study the impact of nucleation layers on the electrical characteristics of capacitors, an experiment was conducted where the dosage factor of the first four layers was varied before proceeding with a standard oxide deposition recipe. These experiments were performed with the

Oxford FlexAl tool since it allowed for setting deposition pressures independently of the N_2 gas flow and the dose times. This allows for more precise control of dosage than with the Cambridge Nanotech ALD tool, which does not allow for changing the pumping rate to adjust the deposition pressure. The dose of the precursors was controlled both by varying the pulse time and by adjusting the deposition pressure. Increasing the pressure during the pulse period resulted in a larger exposure since the deposition pressure was correlated to the pumping rate. Table 8 shows the different conditions that were used for this experiment.

Condition	TMA Pulse Time	DI Pulse Time	Deposition Pressure
Standard Dose (StdDose)	30 ms	100 ms	80 mTorr
High Dose (HiDose)	300 ms	300 ms	80 mTorr
High Dose with High Pressure (HiPressure)	300 ms	300 ms	200 mTorr

Table 8: Dosing Conditions for ALD nucleation study

Samples were processed using the same gate first process detailed in 0 with the only difference that the Oxford FlexAl ALD tool was used. The deposition temperature was 300°C and after the nucleation layer was deposited, another 240 cycles of Al_2O_3 were deposited using the standard dose conditions. In addition to the processed samples, a set of samples was prepared for AFM studies where only the nucleation layers were deposited. AFM studies were performed in order to see the difference in surface roughness as a function of deposition conditions.

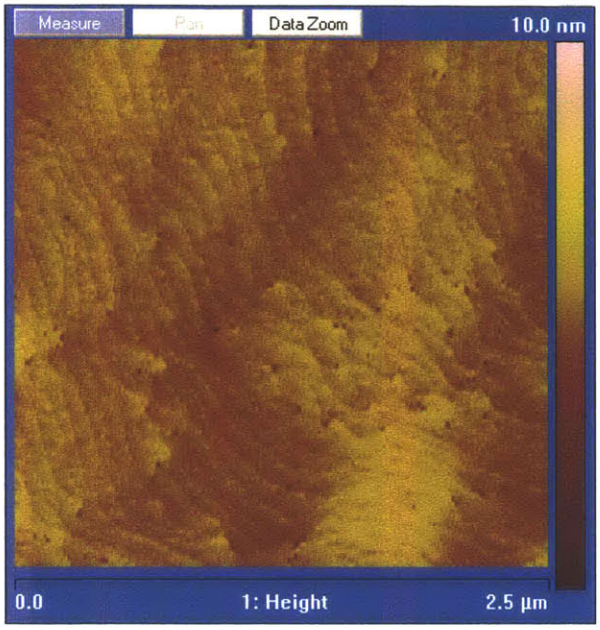


Figure 6-1: AFM scan of AlGaN/GaN substrate with 4 cycles of the Standard Dose nucleation layers. R_a = 0.307 nm

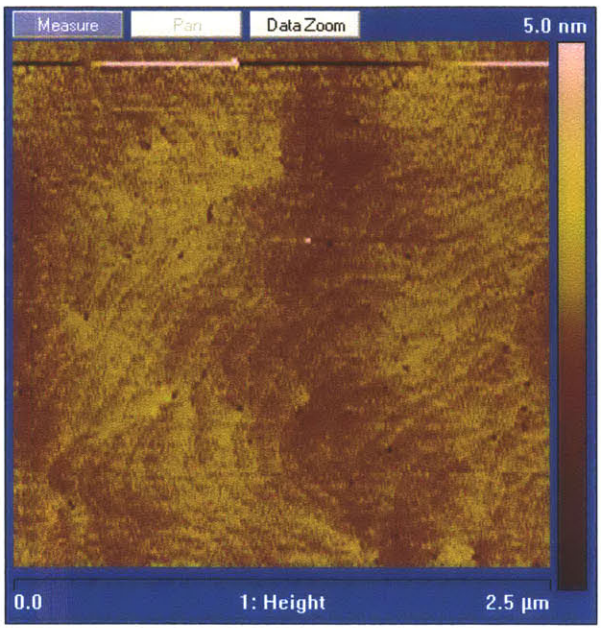


Figure 6-2: AFM scan of AlGaN/GaN substrate with 4 cycles of the high dose nucleation layers. R_a = 0.23 nm

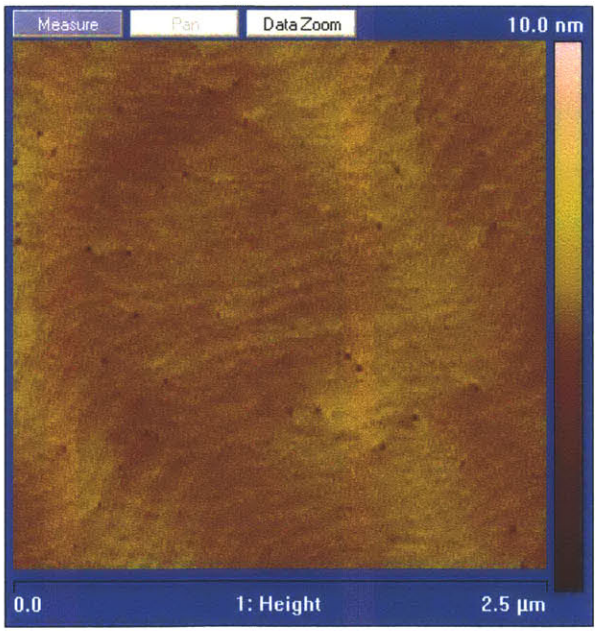


Figure 6-3: AFM scan of AlGaN/GaN substrate wit 4 cycles of the high pressure nucleation layers. R_a = 0.20 nm

Electrical Characterization of different nucleation layers

The same set of CV and IV characterization techniques used to perform the comparison between gate first and ohmic first samples were used to differentiate between the different samples.

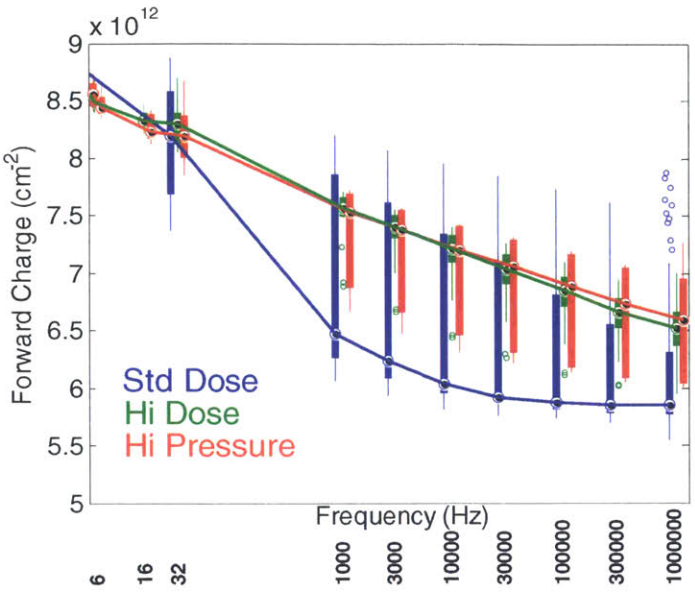


Figure 6-4: The variation in forward charge as a function of frequency. The standard dose samples show the greatest amount of frequency dispersion. This behavior is consistent with the degradation seen for the ohmic first transistors

As seen in Figure 6-4, the sample with the StandardDose initialization layer shows the worst frequency dispersion behavior. Positive gate Pulsed I_d-V_{ds} measurements were also performed in order to correlate transistor behavior to capacitor behavior. The degradation in current as a function of quiescent gate bias ($V_{G,Q}$) was characterized by looking at the change in on-resistance (R_{on}) and maximum current ($I_{ds,max}$) as seen in Figure 6-5.

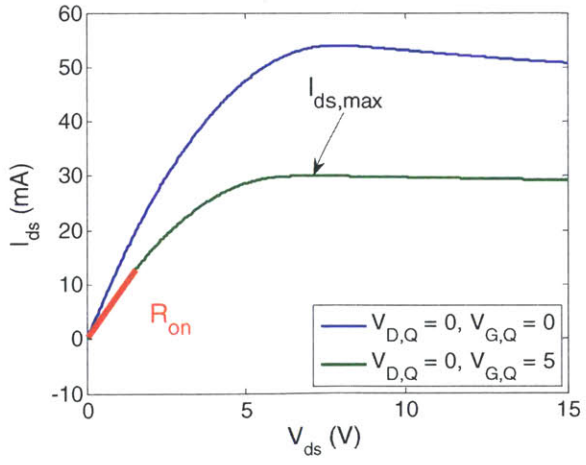


Figure 6-5: Representative positive gate Pulsed I_D-V_{DS} measurements. The change in R_{on} and $I_{ds,max}$ is plotted for the different nucleation conditions in Figure 6-6 and Figure 6-7.

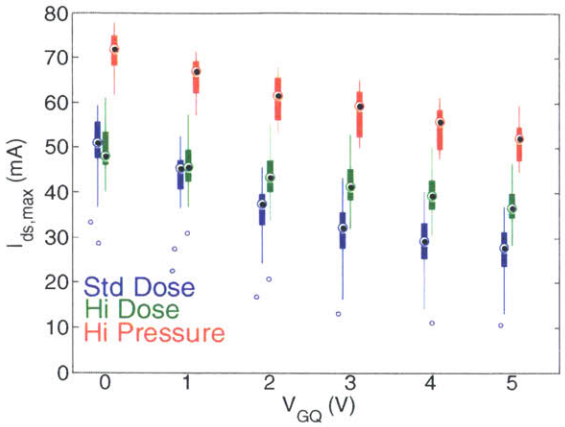


Figure 6-6: Evolution in Ids,max as a function of $V_{G,Q}$. Hi Pressure samples show least amount of degradation.

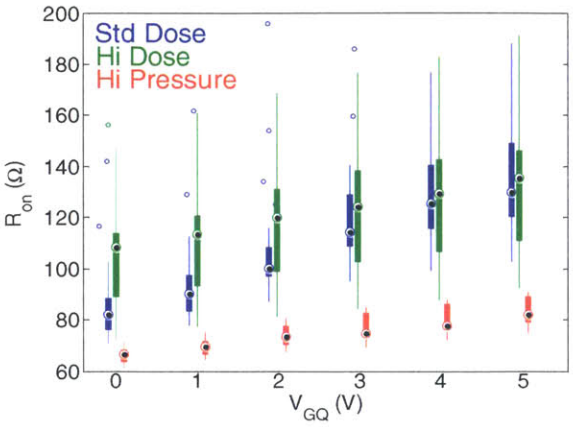


Figure 6-7: Evolution in R_{on} as a function of $V_{G,Q}$. Hi Pressure samples show least amount of degradation.

Positive gate pulsed IV measurements also show that the Hi Pressure samples show the least amount of degradation both in terms of $I_{ds,max}$ (Figure 6-6) and R_{on} (Figure 6-7) as a function of larger $V_{G,Q}$ values. This is consistent with the forward bias CV measurement results which show that the standard dose sample has the greatest amount of frequency dispersion.

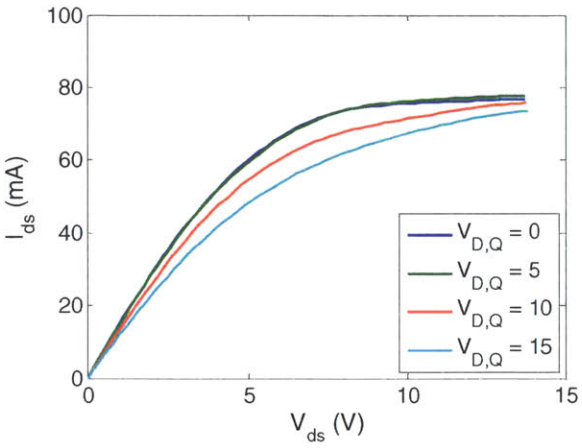


Figure 6-8: Drain lag measurements for standard dose transistor

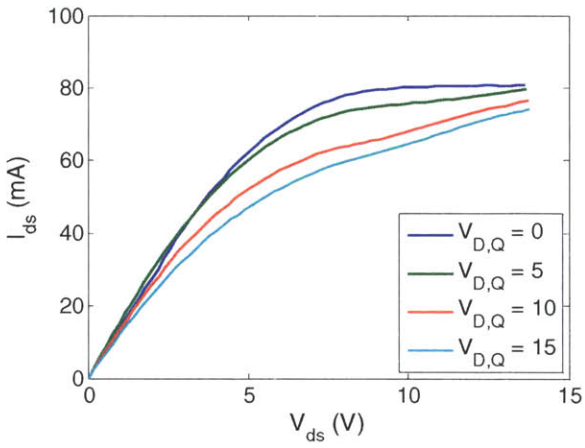


Figure 6-9: Drain lag measurements for high dose transistor

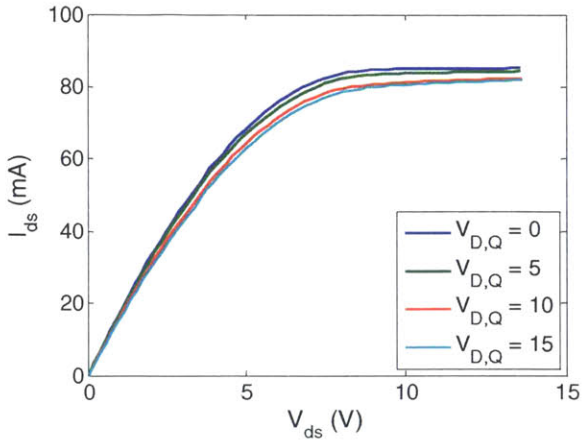


Figure 6-10: Drain lag measurements for high pressure transistor.

As can be seen by Figure 6-8, Figure 6-9 and Figure 6-10, the high pressure sample shows the least amount of current collapse after drain lag measurements. This is also consistent with the CV measurements.

Transient current measurements were also performed on the HighPressure sample and the StdDose sample across different temperatures ranging from 25°C to 205°C and with different base voltages. The StdDose samples showed more initial decay and a greater dependence on temperature for recovery as seen in Figure 6-12. This is similar to the behavior of the ohmic first samples, which also had greater frequency dispersion in high bias CV measurements. At the same time, the high pressure sample, which exhibited low forward bias CV dispersion like the gate first capacitors, showed less temperature dependence on the recovery rate and less degradation immediately after the pulse as seen in Figure 6-11.

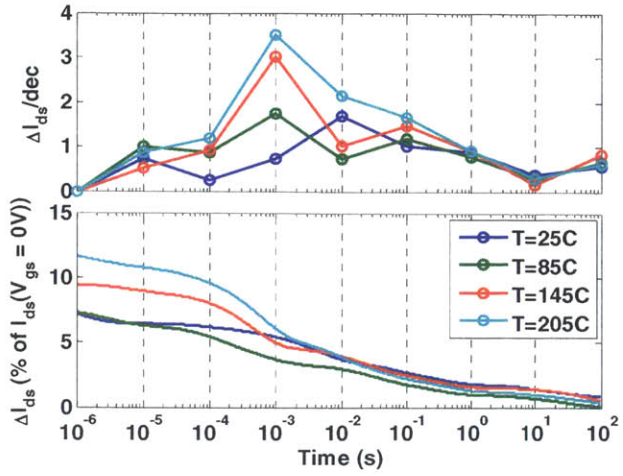


Figure 6-11: HiP-VBase = 0V. There is weak temperature dependence on the recovery. For all temperatures, the greatest recovery occurs between 10^{-4} s and 10^{-2} s.

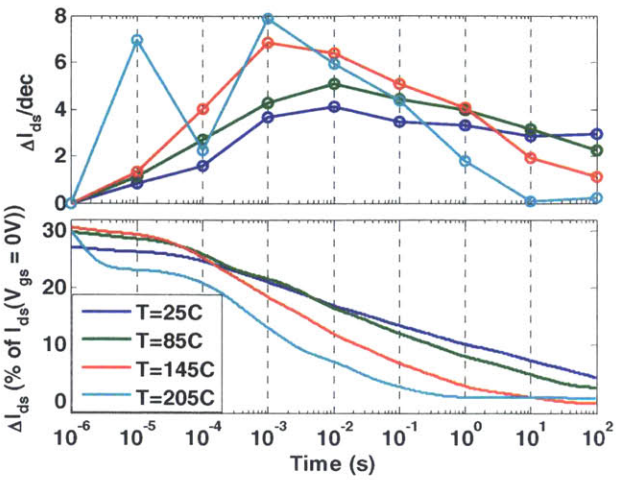


Figure 6-12: StdDose-VBase = 0V. There is a strong temperature dependence on the recovery

At the same time, elevating the temperature and applying a more negative bias accelerated the recovery process for the StdDose sample. Note that for the high pressure sample, even at 205°C, the current recovery approaches 0%, meaning that it does not exceed the measured current before the gate pulse (Figure 6-13). On the other hand, for the Standard Dose sample, the recovery is achieves negative values at both T = 145°C and 205°C, meaning that there is more current than before the 5V pulse (Figure 6-14). This indicates that the combination of temperature and reverse bias for the Standard Dose sample is enough to detrap the trapped electrons that had accumulated over previous measurements.

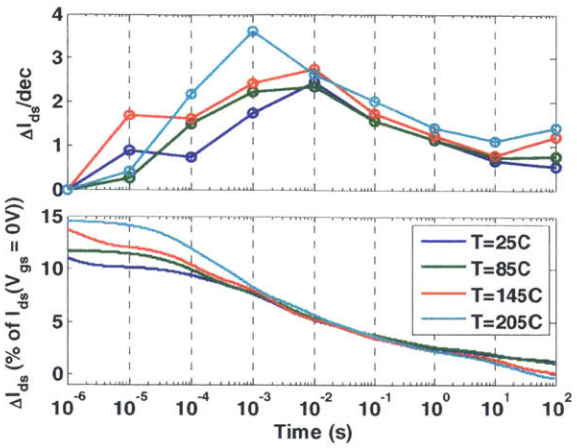


Figure 6-13: HiP-V_{Base} = -4V. Note that there is very little dependence on temperature and that the recovery does not go below 0%.

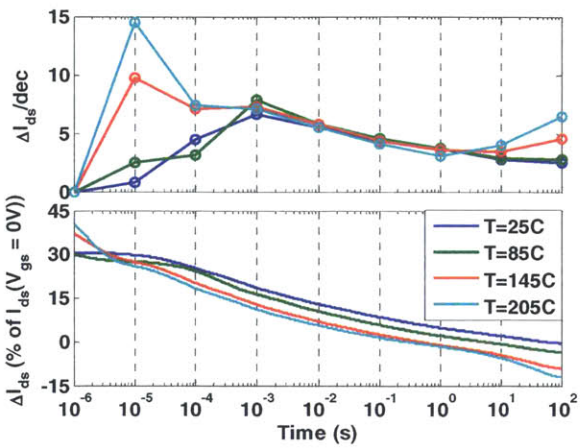


Figure 6-14: StdDose V_{Base} = -4V. Note that when T ≥ 145°C, the current during the recovery exceeds the value before the 5 V pulse. This is indicative of detrapping of slow traps that did not detrap within 100s at lower temperatures.

Nucleation of ALD had been found to play a large role in determining the quality of the AlGaN/Al_2O_3 interface. The Standard dose sample had an Al_2O_3 dielectric that was deposited with insufficient nucleation doses and as a result, it show trapping behavior similar to that of the ohmic first sample. This is noteworthy for it indicates that simply having a clean interface is not sufficient to ensure a good interface. Rather, attention must also be given to the nucleation steps to ensure a good interface.

Impact of AlN interlayer

The previous studies have been performed with samples with an AlN interlayer. AlN interlayers have served to improve the mobility of AlGaN/GaN HEMTs by reducing alloy scattering from the AlGaN [97]. However, as can be seen by the simulated band diagrams (Figure 6-15 and Figure 6-16), the presence of the AlN increases the E_c band offset. While this is advantageous for confining the 2-DEG in normal operation, it does mean that when the structure is forward biased, there is a source of additional forward access resistance which distorts forward bias CV measurements.

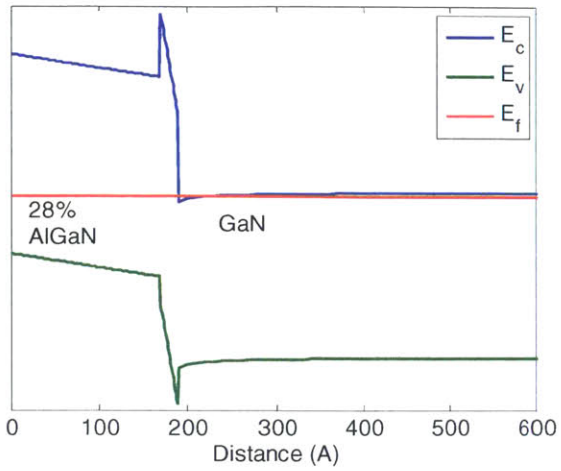


Figure 6-15: Band Diagram of AlGaN/AlN/GaN heterostructure simulated by BandEng [98].

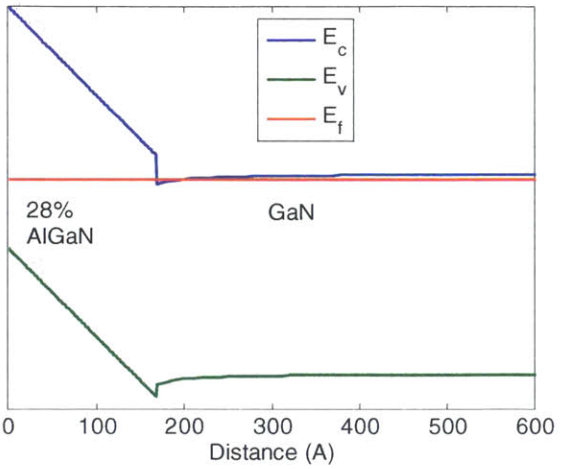


Figure 6-16: Simulated band diagram of AlGaN/GaN heterostructure. Simulated by BandEng [98]

Samples both with and without an AlN interlayer were fabricated using the gate first process and characterized by using forward bias CV measurements. Representative CV measurements for the sample with and without AlN can be seen in Figure 6-17 and Figure 6-18 respectively.

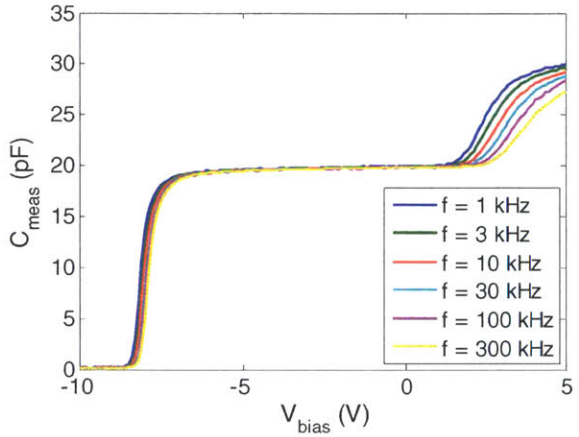


Figure 6-17: CV measurements for representative sample with AlN interlayer at 25°C.

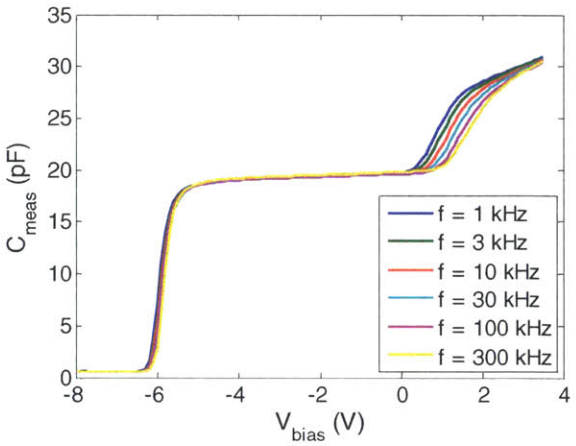


Figure 6-18: CV measurements for representative sample without AlN interlayer at 25°C.

As can be seen from the CV measurement (Figure 6-18), the measured capacitance values for the sample without AlN interlayer eventually converge upon a single value of 30.5 pF while for the sample with AlN, the CV curves do not converge. Measurements were also performed at elevated temperatures in order to decouple the impact of access resistance. Two different kinds of fittings were performed in order to extract D_{it}. First, the change in charge for a given measurement frequency was calculated as a function of temperature as shown in Figure 6-19. In addition, the change in charge as a

function of frequency at a given measurement was used to calculate D_{it} as shown in Figure 6-20. The change in charge was then plotted vs the calculated trap energy for the given measurement frequency and temperature. The D_{it} corresponded to the slope of the linear fit as shown in Figure 6-21 and Figure 6-22.

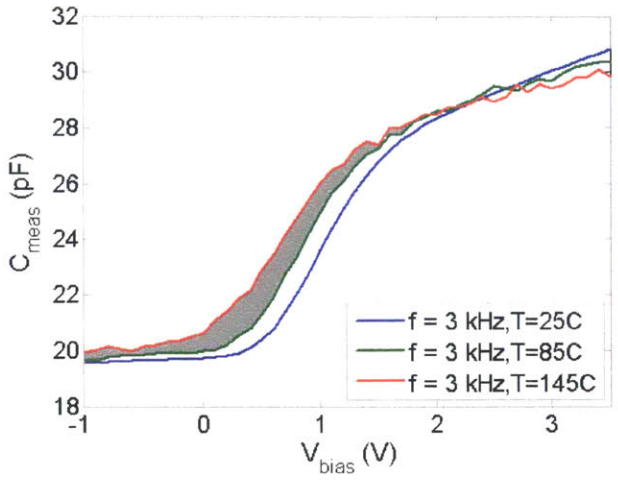


Figure 6-19: CV measurements of sample without AlN interlayer at different temperatures. The shaded region captures the additional Q_{it} probed by raising the temperature from 85°C to 145°C.

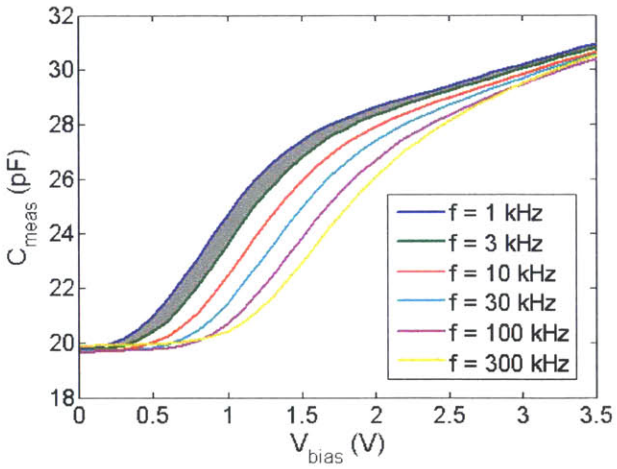


Figure 6-20: CV measurements of sample without AlN interlayer at different frequencies at 25°C. The shaded region captures the additional Q_{it} probed by changing the measurement frequency from 3 kHz to 1 kHz

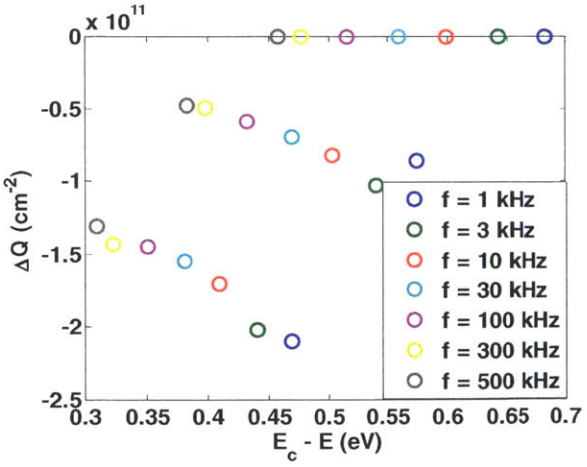


Figure 6-21: Change in integrated charge vs temperature for different measurement frequencies ranging from 1 Khz to 500 kHz. The linear fit is used to calculate D_{it}. Note that these fits are dependent σ_{th}

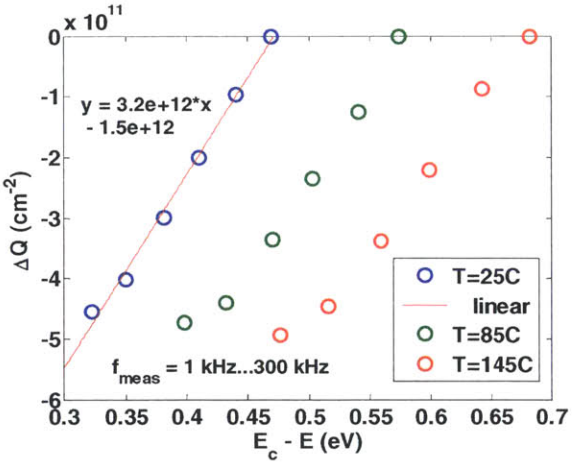


Figure 6-22: Change in integrated charge (as defined in Figure 6-20) vs frequency for different measurement temperatures. The linear fit is used to calculate D_{it}.

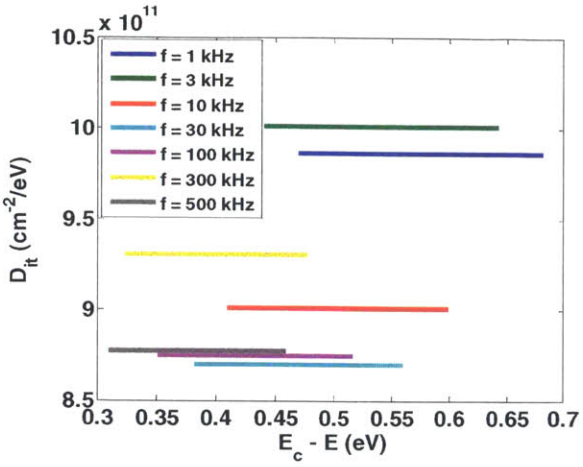


Figure 6-23: Calculated D_{it} from fits plotted in Figure 6-21.

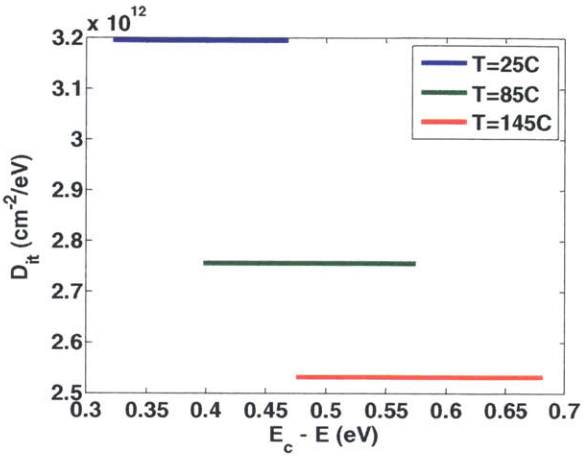


Figure 6-24: Calculated D_{it} from fits plotted in Figure 6-22.

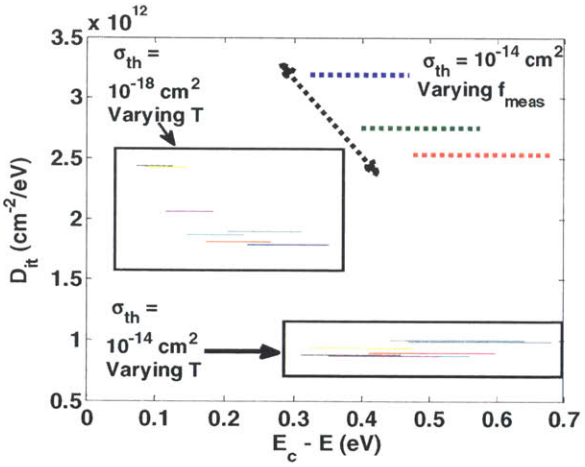


Figure 6-25: Plot of different D_{it} calculations for the capacitor analyzed in Figure 6-19 to Figure 6-24. D_{it} calculations that rely on varying the temperature are dependent on the assumed value for σ_{th}.

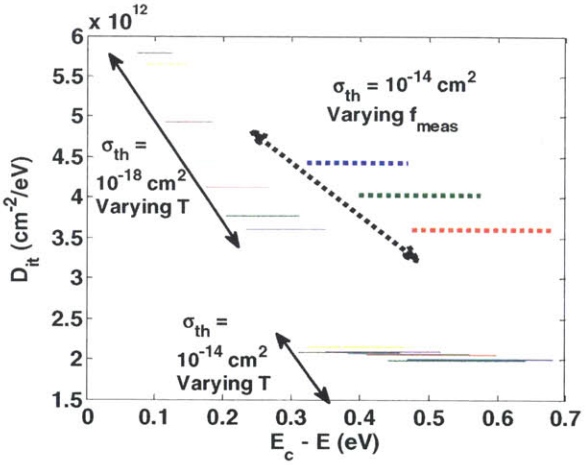


Figure 6-26: Another capacitor that does not have an AlN interlayer. Unlike the capacitor in Figure 6-25, the D_{it} values calculated from varying the temperature and assuming that σ_{th} is 10^{-18} cm^2 are larger than the D_{it} values extracted from variable frequency measurements.

If D_{it} is calculated by varying the measurement frequency and looking at the change in forward charge, it is not necessary to know the trap cross section or any other constants found in Equation (1) since those terms drop out as noted by Hori et al. [99]. On the other hand, it is necessary to know the value of σ_{th} if D_{it} is calculated by varying the measurement temperature. As shown in Figure 6-25, the value of extracted D_{it} from varying the temperature can change from 1×10^{12} to 2.5×10^{12} cm^{-2} depending on what σ_{th} value is used. Ideally, if the series resistance were negligible, the value for σ_{th} could be

found by matching the extracted D_{it} values from variable temperature measurements and variable frequency measurements. However, the differences between 2 capacitors from the sample suggest that making that correlation is not feasible. For example, by looking at Figure 6-25, one can conclude that σ_{th} is smaller than 10^{-18} cm^2 but by looking at Figure 6-26, one would conclude that σ_{th} is between 10^{-14} and 10^{-18} cm^2.

For the capacitors with an AlN interlayer, the frequency dispersion is more apparent and unlike the capacitors without AlN, the maximum capacitance value does not converge to a single value as seen in Figure 6-17. Therefore, using frequency dispersion to characterize D_{it} will lead to an overestimate in D_{it} given that some of the dispersion is due to series resistance as shown in the differences between Figure 6-27 and Figure 6-28.

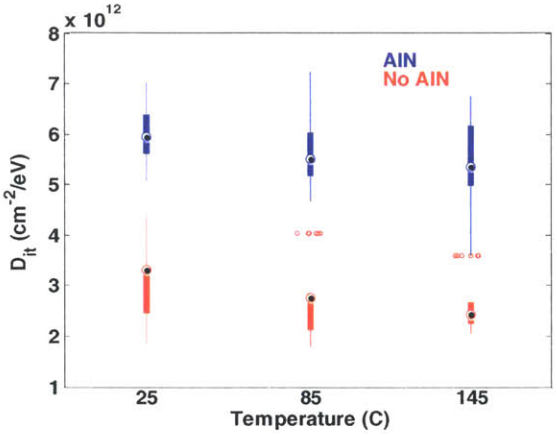


Figure 6-27: Calculated Dit from frequency dispersion for sample with and without AlN. 6-8 capacitors were measured per sample. Fit from 1 KHz to 100 kHz

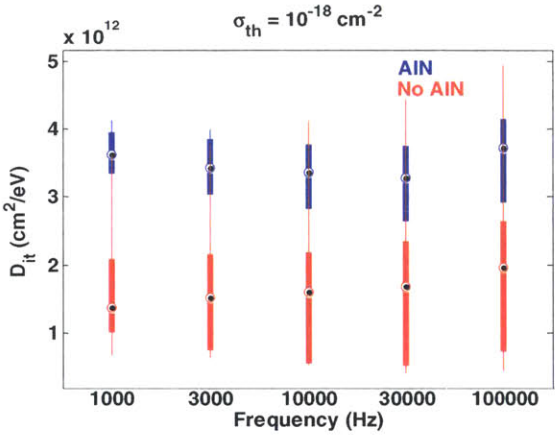


Figure 6-28: Calculated Dit from Temperature dispersion for $\sigma_{th} = 10^{-18}$ cm^2. Fit from 25°C to 145°C

Impact of Annealing Conditions on Electrical Characteristics

In order to study the impact of the ohmic anneal ambient, a set of gate first samples were fabricated where one sample had an ohmic anneal performed in a forming gas ambient while the other sample had an ohmic anneal performed in a nitrogen ambient. Hydrogen was first found to passivate traps in SiO_2/Si gate stacks in the 1960s [100]. Forming gas anneals have been reported to passivate

border traps for Al_2O_3/InGaAs stacks [101] and reduce hysteresis in Al_2O_3/Si gate stacks [102]. Anneals in general have been reported to improve the quality of Al_2O_3/AlGaN/GaN stacks [38].

Both samples used in this study were fabricated by using the standard gate first process flow. 240 cycles of Al_2O_3, for a target thickness of 20 nm, were deposited by using the Oxford Flex-AL ALD system and the initialization dose was calibrated to ensure a good interface. Below are representative CV measurements for both gate stacks. It should be noted that a Mo gate was used for both samples. Many reports that show improvement due to forming gas anneals use a Pt gate [101] since Pt helps crack hydrogen. However, Pt can only be patterned by using liftoff due to the relative difficulties of etching Pt without attacking the underlying Al_2O_3 [64]. Given that performing liftoff causes Al_2O_3 to get etched (Figure 4-4) and can contaminate the oxide surface as well (Figure 4-7), patterning Pt by liftoff is not seen as desirable.

CV Measurements show that the difference in forward charge (Figure 6-29) and channel charge (Figure 6-30) between the two samples is negligible.

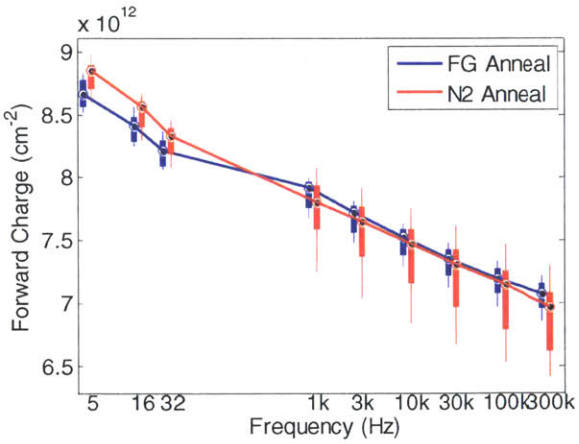


Figure 6-29: Forward charge for capacitors with both annealing conditions.

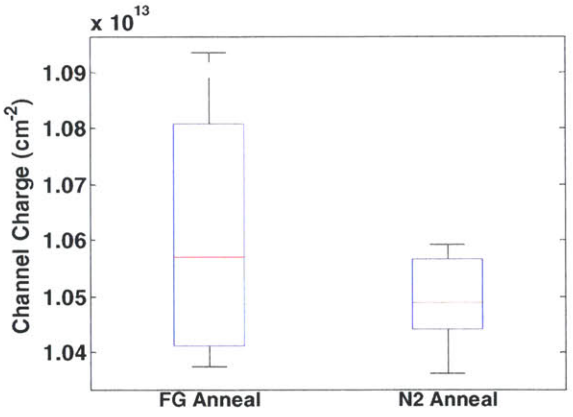


Figure 6-30: Channel charge for both annealing conditions. Note that the difference in channel charge is trivial

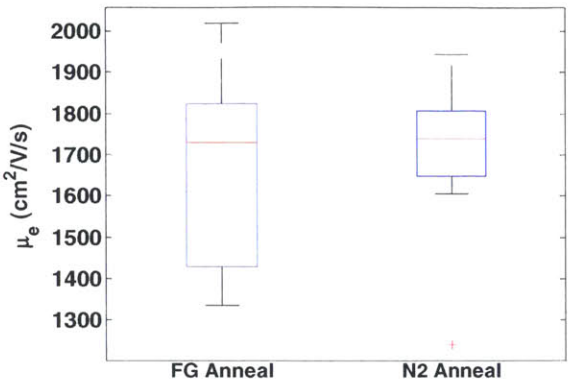


Figure 6-31: Extracted electron mobility from CV-IV measurements with V_D = 200 mV. Note that the median values for both samples are the same despite

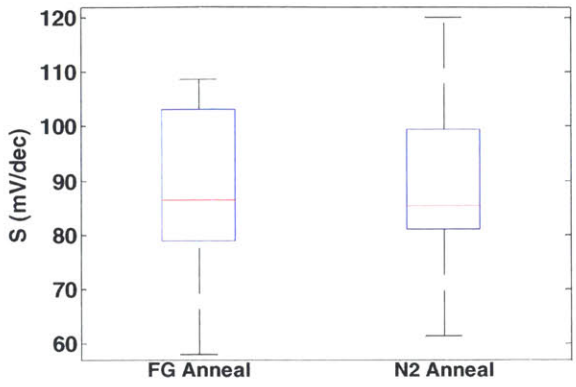


Figure 6-32: Extracted subthreshold slopes from CV-IV measurements with V_D = 200 mV

Likewise, the extracted electron mobility (Figure 6-31) and the extracted subthreshold slope (Figure 6-32) of both samples are very similar.

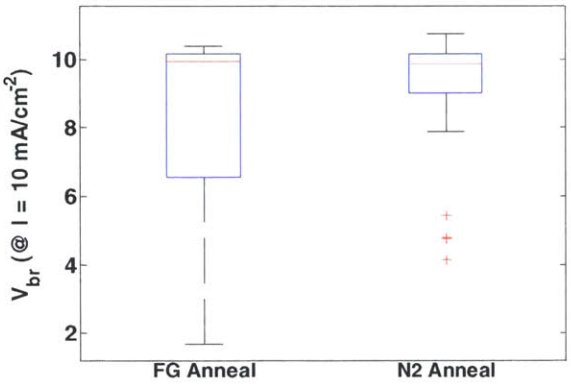


Figure 6-33: Forward breakdown measurements for both samples show little difference in the median value.

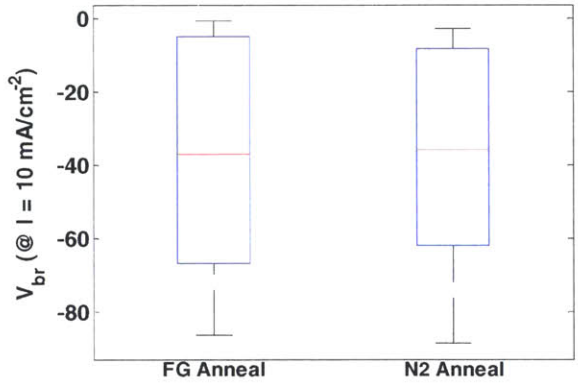


Figure 6-34: Reverse breakdown measurements for both samples show little difference in the median value.

Given that the forward bias dispersion (Figure 6-29), subthreshold slope (Figure 6-32) and breakdown voltages (Figure 6-33 and Figure 6-34) are similar for both samples, it is assumed that the annealing ambient does not impact devices with a Mo/Al_2O_3 gate stack.

Impact of Oxidation on Breakdown Voltage

GaN and AlGaN can be oxidized in oxygen containing ambients at temperatures as low as 300°C as per reported results in the literature. Pearton et al. studied the outdiffusion of oxygen atoms from a SiO_2 layer deposited on top [103] after annealing it at temperatures ranging from 550°C to 900°C. By using O^{17} containing SiO_2, they found that annealing at 550°C caused some oxygen diffusion while annealing at 900°C caused O^{17} to diffuse up to 180 nm below the surface. Oxidized AlGaN/GaN has been reported to be insulating by multiple groups. Masato et al. annealed both GaN and AlGaN at 900°C under dry oxidation conditions and used the oxidized region to isolate devices [104]. Roccaforte et al. found that the isolation takes place even if only part of the AlGaN barrier was oxidized [105],[106]. Another similar study by Grecoet et al. found that GaN was oxidized around defects in the AlGaN barrier [107]. This is consistent with the observation in the study by Pearton et al. [103]. Eickelkamp et al. also observed that oxidizing InAlN/GaN by annealing in an O_2 environment at temperatures ranging from 700°C to 800°C caused a reduction in carrier concentration [108].

In order to study the impact of oxidation and oxidizing conditions on AlGaN/GaN HEMTs, a study was performed where the gate first samples were exposed to varying amounts of ozone before depositing Al_2O_3 by ALD. The samples were exposed in-situ in the Cambridge Nanotech ALD system at 300°C for either 10 min, 3 min or for no time to ozone before depositing 20 nm of Al_2O_3. Ozone has been reported to be far more effective at oxidizing GaN than water pulses during an ALD process [94].

Breakdown measurements were performed on capacitors where the bias was swept either forward or in the reverse direction to the point where the leakage current exceeded 10 mA/cm^2. Particularly for reverse bias measurements, this would involve a catastrophic breakdown for many devices while for forward bias measurements, it was almost always a gradual increase in current. Also, the forward bias breakdown measurements always yield a lower voltage value given that when a forward bias is applied, all the field drops across the oxide. However, when a reverse bias is applied, the

field drops across the oxide, AlGaN layer and even across some of the access region depending on the trapping conditions. Therefore, the forward bias measurements can be used to assess the integrity of the oxide while the reverse bias measurements can give an idea of the breakdown strength of the AlGaN in addition to the strength of the oxide. Representative reverse and forward bias breakdown measurements are shown in Figure 6-35 and Figure 6-36.

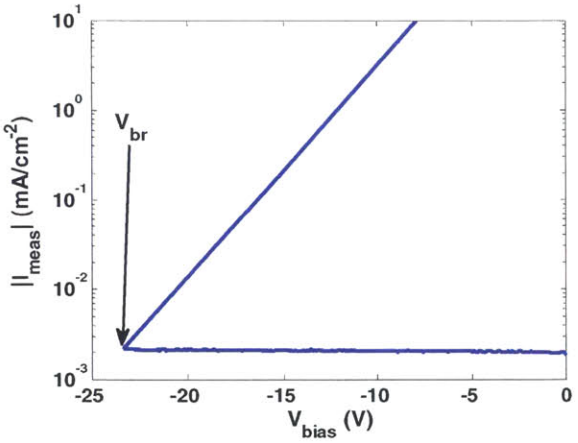


Figure 6-35: Example of a reverse breakdown measurement. The breakdown voltage in this case is -23V. Notice that the onset of breakdown is quite sudden.

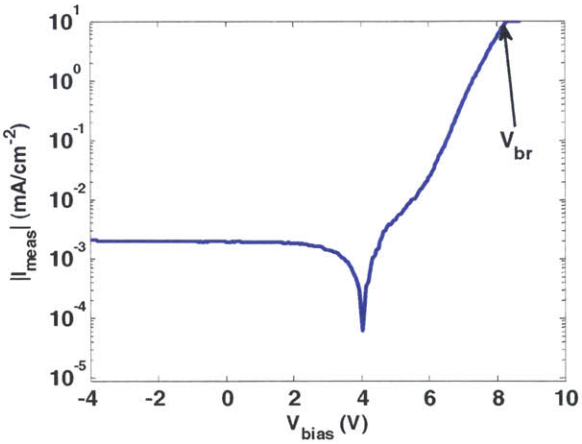


Figure 6-36: Example of forward breakdown measurement. The breakdown voltage is 8.2V in this measurement. The breakdown in quite gradual in comparison to the reverse bias breakdown measurements.

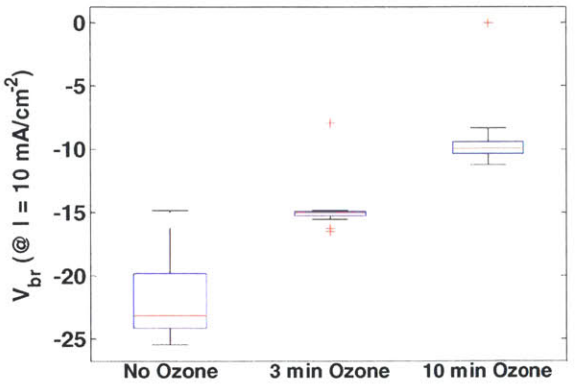


Figure 6-37: Boxplot showing reverse breakdown voltage for samples exposed to ozone for varying times. 15-20 devices were measured per sample in order to gain meaningful statistics.

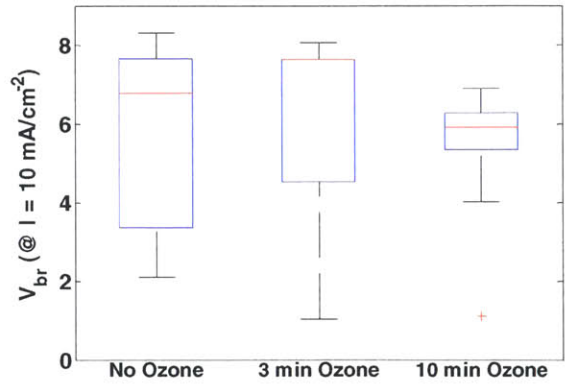


Figure 6-38: Boxplot showing forward breakdown voltage for samples exposed to ozone for varying times. Unlike the reverse breakdown measurements, there is no clear dependence on the ozone time and forward breakdown voltage.

All three samples showed similar forward bias dispersion behavior (Figure 6-39) and forward breakdown voltages (Figure 6-38) which indicates both that the interfaces were similar and that the quality of the Al_2O_3 was similar. However, the carrier concentration dropped dramatically for the sample that had been subjected to ozone pretreatment for 10 min as seen in Figure 6-40. This drop in charge is consistent with previous reports of oxidized barriers resulting in lower carrier concentration [108]. Oxidation of AlGaN by using ozone seems to cause reliability challenges without much corresponding gain in terms of interface quality.

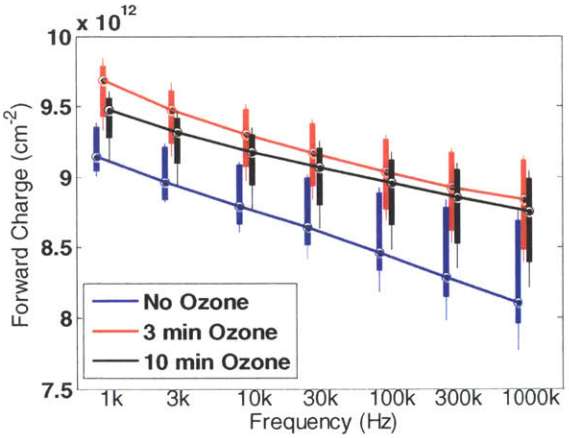


Figure 6-39: Forward Charge for different ozone conditions

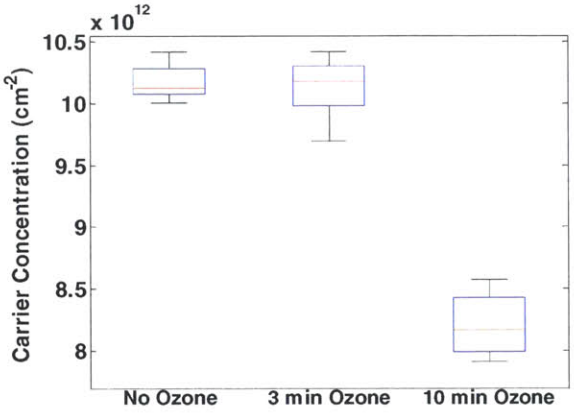


Figure 6-40: Carrier concentration for different ozone pretreatment conditions. Note the drop in carrier concentration for the sample that is exposed to ozone for 10 min

Oxidized polysilicon gate stacks

Before scaling required the replacement of SiO_2 with high-k materials like HfO_2, gate stacks on silicon were fabricated by oxidizing silicon at high temperature in order to yield a high quality SiO_2 gate stack. SiO_2 based gate stacks have been demonstrated in GaN previously where the SiO_2 was deposited

by PECVD [11], e-beam evaporation [109], and atomic layer deposition [110]. SiO_2 is of interest given that it has a large band gap. However, before high-k dielectrics were used, the SiO_2/Si gate stacks relied on thermally oxidized Si to form the high quality gate stack [28], [29] as opposed to these alternative methods of depositing SiO_2. Therefore, one method to achieve a thermal oxide would be to deposit polysilicon and oxidize it.

Two different kinds of samples were fabricated. After performing a piranha clean and an HCl:DI (1:3) dip, 8 nm amorphous silicon using low pressure chemical vapor deposition (LPCVD). One sample had 5 nm of SiN deposited by LPCVD before the Si deposition while the other sample had polysilicon deposited directly on top. The deposition took place at a target temperature of 517°C, a target SiH_4 gas flow of 110 sccm and a target pressure of 200 mTorr. After the polysilicon deposition, the samples were oxidized for a 100 min at 700°C in wet conditions. Wet oxidation allows for a faster oxidation rate at a given temperature than dry oxidation [29]. Following the oxidation, the two samples were processed using the standard gate first process flow. The samples were evaluated by performing high bias CV measurements, positive gate pulsed-IV measurements, and by performing breakdown measurements. In addition, the SiN + SiO_2 sample had CV measurements performed at elevated temperatures in order to further study the D_{it} of the AlGaN/SiN surface.

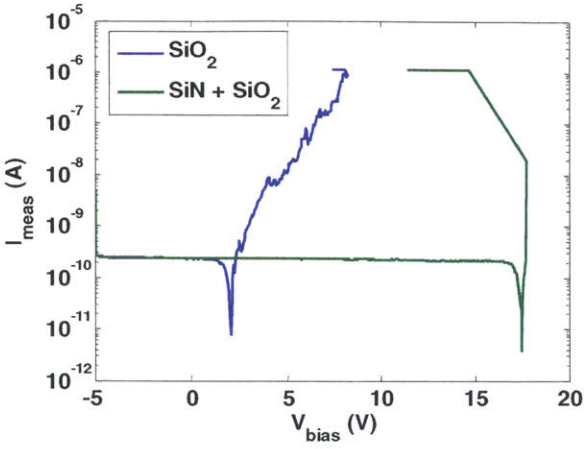


Figure 6-41: Comparison for forward bias breakdown for representative SiO_2 and SiN + SiO_2 capacitors. Note that the addition of the 5 nm SiN interlayer improves the forward breakdown voltage from 8V to 18 V.

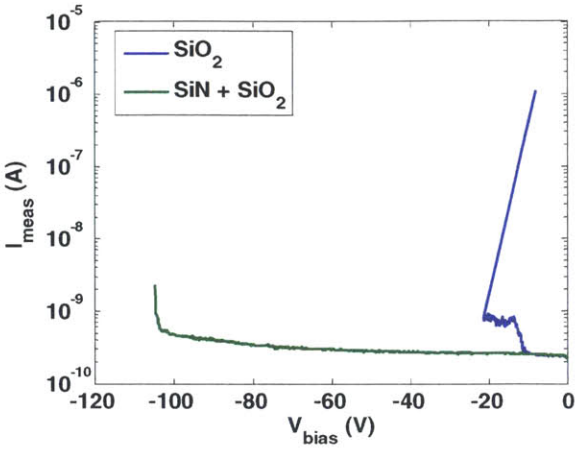


Figure 6-42: Comparison of reverse bias breakdown for SiO_2 and SiN + SiO_2 capacitors

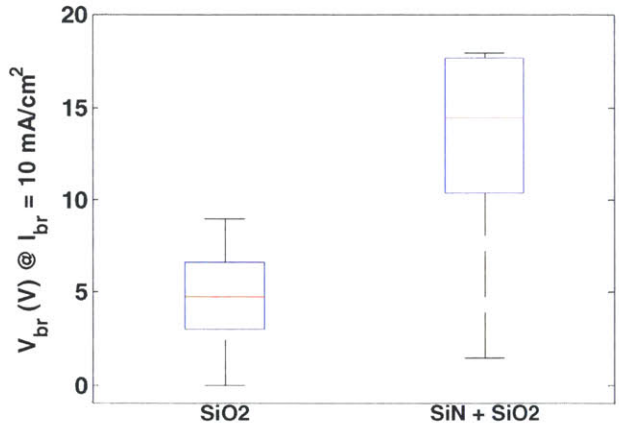


Figure 6-43: Boxplots showing distribution of forward breakdown measurements (as defined in Figure 6-41).

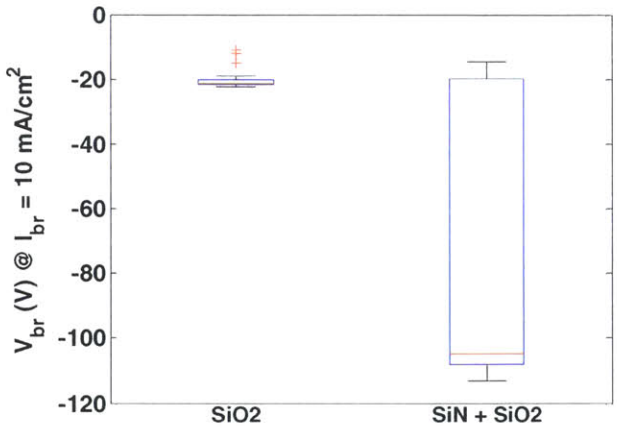


Figure 6-44: Boxplots showing distribution of reverse breakdown measurements. Note that SiN + SiO_2 capacitors display a significantly larger breakdown voltage than the SiO_2 capacitors.

Adding the 5 min thick SiN layer to the 18 nm SiO_2 gate stack improved the forward breakdown voltage from a median value of 5V to 14.5V. Improvement in leakage current due to Si_3N_4 interlayers has also been reported for Al_2O_3/SiN/AlGaN/GaN stacks [22]. SiN is a very effective barrier for blocking oxygen and water and therefore, when doing wet oxidation, it can serve to protect GaN from the wet

oxidation ambient. Readinger et al. reported that wet oxidizing GaN results in a Ga_2O_3 layer that exhibited a breakdown field as low as 5×10^4 V/cm [111].

Representative CV plots for both the SiN+ SiO_2 and SiO_2 stacks are plotted in Figure 6-45 and Figure 6-46. The capacitance of the SiO_2 stack is greater than the capacitance of the SiN + SiO_2 stack because of the additional SiN layer.

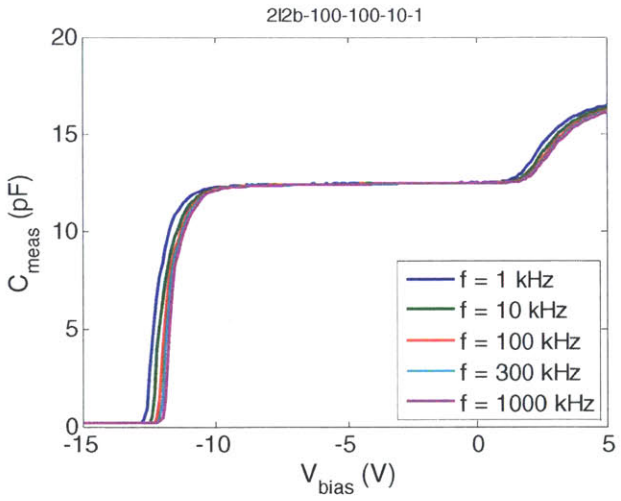


Figure 6-45: Representative CV plot for SiO_2 capacitor

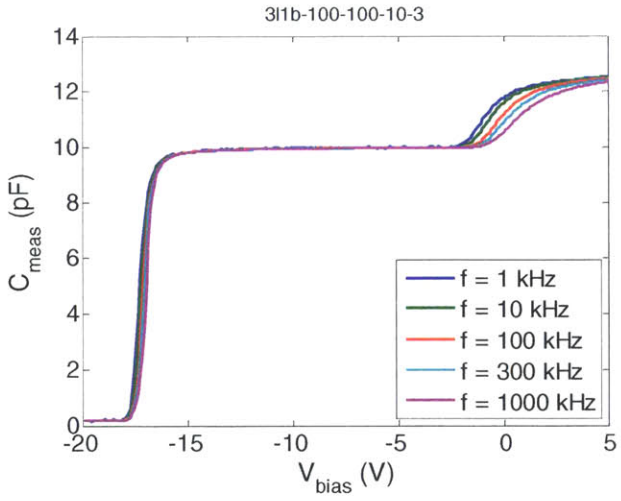


Figure 6-46: Representative CV plot for SiN + SiO_2 capacitor

The D_{it} of the SiO_2 capacitor and the SiN + SiO_2 capacitor was first calculated by looking at the change in forward charge as a function of frequency and then converting it to a change in trap energy. Figure 6-47 shows an extracted D_{it} calculation for the SiO_2 capacitor at 25°C while Figure 6-48 and Figure 6-50 show the calculated D_{it} calculation for the SiN + SiO_2 capacitor. In addition, since the SiN + SiO_2 capacitor was measured at elevated temperatures, D_{it} was also calculated by fitting the change in charge as a function of temperature for different measurement frequencies as shown in Figure 6-49 and Figure 6-51. The extracted D_{it} value for the SiN + SiO_2 capacitors are between 1×10^{12} to 2×10^{12} cm^{-2}/eV depending on how it is extracted while the D_{it} value for the SiO_2 capacitor is 1×10^{12} cm^{-2}/eV. As with the

capacitors without AlN, varying the measurement temperatures led to a lower extracted D_{it} value than the calculated D_{it} values from fits where the measurement frequency was varied.

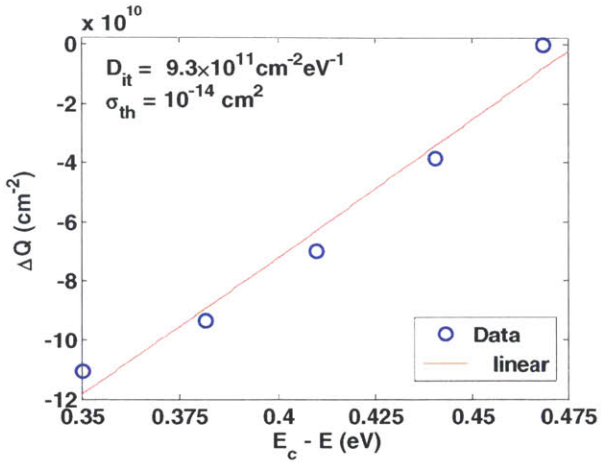


Figure 6-47: D_{it} extraction for representative SiO_2 capacitor. D_{it} values for capacitors were between 8.5×10^{11} to 1×10^{12} cm^{-2}/eV

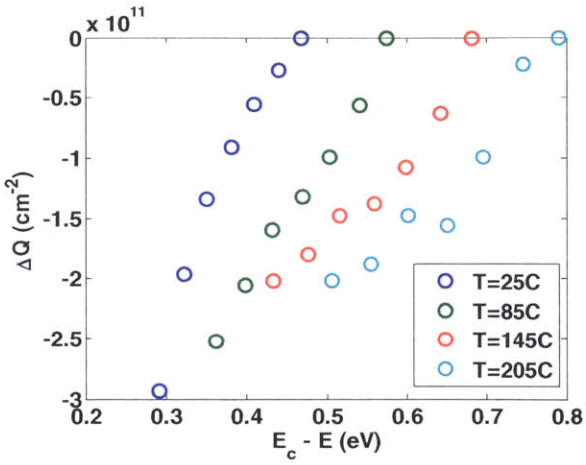


Figure 6-48: D_{it} extraction for representative SiN + SiO_2 capacitor. The CV measurements were performed at temperatures ranging from 25°C to 205°C and the D_{it} extraction is done by fitting the change in Q vs measurement frequency. As discussed earlier, extracting D_{it} from looking at Q_{it} vs f means that this value is independent of the value of σ_{th}

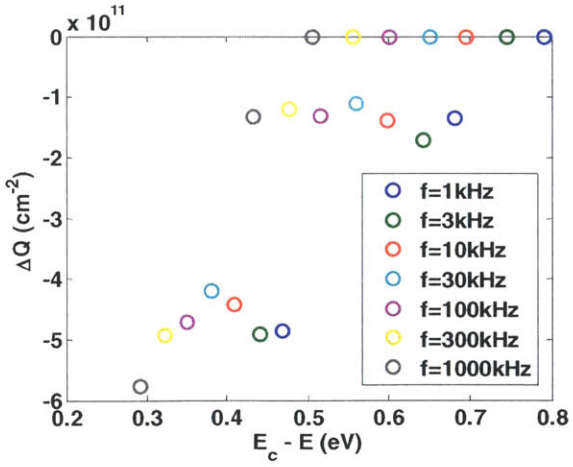


Figure 6-49: D_{it} extraction for same capacitor in Figure 6-48. D_{it} extraction is done by fitting the change in Q_{it} vs temperature for all measurement frequencies. This technique helps decouple the impact of series resistance but is more dependent on the value of σ_{th} used for calculations

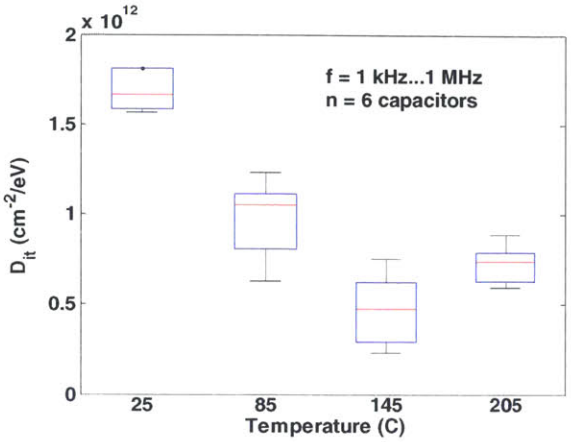


Figure 6-50: Extracted D_{it} for SiN + SiO_2 capacitors using technique described in Figure 6-48

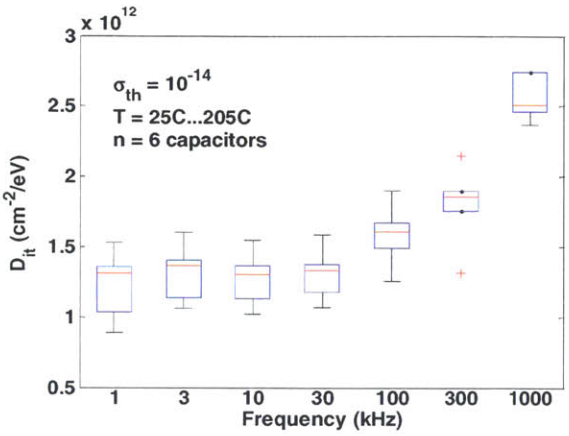


Figure 6-51: Extracted D_{it} for SiN + SiO_2 capacitors using technique described in Figure 6-49.

Transistors were also assessed by performing I_D-V_{gs} and I_D-V_{ds} measurements. Given that the reverse breakdown voltage of the SiO_2 capacitors was around -20V and that the pinchoff voltage was -12V, many SiO_2 transistors broke when performing I_D- V_{ds} measurements where the V_{ds} was swept to 10V given that at pinchoff, there was a drop of 22V across the drain-gate edge. Therefore, out of 15 devices measured, only 6 devices survived multiple I_D-V_{gs} measurements.

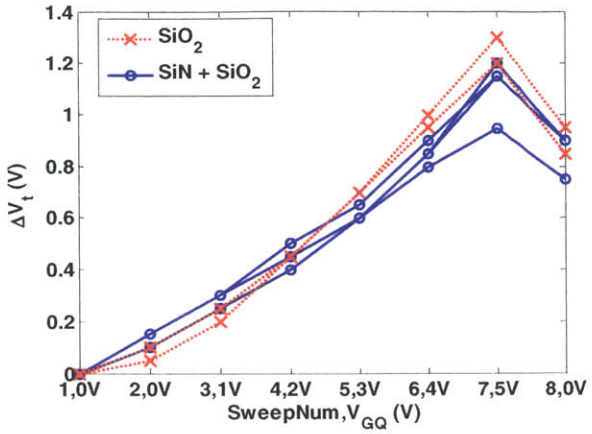


Figure 6-52: Pulsed I_D-V_{gs} measurements for both the SiO_2 transistors and SiN + SiO_2 transistors

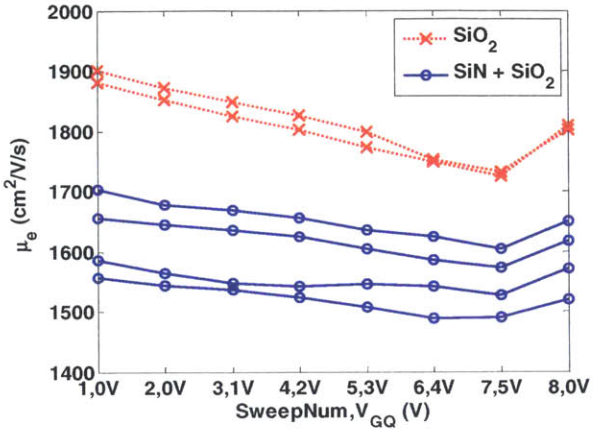


Figure 6-53: Mobility (extracted by a combination of CV-IV and Pulsed I_D-V_{gs} measurements) for both SiO_2 and SiN + SiO_2 transistors. Note that the 700°C oxidation did not cause mobility degradation.

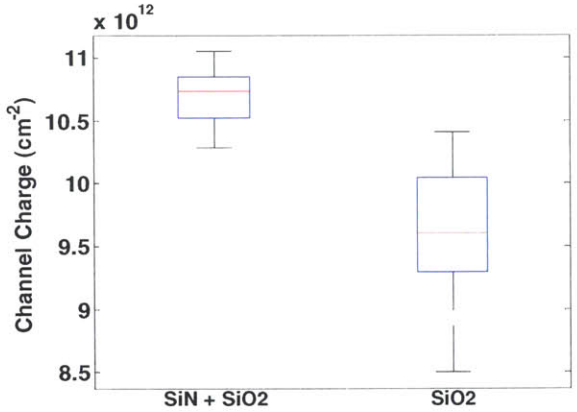


Figure 6-54: Channel Charge differences between SiO_2 and SiN + SiO_2

From CV-IV measurements, the charge in the channel was calculated by integrating the CV curves from threshold voltage to 0V. On average, the devices with SiN had 1×10^{12} cm^{-2} more charges than the devices without SiN as seen in Figure 6-54. The 10% increase in channel charge due to the SiN interlayer can be attributed to two different factors. First, silicon nitride has been reported to have positive charges in the film [96]. Second, it is likely that the AlGaN barrier was oxidized during the oxidation process and thus contributed to a reduction in channel charge.

To summarize, the gate first process allowed for studying the impact of different processing conditions while ensuring that the results were not skewed by organic contamination at the interface. First, the importance of properly nucleating the surface when depositing films by ALD in order to ensure a good interface has been demonstrated by showing how insufficient nucleation can cause roughness and trapping. Second, the impact of AlN on the forward bias CV measurements was identified. Finally, the role of oxidation in causing premature breakdown of the AlGaN barrier was highlighted by experiments with oxidizing the sample with ozone and by the contrast in breakdown behavior between gate stacks with SiO_2 vs gate stacks with SiN + SiO_2.

Chapter 7 Conclusions and Future Work

Summary of Contributions

This thesis has made the following contributions to the understanding of GaN based MIS-HEMTs

- When characterizing the charges present in oxide films, semiconductor grade glassware and strict cleaning protocols should be used in order to prevent mobile ion contamination. Otherwise, mobile ion contamination will distort the number of carriers in the channel and cause threshold voltage instability.
- Samples processed using a CMOS style gate first process was compared to a traditional Au-based, liftoff processing based ohmic first process for the first time. Gate first processing yielded a better interface than devices processed using an ohmic first process. By looking at samples that had been pre-annealed together with ohmic first samples that had protective oxide layers to enable piranha cleaning, organic contamination was identified as a key culprit. By designing a process flow that allows for aggressive piranha cleaning before depositing gate dielectrics, it is possible to get a good interface even with samples with standard Au based ohmic contacts.
- Transient current measurements showed that transistors with a good interface have a recovery process that is seemingly limited by tunneling. This is based on the fact that the recovery is temperature independent and dependent on the recovery bias. This technique was used to successfully discriminate between a good interface and a bad interface by looking at the temperature dependence on the recovery.
- Positive Gate Pulsed-IV measurements indicated that there is mobility degradation in addition to charge depletion when the gate is pulsed with a positive bias. This mobility degradation might be due to Coulomb scattering from electrons piling up at the AlN/AlGaN interface close to the 2-DEG.

- The initial nucleation layers play a large role in determining the interface quality. Insufficiently dosed nucleation layers cause surface roughness, which in turn cause more trapping sites. Using the gate first process with its intrinsic cleanliness helped identified this trend.
- SiO_2 gate stacks with oxidized polysilicon gates were developed. The role of a silicon nitride interlayer in improving the breakdown voltage from 5V to 15 V on average coupled with experiments showing the role of ozone on causing premature breakdown point to unintentional oxidation as a reliability concern.

Future Work

The work presented in this thesis can be expanded further by exploring the following areas:

- The impact of the substrate and dislocations on the oxide/AlGaN interface
- Exploring other dielectric materials and combinations
- Applying processing knowledge and characterization techniques to enhancement mode GaN

All the work in this thesis involved the use of AlGaN/GaN HEMTs grown on sapphire. Typically, these epitaxial structures have a dislocation density on the order of 10^8 cm^{-2}. As discussed earlier, oxygen diffuses through dislocations and defects in the epitaxy [103],[107]. Bulk GaN grown by the ammonothermal method has been reported to have dislocations on the order of 10^3 cm^{-2} [112] while bulk GaN grown by HVPE has dislocations on the other of 10^5-10^6 AlGaN/GaN Schottky diodes grown on ammonothermal GaN has been demonstrated to exhibit lower leakage current than AlGan/GaN diodes grown on sapphire substrates [113].

It would be of interest to fabricate AlGaN/GaN MIS-HEMTs grown on an bulk ammonothermal GaN substrate and on HVPE grown GaN using the optimal processing parameters identified in this thesis. One key experiment would be to see if these substrates are as prone to oxidation as AlGaN/GaN on sapphire substrates and to see if there is a correlation between dislocation density and oxidation.

Another related experiment would be to see if subjecting low dislocation density substrate to oxidizing ambient conditions (either ozone in an ALD reactor or oxygen in a wet ambient) would cause premature reverse breakdown as has been observed for AlGaN/GaN on sapphire substrates. Again, correlating the reverse breakdown voltage to dislocation density would help with understanding the role of oxidation in causing premature breakdown. If substrates with low dislocations don't oxidize as readily, it would allow for using ozone to help facilitate more uniform nucleation on a substrate.

The oxidized polysilicon gate stack experiments helped highlight the role that silicon nitride can play in preventing oxidation. However, as evidenced by the higher D_{it} figures, the silicon nitride deposition can be optimized. At the same time, it would be of interest to integrate silicon nitride with Al_2O_3. The Oxford FlexAl ALD tool can be used to deposit Silicon Nitride using BTBAS and NH_3 plasma and therefore, if the BTBAS precursor were purchased and if the silicon nitride process were developed, it would be possible to fabricate a gate stack composed on ALD deposited Si_3N_4/ Al_2O_3.

All the devices studied in this thesis are depletion mode devices. It would help further validate forward bias CV measurements and the transient current measurements by performing these measurements on different kinds of enhancement mode devices. Enhancement mode operation can be achieved by recessing the gate, using fluorine treatment or by using a p-GaN gates. Since all methods of achieving enhancement mode operation introduce different kinds of defects, it would be of value to see the differences in forward bias CV measurements and transient current measurements.

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