Ultrathin Crystalline Silicon Solar Cells Incorporating Advanced Light-Trapping Structures

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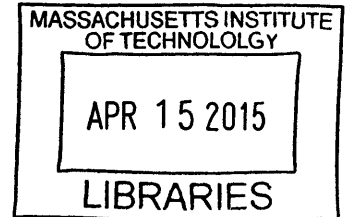

By

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Submitted to the Department of Mechanical Engineering in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY IN MECHANICAL ENGINEERING
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ABSTRACT

Solar photovoltaics, which convert the energy potential of photons from the sun directly into electrical power, hold immense promise as a cornerstone of a clean energy future. Yet their cost remains greater than that of conventional energy sources in most markets and a barrier to large-scale adoption. Crystalline silicon modules, with a 90% share of the worldwide photovoltaic market, have witnessed a precipitous drop in price over the last decade. But going forward, further evolutionary cost reduction will be difficult given the significant cost of the silicon wafer alone – roughly 35% of the module. Dramatically reducing the thickness of silicon used to make a solar cell from the current 350 μm could rewrite the economics of photovoltaics.

For thin-film crystalline silicon solar cells to deliver the anticipated cost benefits of reduced material requirements, it is essential that they also yield power conversion efficiencies comparable to commercial solar cells. A significant hurdle to realizing elevated efficiency in crystalline silicon films thinner than 20 μm is the loss of current resulting from reduced photon absorption. A range of light management structures have been proposed in the literature to address this issue and many have been demonstrated to provide high absorption across the spectral range relevant to crystalline silicon, but their promise has yet to be realized in an active photovoltaic device.

The focus of this thesis is the development of an experimental platform and fabrication process to evaluate the effectiveness of theoretically-designed light-trapping structures in functional photovoltaic devices. The experimental effort yielded 10-μm-thick crystalline silicon solar cells with a peak short-circuit current of 34.5 mA cm^{-2} and power conversion efficiency of 15.7%. The record performance for a crystalline silicon photovoltaic of such thinness is enabled by an advanced light-trapping design incorporating a 2D photonic crystal and a rear dielectric/reflector stack.

A parallel line of questioning addressed in this thesis is whether periodic wavelength-scale optical structures are superior to periodic or random structures with geometric-optics-scale features. Through the synthesis of experimental and theoretical evidence, the case is constructed that wavelength-scale light-trapping structures are in fact comparable to conventional random pyramid surface structures for broad-spectrum absorption in silicon solar cells as thin as 5 μm.

These results have important implications for the design of cost-effective and manufacturable light-trapping structures for ultrathin crystalline silicon solar cells.

Thesis Supervisor: Gang Chen
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Although it might seem that doctoral research is an individualistic pursuit, the reality is far different. This thesis would not have been completed without the immense encouragement, camaraderie, and instruction of my friends and colleagues at MIT. It is my firm belief that the most valuable aspect of pursuing this degree has been the fantastic people whom I have had the privilege to learn from and work alongside.

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I want to express my infinite appreciation to my parents for being a firm foundation and granting me the opportunities in life that have made it possible for me to pursue my academic and personal dreams, and to my whole family – Dad, Mom, Lucas, Jordan, and Ben – for the unfaltering support they have always provided me, the past five years being no exception.

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Chapter 1: Introduction

1.1 Big Numbers and Big Problems: Energy in the 21st Century

In the next 24 hours, the world as a whole will consume 90 million barrels of oil[1], enough to cover all of Manhattan in a layer 6 inches deep. It will combust 21.4 million metric tons of coal – equivalent to 40 times the volume of Fenway stadium – and it will burn 9.5 billion cubic meters of natural gas, or enough to fill the volume of the 14,179-foot Mount Shasta volcano once a month[2]. All together, today the world will utilize 62,000,000,000 kWh (62 TWh) of electrical power and another 77,000,000,000 kWh (77 TWh) of fuels for locomotion. These astoundingly large numbers belie the fundamental connection between modern life and energy.

Abundant and inexpensive access to energy sources has motivated a spectacular improvement in well-being for the vast majority of the world's population over the past three hundred years. Indeed, there is a strong correlation between increasing energy usage and improving standards of living[3,4] (Fig. 1). Yet the explosive growth in the worldwide use of carbonaceous fuels combined with their negative environmental impacts has, paradoxically, brought the planet to a threshold where their additional large-scale exploitation could begin to roll back those advances in quality of life. Extreme levels of localized pollution from fossil fuel combustion impacts populations worldwide; air pollution in the north of China, for example, cuts life expectancy by over five years[5]. On a global basis, mercury levels in the ocean have risen by a factor of 3 since the start of the industrial revolution – largely mobilized through coal combustion – imperiling a major global food source[6]. Atmospheric carbon dioxide, meanwhile, continues its exponential rise, putting the globe in the early stages of a warming process the outcome of which is uncertain, but that could result in profound population dislocations and disruption to agriculture and ecosystems (Fig. 2).

With global primary energy consumption expected to continue its swift pace of growth, from 560 quadrillion BTU in 2014 to 820 quadrillion BTU by 2040[7], we are beset by two existential challenges: 1) How to provide sufficient energy to meet the needs and demands of a planet with a population growing in size and affluence and 2) how to harness that energy in such a manner that the planet is not destroyed in the process. Addressing these generational issues will require a combination of energy efficiency and new technologies leveraging pollution-free energy sources. The ubiquity and abundance of the solar resource – at 36000 TW, 2000 times greater than the rate of total primary energy use – necessitates that solar energy be an integral part of the global energy mix.

The focus of this thesis is technology aimed at unlocking the potential of solar energy - ultrathin crystalline silicon photovoltaics (PV). Although solar energy installations generate vastly more power – and cost substantially loss – than even a decade ago, they are still more expensive than conventional alternatives in most markets. Silicon photovoltaics, which constitute the primary solar energy conversion technology, are expensive in part because of the relatively large amount of costly silicon used in each cell. Reducing the thickness of silicon used per solar cell is one potential pathway to reduce cost, but doing so leads to new challenges resulting from poor absorption of light in thin silicon films. The objective of this work is to develop a platform and a process for integrating advanced optical designs into thin solar cell devices to 1) validate their effectiveness at raising efficiency and 2) produce commercially competitive solar cells using 30-40 times less silicon than conventional devices. Coupled with

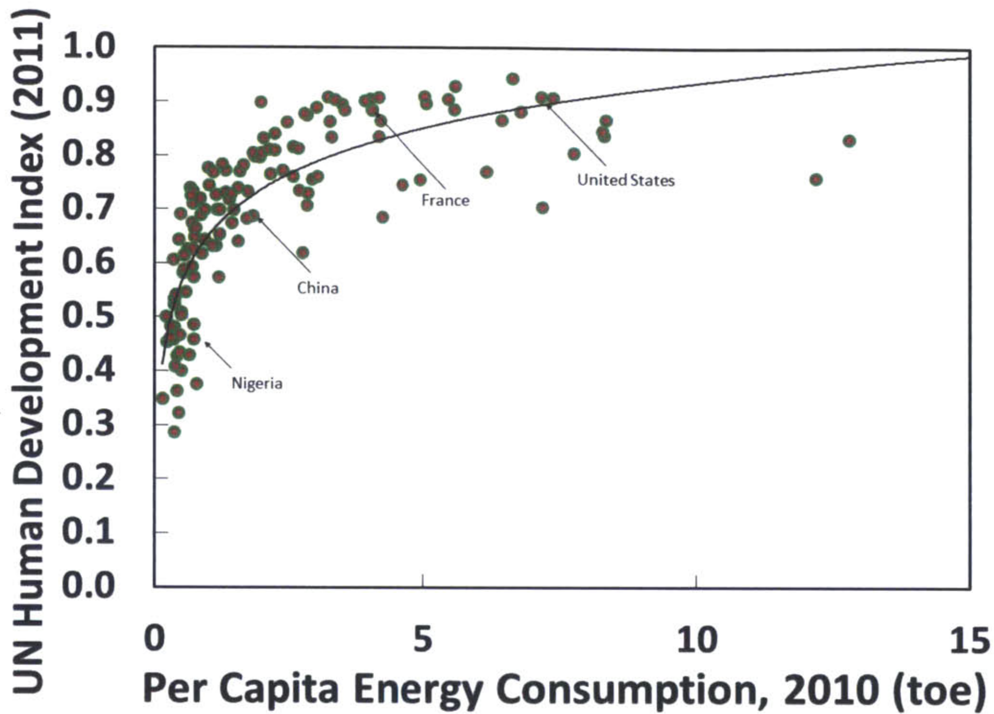


Figure 1 | National development index score compared to per capita energy consumption. TOE = tons of oil equivalent. (Refs. 3,4)

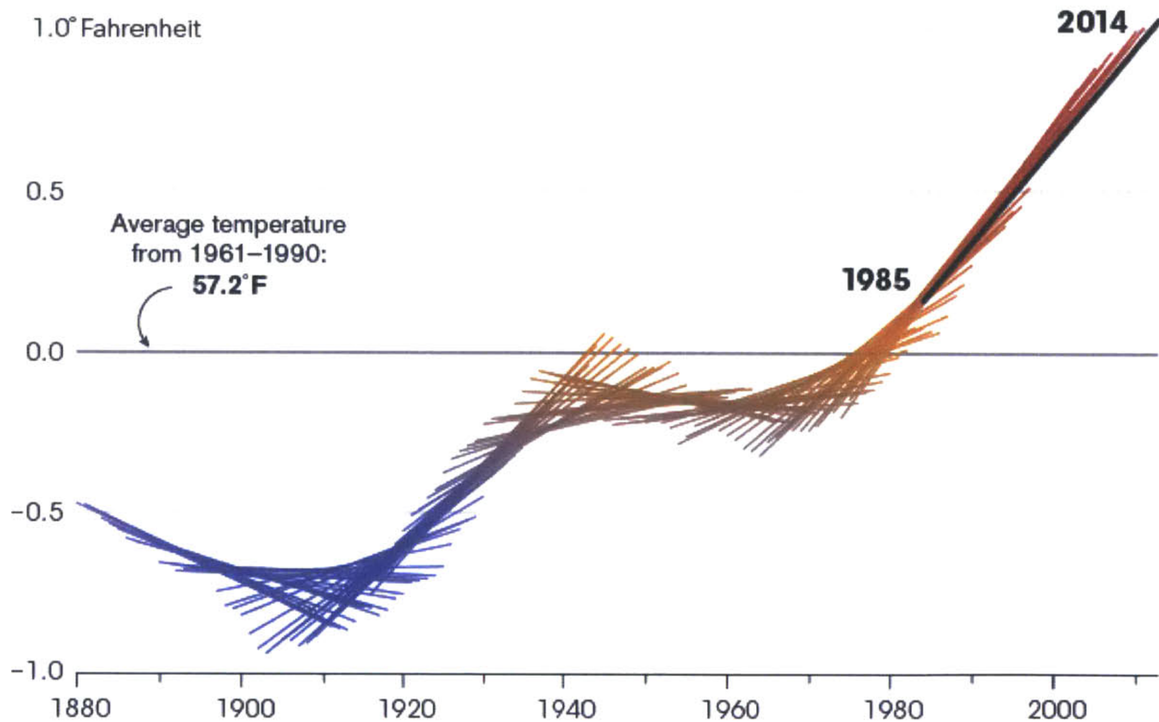


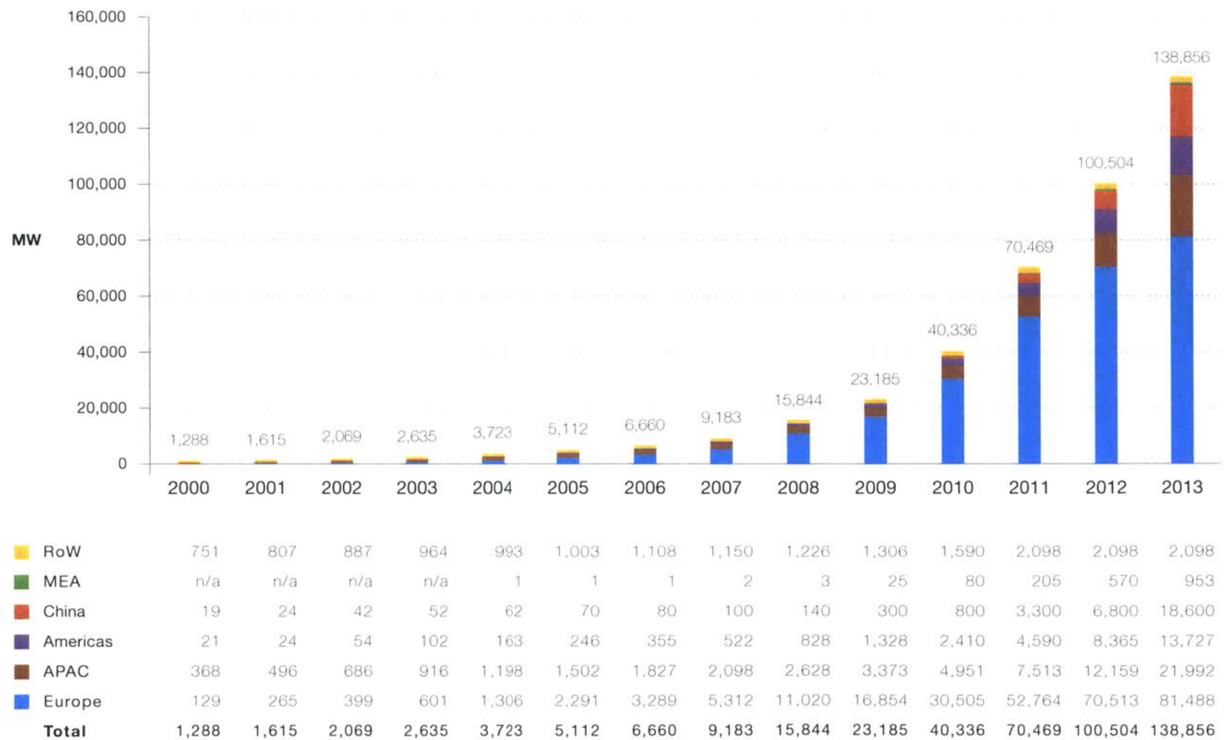
Figure 2 | Change in global average air temperature over 30-year periods. [E. Roston, *Bloomberg* (Ref. 8)]

complementary advances in the handling and manufacture of thin silicon films, the results point to the viability of ultrathin crystalline silicon photovoltaics as a promising approach to making solar energy universally affordable.

One more fact about the next 24 hours: today, the world's solar photovoltaic manufacturers will produce enough solar panels to cover 0.85 km^2 of land area, generating 136 MW of electricity with the sun shining – enough to power 45,000 average American homes. If the global PV industry increased production to 150 square kilometers of solar panels per day, or 175 times more than at present, it would require but 10 years to produce enough panels to power the total primary energy needs of the planet. The vision of abundant clean energy in the foreseeable future has transformed from dream to possibility; by reducing the materials intensity and cost of silicon photovoltaics, the goal is to transform it again… into reality.

1.2 The Photovoltaic Industry

The photovoltaic industry is in the midst of a period of extraordinary growth. Although it has been 175 years since the discovery of the photovoltaic effect by Edmond Becquerel in 1839 and 60 years since the demonstration of the first modern solar cell by Daryl Chapin, Gerald Pearson, and Calvin Fuller at Bell Labs in 1954[9,10], over most of their existence solar cells were confined to miniscule niche markets. In 2000, the total global installed capacity of photovoltaics



	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
RoW	751	807	887	964	993	1,003	1,108	1,150	1,226	1,306	1,590	2,098	2,098	2,098
MEA	n/a	n/a	n/a	n/a	1	1	1	2	3	25	80	205	570	953
China	19	24	42	52	62	70	80	100	140	300	800	3,300	6,800	18,600
Americas	21	24	54	102	163	246	355	522	828	1,328	2,410	4,590	8,365	13,727
APAC	368	496	686	916	1,198	1,502	1,827	2,098	2,628	3,373	4,951	7,513	12,159	21,992
Europe	129	265	399	601	1,306	2,291	3,289	5,312	11,020	16,854	30,505	52,764	70,513	81,488
Total	**1,288**	**1,615**	**2,069**	**2,635**	**3,723**	**5,112**	**6,660**	**9,183**	**15,844**	**23,185**	**40,336**	**70,469**	**100,504**	**138,856**

Figure 3 | Cumulative worldwide photovoltaic installations (MW), 2000-2013. RoW, MEA, and APAC are abbreviations for rest-of-world, Middle East and Africa, and Asia-Pacific, respectively. (Ref. 11)

was a mere 1,288 MW_p. (The output of a photovoltaic module is given in terms of watts peak (W_p) – the power produced by a solar module under standard one-sun conditions.) Fast forward to 2013, when total installed global photovoltaic capacity reached 138,900 MW_p, a staggering 43% compound annual growth rate over thirteen years, and it is obvious that the industry has undergone transformational change[11] (Fig. 3). The gravitational center of the photovoltaic industry has shifted during this time, first with the ascendance of photovoltaic manufacturing in Asia-Pacific and the concomitant decline in Europe and the United States in the late 2000s, followed by Asia taking the top spot in global PV installations beginning in 2013. Whereas Europe in 2011 saw 74% of the world's photovoltaic installations compared to 17% in Asia, in 2013 Europe was the destination of only 29% of installations compared with 56% in Asia.

Since the start of the new millennium, the cost of photovoltaic modules has declined steeply from about \$5.50/W_p in 2000 to just \$0.63/W_p in the second quarter of 2014 (2013 dollars)[12,13] (Fig. 4). The dramatic decline in photovoltaic module prices is a result of the confluence of a wide range of factors. The most significant has been the effect of scale as well as improvements in manufacturing processes and supply chain efficiencies that have amplified the effect of lower input prices. To this point, technology development has played a surprisingly backseat role in reducing the cost of PV modules. In spite of more than a decade of intense development of alternative photovoltaic technologies, second-generation technologies – such as thin film solar cells with absorbing films made of CdTe, CIGS, GaAs, or a-Si – have not been successful in gaining significant market share (First Solar and Solar Frontier are notable

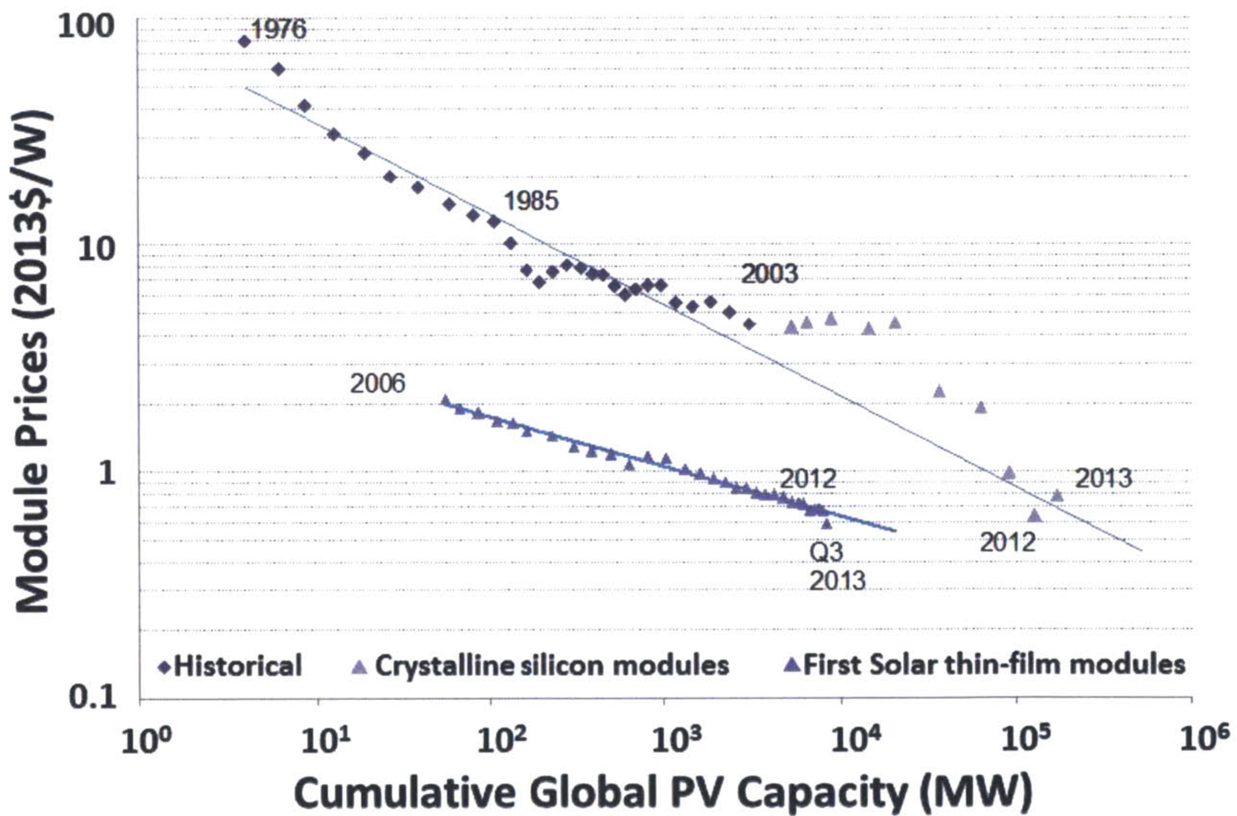


Figure 4 | Crystalline silicon and CdTe (First Solar) PV module average selling price (ASP) as a function of annual production volume. (Ref. 13)

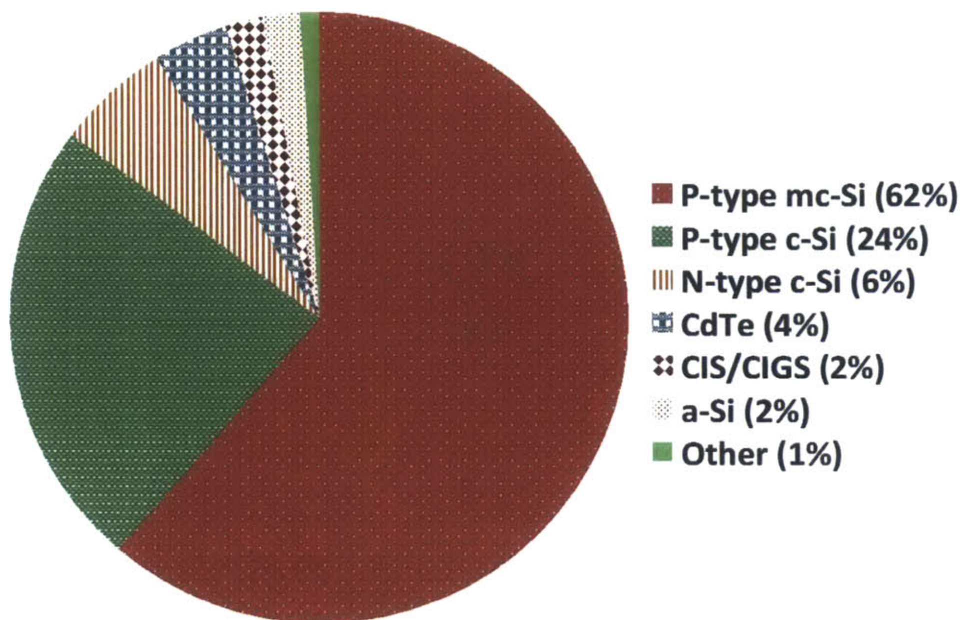


Figure 5 | 2014 global module sales mix. The abbreviations mc, c, and a refer to multicrystalline, crystalline, and amorphous, respectively. CI(G)S is an abbreviation for copper indium (gallium) diselenide. (Ref. 14)

exceptions, having successfully commercialized CdTe (6% of the global market) and copper-indium-diselenide (CIS) cells, respectively. The dominant technologies today remain p-type crystalline and multicrystalline silicon wafers with diffused junctions and screen-printed top-and-bottom contacts (Fig. 5).

1.3 A New Paradigm: Ultrathin Crystalline Silicon Solar Cells

Silicon has consistently served as the material system of choice for photovoltaics, presently owning a 90% share of the market[14]. And with good reason: Silicon has a bandgap that at 1.12 eV, while not ideal, is well-suited to producing efficient single junction solar cells. It is abundant and therefore not subject to resource constraints at scale. Moreover, given the lengthy history of the semiconductor industry there exists a vast pool of knowledge and experience around purifying, crystallizing, and processing on silicon.

The drawback to silicon is that it is a pricey material, at least in its current commercial incarnation. Silicon solar cells are typically fabricated on wafers ~170-180 μm thick (although SunPower is using wafers as thin as 135 μm), while a similar thickness is lost during wafer production when the wafers are sawn from a boule, known as "kerf loss". Combined with the expensive, multi-step process to purify and crystallize it, the silicon wafer alone accounts for 30-40% of the total module cost[15-17] (Fig. 6). Lowering the cost contribution of silicon could yield the needed price decreases to open up vast new markets for solar energy.

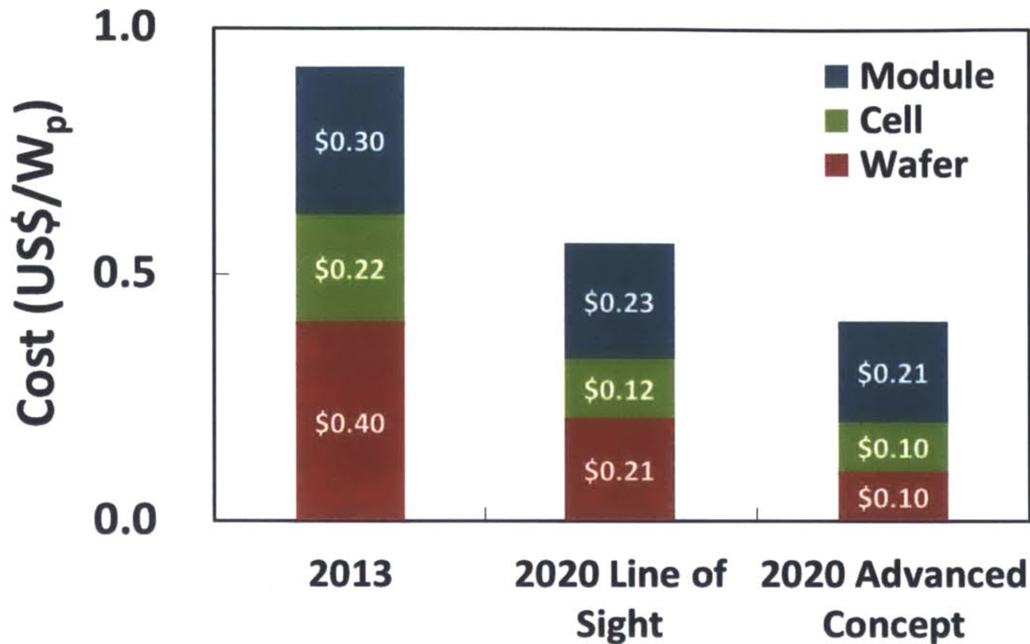


Figure 6 | Composite 2013 cost to manufacture a silicon photovoltaic module in the United States, along with cost projections out to 2020 for two different technology pathways. (Adapted from Ref. 15)

Promising approaches to cutting the silicon cost component of solar modules include innovative module designs with miniature concentrators[18] (J Yoon 2008); cell designs that leverage lower purity, low cost silicon[19] (Kwok 2012); and utilizing new wafer manufacturing strategies such as epitaxial silicon growth on porous silicon[20-22], forming a wafer directly from a melt (direct wafering)[23], or mechanical separation of thin films (spalling)[24] to reduce the volume of silicon used in a photovoltaic cell. In this work, the focus is on the latter approach, but with a focus on a specific question: Can silicon solar cells using drastically less silicon than commercial solar cells maintain competitively high efficiency? To do so, we must first address one of the principal obstacles to realizing thin film silicon photovoltaics: how to maintain high efficiencies while shrinking the volume of silicon available to absorb incident photons.

1.4 Light Trapping Background

As an indirect bandgap material, silicon photovoltaics are handicapped by poor absorption in the near-infrared wavelengths, which becomes particularly problematic for thin devices and can lead to unacceptable photocurrent loss. A large body of research has been built up to address this challenge by developing strategies to control the transport of radiative energy in a thin silicon absorber, "trapping" electromagnetic energy in the film and increasing the absorption probability so as to improve overall solar cell performance.

The concept of light trapping is not a new one. In 1974, Redfield introduced a solar cell design making use of angled features to increase the number of passes a photon makes through the absorber[25]. In the 1980s, random pyramid textures formed by etching silicon in a weak alkaline/IPA solution was pioneered, becoming the de facto standard for absorption enhancement

in wafer-based crystalline silicon solar cells[26]. The rise of ultrathin silicon PV concepts has generated renewed interest in the design of light-trapping structures. It is typically assumed that conventional random pyramid surface textures – on the order of 5-10 μm in height – are inappropriate for ultrathin films because the total volume of silicon removed during etching would compromise overall absorption. Nanophotonic light-trapping structures seek to address this issue by exploiting photon transport in the wave optics regime, leading to better absorbers that limit silicon removal.

A great variety of nanophotonic surface light-trapping geometries have been proposed in the literature, including nanoholes and nanocylinders[27-32], nanocones and nanodomes[33-38], inverted nanopyramids[39-42], nanowires[43-47], as well as more complicated random and parametric designs[38,48-49]. See Ref. 50 for an excellent review of nanophotonic light trapping designs. Other light-trapping approaches include Bragg reflectors integrated with rear diffraction gratings[51-55] and nanoparticles for plasmonic scattering and enhanced absorption[56-62]. Experiments have confirmed that many of these concepts increase absorption and some have been integrated into photovoltaic devices, but to date there has yet to be experimental confirmation of high photocurrent – and associated high efficiency – in a crystalline silicon device thinner than 20 μm based on an advanced light-trapping design.

1.5 Thin Crystalline Silicon Solar Cell Development

In parallel, research has proceeded apace on the development of crystalline silicon photovoltaics using thin and ultrathin substrates. Notable results include a 21.5% efficient, 47 μm device using a substrate thinning approach[63], and 19.1% and 16.8% efficient cells 43- and ~20-μm-thick, respectively, using epitaxial deposition and a porous silicon transfer process[20,64]. (Note that efficiency references in this thesis are based on the one-sun AM1.5G reference spectrum.) All use conventional surface texturing approaches – randomly spaced and sized upright pyramids greater than 1 μm in height - to increase absorption. (For reference, the best reported single-junction silicon solar cell of any thickness has an efficiency of 25.6% and short-circuit current (J_{SC}) of 41.8 mA cm^{-2} (Ref. 65).) For devices as thin as 10 μm, however, fabricating efficient crystalline silicon photovoltaics with integrated nanophotonic light management structures has proven very challenging given the combined optical and electronic design demands. Successes include 10-μm-thick devices with a nanocone surface light-trapping structure and 13.7% efficiency[35], nanowire solar cells with 5.3% efficiency[45], and 3-μm-thick devices with a nanocylinder surface texturing and 8.5% conversion efficiency[28]. In spite of these advances, the current delivered by existing devices with advanced light-trapping structures is not commensurate with the potential indicated by simulation.

1.6 Thesis Overview

The 10-μm-thick crystalline silicon photovoltaic cells presented in this thesis with a peak efficiency of 15.7% incorporate a two-dimensional inverted nanopyramid surface texture and rear metallic reflector light-trapping structure that has been previously shown to possess excellent anti-reflection and long-wavelength absorption capabilities[40,50]. Peak short-circuit current measures 34.5 mA cm^{-2}, marking a substantial improvement over previous devices in this

thickness range. Chapter 2 presents an overview of light-trapping theory and describes the optical design of the device, which demonstrates near-Lambertian absorption across the bulk of the spectrum from 500-1100 nm. Chapters 3 and 4 detail the parametric design considerations and the design of a fabrication process, respectively, for the ultrathin crystalline silicon photovoltaics developed in this work. The devices' optical and electronic characteristics are covered in Chapter 5, supplemented by simulation to help understand possible sources of voltage and current loss.

Chapter 6 relates a parallel experimental effort to test the assumption that periodic wavelength-scale optical structures are superior to periodic or random structures with micron-scale features. Through a combination of experiment and simulation, the relative absorption effectiveness of thin silicon films with a variety of pyramidal surface textures are compared: sub-micrometer inverted pyramids, micrometer-scale inverted pyramids, and random upright pyramids similar to conventional surface textures. The ultimate conclusion – that both periodic and random pyramidal structures of a wide range of sizes can provide near-ideal absorption in thin silicon films – will make it worth the read to the end of this thesis!

Chapter 2: Optical Design of Light-Trapping Structures for Thin Crystalline Silicon Photovoltaics

The current and efficiency advances of the ultrathin crystalline silicon photovoltaics described in this thesis are rooted in optical design. Developing an optical structure that minimizes surface reflection and parasitic absorption while maximizing internal absorption in silicon becomes all the more important as the device thickness shrinks. Beginning with the hypothesis that surface structures with unit cells on the order of the wavelength of visible light are most appropriate to very thin silicon films (which will be challenged later in Chapter 6), this chapter describes the design of the periodic wavelength-scale photonic crystal that is central to the optical performance of the thin film photovoltaics presented in this thesis. But first, we review light absorption in solid-state materials and its physical limits. Key equations are boxed in red.

2.1 Light Absorption and its Limit in Solid Films

The absorption of light in a solid is fundamentally a quantum mechanical process. In a direct bandgap semiconductor, photon absorption is a straightforward two-particle process involving an electron and a photon in which the photon is destroyed (absorbed) while donating its energy to a valence electron, promoting it to a discrete energy level available in the conduction band. The process is somewhat more complicated in an indirect bandgap semiconductor such as silicon where the smallest energy gap separating the valence and conduction bands is misaligned in momentum. Absorption of a photon is (most commonly) a three-particle process in this case, requiring a valence electron to couple simultaneously with a photon of appropriate energy and a phonon of appropriate momentum in order for the electron to transition from the valence to the conduction band (Fig. 7).

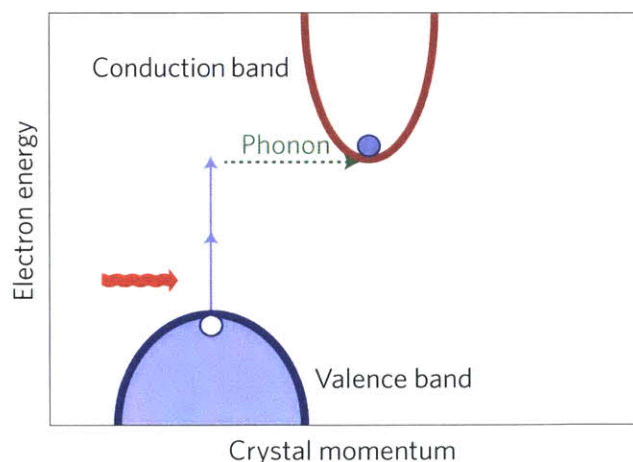


Figure 7 | Schematic of the photon absorption process in an indirect bandgap semiconductor.

Given the uncountable number of photons interacting with a solid at any given time, practical absorption processes are described statistically. The change in the intensity (I, W cm^{-2}) of an ensemble of photons with incident intensity (I_0) owing to absorption is give by the Beer-Lambert law:

$$I(z) = I_0 e^{-\alpha z} \tag{1}$$

where z is the depth into a film, and the effectiveness of a material at absorbing photons is given by the absorption coefficient (α) as a function of photon wavelength (λ):

$$\alpha(\lambda) = \frac{4\pi\kappa(\lambda)}{\lambda} \tag{2}$$

where κ is the imaginary part of the material's refractive index. The absorption coefficient is best conceptualized in terms of its inverse, $\alpha(\lambda)^{-1}$, which defines the *penetration length* – that is, the depth into a material sample at which ~67% (i.e., $1 - e^{-1}$) of photons at a given wavelength are absorbed.

Whereas the absorption coefficient is an intrinsic material property, absorptance – the ratio of the total number of photons absorbed in a material to the incident flux – is an extrinsic property of a material system that can be engineered. A very basic interpretation of Eq. 1 suggests that increasing the thickness of an absorbing film can raise the absorptance. Simple. But what if instead of increasing the material thickness, a material was engineered such that incident photons were guided into vectors that allowed the photon to remain in the material for much longer – to travel a much longer path length – thereby increasing the probability of absorption? This, in short, is the goal of light trapping.

2.1.1 The Yablonovitch Limit and Lambertian and Deterministic Light Trapping

There are multiple approaches to defining limits to photon absorption in a given material system. Perhaps the most well known was formalized by E. Yablonovitch using statistical mechanics[66]. A critical factor in the derivation of the Yablonovitch limit is the requirement that photons are randomized in orientation soon after encountering the absorbing film. The Yablonovitch limit is strictly valid in the geometric optics regime – where the wavelength is much longer than the film thickness and scattering features – but it is often extended to evaluate the effectiveness of wavelength-scale light-trapping designs.

The derivation of maximum absorption in the Yablonovitch limit begins with an assessment of the loss mechanisms of photons entering an absorbing film of thickness d. Assuming zero parasitic absorption at the boundaries and weak absorption, light is lost either through absorption in the bulk, which is given as:

$$2\alpha d I_{int} A_{inc} \tag{3}$$

assuming isotropic volumetric absorption, or it escapes out the front surface:

$$\frac{A_{esc}I_{int}\bar{t}_{esc}}{2n^2}$$

(4)

with A_{esc} and A_{inc} the surface area through which radiation exits and enters, respectively, I_{int} the internal radiation intensity, $\bar{t}_{esc}$ a weighted average transmissivity for escaping light, and n the real portion of the refractive index. These loss mechanisms are then equated in an energy balance with the incident radiative power, $A_{inc}t_{inc}I_{inc}$ – with t_{inc} the transmissivity of incident radiation of intensity I_{inc} – eventually yielding absorptance (A) in the Yablonovitch limit:

$$A = \frac{2\alpha d t_{inc}}{\frac{A_{esc}}{A_{inc}}\frac{\bar{t}_{esc}}{2n^2} + 2\alpha d}$$

(5)

Using the simplifying assumptions that $A_{inc} = A_{esc}$ and $t_{inc} = \bar{t}_{esc} = 1$, we recover the Yablonovitch limit:

$$A = \frac{4n^2\alpha d}{1 + 4n^2\alpha d}$$

(6)

Eq. 6 is actually an approximation of the exact formulation of the absorption limit, given in (Ref. 67) as:

$$A = \frac{1 - e^{-4\alpha d}}{1 - (1 - \frac{1}{n^2})e^{-4\alpha d}}$$

(7)

Whereas Eqs. 6 and 7 denote the maximum absorption that a film can experience in the geometric optics limit, the *absorption enhancement factor*, F, describes the benefit of a given optical light-trapping design compared to a flat film. The enhancement factor has a fairly straightforward geometric interpretation: it is the mean increase in path length for photons of wavelength λ in an absorbing film. As suggested in section 2.1, a longer path length – greater enhancement – leads to a correspondingly greater opportunity for absorption. For weakly absorbed photons and an isotropic emission pattern, the Yablonovitch limit gives a maximum average enhancement of[68,69]:

$$F = 4n^2$$

(8)

The Yablonovitch limit is a mathematical construct that defines the absorption limit in the geometric regime without prescribing a specific strategy to achieve the limit. There are in fact a multitude of theoretical schemes that satisfy the Yablonovitch limit. A common one is Lambertian light trapping, in which one or both surfaces reflect and refract incident photons diffusely, that is, after a scattering incident the "memory" of the incident angle is lost. However, as discussed in more detail in Ref. 69, Lambertian light trapping results in a collection of short path lengths within the total distribution of path lengths associated with the randomly scattered light. These photons are less likely to be absorbed. (Recall that F is given in terms of *average*

path length enhancement, meaning that many photons may still travel very short paths before coupling out of the film.) In this document, "Lambertian absorption" will commonly be used interchangeably with "Yablonovitch limit" in reference to the ideal geometric light trapping limit represented by Eq. 7.

An alternative theoretical scheme to Lambertian light trapping, coined "deterministic light trapping," imposes constraints on the angles that a photon can be reflected with each interaction with a surface. As a result, each photon undergoes a minimum number of internal reflections equal to 2n. Although the average path length enhancement is the same as Lambertian light trapping, the number of photons travelling long path lengths is greatly increased, as is overall absorption potential[69] (Fig. 8). The important takeaway is that the Yablonovitch limit and Lambertian absorption are crafted using specific assumptions; they are not in fact strict limits on the degree of absorption possible in a material film.

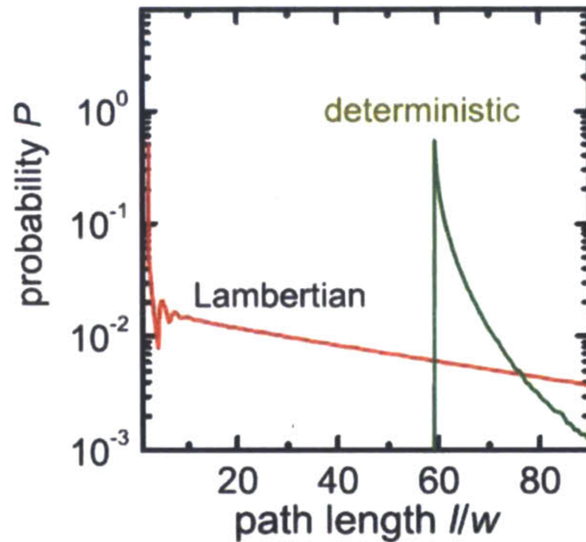


Figure 8 | Probabilistic distribution of photon path lengths for Lambertian and deterministic light trapping schemes. The relative path length (l/w) traveled by a photon in a material is the ratio between the absolute distance traveled by the photon l and the device thickness w. [(U. Rau, *PRB* (Ref. 69)]

2.1.2 The Thermodynamic Limit of Light Trapping and Size Effects

A more fundamental absorption limit would be that imposed by the second law of thermodynamics, which places a firm upper bound for the efficiency of any energy conversion process. Z Yu *et al.* develop the thermodynamic upper bound of absorption beginning with a definition of the number of photons emitted per optical mode (m) coupling to free space (p_m) for a material with thickness d and area L^2 (Ref. 70):

$$p_m = \frac{\gamma_m}{e^{\hbar\omega/k_B T} - 1} \tag{9}$$

where $\hbar$ is the reduced Planck constant (1.054×10^{-34} J•s), ω is the photon angular frequency, k_B is the Boltzmann constant (1.38×10^{23} J/K), T is the sample temperature (K), and γ_m is the external coupling rate of a given mode, the sum of which is subject to the condition:

$$\sum_m \gamma_m \leq \frac{L^2\omega^2}{4\pi^2c^2}\Delta\omega \tag{10}$$

for the angular frequency range ω to (ω + Δω), where c is the speed of light in vacuum. An insightful simplification to (4) can be obtained if the external coupling rate γ_m is equal for all modes:

$$\gamma_m = \gamma \leq \frac{c}{4d}\frac{\rho_{vac}}{\rho} \tag{11}$$

where ρ_{vac} is the density of states in vacuum ($\omega^2/\pi c^3$) and ρ is the density of states in the medium. From the second law, the sum of photons emitted by all optical modes ($\sum p_m$) must be equal to or less than the total photon flux of a black body (P_{bb}) at the same temperature, given by:

$$P_{bb} = L^2\frac{\omega^2}{4\pi^2c^2}\frac{1}{e^{\hbar\omega/k_BT}-1}\Delta\omega \tag{12}$$

After some manipulation, the resulting thermodynamic upper bound for the absorption coefficient A can be expressed as:

$$A \leq \frac{\alpha d}{\alpha d + \frac{1}{F}} \tag{13}$$

where F is the light-trapping enhancement factor described in section 2.1.1 and given here as

$$F = \frac{M}{N}\frac{2\pi\tilde{\gamma}}{\alpha d\Delta\omega} \tag{14}$$

M is the total number of modes supported by the material in the frequency range (ω, ω + Δω), N is the total number of free space channels, and $\tilde{\gamma}$ is the internal loss rate.

In a bulk structure with a grating of pitch a and thickness d, both much larger than the wavelength of interest, the number of channels N is:

$$N = \frac{2\pi\omega^2}{c^2}\left(\frac{a}{2\pi}\right)^2 \tag{15}$$

and M is given by[68]:

$$M = \frac{4\pi n^3\omega^2}{c^3}\left(\frac{a}{2\pi}\right)^2\left(\frac{d}{2\pi}\right)\Delta\omega \tag{16}$$

where n is the real part of the material's refractive index. From Eqs. 15 and 16, the absorption enhancement in the bulk case for normally incident radiation distills to:

$$F_{bulk} = 4n^2 \tag{17}$$

which is identical to the result found for the Yablonovitch limit in section 2.1.1. For silicon with $n \approx 3.9$, $F_{bulk} \approx 61$. For reference, the maximum theoretical absorption enhancement factor is $F \approx 200$ (Ref. 70).

When the length scale of the unit cell of a grating structure begins to approach the wavelength range, Eq. 15 loses its validity, opening up the possibility to improve the absorption enhancement factor over the bulk case. As shown in Fig. 9 for a related grating structure with periodicity L, enhancement above $4n^2$ is possible for specific wavelength ranges. The grating serves to restrict the number of channels available to free space, limiting out-coupling of trapped modes and increasing the average effective path length in the material. The discontinuities in the enhancement factor result from the availability of new channels to free space, allowing more modes to couple out of the slab and reducing path length enhancement.

In this thesis, the focus is on photovoltaics that range in thickness from 5-20 μm and Eq. 16 is applicable to the calculation of the number of waveguide modes in the film. Additional opportunities to improve the enhancement factor F arise when the film thickness becomes much smaller than the wavelength. Please see Ref. 68 for more discussion about light trapping in wavelength-scale films.

With this understanding of the physical bounds on absorption in thin films with gratings, we now transition to a qualitative discussion of the design of light-trapping structures for ultrathin crystalline silicon solar cells.

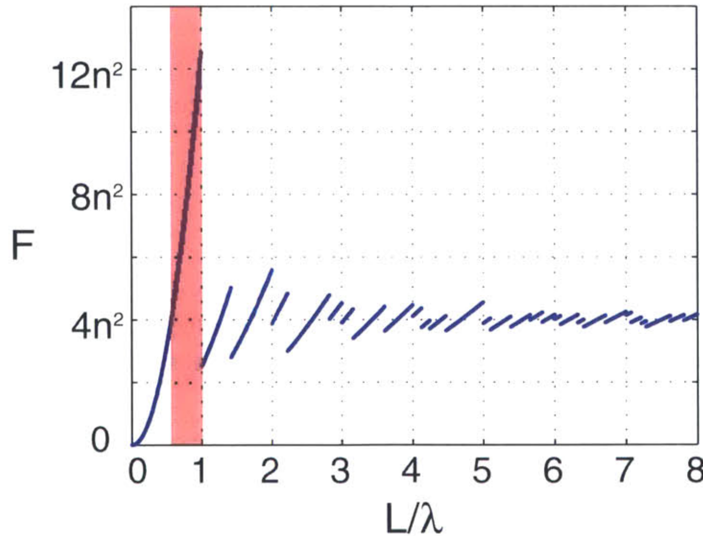


Figure 9 | Average path length enhancement as a function of grating period normalized by wavelength. These results are calculated for a planar surface with a backside square grating. The abrupt changes in the enhancement factor are the result of new emission channels becoming available. [Z. Yu, *Proc. Natl. Acad. Sci. USA* (Ref. 68)]

2.2 Design of Light-Trapping Structures for Ultrathin Silicon Solar Cells

Texturing surfaces to enhance the absorption of photons – and therefore short circuit current – has been a part of the PV engineer's toolkit since the 1970s[25,26]. The light-trapping schemes that have been traditionally applied to thick-film solar cells consist of randomly textured pyramids that are large in comparison with the bandgap wavelength of silicon and function in the geometric optics regime where light propagation can be described by ray tracing of photons (Fig. 10). Using a Monte-Carlo ray tracing analysis, Campbell & Green find that more than half of incident photons are coupled out of a surface with large random pyramid textures after one pass through the material, but that the total average path length enhancement still approaches the Lambertian case (factor of 43 enhancement for $n = 3.4$, compared to 46 in the Lambertian case)[26]. Clearly, these large format (~5-10 μm average height) random pyramids function as effective light-trapping structures for thick silicon films.

The design of light-trapping structures for solar cells thinner than 20 μm requires an altogether different design approach than can be applied to conventional silicon solar cells. As the thickness of silicon used to produce a solar cell shrinks, so does the available space for light-trapping elements. The logical strategy to develop efficient light management designs in ultrathin films is to utilize very small features that can leverage wavelength optics effects to maximize absorption in a film while minimizing material loss. The design criteria by which a surface structure approaching the Lambertian limit might be realized are detailed in Ref. 39:

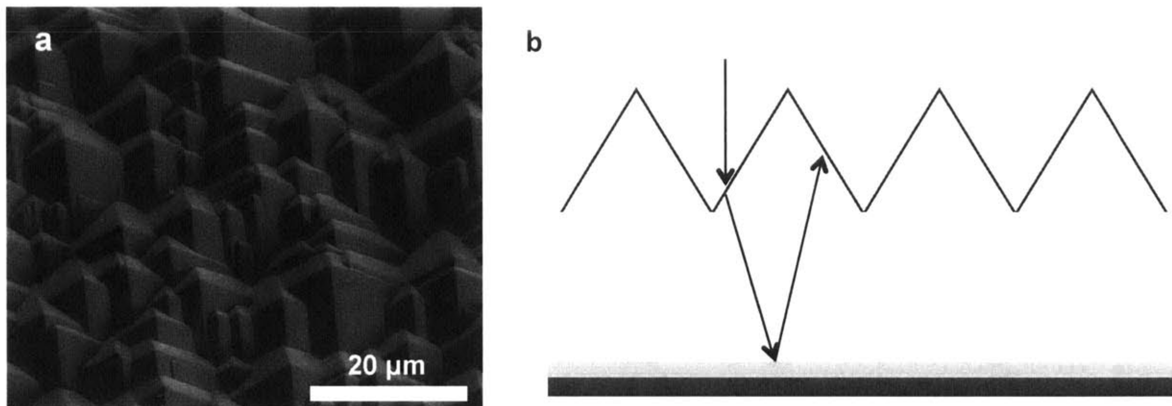


Figure 10 | Geometric light trapping and conventional surface textures for enhanced absorption. **a,** Sample image of random pyramid surface texturing used in most commercial solar cells. (Source: Ref. 71) **b,** Schematic of geometric light trapping. Photons, represented as particles, are confined in an absorbing film by multiple internal reflections.

Table 1: Design criteria for effective anti-reflection and light trapping

	Design Criteria	Design Application
#1	Maximize number of diffraction channels	Two-dimensional gratings superior to one-dimensional
#2	Optimize light coupling	Tapered and index-matched structures yield best results
#3	Excite all available waveguide modes	Minimize symmetries in the structure

Even with these guidelines, there exists a virtually infinite solution space of designs. To constrain the range of potential solutions, we focus on concepts that can be readily and inexpensively fabricated on real materials. One of the most robust and repeatable approaches in microfabrication to producing tapered surfaces on silicon (Criterion #2) is to use alkaline wet etchants, such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH)[72,73]. This class of silicon etchants has an exceptionally high selectivity – on the order of 30:1 – between the major crystal planes (100) and (110) and the (111) plane, resulting in precise 54.7° sidewalls (relative to the surface plane).

Nature was very kind in facilitating the alkaline/silicon system for it happens that the etch angle is nearly ideal for minimizing surface reflection and maximizing total absorption in a thin silicon film. As can be seen in Fig. 11 from the results of finite element electromagnetic wave

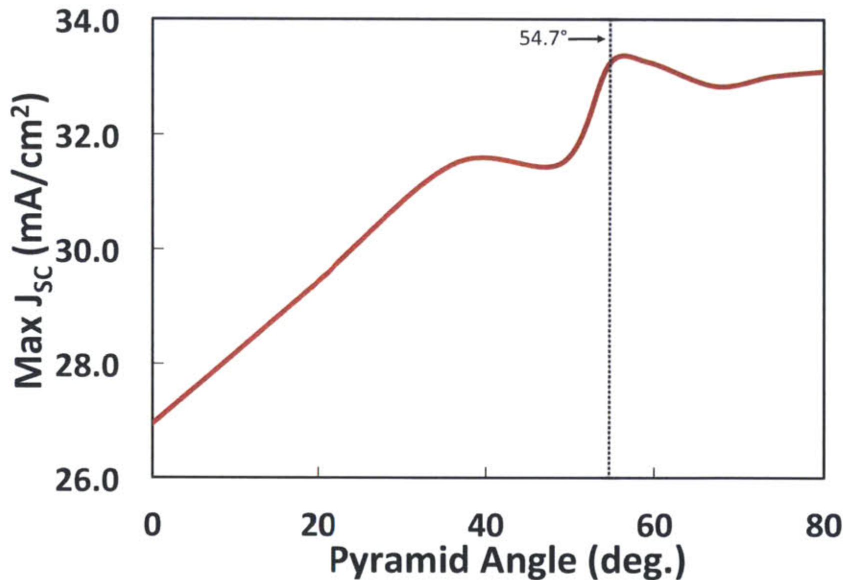


Figure 11 | Total integrated absorption (300<λ<1105 nm) for periodic inverted pyramids as a function of pyramid angle for a fixed 700 nm pitch. The simulated film structure is the same as Fig. 42d, with a textured silicon film sandwiched between a 100 nm PECVD silicon nitride layer on the top surface and 200 nm silicon dioxide layer below. The back reflector is a 200 nm aluminum layer. Silicon film thickness is 10 μm; ridge width is fixed at 50 nm. *Data courtesy W.–C. Hsu, MIT.*

simulation for absorption in silicon films with surface pyramidal light-trapping structures of varying angle, total absorption reaches a local maximum almost precisely at the 54.7° etch angle of KOH. In Fig. 11 as throughout this thesis, total absorption is represented in terms of maximum short-circuit current ($J_{SC,max}$), which is calculated as the inner product of the absorption and solar spectra (AM 1.5G):

$$J_{SC,max} = \int_0^{\lambda_g} \left(\frac{q\lambda}{hc}\right) * A(\lambda) * I_{AM1.5}(\lambda) d\lambda \tag{18}$$

The maximum short-circuit current is defined as the current that a photovoltaic device would produce if all absorbed photons from the solar spectrum were converted into current under short-circuit operating conditions.

By constraining the solution space of light-trapping designs to ones with pyramidal features and following the remaining design guidelines, a series of candidate geometries were developed. In earlier work in the NanoEngineering group at MIT, the transfer matrix method was used to simulate the absorption effectiveness of silicon films with these various textures[39,74]. As can be seen in Fig. 12, all approach Lambertian light trapping. Skewed pyramids (those having an apex not centered over the base) offer the best performance of pyramidal structures owing to a reduction in symmetry compared to the other designs.

Considering the need for straightforward fabrication, normally-oriented inverted pyramids were eventually selected as the surface structure that would be implemented in

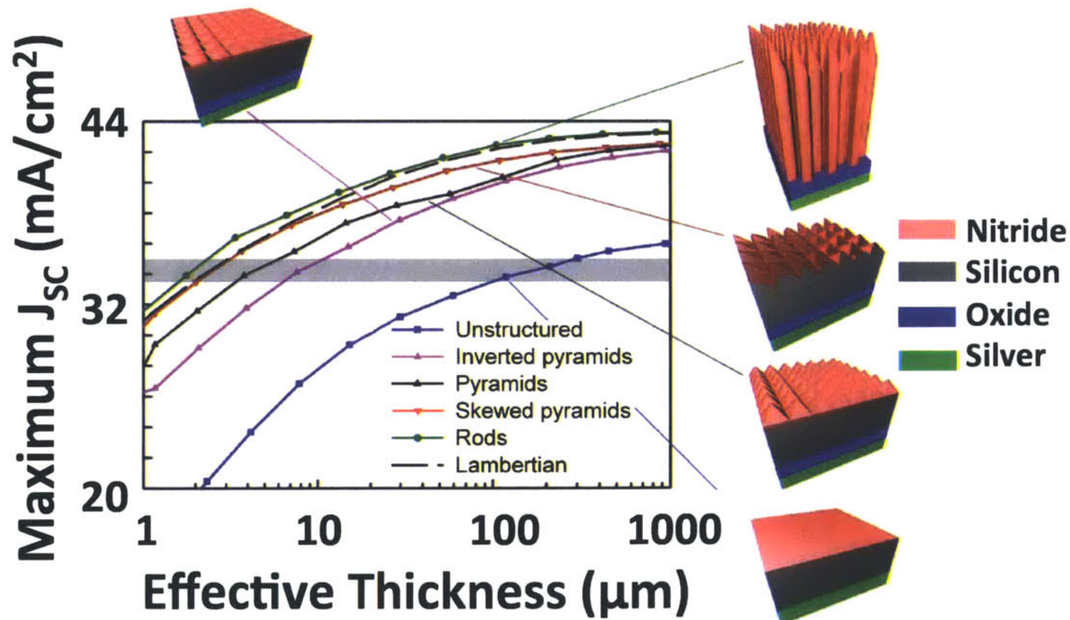


Figure 12 | Absorption effectiveness of pyramidal light-trapping structures. The effective thickness is defined here as the thickness of a planar silicon film with the same mass as the structured silicon layer. Each silicon structure is topped with a 90-nm-thick silicon nitride anti-reflection coating and has a 1 μm silicon dioxide (blue) and 200 nm silver (green) back reflector stack (except for the planar case, which has a 61 nm nitride and no oxide layer). [S. E. Han, *Proc. SPIE Micro- Nanotech. Sensors, Systems, Appl. III* (Ref. 74)]

experimental devices. These structures can be formed from (100) silicon wafers using a nitride hard mask and alkaline wet etchant. As described in Chapter 7, skewed inverted pyramids were successfully fabricated using (210) silicon. However, (210) silicon wafers are currently expensive and difficult to source, particularly in SOI form.

Early simulation using the transfer matrix method indicated that a 700 nm pitch yielded maximum absorption for the inverted pyramid geometry[40]. The surface texture geometry is only one element of the total optical design required for high absorption capability. The remainder of the optical design shall be described in Section 3.4.1.

2.3 Experimental Validation of Inverted Nanopyramid Absorption Effectiveness

The light-trapping efficiency of inverted nanopyramid structures was confirmed in earlier experiments within the NanoEngineering group at MIT[40]. Samples were fabricated on SOI wafers with 10-μm-thick device layers using a procedure similar to that described in Section 4.1 and 4.2 (except using interference lithography) to form a two-dimensional array of inverted pyramids on a 700 nm pitch. The samples were completed with a 90 nm top nitride anti-reflection coating ARC, 1 μm rear dielectric, and silver back reflector as in Fig. 12.

The absorptance of the textured film stack, measured using a spectrophotometer with an integrating sphere and plotted in Fig. 13, confirmed the theoretical findings very nicely over

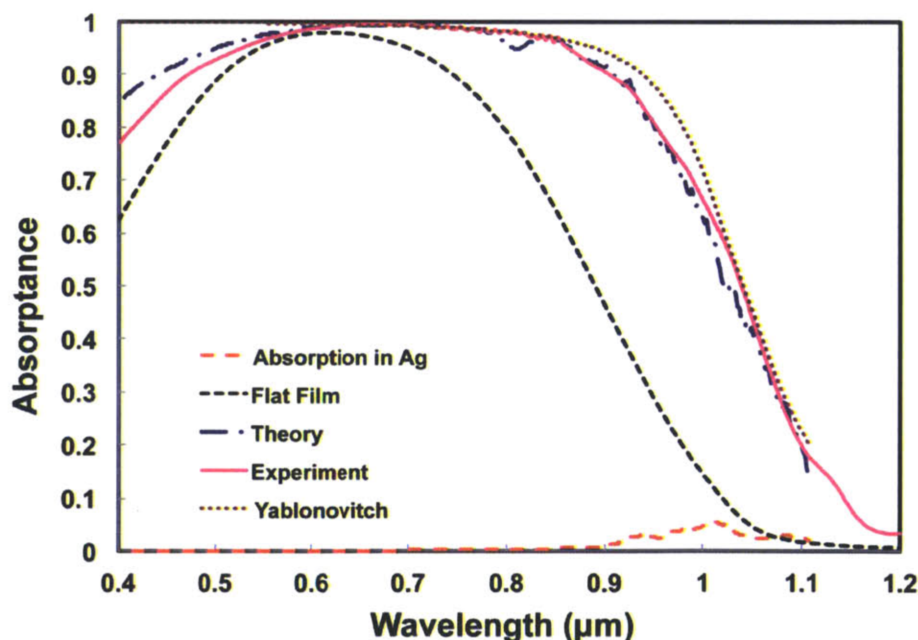


Figure 13 | Theoretical and experimental absorption spectra of a 10-μm-thick silicon film textured with inverted pyramids on a 700 nm pitch. The structure is given in Fig. 12. The Yablonovitch limit and the experimentally-measured absorptance spectrum of a planar silicon film of the same thickness are included for reference, as well as calculated absorptance in the silver layer. Note that absorption in the modeled and experimental data is not limited to the silicon film and includes all layers in the film stack. [A. Mavrokefalos, *Nano Lett.* (Ref. 40)]

most of the relevant spectral range for silicon photovoltaics. With the exception of the short wavelength region, the experimentally-measured values of absorptance approach the maximum defined by the Yablonovitch limit. Most importantly, absorption in the infrared portion of the spectrum from 800 nm to 1100 nm is dramatically enhanced with respect to a 10-μm-thick planar silicon film with a nitride ARC and back reflector. The planar cell absorbs roughly 79% of normally-incident radiation compared to 98% for the textured film at 800nm. At 1000 nm, the difference is even more pronounced: 66% absorption for the planar film compared to 14% for the textured film, an impressive 5–fold enhancement. At short wavelengths (below 500 nm), the experimental results for absorption deviate from those predicted theoretically. The source of this disagreement is suspected to be the difference in the width of the ridges separating the inverted pyramids, which vary over the range of tens of nanometers in experimental fabrication. As the width of the ridges separating inverted pyramids increases, more surface area is available that is normal to the direction of incident radiation, which increases reflection across the spectrum but most dramatically in the short wavelength range.

2.4 Summary

The Yablonovitch limit prescribes an upper limit for absorption in films with dimensions that are large in comparison with the wavelength of light. Wavelength-scale features and film thicknesses make it theoretically possible to exceed this limit, opening up the potential for silicon solar cells that are much thinner than current technology but of comparable efficiency. A range of sub-micron, angled surface geometries were developed prior to this thesis work in the pursuit of a design with absorption exceeding the Yablonovitch limit, with skewed upright pyramids performing the best (Section 2.2). Films with inverted pyramid surface textures, though less effective than upright normal and skewed pyramids, were also demonstrated theoretically and empirically to absorb very effectively (Section 2.3). Given that inverted pyramids are more easily fabricated – and thus a more promising geometry for commercial applications – than the alternatives, inverted pyramids were selected as the basis for the ultrathin silicon photovoltaics developed in this thesis.

Chapter 3: Design of a High-Efficiency Thin-Film Crystalline Silicon Solar Cell

3.1 Silicon Solar Cell Fundamentals

A photovoltaic is fundamentally a thermodynamic engine that converts the excess potential energy of photons into useful electrical power. In a silicon solar cell, the heart of the device is the pn-junction, the boundary between adjacent material layers with different doping polarities – one that contributes excess holes and one that contributes excess free electrons. As illustrated in Fig. 14, the pn-junction serves to separate an excited minority charge carrier – generated through the photon absorption process described in Section 2.1 – from its counterpart to harness the excess energy imparted by the photon. If instead of crossing the pn-junction an excited carrier recombines with its counterpart, the potential energy is dissipated through thermalization or re-radiation. This simple depiction helps make clear the basic origin of the current produced by a solar cell, which to first order is given by the number of photons absorbed in the silicon and subtracting those that dissipate their energy through recombination before reaching the pn-junction. A more detailed description of the operating principles of photovoltaics is outside the scope of this thesis, but an excellent resource with interactive tutorials can be found at: http://www.pveducation.org/pvcdrom.

A silicon photovoltaic is a specialized diode. Recall that an ideal diode, without illumination, can be described mathematically as:

$$J = -J_0\left(\exp\left(\frac{qV}{kT}\right) - 1\right) \tag{19}$$

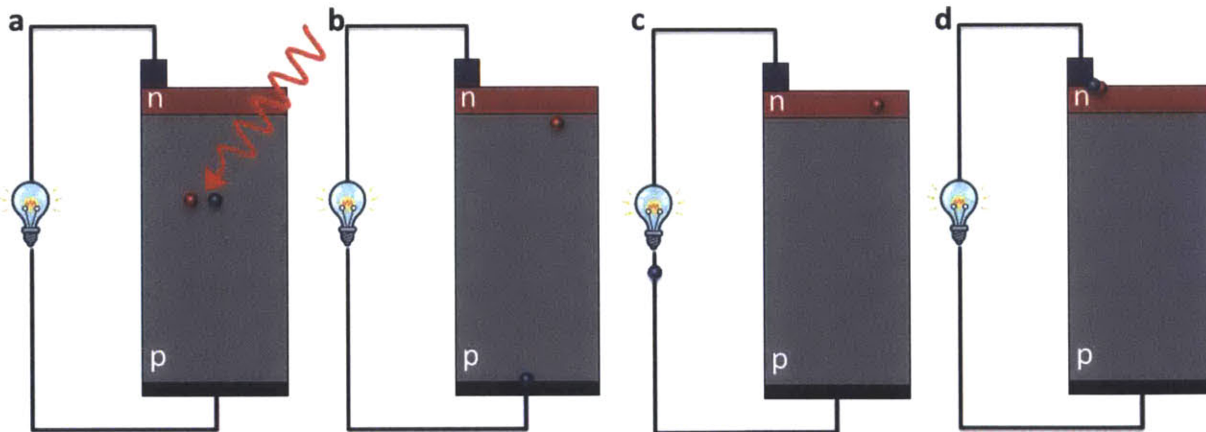


Figure 14 | Operation of a solar photovoltaic. a, A photon with energy $\hbar\omega > E_g$, the bandgap of silicon, generates an electron-hole pair upon absorption. **b,** The minority carrier electron (red) diffuses to the pn-junction, where it is swept across into the n-type region. **c,** To compensate for the loss of a minority carrier from the p-type region, a majority hole conducts out of the device and through the resistive load. **d,** The electron recombines with its counterpart at the top contact to complete the circuit.

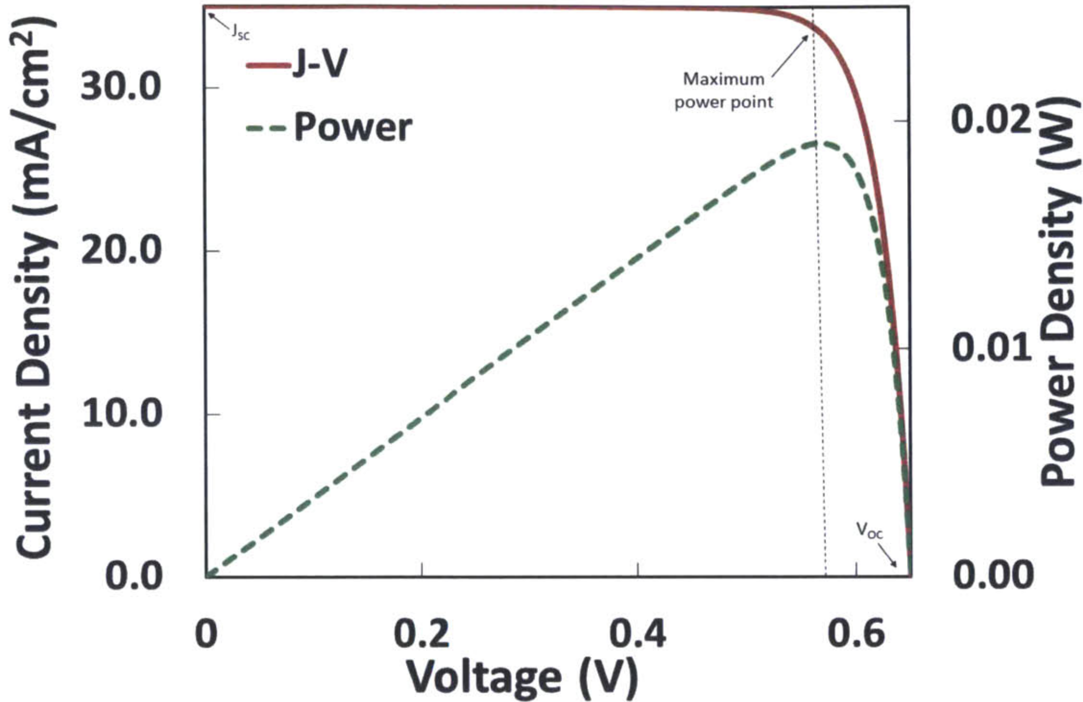


Figure 15 | Current density (J, mA cm^{-2}) and power versus voltage for an ideal solar cell absent shunt and series resistance.

where J and J_0 are the current and dark current densities (A cm^{-2}), respectively, q is the fundamental unit of charge, and V the applied voltage. The negative sign in front of J_0 is a convention in the field of photovoltaics to locate the J-V curve in the first quadrant. Under illumination, the ideal diode curve shifts positive by the value of the light-generated current density (J_L):

$$J = J_L - J_0\left(\exp\left(\frac{qV}{kT}\right) - 1\right) \tag{20}$$

A sample current-voltage plot of the output of a solar cell is given in Fig. 15. The ideal diode model is useful to understand the origin of the power generated by a solar cell. With no voltage applied across the device, a solar cell generates its maximum current – known as the short-circuit current (J_{SC}) – but no power. As the voltage applied across the device begins to rise, the current output drops, first very slowly before rolling off steeply as the open-circuit voltage (V_{OC}) is approached, at which point the current output drops to zero. In an ideal diode, the current decreases with increasing voltage because the applied voltage reduces the electrical barrier across the diode, leading to greater minority carrier injection across the junction and ultimately retarding the diffusion current of minority carriers to the pn-junction. As the rate of minority carrier extraction slows, a greater number of carriers have the opportunity to recombine before being collected. The open-circuit voltage represents that point at which the current generated by illumination is precisely balanced by recombination.

Between the short-circuit current and open-circuit voltage, the power generated by a solar photovoltaic reaches a maximum in the vicinity where the current begins to sharply roll off. It is at this maximum power point that the efficiency (η) of a solar cell is defined:

$$\eta = \frac{V_{mp} I_{mp}}{\Phi} = \frac{V_{OC} I_{SC} FF}{\Phi} = \frac{V_{OC} * J_{SC} * FF * A}{\Phi} \tag{21}$$

where Φ is the incident radiative power, V_{mp} and I_{mp} are the voltage and current at the maximum power point, respectively, I_{SC} is the short-circuit current produced by the device with surface area A, and FF is the fill factor. The fill factor is simply the ratio between the maximum power output of the solar cell and the product of V_{OC} and I_{SC} (i.e., it is a measure of how "square" is the real diode curve). These three top-level parameters – V_{OC}, I_{SC} and FF – are themselves functions of many other intrinsic and extrinsic parameters of an individual solar cell, which can be reviewed in the references listed at the end of this section. Several timeless references derive the maximum efficiency of a silicon solar cell considering radiative[75], Auger[76], and surface recombination[77].

The current-voltage relationship of an actual solar cell can differ substantially from that of the ideal diode case. There are myriad factors that lead to deviations in actual solar cell performance from the ideal case, but the two most important to discuss are shunt and series resistance.

In a real solar cell, current channels can exist that are electrically in parallel with the diode, reducing the current that would otherwise be provided to the load. Shunt resistance captures the resistance of a device to these parallel currents. Shunts typically arise owing to processing defects or contamination, such as improper edge isolation or metal contamination that creates a current path across the pn-junction. High shunt resistance characterizes an efficient solar cell.

Contrarily, an efficient solar cell will possess low series resistance. Series resistance reduces the power output of a photovoltaic cell by dissipating carrier potential through I^2R loss. Series resistance primarily arises from lateral majority carrier transport through the emitter, contact resistance between the semiconductor and the metal contacts, and current flow in the top and bottom contact metals.

The effect of series (R_s) and shunt (R_{sh}) resistance can be added to the ideal diode model to produce a more realistic model of solar cell performance:

$$I = I_L - I_0\left(\exp\left(\frac{q(V + IR_s)}{kT}\right) - \frac{V + IR_s}{R_{sh}}\right) \tag{22}$$

The effect of shunt and series resistance on the current-voltage relationship in a sample device is shown in Fig. 16. It can be seen that low shunt resistance leads to a finite slope of the low voltage portion of the I-V curve, whereas high series resistance leads to a less negative slope of the portion of the I-V curve near V_{OC}. As can be understood from these plots, moderate decreases in shunt resistance and increases in series resistance primarily impact photovoltaic performance by reducing the fill factor.

Still more complicated models of solar cell performance have been developed, beginning with a two-diode model. But the key points necessary to follow the remainder of this chapter are captured in the single-diode model, and the interested reader is encouraged to learn more at the

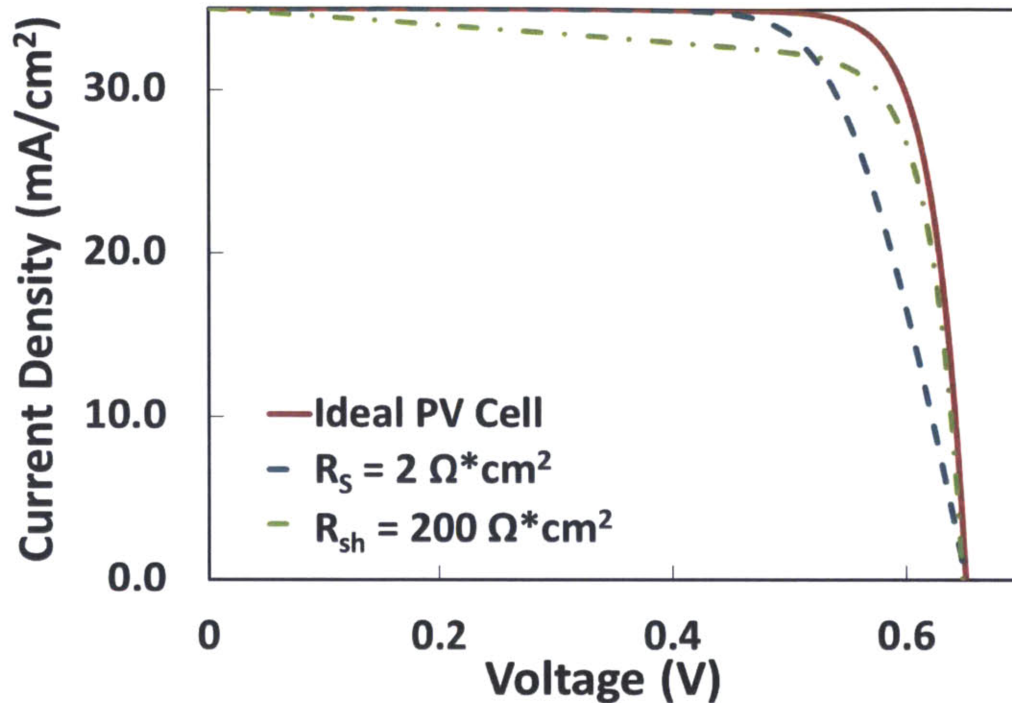


Figure 16 | Impact of series and shunt resistance on current density-voltage characteristics of a model PV cell.

website listed earlier or in Refs. 9 and 78-79. Refs. 80-82 were also quite useful to the author in the parametric photovoltaic device design described in the remainder of this section.

3.2 Thin-Film Crystalline Silicon Substrate Processing Alternatives

A principal technological hurdle to the realization of thin crystalline silicon films is the fabrication and handling of the substrates. Crystalline silicon is a brittle material, and the highly ordered structure makes it susceptible to failure by fracture or chipping, particularly with decreasing thickness. To date, there have been a limited number of approaches to producing the very thin substrates needed to reduce the silicon intensity of photovoltaics, among them epitaxial silicon deposition and removal using the porous silicon process, stress-induced peeling, and direct casting of wafers. Additionally, mechanical thinning of bulk wafers has been used for demonstration purposes.

A promising approach to the manufacture of ultrathin crystalline silicon solar cells is the porous silicon process[21,83]. A low-quality, inexpensive silicon wafer is first electrochemically etched in a dilute hydrofluoric acid solution to form a porous double layer. After annealing in hydrogen, a buried layer forms with a high density of voids. Crystalline silicon is deposited atop the silicon substrate using epitaxy, and the top surface bonded or adhered to a carrier for mechanical support. The newly-formed device can then be easily removed from the original substrate using mechanical force. Such a process allows for multiple uses of the growth substrate and minimal consumption and waste of silicon. It is primarily limited by epitaxial growth rates, which in modern tools can be several micrometers per minute.

Another method that has been explored extensively is the use of stress-induced peeling of silicon[24]. This approach commonly takes two forms. In the first embodiment, a metal (or polymer) is deposited on bulk silicon. The metal (or polymer, at cryogenic temperatures) induces a stress on the silicon surface, which when mechanically disturbed – for example, by a diamond scribe – can allow the silicon to simply be peeled off using an adhesive like Scotch® tape[84]. The choice of metal and the temperature of the substrate dictate the depth at which the peeling occurs. AstroWatt and IBM have both worked on research and commercialization of this technique. In the second embodiment, ion implantation is used to heavily dope a silicon layer with hydrogen at a prescribed depth. After annealing, this hydrogen forms a weakened porous layer, which again can allow the thin top layer to be mechanically removed using an adhesive or by crack initiation. SiGen and Twin Creeks Technologies (now owned by GT Advanced Technology) have attempted to commercialize this approach. The advantages of stress-induced peeling are the lack of kerf and the potential to complete several solar cells fabrication steps prior to separation, but there are still significant handling and uniformity challenges to be addressed before this technology can be considered for commercial application.

A third manufacturable approach to thin silicon wafer fabrication is direct casting. Commercialized by 1366 Technologies, a high-quality multi-crystalline wafer is cast directly from silicon melt, avoiding many of the lossy and costly intermediate steps involved with producing a wafer using the preceding methods or conventional die sawing. It is unclear if this technology can produce substrates thinner than 20 μm with high yield, but it bears mention for its expected low cost and high quality.

Substrate thinning is a fourth technique that is employed for making ultrathin crystalline silicon films. Typically, a solar cell is fabricated on a bulk wafer and then mechanically thinned using chemical mechanical polishing to the desired thickness and then mounted to a carrier for final processing. Although it is prohibitively expensive to manufacture solar cells in this way, it is useful for building laboratory demonstration devices. In fact, a 21.5% efficient, 47-μm-thick device was fabricated using this method, the most efficient "thin" silicon solar cell ever reported[63].

In this thesis, a derivative of the substrate thinning approach is used to demonstrate a high-efficiency ultrathin silicon solar cell. Given the combination of demanding cleanliness requirements, multiple mask layers requiring both front- and back-side alignment, and the sub-micron scale of the surface light-trapping structure, fabrication was carried out in the Microsystems Technology Lab (MTL) cleanroom facility at MIT. Essential processing tools require a 6" wafer, and given that an unsupported silicon film thinner than 20 μm would be too fragile for such an involved process, silicon-on-insulator (SOI) wafers served as a platform for the photovoltaic cells. As will be described later, the determination of substrate carrier is a critical one, and in this case the use of freely-suspended membranes embedded in a bulk SOI wafer introduced its own challenges. A compelling alternative would be to use whole-wafer-thinning and bonding methods, similar to those described in Ref. 51.

3.3 Ultrathin Crystalline Silicon Membrane Solar Cell Architecture

The architectural design of the ultrathin crystalline silicon solar cells developed in this thesis reflect the goal of optimizing optical performance while maintaining excellent electrical performance, subject to the constraints of the cleanroom environment and microelectronic

fabrication equipment available. In selecting a membrane architecture embedded in a rigid substrate, the challenges of layer transfer are avoided at the expense of significant yield loss owing to both breakage of the fragile devices and KOH attack during the membrane formation step.

One of the consistent challenges in the design of these ultrathin solar cells is electrical isolation of the device to prevent electrical communication with the surrounding silicon. Failure to do so can result in erroneous measurements – by collecting carriers from outside of the defined collector area – or poor performance through current shunts.

Early designs consisted of a one-micrometer-deep "isolation trench" to define the active area of the device (Fig. 17a), which led to persistent isolation issues. The device architecture evolved significantly over the course of the development effort, ultimately leading to the mesa design depicted in Fig. 17b. A mesa structure, in which all adjacent silicon is etched away to leave each individual cell isolated from the surrounding silicon device layer, addressed the isolation issue and provided for reliable and repeatable device characterization.

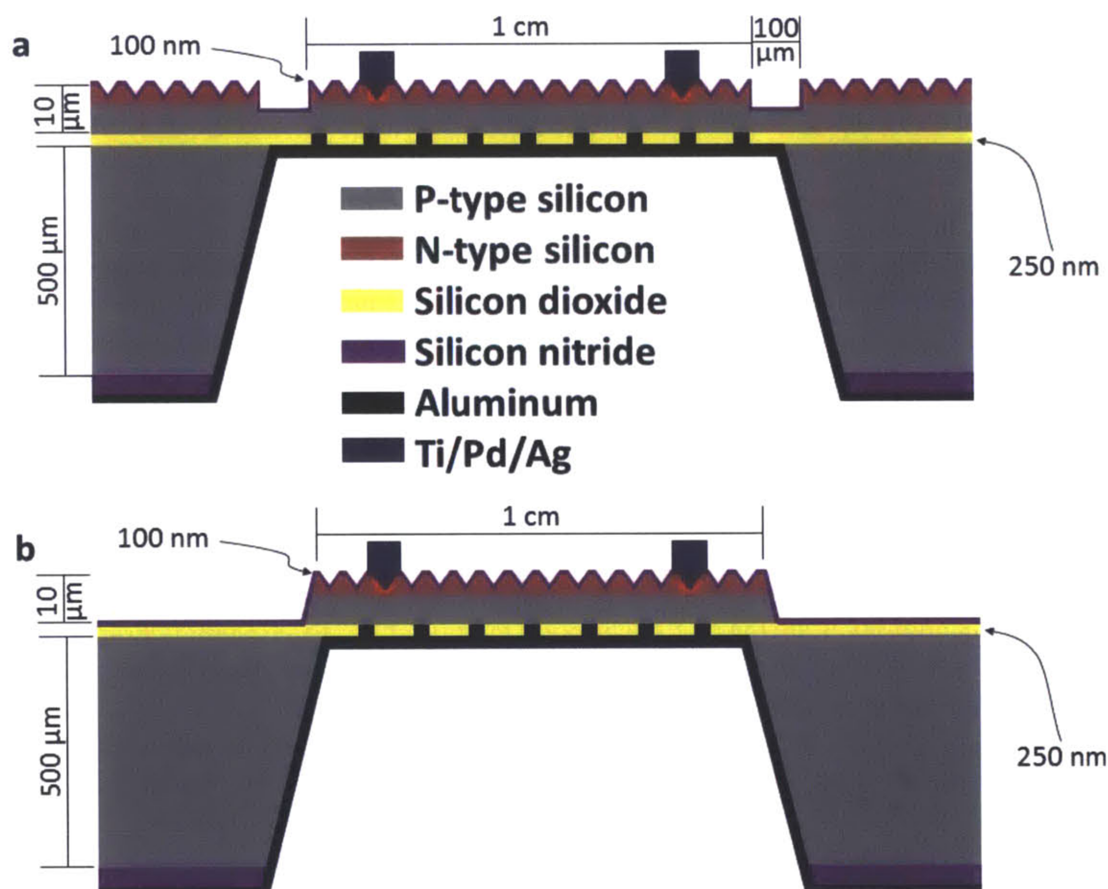


Figure 17 | Schematic of thin crystalline silicon photovoltaics emphasizing different isolation techniques. a, The original solar cell design implemented an isolation trench to define the active one square centimeter device area. **b**, In the final design, isolation was achieved using a mesa structure to ensure robust device characterization and improve operating performance by eliminating the possibility of shunts to the remainder of the silicon device layer.

3.4 Solar Cell Parameter Design

Solar cell design requires the simultaneous consideration of both electronic and photonic transport when specifying materials and geometries. The incorporation of a nanostructured light-trapping structure and the extraordinary fragility of crystalline silicon thin films constrain the design of such devices even further. This section reviews the design of material parameters and relates their impact on the design and fabrication of the entire thin film solar cell. As described in section 3.2, the devices are fabricated on 10 μm silicon films supported by an SOI wafer.

3.4.1 Optical Design

The optical elements of the device were designed using the transfer matrix method and finite element analysis in previous work and are reviewed in more detail in Chapter 2 (Ref. 40). Sub-micron inverted pyramids with a KOH etch angle of 54.7° were found to provide peak absorption for a 700 nm pitch when coupled with a PECVD nitride ARC of 100 nm thickness. A back reflector is required in concert with the front surface texturing to confine electromagnetic energy in the silicon absorber. Silver would be preferred for purely optical purposes owing to its low parasitic absorption, but silver tends to adhere poorly to silicon and forms a very rough interface without the presence of an adhesive film such as titanium. Furthermore, in the design of a photovoltaic device, the back reflector needs to serve as a contact metal. Aluminum provides a superior ohmic contact to p-type silicon than silver[85], so it is specified as the back metal in spite of higher parasitic absorption. A dielectric film placed between the absorber and the back reflector minimizes parasitic absorption in the aluminum reflector by channeling electromagnetic energy away from it into the absorber (much like how a bathroom mirror is far more reflective than a bare sheet of metal). The absorption effectiveness of the overall design is relatively insensitive to oxide thickness beyond a few tens of nanometers; in this design, the thickness of the buried oxide layer of the SOI wafer was specified at 250 nm. This thickness provided leeway in the event of overetching during the backside membrane release etch in KOH.

3.4.2 Emitter, Contact, and Base Doping

The carrier concentration in the n- and p-type silicon layers is a key parameter dictating overall device performance. This section describes the design of doping levels for the n-type emitter and top contact regions, as well as the p-type base. Ideally, the doping level in the vicinity of the back contact would also be prescribed and carefully engineered. Owing to the difficulty of implanting the back of the wafer after forming the suspended membrane, boron-implanted p^{++} back contacts are omitted. The design relies instead on diffusion of aluminum during a final high temperature anneal in forming gas to impart p^{+} character to the back contact region. Aluminum doping will result in higher back surface recombination velocities compared to boron[86].

3.4.2.1 Base Doping Design

Even in the case of a 10-μm-thick solar photovoltaic, the base – or collector – is responsible for the majority of light absorption. In this design, it is specified as p-type and electrons are the minority carriers. The background doping level in the base (N_A) directly influences V_{OC} through the saturation current (I_0), as can be understood from the following equations for a solar cell with an ideal abrupt pn-junction and n- and p-type regions much longer than the minority carrier diffusion lengths[78]:

$$V_{OC} = \frac{k_B T}{q} \ln\left(\frac{I_{SC}}{I_0} + 1\right) \tag{23}$$

$$I_0 = \left(\frac{q D_n n_i^2}{L_n N_A} + \frac{q D_p n_i^2}{L_p N_D}\right) \tag{24}$$

The diffusivity and diffusion lengths are given as D_n and L_n, respectively, for electrons as the minority carriers in the region of p-type doping with concentration N_A, and D_p and L_p for holes as the minority carriers in the region of n-type doping with concentration N_D. The intrinsic carrier concentration, n_i, has a value of approximately $1.1*10^{10}$ cm^{-3} at 300 K, and the short-circuit current (I_{SC}) is a positive value in this formulation. The inverse relationship between saturation current and base doping implies that N_A should be very high. However, higher doping simultaneously decreases the minority carrier diffusion length (L_n), which negatively impacts V_{OC}. These conflicting requirements for the base dopant concentration imply that an optimal doping level exists.

In a real device, the optimal doping level is a complex function of the aforementioned factors, as well as the thickness of the device, the emitter characteristics, and rear surface recombination rates. Very thin devices such as the one being developed here can tolerate higher doping levels since the effect of bulk lifetime is somewhat subdued[78,87]. For the purposes of this project, the background doping level was designed using PC1D, a one-dimensional solar cell simulation software[88]. A more rigorous calculation of the base doping level would require treatment of the three-dimensional nature of the device using a finite-element solver such as COMSOL or Sentaurus Device.

The PC1D simulation results suggest an optimal base doping level of 9.0×10^{16} to 2.5×10^{17} cm^{-3} (0.1-0.2 Ω cm) (Fig. 18). Low resistivity SOI wafers are challenging to source, however, and the actual SOI device layers were specified with p-type doping levels of 2.0×10^{16} to 3.1×10^{16} cm^{-3} (0.5-0.735 Ω cm).

3.4.2.2 Emitter Doping Design

The two most important roles of the n-type emitter are to: 1) absorb high-energy photons and injects minority carrier holes into the p-type base region and 2) provide lateral transport for majority carrier electrons to the top contacts. Similar to the base, these two demands impose contrasting doping requirements: to satisfy the first role, doping levels should be lower so as to minimize Auger recombination of minority carriers in the emitter (which will otherwise reduce open-circuit voltage), whereas the second role dictates that the doping be high

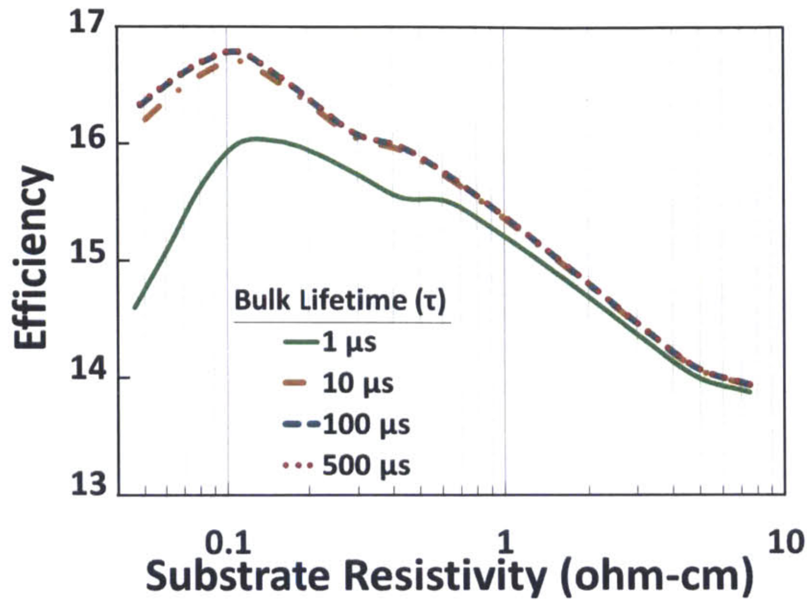


Figure 18 | Dependence of base doping level on efficiency for a 10 μm-thick photovoltaic cell. Simulated efficiency as a function of base background doping level and lifetime for a 1D solar cell using PC1D. Simulation parameters: exterior front reflectance = 5%, internal optical reflectance = 100%, front surface recombination = $9x10^2$ cm s^{-1}, rear surface recombination = $1x10^5$ cm s^{-1}, front surface doping peak = $1.4x10^{20}$ cm^{-3}.

enough to provide low-resistance lateral transport for majority carriers. The emitter can also improve device performance when it is designed with a concentration gradient so as to repel carriers from the surface. The thickness of the emitter, defined by the PN junction depth, also influences solar cell performance in multiple ways. On the one hand, a thin emitter is desired to minimize the number of photons absorbed in the high-Auger-recombination region, while at the same time an overly thin emitter increases the likelihood of shunts caused by contaminants forming conducting channels across the PN junction.

These qualitative guidelines can inform the design of the emitter, but they overlook the many non-idealities inherent in the formation of an emitter using ion implantation into a three-dimensional surface. For this thesis, the emitter parameters were designed in PC1D using a one-dimensional analogue of the real devices to optimize the peak doping level and thickness. One-dimensional simulation is a gross approximation of the three-dimensional problem for the purpose of calculating absolute performance, but it provides useful design guidance. The peak emitter doping level was selected as $2x10^{19}$ cm^{-3}. For the junction depth, given the uncertainty of contamination in the fabrication process and the consequent risk of shunts, the design erred on the side of a thicker junction, ultimately targeting 0.5-0.6 μm, whereas for a standard commercial solar cell it would be 0.25-0.3 μm. Sheet resistance of the emitter is specified to be 60-80 Ω/□.

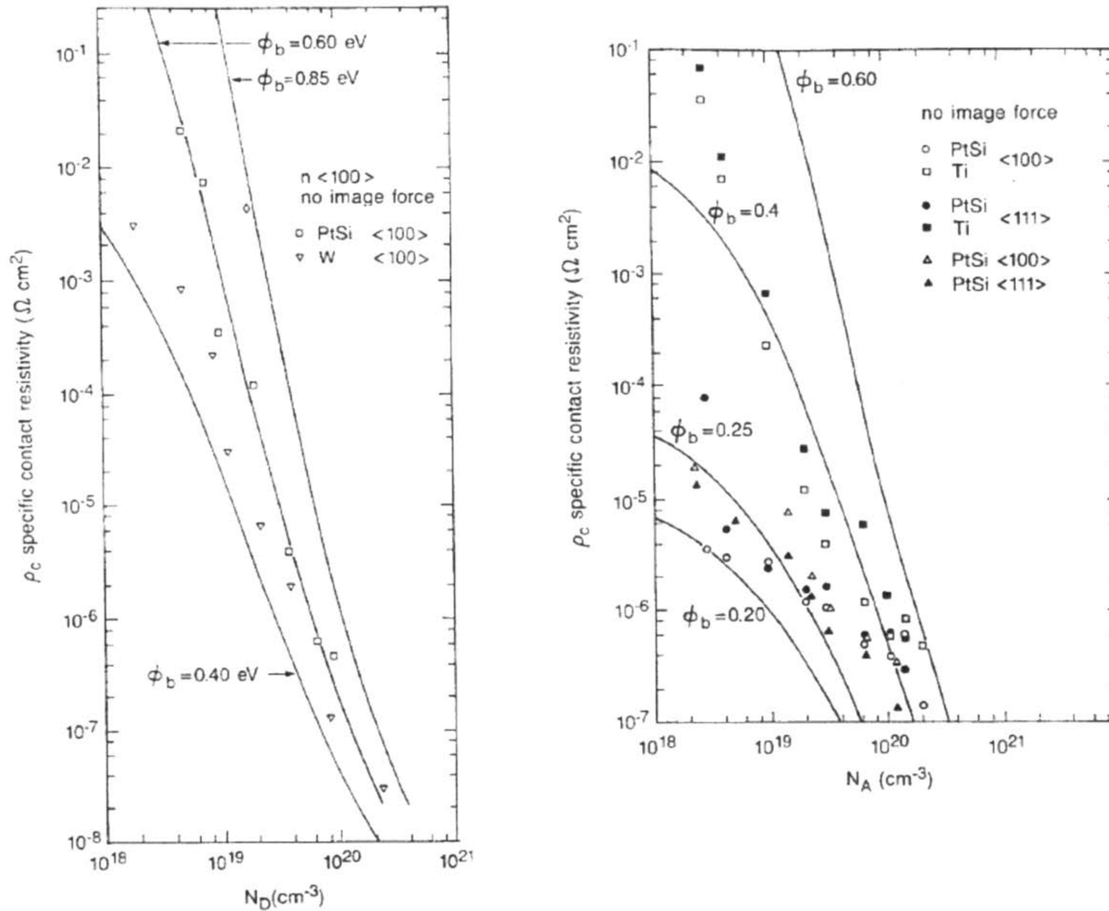


Figure 19 | Contact resistance as a function of silicon doping level for selected metals to n-type (left) and p-type (right) silicon. [S. E. Swirhun, *J. Electrochem. Soc.* (Ref. 89)]

3.4.2.3 Top Contact Selective Doping Design

The doping level in the emitter is too low to provide ohmic contact with the top metal fingers. In lieu of raising the emitter doping – which would increase Auger recombination in the emitter and lower the open-circuit voltage – one may instead increase the doping density locally in the top contact region. High doping in the contact region produces a sharp feature in the silicon band structure across which carriers can travel via tunneling, resulting in a contact resistance with less rectifying behavior (Ref. 79, Ch. 7). The relationship between contact doping and resistance is strongly exponential as can be seen in Fig. 19, and the contact doping level was selected to be $1.5x10^{20}$ cm^{-3}.

3.4.2.4 Implantation and Implant Oxide Parameter Design

One of the notable process design innovations of this work is a single-step implantation process to independently form the emitter and selective contacts using an oxide implant mask of varying thickness. An oxide implant mask serves two roles: 1) it randomizes the direction of implanted ions to minimize channeling effects and 2) it prevents evaporation of the topmost layer

of dopants during the high-temperature diffusion/anneal step. In this design, a thin oxide is specified for the contact regions, while a thicker oxide is specified for the remainder of the cell area. Selective doping is accomplished by first implanting phosphorus ions at high energy but low dosage to dope the emitter, followed by implanting arsenic ions at low energy but high dosage. The arsenic implant is designed such that it only penetrates the oxide in the thin contact regions, leading to heavily doped contacts and lower doping in the remainder of the emitter.

For ion implantation and diffusion of a dopant in silicon, an analytical expression of the resulting dopant concentration C as a function of depth x and diffusion time t is[90]:

$$C(x,t) = \frac{Q}{\sqrt{2\pi(\Delta R_P^2 + 2Dt)}} e^{-\left(\frac{(x-R_P)^2}{2(\Delta R_P^2+2Dt)}\right)} \tag{25}$$

where Q is the implantation dose (cm^{-2}), D is the intrinsic diffusivity of the dopant in single-crystal silicon (cm^2 sec^{-1}), R_P is the implant depth (cm), and ΔR_P is the implant standard deviation (cm) – the latter two of which can be estimated using Fig. 8.3 in Ref. 90. To obtain a more accurate one-dimensional calculation of the implanted profile, particularly in the presence of a silicon dioxide implant layer, the implantation parameters and oxide thicknesses were designed using Sentaurus Process. The targeted doping levels and junction depths are defined in Sections 3.2.2.2 and 3.2.2.3. The oxide thickness was specified to be 35 nm in the contact region and 100 nm elsewhere. The simulation neglected the three-dimensional nature of the actual devices, resulting in the omission of a few key details:

1. Quite obviously, the use of a planar surface omits the impact of varying surface height on the final shape of the emitter, which would yield gross changes in the implanted profile.
2. The simulation was executed assuming an oxide thickness determined by growth on planar (100) silicon. In reality, the pyramidally-textured surface consists of exposed (111) planes (in addition to remnant (100) planes) on which silicon dioxide grows at ~1.54 times the rate of (100) surfaces. The effect of variable oxide thickness is not captured in this simulation.

Based on the results of simulation, the final implantation parameters were specified as:

Dopant	Angle	Energy (keV)	Dose (cm^{-2})
Phosphorus (P)	7°	110	$9x10^{14}$
Arsenic (As)	7°	70	$2.8x10^{15}$

The junction diffusion/annealing step was given as 60 minutes at 1000°C, yielding a junction profile from 1D simulation as shown in Fig. 20 for the contact and non-contact regions. Again, given that the actual device surface is three-dimensional rather than planar, the true junction profile and resistivity are not accurately captured in this simulation.

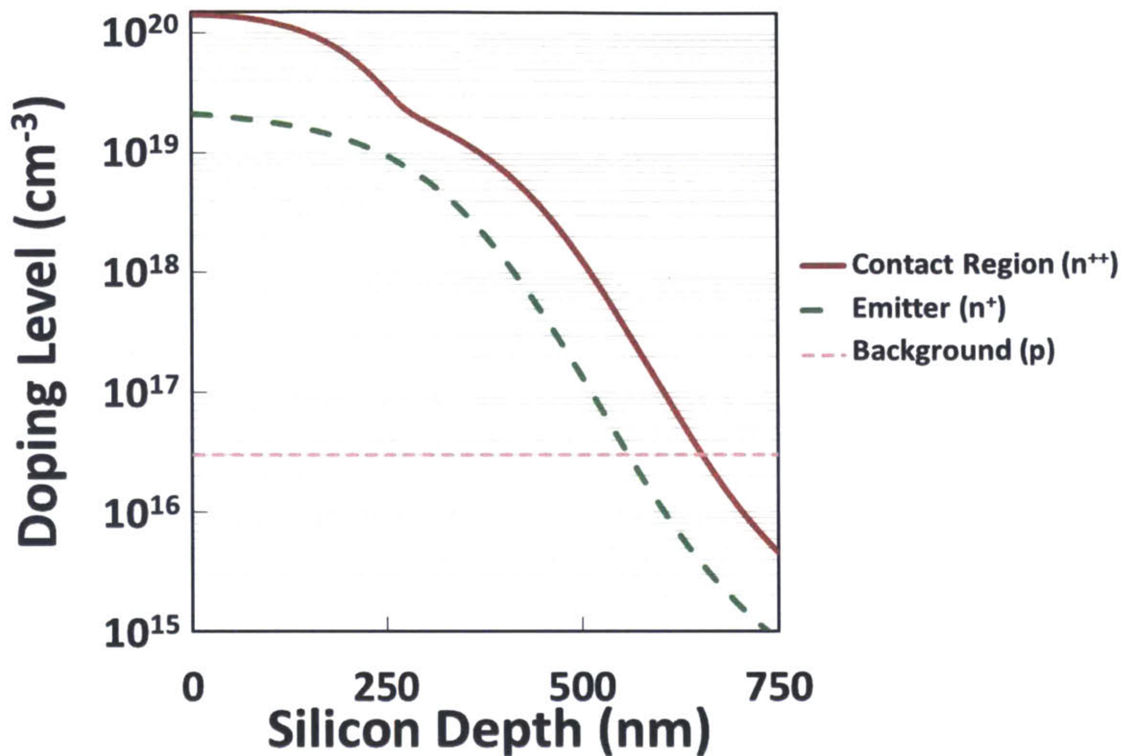


Figure 20 | Simulated pn-junction doping characteristics using a 1D ion implantation model. Implantation parameters: contact region masking oxide = 34 nm, emitter masking oxide = 99 nm, phosphorus dose and energy = 9×10^{14} cm^{-2} and 110 keV, arsenic dose and energy = 2.8 x 10^{15} cm^{-2} and 70 keV, tilt angle = 7°

3.4.3 Surface Passivation

For a silicon solar cell of such thinness, the quality of surface passivation is very important for producing an efficient device. In original process flow designs for this thesis, a very thin (7 nm) thermal oxide provided top surface passivation, which was then coated by LPCVD nitride for optical anti-reflection. The passivation qualities of this material stack are acceptable, with measured surface recombination velocities on low-doped p-type silicon above 100 cm s^{-1}. Instead, it was found that PECVD nitride deposited using the DCVD tool in the ICL cleanroom within the Microsystems Technology Laboratories at MIT yields excellent surface passivation on p-type silicon, measured at less than 10 cm s^{-1} (measured via transient photoconductance decay (PCD) using an inductively coupled RF coil, Sinton Instruments WCT-120). The n = 1.9 index of this material also makes it an excellent anti-reflection coating. The final process design incorporated a 100 nm coating of this brand of PECVD nitride for top surface passivation and anti-reflection.

The rear surface is passivated to some extent by the 250 nm thermally grown buried oxide layer of the SOI wafer, which serves as the default backside passivation layer in this design. Silicon dioxide does not passivate p-type silicon as well as n-type, but the passivation quality is improved by annealing with an aluminum cap as is done in the final step of this

process. This step, referred to as an "alneal" in the literature, provides enhanced passivation of the rear surface over standalone silicon dioxide by hydrogenating dangling bonds at the silicon surface[81]. Rear surface passivation is one important aspect of the design of the device that could be readily improved upon in future experiments to increase power conversion efficiency.

3.4.4 Contact Design

The selection of contact materials, thickness, width, and spacing are particularly important for preserving a high fill factor, while affecting short-circuit current and open-circuit voltage to a lesser extent. This device design employs a double-sided contact scheme, with separate electrical connections to the p-type base on the bottom of the device and n-type emitter on the top. The motivation for designing top- and bottom-contacts is driven by optical performance. The alternative to double-sided contacts is an all-back-contact (ABC) design in which local contact is made to areas of alternating p^+ and n^+ doping[35]. In a very thin cell, the gaps between metal wires that are required for electrical isolation in an ABC design allow a significant fraction of long wavelength light to leak out the back side of the device, as the back metal serves a vital role as a reflector for the light-trapping stack. The attendant short-circuit current loss is avoided by the use of a blanket back contact in a double-sided design.

3.4.4.1 Back Contact Design

Although silver provides superior optical performance as a reflector owing to low parasitic absorption, aluminum was selected for the back contact material because it forms a contact to p-type silicon with more ohmic character[85] while still functioning reasonably well as a back reflector. Contact to the p-type silicon base of the photovoltaic cell was made by etching holes in the silicon dioxide layer before sputtering aluminum. The spacing between contacts was designed with input from coupled optical/electronic device simulation (*courtesy S. Yerci*) and literature. With decreasing contact pitch, fill factor generally improves while open-circuit voltage remains relatively constant[35]. Contrarily, decreasing the back-contact pitch by too large an amount can reduce short-circuit current as a result of the larger areal fraction of metal-coated silicon. This loss occurs because parasitic optical absorption is much higher for bare aluminum on silicon than when an oxide dielectric separates the silicon and aluminum layers. The competing effects of the back contact on device efficiency – combined with the realities of back contact formation (see Chapter 4) – dictated a back contact pitch of 75 μm.

The size of the metal contact area should be kept as small as reasonably possible. Larger contacts degrade device performance by 1) serving as high-recombination-velocity centers for minority carriers and 2) parasitically absorbing a greater fraction of long wavelength radiation than oxide-cladded metal. Typically, a contact on the order of 5 μm in diameter would be preferred. However, given the constraints of fabrication, back contact sizes ranged from 20-30 μm.

The final step of the fabrication process consists of a sintering step at a temperature of 475-500 °C. This step leads to diffusion of aluminum into the silicon to create a p^+ back surface field in the vicinity of the contact. Aluminum-doped silicon yields poorer back contact minority

carrier recombination characteristics than boron-doped selective contacts[86], but it is a substantial improvement over a metal in contact with lightly doped silicon.

3.4.4.2 Top Contact Design

For the top metal contacts, a titanium/palladium/silver metal stack was used for high-quality ohmic contact to n-type silicon[78,91]. The bottom layer is a 40 nm titanium adhesion layer, which also matches the band structure of silicon well. The top layer is a thick 920 nm silver layer that provides low-resistivity conductance. Sandwiched between the two is a 40 nm palladium film that serves to prevent diffusion of silver through titanium and into the silicon emitter.

Designing the top contacts is an optimization problem with the goal of minimizing total power loss through shading and resistive losses. The contact lines should generally be made as thin as possible to limit shading losses, and in this design were designated at 30 μm wide. Power losses owing to reflection from the metal contacts and normalized to the maximum power output ($p_{shading}$) are given as[9]:

$$p_{shading} = \frac{W_F}{S} \tag{26}$$

with W_F the finger width and S the pitch, which implies that larger spacing (along with narrow lines) are preferred to limit shading losses. In contrast, lateral current flow in the device emitter, a major source of resistive power loss in PV cells with double-sided contacts, is reduced with a narrower spacing between contact fingers. For the grid pattern used here, normalized lateral resistance losses in the emitter ($p_{res,lat}$) are given by[9]:

$$p_{res,lat} = \frac{\rho_S}{12} \frac{J_{mp}}{V_{mp}} S^2 \tag{27}$$

with ρ_S the sheet resistance of the emitter. A third source of loss is resistive loss in the metal wires themselves[9]:

$$p_{res,fingers} = \frac{B^2 \rho_{smf}}{3} \frac{J_{mp}}{V_{mp}} \frac{S}{W_F} \tag{28}$$

with B the half-length of the contact fingers (fixed for this cell design at 0.5 mm) and ρ_{smf} the sheet resistivity of the contact metal. Finally, contact resistance ($p_{res,contact}$) between the metal contacts and the semiconductor is a fourth loss mechanism[9]:

$$p_{res,contact} = \rho_c \frac{J_{mp}}{V_{mp}} \frac{S}{W_F} \tag{29}$$

with ρ_c the specific contact resistance (Ω cm^{-2}). As indicated earlier, the objective is to find the contact spacing S that minimizes total power losses:

$$p(S) = min(p_{shading} + p_{res,lat} + p_{res,fingers} + p_{res,contact}) \quad (30)$$

The contact finger spacing is given by iteratively solving Eqs. 26-30 for the given contact width $W_F = 30\mu m$ while varying the contact spacing S. For an initial guess S', subsequent trial values of S can be determined using the equation[9]:

$$S'' = \frac{S'(3p_{shading} - p_{res,lat} - p_{res,contact})}{2(p_{shading} + p_{res,lat})} \quad (31)$$

Using a sheet resistance for the emitter of 80 Ω/□ and specific contact resistance of 10^{-8} Ω cm^{-2}, we arrive at a spacing of ~1.4 mm for the metal contact fingers, or seven contact lines across a 1 cm^2 device area. The shaded area totals 2.1% of the device area, or 2.1 mm^2.

An important innovation in the contact design of these devices is the placement of the bus bars. Bus bars are wider metal lines designed to reduce resistance while carrying the current funneled by many contact fingers, analogous to a large river fed by many small tributaries. Bus bars are typically located on the active area of a solar cell, given that the entire surface area of a solar cell is used for collecting sunlight. Bus bars also serve as contact points for electrical probes during characterization. In the suspended membrane design of the experimental device demonstrated here, probing the physical device area is impossible because of the fragility of the very thin crystalline films. To compensate, the thick metal bus bars were placed outside of the active device area on top of the thick silicon bulk where they could be easily probed without damaging the cell. The seven metal contact fingers collect current from the emitter, then slope down and off the device itself before connecting to the bus bars, as shown in Fig. 21.

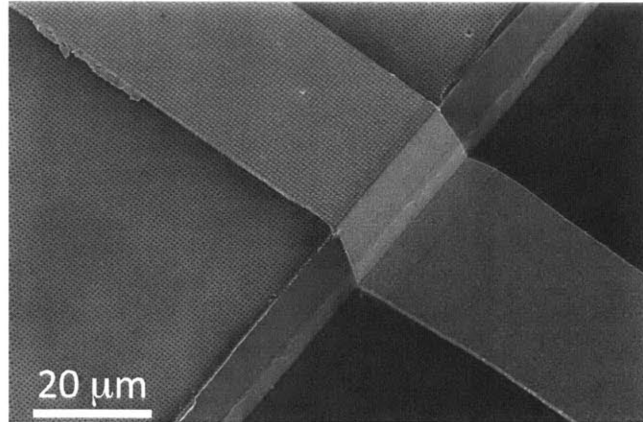


Figure 21 | SEM image of a top metal contact finger on a mesa device. Note the continuity over the mesa sidewall as the contact moves from the membrane device to the bulk region.

3.5 Summary

An efficient ultrathin crystalline silicon solar cell requires careful optical and electronic design, further constrained by the poor mechanical strength of the substrate and limitations imposed by fabrication equipment. This chapter describes the design of laboratory-scale crystalline silicon thin film solar cells fabricated on SOI wafers. Electrical isolation was accomplished by implementing a mesa architecture in which the silicon device layer surrounding each individual cell was removed, resulting in greater confidence in wafer characterization and improved performance over the use of shallow trench isolation (Section 3.3). Optical considerations resulted in a front surface textured with a two-dimensional photonic crystal consisting of inverted pyramids on a 700 nm pitch and coated with 100 nm of PECVD silicon nitride, and a blanket rear aluminum reflector sandwiching a thin (200-250 nm) silicon dioxide dielectric. The aluminum reflector doubled as the bottom contact in this two-sided contact design through 20-30 μm holes on a 75-μm pitch. The top titanium/palladium/silver contact fingers were 30 μm wide with a spacing of 1.4 mm. Additional details, such as doping levels, implantation parameters, and passivation characteristics can be found in Section 3.4 and in the process descriptions that follow in Chapter 4.

Chapter 4: Thin-Film Crystalline Silicon Solar Cell Process Design and Development

This chapter details the fabrication process that was developed to produce a very efficient, ultrathin crystalline silicon solar cell platform useful for experimental demonstration of advanced light-trapping features. A collection of resources that the author found useful in the design of the process flow include Refs. 9, 72, 78, 80-81, 86, & 91-97. A schematic of the final process flow is presented in Fig. 22. Additional useful information gained from processing experience can be found in Appendix 3.

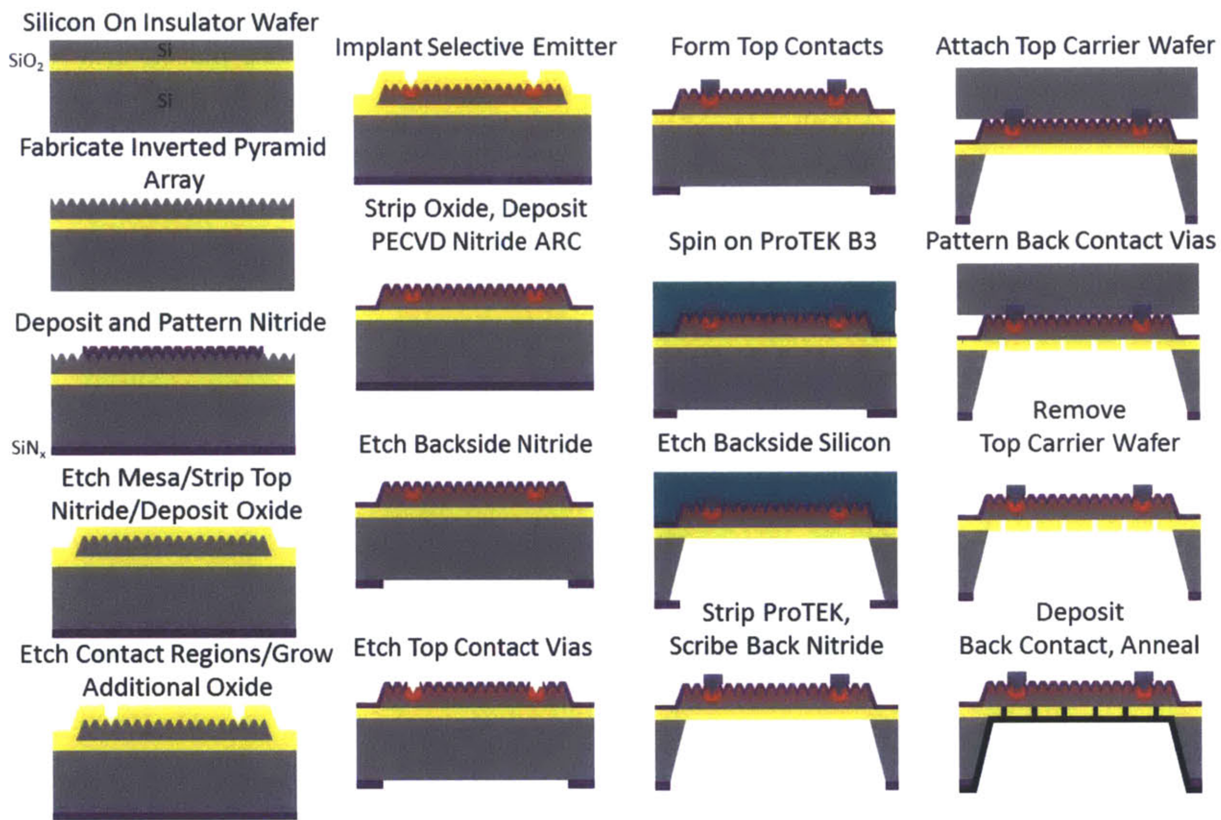


Figure 22 | Ultrathin crystalline silicon solar cell process flow schematic.

4.1 Sequence 1: Inverted Pyramid Photolithography

Preceding sequence: Begins with virgin wafers
Sequence steps:

i. RCA clean
ii. LPCVD silicon nitride deposition (280 nm)
iii. Nitride roughening etch
iv. HF dip
v. Lithography for inverted pyramid mask

Following sequence: Inverted pyramid etches and cleans, beginning with a dry nitride etch

The first sequence in the process – the formation of the inverted nanopyramid surface light-trapping structure – is also one of the most challenging. The primary difficulty is adhesion of the photoresist during development of the lithography step, which we took great pains to address but only partially understand.

The first step in the sequence is a standard RCA clean, required for newly acquired wafers before entering high-temperature deposition or diffusion equipment. The wafers are first cleaned in 5:1:1 H_2O:NH_4OH (29% concentration by weight): H_2O_2 (30% concentration by weight) for 10 minutes at 80 °C to remove particles and organic contaminants, then placed in dilute HF (50:1) for 60 seconds to remove any native oxide and embedded contaminants, followed by cleaning in 6:1:1 H_2O:HCl (36.5-38% concentration by weight): H_2O_2 (30% concentration by weight) for 15 minutes at 80 °C to strip away metal contaminants.

Immediately following RCA cleaning and spin-drying, the wafers are placed in a low-pressure chemical vapor deposition (LPCVD) chamber to deposit a low-stress, silicon-rich, 50-nm-thick silicon nitride film on both sides of the wafer. The film is grown from ammonia (NH_3) and dichlorosilane (H_2SiCl_2) precursor gases at 250 mT and 775 °C. This flavor of nitride is resistant to etching by potassium hydroxide (KOH) and serves as the hard mask during the KOH pyramid etch.

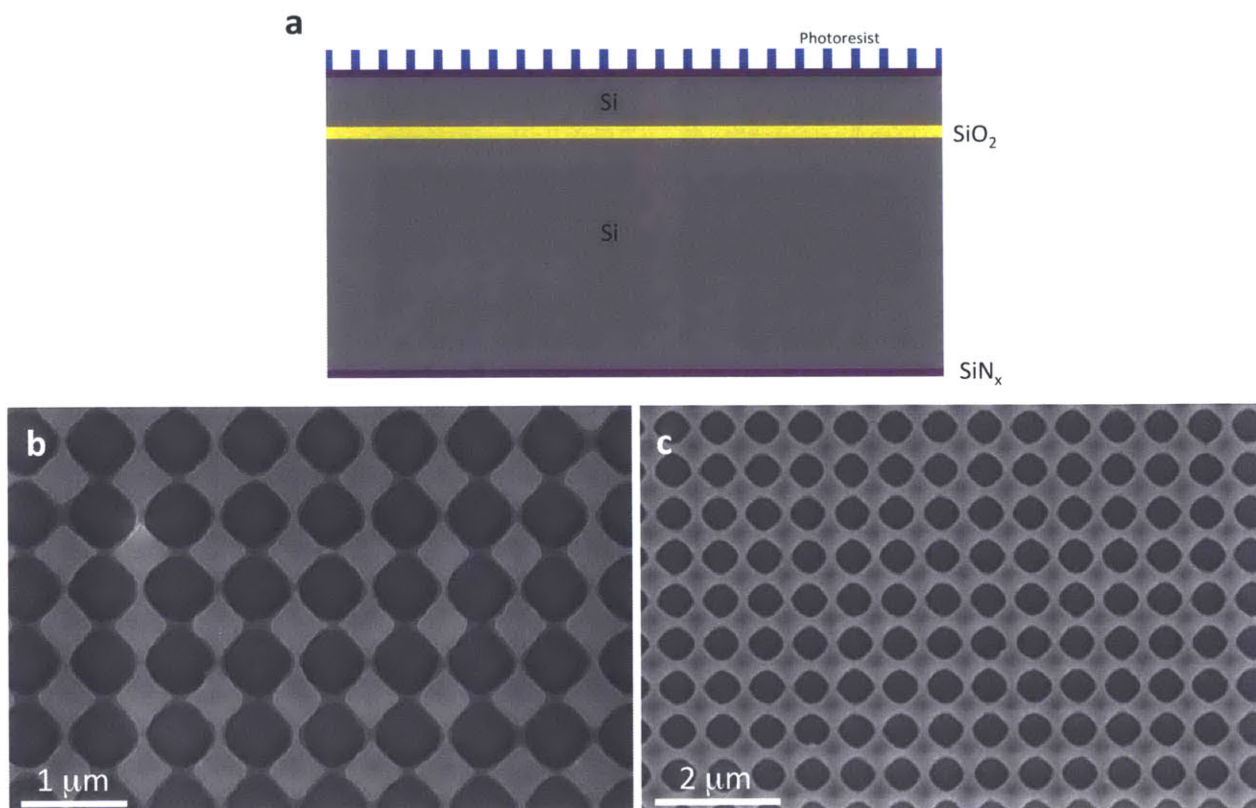


Figure 23 | Photoresist patterning for inverted nanopyramid lithography. a, Cross-section schematic of a single die at the conclusion of Sequence 1 showing the hole pattern in photoresist on the top surface. **b, c,** SEM images of two-dimensional hole arrays in (**b**) underexposed and (**c**) properly exposed photoresist.

The final step in this sequence is the lithography step itself. Futurrex NR7-250P negative tone resist is spun on the device side of the SOI wafer to a thickness of 250-300 nm and oven-baked at 120 °C for 30 minutes. Next, the photoresist is exposed using a Nikon i-line projection lithography stepper. The exposure is done in two steps through a 1D grating mask with 1.5 μm chrome lines separated by 2 μm gaps, which after a 5X reduction by the stepper optics yields 300 nm lines on a 700 nm pitch. The photoresist is first exposed for 350-400 ms before the mask is rotated 90 degrees and the wafer exposed again for an identical amount of time. After baking at 105 °C for 30 minutes and developing in 3:1 Futurrex RD6:H_2O for ~6-10 seconds, a two-dimensional array of holes on a 700 nm pitch emerges in the photoresist, as shown in Fig. 23. An example of an underexposed sample is also presented. The requisite exposure time has been found to vary between runs, as does the development time, and should be trialed before doing a large run.

The photograph in Fig. A3 illustrates typical results from a successful photolithography run, highlighting the iridescent pattern produced by the photonic crystal made of photoresist. After producing the two-dimensional array pattern in photoresist and drying the wafer, the next step is to etch the inverted pyramid features.

4.2 Sequence 2: Inverted Pyramid Surface Texture

Preceding sequence: Inverted pyramid photolithography
Sequence steps:

i. Top nitride RIE etch
ii. Photoresist removal
iii. Anisotropic KOH etch of silicon
iv. Double piranha clean
v. Nitride removal

Following sequence: Mesa isolation structure formation, beginning with an RCA clean

In this sequence, the photoresist patterned in the preceding step is transformed through a series of etches into a three-dimensional surface pattern consisting of inverted pyramids on a 700 nm pitch. In the first step, a two-dimensional array of holes is etched into the top nitride using the existing photoresist pattern as a mask and a carbon tetrafluoride/oxygen (CF_4/O_2) chemistry in a magnetically-enhanced reactive ion etching (MERIE) tool (AME-5000 in MTL-ICL) for 25 seconds. CF_4/O_2 is more selective to silicon than sulfur hexafluoride/oxygen (SF_6/O_2), which is crucial because significant overetching of the silicon will cause the pattern to collapse during the subsequent KOH etch. The nitride etch is followed by a short ash in oxygen plasma to remove the photoresist, leaving a two-dimensional array of holes etched in nitride, as shown in Fig. 24a.

The next step in the process is to etch inverted pyramids into the silicon using a potassium hydroxide wet etch. Prior to immersion in KOH, the wafer is placed momentarily in a 20:1 HF solution to strip any native oxide, which can lead to non-uniform etching outcomes if not first removed. After rinsing in DI water, the nitride-masked silicon wafer is etched in 20% KOH at 80 °C for 4-8 minutes (depending on the diameter of the holes following lithography) (Fig. 24b).

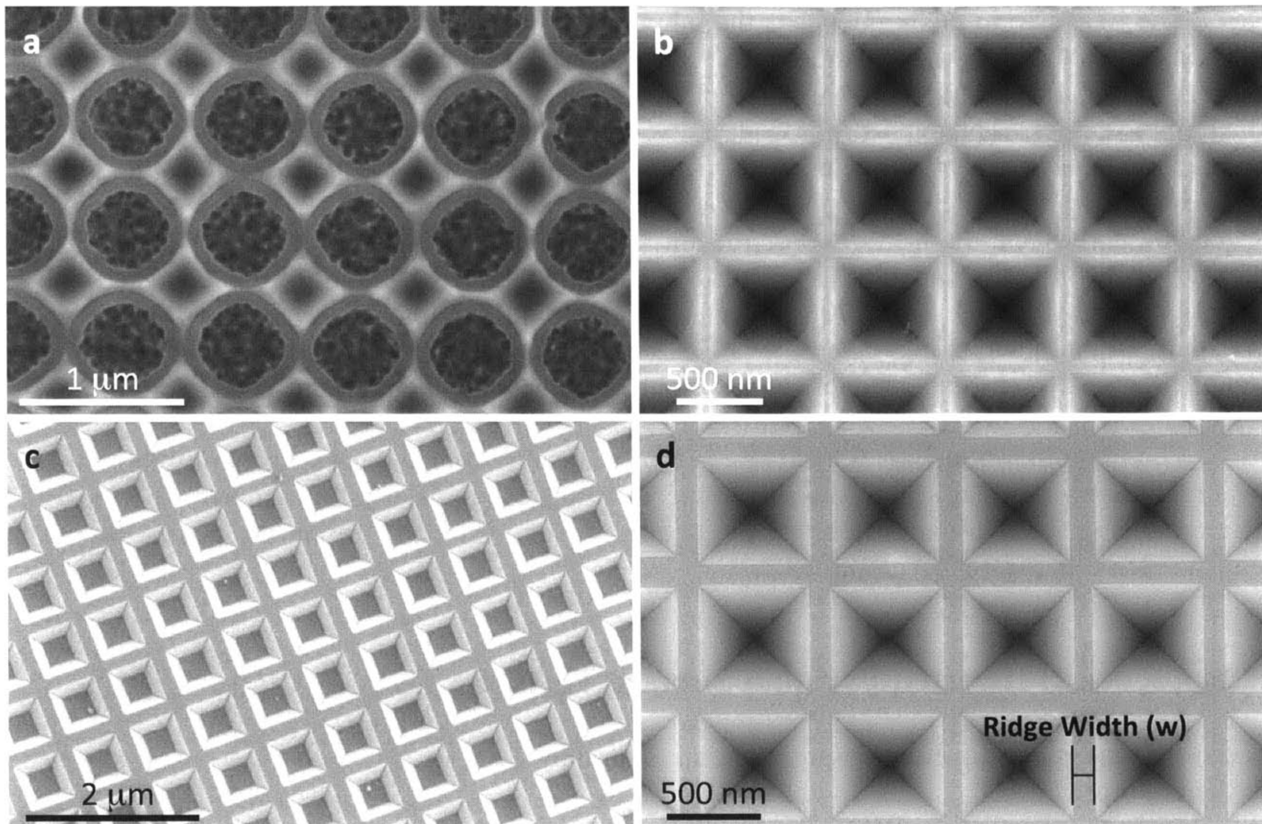


Figure 24 | Inverted nanopyramid formation. **a,** SEM image showing the nitride hard mask with holes etched through into the underlying silicon (areas with roughened appearance). **b,** Sample image following KOH etching of inverted pyramids with the nitride mask still in place; this particular sample was etched in 80 °C KOH for six minutes. **c,** A sample partially etched in KOH to demonstrate the evolution of the pyramid shape. **d,** Inverted nanopyramids with particularly large ridges.

The formation of sub-micron inverted pyramids is a particularly sensitive and difficult processing step to control. Potassium hydroxide etches silicon anisotropically, highly selective to (111) crystallographic planes. When silicon masked by nitride with circular openings is placed in KOH, the solution rapidly etches a pyramid shape into the silicon with the walls defined by (111) planes (Fig. 24c). Each newly formed pyramid is separated by a "ridge" (Fig. 24d) from adjacent pyramids, which is protected by the nitride mask. With increasing etch time the ridge width slowly shrinks. The author found the ridge width to etch (shrink in width) at a rate of 20-30 nm/min in 20% KOH at 80 °C. The etch rate can be estimated by surveying the distance between the edge of a given nitride hole and the ridge under SEM, given the etch time and adjusting for the ~1 minute required to form the initial pyramid (Fig. 24b).

The optical performance of the inverted pyramid structure is maximized – because surface reflection is minimized – when the ridge width separating pyramids is minimized. However, during the KOH pyramid etching process, if the ridge width shrinks to zero, a fresh (100) plane will be exposed under the nitride mask and the ridge will quickly collapse as adjacent pyramids merge (Fig. 25a). When this happens on a large scale, the surface patterning disappears (Fig. 25b). For this reason it is important to error on the side of caution when timing

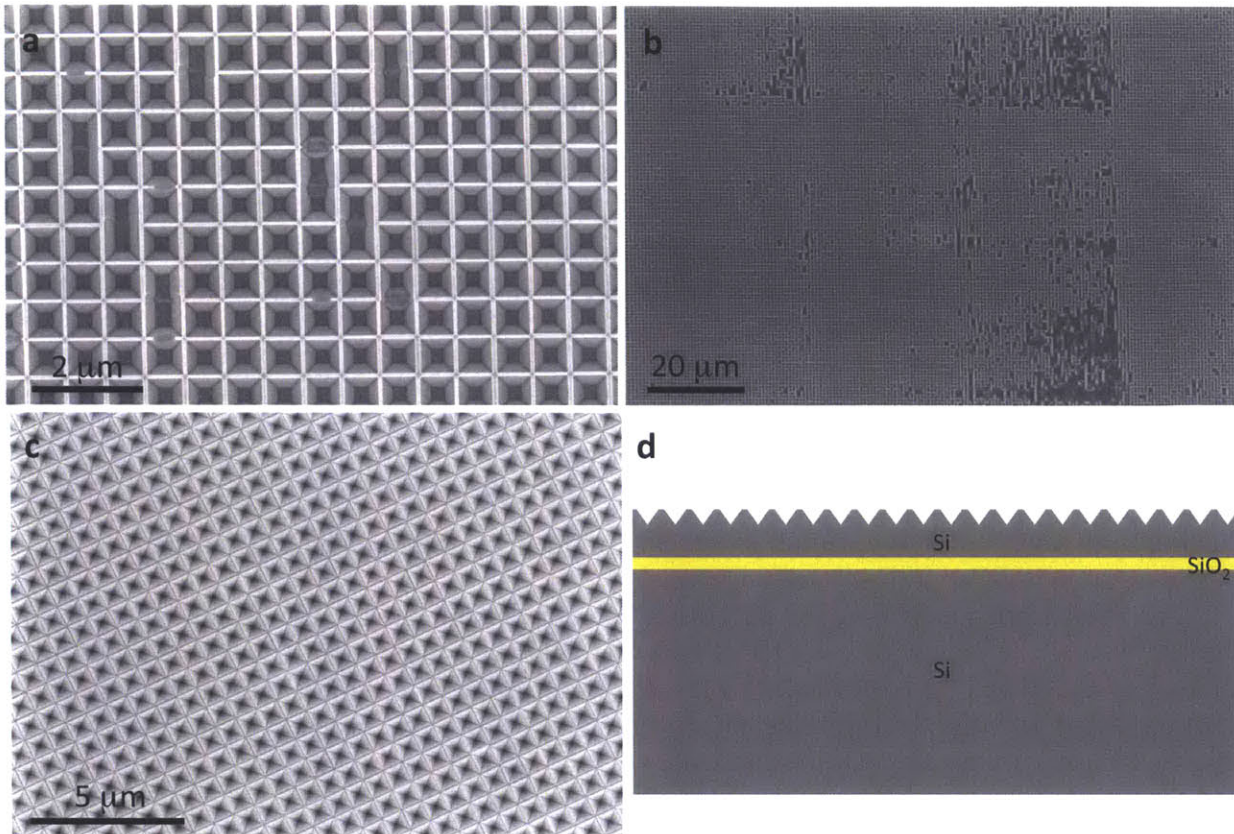


Figure 25 | Defective inverted pyramids and completed inverted pyramid textures. a, SEM image of a silicon substrate partially etched with inverted pyramids, capturing several pyramids in mid-collapse. **b,** Large-scale example of pattern collapse from merging pyramids. **c,** Completed, nearly ideal inverted pyramid surface texturing with ridges thinner than 50 nm. **d,** Cross-section schematic at the conclusion of Sequence 2 with the photonic crystal now etched into the silicon device layer.

the KOH etch. Unfortunately, the lithography process itself has tremendous variability, with hole sizes varying from run to run, from wafer to wafer within a run, and even within a die by as much as 50 nm. The variability mandates that samples be inspected by SEM or AFM prior to etching to estimate appropriate KOH etch times. In the author's experience, minimum ridge widths on the order of 30-50 nm are the best achievable without excessive risk of destroying the patterning.

To guard against potential potassium contamination in the cleanroom, the samples must first undergo a piranha clean (3:1 H_2SO_4:H_2O_2 for 10 minutes), 50:1 dilute HF dip for 15 seconds, and second piranha clean before processing in the cleanroom can continue. Finally, the nitride mask is stripped in boiling phosphoric acid at 165 °C (14 min. etch). The resulting silicon surface is textured with a two dimensional inverted nanopyramid photonic crystal (Fig. 25c,d) that is strongly iridescent (Fig. 29c).

4.3 Sequence 3: Mesa Isolation Structure

Preceding sequence: Inverted pyramid surface texture formation, ending with a hot phosphoric acid etch

Sequence steps:

i. RCA clean
ii. LPCVD nitride deposition (280 nm)
iii. PECVD oxide deposition (200 nm), backside of wafer
iv. Mesa photolithography
v. Top nitride etch
vi. Photoresist removal
vii. KOH mesa etch
viii. Double piranha clean
ix. Nitride strip

Following sequence: Selective emitter oxide patterning, beginning with an RCA clean

The third sequence isolates the photovoltaic cell by etching away adjacent silicon to form a mesa structure. It begins with an RCA clean as described in Section 4.1, followed by the deposition of a 280 nm silicon-rich LPCVD silicon nitride film on both sides of the wafer to serve as a mask during the KOH mesa etch. After nitride deposition, the samples are coated with a 200 nm PECVD oxide film on the backside of the wafer. This oxide film will be used to protect the nitride film on the back of the wafer during step ix.

Photolithography using thick resist defines the portions of the wafer that will eventually hold the one square centimeter solar cell dies. HMDS is evaporated onto the wafer to enhance resist adhesion, followed by spinning on AZP4620 thick positive resist to ~10 μm (1500 RPM spin speed). The resist is oven-baked at 95 °C for 60 minutes, followed by exposure using an i-line mask aligner (20 seconds in four increments of five seconds on/five seconds off using a 10 mW cm^{-2} lamp). Development is accomplished in AZP 405 developer solution for 210 seconds, followed by a hard bake at 95 °C for 30 minutes. The nanopyramid surface texturing, combined

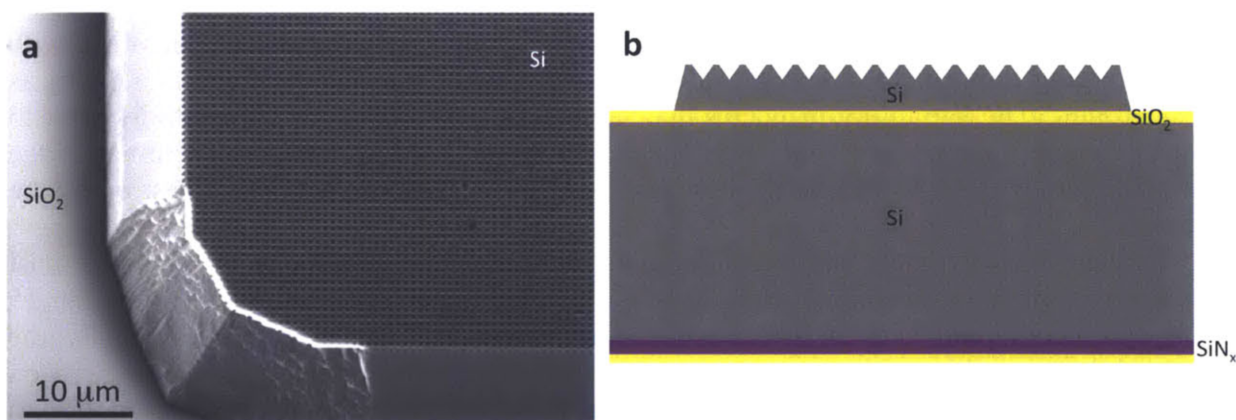


Figure 26 | Completed mesa isolation structure. a, SEM image of the corner of a die showing the surrounding silicon now removed. The roughened surface at the corner is the result of competing etches between the two crystal planes of the intersecting sidewalls. **b,** Cross-section schematic at the conclusion of Sequence 3 with the area of each solar cell now precisely defined by the mesa etch.

with the step height of the die resulting from the inverted pyramid KOH etch step in Sequence 2, makes it challenging to coat the wafer without defects. NOTE: ANY DEFECTS IN THE PHOTORESIST COATING A DIE WILL BE TRANSFERRED THROUGH THE ENTIRETY OF THE SILICON DEVICE LAYER, RESULTING IN MECHANICAL FAILURE OF THE DEVICE AFTER SEQUENCE 10. Extraordinary care must be taken to ensure defect-free photoresist coating of the solar cell dies to limit yield loss.

Following lithography – which results in square photoresist islands 1.0002 cm on a side – the unmasked nitride is MERIE-etched with a CF_4/O_2 chemistry. The remaining photoresist is cleaned in oxygen plasma. A mesa structure is subsequently formed by etching away the exposed silicon of the device layer in a solution of 20% KOH at 80 °C (silicon etch rate ~ 1.25 $\mu m\ min^{-1}$). The anisotropic KOH silicon etch leaves a sidewall angled at 54.7° relative to the surface horizontal, important for making contact to the device after metallization.

Sequence 3 is completed by a double piranha clean (see Sequence 2) as specified by MTL protocol and a hot phosphoric acid etch at 165 °C for 80 minutes to remove the remaining top nitride, leaving the structure shown in Fig. 26. Note that the backside nitride is protected during this step by PECVD oxide deposited during step iii of this sequence.

4.4 Sequence 4: Selective Emitter Preparation

Preceding sequence: Mesa isolation structure formation, ending with a hot phosphoric acid etch
Sequence steps:

i. RCA clean
ii. PECVD oxide deposition (100 nm)
iii. Selective contact pattern photolithography
iv. Top oxide selective contact patterning etch
v. Piranha clean
vi. RCA clean
vii. Implant oxide growth

Following sequence: Ion implantation

The purpose of Sequence 4 is to pattern oxide on the top surface of the device layer in preparation for ion implantation and formation of the selective emitter. At its conclusion, a 100 nm silicon dioxide film will cover the die surface except for 20-μm-wide strips that are 30 nm thick in the future location of the top metal contacts.

To begin this sequence, the samples are RCA cleaned (as described in Section 4.1) before depositing 100 nm silicon dioxide on the top surface via PECVD. Next, a basic lithography process is carried out using positive photoresist to pattern thin strips in the newly deposited oxide. HMDS is evaporated onto the wafer to enhance adhesion, followed by spinning on SPR700-1.0 positive resist to ~1.4 μm (2000 RPM spin speed). The resist is oven-baked at 95 °C for 30 minutes, followed by exposure using an i-line mask aligner (3 seconds with a 10 $mW\ cm^{-2}$ lamp). Development is accomplished in MF CD-26 developer solution for 75 seconds, followed by a hard bake at 120 °C for 30 minutes. The photoresist pattern is then etched into the oxide with a buffered oxide etch (BOE), after which a piranha clean removes the photoresist film.

The next step in the process of forming the oxide for selective emitter ion implantation is another RCA clean, although modified from those described earlier by using a 20-second dilute

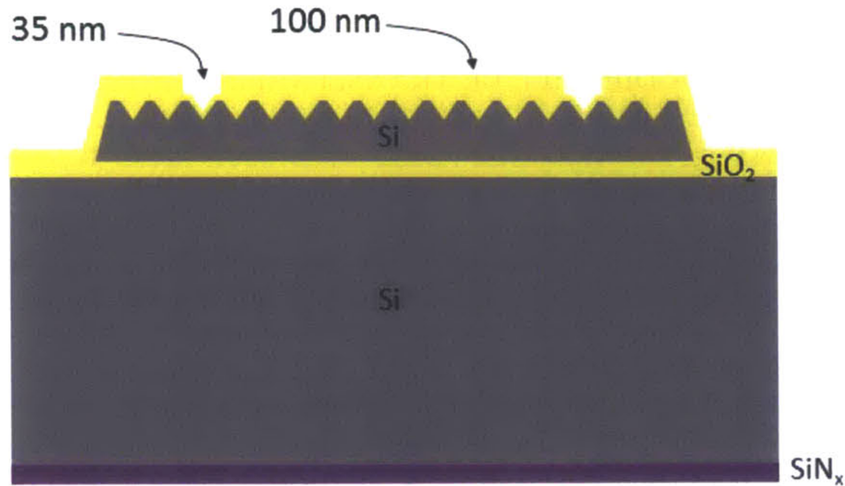


Figure 27 | Schematic of the device structure after Sequence 4 with patterned oxide for selective emitter formation.

(50:1) HF dip in lieu of the normal 60 seconds. After the RCA clean and HF dip, the remaining oxide is thinned to about 80 nm. Finally, the wafer is oxidized at 1000 °C for 24 minutes in a dry O_2 atmosphere, resulting in an oxide thickness of approximately 34 nm in the contact regions and 100 nm everywhere else on the device (Fig. 27). Note that these thicknesses are measured on planar reference surfaces. The exposed (111) planes of the inverted pyramids will have a thicker film by a factor of 1.54.

4.5 Sequence 5: PN-Junction Implantation and Annealing

Preceding sequence: Selective emitter oxide patterning, ending with thermal oxide growth
Sequence steps:

i. Ion implantation
ii. Double piranha clean
iii. RCA clean
iv. Dopant diffusion and annealing

Following sequence: ARC deposition, beginning with an oxide strip

In Sequence 5, the solar cell emitter and selective top contact is formed through ion implantation and diffusion. As prescribed in Section 3.3.2.4, the wafers are implanted in a two-step process at an outside vendor (Innovion Corp., San Jose, CA): first, a low-dose phosphorus implant is deposited at sufficiently high energy to penetrate the masking oxide over the entire device to dope the emitter region, followed by a high-dose arsenic implant at a lower energy that provides a heavy n^{++} doping for the top contact regions covered by thin oxide.

After returning from ion implantation, the wafers must first be cleaned twice in piranha with an HF dip interspersed, as described in Section 4.1, before they are suited for further processing in the cleanroom. An RCA clean, modified with a 15 second dilute HF dip as opposed to the standard 60 seconds so as not to remove the entire oxide film (which once

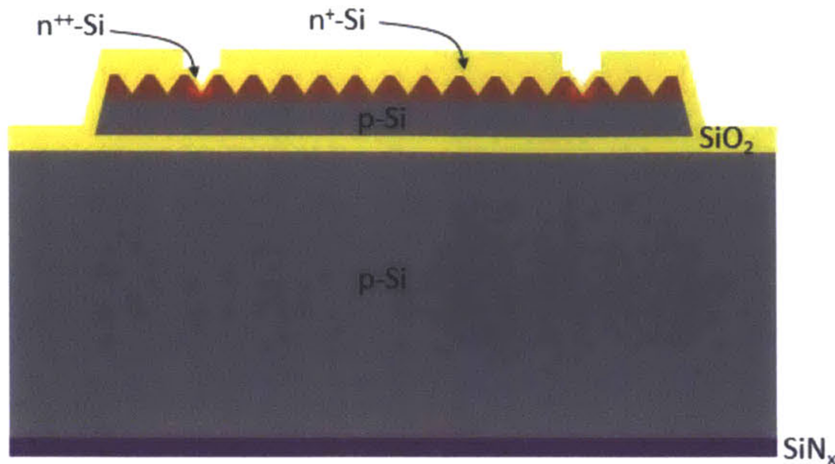


Figure 28 | Device schematic following Sequence 5 depicting the formation of the selective emitter.

damaged by ion implantation etches extremely fast in hydrofluoric acid), is necessary to remove contaminants from the wafer surface prior to diffusion.

In the final step of the sequence, the wafer is annealed at 1000 °C for 60 minutes (Fig. 28). This diffusion step serves two important purposes: 1) it heals damage incurred by the silicon crystal during the implantation process, simultaneously allowing the dopant atoms to migrate to their appropriate, electrically-active positions in the silicon lattice, and 2) it motivates the diffusion of dopant atoms to form a pn junction at a controlled depth. The prescribed junction depth in these devices is 0.5 μm, but the actual depth was not characterized and would be variable on a textured pyramidal surface. The formation of the pn-junction is a critical step in solar cell fabrication, with a wide range of variables (e.g., annealing time and temperature, dopant concentration, cleanliness) that influence the quality of the resulting device.

4.6 Sequence 6: Nitride ARC Deposition

Preceding sequence: Junction implantation and diffusion
Sequence steps:

i. Implant oxide strip
ii. RCA clean
iii. Nitride ARC deposition

Following sequence: Top contact via patterning, beginning with photolithography

During Sequence 6, the top oxide is removed and replaced by a PECVD silicon nitride that provides both excellent passivation as well as optical index matching for low surface reflectivity.

The top oxide – heavily contaminated with n-type dopants and damaged during implantation – is stripped using a buffered oxide etch. This step also removes the oxide from the back surface of the device that served to protect the LPCVD nitride deposited in Sequence 2. Following the protocol given in Section 4.1, an RCA clean prepares the wafer for the final

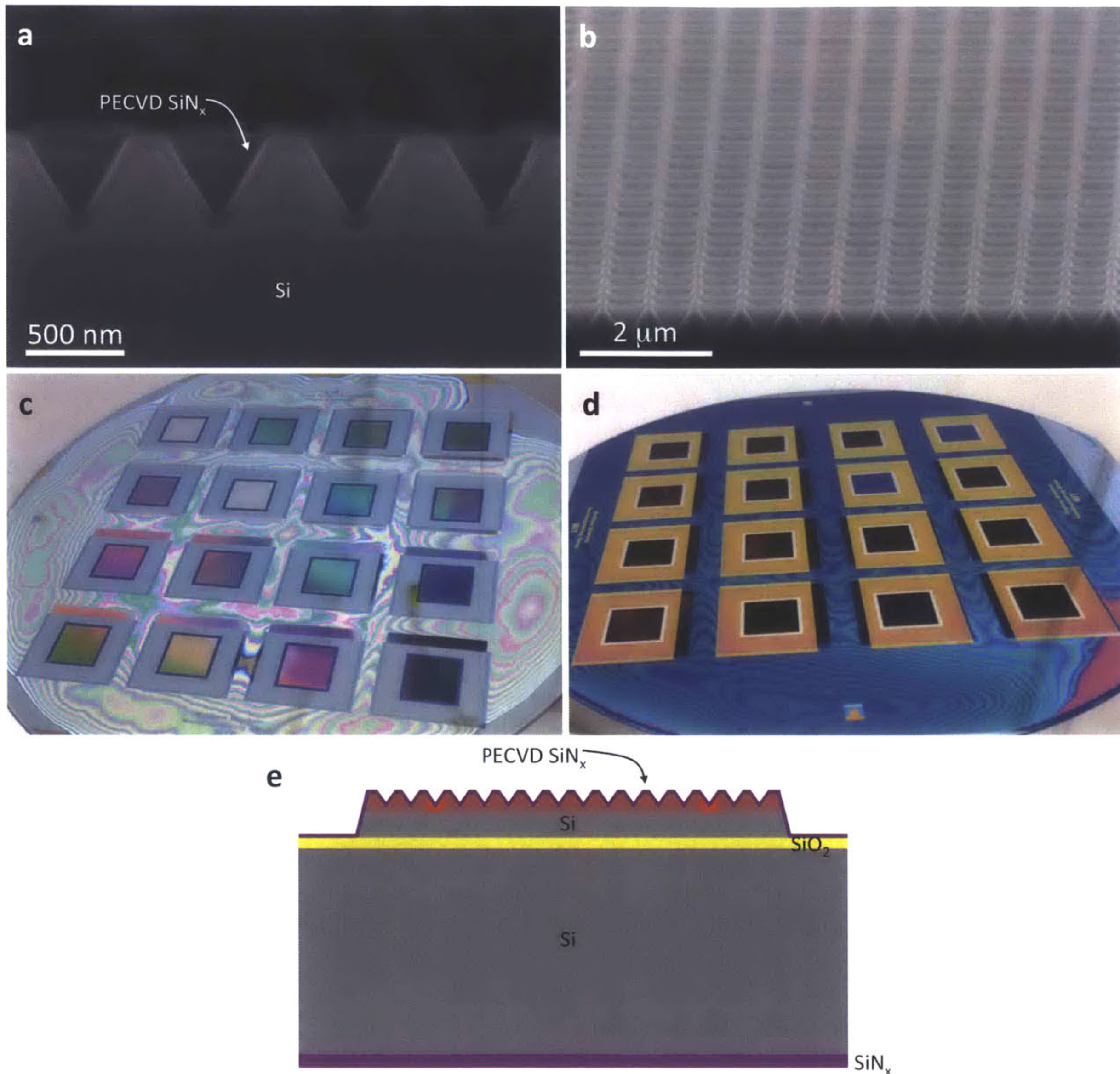


Figure 29 | Deposition of PECVD nitride anti-reflection coating. a,b, SEM cross-sections of the textured silicon surface with the nitride ARC clearly visible. **c,d,** Photographs of the experimental wafer before (**c**) and after coating with silicon nitride (**d**). **e,** Cross-section schematic of the device with the ion implant oxide mask replaced with a 100 nm silicon nitride ARC.

sequence step, which is the deposition of a PECVD silicon nitride ARC coating. The passivation characteristics of silicon nitride are heavily dependent on deposition parameters, particularly temperature but also film composition. The PECVD nitride used for the ARC coating was deposited at 400 °C and 4.7 Torr, an RF power of 875 W, and precursor gases: silane (SiH_4) = 300 sccm, ammonia (NH_3) = 120 sccm, and nitrogen (N_2) = 4000 sccm. The resulting film has a refractive index of n = 1.9 (λ = 600 nm) and measured surface recombination rates of 5-10 cm s^{-1} on p-type silicon. The nitride film thickness is measured on a planar reference as 100 nm (Fig. 29). After deposition the surface appears very dark with some subtle iridescence from the photonic crystal.

4.7 Sequence 7: Top Contact Via Lithography and Etch

Preceding sequence: PECVD silicon nitride surface ARC deposition
Sequence steps:

i. Contact via lithography
ii. Contact via etch
iii. Photoresist removal

Following sequence: Backside window etch, beginning with photolithography

During Sequence 7, thin 10-μm-wide openings are patterned in the top ARC nitride – deposited during the preceding sequence – aligned with the n^{++} regions of the emitter. By this stage in the process, the wafer surface has very sharp topographical features, particularly the 10 μm step height of the mesas. In order to properly pattern the surface, the author recommends using a double coat of thick resist for photolithography to best mask features that need to be protected. Following a similar photolithography process as described in Sequence 3, HMDS is evaporated onto the wafer to enhance adhesion, followed by spinning on AZP4620 positive thick resist to ~10 μm (1500 RPM spin speed). The resist is baked at 95 °C for 30 minutes in an oven, coated a second time with AZP4620 to increase the photoresist thickness to ~20 μm, and then baked again at 95 °C for 60 minutes. Next, the photoresist is exposed using an i-line mask aligner (105 seconds in seven increments of fifteen seconds on/fifteen seconds off using a 10 mW cm^{-2} lamp). Development is accomplished in AZP 405 developer solution for 8 minutes, followed by a hard bake at 95 °C for 30 minutes.

The exposed nitride strips are then etched using MERIE and a CF_4/O_2 chemistry. The combination of etch chemistry and tool configuration yielded a uniform etch on the patterned surface and high selectivity to silicon. In contrast, a sulfur hexafluoride (SF_6) and oxygen (O_2) plasma etch in a parallel-plate RIE tool removes material in a planarizing fashion, leaving nitride inside each of the individual pyramids and limiting the surface area in contact with metal (whether that is advantageous or disadvantageous has not been determined). The latter etch is not selective to silicon.

Finally, the remaining photoresist is removed using oxygen plasma. At the conclusion of this sequence, the individual solar cells now have contact via openings etched in the top nitride ARC (Fig. 30).

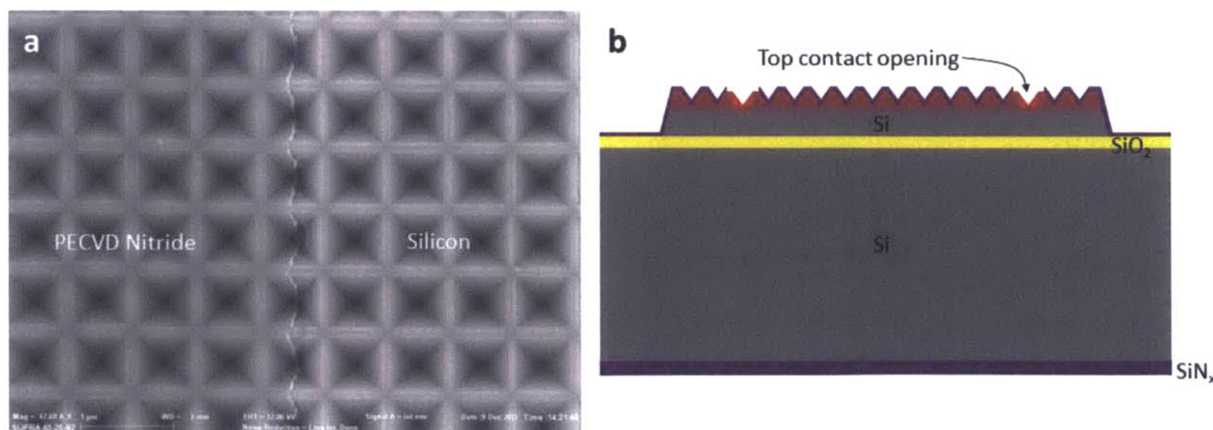


Figure 30 | Contact openings in silicon nitride. a, Top view of a device after opening contact vias in the silicon nitride. **b,** Device cross-section at the conclusion of Sequence 7.

4.8 Sequence 8: Backside Window Etch

Preceding sequence: Top contact via lithography and etch, ending with photoresist ash
Sequence steps:

i. Backside window lithography
ii. Backside window nitride etch
iii. Piranha clean

Following sequence: Top contact formation, beginning with photolithography

Sequence 8 is similar to Sequence 7, except that instead of patterning the front nitride, the back nitride is patterned with square openings that are aligned with the dies on front. The sequence begins with a basic lithography process using SPR700-1.0 positive resist (as explained earlier in Sequence 4) to pattern photoresist with squares that are 1.056 centimeters on a side. Next, the unmasked silicon nitride on the back surface of the wafer is etched in a parallel-plate RIE tool with a SF_6/O_2 chemistry. The wafer is then cleaned in piranha to strip off the photoresist and other organic and metallic contaminants in preparation for top contact metallization (Fig. 31).

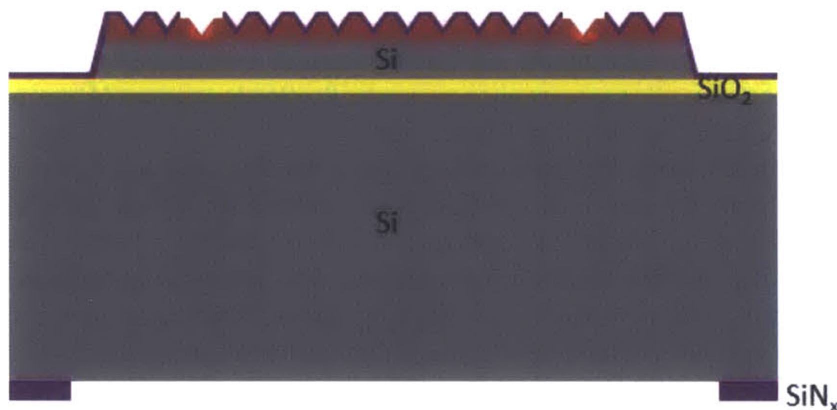


Figure 31 | Device cross-section after Sequence 8 showing the back window patterned in nitride in preparation for membrane formation.

4.9 Sequence 9: Top Contact Metallization

Preceding sequence: Backside window etch, ending with piranha clean
Sequence steps:

i. Lithography for top contact metal lift-off
ii. BOE silicon clean
iii. Top contact metals evaporation
iv. Lift-off

Following sequence: Backside window KOH etch, beginning with ProTEK coating

In Sequence 9, the top metal contacts are fabricated using lift-off lithography. The first step is to pattern the wafer using a negative resist that is suitable for lift-off, in this case Futurrex NR9-1000PY. Ideally, one would use a thicker lift-off resist – such as NR9-8000PY – to coat

the significant topographical features on the wafer, but alternatives were not available in the cleanroom facility at the time of fabrication. The resist was spun on to the samples at a spin speed of 1500RPM, giving a coating thicker than the standard 1 μm. The wafers were then pre-baked on a hotplate at 150 °C for 65 seconds, exposed for 39 seconds using a 10 mW cm^{-2} i-line mask aligner, baked at 100 °C for another 65 seconds on a hotplate, and then developed in full-concentration Futurrex RD6 for 10 seconds.

Prior to evaporating the top contact metals, it is essential to clean the silicon contact regions and remove any native oxide as well as contaminants that may have adsorbed into the oxide. A quick 10 second buffered oxide etch or dip in 10:1 H_2O:HF satisfies this requirement, without which higher contact resistance can be expected.

Immediately after cleaning the silicon contact regions and spin-drying the samples, they are placed in an e-beam metal evaporation tool to deposit the contact materials with thicknesses specified in Section 3.4.4.2: 40 nm titanium, 40 nm palladium, and 920 nm silver (in order from bottom to top). After removing the samples from the e-beam tool, they are placed overnight in acetone to remove unwanted metal through lift-off (Fig. 32).

Given the sharp topographical features on each wafer, manual assistance using tweezers is often needed to remove metal segments. (Using a thicker lift-off resist would likely reduce the need for manual lift-off.) Note that it is very important to remove all metal shards and remnants

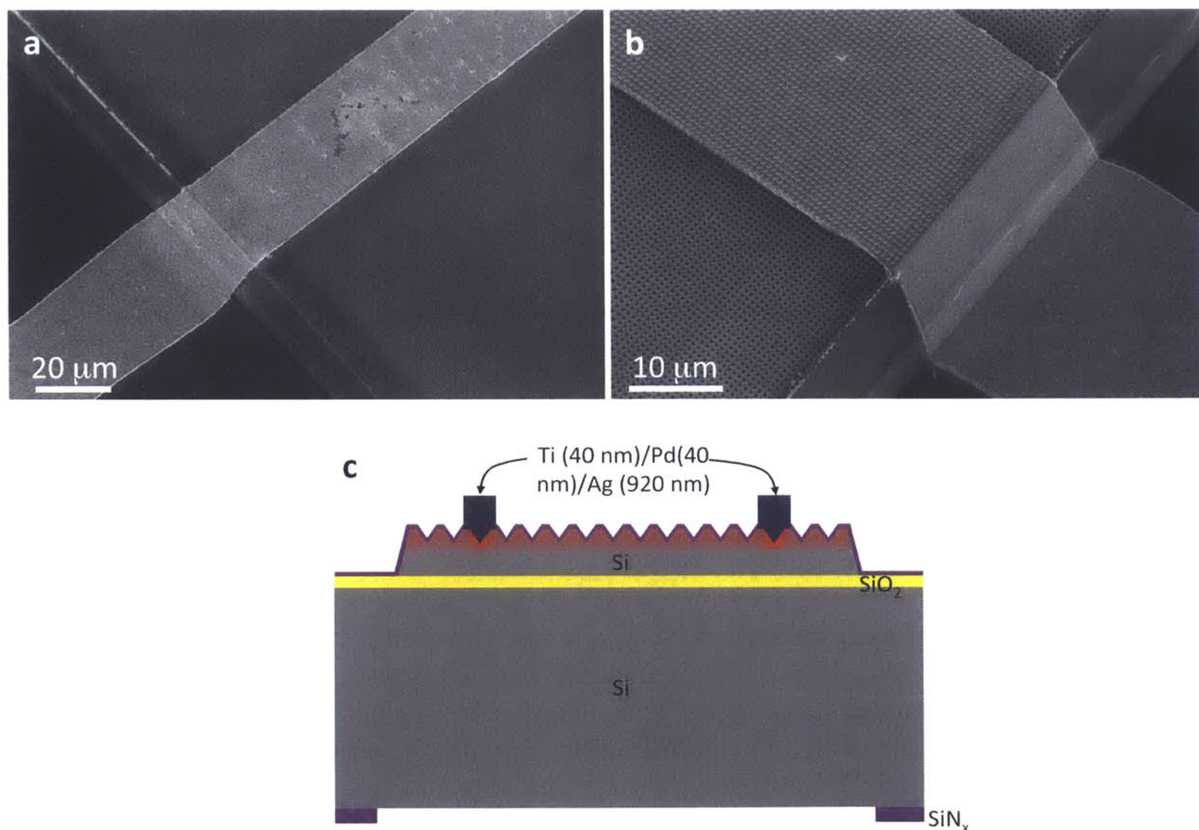


Figure 32 | Top contact metal deposition and lift-off. a, b, SEM views of metal contact fingers. The seven contact fingers per device are 30 μm wide and run down the sloped sidewalls at the edge of each device, connecting to bus bars and probe pads that are located off of the membrane area. **c,** Cross-section schematic of a device after deposition of Ti/Pd/Ag contact fingers.

that are not part of the solar cell contacts. In the author's experience, metal shards that project in the vertical direction disturb the integrity of the polymer film that protects the devices during the membrane etch (as described in the following Sequence 10), leading to a high probability that a given device will be damaged by KOH.

Following the acetone soak, the samples are cleaned in fresh acetone, then methanol, IPA, and finally DI water. The cleaned and metallized wafers are spun dry to complete Sequence 9.

4.10 Sequence 10: Membrane Formation

Preceding sequence: Top contact metal lift-off, ending with three-solvent clean and spin-drying
Sequence steps:

i. Coat with ProTEK
ii. Etch backside silicon KOH membrane
iii. Strip ProTEK

Following sequence: Back oxide patterning, beginning with mounting to a carrier wafer

In this critical sequence, the top surface of the wafer is protected with an alkaline-resistant polymer and the silicon handle layer is then etched through using KOH, forming a membrane and opening access to the rear of the solar cells. The 54.7°-angled sidewall remaining after KOH etching permits electrical contact to be made to the back of the solar cell through metal deposited over the entire back of the wafer.

In the first step of this sequence, the top surfaces of the samples are coated with a double layer of ProTEK B3 (Brewer Science). ProTEK B3 is a liquid polymer that, when cured, forms a hardened film resistant to attack by alkaline etchants. It is often used in MEMS manufacturing to protect delicate circuitry during backside processing. In the case of these ultrathin membrane solar cells, the ProTEK serves to encapsulate the top metal contacts – deposited in the preceding Sequence 9 – as well as the nitride ARC during the long backside KOH etch through the silicon handle wafer.

To prepare the ProTEK film, a layer of ProTEK B3 Primer is first spun on at 1250 RPM for 60 seconds and baked on a hotplate at 205 °C for 60 seconds. Next, the first coat of ProTEK B3 is spun on at 1250RPM as well, followed by a 130 °C hotplate bake for 120 seconds. A second coat of ProTEK is applied at the same spin speed and baking parameters. A final hard bake at 205 °C for 60 seconds completes the curing process, resulting in a film nominally 16 μm thick.

Proper coating of the device side of the SOI wafer with ProTEK is essential to limit yield loss. ProTEK's failure modes during alkaline etch are of two types: 1) peeling of the ProTEK from the top surface, beginning at the edges of the wafer, and 2) pinhole defects that allow KOH access to the wafer surface. The first failure mode, peeling, is intrinsic to the KOH/ProTEK system. In normal conditions, it happens at a very slow rate and is confined to the outer rim of the wafer. However, the adhesion between ProTEK and silicon nitride is not as strong as between ProTEK and oxide in the author's experience, and the peeling rate tends to be somewhat higher for nitride-coated surfaces. Additionally, ProTEK does not adhere to silver, so large areas of metallization on the edge of the device wafer should be avoided to prevent significant ProTEK peeling. Should the ProTEK peel away from the edge of the wafer enough to expose a die, the solar cell will be rapidly attacked by KOH – first the titanium adhesion layer followed by the

underlying silicon – resulting in the loss of the device. One of the most significant factors governing the magnitude of peeling is the age of the ProTEK solution. ProTEK containers significantly past expiration should not be used.

The second common failure mode occurs when KOH penetrates the ProTEK film through defects to access the underlying wafer. Once in contact with the surface, the KOH begins to react and evolve gaseous byproducts, ultimately forming a bubble in the ProTEK that accelerates peeling and increases the area susceptible to KOH attack. The most common source of defects in the ProTEK film are metal slivers remaining from the lift-off process of Sequence 9 that project outward from the wafer surface. In some cases, it can be worth the effort to coat the wafer with ProTEK, manually remove the film with embedded metal shards, and then recoat it to minimize defects.

The ProTEK-coated wafer is placed in a 20% solution of potassium hydroxide heated to 80 °C to etch windows in the silicon handle wafer. With the wafers in a vertical orientation for the fastest etch rate, the 500 μm handle wafer can be etched through in approximately 6 hours and 50 minutes. The wafers are then thoroughly, but gently, rinsed in DI water and carefully dried.

To remove the polymer film, the samples are immersed in acetone for ten minutes. It is at this step, when the suspended membranes lose the structural support provided by ProTEK, that the bulk of yield loss occurs. Individual dies with structural deficiencies – such as defects in the silicon device layer formed when etching the inverted pyramids (Sequence 2) or the mesa structure (Sequence 3) with KOH – typically tear out of the wafer during this step. Aside from handling the wafer gently, the best way to minimize failures at this step is to minimize defects transferred to the silicon during Sequences 2 and 3. After the ProTEK is removed, the samples are cleaned in fresh acetone, then methanol and IPA for five minutes each (Fig. 33).

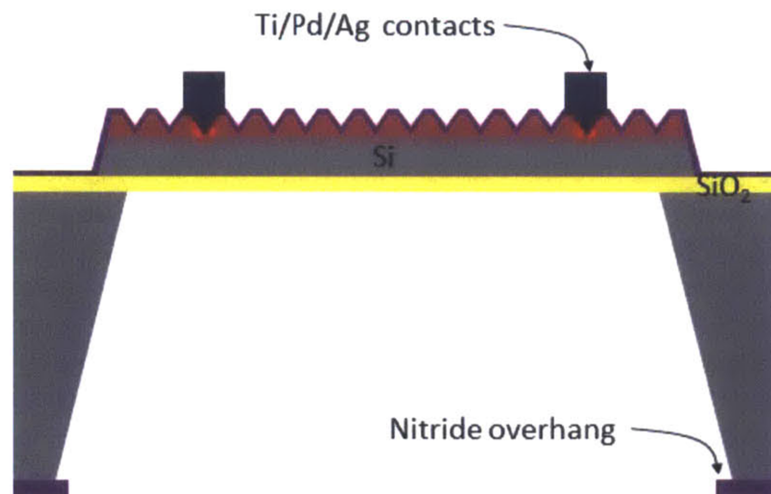


Figure 33 | Device structure after etching the silicon handle to form a membrane. The nitride lip forms as KOH gradually etches back the (111)-oriented silicon sidewalls.

4.11 Sequence 11: Pattern Back Oxide

Preceding sequence: Backside window etch, ending with ProTEK removal using a three-solvent clean

Sequence steps:

i. Coat with HMDS
ii. Bond carrier wafer
iii. Back oxide lithography
iv. Scribe nitride overhangs on back windows
v. Etch back oxide
vi. Remove carrier wafer and photoresist

Following sequence: Back contact aluminum deposition

During Sequence 11, the samples are bonded to carrier wafers using photoresist. The purpose of the carrier is to provide mechanical support to the membranes during the lithography process that defines contact holes in the silicon dioxide layer covering the back of the solar cell. Additionally, the nitride overhangs on the back window (from the KOH window etch in Sequence 10) are manually scribed off to ensure continuity of the conductive aluminum back contact film that will be deposited in Sequence 12.

In preparation for photolithography on the now-exposed back oxide, the first step is to coat the sample wafer with HMDS, which is needed to enhance photoresist adhesion in step 3 of this sequence.

The samples are next attached to a carrier wafer using a thick photoresist, such as AZP4620, and a Q-tip. The photoresist is brushed on the top surface of the device wafer, carefully avoiding contact the very fragile dies. See more about the photoresist painting procedure in Appendix 3. After applying the resist, a dummy carrier wafer is pressed into contact with the sample. The stack is then baked in an oven at 95 °C for 60 minutes to harden the resist.

The next step in Sequence 11 is photolithography on the exposed back oxide of each membrane solar cell. The wafer stack is placed on the vacuum chuck of a spin-coater (the raison d'être of the carrier wafer is to prevent the vacuum from tearing out the membrane solar cells during this step). Standard thin positive photoresist, in this case SPR700-1.0, is pipetted into the well at the back of each solar cell and then spun at 1750 RPM, followed by baking at 95 °C for 30 minutes in an oven.

Patterning this oxide is made difficult by the 500 μm offset between the surface to be patterned and the back wafer surface. Two notable problems that arise are:

1. The photoresist coat at the bottom of each well is highly uneven given the flow patterns of the resist out of (and sometimes into) each well, with the resist tending to pile up against the walls on the downstream side of each die. A more uniform coating process, such as aerosol spraying, might yield superior results during the exposure process.
2. The offset between the mask and the image plane at the base of the wells leads to diffractive effects that complicate the exposure process. In a typical exposure process, the mask is brought into contact (or near contact) with the surface being patterned to ensure accurate transfer between the mask and substrate. When exposing a pattern at a distance as in this case, diffraction can generate significant

distortions between the mask and the pattern transferred to the photoresist. As the pattern features become smaller (and more densely packed), diffraction becomes worse, which poses a lower limit on the size of the contact pattern that can be used for the back of the solar cell. In an early embodiment, 12 μm holes on a 75 μm pitch were used. Owing to diffraction, virtually the entirety of the positive resist was removed during exposure, an effect that is aggravated in regions of the well where the photoresist is particularly thin. To combat diffraction, a mask was designed with larger (25 μm) holes on a 75 μm pitch, combined with a buffer zone on the four edges of the die with a much larger pitch. See more on this problem in Appendix 3.

The wafer is exposed for ~3.5 seconds using a 10 mW cm^{-2} i-line mask aligner, developed in MF CD-26 for 75 seconds, and then hard-baked in an oven at 120 °C for 30 minutes.

After photolithography, the next step is to scribe the nitride overhang from each of the solar cell window openings on the back of the SOI wafer. This step is actually in preparation for the final sequence in which aluminum is sputtered over the backside of the wafer. In order to make electrical contact to the p-type region of the device, the aluminum film needs to be continuous from the back of the solar cell, up the angled sidewalls of the well, and onto the bulk area of the handle wafer. During the KOH membrane etch of Sequence 10, the KOH undercuts the nitride mask, leaving a 'lip' of nitride overhanging the silicon sidewall. Using a diamond-tipped scribe, the unwanted material is manually removed, being very careful not to contact the delicate solar cell in the process.

The next step in the sequence is to etch the back oxide using the patterned photoresist as a mask. First, the wafers are immersed in DI water for a short time. This key step allows water to fill the air gaps between the carrier and device wafers, which would otherwise be filled with BOE solution. After the DI water immersion, the oxide is etched in BOE for ~250 seconds to open up contact holes in the oxide and expose the underlying p-type silicon.

Once the samples have been thoroughly rinsed and lightly dried, they are placed in acetone overnight to dissolve all of the photoresist on the wafers and separate the carrier. After separating the device wafer from the carrier, it is washed in fresh acetone, then methanol and IPA (Fig. 34). The IPA dries without leaving behind a residue, after which the devices move immediately into Sequence 12, which begins with coating the back of the device with aluminum.

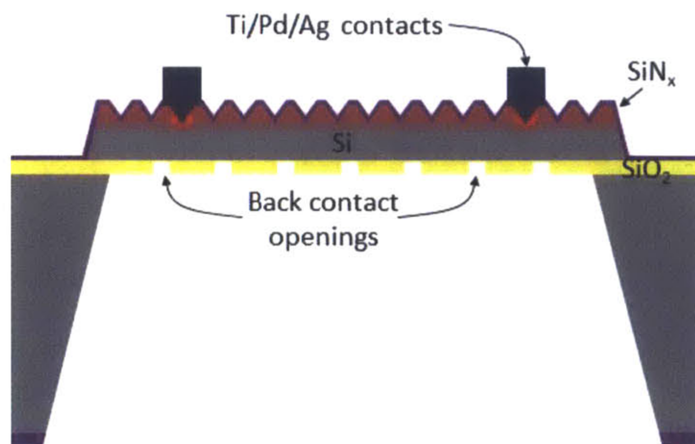


Figure 34 | Back contact holes patterned in oxide and nitride overhangs removed at the conclusion of Sequence 11.

4.12 Sequence 12: Back Contact Deposition and Anneal

Preceding sequence: Patterning the back oxide, ending with carrier wafer removal in three-solvent clean
Sequence steps:

i. Deposit aluminum on back side of device
ii. Anneal

Following sequence: Completed device!

In the final process sequence, the back aluminum contact is formed and the structure annealed to complete the fabrication process. To begin Sequence 12, the wafer is moved straightaway from the three-solvent clean to the vacuum chamber of a sputtering tool to limit contamination and native oxide growth in the back contact region. A 600 nm aluminum film is sputtered over the back of the wafer, coating the p-type silicon contact regions, the remaining oxide on the back of the devices, as well as the sidewalls and back surface of the silicon handle wafer (Fig. 35).

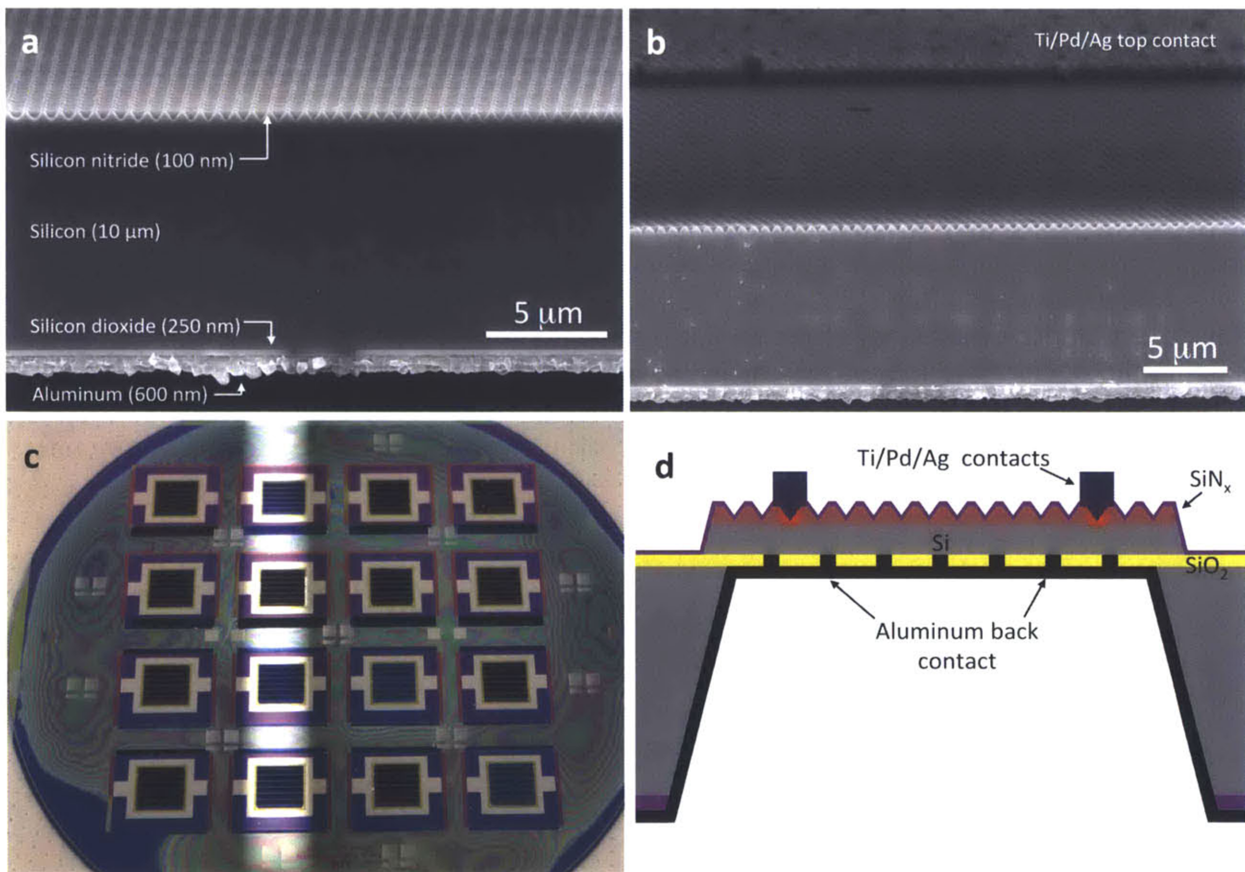


Figure 35 | Completed ultrathin crystalline silicon solar cell on a suspended membrane. a, b, c, d, SEM cross-sections (**a, b**), photograph (**c**), and schematic (**d**) of completed thin silicon photovoltaics.

Finally, the device is annealed at 400-500 °C in an oven flowing forming gas (7:1 N_2:H_2). The best results obtained by the author were using a temperature of 475 °C. The total oven time is 30 minutes: the first 15 minutes allow the temperature to equilibrate, followed by ten minutes of forming gas flow and then five minutes to evacuate hydrogen.

The annealing step is critical to reduce contact resistance and improve the open-circuit voltage and fill factor of the completed device. In addition, hydrogen available in the forming gas diffuses into the nitride surface of the device, improving passivation and open-circuit voltage.

4.13 Summary

Chapter 4 details the design of the fabrication process and processing parameters used to produce the experimental, high efficiency crystalline silicon thin film photovoltaics presented in this thesis. The 82-step process is divided into 12 sequences highlighting major deposition, patterning, doping, and thermal steps:

1. Inverted Pyramid Photolithography
2. Inverted Pyramid Surface Texture
3. Mesa Isolation Structure
4. Selective Emitter Preparation
5. PN-Junction Implantation and Annealing
6. Nitride ARC Deposition
7. Top Contact Via Lithography and Etch
8. Backside Window Etch
9. Top Contact Metallization
10. Membrane Formation
11. Pattern Back Oxide
12. Back Contact Deposition and Anneal

In addition to the resources provided in this section, suggestions and recommendations for troubleshooting problems can be found in Appendix 3.

Chapter 5: Thin-Film Crystalline Silicon Solar Cell Device Performance

The device and fabrication process designs of the preceding chapters were refined over successive generations of experiments, steadily improving the efficiency and yield of completed devices. The experimental effort culminated in 10-μm-thick crystalline silicon photovoltaics with peak efficiency of 15.7% and short-circuit current of 34.5 mA cm^{-2}, marking a substantial improvement over competing devices in this thickness range (Fig. 36).

In this chapter, the optical and electronic characteristics of the two best-performing devices – the one yielding the highest efficiency, Device A, and the highest short circuit current, Device B – are presented in detail (Fig. 37). A planar reference with an identical material stack – save for a 70 nm nitride ARC instead of 100 nm – is included for reference. In section 5.3, insight from simulation is applied to understand the possible origins of low V_{OC} in completed devices, focusing on the effects of back contact doping and bulk and surface recombination. Then in section 5.4, an analysis of current loss mechanisms is developed using data synthesized from simulation and experiment to focus attention on specific areas of improvement. Much of the potential for additional current gain is dependent on reducing parasitic absorption losses in the back aluminum reflector and nitride ARC, while the most significant efficiency improvements can be found by improvements to the device design that increase V_{OC}. Addressing the voltage issue in particular would yield device efficiencies competitive with current commercial crystalline silicon photovoltaics while requiring 35 times less material.

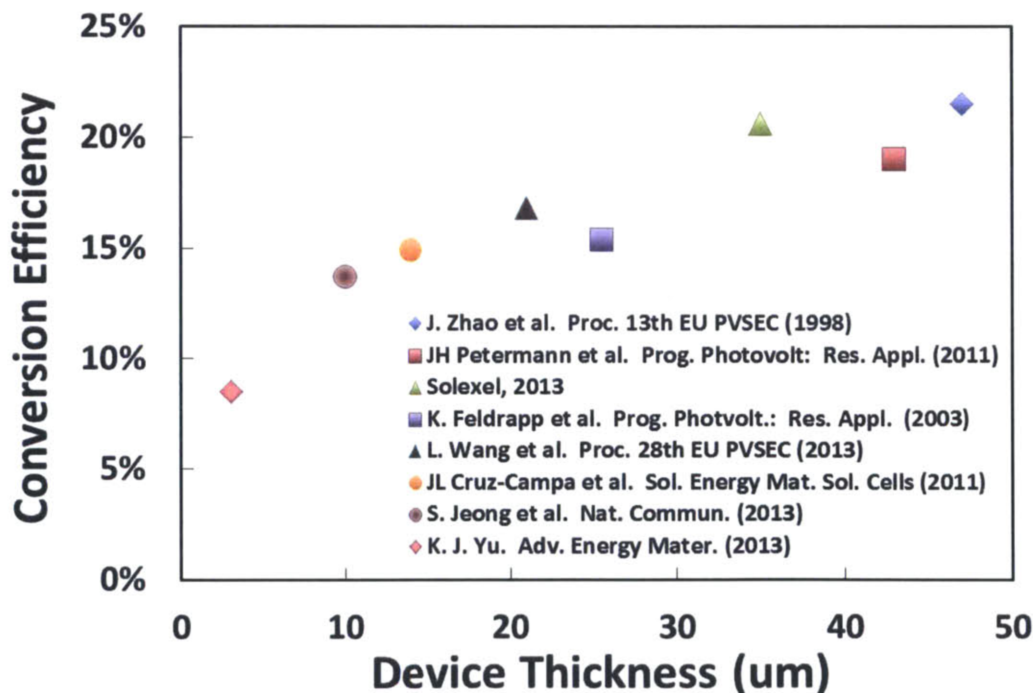


Figure 36 | Select power conversion efficiency data from literature for ultrathin crystalline silicon solar cells. (Refs. 20, 28, 35, 63-65, 98-99)

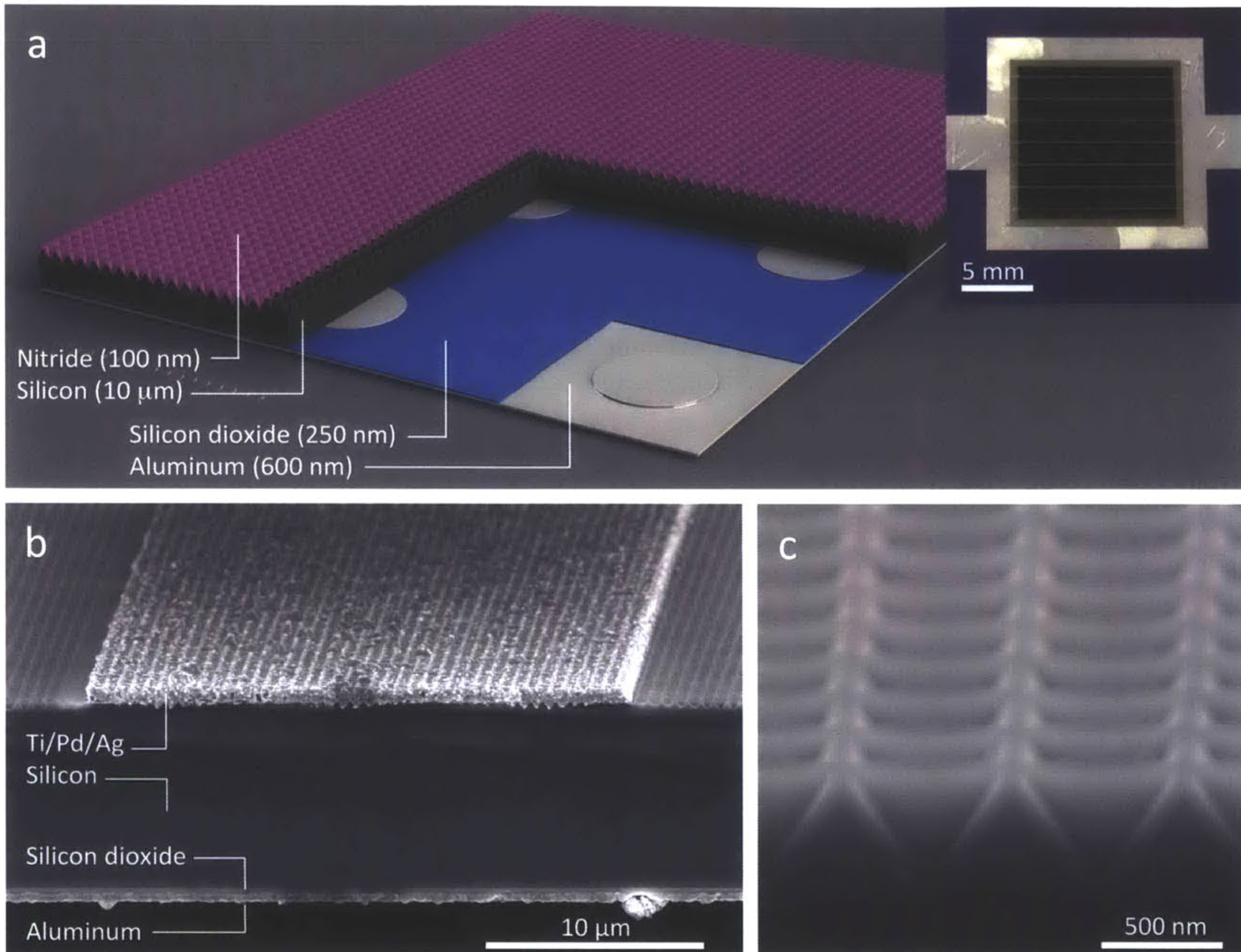


Figure 37 | Design of an ultrathin silicon solar cell with a periodic inverted nanopyramid light-trapping structure. **a,** Schematic and photograph (inset) of a 10-μm-thick crystalline silicon photovoltaic cell with an integrated periodic surface light-trapping structure. **b,** SEM cross-section image of the device highlighting the material stack. **c,** High magnification SEM cross-section emphasizing the conformal PECVD nitride ARC. *Schematic courtesy J. Loomis, MIT.*

5.1 Optical Characteristics

The exceptional absorption in these devices, in spite of such a thin absorbing layer, underpins their power conversion efficiency. Figure 38a presents the total measured absorptivity as a function of wavelength for Devices A and B, where it can be seen that greater than 90% of photons for wavelengths ranging from 400-920 nm are absorbed. The impact of this specific light-trapping design becomes most apparent in the wavelength range between 800nm and 1100nm. Beginning at 800nm, the photonic absorption depth in silicon rapidly lengthens beyond 10 μm and a longer residence time is required for the energy of individual photons to be absorbed in the silicon. The surface inverted nanopyramids – combined with the rear

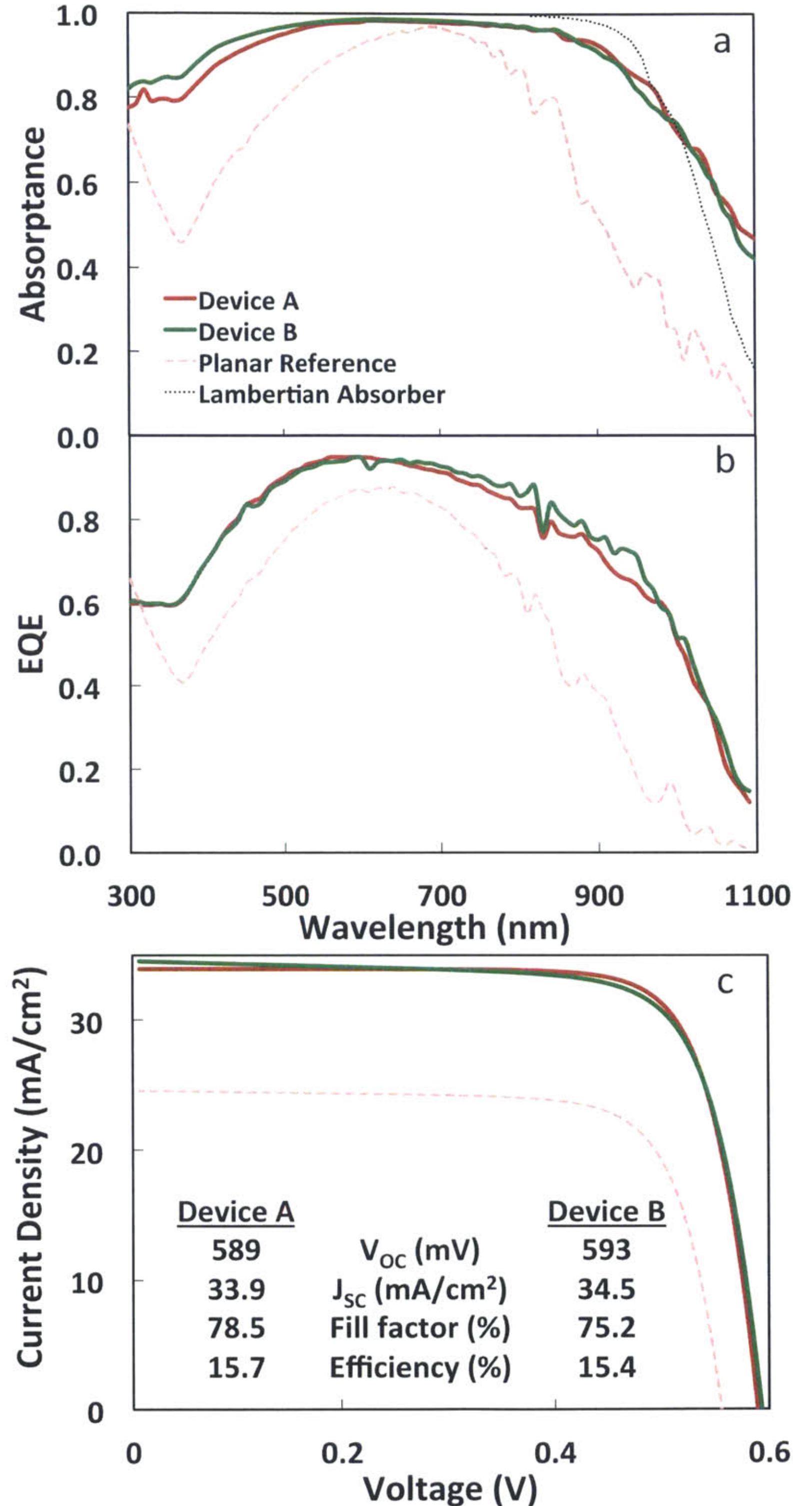


Figure 38 | Optical and energy conversion characteristics of inverted nanopyramid ultrathin silicon solar cells. a, b, Experimentally-measured absorptance (**a**) and external quantum efficiency (**b**) of devices A (highest efficiency), B (highest current), and a planar reference as a function of wavelength. (**c**) Current-voltage (I-V) characteristics of devices A and B and a planar reference cell.

dielectric/reflector stack – work to confine the electromagnetic energy in guided modes in the absorbing film, raising the absorptance substantially in the range $800<\lambda<1100$ nm. Absorptivity noticeably tails off beyond 1000 nm as the bandgap is approached. Yet as can be seen by comparison with a Lambertian absorber the inverted nanopyramid array performs very well, with measured absorptivity at wavelengths longer than 800 nm at most 7% (absolute) less than Lambertian. It should be noted that at these longer wavelengths a portion of the measured absorption in the device takes place in the rear aluminum reflector, estimated from simulation to be approximately 2%, 20%, and 60% of total absorption at λ = 800, 950, and 1100 nm, respectively. As a result, measured total absorption exceeds Lambertian light trapping for $\lambda>1000$ nm. The Lambertian calculation only includes absorption in a 10 μm silicon film.

5.2 Electrical Performance

The electronic design described in Chapter 3, combined with excellent trans-spectral absorption, deliver high quantum conversion efficiencies. Between 440 and 850 nm, the external quantum efficiency (EQE) exceeds 80% (Figure 38b). For $\lambda<450$ nm and $\lambda>850$ nm, the light-trapping structure plays an important role in raising quantum efficiency, but it can be seen that the EQE still decays in both ranges. Compounding the effect of higher reflection below 450 nm, EQE is also reduced by surface and Auger recombination as these high-energy photons are largely absorbed within the heavily-doped ~600 nm thick n-type emitter. Above 850 nm, EQE begins to roll below 80% and fall rapidly after 970 nm. In addition to the negative impact of declining absorption discussed in the preceding paragraphs, a major driver of the decline in EQE is parasitic photon absorption in aluminum and nitride. Parasitic absorption is particularly strong in the back contact regions where the aluminum is not cladded by oxide. The remainder of the back aluminum reflector is also affected by parasitic absorption, although to a reduced degree since the oxide works to channel electromagnetic energy away from the rear aluminum reflector.

Elevated spectrum-wide quantum efficiency translates to high short circuit current, a key component of power conversion efficiencies greater than 15% (Fig. 38c). The 34.5 mA cm^{-2} short-circuit current of Device B marks a new record for crystalline silicon devices of 10 μm thickness, only 5 mA cm^{-2} less than the 39.6 mA cm^{-2} for a 10 μm Lambertian absorber. Device A, with a slightly lower current (33.9 mA cm^{-2}) but superior fill factor sets a new power conversion efficiency mark at 15.7%. The EQE measurements corroborate the J_{SC} data. For both devices, the open-circuit voltage is around 590 mV, allowing ample room for improvement[35]. Potential origins of reduced V_{OC} are explored through simulation.

5.3 Voltage Dependence On Recombination and Back Contact Doping

The efficiency advances realized in this these ultrathin crystalline silicon devices is largely a result of gains in short circuit current, while the open circuit voltage still offers significant space for improvement. The NanoEngineering group at MIT developed an integrated photonic/electronic transport model to guide the design and development of these nanostructured thin-film solar cells, which can also be used to gain insight into potential sources of V_{oc} degradation that adversely impact overall device efficiency. The finite element simulation is carried out using the COMSOL Multiphysics® semiconductor module applied to a two-

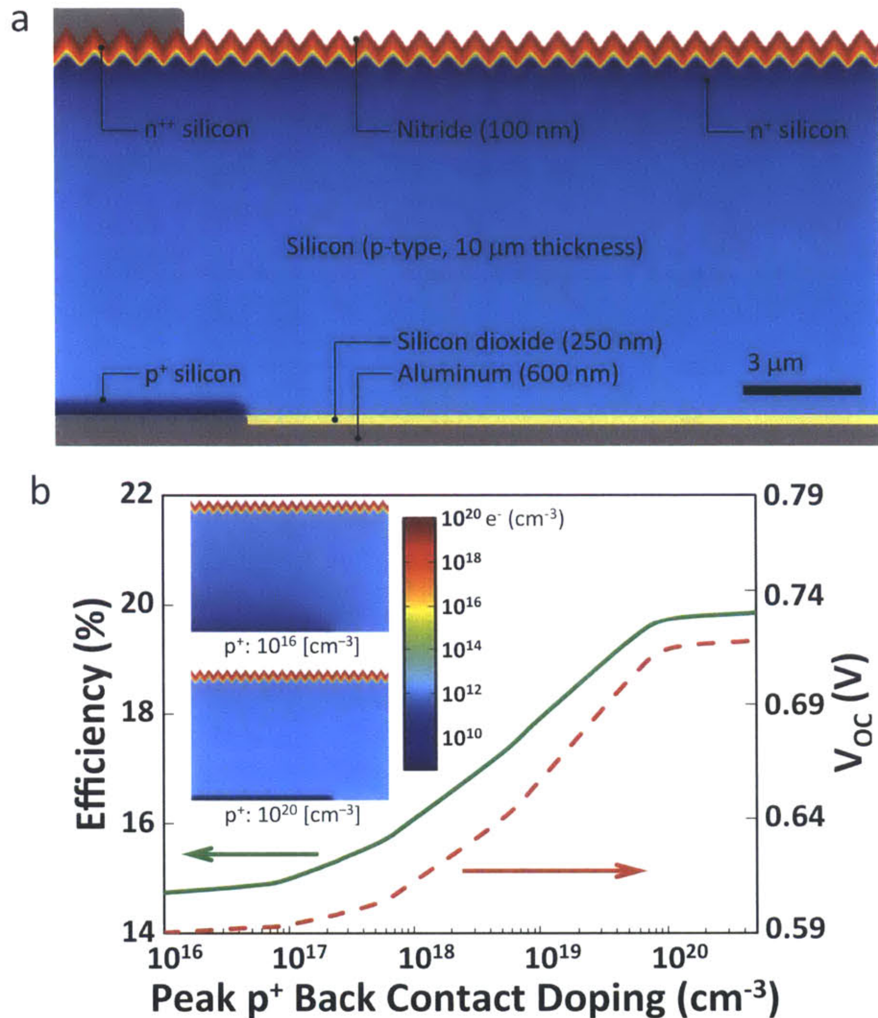


Figure 39 | Dependence of open-circuit voltage and efficiency on local back contact doping. a, Diagram of the structure used for integrated electrical and optical finite element simulation. The top contact metal shown is removed during optical simulation and front surface recombination velocity is fixed at 5 cm/sec. **b,** Simulated V_{OC} and efficiency as a function of p^+-dopant concentration at the back contact. The insets show how the electron concentration profile changes with rear p^+-doping at an operating voltage (V_a) = 0.56V. *Data courtesy W.–C. Hsu, MIT.*

dimensional analogue of the physical devices with a 50 nm ridge separating one inverted pyramid from another (Fig. 39a). The data presented herein are courtesy of W. – C. Hsu and S. Yerci; additional simulation details can be found in Appendix 1.

One of the most likely culprits for low open-circuit voltage in the experimental devices is the lack of a heavily-doped p^+ region in the vicinity of the rear contact holes. Without the field induced by highly-doped silicon, minority carriers will readily recombine at the rear contacts[91]. Fig. 39b captures the roll-off in open circuit voltage from 720 mV to 600 mV as the strength of the p^+-doping in the rear contact region is reduced from $5x10^{20}$ cm^{-3} to the level of the base (3 x 10^{16} cm^{-3}). The final step in the fabrication process is annealing at 475°C in forming gas (7:1 $N_2:H_2$) which will augment the p-type character of the silicon contact region through aluminum diffusion. Yet it is likely the doping level is insufficient to stem back contact recombination

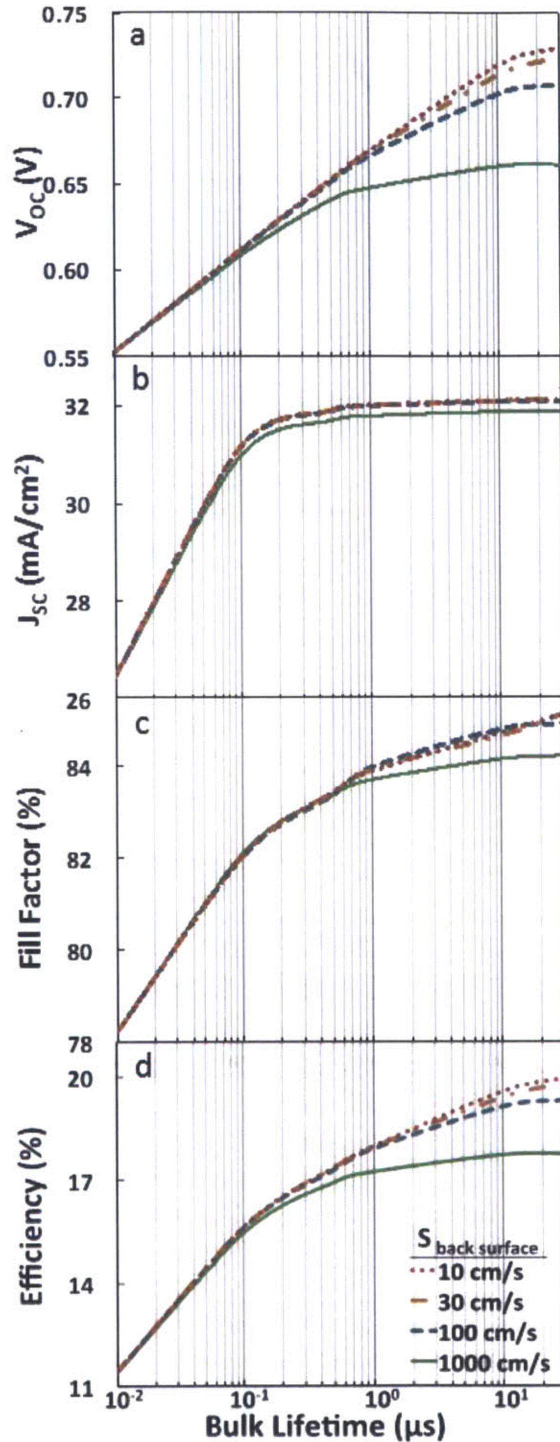


Figure 40 | Photovoltaic characteristics of a top- and bottom-contact ultrathin crystalline silicon solar cell as a function of bulk lifetime and surface recombination rates. a, b, c, d, Simulated open-circuit voltage (**a**), short-circuit current (**b**), fill factor (**c**), and power conversion efficiency (**d**) as a function of bulk lifetime and back oxide surface recombination velocity. The structure used for simulation is that shown in Fig. 39a. Front surface recombination velocity is fixed at 5 cm s^{-1}. *Data courtesy W.–C. Hsu, MIT.*

losses, and open-circuit voltage could see substantial improvements by designing the device to include a controlled, local boron p^+-diffusion/implantation of the rear contact as is typical for high-efficiency designs[94].

A second suspect for V_{OC} degradation is surface passivation and material quality. Thin devices have the advantage of being more tolerant of lower lifetime silicon material, but at the same time they are less resilient to high surface recombination velocities. The interplay between these two parameters can be seen clearly in Fig. 40a; open circuit voltage generally rises logarithmically with increasing lifetime until plateauing at a value dictated by the rear surface recombination velocity ($S_{R,back}$). In the device design presented here, recombination at the rear oxide/silicon interface may be higher than desired because silicon dioxide does not passivate p-type silicon particularly well[80]. The final anneal in forming gas of aluminum on top of oxide improves recombination characteristics at the rear surface through the "alneal" process[80,81], but more advanced rear surface passivation techniques could potentially boost open circuit voltage and efficiency significantly, particularly given the thinness of the devices and the attendant importance of surfaces.

Although bulk lifetime is less impactful on voltage and efficiency in thin devices than in thick ones, declining lifetime can have a significant effect on V_{OC} and efficiency, particularly for well-passivated devices. This is most evident in Fig. 40a where for $S_{R,back}$ of 10 and 30 cm s^{-1}, V_{OC} plateaus for $\tau > 30$ μs. Interestingly, as lifetime decreases, the optimal thickness of a silicon device for peak efficiency also decreases. As shown in Bozzola et. al., given assumptions about surface recombination and light trapping effectiveness, for bulk lifetimes below ~10 μs the optimal thickness of silicon is less than 20 μm[87]. It is understood that the manufacture of an SOI device layer can lead to a reduction in lifetime and consequent decrease in voltage and efficiency. Although low bulk lifetime might contribute to the observed V_{OC} degradation, the device thickness is such that the effect of low bulk lifetime is somewhat mitigated.

5.4 Photon Flow Analysis

One standard reference sun (AM1.5G spectrum) radiates approximately 2.73 x 10^{17} photons cm^{-2} s^{-1} between 300 nm and 1105 nm, giving a maximum short circuit current of 43.8 mA cm^{-2} for a silicon solar cell with a 1.12 eV bandgap. Although the 34.5 mA cm^{-2} peak J_{SC} for the devices presented here is a substantial improvement over existing thin film devices, we seek to understand the origins and magnitudes of current loss in these experimental devices to better inform strategies for improvement.

The principal sources of current loss in a thin p-type crystalline silicon device with a double-sided contact design are:

1. Reflection losses, consisting of:
    a. Reflection from the top metal contact fingers
    b. Reflection from the top surface of the device at the nitride/air interface
    c. Leakage of long wavelength, unabsorbed radiation from the internal device
2. Parasitic absorption, consisting of:
    a. Parasitic absorption in the top nitride film
    b. Parasitic absorption at rear aluminum metal contact points
    c. Parasitic absorption in the rear oxide-cladded aluminum reflector

3. Recombination (predominantly Auger) in the heavily-doped n-type emitter and at the top surface
4. Recombination in the p-type base, consisting of:
   a. Shockley-Read-Hall (SRH) recombination
   b. Recombination at the rear semiconductor/metal interface
   c. Recombination at the rear semiconductor/oxide interface

Through the synthesis of empirical absorption and quantum efficiency data with results from simulation, an analysis of the various destinies of all photons incident on device B from the sun is presented in Fig. 41 and Table 2. The units of the ordinate are translated into short-circuit current per unit area and wavelength (mA cm^{-2} nm^{-1}) to connect the contribution of specific wavelength ranges to actual device current.

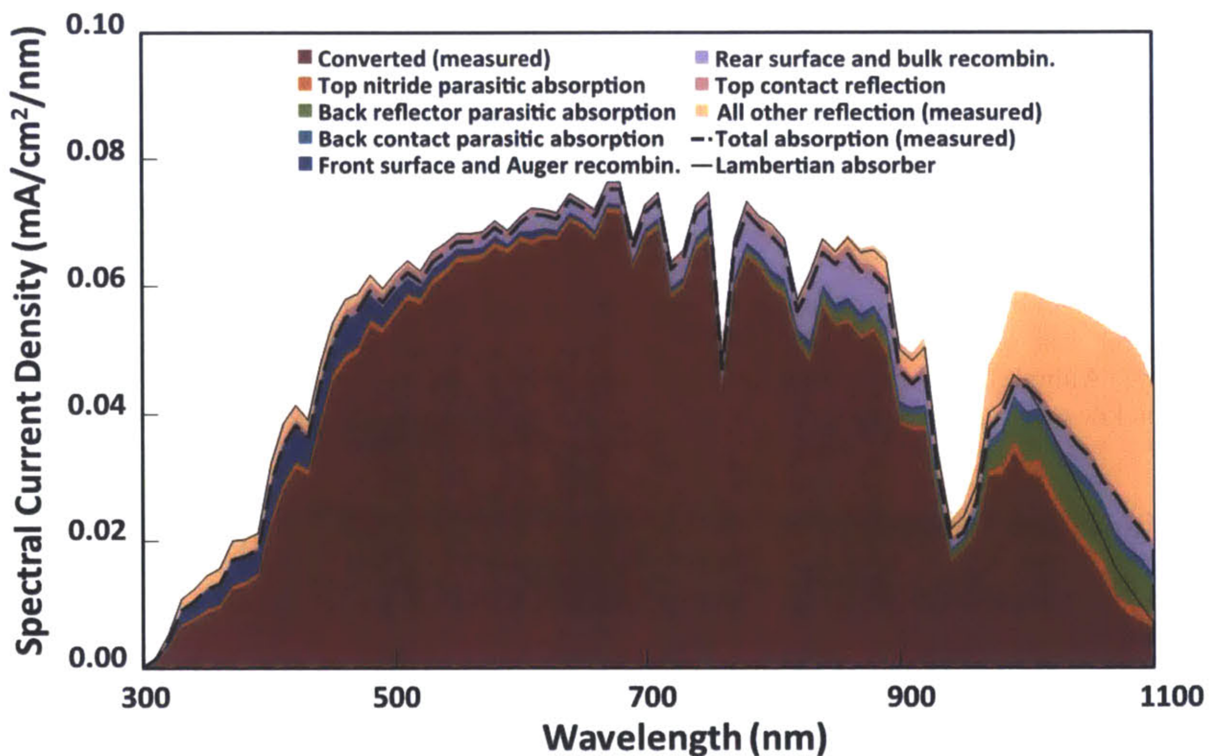


Figure 41 | Photon flow analysis. Spectral distribution of absorbed photons, collected carriers, and loss mechanisms as a function of wavelength for device B operating under short-circuit conditions (0V). The units of the ordinate are presented in terms of potential (or actual) short circuit current contribution per unit area per wavelength (mA cm^{-2} nm^{-1}). The area under the entire colored envelope corresponds to the total photon flux of the solar spectrum (AM1.5G), whereas that under the red envelope gives the measured output current at short-circuit operating conditions. Total absorption, given by the area under the dashed black line, includes those photons absorbed parasitically in the device structure as well as in the silicon absorber. Lambertian absorption is plotted as a reference. The converted current, total absorption, and reflection are from direct measurement; loss mechanisms (aside from reflection) are inferred from simulation. *Simulation data courtesy W.–C. Hsu, MIT.*

Wavelength Range (nm)	Solar Flux	Lambertian Limit	Total Absorption	Collected
		Photon Flux/Current (mA/cm^2) / % solar flux		
300≤λ<395	1.22	1.22 / 100%	1.04 / 85%	0.76 / 62%
395≤λ<495	4.92	4.92 / 100%	4.63 / 94%	4.00 / 81%
495≤λ<595	6.66	6.66 / 100%	6.51 / 98%	6.16 / 93%
595≤λ<695	7.27	7.27 / 100%	7.17 / 99%	6.81 / 94%
695≤λ<795	6.85	6.85 / 100%	6.71 / 98%	6.17 / 90%
795≤λ<895	6.57	6.53 / 99%	6.28 / 96%	5.35 / 81%
895≤λ<995	4.27	3.84 / 90%	3.57 / 84%	2.89 / 68%
995≤λ<1105	5.97	2.72 / 46%	3.52 / 59%	1.92 / 32%

Table 2 | Tabulated photon flux analysis data in 100 nm wavelength intervals.

The most conspicuous observation from the photon flow analysis is the significant fall-off in absorbed and converted photons beyond 970nm. In this range, the exponential increase in the photonic absorption length in silicon becomes problematic for ultrathin cells; whereas at λ = 950 nm the absorption length is 60 μm, at λ = 970 nm it is 120 μm, and by λ = 1000 nm it is 200 μm. The difficulty of converting these long-wavelength photons to current is illustrated by the rapid decline of the Lambertian absorber. In comparison to the Lambertian reference, however, the inverted nanopyramid structure functions extremely well. As a result of parasitic absorption in the back reflector and contacts, total absorption in the device actually exceeds the Lambertian limit for λ>1000 nm. The consequence is that a significant fraction of absorbed photons in the λ>970 nm regime are not converted to photocurrent. Photon conversion enhancement in the λ>970 nm wavelength range could be gained by reducing the rear contact size to lower parasitic absorption, among other strategies.

A current loss analysis can also be informative in the debate between top and bottom contacts versus all-back contact designs for thin film silicon solar cells. Note that the current loss owing to reflection from the top metal contacts is a constant 2.1% across the solar spectrum, for a total short circuit current density loss of 0.918 mA cm^{-2}. In an all-back contact design, both the p- and n-type contacts are placed at the rear of the device to eliminate reflection from top contact metals. Yet an all-back contact design includes a significant engineering trade-off for a thin-film crystalline device: because the n- and p-type metal contacts must be electrically isolated, a physical gap separates them. This gap allows long wavelength photons to leak out the back of all-back-contact cells. To a much greater degree than bulk silicon solar cells, the back metal contact serves a second critical role in ultrathin cells as the rear reflector, which is essential for optical performance. Based on an ideal contact pitch of 50 μm for an all-back contact design and a realistic contact separation of 5-10 μm[35], an all-back-contact design leaves 10-20% of an ultrathin device without a back reflector. For wavelengths λ>870 nm with absorption lengths greater than ~20 μm, a discontinuous back reflector has a non-negligible deleterious effect on total absorption and therefore current. Considering the measured current contribution of photons between 870 and 1100 nm is 6.25 mA cm^{-2} for Device B, losing 15% of these photons to leakage

out of the backside of the device in the absence of a rear reflector balances the reflection loss that top contacts would generate. Of course, this analysis does not
take into account other effects of top-bottom versus all-back contact designs that affect efficiency, such as the effect of changing the doping of the front surface field (FSF)/emitter between the two contact designs on V_{OC} and J_{SC}, and more experimental and simulation work is necessary to evaluate the trade-offs. The ultimate arbiter of success will likely be the relative manufacturability of one design over the other.

Summing the contribution of absorbed, collected, and lost current into 100 nm wide wavelength "bins" as in Table 2 allows for rapid quantitative assessment of the strengths and deficits of these devices from the perspective of current collection. For example, in the range $300 \leq \lambda < 395$ nm, Device B converts only 62% of incident photons to useful current after absorbing 85%, whereas an ideal Lambertian film would absorb 100% of incident photons. Absorption in this range is reduced in part by reflection losses from the nitride-coated surface, which is a direct consequence of optimizing the nitride coating and structure design for the higher photon flux regime of $\lambda > 500$ nm. Reflection losses are also enhanced by the finite ridge of silicon separating one inverted nanopyramid from another that in these devices is ~75-100 nm wide; reducing this width would lead to improved absorption in the short wavelength range[40]. Additionally, collection of minority carriers is relatively low for short wavelengths since carriers generated so close to the surface often recombine at the surface or through Auger recombination in the heavily-doped emitter. However, only 1.22 mA cm^{-2} worth of current density is available from the solar spectrum in the range $300 \leq \lambda < 395$ nm, and even double-digit percentage gains in absorption or collection efficiency would lead to negligible improvement in overall short-circuit current and device efficiency.

For wavelength ranges $\lambda > 495$ nm, the cells absorb all but 1-3% of possible photons compared to a Lambertian absorber, although conversion of the generated carriers to current can still be improved upon. Photon conversion to current is very high for $495 \leq \lambda < 795$ nm, where the solar flux is at its peak. In fact, only 1.64 mA cm^{-2} of potential short-circuit current density is lost over that wavelength range. Potential improvements could be most readily sought in the $395 \leq \lambda < 495$ nm and $795 \leq \lambda < 895$ nm ranges, where collection efficiencies of 81% are found despite photon absorption rates of 94% and 96%, respectively. Losses in these ranges primarily result from recombination in the emitter for the former, and parasitic photon absorption by aluminum and backside recombination for the latter.

5.5 Summary

The solar cells presented in this chapter realize the potential of new light-trapping designs to deliver high current and efficiencies in ultrathin crystalline silicon devices. Absorption approaches the Lambertian case over much of the relevant spectral range, and the devices convert these photons to current carriers very efficiently. From an optical perspective, advances in design that limit parasitic absorption in the rear reflector would be most beneficial. One approach could involve the inclusion of a Bragg reflector in lieu of a metal, although doing so in a cost-effective manner could prove challenging[51]. Significant challenges remain in designing fabrication flows and handling procedures for thin-film crystalline silicon solar cells, but the progress being made in that arena suggests that the promise of this light-trapping design to reduce module costs by cutting silicon material requirements is attainable.

Chapter 6: Empirical and Theoretical Study of Absorption Using Random and Periodic Pyramidal Surface Light Trapping Structures on Silicon

The development of new, wavelength-scale optical structures for enhancing absorption in thin-film crystalline silicon photovoltaics is premised on the thesis that conventional, micrometer-scale random pyramids are inappropriate for very thin silicon films. It is also posited that light-trapping structures with feature sizes in the wave optics regime could provide unusual absorption enhancement that is inaccessible to larger, geometric-optics features. While it is true that nanophotonic light-trapping structures would be required for absorbing films below ~2 μm in thickness, their benefit is not clear for commercially relevant thin crystalline silicon photovoltaics in the thickness range 5-40 μm.

Although newly-designed light-trapping structures are often compared with a theoretically optimal Lambertian absorber, absent in the literature are empirical and theoretical studies comparing the relative absorption effectiveness of "advanced" nanophotonic light-trapping structures with conventional, random pyramid structures. There are two primary explanations for this gap: 1) Thin silicon films are challenging to fabricate, particularly with pyramidal surface shapes formed using alkaline etching and 2) both random surface textures and periodic surface textures with features greater than one micrometer are challenging to simulate. There have been related studies that provide insight into the debate between random/periodic and wave optics/geometric optics for thin-film light trapping. Peters *et al.* compare absorption in random and periodic parabolic structures through simulation and find the best periodic structures slightly better than random ones[100]. R Dewan *et al.* find conflicting results between periodic inverted pyramids and randomly rough textures in microcrystalline silicon solar cells deposited on glass[55]. And in Khandelwal *et al.*, the authors find that periodic micron-sized cones provide superior optical performance to random pyramids on thick (520 μm) silicon wafers[34]. Meanwhile, Paetzold et. al. report an experimental study showing that randomness improves light trapping in nanophotonic light-trapping schemes for solar cells[101]. At best, the literature on the subject is inconclusive.

The focus of this chapter shifts from the design and fabrication of highly efficient thin silicon solar cells of the preceding chapters, seeking instead to understand the relative absorption capability of nanophotonic light-trapping designs – represented by inverted nanopyramids – compared to both periodic, micron-scale inverted pyramids as well as random upright pyramids. The findings indicate that, although inverted nanopyramid structures absorb very well, they are in fact comparable to both random pyramids and micrometer-scale periodic pyramids for light trapping in thin crystalline silicon films.

6.1 Absorption in Pyramidally-Textured Thin Silicon Films: Sample Preparation and Measurement

Beginning with SOI wafers (Ultrasil, 500 μm handle wafer, 250 nm buried oxide, varied p-type device layer thickness), samples were fabricated with four different surface morphologies: 1) randomly sized and spaced upright pyramids, periodic inverted pyramids on 2) 700 nm and 3) 2.2 μm pitches, and 4) planar (Fig. 42). Samples with periodic surface textures were

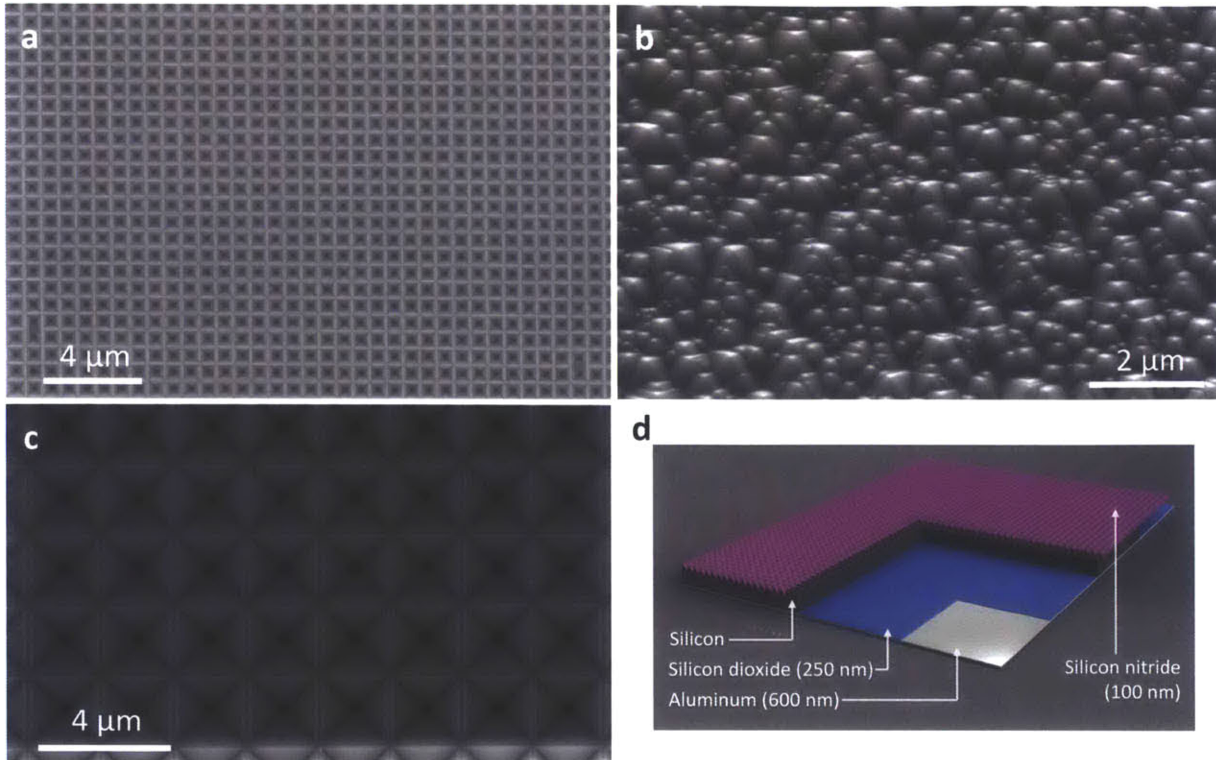


Figure 42 | Silicon thin films with pyramidal surface light-trapping structures. a, b, c, SEM images of (**a**) 700-nm-pitch periodic inverted pyramids, (**b**) randomly sized and spaced upright pyramids, and (**c**) 2.2-μm-pitch periodic inverted pyramids. **d,** Schematic of the design of the periodically-textured surfaces, which include a 100 nm PECVD nitride on the top surface, a 10 μm silicon absorber, a 200-250 nm silicon dioxide layer, and a back aluminum reflector.

produced following the same procedure as Sequences 1 and 2 in Chapter 4. Randomly-textured samples were formed by first treating a bare SOI wafer in SunSource 68 (Air Products) – a proprietary surfactant indicated to yield smaller pyramid heights – and then etched in a 4% KOH/2% IPA solution at 80°C for five to six minutes[73]. All sample types were then coated with ProTEK B3 after which windows were etched through the handle wafer using KOH, stopping on the buried oxide (see Section 4.10 for details). After stripping the ProTEK film in acetone, all samples were coated with a PECVD nitride ARC (n = 2.0) of variable thickness on the top surface and completed by sputtering a 300 nm aluminum film to serve as the back reflector.

6.2 Empirical Absorption Comparison of Pyramidal Light-Trapping Structures

The spectral details of absorption characteristics shown in Fig. 43a-c reveal subtle, informative differences between the three different surface structures for substrates of 5, 10, and 20 μm thickness, respectively. Virtually all of the periodic and random-pyramid-textured samples absorb extremely well for $500<\lambda<800$ nm, generally absorbing 95-99% of all photons in this range for all sample types. This portion of the solar spectrum also contains the highest

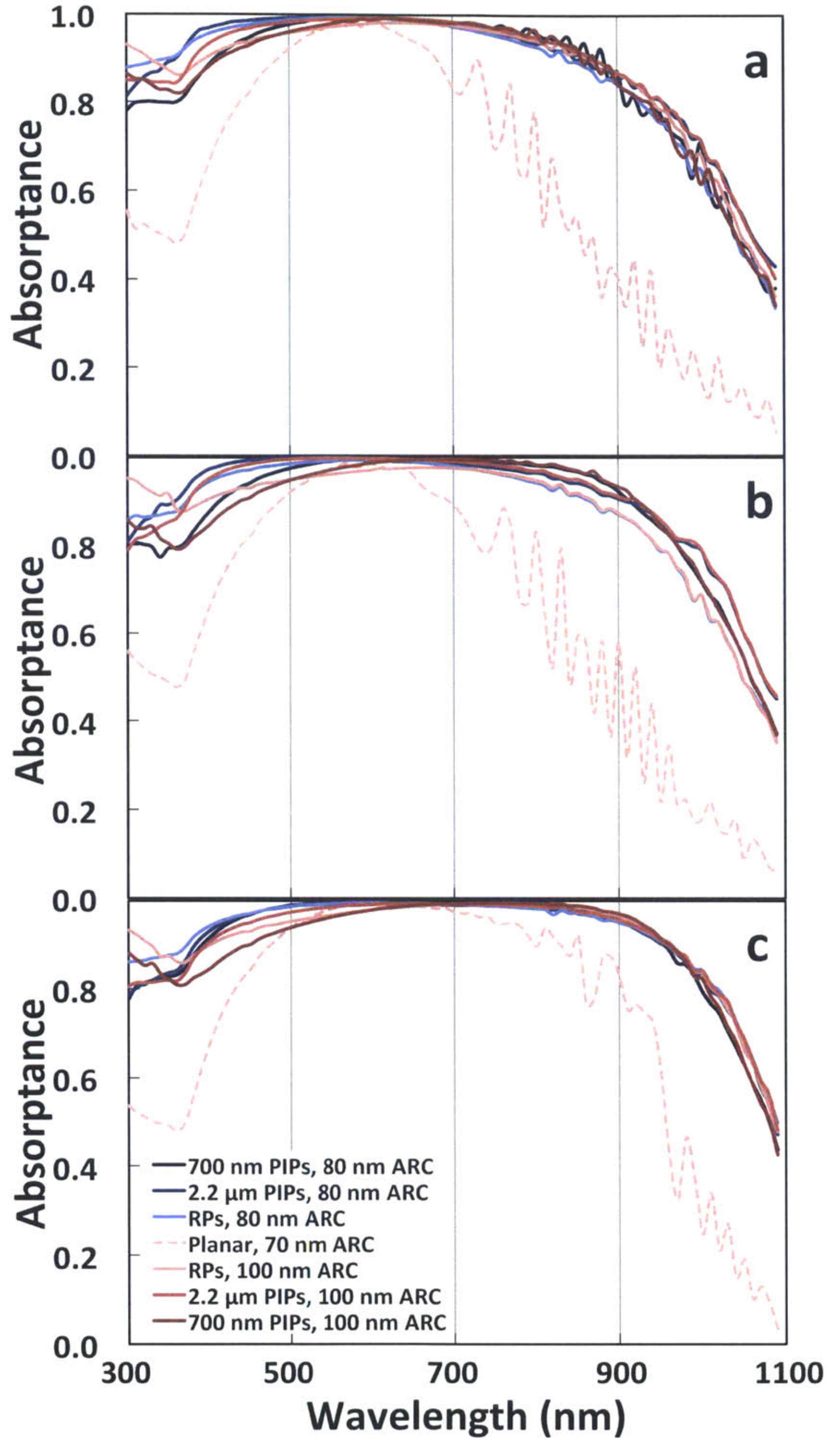


Figure 43 | Experimentally-measured spectral absorption in pyramidally-textured crystalline silicon thin films. a, b, c, Absorption spectra for silicon films (**a**) 5 µm, (**b**) 10 µm, and (**c**) 20 µm thick with surfaces textured with periodic inverted pyramids on 700 nm and 2.2 µm pitches, random upright pyramids, and planar surfaces for comparison. Each sample has a back oxide ~200 nm thick and a rear aluminum reflector. The thickness of the surface PECVD nitride ARC is provided in the legend.

density of photons (photons nm^{-1}), with about half (20.8 mA cm^{-2}) of the 43.8 mA cm^{-2} total current potential for $300<\lambda\leq1105$ nm falling in this range. Outside of this range, the differences in spectral absorption that can be seen from one textured sample type to another for a given silicon thickness arise from differences in the characteristic sizes of the surface textures, small variations in geometry, and experimental variation between samples. For example, in analogy with the case of a planar surface with an anti-reflection coating, decreasing the ARC thickness causes a distinct blueshift of the wavelengths of peak absorption. The signature of this effect is visible in Fig. 43a-c in the range $350<\lambda<500$ nm, where on average for a given surface structure type, those with an 80 nm ARC are more absorptive. Similarly, for $\lambda>800$ nm, the version of a given structure with a 100 nm ARC tends to be more absorptive, although this trend is somewhat confounded by other variables for some of the samples.

Simultaneously, details of the surface textures themselves impact specific portions of the spectrum. Simulation indicates that reflection from the top surface increases in the "blue" range ($300<\lambda<500$ nm) as the width of the ridge, w, separating one pyramid from another increases for periodic inverted pyramids in the size range considered here. This effect can be understood by considering that the fixed pitch of the pyramids requires that for larger ridge widths, the proportion of surface area that is normal to incident photons is greater. Blue photons can better "see" these narrow regions of the surface by virtue of their short wavelength, and since the normal surface area presents a more abrupt index change, overall in-coupling effectiveness of the light-trapping structure decreases. As a result of the constraints of the fabrication process, the ridge width for the 700 nm periodic inverted pyramids is ~50-100 nm in width (15-25% of the surface area), while for the 2.2 μm period samples the ridges tend to be 100-200 nm in width (10-20% of the surface area). Although the impact of ridge width is convoluted with ARC thickness and other factors, the general trend can be observed in Fig. 43a-c that for $300<\lambda<500$ nm, the 2.2 μm samples with a smaller fraction of planar surface area exhibit superior absorption to the 700 nm-pitch periodic inverted pyramids for a given ARC thickness.

The random pyramid samples offer some of the best results in the range $300<\lambda<500$ nm (with the exception of the 10 μm cells where the random samples measured were of overall lower absorptance) while tailing off in the infrared wavelengths for $\lambda>800$ nm compared to the periodically textured samples. The improved performance in the short wavelength range may be a function of the lack of planar surface area for upright pyramids, per the discussion in the preceding paragraph. It may also be influenced by the relatively small sizes of the random pyramids for these experimental samples, ranging in height from 300-700 nm. The somewhat lower long-wavelength performance likely is a result of decreased maximum thickness of the random samples. For all sample types, the thickness referenced is the starting film thickness; owing to the fact that the random etching is done without any masking and the entire surface is etched in the process of forming pyramids – in contrast with the fabrication of the periodic textures – the maximum film height is reduced by 1-2 μm from nominal.

Note that in these ultrathin films, a non-negligible fraction of infrared photons are actually absorbed in the backside aluminum of the device. It is assumed that to first order the impact of parasitic photon absorption in aluminum is comparable between textured sample types; therefore, the measured total absorption without modification. For reference, Fig. 44 illustrates the magnitude of absorption in the backside aluminum calculated for a structure with 700 nm periodic inverted pyramids.

In spite of the small differences in spectral absorption characteristics between the pyramidally-textured samples, the total integrated absorption provided by the various surface

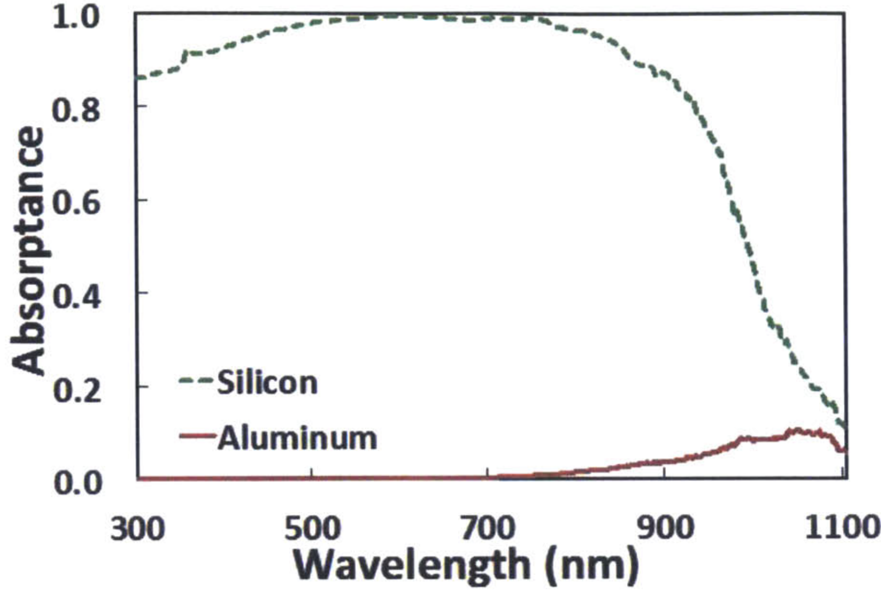


Figure 44 | Parasitic photon absorption in aluminum reflector. Simulated photon absorption in the rear aluminum reflector and silicon absorber for the structure shown in Fig. 42d with 700-nm-pitch periodic inverted pyramids and a 10 μm silicon layer. *Data courtesy S. E. Han, UNM.*

light-trapping structures is quite similar. To convey full-spectrum absorption capability, we use the maximum short circuit current ($J_{SC,max}$) as a metric. $J_{SC,max}$ is calculated as the inner product of the absorption and solar spectra (AM 1.5G):

$$J_{SC,max} = \int_0^{\lambda_g} A(\lambda) * I_{AM1.5}(\lambda) * \left(\frac{q\lambda}{hc}\right) d\lambda \tag{32}$$

As suggested by its name, maximum short circuit current represents the total electrical current that would be generated by a photovoltaic device with a bandgap wavelength of λ_g and 100% internal quantum efficiency operating at 0V. It is used here as a convenient representation of the total number of photons absorbed by a structure in terms that are familiar to solar cell specialists.

The spectral differences between the three flavors of pyramidal surface structures considered here average out to total absorption that, in addition to being comparable, is very high (Fig. 45). Consider 5 μm silicon films as an illustrative example. The mean $J_{SC,max}$ is 38.0 and 38.1 mA cm^{-2} for the 700 nm-pitch periodic inverted pyramids and random pyramids, respectively, while for the 2.2 μm-pitch periodic inverted pyramids it is slightly higher at 38.7 mA cm^{-2}. Even the most extreme difference – between random pyramids and 2.2 μm-pitch periodic inverted pyramids for 10 μm films – is only 1.5 mA cm^{-2}, and this is probably attributable in part to the small sample size and reduced sample quality of the random pyramid samples for 10 μm films. Broadly speaking, the difference in absorption effectiveness between large and small period periodic inverted pyramids and conventional random pyramids is effectively insignificant.

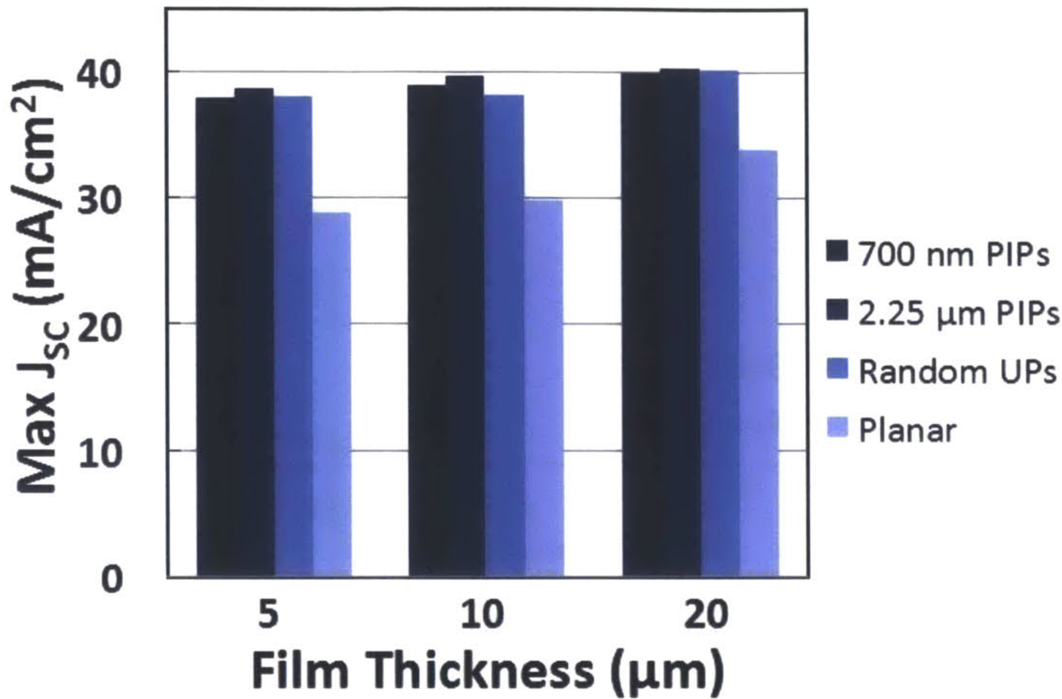


Figure 45 | Integrated total absorption in pyramidally-textured crystalline silicon thin films. Average experimentally-measured total integrated spectral absorptivity, expressed in terms of $J_{SC,\,max}$, for silicon films of 5, 10, and 20 µm thickness with random upright and periodic inverted pyramid surface textures. PIP and UP are shorthand for periodic inverted pyramid and upright pyramid, respectively.

Table 3 | Comparing pyramidal surface textures with Lambertian absorption. $J_{SC,max}$ for a Lambertian silicon surface compared with the best-measured value of total absorption for experimental samples with 700-nm-pitch periodic inverted pyramids and the structure shown in Fig. 42d. The right-most column gives the estimated absorption in silicon of the measured results using input from simulation.

Silicon Film Thickness (µm)	$J_{SC,\,max}$ (mA cm^{-2})		
	Lambertian Absorption	Total Absorption	Estimated Silicon Absorption
5	38.6	38.2	36.0
10	40.0	39.1	37.0
20	41.2	40.2	38.3

The similarity between these sample types is understandable since all approach the physical limits of total absorption in a thin film. From Table 3 it can be seen that for all thicknesses considered, the experimental samples fail to absorb at most 1 mA cm^{-2} of the photons that would be absorbed by a Lambertian absorber (3 mA cm^{-2} if excluding absorption in the aluminum). A significant fraction of the difference between the experimental and Lambertian values for these samples originates in the spectral range $300<\lambda<500$ nm, where the Lambertian

limit gives absorption values of better than 99.9% but reflection reduces absorption in the experimental samples. The finding that total absorption is similar in both random and periodic embodiments of a given geometry generally aligns with conclusions from other groups evaluating random and periodic textures in amorphous and microcrystalline silicon[100-102].

6.3 Comparing Absorption in Pyramidal Light-Trapping Structures: Simulation

The fundamental physical basis for the uniformly high absorption of these various pyramidal structures can be better understood through results from simulation. A three-dimensional finite element optical simulation was constructed in COMSOL Multiphysics® to model a variety of periodic structures (*Courtesy S. Yerci and W.-C. Hsu*). The first investigation is on the impact of the angle of the surface light-trapping structure unit cell on absorption effectiveness. In Fig. 11, spectrally integrated absorption is plotted against the feature angle for a periodic array of inverted pyramids. From these results, a local maximum is evident in the vicinity of 55° – almost exactly the angle provided by the anisotropic alkaline etch of silicon. Higher aspect ratio structures also perform well by this measure. It is well known that a graded effective index of refraction tends to reduce reflection from a surface across all wavelengths, which is reflected in these results by rapidly rising total absorption with increasing pyramid angle. The most pronounced effect of changing the pyramid angle, however, is on the "blue" portion of the spectrum $300<\lambda<500$ nm. In this range, the surface texture is large enough compared to the wavelength of light that the particle analogy of light from geometric optics can help visualize the way in which the angled sides of a given pyramid can reflect a normally-incident electromagnetic wave back and forth multiple times while channeling it toward the bulk to increase the odds of absorption. These two effects – grading of the index change and short wavelength channeling – combine to yield a relatively optimal result for the natural alkaline etch angle of silicon, 54.7° relative to a (100) surface.

The size (pitch) of the surface texture is another variable expected to impact the total absorption effectiveness of the light-trapping structure. In Fig. 46, total integrated absorption is plotted for periodic inverted pyramid light-trapping structures on a 10 μm silicon slab as a function of pitch, which by virtue of the fixed pyramid angle correlates to pyramid height as well. Total absorption increases precipitously until reaching a local maximum around 700 nm, then declines slightly. Interestingly, beyond a one-micrometer pitch, total absorption climbs back to a value comparable to a 700 nm pitch and remains steady. This finding is surprising because it implies that in spite of the greater volume of silicon that is removed for larger inverted pyramids, total absorption does not decline and even shows a somewhat positive trend for pitches larger than one micrometer.

The physical basis of the relationship between pitch size and total integrated absorption is challenging to visualize, but it is helpful to consider the distinction between geometric optics – in which photons can be treated as particles – and wave optics, in which phase matters. As the pitch of the light trapping structures increases, the range of wavelengths that can be described reasonably well using geometric optics grows. In the absorption maps shown in Fig. 47 for periodic inverted pyramids with 700 nm and 2.2 μm pitches, for example, the morphology of the absorption patterns is reasonably similar for both structures at wavelengths of (and between) 400, 600, and 800 nm, where either geometric optics or a blend of geometric and wave interpretations

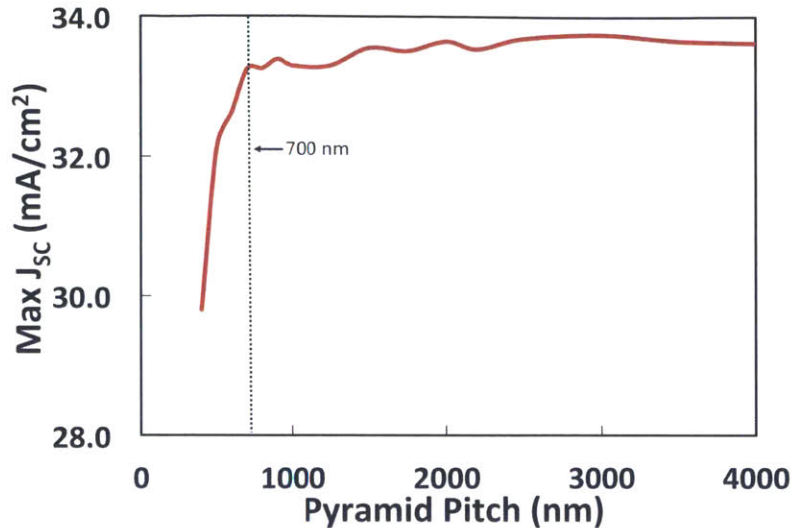


Figure 46 | Relationship between absorption and inverted pyramid size. Total integrated absorption ($300<\lambda<1105$ nm) as a function of pitch (pyramid size) for a silicon film textured with periodic inverted pyramids. The simulated film structure is the same as Fig. 42d, with a textured silicon film sandwiched between a 100 nm PECVD silicon nitride layer on the top surface and 200 nm silicon dioxide layer below. The back reflector is a 200 nm aluminum layer. Silicon film thickness is 10 μm; ridge width is fixed at 50 nm. *Data courtesy W.–C. Hsu, MIT.*

is relevant. Notice the stark contrast in the absorption pattern at λ=1000 nm, however. At this wavelength, a strong resonant signature is visible in the 700 nm periodic inverted pyramids – evidence of a wave optic effect – compared to an interference pattern typical of geometric optics for the 2.2 μm structures. We can thus understand the relatively constant, high absorption of periodic inverted pyramid structures with pitches beyond ~1200 nm by the fact that the interaction of such structures with the solar spectrum of relevance to silicon is largely on a geometric optics basis. For smaller pitch sizes, the total absorption potential tends to be more variable as wave optics descriptions are required for a greater and greater slice of the solar spectrum and absorption modes in the structures overlap with troughs and peaks in the solar spectrum. Another realistic consequence of nanophotonic periodic inverted pyramids is a proportionally larger planar area on the wafer surface compared to larger period inverted pyramids for a fixed ridge width, leading to higher reflection in the short wavelengths where $\lambda<500$ nm. The sum total result of these effects is to lead to an optimal pitch for nanophotonic inverted pyramids of ~700 nm, while micron-sized pyramids appear to be able to meet or exceed the nanophotonic results for a given ridge width.

The implications of these simulation results are significant to the study of light trapping for ultrathin crystalline silicon solar cells. Critically, they contradict the assumption that wavelength-scale features are requisite for high absorption in thin silicon slabs. Rather, near-ideal absorption values are obtainable using pyramidal features of a wide range of sizes, with the peak top-to-bottom thickness of the absorber and the slope of the feature serving as two major determinants of the absorption effectiveness for a specific surface geometry. A principal benefit of this result is that larger light-trapping features are more straightforward to fabricate, opening the possibility of a range of lithographic and non-lithographic masking approaches to produce effective periodic light-trapping structures inexpensively.

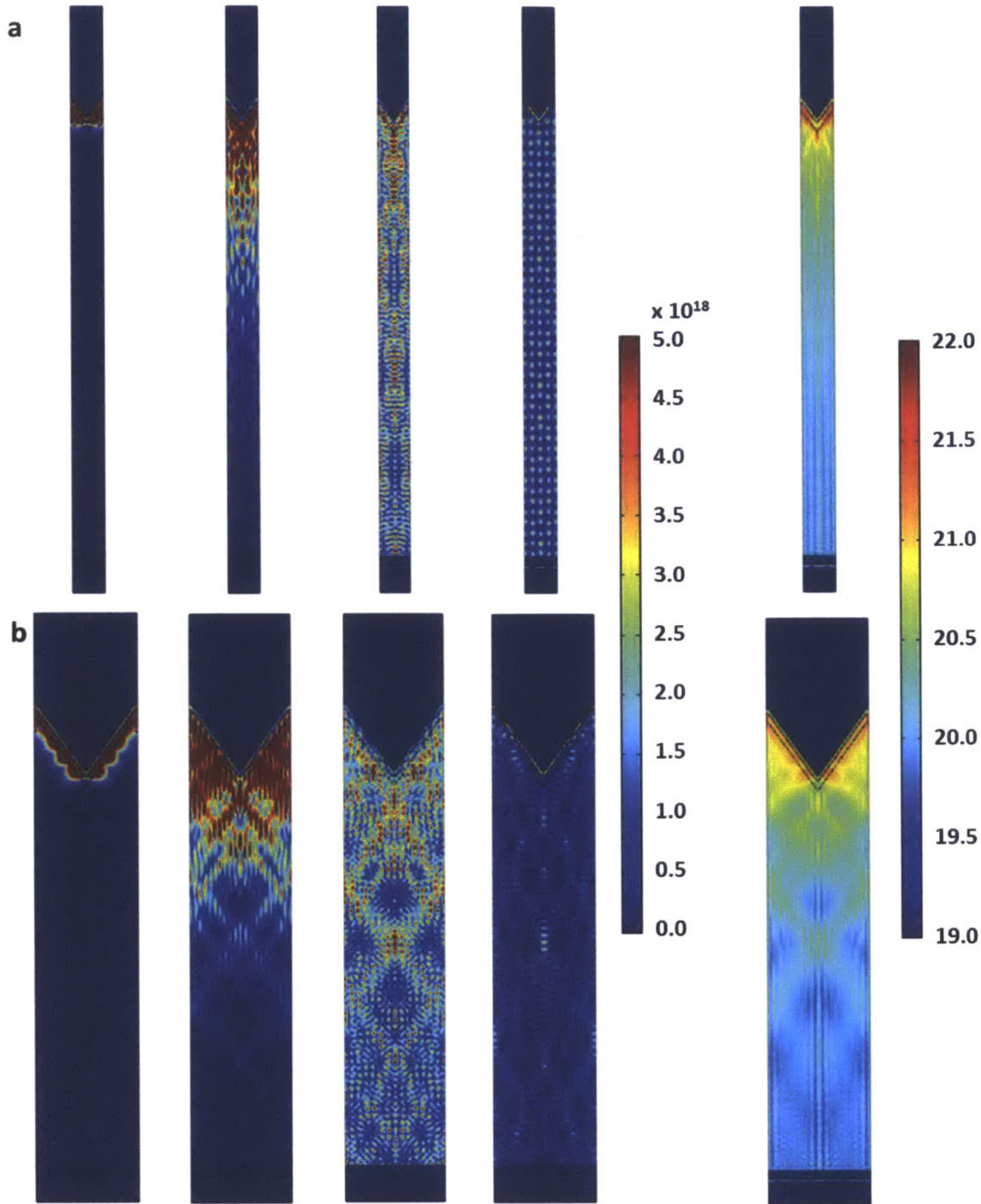


Figure 47 | Spatial generation patterns in textured thin crystalline silicon films. a, b Simulated spatial absorption profiles for two-dimensional analogues of periodic inverted pyramids with (**a**) 700 nm and (**b**) 2.2 μm pitches. Absorption is plotted for sample wavelengths of (from left to right) 400 nm, 600 nm, 800 nm, and 1000 nm, as well as cumulative absorption. The scale bar for the individual wavelength cross-sections is in units of cm^{-3}, while for the cumulative cross section it is in units of $\log_{10}$ cm^{-3}. Samples are modeled with 100 nm PECVD nitride AR coatings (70 nm for planar), 200 nm silicon dioxide rear dielectric, an aluminum reflector, and a 50 nm ridge width separating inverted pyramids. *Data courtesy W.-C. Hsu.*

6.4 Summary

The combined findings from experiment and simulation lead to the conclusion that conventional, random-pyramid-textured surfaces perform on par with newly-designed periodic structures. This result is informative for the design of ultrathin silicon solar cells. It should nonetheless be emphasized that random pyramid texturing cannot be applied to ultrathin silicon solar cells ad hoc and expected to perform perfectly. Without an etch mask, random pyramid texturing processes can significantly reduce the peak height of a film depending on the etch time, chemistry and concentration, and temperature. An overall decrease in film thickness will reduce absorption effectiveness, as evidenced by the decline in the Lambertian limit (Fig. 12). In the samples presented here, the five minute etches in 4% KOH:2% IPA solutions removed a minimum of 1 μm of thickness from the silicon films.

The similarity in total spectral absorption between conventional random surface textures and periodic inverted pyramids in ultrathin crystalline silicon solar cells is a very useful result. Two- and three-dimensional integrated photonic and electronic transport simulations can now be built for device modeling with the confidence that periodic surface structures and boundary conditions can realistically capture the physics at play in randomly textured solar cells. At the same time, it is simple to conceptualize new manufacturing flows incorporating periodic light-trapping structures that could provide easier and less expensive fabrication for thin film devices compared to traditional random pyramid texturing techniques, making the periodic inverted pyramids studied here a potentially valuable tool in the development of efficient and inexpensive solar power.

Chapter 7: Summary and Next Steps

7.1 Review of Contributions

The primary objective of this thesis was to develop a platform and a process for the incorporation and evaluation of advanced light-trapping structures into active, ultrathin crystalline silicon photovoltaic devices. As described in Chapters 2-4, an SOI-based cleanroom-compatible device architecture and fabrication flow was conceived and refined to produce progressively better devices with higher yield and improved repeatability of characterization. The resulting samples allow our team to probe previously inaccessible experimental questions regarding the optical and electronic characteristics of crystalline silicon solar cells with very thin absorbing layers. Although not suitable for commercial production, the platform itself, as well as insights gained in its development, have already and will continue to provide valuable data that will contribute to the eventual realization of commercially viable ultrathin crystalline silicon solar cells.

The second objective of this work was to utilize the nanophotonic light-trapping structures designed in the NanoEngineering group to demonstrate the energy conversion capabilities of a very thin solar cell. In producing a 15.7% efficient cell with a short-circuit current of 34.5 mA cm^{-2} using only 10 μm of silicon, this work establishes a new bar for a crystalline silicon solar cell of such thinness. Moreover, the efficiency mark was achieved in spite of a relatively low 590 V open-circuit voltage, indicating 1) the potential for devices fabricated on this platform to approach 20% conversion efficiency and 2) the excellent absorbing characteristics of the device's optical structure.

Finally, this work sought to address the literature gap comparing advanced, nanophotonic light-trapping designs with larger-scale periodic and random light-trapping structures. Leveraging the platform designed for solar cell development, pyramidal light-trapping structures were fabricated on suspended silicon membranes. The finding that pyramidal surface textures – both periodic and random, sub-micrometer- and micrometer-scale – yield comparable absorption in a thin silicon film is valuable for a number of reasons. Not only should it help guide the future work of others in the field of light trapping, but by showing that microscopic pyramids lead to absorption comparable to nanoscopic ones, it may steer future manufacturers of thin film crystalline silicon devices toward more manageable process flows based on surface textures with larger feature size.

There remains a multiplicity of research problems to address on the road to a 20% efficient ultrathin crystalline silicon solar cell. Beginning with the device results presented in chapter 5, the improvements can be broken down broadly into design and process changes to improve short-circuit current, and modifications that can improve open-circuit voltage. Here I discuss several promising research directions, as well as cursory findings from my experimental work that could provide starting points for fruitful research projects.

7.2 Improving Short-Circuit Current

As argued in section 5.4 and chapter 6, the inverted nanopyramid light-trapping structures implemented in both inactive silicon films and active devices for this thesis absorb extremely well, leaving only about 5.5 mA cm^{-2} of short circuit current potential remaining to be extracted

out of 40 mA cm^{-2} for an ideal Lambertian absorber. Nonetheless, the experimental platform that has been demonstrated here can be combined with the simulation capabilities developed in the NanoEngineering group to design light-trapping structures that perform even better than the one-sided pyramidal designs described in this thesis. Implementing features with curved surfaces, multi-scale randomness, or skewing could boost silicon absorption, and thus device current. Additionally, the author serendipitously fabricated a structure that shows unusually high blue-response and which should be investigated further for commercial applicability.

7.2.1 Advanced Light Trapping Design Using FEA Simulation

The three-dimensional combined optical and electronic finite element simulation developed in the NanoEngineering group can be combined with the experimental platform described in this thesis to produce new and even more effective light-trapping structures. The simulation capabilities have the most promise for designing structures that carefully sculpt the profile of absorbed photons to limit absorption in specific regions, like high recombination centers near sharp features (e.g., the apex of inverted pyramids), while maximizing overall absorption. Structures that have rounded features may be particularly suitable for meeting such requirements. Structures with rounded features could be produced by oxidizing pyramidal surfaces, for example, or using dry etching or a combination of KOH etching and dry etching to produce light-trapping features without the sharp tips of pyramids. Recent findings from simulation have also indicated that texturing both the front and back surfaces of a solar cell could provide up to a 10% increase in absorbed photons. The use of the powerful simulation tools developed in the NanoEngineering Group, combined with the ability to test those structures experimentally, has great potential to produce devices with even higher short circuit current.

7.2.2 Skewed Pyramid Light-Trapping Structures

As described in chapter 2, reducing the symmetry of light-trapping structures can increase absorption by reducing the degeneracy of waveguide modes in an absorbing material. Skewed nanopyramids, in which the centerline of the pyramid is not perpendicular to the base, have been shown through simulation to absorb even better than standard inverted or upright pyramids (Fig. 12). Skewed pyramids have also been shown to increase absorption in the geometric optics regime[103].

Using a (210)-oriented wafer, the author successfully fabricated skewed inverted pyramids using the same nitride-masked KOH etch process as was used to fabricate normal inverted pyramids (Fig. 48). As can be seen in the SEM image, by changing the crystallographic direction, the spacing between skewed inverted pyramids also changes, leaving large planar areas between them. Planar spaces increase reflection from a surface. Instead of a rectangular array, a hexagonal array would result in more densely-packed inverted pyramids and better optical performance.

Commercial monocrystalline silicon solar cells are fabricated using (100) wafers and upright, randomly spaced pyramids. **The recommendation from this thesis that could have the most immediate commercial impact would be to transition to (210)-oriented wafers**

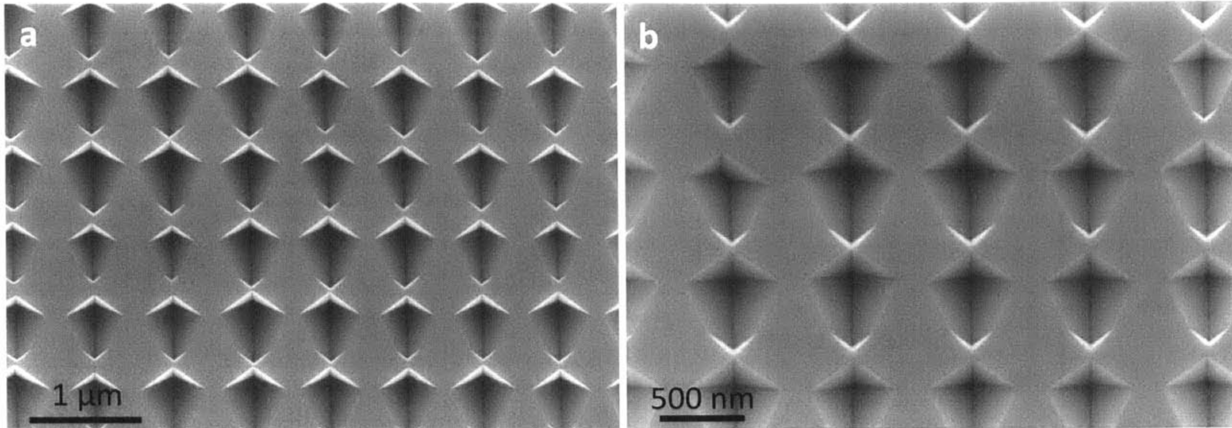


Figure 48 | Skewed inverted pyramids in (210) silicon. Images are taken at 0° (**a**) and 20° (**b**) angles.

from the standard (100) while using the same alkaline etch. The resulting skewed random pyramids would boost short-circuit current and overall device efficiencies.

In addition to skewed pyramids, symmetry-breaking through the design of structures with random order over different length scales points to another route to improve absorption beyond that accomplished in this thesis[48].

7.2.3 Abnormally High Short-Wavelength Absorptivity in Films Textured with Partially-Dielectric-Filled Inverted Pyramids

The author unintentionally fabricated an inverted-pyramid-based structure in silicon that showed impressively low reflectivity over the short wavelength spectrum while maintaining high absorptivity in the infrared region. In the effort to target the high-photon-flux portion of the spectrum between 500 and 800 nm, light-trapping structures often sacrifice absorptivity in the short wavelength region. Through the deposition of dielectric films inside the cavity of inverted pyramids, which were only partially removed in subsequent etches, the author arrived at a surface that absorbed extremely well for the entirety of the solar spectrum below the silicon bandgap (Fig. 49). Owing to time limitations, the exact structure of the sample has not resolved but was developed using the following process flow:

i. Started with a wafer surface patterned with inverted pyramids
ii. Grew ~6 nm thermal oxide over surface
iii. Deposited 61 nm LPCVD silicon nitride (n=2.25)
iv. Etched surface anisotropically (in a planarizing fashion) using SF_6/O_2 plasma, likely leaving behind silicon nitride in the inverted pyramid cavities but removing most of it from the surface ridge
v. Etched silicon nitride isotropically using hot phosphoric acid at 165 °C for 8 minutes (etch rate ~ 4 nm/min)
vi. Placed in BOE for 15 seconds (would have etched any exposed oxide)
vii. Deposited a 90 nm PECVD nitride ARC

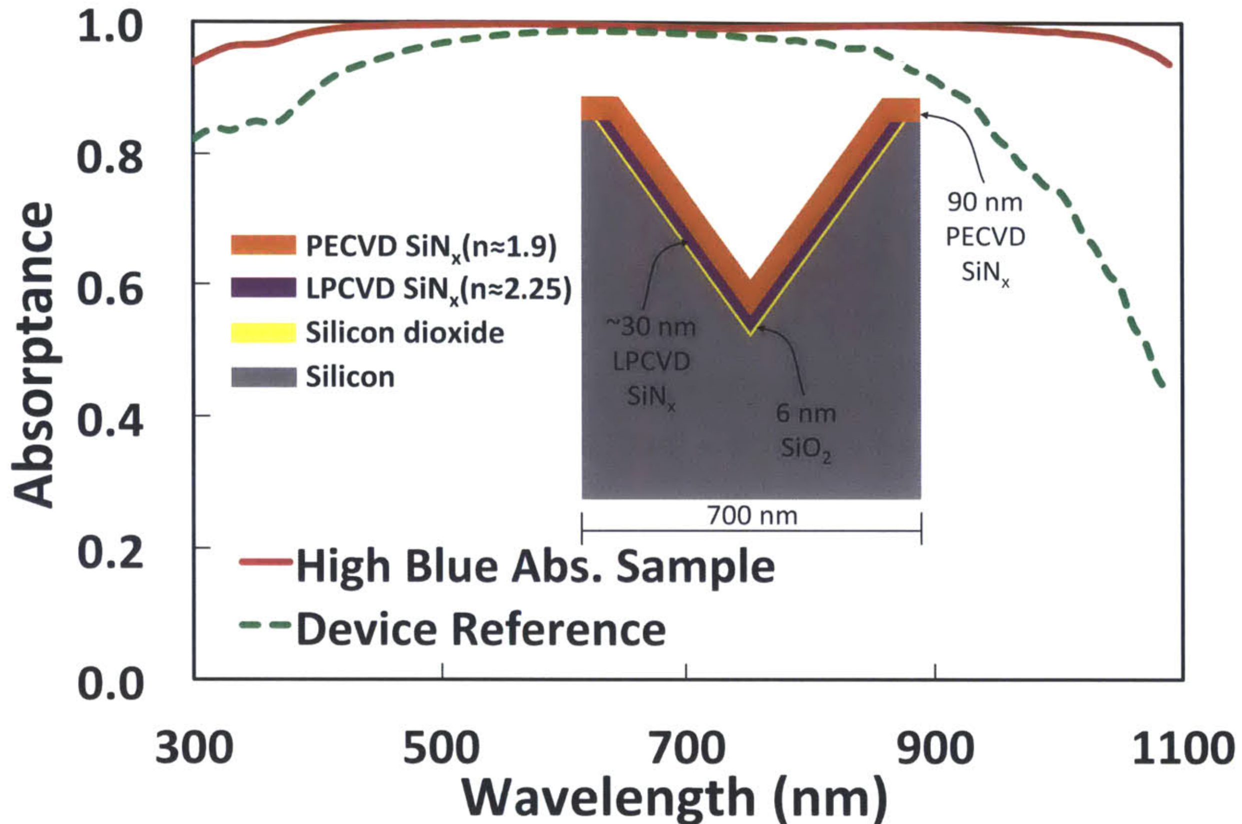


Figure 49 | Absorptance of the 625 μm silicon wafer described in Section 7.2.3 showing exceptionally high short wavelength absorption. The absorption spectrum of Device B (highest current experimental device, 10 μm silicon) is given for comparison. The inset is a schematic of the likely film structure coating the pyramidally textured wafer surface. Note that the LPCVD nitride and silicon dioxide is only present in the pyramid cavity.

It would be worthwhile to characterize more precisely the film structure that led to these results and explore process flows that could yield similar results intentionally, likely relying on anisotropic etches to non-uniformly coat textured surfaces with dielectrics.

7.3 Improving Open-Circuit Voltage

Although engineering the open-circuit voltage of a solar cell is outside the scope of this thesis, it also affords the most potential for improvement on the path to a 20% efficient silicon solar cell less than 20 μm thick. As discussed in section 5.3, the design change most likely to improve open-circuit voltage is to incorporate a controlled heavily-doped region at the back contacts into the device. Additional improvement may be explored using the integrated electronic/optical simulation developed in the NanoEngineering group. The sharp features of pyramidal light-trapping structures tend to concentrate light in their vicinity, leading to particularly high absorption in areas near to major recombination centers, like the top surface or the emitter. Designing light-trapping structures that sculpt photon absorption profiles to minimize recombination could also lead to higher open-circuit voltages.

Appendix 1: Experimental Sample Characterization Protocols and Simulation Details

The IV characteristics of the devices were measured using a Keithley 2400 sourcemeter and a 100 mW cm^{-2} solar simulator from PV Measurements with a 1300 W xenon lamp, AM1.5G filter, and a Newport Oriel 68951 flux controller calibrated by an NREL-certified Si reference cell.

Quantum efficiency was measured in 10 nm increments by first recording the photon flux from a Newport Oriel 74125 monochromator using a calibrated Newport Oriel 71675_71580 silicon photodiode connected to a power meter (Newport 2936-R). The current output from the solar cells was measured using the monochromator at the same settings and a Keithley 2400 sourcemeter.

Absorptance was measured using a Newport Oriel 74125 monochromator, a Newport Oriel 70672 integrating sphere, and a calibrated silicon photodiode (Newport Oriel 71675_71580) connected to a Newport 2036-R power meter. Light from the monochromator entered through the topmost port of the 6-port sphere and passed through the sphere before encountering the sample die at the far port, which was angled at 8° using a custom-machined wedge. A custom-designed port with an 8° angle and the same Spectralon® diffuse reflecting coating as the inside of the integrating sphere ensured that photons from high-order reflection modes were reflected into the sphere. The measurement was repeated using a diffuse reflective reference sample (Avian Technologies, FWS-99-02c) to convert the measured signal strength into absolute absorptance. Measurements were corroborated with a specular reflective sample (Thorlabs, PF20-03-G01).

Combined optical and electronic FEA simulation data were provided courtesy of Wei-Chun Hsu and Selcuk Yerci. The simulations use the wave optics and semiconductor modules of COMSOL Multiphysics®. Generation profiles of electron-hole pairs are simulated using the wave optics module and imported into the semiconductor module for electrical simulation using the drift-diffusion model. Standalone optical simulations are run in three dimensions. Optical simulation for use with the electrical model is run in two dimensions, limited by the computational requirements of the electrical model. The cross-section used for simulation is shown in Fig. 39a. Top contact and bottom contact separations are set to 141.4 μm and 52.5 μm, respectively. The width of the top contact is 2.8 μm and that of the bottom contact is 21 μm, with the top contact removed for optical simulation. Total thickness (pyramid-tip to bottom) of silicon is taken as 10 μm with the 700-nm-pitch inverted pyramids etched into the silicon. 100-nm-thick silicon nitride is added on top of the textured silicon. Doping levels are set to: $2x10^{16}$ cm^{-3} (constant) for the p-type body, $2.5x10^{19}$ cm^{-3} (peak, Gaussian profile) for the implanted n^+ region with a junction depth of 500 nm, and $1.4x10^{20}$ cm^{-3} (peak, Gaussian profile) for the implanted n^{++} region with a junction depth of 500 nm. The doping level of the p^+ region is set at $1.4x10^{20}$ (peak, Gaussian profile) for the simulations shown in Figs. 40a-d but is variable in Fig. 39b, with a junction depth of 500 nm.

Appendix 2: Thin-Film Silicon Solar Cell with Integrated Nanophotonic Light-Trapping Structure – Final Process Plan

The process flow given below is designed for the equipment set available in the MIT Microsystems Technology Laboratories (MTL) cleanrooms. The specific tools utilized are listed in the far right column; those shaded red use gold-contaminated equipment, which generally have lower cleanliness standards than the "green" integrated-circuit-caliber equipment. The process begins with a 6" p-type SOI wafer, resistivity 0.5-0.785 Ω cm, purchased from Ultrasil.

	Step description	Details	Tool
1.	Pre-process clean	RCA clean	rca-ICL
2.	Nitride deposition	45nm LPCVD	VTR
3.	Nitride roughening	Use SF_6 with O_2, ~ 5 seconds	LAM490B
4.	HF dip	50:1 HF for 1 minute	acid-hood2
5.	Inverted pyramid lithography	Resist coat (250nm NR7-250P negative resist)	coater
6.		Bake @ 120C for 30 min.	postbake
7.		Exposure (370-390ms, rotate mask 90 degrees, 370-390ms)	i-stepper
8.		Bake @ 105C for 30 min.	varTemp
9.		Develop for ~6 sec in 3:1 RD6:H_2O	
10.		Rinse with DI water and spin dry	
11.	Nitride etch	Use CF_4 with O_2, ~24 seconds for 40nm LPCVD nitride (2nm/sec)	AME-5000
12.	Ash photoresist	2 min.	asher-ICL
13.	KOH etch	80ºC for 3-6 min.	TMAH-KOHhood
14.	Post-KOH clean	2 x Piranha + HF dip	premetal-Piranha
15.	Remove nitride	H_3PO_4 @ 165ºC, 14 minutes	nitrEtch-HotPhos
16.	Clean wafer	RCA clean	rca-ICL
17.	KOH etch nitride mask	280nm	VTR
18.	Backside oxide mask	200nm PECVD oxide	DCVD
19.	Mesa etch lithography	HMDS #3	HMDS
20.		Resist coat (thick resist), spin 1500RPM	coater
21.		Prebake @ 95°C for 60 min.	pre-bakeovn
22.		Exposure for 20 seconds, in 4 x 5 sec. increments (5 sec. pauses)	EV-LC
23.		Develop in AZP 405 for 3 min.	photo-wet-r
24.		Postbake @ 95°C for 30 min.	photo-wet-r
25.	Etch nitride		AME-5000
26.	Ash photoresist	3 min.	asher-ICL
27.	Mesa etch		TMAH-KOHhood

28.	Post-KOH clean	2 x Piranha + HF dip	premetal-Piranha
29.	Remove top nitride	H_3PO_4 @ 165°C, 80 minutes	nitrEtch-HotPhos
30.	Clean wafer	RCA clean	rca-ICL
31.	Implant oxide deposition	100nm PECVD oxide	DCVD
32.	Implant oxide patterning	HMDS #5	HMDS-TRL
33.		SPR700-1.0 resist, ensure full wafer coverage, spin @ 2000RPM	coater
34.		Bake @ 95C for 30 min.	pre-bakeovn
35.		Exposure for 3 seconds	EV-LC
36.		Develop in MF CD-26 for 75 seconds	photo-wet-r
37.		Bake @ 120C for 30 min.	photo-wet-r
38.	Etch oxide	BOE, 30 seconds	oxEtch-BOE
39.	Strip photoresist	Piranha clean	premetal-Piranha
40.	Clean wafer	Modified RCA clean (20 second HF dip)	rca-ICL
41.	Implant oxide growth	30nm oxide, dry O2 @ 1000°C for 24 minutes	5C-FieldOx
42.	Dope junction	Ion implantation (Phosphorus, 110keV, 9E14cm^{-2}, 7° Tilt – Arsenic, 70keV, 2.8E15cm^{-2}, 7° Tilt)	Off-campus vendor (Innovion)
43.	Post-doping clean	2 x Piranha	premetal-Piranha
44.	Clean wafer	Modified RCA clean (15 second HF dip)	rca-ICL
45.	Anneal	60 min., 1000°C	5B-Anneal
46.	Remove implant oxide	BOE, 30 seconds	oxEtch-BOE
47.	Pre-passivation clean	RCA clean	rca-ICL
48.	AR nitride coating	90 nm PECVD nitride	DCVD
49.	Via pattern lithography (top side)	HMDS #5	HMDS
50.		SPR700-1.0 resist, ensure full wafer coverage, spin @ 2000RPM	coater
51.		Bake @ 95C for 30 min.	pre-bakeovn
52.		Exposure for 3 seconds	EV-LC
53.		Develop in MF CD-26 for 75 seconds	photo-wet-r
54.		Postbake @ 120°C for 10 min.	photo-wet-r
55.	Backside window pattern lithography	SPR700-1.0 resist, ensure full wafer coverage, spin @ 1750RPM	coater
56.		Bake @ 95C for 30 min.	pre-bakeovn
57.		Exposure for 3 seconds	EV-LC
58.		Develop in MF CD-26 for 75	photo-wet-r

		seconds	
59.		Postbake @ 120°C for 30 min.	photo-wet-r
60.	Etch backside nitride/oxide	Use SF_6 with O_2	LAM490B
61.	Etch topside nitride/oxide	Use CF_4 with O_2	AME-5000
62.	Remove photoresist	Piranha clean	premetal-Piranha
63.	Top contact pattern lithography (lift off)	Resist coat (NR9-1000PY), spin at 1500-2000rpm	coater
64.		Bake @ 150C for 65 sec.	hotplate
65.		Exposure, 39 seconds (TC Mask)	EV-1
66.		Bake @ 100C for 65 sec.	hotplate
67.		Develop	photo-wet-r
68.	Front oxide etch/clean	BOE dip	acid-hood
69.	Evaporate front contact	Titanium, 40nm	e-beamAu
70.		Palladium, 40nm	e-beamAu
71.		Silver, 1120nm	e-beamAu
72.	Lift off	Acetone, methanol, IPA	photo-wet-r
73.	KOH etch protection	Spin on ProTEK B3 Primer, 1250rpm for 60 sec.	coater
74.		Bake @ 205C for 60 sec.	hotplate
75.		Coat with ProTEK B3, 1250rpm for 60 sec.	coater
76.		Bake @ 140C for 120 sec.	hotplate
77.	Second coat	Coat with ProTEK B3, 1250rpm for 60 sec.	coater
78.		Bake @ 140C for 120 sec.	hotplate
79.		Bake @ 205C for 60 sec.	hotplate
80.	Backside etch	KOH etch, 7 hours @80C	TMAH-KOHhood
81.	Scribe nitride	Using a scribe tool, break off backside nitride crust around etched windows	
82.	Strip ProTEK	Acetone, methanol, IPA	photo-wet-r
83.	HMDS	Recipe #5	HMDS-TRL
84.	Attach carrier wafer	Brush thick resist onto process wafer topside, press carrier wafer into contact, bake at 95C for 45 minutes	
85.	Backside oxide pattern lithography	Pipette SPR700-1.0 resist into each window, spin @ 3000RPM	coater
86.		Bake @ 95C for 30 min.	hotplate
87.		Exposure for 3-4 seconds	EV-LC
88.		Develop in MF CD-26 for 75 seconds	photo-wet-r
89.		Bake @ 120C for 30 min.	hotplate

90.	Back oxide pattern etch	BOE for 250 seconds	acid-hood
91.	Strip resist and remove carrier wafer	Acetone	photo-wet-r
92.	Sputter back contact	Aluminum, 600nm	AJA-TRL
93.	Anneal contacts	In forming gas 500°C, 30 minutes	B1

Appendix 3: Thin Silicon Photovoltaic Fabrication – Lessons from the Cleanroom

The purpose of this appendix is to review some of the critical challenges faced in the experimental process flow given in Appendix 2 and describe the solutions to provide guidance for future fabrication efforts. It is not intended to be comprehensive and does not include many of the hurdles that were overcome in the development of the final process flow. This appendix is organized in sections according to the sequence structure presented in chapter 4.

Sequence 1: Inverted Pyramid Photolithography

- **Problem: Poor adhesion of NR7-250P resist to silicon nitride for sub-micron lithography**

  The first serious difficulty that is encountered in the process flow – and one of the most intractable problems to solve – is poor adhesion to LPCVD silicon nitride of the NR7-250P photoresist. The adhesion issue manifests itself during the development step when forming the two-dimensional periodic array of sub-micron holes in photoresist. (The author typically used a 3:1 or 4:1 concentration ratio of Futurrex developer RD6:H_2O for a develop time of approximately 10 seconds.) Almost as soon as the sub-micron hole pattern begins to develop out (evidenced by an iridescent appearance of the exposed dies), the pattern rapidly disappears as the resist sloughs off.

  Solution: The origin of poor adhesion between the photoresist and the nitride film is not well understood. A wide variety of solutions were attempted to address the problem by manipulating the nitride surface chemistry and roughness, including the use of solvent cleans, short exposures to oxygen plasma, harsh piranha cleans, treatment with varying

Table A3.1: Solutions attempted to address poor photoresist adhesion during photolithography for pyramid structure fabrication

Trial solution	When applied	Notes
Acetone, methanol, IPA clean	Prior to spin-coating	No observed improvement in adhesion
Oxygen plasma (5 min.)	Prior to spin-coating	No observed improvement in adhesion
Piranha clean (10 min.)	Prior to spin-coating	No observed improvement in adhesion
Hydrofluoric acid dip (>1 min.)	Prior to spin-coating	Observed improvement in adhesion, though inconsistent
Roughening etch (SF_6/O_2 plasma ~ 5 seconds)	Prior to spin-coating	Inconclusive impact on adhesion
Increase bake temperature from 100 °C to 105 °C	Post-exposure bake	Improved adhesion observed

concentrations of hydrofluoric acid, and short roughening etches (see Table A3.1). Alternative bake times and temperatures and developer concentrations were also trialed.

The author has strong empirical evidence that an HF dip prior to spin-coating the wafer is a critical step to enable better photoresist adhesion. The mechanism by which the HF dip improves adhesion is unknown, but it is hypothesized that it either serves to 1) functionalize or otherwise modify the nitride surface chemistry to improve bonding to the photoresist or 2) roughen the nitride surface and thereby increase the area available for adhesion. The process developed to improve the photoresist adhesion consists of a brief (5 second) dry etch using a sulfur hexafluoride (SF_6) and oxygen chemistry to intentionally roughen the nitride surface followed by soaking in 20:1 HF for one minute. These preparation steps, though they have worked very well in some instances, are far from a silver bullet and typically require several trials with a given wafer before achieving usable results.

- **Problem: Uniform patterning of a large area (2 cm x 2 cm) with sub-micron holes in photoresist**

The formation of a two-dimensional periodic array of sub-micron holes in photoresist over a large area is a particularly mercurial process step when using projection lithography, with variation in the size of holes not only within a die, but also from die to die and wafer to wafer.

Solution: In the process presented here, the problem of variability in the production of sub-micron holes in photoresist was never completely resolved, but it was wrested under control. In order to facilitate mask design at a reasonable price, a one-dimensional grating mask (2 μm chrome lines on a 3.5 μm pitch) was used to produce a two-dimensional array of holes in negative photoresist by rotating the mask 90 ° between two successive exposures. In retrospect, the extra time and money spent to produce a two-dimensional grating mask would likely make a significant improvement in the uniformity of the resulting pattern; the author would recommend the latter approach.

Variability in the pattern output for pyramid lithography was observed over a range of temporal and spatial scales. At the finest scale is variability between the diameter of holes within individual dies (see Fig. 23). The largest diameter holes are generally found in the middle of a die and are relatively consistent over much of the die area. Toward the edges, the diameters shrink markedly until the holes disappear completely. A representative comparison can be seen in Fig. A1. The origin of the problem is not well understood, but is likely rooted in the light field of the stepper and the wavelength-scale, periodic nature of the pattern. Locating each 1 cm^2 solar cell in the center of a 2 cm x 2 cm patterned area mitigated the problem.

Significant variation in pattern results for a given exposure time was observed between trial runs spaced several months apart in time. The exposure time required using the i-stepper to produce a satisfactory exposure increased from around 700 ms (two exposures of 350 ms with the mask rotated 90 ° between rotations) to about 760 ms (2 x 380 ms) by the end of the project. As a result of this variability, the proper exposure time needs to be confirmed before each new run. In Fig. A2, examples are given of underexposed and properly exposed photoresist for the inverted pyramid photolithography process, while Fig. A1b is an example of overexposed negative resist.

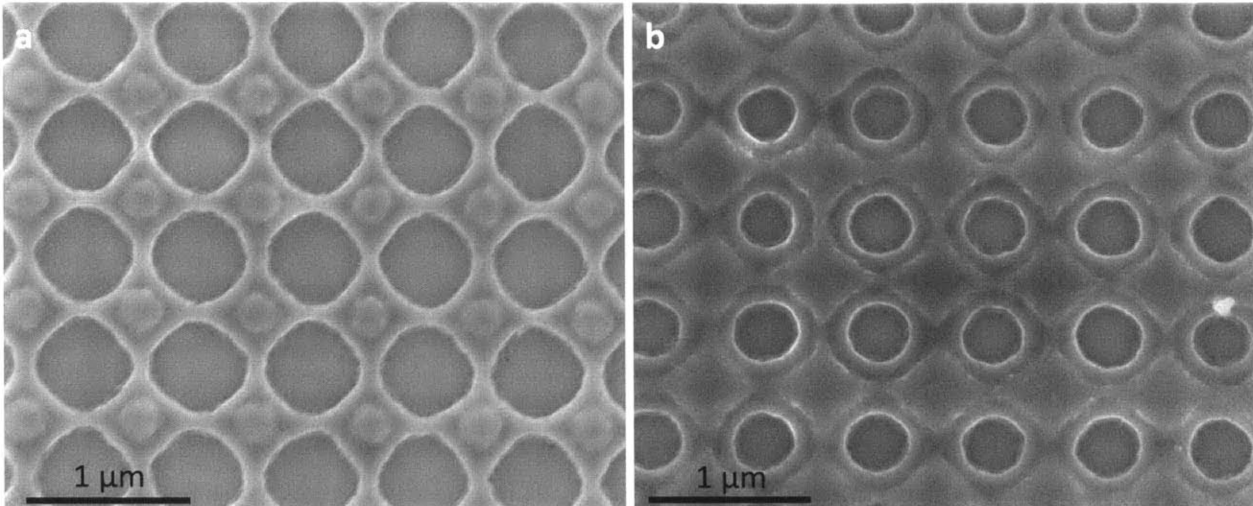


Figure A1 | Variation of projection photolithography results within a die. a, b, SEM images of exposed and developed photoresist for inverted pyramid photolithography. The resulting holes are larger in the center of a die (**a**) than at the edge (**b**).

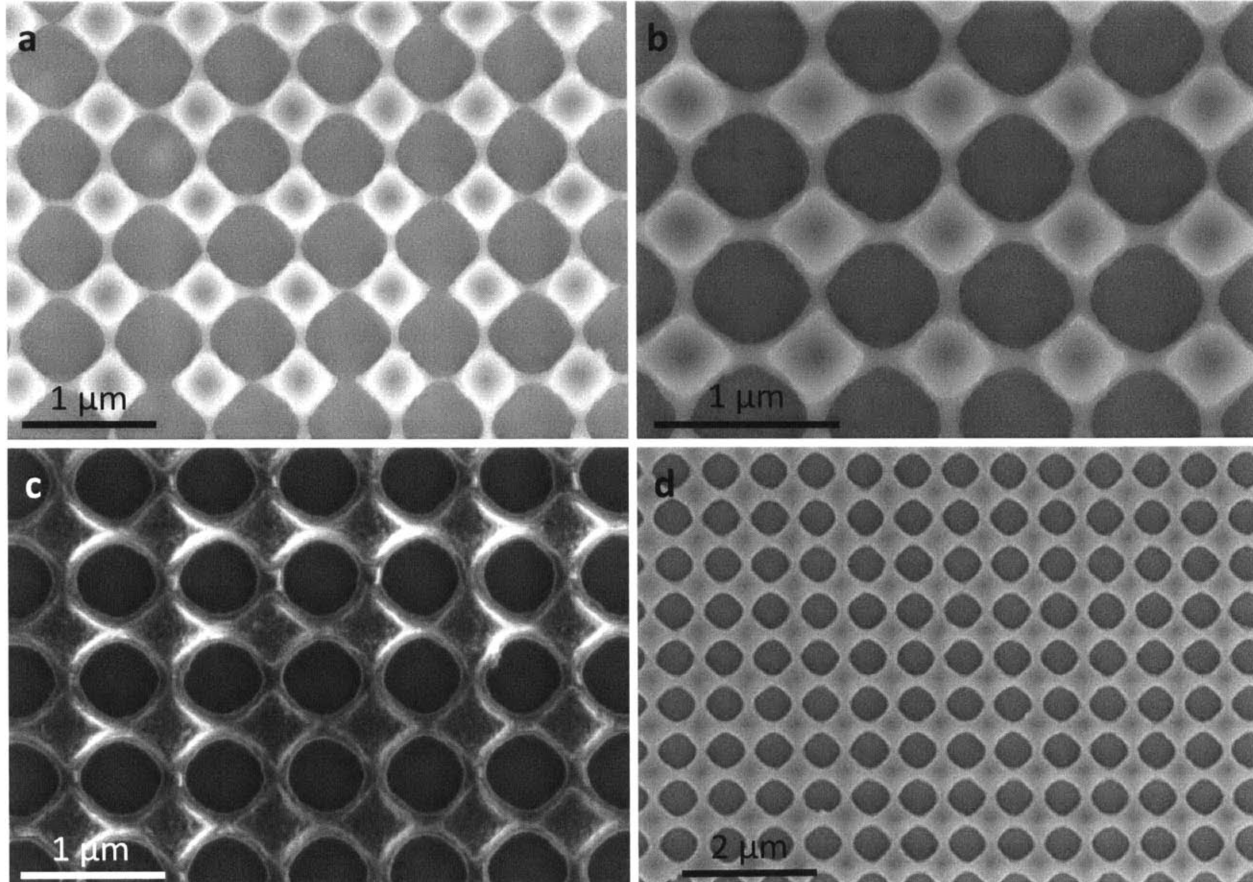


Figure A2 | Sample inverted pyramid photolithography results. a, b, c, d, SEM images of (**a, b**) underexposed and (**c, d**) properly exposed photoresist at the conclusion of the photolithography process described in Sequence 1.

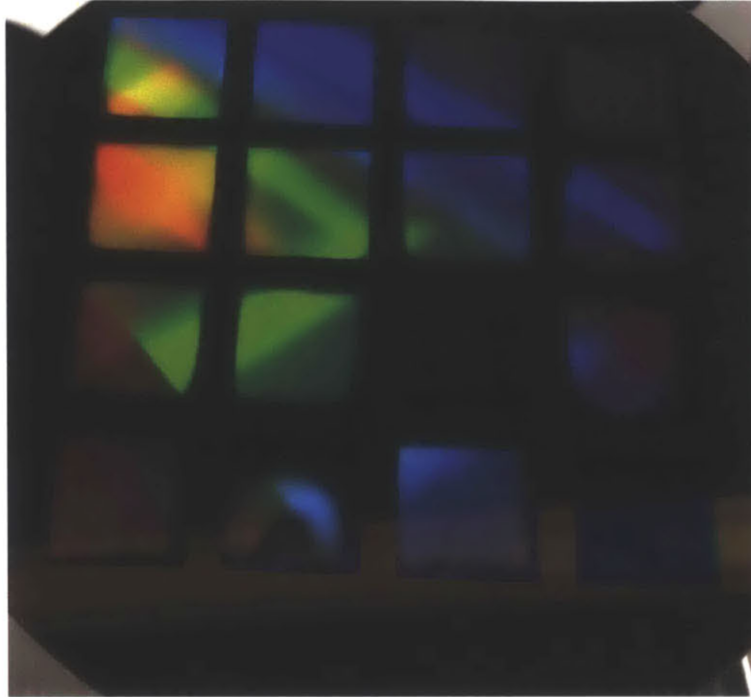


Figure A3 | Aberrant patterns resulting from projection lithography for inverted pyramid formation. Photographic image of a wafer following inverted pyramid photolithography, with 16 – 2 cm x 2 cm dies of patterned photoresist. Inexplicable patterns often materialize, such as the swirl of properly exposed photoresist surrounded by overexposed resist shown here in die 14 (dies are numbered from left to right, top to bottom). Dies 11 and 16 are intentionally overexposed.

In addition to intra-die and run-to-run variation, the projection lithography process for sub-micron periodic structures also has the tendency to yield zany, completely inexplicable results such as the swirl of overexposed photoresist shown in Fig. A3.

- **Problem: Loss of wafer yield owing to defects in photoresist during pyramid photolithography**

  Defects in the coating of photoresist (e.g., pinholes, bubbles or scratches) will result in holes etched through the silicon device layer down to the buried oxide during inverted pyramid etching with KOH. Such defects lead to sharp reductions in the survivability of individual dies.

  Solution: During the photolithography process, care must be taken to minimize defects in the photoresist, particularly during coating. If an excess of defects are visible under optical microscope in the areas where devices will be located, the resist should be rinsed off in piranha and the process restarted.

Sequence 2: Inverted Pyramid Surface Texture

- **Problem: Minimizing pyramid ridge width during the anisotropic KOH etch**
  Optical performance of the top surface texture is maximized when the width of the planar ridge separating one pyramid from another is minimized. However, there are a multiplicity of variables that make it extremely challenging to repeatably and precisely deliver ridge widths thinner than 50 nm during the KOH etching process.

  Solution: Given the variation in the diameter of the holes in nitride produced during the pyramid lithography and nitride etch process, it is necessary to adjust the length of the KOH etch from run-to-run and wafer-to-wafer. This is a time consuming process and one of the major advantages of moving to larger pyramid sizes (Section 6.3). Generally, an SEM is used to observe the space separating holes produced during photolithography, and etch times are extrapolated accordingly. Even this approach is not fool-proof, given that an SEM can image with high resolution an area containing about sixteen holes at a time – or 1.9×10^{-6} % of the roughly 816,000,000 holes in a 2 cm x 2 cm die. The significant intra-die and die-to-die variation mandates a conservative approach, because the penalty of overetching is that the pyramids merge and the pattern collapses. A small number of pyramids merging is normal and acceptable; a large number will ruin a die.

  The strategy used by the author to calculate KOH etch time was to image a representative area in the center of a sample die and identify the thinnest width separating two holes in photoresist (Fig. A4). Then an etch time is calculated by assuming a rate of etching of the pyramid ridge width – that is, the rate at which the ridge separating two pyramids shrinks – in KOH at 80 °C of ~ 25 nm/sec and adding an extra minute to account for the initial pyramid formation pyramid. For example, the etch time used by the author for the diagram in Fig. A7, using a minimum separation of 150 nm, would be:

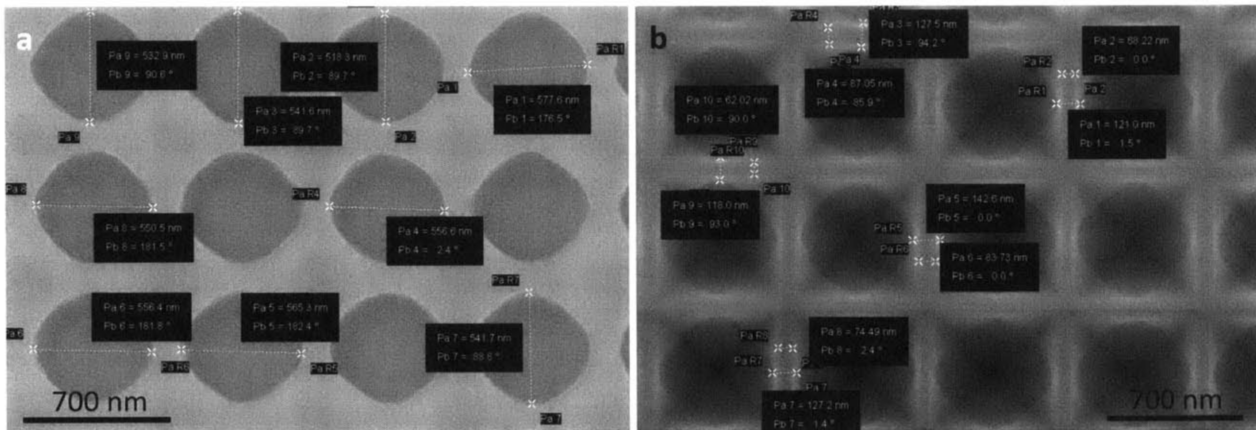


Figure A4 | Calculating KOH etch times and rate. **a,** Sample SEM mark-up used to calculate the appropriate KOH etch time by estimate the initial hole diameter. **b,** SEM image of a KOH-etched surface prior to removing the silicon nitride, which can be used to estimate the actual KOH etch rate by comparing the difference in nitride hole diameter with the remaining ridge width (Eq. A1).

$$t_{etch} = \frac{150\,nm}{25\,nm/s} + 60s = 7\,minutes$$

(A1)

Unfortunately, the pyramid etch is not a step that can be redone in the case of failure. Efforts to narrow the ridge width after an initial etch leaves it too large were unsuccessful. Once the wafer has been etched and dried, the holes in the surface nitride trap air in the inverted pyramids, preventing access of the KOH etchant to the inverted pyramid.

Sequence 3: Mesa Isolation Structure

- **Problem: Loss of wafer yield owing to defects in photoresist during mesa photolithography**

  The photolithography for etching the mesa structure is a critical one to maintain yield. As with the pyramid lithography process described in A3.1, defects in the photoresist coat (e.g., pinholes, bubbles or scratches) will result in the etching through to the buried oxide during the KOH mesa etch. Such defects lead to sharp reductions in the survivability of individual dies by initiating catastrophic tears in the thin silicon film after membrane formation in Sequence 10.

  Solution: At this point in the process, the wafer surface has taken on significant topographical variation owing to the pyramidal texture covering the sixteen dies and also the large step change in height at the edge of each die. (A consequence of using negative photoresist in Sequence 1 is that, during the pyramid lithography/nitride etch, areas off the 2 cm x 2 cm die are not masked with resist and the KOH etches away a significant thickness of silicon.) The variable topography makes it challenging to uniformly coat the wafer surface with photoresist, which is all the more problematic because of the yield ramifications of defects in the photoresist coat.

  Thick photoresist is used in this step of the process in an effort to properly coat the wafer surface. Results were improved by double-coating the wafer with photoresist, but photoresist coating individual dies should be inspected and the wafer stripped and re-coated in the advent of excess defects.

Sequence 5: PN-Junction Implantation and Annealing

- **Problem: Accidental stripping of the buried oxide layer to expose the handle wafer**

  During the HF dip of the RCA clean prior to diffusion, as well as during the first two steps of Sequence 6, there is a risk of etching through the buried oxide layer exposed during the pyramid/mesa etches. The risk is enhanced because heavily implant-damaged oxide etches very quickly, even in dilute (50:1) HF (the author observed 50:1 HF rates of implant-damaged oxide up to 1 nm sec^{-1}).

Solution: To eliminate the risk of removing the insulating buried oxide (without which the top metal contacts could short to the back contact through the p-type handle wafer), an additional PECVD oxide film was deposited over the wafer surface and patterned to open up the solar cell dies. This step is not shown in the final process plan (Appendix 2) because it is optional; in reality, the PECVD nitride ARC that covers the whole wafer, combined with any remnant buried oxide should provide sufficient insulation for the handle wafer.

Sequence 8: Backside Window Etch

- **Problem: Defects etched into the backside silicon nitride lead to damage during the KOH etch that can result in broken wafers**

  Areas on the back of the wafer outside of the 16 defined dies that have defects in photoresist or nitride coverage will be attacked by KOH in the membrane formation step (Sequence 10), resulting in a more fragile wafer that can be prone to splitting.

  Solution: The risk of unintentional damage by potassium hydroxide etching areas outside of the dies was mitigated by painting photoresist over defective regions of the original photoresist coat.

Sequence 9: Top Contact Metallization

- **Problem: Unwanted metallization is difficult to remove during lift-off**

  In certain places on a wafer surface – most commonly in areas with significant change in surface height such as at the edge of dies – the evaporated metal tends to stick and lifts off only partially.

  Solution: Unfortunately, the removal of metal from the wafer surface via lift-off is a painstaking task, particularly given the highly variable surface topography. After experimenting with sonication and finding only limited success, the author found that the most reliable approach to removing the undesired metal is to use tweezers while avoiding scratching the surface. The relative thickness of the metal film makes peeling fairly easy, whereas sonication leaves fragmented traces behind that are very difficult to dislodge. Before peeling, one should first allow the wafers to sit in acetone overnight (a few hours is not sufficient) to dissolve the photoresist under the largest areas of metallization. Also, it would be worthwhile to experiment with a thicker lift-off resist than the ~1.4 μm coating of NR9-1000PY used here.

Sequence 10: Membrane Formation

- **Problem: Excessive peeling or KOH penetration of the Pro-TEK film**

  As described in Section 4.10, there are two common sources of KOH damage to the Pro-TEK coated wafer surface: 1) peeling of the ProTEK from the top surface,

beginning at the edges of the wafer, and 2) pinhole defects that allow KOH access to the wafer surface.

Solution:

1. Do not use Pro-TEK that is more than a few months past its expiration date. The adhesive quality of the material seems to degrade with time, which can lead to large-area peeling when immersed in KOH.
2. As described in Section 4.10, minimize the presence of metal shards on the wafer surface. These fragments allow KOH access to the wafer surface, which reacts and generates bubbles to cause additional peeling of the Pro-TEK and eventual damage to individual dies. In some cases, the author first coated the wafer with Pro-TEK, cured the Pro-TEK into a hardened film that could then be mechanically peeled to remove any stubborn pieces of metal from the wafer surface, and then re-coated the wafer with a fresh Pro-TEK film.
3. A double coat of Pro-TEK is necessary to ensure coverage of the varying topography of the wafer surface. However, NEVER USE A TRIPLE COAT OF PRO-TEK!!! The residual stress in a triple coat is strong enough to cause it to auto-peel upon drying after the KOH etch. In the process, all of the newly-formed membranes will be ripped out, and five weeks of work will be lost. I know because that happened to me.

- **Problem: Solar cells tear during Pro-TEK removal**

Upon placing the wafer with newly-minted membranes in acetone, dies tear out of the substrate.

Solution: Unfortunately, at this point in the process there is not anything that can be done to minimize the loss of yield that occurs in this step. The tearing arises from defects that are etched through the silicon device layer either during the KOH etches for formation of the inverted pyramids and mesa structure (Sequences 2 and 3) or during the membrane formation KOH etch itself. Care must be taken to minimize the creation of defects in the device layer at earlier steps in the process.

Sequence 11: Pattern Back Oxide

- **Problem: The photolithography for back oxide etch yields hole diameters that vary widely**

The significant (500 μm) distance between the photomask and back oxide surface to be patterned – on the underside of the membrane – makes photolithography for the back oxide etch very challenging. Diffraction dramatically distorts the optical image over such a large distance, rendering precise pattern transfer impossible. Moreover, complications arising from diffraction become exponentially worse as the size of the features shrink, making it hard to generate the very small (5-10 μm diameter) point contacts that are desired while also maintaining a pitch smaller than 100 μm. Finally, the photoresist application method used here (spin-coating after pipetting resist into each

well) leaves large variations in resist thickness within a die and from die-to-die, further complicating the effort to produce uniform, small hole diameters.

Solution: Properly patterning the contact hole array in the back oxide requires several engineering trade-offs. First, the photomask was designed with relatively large point-contacts – squares 25 μm on a side – to minimize the severe diffraction encountered with squares 12 μm on a side that could at times cause the entire pattern to wash out (note that 25 μm is not an optimized value, but it works well).

Secondly, the mask pattern is designed with two periodicities: a sparse array of contact holes rings the edge of the die while a denser array of point contacts populates the remainder. The edges of the dies, particularly on the upstream side of the spin-coating flow, often have thin photoresist coverage. The thin areas of positive result in much larger hole diameters – and in some cases even complete pattern removal – when using more densely-spaced patterns.

Finally, exposure time has a significant impact on the resulting photoresist hole diameter. With positive photoresist, an exposure time above par is necessary to deliver satisfactory results; the 3.5 second exposure for SPR700-1.0 that the author found to be ideal is about twice as long as a standard recipe.

- **Problem: After separating the device wafer from the carrier in acetone, the top contact metals and nitride ARC are occasionally found to have been attacked by BOE**

Damage to the surface layers of the device will occur if BOE infiltrates the gap between the carrier and device wafers during the back oxide etch. Once there, it is virtually impossible to remove until the wafers are separated, by which point the damage to the devices is irreversible.

Solution: The first chance to address this problem comes when attaching the device wafer to a carrier. In the process flow presented here, a carrier wafer is attached to the device wafer by first painting thick photoresist (AZP 4620) on the top side of the device wafer and then bringing the carrier wafer into contact before baking. In order to reduce the likelihood of BOE coming into contact with the devices, photoresist is painted in such a way as to "wall off" the area around each device (i.e., a ring of photoresist is painted around the edge of the wafer, as well as around each broken device).

Second, immediately before the BOE etch the wafers should be placed in DI water for a short period of time, allowing water to fill the air gap between the carrier and device wafer. During the subsequent etch, BOE can then access the dies only by diffusion, since the narrow dimensions limit mixing by flow. In the opposite case where the wafer is first placed in BOE, the etchant floods the spacing between the wafers and cannot be flushed out until the two wafers are separated. However, with proper photoresist coverage and a DI water dip before etching, yield loss owing to incidental exposure of the top surface to BOE can be eliminated.

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