

OPTIMIZATION OF A RESIN CURE SENSOR

by

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ABSTRACT

The low frequency dielectric properties of epoxy resins can provide information about the extent of polymerization as the curing reaction proceeds. Mechanical quantities such as viscosity and dipolar relaxation times can also be inferred from these measurements. The "microdielectrometer chip," a device used to obtain dielectric data, is an integrated circuit sensor consisting of a planar interdigitated capacitor with a pair of matched FET's to provide on-chip amplification. Its size allows measurements to be made either with a few milligrams of resin for laboratory experiments, or by embedding the device in larger structures.

This thesis reports on a generalized method of finite difference simulation used to solve Poisson's equation for lossy dielectrics in the sinusoidal steady state. The simulation allows calculation of the microdielectrometer's response in dissipative media, enabling calibration of different electrode geometries and the extraction of quantitative dielectric information from raw gain-phase data. Testing of the calibration was performed with sensors fabricated by a double-level metal process. Electrode height above the substrate, and therefore device geometry, was systematically varied by selecting the thickness of a polyimide insulating layer between first- and second-level metal.

Experiments were performed with the reaction of diglycidyl ether of bisphenol-A and the curing agent meta-phenylene diamine (DGEBA/MPDA), using sensors having electrode heights of 0.45, 0.85, 1.66 and 2.15 microns above the ground plane. Good agreement of dielectric data was obtained among all

device geometries tested, confirming the correctness of the calibration procedure. After extraction from loss factor measurements, the time dependence of the low-frequency AC conductivity for the curing DGEBA/MPDA resin agreed well with published data, and demonstrates the sensor's utility as an alternative to parallel plate geometries for dielectric and conductance measurements.

A consistent gain offset of approximately -1 dB from the origin at the beginning of cure has been observed, with the conclusion that it is a real feature of the curing DGEBA/MPDA system and results from a blocking layer between the electrodes and resin. Analyses of electrode polarization and discharge effects, which can produce such blocking layers, has shown that the space-charge contribution causes apparent permittivity and loss factor to depend on frequency, with a single relaxation time, according to the Debye dielectric dispersion equations.

It has been concluded, therefore, that the dominant electrical feature of curing DGEBA/MPDA resin is a simple, initial decrease in bulk conductivity, until it is small enough to reveal dipole relaxation in the form of an AC loss peak. Further monitoring of the resin results in the observation of increasing dipole relaxation time until the end of cure.

A diode temperature sensor was incorporated into the design of the experimental chip. Preliminary tests indicate that it should be accurate to at least 2 °C over the range from 20 °C to 150 °C.

A parasitic resistance in the substrate was determined to cause positive phase shift in data due to modulation of transistor current by the body effect. The effect of threshold voltage and transistor gain mismatches were assessed, and an optimized resin cure sensor was designed to reduce the effects of processing variations, device mismatches, and parasitic elements.

Thesis Supervisor: Stephen D. Senturia
Title: Professor of Electrical Engineering

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CHAPTER 1 INTRODUCTION

1.1 Historical Perspective

During cure, the dielectric properties of resins and other polymers can change greatly, reflecting the altering physical and chemical states of the material. The ability of integrated circuit sensors to monitor dielectric permittivity and loss factor has many potential applications for "in situ" measurements of these processes. Such devices are small and can remain embedded in a finished article for long term monitoring, or be used for non-destructive testing and manufacturing control of individual components.

A sensor of this type is the charge-flow transistor, or CFT [1],[2] originally developed by Senturia and co-workers to monitor the sheet resistance of thin films, both for use as chemical gas sensors and for fundamental studies of the film's electrical properties. The early CFT, as illustrated in Figure 1.1, was an enhancement field effect transistor with the metal removed from part of its gate, and replaced by a polymer film. Ordinarily an FET turns-on immediately after the application of a gate voltage exceeding its threshold voltage. CFT operation, however, depends on the finite time required for charge to flow through the highly resistive polymer before fully inducing a

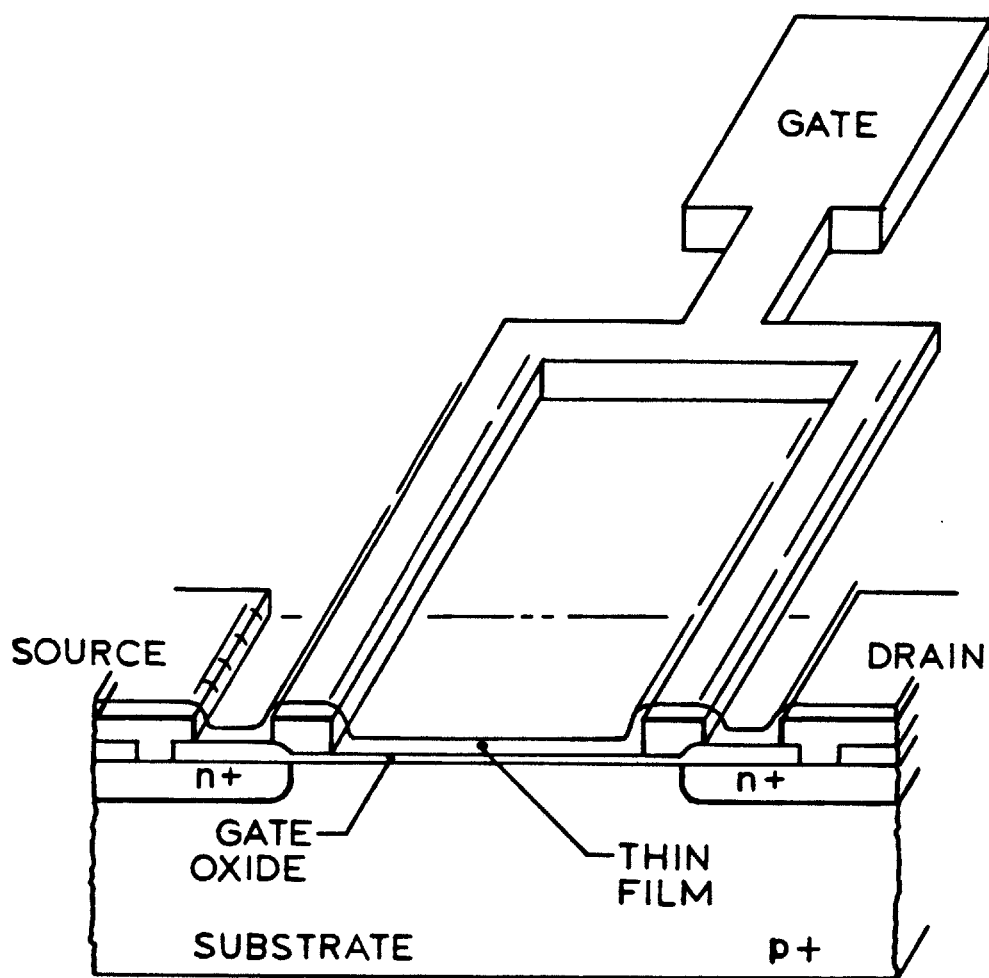


Figure 1.1 Cross-section of Original Charge-Flow Transistor

channel beneath the gate. This delay is a function of sheet resistance, and if this electrical quantity varies with the ambient, then the device is environmentally sensitive. Use of a charge-flow transistor to monitor the changing dielectric properties of curing resins was first proposed by Dr. L. H. Peebles Jr. of the Office of Naval Research [3], and later demonstrated to be feasible by H. R. Appelman in an undergraduate project [4]. Senturia, Sheppard, Poh, and Appelman continued the work, and subsequently devised an RC lumped element model to describe qualitatively the data they obtained [5].

The nonlinearities of the CFT response made quantitative modeling difficult, and led to Senturia's development of the floating gate CFT and its differential measurement system [1],[6]. Charge flow in this configuration occurs between a pair of interdigitated electrodes, one driven and one floating, with the FET channel conductance responding only to the potential on the floating electrode.

Sheppard [7],[8] incorporated the floating gate CFT in experiments to monitor the cure of resins, and designed a computerized system for automated data acquisition. The word "microdielectrometry" was coined to describe this application of the charge-flow transistor. At first an RC transmission line model [7] was used to infer the real and imaginary components of the resin's complex dielectric

constant, i.e. the permittivity and loss factor. The calculations, though, relied on a semi-empirical "thickness parameter" that failed in detail. A preliminary version of the two-dimensional simulation described in this thesis was used to calculate the sensor's response in lossy dielectrics [9]. It was then possible to correlate changes in the resin's permittivity and loss factor with similar changes in relaxation time and viscosity, and to show the applicability of microdielectrometry in the study of thermosetting plastics.

1.1 Summary of this Work

This thesis describes the use of a generalized method of finite difference calculation which treats potentials in lossy dielectrics as phasors coupled by Poisson's equation. A full two-dimensional simulation of the floating gate CFT has been used to determine its sinusoidal steady state transfer function when the resin-electrode system has arbitrary loss. Computation of the response over a range of permittivities and loss factors can generate tables which calibrate the CFT geometry being modeled. In this way, calibration curves were obtained for a series of four devices used in subsequent experiments. The sensors had electrode-ground plane separations of 0.45,

0.85, 1.66 and 2.15 microns, and represent a broad selection of device geometries.

The sensors were fabricated with a double-level metal process employing polyimide as an inter-level insulator. Increasing electrode height above the substrate with an additional dielectric layer increases sensor gain by reducing electrode coupling to the ground plane. In addition, polyimide passivates the transistors of the microdielectrometer and, with proper passivation of the bond wires, eliminates the spurious conduction path reported by Sheppard [8].

To test the calibration across a wide range of permittivities and loss factors, the isothermal cure of an epoxy resin-amine hardener was monitored, using the series of four devices. The material studied was diglycidyl ether of bisphenol-A with meta-phenylene diamine (DGEBA/MPDA), which is a well characterized commercial epoxy, and the same one used by Sheppard in his experiments. The dielectric data obtained during the cure agreed well between all sensors, indicating that the calculated calibration correctly accounts for variations in device geometry.

Chapter 2 of this thesis provides background material on the microdielectrometer chip and measurement system. Chapter 3 presents the theory of the complex-potential finite difference method used to simulate the resin-sensor

system, with a description of the program algorithm and a discussion of computation speed and error criteria, device calibration and limitations. Chapter 4 describes the design of the microdielectrometer chip used in the experiments, discussing the use of polyimide as an inter--level insulator. Chapter 5 describes the experimental work and raw data, and then presents the dielectric information extracted from calibration curves generated with the finite difference simulation. The correlation between different devices and experimental conditions is discussed, and the effects of various offsets and parasitics evaluated. Finally, Chapter 6 presents the conclusions; the optimized sensor, which was designed with consideration of various parasitic effects; and the direction of possible future work.

CHAPTER 2 BACKGROUND

2.1 Microdielectrometer Chip and Measurement Circuit

The original microdielectrometer chip was designed by Garverick [6],[10] and first used for studying the sheet resistance and electrical properties of thin films. The sensor is an integrated circuit with a pair of interdigitated electrodes, one completely surrounding the other and serving as the input for voltage signals. The inner electrode forms an extension to the gate of a depletion field effect transistor. This array, more descriptively called a "lock and key," is illustrated in Figure 2.1. In addition to the sensor itself, the chip has a second, identical transistor which is the reference device for a differential measurement technique.

A section across a pair of electrode "fingers" is shown in Figure 2.2. The lock and key is separated from the silicon substrate by a dielectric insulator, which is silicon dioxide in the original Garverick design. The sample to be studied fills the space above the lock and key and forms a semi-infinite medium. The electrodes comprise the plates of a planar capacitor, above a ground plane, with the resin as one component of the inter-electrode dielectric. Since the inner electrode is electrically isolated and floating, and modulates the transistor's

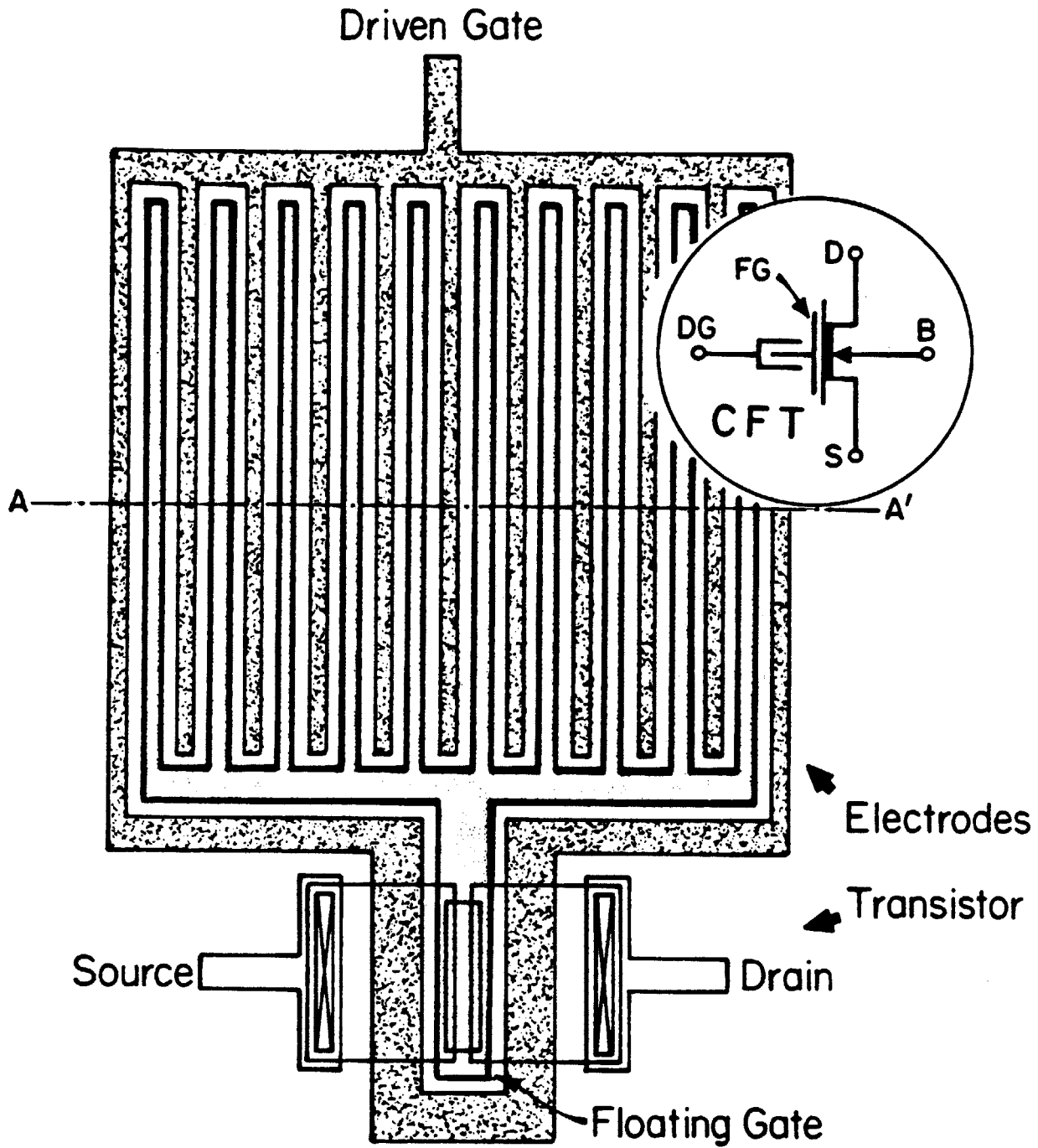


Figure 2.1 Top View of Sensor Portion of Microelectrometer Chip

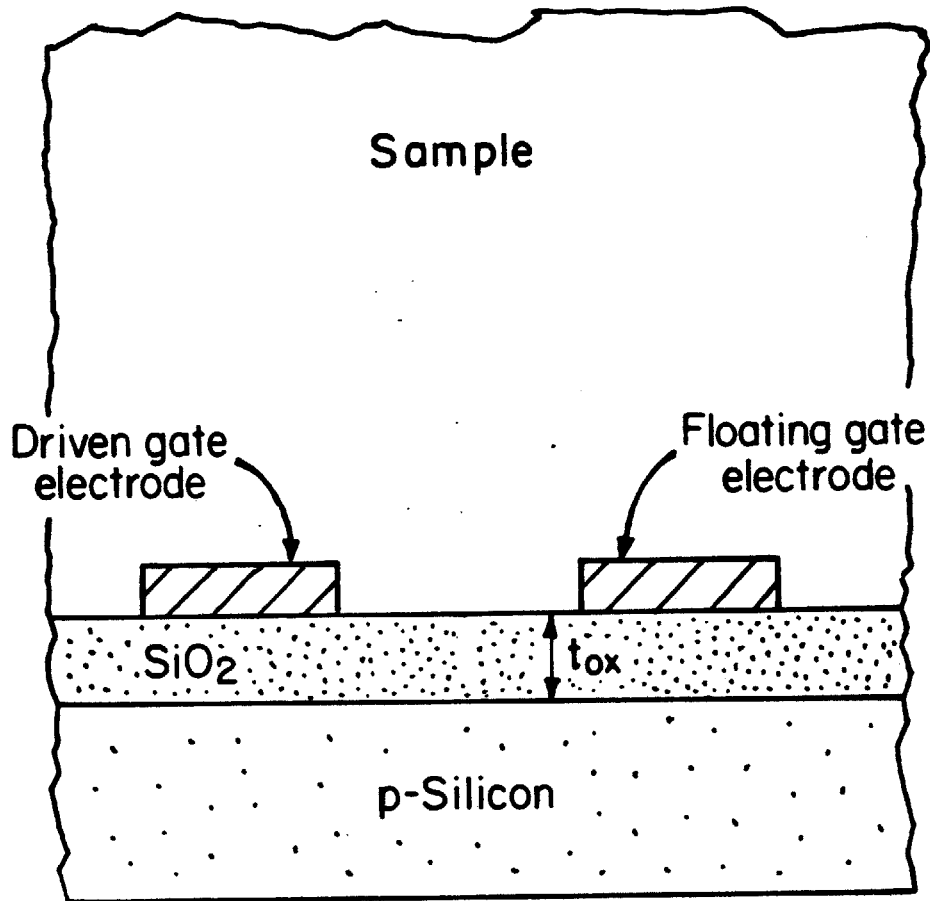


Figure 2.2 Cross-section of Lock and Key Structure

channel conductance, it is called the floating gate. The outer electrode is the driven gate, and the entire lock and key structure with transistor is a floating gate CFT.

The sensor operates by measuring the lock and key's output response to an input signal. When a sinusoidal voltage is applied to the driven gate, an AC current with conduction and displacement current components flows through the intervening medium to the floating gate. The capacitance between the floating gate and ground collects this current and develops a voltage which is attenuated in amplitude and shifted in phase relative to the input sine wave. The transfer function depends on electrode width, spacing and height above the ground plane; on resin permittivity and loss factor; and on load admittance, the additional capacitance to ground due to the CFT. With all geometric quantities fixed, only the resin's changing dielectric properties affect the signal reaching the floating gate. Although it cannot accurately describe distributed admittances, Figure 2.3, the lumped element model of the resin-electrode system, can provide insight into the lock and key's overall behavior. C_{12} and R_{12} represent the coupling through the medium between the driven and the floating gate. The C_{11} associated with the floating gate represents the electrode capacitance-to-substrate whose voltage controls the FET.

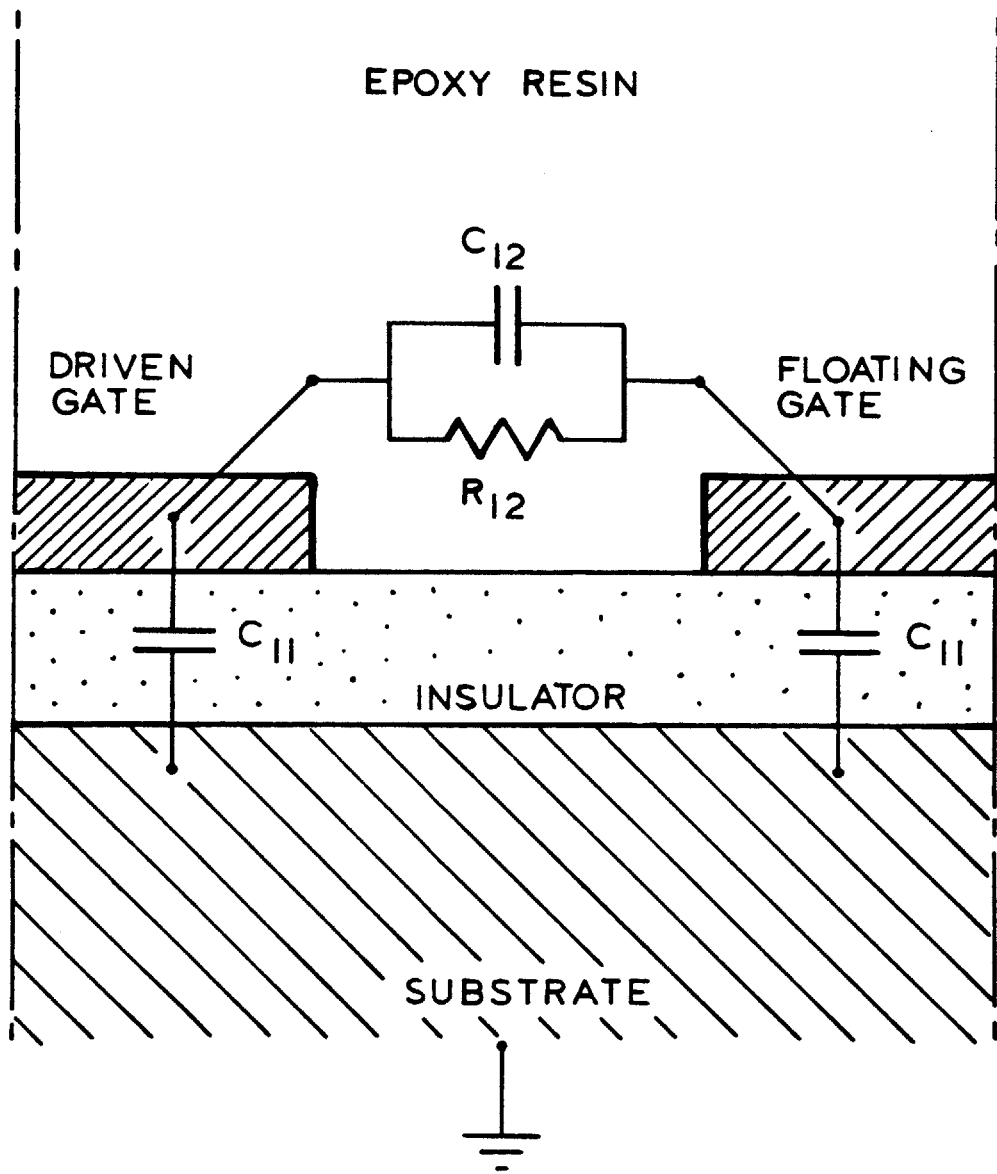


Figure 2.3 Lumped Element Model of Resin-Electrode System

The CFT's transconductance converts the floating gate voltage to a similarly modulated source current, effectively amplifying the charge flow by approximately one million. Direct measurement of this CFT current can be used to calculate the gate voltage, but accurate knowledge is required of transistor geometry, threshold voltage and gain. These parameters, however, differ from chip to chip due to normal random processing variations. In addition, the dependence of transconductance on pressure and temperature may not be determinable. Instead, a differential measurement scheme is employed using a reference FET. The feedback circuit of Figure 2.4 is a current comparator which adjusts the reference device's gate voltage to match its source current to that of the CFT.

The proximity of the transistors to one another insures matching of process-dependent characteristics like threshold voltage, channel doping and carrier mobility. If the physical dimensions of the two devices are identical, and their source voltages and drain voltages are the same, then if they carry the same drain currents, their gate voltages should also be identical. The reliability of measurements with the sensor critically depends on this matching. If the CFT and FET geometries or threshold voltages are not the same, then the feedback circuit, in trying to equalize drain currents, will introduce a DC

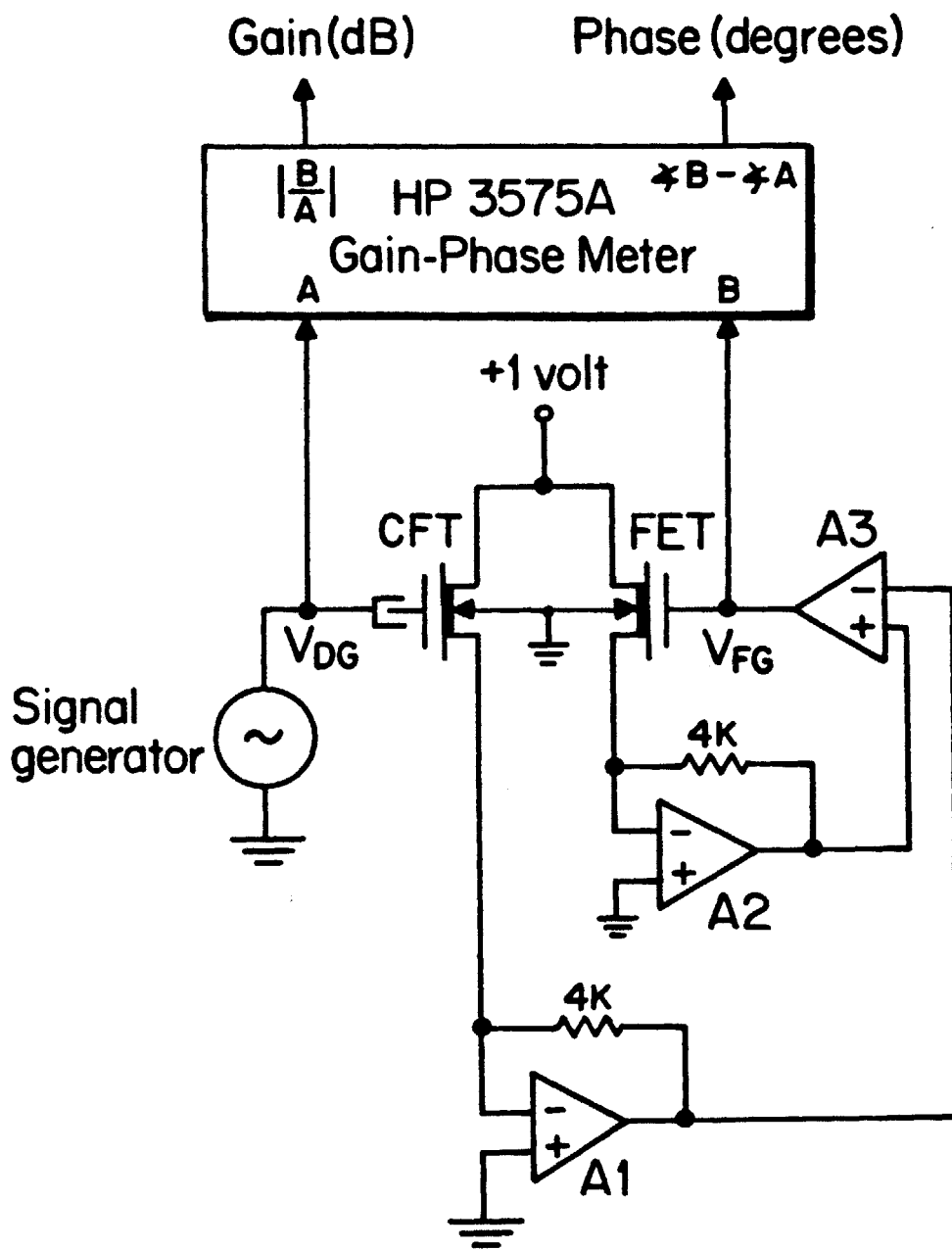


Figure 2.4 Microdielectrometer Interface Circuit

offset between the quiescent gate voltages of the two devices. With different operating points, and the mismatching, the transistors will have different transconductances. Depending on the nature of this mismatch, the feedback circuit will add to all data an AC gain offset which can be either positive or negative. In the Garverick design this error varies between -1.6 dB and +1.2 dB [8], and represents a considerable uncertainty in experimental measurements.

As a result of the differential measurement technique, the output is a buffered reading of the CFT's floating gate signal, which is measured by the HP-3575A gain/phase meter as a gain and phase relative to the driven gate voltage.

2.2 Data Acquisition System

An important function of the data acquisition system employed in this work is the ability to convert raw gain-phase information to dielectric permittivity and loss factor. An HP-1000 minicomputer has performed a full two-dimensional finite difference simulation of the lock and key to generate calibration tables for each of the sensor geometries used in later experiments. FORTRAN programs for use on the HP-1000 were written to interpolate

data and perform other tasks associated with data manipulation and calibration.

The automated data acquisition system assembled by Sheppard [7],[8], and shown schematically in Figure 2.5, is designed to conduct and monitor resin cure experiments without the need for constant human supervision. One of the major components is an HP-85 desktop computer, which serves as the system controller. During an experiment, it records gain-phase data at periodic intervals and controls an HP-6940B multiprogrammer data acquisition module. Other components are an HP-59500 interface, an HP-3325A function generator, an HP-3575A gain/phase meter, plug-in circuit cards with an analog/digital converter for the multiprogrammer, and the interface circuit of Figure 2.4.

The system uses an Analog Devices AD-590 PTAT temperature sensor, but can be adapted to use the temperature sensor integrated on the redesigned microdielectrometer chip, described later in this thesis.

Software written for the system allows the user to select a series of input signal frequencies, the number of readings to be taken and the time between readings. The HP-85 thereafter controls the experiment, simultaneously printing on paper tape and recording on a cassette the data obtained. A stored look-up table of the microdielec-

MEASUREMENT SYSTEM

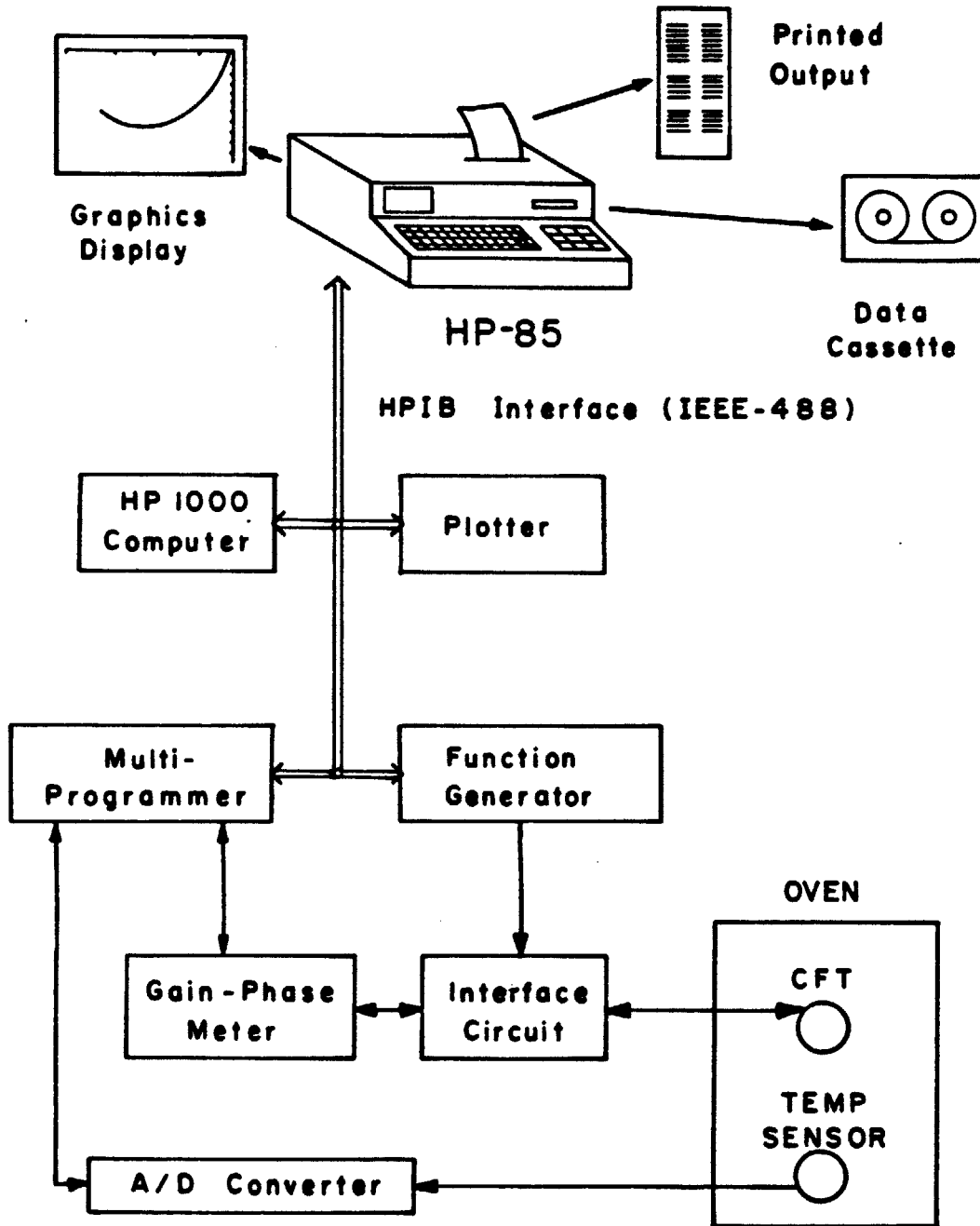


Figure 2.5 Data Acquisition System

trometer calibration, generated by the HP-1000, permits real-time computation of permittivity, loss factor and loss tangent with the HP-85 as the experiment proceeds.

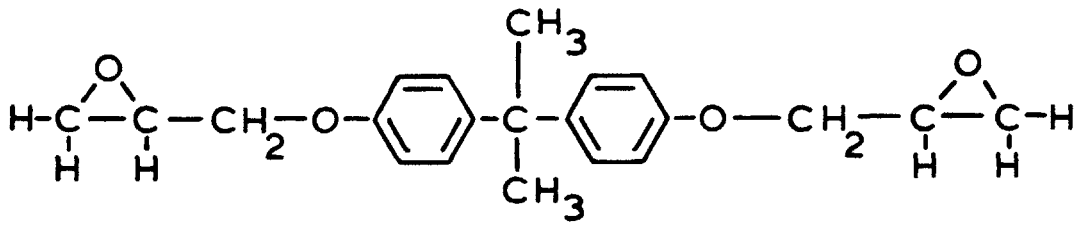
2.3 Dielectric Properties of Resins

Epoxy resins are thermosetting plastics which have important uses as potting compounds, adhesives and surface coatings. When binding graphite fibers in composite materials, for example, these resins make possible lightweight structures with high tensile strengths. Process control becomes an important issue because the resin's final properties are affected by the type of resin and curing agent, curing temperature and cure time.

The chemical structures of a typical epoxy resin and curing agent are shown in Figure 2.6.a. The resin diglycidyl ether of bisphenol-A, DGEBA, has two epoxide end-groups. The curing agent meta-phenylene diamine, MPDA, has two amine groups, each capable of joining two epoxide groups in the crosslinking reaction of Figure 2.6.b. As cure proceeds, a three dimensional network of essentially infinite molecular weight forms. The process is illustrated in Figure 2.6.c [11].

Initially the resin/amine mixture is a liquid whose viscosity increases as more and more crosslinks bind the monomers. When a sufficient number of crosslinks have

Diglycidyl ether of bisphenol-A



Meta phenylene diamine

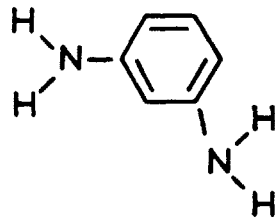


Figure 2.6.a Epoxy Resin DGEBA and Amine Curing Agent MPDA

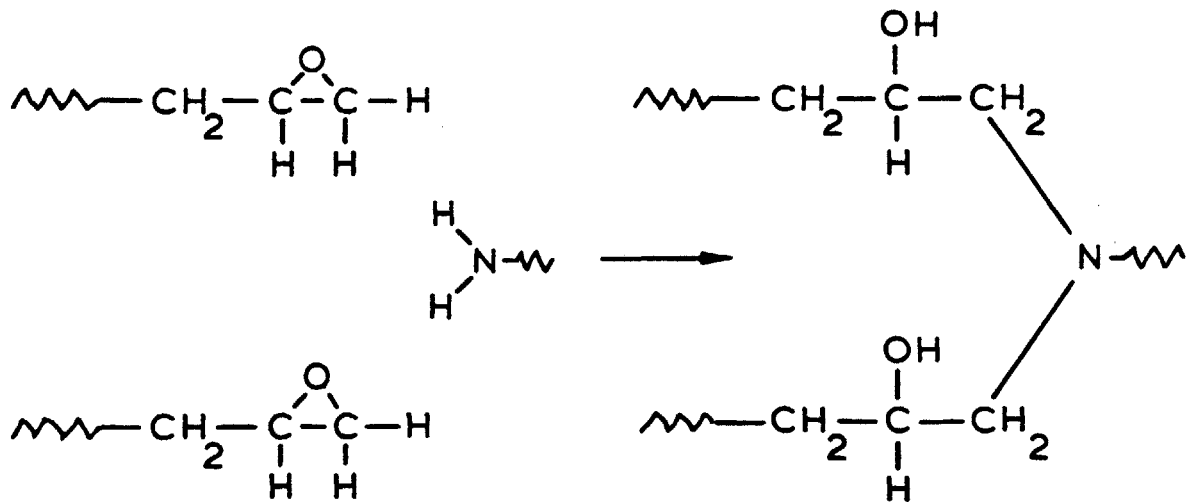


Figure 2.6.b Epoxide-Amine Crosslinking Reaction

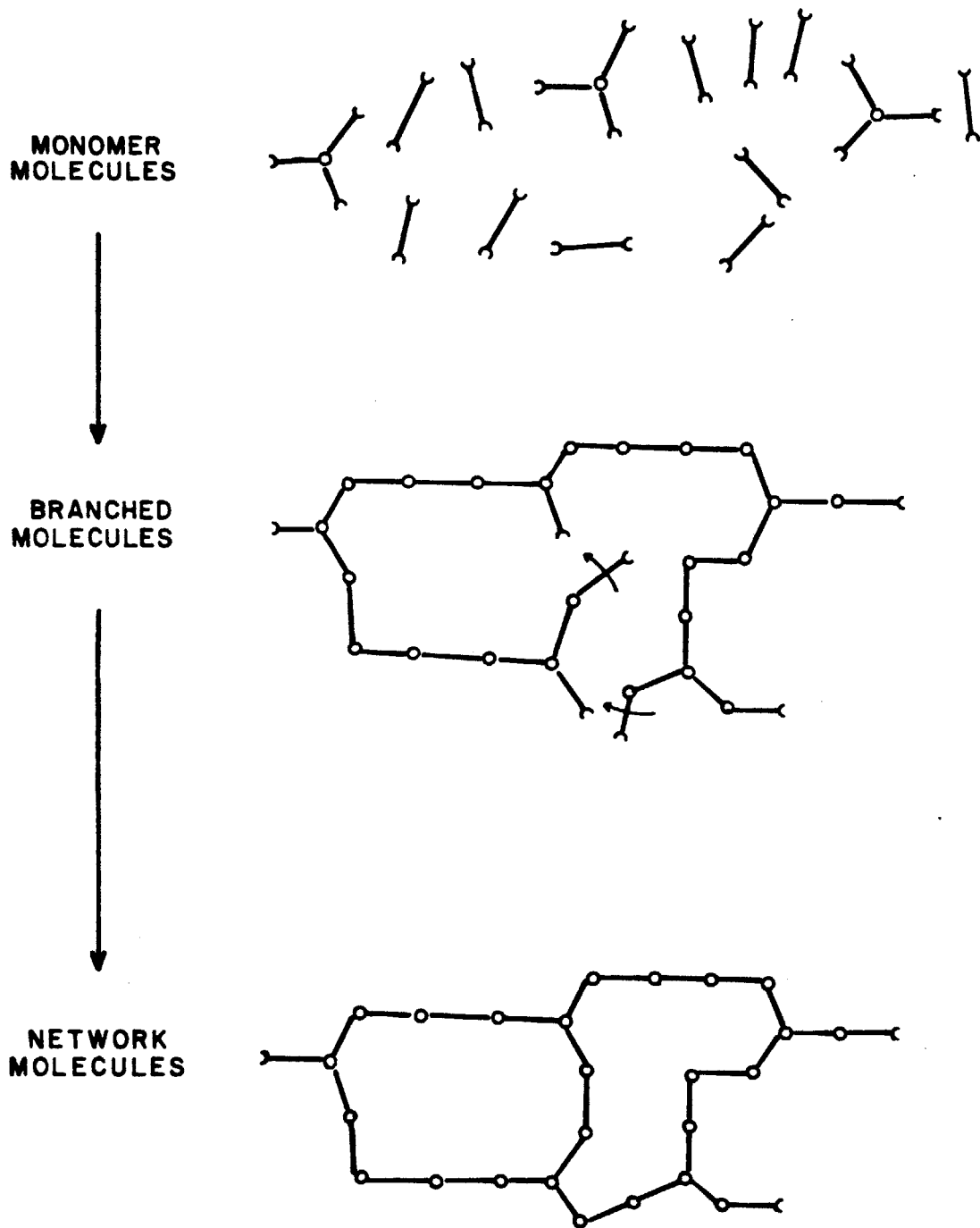


Figure 2.6.c Development of Network Structure by Crosslinking [11]

formed, the mixture becomes a rubbery gel. This stage of cure is called gelation, and occurs with the development of the infinite molecular network and its accompanying rapid increase in viscosity. For a given resin/amine system gelation occurs when a fixed percentage of crosslinks has formed, and corresponds to a given extent of reaction. The time to gelation therefore indicates the rate of chemical reaction. Additional crosslinking beyond the gel phase forms a rigid glassy solid in which the mobility of the reactants decreases to the point that the reaction stops. This stage is called vitrification.

These changes in the resin's chemical and physical composition can be used to evaluate the extent of polymerization. Cure monitoring techniques include infrared spectroscopy [12]; nuclear magnetic resonance [13]; torsional braid analysis [14],[15],[16]; differential scanning calorimetry [12],[15],[17]; and viscosity [18] and hardness [19] tests. All of these require laboratory examination, destroy the sample, or are complex and cumbersome. As a result, they cannot evaluate epoxy cure in an object being manufactured.

Residual, and possibly intrinsic, ionic impurities exist in the resins and hardeners, and it has been suggested that the DC conductivity of curing polymers decreases because network formation impedes impurity mobility [20].

Epoxies and their hardening agents typically are also very polar, exhibiting a dipole moment that can be oriented in an electric field.

AC electrical properties of resin-amine systems have been studied by placing the material in a parallel plate capacitor and measuring the current from an applied sinusoidal voltage. The AC admittance can be described by a complex dielectric constant:

$$\epsilon^* = \epsilon' - j\epsilon'' \quad [2.3.1]$$

The real part of the dielectric constant, ϵ' , is the permittivity, proportional to the displacement current or capacitive component. The imaginary part, ϵ'' , is the loss factor or AC conductivity, proportional to the current's resistive component.

An additional quantity used in characterizing a material's electrical properties is the loss tangent, which is the ratio of the imaginary component of the dielectric constant to its real component.

$$\tan \delta = \frac{\epsilon''}{\epsilon'} \quad [2.3.2]$$

In general the permittivity and loss factor vary with frequency. By modeling the dipoles as spheres in a continuous viscous medium, Debye [21] calculated the viscous friction using Stoke's law and derived the following relations:

$$\epsilon' = \epsilon_{\infty} + \frac{\epsilon_0 - \epsilon_{\infty}}{1 + (\omega\tau)^2} \quad [2.3.3]$$

$$\epsilon'' = \frac{(\epsilon_0 - \epsilon_\infty)(\omega\tau)}{1 + (\omega\tau)^2} \quad [2.3.4]$$

where ϵ_∞ is the limiting high frequency dielectric constant, ϵ_0 is the limiting low frequency dielectric constant, ω is the angular frequency and τ is the dipole relaxation time. Figure 2.7 shows the frequency dependence of permittivity and loss factor as modeled by Debye. These equations express a close relation between the real and imaginary parts of the dielectric constant; however, they can apply only when these quantities arise solely from dipole orientation.

Physically, the permittivity is maximum at low frequencies because the molecular dipoles have sufficient time to orient themselves in response to a varying electric field. In this regime, the medium is lossless because the dipoles move very slowly and with little drag. As frequency increases, the medium's viscosity dissipates energy when the dipole rotates, and inhibits full orientation. In this case the permittivity has decreased from its maximum, DC value, and the loss has increased, with the loss peak occurring at $\omega = 1/\tau$. In the limit of very high frequency, little reorientation occurs, and the modeled minimum permittivity arises from atomic and electronic polarization. The loss has also disappeared because the dipoles have no time to reorient themselves, and are stationary.

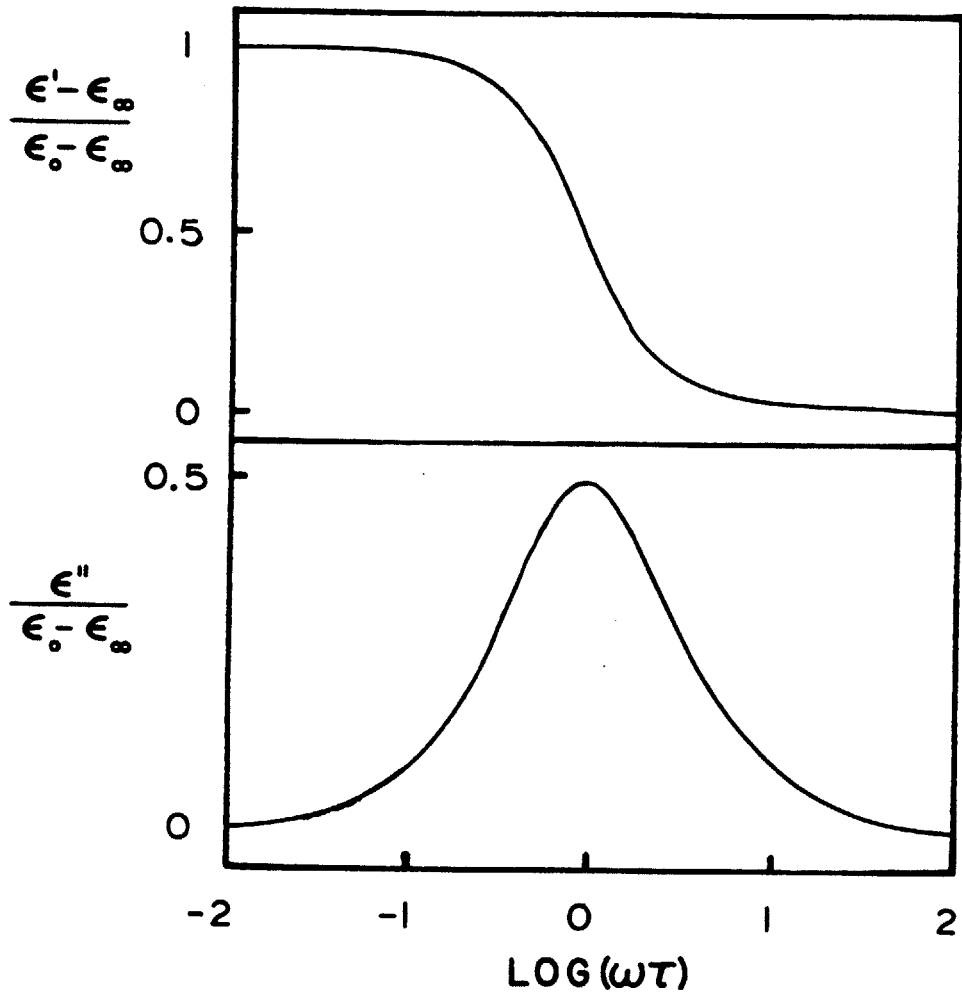


Figure 2.7 Frequency Response of Debye Dielectric Equations

When loss factor is plotted versus permittivity, with ωT as a parameter, the Debye equations describe a semicircle. Cole and Cole [22], however, found that in general the dielectric data for various materials did not fall on a semicircle, but instead fell on the arc of a circle with its center below the permittivity axis. To explain this, they proposed an empirical modification of the Debye model:

$$\epsilon' - j\epsilon'' = \epsilon_{\infty} + \frac{\epsilon_0 - \epsilon_{\infty}}{1 + (j\omega T)^{\beta}} \quad [2.3.5]$$

β is an adjustable parameter, and if $\beta = 1$ the original Debye equations are obtained. Figure 2.8 graphs ϵ' versus ϵ'' in what is often called a Cole-Cole plot. The variable β corresponds to an assumed distribution of relaxation times, although it may not have any physical significance.

The permittivity and loss factor described by the Debye relaxation time model are frequency dependent, and correspond only to the AC component of dielectric properties due to dipole orientation. The model does not take bulk conductivity into account, and in fact states that a medium ultimately becomes lossless at very low frequencies. When a material has mobile charge and a bulk conductivity, in addition to orientable dipoles, the loss factor has two terms:

$$\epsilon'' = \epsilon''_{\text{dipoles}} + \frac{\sigma_{\text{bulk}}}{\omega} \quad [2.3.6]$$

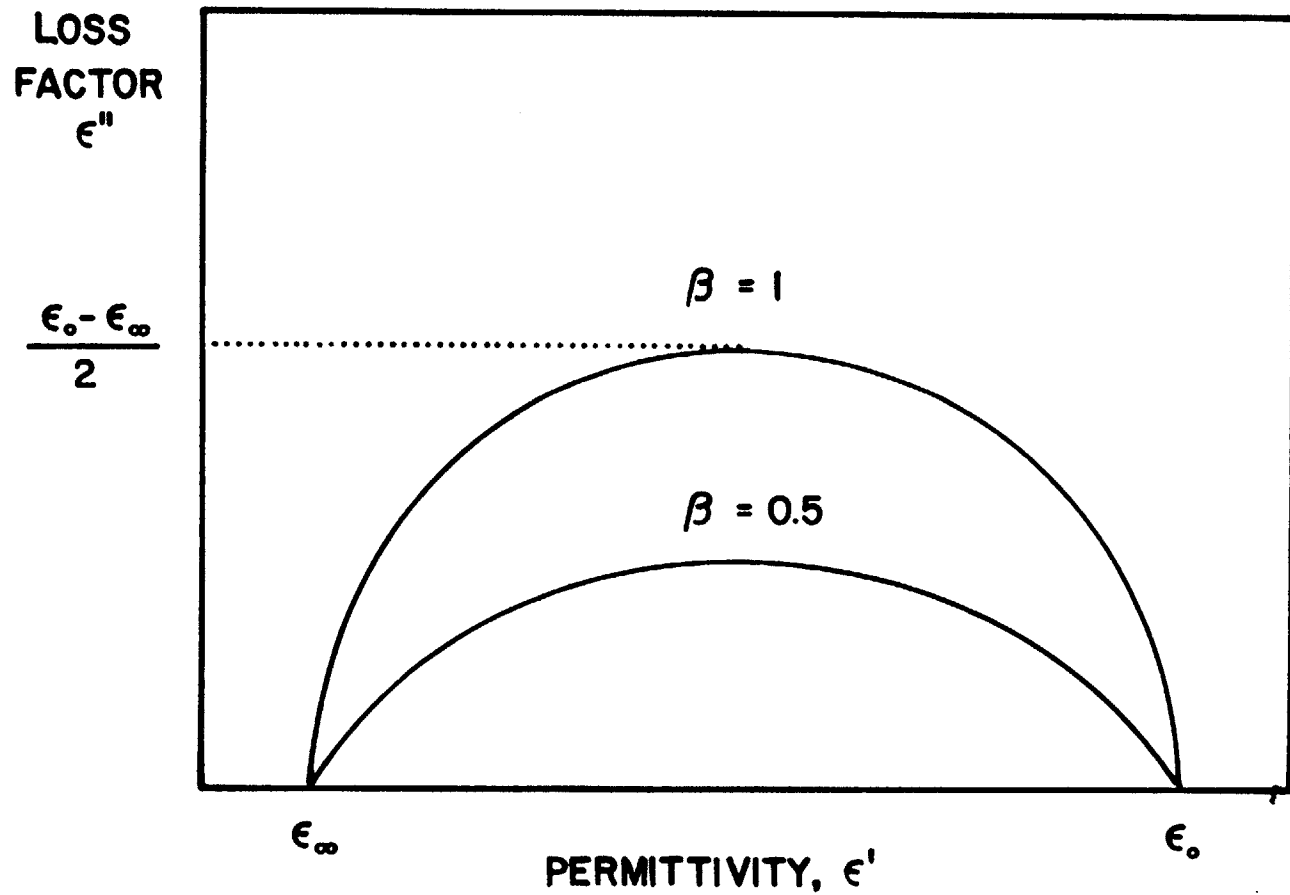


Figure 2.8 Cole-Cole Plot of Debye Dielectric Equations

where bulk conductivity contributes the σ_{bulk} term.

By plotting loss factor versus frequency it is possible to determine whether a material has dissipation originating from dipole orientation, bulk conductivity, or both. If dipole orientation occurs alone, then the plot would look like Figure 2.7, with a loss peak at a $\omega = 1 / \tau$. If the loss is due only to a bulk conductivity, then loss factor is inversely proportional to frequency, and would be a straight line on log-log scales. When both mechanisms exist, the plot would have features resulting from the sum of the two conductances.

If the range of frequencies is limited, however, it may be difficult to distinguish between either loss mechanism. Examination of equation [2.3.4] shows that for $\omega \gg 1 / \tau$, the Debye model has a loss factor which, like a bulk conductivity, is inversely proportional to frequency.

The initial assumptions in this work, and in work by researchers using parallel plate geometries, are that the resin is homogeneous and that interfacial phenomenon do not occur. In fact, the literature [23],[24] has shown that in highly conductive media with mobile space charge, the formation of blocking layers on electrode-resin interfaces can affect the observed permittivities and loss factors, and complicate the interpretation of dielectric data.

2.4 Microdielectrometry

The Debye model suggests a relationship between a resin's viscosity and dielectric properties, and is the basis behind dielectrometry as a cure monitoring technique. In the usual application of this method, the sample is placed between parallel foils, and the AC current through the resulting capacitor is recorded [25],[26],[27]. To eliminate voids which can form during cure, the resin may be subjected to pressures as high as 100 psi [8],[27]. A constant electrode separation is impossible to maintain under these conditions, and conventional dielectrometers can measure only the loss tangent, which is independent of geometry as long as the capacitor plates remain parallel. Without knowledge of electrode geometry, neither permittivity nor loss factor, and consequently, conductivity, can be obtained, and much important information is lost.

As a cure monitoring technique, microdielectrometry offers several unique advantages stemming from its integrated circuit nature. On-chip amplification allows detection of tiny currents flowing between the driven and floating gate, and extends the useful frequency range to less than 1 Hz for measurement of dielectric constants. In this regime it becomes possible to observe material relaxation

times on the order of one second, which are typical of mechanical relaxations in polymers. Low frequency measurements can be made with good resolution farther into cure, when loss factors become extremely small. In contrast, conventional dielectrometry is limited to frequencies greater than 100 Hz, with a commensurate loss of sensitivity in the later stages of cure.

The chip's small size requires only a few milligrams of sample for measurement. Isothermal cures, or experiments with well controlled, ramped temperatures may be conducted. In a manufacturing environment the microdielectrometer can be embedded in a part for in-situ monitoring or closed-loop process control. The transistor amplification provides good noise immunity, and the planar geometry remains constant despite changes in temperature or pressure.

The differential measurement scheme used in microdielectrometry allows reliable sensor operation up to 250 °C regardless of how the CFT parameters change, for the reference FET changes similarly. In addition, the sensor's geometry is well characterized and highly reproducible with integrated circuit technology.

These advantages suggest the potential of microdielectrometry in manufacturing process control, as the sensor

in the feedback controller of an autoclave, or as a research tool to investigate the dielectric properties of resins and other materials.

CHAPTER 3 FINITE DIFFERENCE SIMULATION

3.1 Introduction

Unlike parallel plate geometries, the lock and key presents an intrinsically two-dimensional problem. The inter-electrode coupling is much less efficient than for parallel plates because the electric field is not confined to the space between two planes, but instead has considerable fringing that extends into a semi-infinite region. The system is further complicated by its inhomogeneity, for the insulator that separates the lock and key from the ground plane develops interface charge whenever the semi-infinite medium has dissipation. Any solution of the field problem must satisfy a boundary condition in which the electric flux may be discontinuous across this dielectric interface.

This chapter presents a general method of finite difference modeling which is capable of dealing with arbitrarily lossy dielectrics in the sinusoidal steady state. Potentials in a two-dimensional model are represented as phasors, and Poisson's equation is solved using Gauss-Seidel iteration with successive over-relaxation. The expression for interfacial charge in an inhomogeneous system is derived and incorporated in a general finite difference equation. The simulation algorithm for the

resin-sensor system is described, and issues of convergence, computing time and error criteria are discussed.

3.2 The Method of Finite Differences

The lock and key, with the ground plane and semi-infinite medium, form a two-dimensional distributed system in which the presence of significant loss adds a dispersive, frequency dependent component to the current flow, and therefore also to the fields, between electrodes. This configuration falls into the broad class of electromagnetic problems with boundaries which either lack symmetry or are too irregular for simple analytic solutions. Finite difference modeling is often used in these cases to calculate the potential distribution numerically.

In a two-dimensional problem the area of interest is discretized into a rectangular grid of nodes at which the solutions are to be computed. Depending on whether the particular application has space charge, either Laplace's equation or Poisson's equation is used to describe the potential at each point. These are elliptic partial differential equations which require the specification of boundary conditions for a unique solution. Figure 3.1 is a schematic example of a rectangular region with a finite difference grid and boundary conditions imposed upon it.

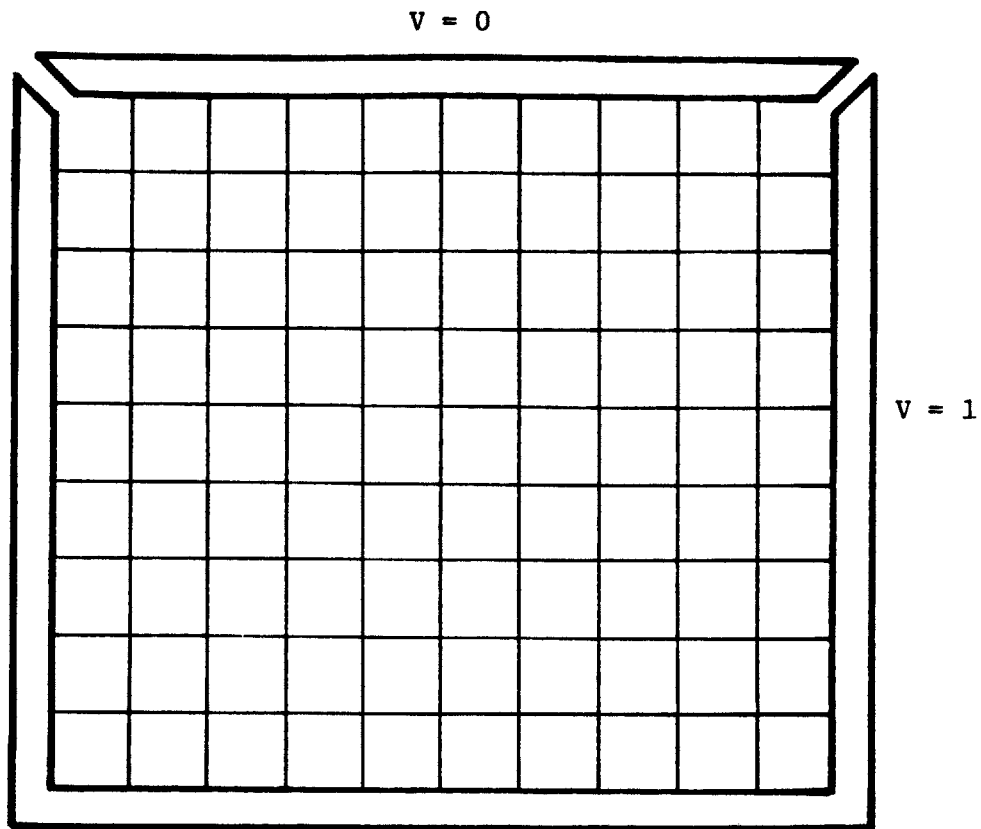


Figure 3.1 Example Finite Difference Grid with Imposed Boundary Conditions

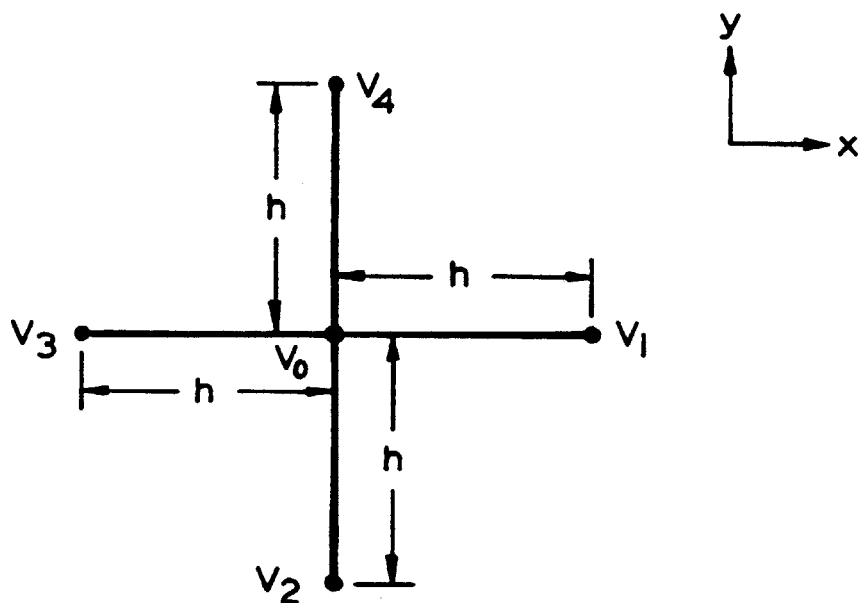


Figure 3.2 Finite Difference Node with Equidistant Neighbors

The most fundamental operation in finite difference modeling is the conversion of a continuous function into a discrete one. Since the potential varies smoothly with position, it can be expanded in a Taylor series around a node, such as the one typified in Figure 3.2. Only the four surrounding points closest to the node are considered in what is called the five-point formula. Assuming that all nodes are equidistant, the expansion yields:

$$V_1 = V(x + h, y) = V_0 + h(\partial V/\partial x)_0 + \frac{h^2}{2} (\partial^2 V/\partial x^2)_0 + \dots \quad [3.2.1.a]$$

$$V_2 = V(x, y - h) = V_0 - h(\partial V/\partial y)_0 + \frac{h^2}{2} (\partial^2 V/\partial y^2)_0 + \dots \quad [3.2.1.b]$$

$$V_3 = V(x - h, y) = V_0 - h(\partial V/\partial x)_0 + \frac{h^2}{2} (\partial^2 V/\partial x^2)_0 + \dots \quad [3.2.1.c]$$

$$V_4 = V(x, y + h) = V_0 + h(\partial V/\partial y)_0 + \frac{h^2}{2} (\partial^2 V/\partial y^2)_0 + \dots \quad [3.2.1.d]$$

Rearranging these equations and ignoring higher derivatives, the potential V_0 at node 0 becomes:

$$V_0 = \frac{(V_1 + V_2 + V_3 + V_4)}{4} - \frac{h^2}{4} (\partial^2 V/\partial x^2 + \partial^2 V/\partial y^2) \quad [3.2.2]$$

The second order term is proportional to the space charge density as given by Poisson's equation, and because this charge is zero in a homogeneous linear medium the potential at a node is just the average of potentials at its four surrounding neighbors.

$$V_o = \frac{(V_1 + V_2 + V_3 + V_4)}{4} \quad [3.2.3]$$

Equation [3.2.3], then, is the discretization of Laplace's equation in two dimensions. This "space averaging" is a property of elliptic equations, and is the reason why boundary conditions must be imposed for a unique solution. In other cases, where the nodes are not equidistant, or where a dielectric interface or a conducting surface exists, the above formula must be modified. A more general derivation will be developed later.

The expression for V_o applies to all other nodes in the homogeneous medium, and, in effect, couples any point to its four nearest neighbors. Thus, a set of simultaneous equations describes the potential distribution. If these coupled equations are arranged in a matrix equation, then the solution can be calculated with matrix inversion. Practical problems, though, often involve 1000 or more nodes, and the round-off errors from computerized operations can lead to inaccurate answers. Typically, iterative schemes are used instead. Initial values are assigned to each node in the grid, and, one by one, the potential is calculated at every point using equation [3.2.3], with results stored in an array. After the entire grid has been swept through, the procedure is repeated until the potential at each point converges.

In the method of Jacobian iteration, the potential is calculated using equation [3.2.3] and the information from the previous iteration. The new potential is stored in an array with all other answers for the current iteration. Thus during the nth pass

$$v_o^n = \frac{(v_1^{n-1} + v_2^{n-1} + v_3^{n-1} + v_4^{n-1})}{4} \quad [3.2.4]$$

The Jacobian method is relatively inefficient because it converges slowly and requires storage of two complete arrays of data. As a result, it is rarely employed.

A faster alternative is Gauss-Seidel iteration, which requires only one array, and the most recently updated values of node potentials. As soon as the new result for a point has been computed, it replaces the old one in storage and is used immediately in calculations for the next node. For example, in Figure 3.1, if the sweep through the grid proceeds from left to right, bottom to top, then the new and updated node potentials are always to the left and underneath the point currently being evaluated. The old potentials, from the previous iteration, are to the right and above the point of concern. Therefore at the nth iteration

$$v_o^n = \frac{(v_1^{n-1} + v_2^n + v_3^n + v_4^{n-1})}{4} \quad [3.2.5]$$

The Gauss-Seidel technique converges roughly twice as quickly as the Jacobian method because two old and two new potentials are used in each calculation.

Convergence can be accelerated further with the use of successive relaxation in conjunction with Gauss-Seidel iteration. Instead of substituting the result of equation [3.2.5] for the new node potential, an error term, or residual R , is defined. For a node in Figure 3.1, with a left to right, bottom to top progression:

$$R^n = \frac{(V_1^{n-1} + V_2^n + V_3^n + V_4^{n-1})}{4} - V_o^{n-1} \quad [3.2.6]$$

With relaxation methods the object is to compute this residual at each point and, in the course of succeeding iterations, reduce it to zero. This goal is accomplished by defining the new node potential, at the n th iteration, as:

$$V_o = V_o^{n-1} + \alpha R^n \quad [3.2.7]$$

where α is the relaxation or acceleration factor. If $\alpha > 1$, the method is over-relaxation and changes the sign of the residual. If $\alpha < 1$, the method is under-relaxation and does not change the sign of the residual. Over-relaxation tends to be faster in most cases, and is used more often, but situations exist where under-relaxation can be

advantageous [31]. With Gauss-Seidel iteration it can be shown that the solution diverges for $\alpha > 2$ [28].

Although the finite difference technique demands no special symmetry or boundary conditions, it has been used in the literature only for lossless dielectrics and/or static fields [28],[29],[30],[31],[32],[33],[34]. A technique is presented in this thesis for use with finite difference calculations and lossy dielectrics. It is general and allows determination of the potential distribution in the sinusoidal steady state without restriction in the magnitude of the loss factor. Hence, the method is useful for determining the conductance between electrodes immersed in a conducting dielectric medium, as well as for calculating the capacitance in a lossless one.

3.3 Derivation of the Interface Charge between Lossy Media

According to Poisson's equation, whenever interface charge exists between two dielectric media, the electric flux across that interface is discontinuous. Finite difference routines developed for MOS device simulation, [30], necessarily take such interface charge into account to calculate correctly the potential distribution in the system, but only deal with static, lossless situations. When calculating the potentials around the lock and key, however, in the presence of dissipation for the sinusoidal

steady state, the problem explicitly becomes one of finding not only the magnitude of the interface charge, but also its time dependence. If an electric field exists in a non-homogeneous region, charge is induced at the interface of two media whose time constants, ϵ / σ , are not equal. The determination of this charge is important to the numerical technique used in this thesis, and its derivation follows.

Maxwell's equations express the fundamental relationships between all electromagnetic phenomena. In sinusoidal steady state form, they are

$$\nabla \times \bar{E} = -j\omega\bar{B} \quad [3.3.1]$$

$$\nabla \times \bar{H} = \bar{J} + j\omega\bar{D} \quad [3.3.2]$$

$$\nabla \cdot \bar{D} = \rho \quad [3.3.3]$$

$$\nabla \cdot \bar{B} = 0 \quad [3.3.4]$$

where $\bar{E} = |E|e^{j\omega t} \cdot \hat{E}$, Electric field,
 $\bar{H} = |H|e^{j\omega t} \cdot \hat{H}$, Magnetic field,
 $\bar{D} = |D|e^{j\omega t} \cdot \hat{D}$, Electric flux,
 $\bar{B} = |B|e^{j\omega t} \cdot \hat{B}$, Magnetic flux,
 $\bar{J} = |J|e^{j\omega t} \cdot \hat{J}$, Current density,
 $\rho = |\rho|e^{j\omega t}$, Charge density,
 $\hat{X} =$ Unit directional vector of \bar{X} ,

and ω is the angular frequency. The constitutive equations relating fluxes to fields are assumed for all media to have the form:

$$\bar{D} = \epsilon'(\omega) \bar{E} \quad [3.3.5]$$

$$\bar{B} = \mu(\omega) \bar{H} \quad [3.3.6]$$

$$\bar{J} = \sigma(\omega) \bar{E} \quad [3.3.7]$$

where $\epsilon'(\omega)$ = Dielectric permittivity,

$\mu(\omega)$ = Magnetic permeability,

$\sigma(\omega)$ = Conductivity.

Note that these constitutive relationships assume linear, homogeneous media, and take account of the fact that the permittivity, permeability and conductivity are in general functions of frequency. In the remainder of this thesis μ is assumed constant and equal to μ_0 , and ϵ' and σ are implicitly taken to be frequency dependent.

The charge between two lossy, non-magnetic dielectrics can be calculated by first drawing a small Gaussian surface enclosing a region of the interface, as in Figure 3.3.

Using phasor notation, the curl of the magnetic field at points 1 and 2 on either side of the interface becomes:

$$\text{Region 1} \quad \nabla \times \bar{H}_1 = \bar{J}_1 + j\omega\epsilon_1 \bar{E}_1 \quad [3.3.8]$$

$$\text{Region 2} \quad \nabla \times \bar{H}_2 = \bar{J}_2 + j\omega\epsilon_2 \bar{E}_2 \quad [3.3.9]$$

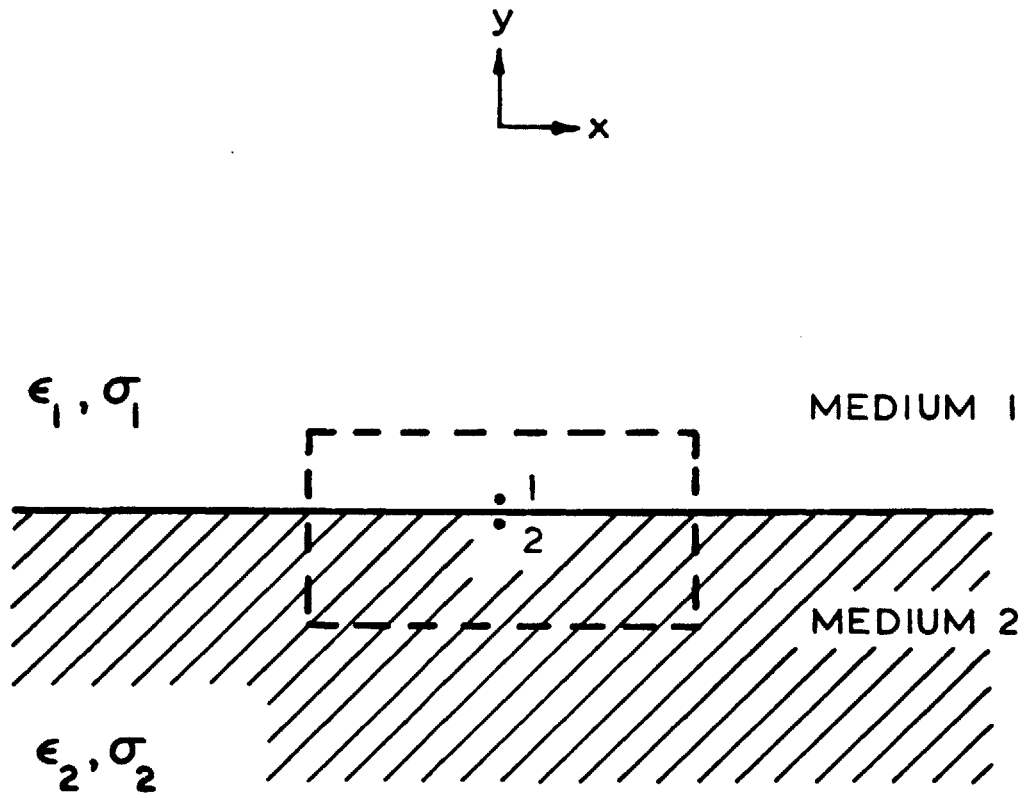


Figure 3.3 Gaussian Surface Enclosing a Differential Length of a Dielectric Interface

Since neither material is magnetic, both the perpendicular and tangential components of the magnetic field are continuous across the interface. It is assumed that points 1 and 2 are only infinitesimally separated. Therefore it is possible to say that the total magnetic fields are equal at those positions:

$$\bar{H}_1 = \bar{H}_2 \quad [3.3.10]$$

as are their curls:

$$\nabla \times \bar{H}_1 = \nabla \times \bar{H}_2 \quad [3.3.11]$$

Substitution of [3.3.8] and [3.3.9] into [3.3.11] yields the expression:

$$\bar{J}_1 + j\omega\epsilon_1'\bar{E}_1 = \bar{J}_2 + j\omega\epsilon_2'\bar{E}_2 \quad [3.3.12]$$

But the conduction current is simply conductivity times electric field, and [3.3.12] becomes:

$$(\sigma_1 + j\omega\epsilon_1')\bar{E}_1 = (\sigma_2 + j\omega\epsilon_2')\bar{E}_2 \quad [3.3.13]$$

Rearranged in terms of permittivity and loss factor, [3.3.13] becomes:

$$(\epsilon_1' - j\epsilon_1'')\bar{E}_1 = (\epsilon_2' - j\epsilon_2'')\bar{E}_2 \quad [3.3.14]$$

where ϵ' = dielectric permittivity,

and $\epsilon'' = \sigma / \omega$, loss factor.

If the electric field and flux are complex, then by defining the flux as

$$\bar{D} = \epsilon^* \bar{E} \quad [3.3.15]$$

where $\epsilon^* = \epsilon' - j\epsilon''$, it becomes possible to write Maxwell's equations in a much simplified form:

$$\nabla \times \bar{E} = -j\omega\bar{B} \quad [3.3.16]$$

$$\nabla \times \bar{H} = j\omega\bar{D} \quad [3.3.17]$$

$$\nabla \cdot \bar{D} = 0 \quad [3.3.18]$$

$$\nabla \cdot \bar{B} = 0 \quad [3.3.19]$$

When all quantities are generalized as phasors, the usual charge density term of Poisson's equation becomes incorporated into the complex dielectric constant ϵ^* . Considered this way, the interface charge problem is transformed into one analogous to determining the potential distribution across the boundary between two lossless dielectrics, where the flux is continuous across the interface.

Although equation [3.3.18] states that no sources or sinks of electric field exist in the sinusoidal steady state, it does not imply that interface charge, also, does not exist. Poisson's equation [3.3.3], defines space charge as:

$$\rho = \nabla \cdot \epsilon' \bar{E} \quad [3.3.20]$$

From equation [3.3.14], the charge density is

$$\rho = j\nabla \cdot \epsilon'' \bar{E} \quad [3.3.21]$$

Equation [3.3.20] relates interface charge to the usual presence of a discontinuous electric flux. Equation [3.3.21] emphasizes that such a discontinuity occurs when the system has loss or conduction. Thus, if ϵ'' is zero everywhere in the media, there is no space charge.

For a horizontal interface between two media, equation [3.3.21] reduces to the expression:

$$Q_I = j(\epsilon_1'' E_{1y} - \epsilon_2'' E_{2y}) \quad [3.3.22]$$

where only the electric field component perpendicular to the boundary can induce charge. When the electric field is a phasor, the charge density term of [3.3.22] is also a phasor. The actual, physically meaningful charge is determined after multiplying this phasor by an $e^{j\omega t}$ term, and taking the real part of the product. Thus the interface charge varies sinusoidally with time.

3.4 Derivation of the General Finite Difference Formula

It is essential to the development of finite difference simulation with lossy dielectrics, that the interface charge density, once obtained, is incorporated into an expression that discretizes the continuous form of Poisson's equation. Figure 3.4 illustrates a general node in a finite difference grid. The node lies on the horizontal dielectric interface between two media, either of which

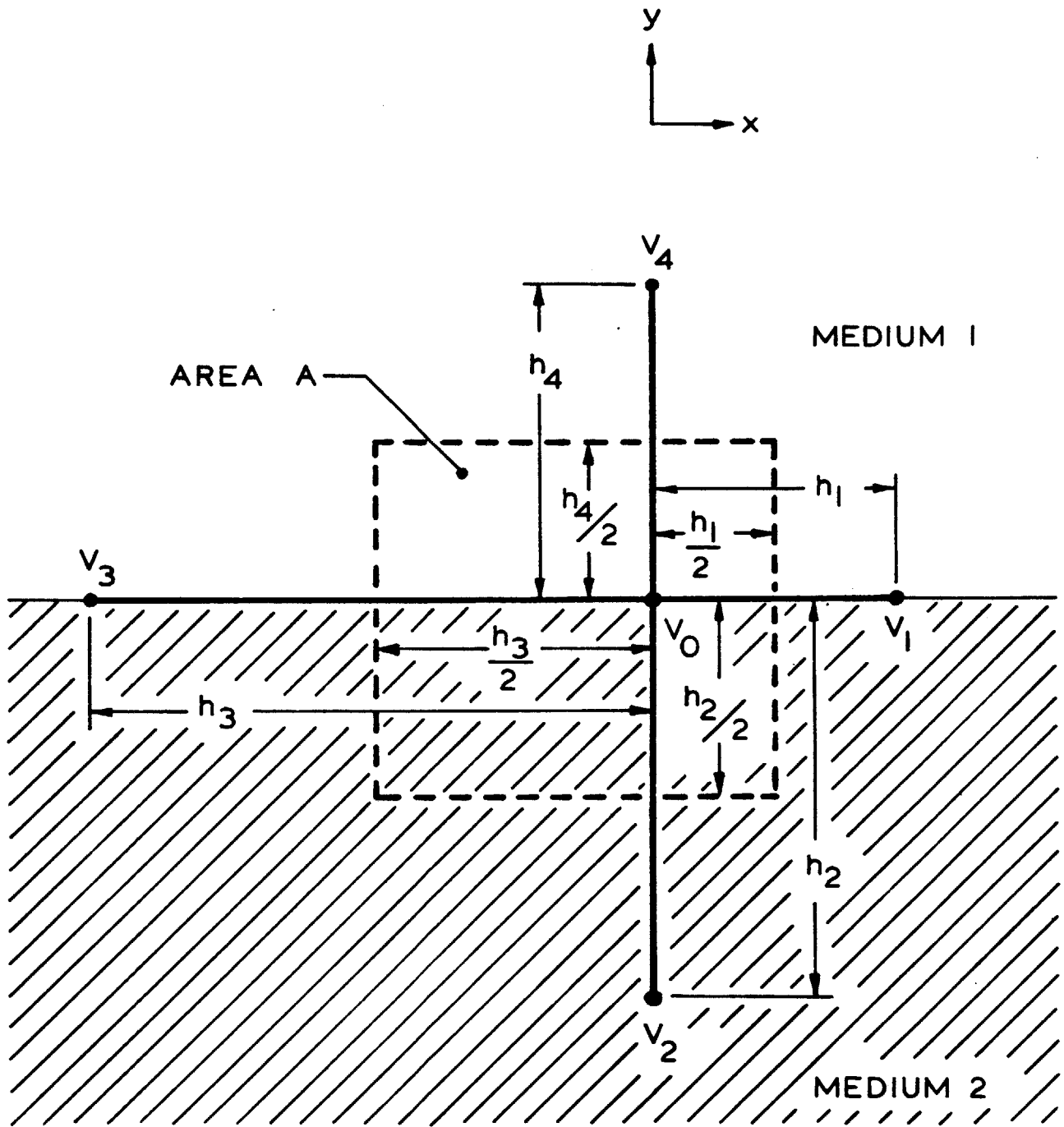


Figure 3.4 General Finite Difference Node on a Dielectric Interface

may be lossless or lossy. Distances to the four nearest neighbors are not necessarily equal. In two dimensions Poisson's equation is

$$\nabla \cdot [\epsilon' \nabla V(x,y)] = -\rho(x,y) \quad [3.4.1]$$

The potential $V(x,y)$ is complex and treated as a phasor, as is the charge term $\rho(x,y)$. As shown previously, the interfacial charge density is

$$Q_I = j(\epsilon_1'' E_{1y} - \epsilon_2'' E_{2y}) \quad [3.3.22]$$

The space around each node in the finite difference grid is discretized into a rectangular region A whose sides bisect the arms between a node and its four nearest neighbors. The potential along any side is considered constant, and has a value somewhere between that of the nodes on the ends of the bisected line segment. Integrating over area A, Poisson's equation becomes:

$$\iint_A \nabla \cdot (\epsilon' \nabla V(x,y)) dx dy = - \iint_A \rho(x,y) dx dy \quad [3.4.2]$$

Strictly speaking, the interface charge term is given by [3.3.22], but this expression assumes that the tangential flux through the Gaussian surface of Figure 3.4 is zero. This assumption is true in the limit where the vertical dimension of the Gaussian surface becomes infinitesimally small, but cannot apply when the vertical sides have finite

extent. The interface itself becomes discretized into the area A; the "interface" charge is then described by [3.3.21], and is substituted into Poisson's equation:

$$\iint_A \nabla \cdot (\epsilon' \nabla V(x,y)) \, dx dy = \iint_A j \nabla \cdot (\epsilon'' \nabla V(x,y)) \, dx dy \quad [3.4.3]$$

where $\bar{E} = -\nabla V$. Equation [3.4.3] can be rearranged into Laplace's equation if the dielectric permittivity is considered complex.

$$\iint_A \nabla \cdot (\epsilon^* \nabla V(x,y)) \, dx dy = 0 \quad [3.4.4]$$

Using Green's theorem, the surface integral becomes a line integral along the perimeter of area A.

$$\iint_A \nabla \cdot (\epsilon^* \nabla V(x,y)) \, dx dy = \oint_A \epsilon^* \nabla V(x,y) \cdot \hat{n} \, dl \quad [3.4.5]$$

The total line integral is the summation of line integrals over each edge of the rectangle.

$$\oint_A \epsilon^* \nabla V(x,y) \cdot \hat{n} \, dl = \sum_{m=1}^4 \int_{h_m} \epsilon_m^* \nabla V(x,y) \cdot \hat{n}_m \, dl \quad [3.4.6]$$

The integral is now approximated with the discrete form of the gradient operator.

$$\nabla V(x,y) \cdot \hat{n}_m = \frac{V_m - V_o}{h_m} \quad [3.4.7]$$

If $\nabla V(x,y) \cdot \hat{n}_m$ is constant along the side of area A, then

$$\oint_A \epsilon^* \nabla V(x,y) \cdot \hat{n} \, dl = \sum_{m=1}^4 \left(\frac{V_m - V_o}{h_m} \right) \int_{h_m} \epsilon_m^* \, dl = 0 \quad [3.4.8]$$

Expanding the summation in the case of a general interfacial node yields the general finite difference equation coupling neighboring nodes in a grid:

$$v_o = \frac{\frac{v_1}{h_1(h_1 + h_4)} + \frac{\frac{\epsilon_2^*}{\epsilon_1^*} v_2}{h_2 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)} + \frac{v_3}{h_3(h_1 + h_3)} + \frac{v_4}{h_4 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)}}{\frac{1}{h_1 h_3} + \frac{1}{h_2 h_4} \left(\frac{\frac{\epsilon_2^*}{\epsilon_1^*} h_4 + h_2}{h_4 + \frac{\epsilon_2^*}{\epsilon_1^*} h_2} \right)} \quad [3.4.9]$$

In the case where $h_1 = h_2 = h_3 = h_4$ and $\epsilon_1^* = \epsilon_2^*$, a square grid in a homogeneous medium,

$$v_o = \frac{(v_1 + v_2 + v_3 + v_4)}{4}$$

Equation [3.2.3] is regained, demonstrating the "space averaging" property of elliptic partial differential equations.

Additional insight and a different viewpoint on the treatment of lossy dielectrics can be obtained with a second derivation using a circuit analogy. The node of Figure 3.5.a illustrates a general point on the interface of two lossy dielectrics. Again the distances to its four nearest neighbors may not all be equal. The space around the node can be discretized into admittance elements coupling the five points to form the circuit model of

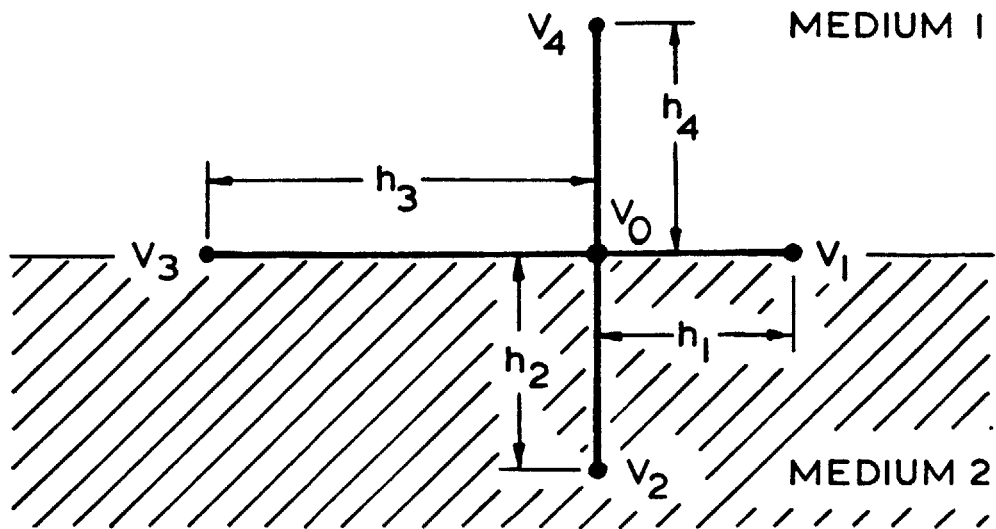


Figure 3.5.a General Finite Difference Node on a Dielectric Interface

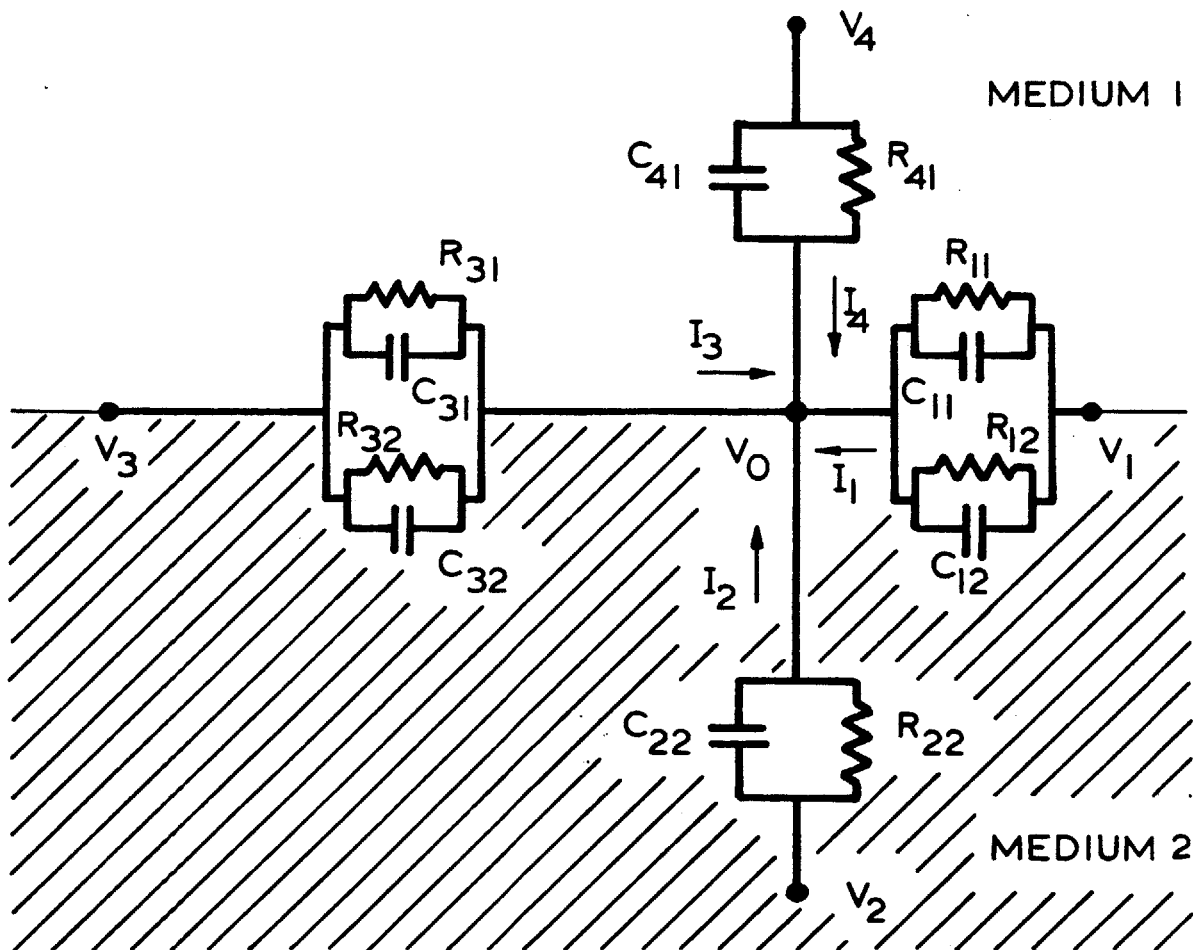


Figure 3.5.b General Finite Difference Node Illustrating Circuit Analogy

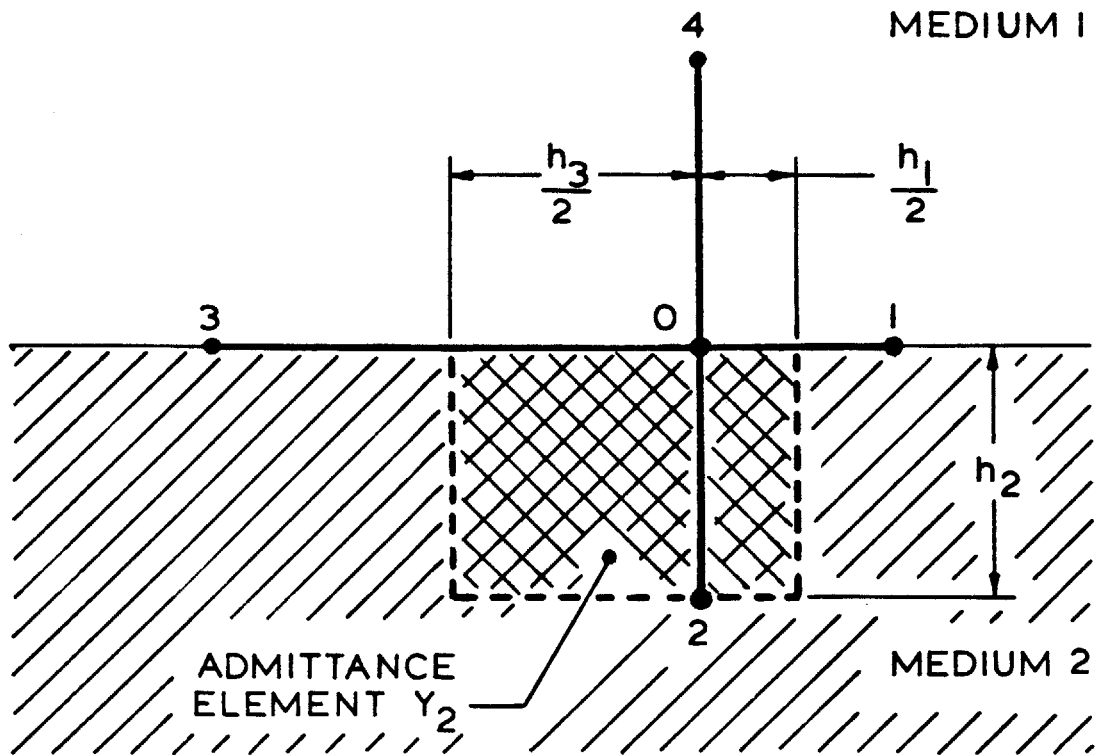


Figure 3.5.c Geometry of a Discretized Admittance Element between Nodes 0 and 2

Figure 3.5.b. The conductivity between two nodes is represented with a resistor whose conductance is that of the material between the nodes, where $G = 1/R$. At an interface, two different resistors must be included in the model, one for each material. Likewise capacitors connect the nodes, and the modeling is similar; the permittivity of the capacitance is equal to that of the material between the nodes.

The admittance of a circuit element is

$$Y = (\sigma + j\omega\epsilon') A/L \quad [3.4.10]$$

where A = Cross sectional area,

L = Length of the element.

Equation [3.4.10] can be cast into different form emphasizing the complex nature of the dielectric permittivity:

$$Y = j\omega(\epsilon' - j\epsilon'') A/L = j\omega\epsilon^* A/L \quad [3.4.11]$$

The length of the admittance element between two nodes is the distance between the nodes. The thickness is unity and the width is half the perpendicular distance to the next row of nodes on one side, plus half the distance to the next row of nodes on the other. For example, an element between nodes 0 and 2 of Figure 3.5.b has the geometry shown in Figure 3.5.c, and an admittance of:

$$Y_2 = \epsilon_2^* \frac{(h_1/2 + h_3/2)}{h_2} \cdot 1 \quad [3.4.12]$$

Y_2 is equivalent to an RC parallel admittance because the material between nodes 0 and 2 has both a conductivity and permittivity.

Nodes along an interface must be treated somewhat differently. Two different admittance elements must connect nodes 0 and 1, one for each medium. The admittance for the upper half of the interfacial region has the geometry of Figure 3.6.a, and an admittance of:

$$Y_{11} = \epsilon_1 * \frac{(h_4/2)}{h_1} \cdot 1 \quad [3.4.13]$$

The admittance of the lower half has the geometry of Figure 3.6.b, and an admittance of:

$$Y_{12} = \epsilon_2 * \frac{(h_2/2)}{h_1} \cdot 1 \quad [3.4.14]$$

The total admittance of the circuit element connecting nodes 0 and 1 is

$$Y_1 = \frac{(\epsilon_1 * h_4/2 + \epsilon_2 * h_2/2)}{h_1} \cdot 1 \quad [3.4.15]$$

Similarly the admittances for the remaining two elements connecting nodes 0 to 3, and 0 to 4 can be written:

$$Y_3 = \frac{(\epsilon_1 * h_4/2 + \epsilon_2 * h_2/2)}{h_3} \cdot 1 \quad [3.4.16]$$

$$Y_4 = \epsilon_1 * \frac{(h_1/2 + h_3/2)}{h_4} \cdot 1 \quad [3.4.17]$$

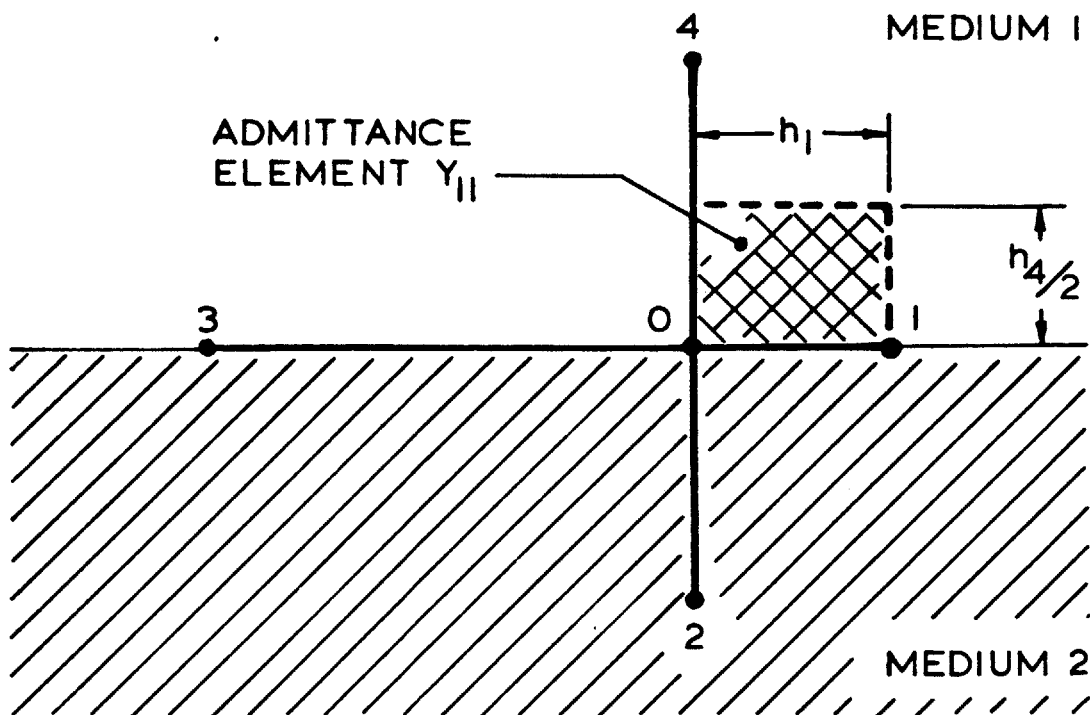


Figure 3.6.a Geometry of the Upper Discretized Admittance Element along an Interface

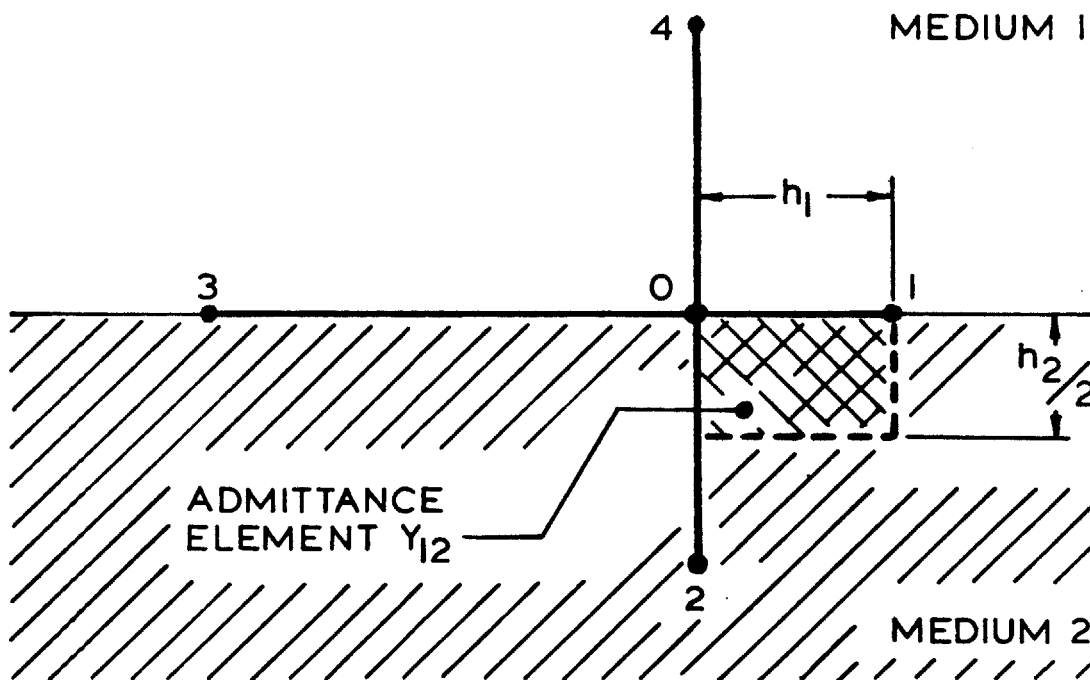


Figure 3.6.b Geometry of the Lower Discretized Admittance Element along an Interface

By Kirchhoff's current law, using the current orientations of Figure 3.5.b:

$$I_1 + I_2 + I_3 + I_4 = 0 \quad [3.4.18]$$

where

$$I_n = Y_n (V_n - V_o) \quad [3.4.19]$$

Combining [3.4.12]--[3.4.19] and rearranging terms to isolate V_o , the voltage at the center node, the following relationship is obtained:

$$V_o = \frac{\frac{V_1}{h_1(h_1 + h_4)} + \frac{\frac{\epsilon_2^*}{\epsilon_1^*} V_2}{h_2 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)} + \frac{V_3}{h_3(h_1 + h_3)} + \frac{V_4}{h_4 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)}}{\frac{1}{h_1 h_3} + \frac{1}{h_2 h_4} \left(\frac{\frac{\epsilon_2^*}{\epsilon_1^*} h_4 + h_2}{h_4 + \frac{\epsilon_2^*}{\epsilon_1^*} h_2} \right)} \quad [3.4.20]$$

which is the same as [3.4.9], derived by calculating the surface integral around the central node.

3.5 Electric Field and Interface Charge

Knowledge of potentials throughout the simulation grid also makes possible calculation of the electric field at each node. From the definition of electric field:

$$\vec{E} = -\nabla V$$

a Taylor series expansion around a point yields a discrete form of the gradient of the potential. Referring to the general node of Figure 3.4, the x and y components of the electric field are

$$E_{x_0} = -\frac{1}{2} \left(\frac{V_1 - V_0}{h_1} + \frac{V_3 - V_0}{h_3} \right) \quad [3.5.1]$$

$$E_{y_0} = -\frac{1}{2} \left(\frac{V_4 - V_0}{h_4} + \frac{V_2 - V_0}{h_2} \right) \quad [3.5.2]$$

An expression for the discretized interface charge can also be obtained from Poisson's equation. Proceeding from equation [3.4.2] in a derivation similar to that for the general finite difference formula, the interface charge about the node of Figure 3.4 is

$$Q_I = - \left[\frac{V_1 - V_0}{h_1} \left(\frac{\epsilon_1' h_4 + \epsilon_2' h_2}{2} \right) + \frac{V_2 - V_0}{h_2} \left(\epsilon_2' \left(\frac{h_1 + h_3}{2} \right) \right) \right. \\ \left. + \frac{V_3 - V_0}{h_3} \left(\frac{\epsilon_1' h_4 + \epsilon_2' h_2}{2} \right) + \frac{V_4 - V_0}{h_4} \left(\epsilon_1' \left(\frac{h_1 + h_3}{2} \right) \right) \right] \quad [3.5.3]$$

In a homogeneous medium with $\epsilon_1' = \epsilon_2'$, and $h_1 = h_2 = h_3 = h_4$, the charge is zero, as expected. The term Q_I is actually the charge contained in area A, instead of a true interface charge, for A is the discretized model of the interface. Therefore the analog of interface charge

is the surface integral of charge density over A, as given by equation [3.4.2]

3.6 Simulation Grid and Boundary Conditions

A program was written in FORTRAN and implemented on the laboratory's HP-1000 minicomputer for the modeling of sensor geometries and the analysis of experimental data. The routine simulates the lock and key response to a sinusoidal input voltage, given the lock and key geometry, resin permittivity and conductivity, and signal frequency.

The lock and key is a pair of electrodes with alternate "fingers" connected to the driven and floating gates. It is equivalent to a periodic arrangement of many parallel strips, where every other strip has the same potential. For the lock and key, the space between electrodes is folded into a meander whose length determines the magnitude of the inter-electrode coupling, and the total capacitance from the electrodes to ground. The intrinsic, or unloaded, gain of the lock and key, however, is fixed by the ratio of electrode width to electrode height above the ground plane. Lengthening the meander increases both the inter-electrode coupling and the capacitance-to-ground by the same proportion, and consequently leaves the voltage division unaffected at the floating gate.

As Figure 2.1 shows, the electrodes are finite, both in their length and in the width of the array. It is assumed that the lock and key structure is large enough for its periodicity to dominate the deviation from periodicity around its perimeter. Therefore the stray fields there can be neglected. Another non-symmetrical feature is the meander, which has corners where the inter-electrode gap folds around the lock and key fingers. The field at these corners violates the assumed regularity, but their effect is also ignored because the corners make-up only 5% of the total meander length. Since the field does not vary along the length of the fingers, the above simplifications reduce the problem to two dimensions, with the entire lock and key represented as a pair of half-electrodes bounded by vertical planes of symmetry, as shown in Figure 3.7. The geometry is fixed so electrode width and separation are each equal to W . The electrodes are separated from the ground plane with a height H by a layer of silicon dioxide and/or insulator. The space above the electrodes is semi-infinite, and is filled with a dielectric which may be either lossless or lossy. The total length, M , of the meander between electrodes is measured at its center, but is not used in the simulation. It is needed later to scale the two-port admittances of the lock and key when the effect of a load is taken into account.

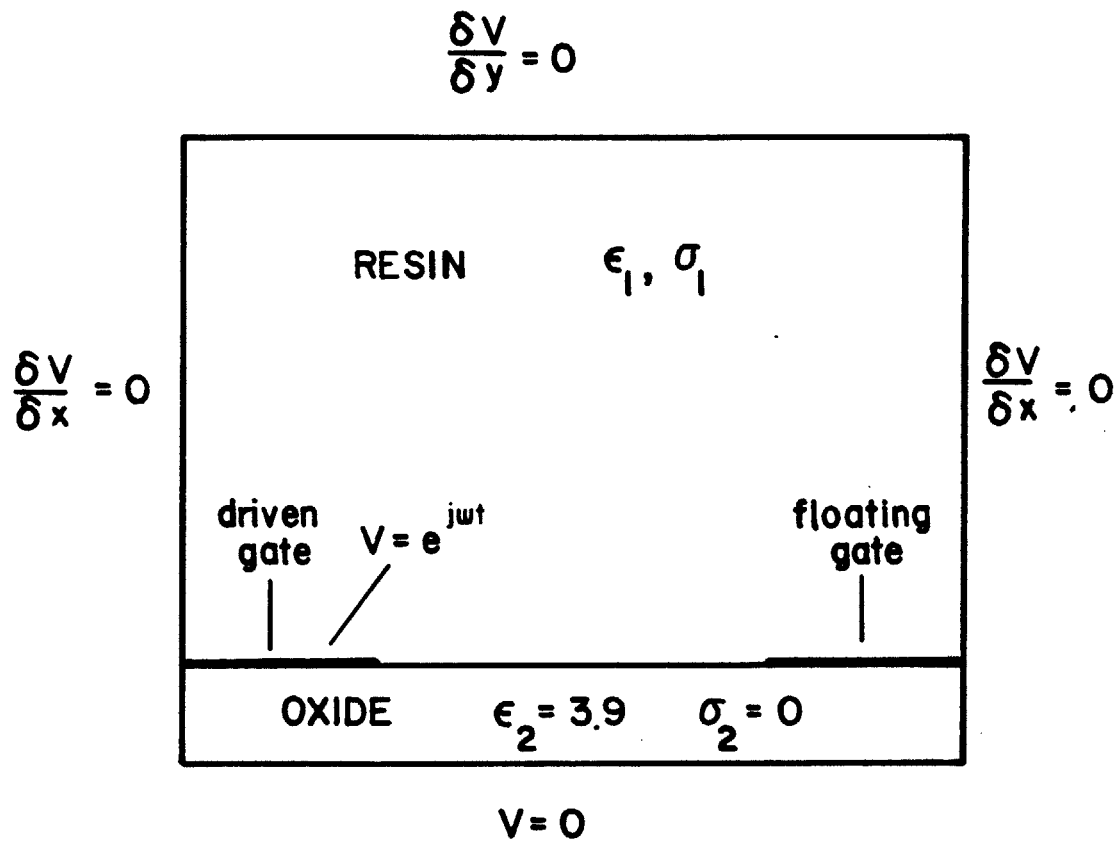


Figure 3.7 Lock and Key Model, with Boundary Conditions, used in Simulation

The finite difference grid imposed on this model, Figure 3.8, has three regions: 1) a fine mesh between the electrodes and ground plane, 2) a medium mesh just above the electrodes and interface, and 3) a coarse mesh far above the electrodes. The accuracy of simulation depends directly on the fineness of the grid, and areas with intense electric fields require close node spacing. Regions where the potential varies less rapidly can be adequately served with a coarser network of points. The potential changes most rapidly between the electrodes and ground plane, and there the mesh has 10 nodes in the vertical and 27 nodes in the horizontal direction. Here the horizontal spacing between grid points is $W/12$. The vertical spacing between points is $H/10$.

The intermediate region has a square array of 27 nodes in the horizontal direction and a user defined number between 8 and 20 nodes in the vertical. Horizontal and vertical spacings are both $W/12$.

The coarse mesh has 15 nodes in the horizontal direction and a user specified number between 3 and 15 in the vertical. Horizontal and vertical spacings are both $W/6$. The electric field is quite weak in this uppermost region, thus the fine mesh in the insulator is not necessary, for it would greatly increase computing time with only a marginal gain in accuracy.

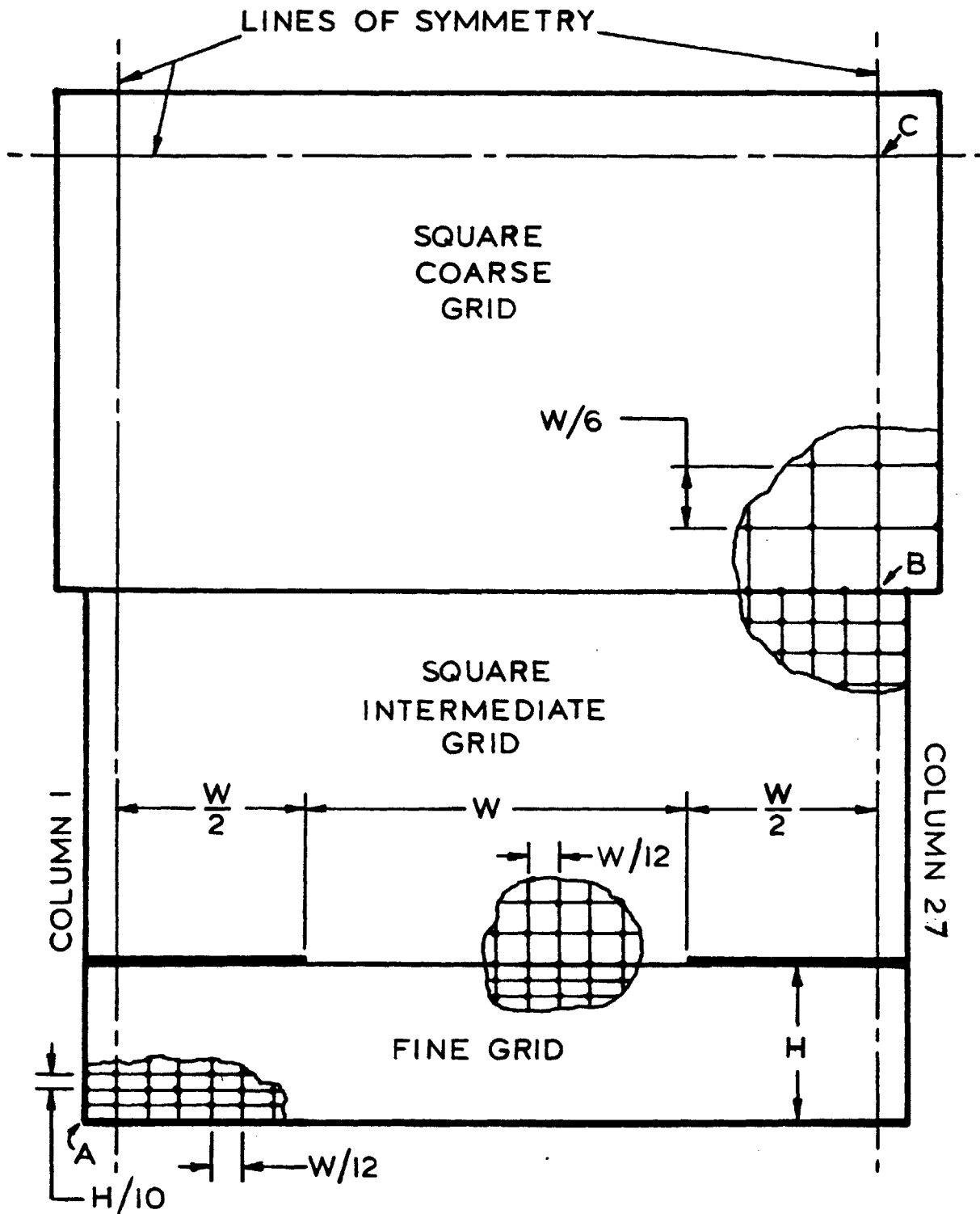


Figure 3.8 Finite Difference Grid used in Simulation

At the interface between the upper and middle grids, some nodes have four nearest neighbors and others have five, as detailed in Figure 3.9.a. The general finite difference formula [3.4.9] is a five point equation coupling the potentials of a central node to four neighbors which lie on perpendicular arms. For a point such as node B in Figure 3.9.a, a power series approximation to the continuous field is employed to derive a six point formula.

If the approximate potential can be described with a series of the form

$$V(x,y) = V_0 + Ax + By + Cx^2 + Dy^2 + Exy \quad [3.6.1]$$

then the constraint of Laplace's equation, $\nabla^2 V = 0$, requires that $C = -D$. The coefficients are determined by boundary conditions imposed by the five neighboring grid points, where x and y are the node coordinates relative to the central node A. A system of five equations in five unknowns must be solved. In the general case of Figure 3.9.b, the finite difference formula is

$$\begin{aligned} V_T(n - \delta) + \delta V_U + n^2 V_R + \frac{1}{2} (n^3 + n^2 - \delta n^2 + \delta^2 n) (V_Q + V_S) \\ = (n^3 + 2n^2 - \delta n^2 + n + \delta^2 n) V_P \end{aligned} \quad [3.6.2]$$

Substitution of $n = 2$, $\delta = 1$ provides the equation used at the interface of the uppermost coarse, and central

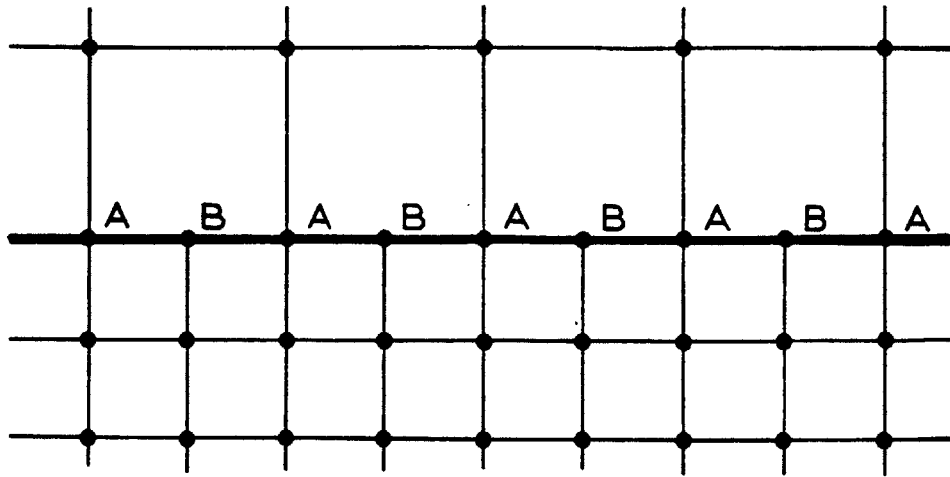


Figure 3.9.a Nodes at Interface between Coarse and Intermediate Grids

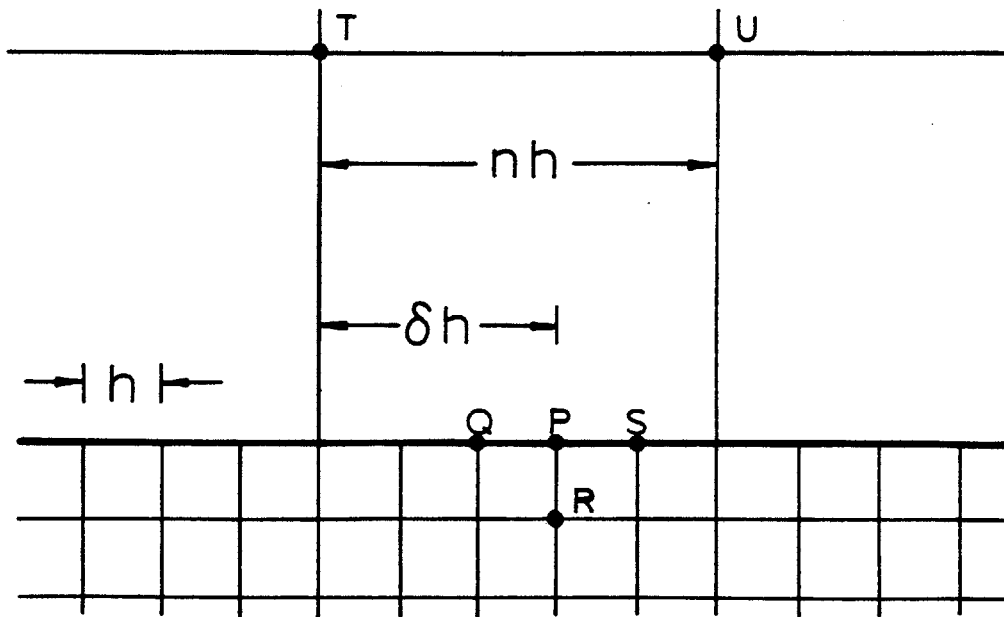


Figure 3.9.b General Node with Five Nearest Neighbors

intermediate grids. Since this region is homogeneous, no provision is necessary to accommodate fixed or space charge.

Charge does accumulate at the resin-oxide dielectric interface, as derived in section 3.3, and equation [3.4.9] must be used at the nodes there.

The potentials at all nodes are complex, and are treated as phasors with a magnitude and phase. The uniqueness theorem, which has been applied to static, real fields, can be generalized for complex fields and guarantees that any complex potential distribution satisfying Laplace's or Poisson's equation must be the only solution for a given set of complex boundary conditions.

The finite difference grid describing the resin-electrode system has Dirichlet boundary conditions, where the potential is defined, and Neumann boundary conditions, where the potential's normal derivative is defined. Along the entire ground plane $V = 0 + j0$, or $0e^{j0^\circ}$. At the driven gate, $V = 1 + j0$, or $1e^{j0^\circ}$. At the floating gate, all nodes must have the same potential. Since the grid is bounded by vertical lines of symmetry that divide electrode fingers in half, the Neumann boundary condition is imposed, with the normal derivative of the potential equal to zero, or $\partial V / \partial x = 0$.

The upper boundary condition is somewhat more difficult to deal with because the area above the electrodes is

semi-infinite, although it is modeled as a field with finite dimensions. Several methods exist for treating boundaries at infinity [32],[33],[34], but it is sufficient to set the normal derivative of the potential to zero at this edge, that is, $\partial V / \partial y = 0$. This implies the existence of a mirrored set of conductors, but if the line of symmetry is far from the electrodes, then the interaction with these images becomes negligible, and adequately models a boundary at infinity.

3.7 The Simulation Algorithm

In the finite difference simulation program, the required inputs are the permittivity and conductivity of the resin, the permittivity and conductivity of the insulator beneath the electrodes, the electrode height above the ground plane, and the signal frequency. These data are sufficient to define the resin-electrode system. Calculations are performed using Gauss-Seidel iteration with successive over-relaxation. Several assumptions were made during the development of this simulation:

- 1) The electrodes are infinitely thin. This is valid because the metal is approximately one micron thick, while the electrodes are 12.5 microns wide. Dang and Shigyo have made finite difference simulations of an electrode

array identical to the lock and key, but also included the effect of finite electrode thickness [33]. For electrode geometries used in the experiments, there is essentially no difference between their results and the simulation in this thesis.

2) The electrode-resin contact is ohmic. Sheppard [8] has shown this assumption is not true in certain circumstances, particularly when the lock and key is coated with uncured, highly conductive resin, and electrochemical corrosion occurs.

3) The semi-infinite medium is uniform; the permittivity and conductivity do not change with position. This assumption is employed for simplicity because the effects of inhomogeneities are difficult to model, and are often unknown. Electrode polarization and discharge, though, do occur and, when a homogeneous medium was assumed, have been known to influence the apparent measured dielectric properties of materials in parallel plate experiments [35],[36]. Macdonald has shown that under certain conditions space charge in highly conductive media can produce an observed permittivity and loss factor that vary with frequency in a manner that can be described by the Debye dielectric dispersion equations with a single relaxation time [23],[24].

- 4) The semi-infinite medium is linear.
- 5) The effects of surface conductance and capacitance are at the resin-oxide interface are negligible.
- 6) The effects of edge fringing at the perimeter of the lock and key, and end fringing at the tips of the electrode fingers, are negligible. The electrode array is large enough so the asymmetrical field around the perimeter has a relatively small influence. In addition, the corners of the meander between electrodes are only 5% of the total meander length, and the electrode themselves are 35 times longer than their width. Thus the field fringing at the meander corners and electrode ends is only a tiny effect on the total inter-electrode coupling.

The simulation uses the electrode model of Figure 3.8. Electrode width, W , is 12.5 microns, but symmetry permits use of half-electrodes 6.25 microns wide. The separation between fingers of the lock and key is fixed at 12.5 microns. For the simulation of different geometries, the program accepts the electrode height above the ground plane, H , as an input parameter. Therefore, the quantity which specifies a particular electrode geometry is the width to height ratio, W/H .

Given the parameters describing physical quantities of the resin-electrode system, the program applies equation [3.4.9] at each node of Figure 3.8 in a sequence starting at point A, proceeding left to right, bottom to top, until reaching point B. Data about nearest neighbor distances are pre-programmed in the routine. Permittivity and conductivity information for both the resin and insulator are pertinent only at the dielectric interface. When the recalculated potential for each node is obtained, it is substituted into the storage array for use during the next calculation by the Gauss-Seidel method.

As soon as potentials are computed for nodes of column 3, they are substituted in reflecting nodes of column 1, simulating the zero normal component boundary condition at lines of symmetry. Similarly, potentials computed for nodes of column 25 are reflected into nodes of column 27.

At the interface between the intermediate grid and the coarse upper grid, nodes with four nearest neighbors are treated with the five point formula, while those with five nearest neighbors are treated with the six point formula of equation [3.6.2]. Potentials for nodes in the upper grid are calculated from left to right, bottom to top, in the same way as the lower grid. The zero-normal component boundary condition at the upper edge is simulated in the same way as the vertical lines of symmetry, with

potentials of nodes just below the line of symmetry reflected to the row just above the line. Each iteration stops when point C on the upper line of symmetry is reached.

3.8 Relaxation Parameter

When using relaxation methods, the choice of relaxation parameter α is critical for efficient convergence. While any α greater than 1 and less than 2 will generally accelerate convergence, some values can cause oscillations in the residue, and possibly divergence.

The optimum value of α , which reduces the residue R most quickly, differs from problem to problem, and no general theory exists to determine the best relaxation parameter. Frankel [37] and Young [38] have obtained expressions that provide the optimum parameter for a Dirchilet problem with a simple rectangular boundary. Other techniques have been proposed by Carré [39] and Kulsrud [40], but these are empirical and deal with different specialized types of boundaries.

The finite difference algorithm developed for this thesis uses relaxation parameters whose values are adjusted continually during the calculation. It has been observed for this problem that a larger relaxation parameter generally produces faster convergence--until, for certain unpre-
dic-

table combinations of permittivity and conductivity, the calculation oscillates or diverges.

A relative residue is defined as the difference in calculated potential at a node for the latest two iterations, normalized by the most recently calculated potential for that node, or:

$$R' = \frac{V^n - V^{n-1}}{V^n} \quad [3.8.1]$$

The relaxation parameter for a particular region, for example, the oxide/insulator grid, is assigned an initial value for the start of the finite difference calculation. At every third iteration the sum of magnitudes of the relative residues is determined for each of the three grid regions. For a particular region, if the total magnitude increases, signaling a diverging solution, the relaxation parameter is reduced by 0.02. If the total magnitude decreases, the solution is converging and the relaxation parameter is increased by 0.01 to accelerate the process. The relaxation parameter is reduced by a greater amount than it is increased because a diverging solution must be rectified quickly. In all cases α is restricted to values between 1.2 and 1.9.

3.9 Convergence of the Solution

In its usual application, a finite difference solution is defined to converge when the largest nodal residue falls below some maximum value. Ideally, when the solution has fully converged, the residues are zero everywhere. Considerations of computer time, though, typically lead to a maximum relative residue on the order of .0001 for acceptable accuracy.

The complex finite difference routine for the resin-electrode simulation employs a somewhat more generalized definition of convergence. Since the potential at a node is adjusted during each iteration, the difference between consecutive iterations may be thought of as an error term, which is complex because the potentials are phasors. Convergence is then defined to occur when the magnitude of the relative residue is no greater than .0001 everywhere in the finite difference grid. The simulation algorithm retains in its memory the value of the largest such relative residue for each iteration, and when its magnitude is less than .0001, the computation stops.

Conceptually, this error term is a phasor which, when added to the complex node potential, sums to another phasor that is the new node potential for the current iteration. If the error phasor is sufficiently small in magnitude,

the difference in magnitude and phase for the newly calculated potential is negligible.

3.10 Effect of Arbitrary Loads

Solution of the complex finite difference problem for the grid network of Figure 3.8 will yield a magnitude and phase for the potential at the floating electrode. The lumped element model of Figure 2.3, however, shows that the resin-electrode system does not exist in isolation, but is loaded by the FET gate capacitance. This extra capacitance will change the output response of the lock and key. The computer simulation accounts for arbitrary loads by extracting the lock and key's two-port admittance parameters and then adding the FET capacitance to the output admittance term. The terminal voltages of the resulting new two-port can then be calculated.

For a lock and key with a semi-infinite medium of given permittivity and loss factor, the terminal currents can be described by the admittance matrix equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & -Y_{12} \\ -Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad [3.10.1]$$

Where the currents and voltages are complex and have the orientations of Figure 3.10. Since the lock and key is

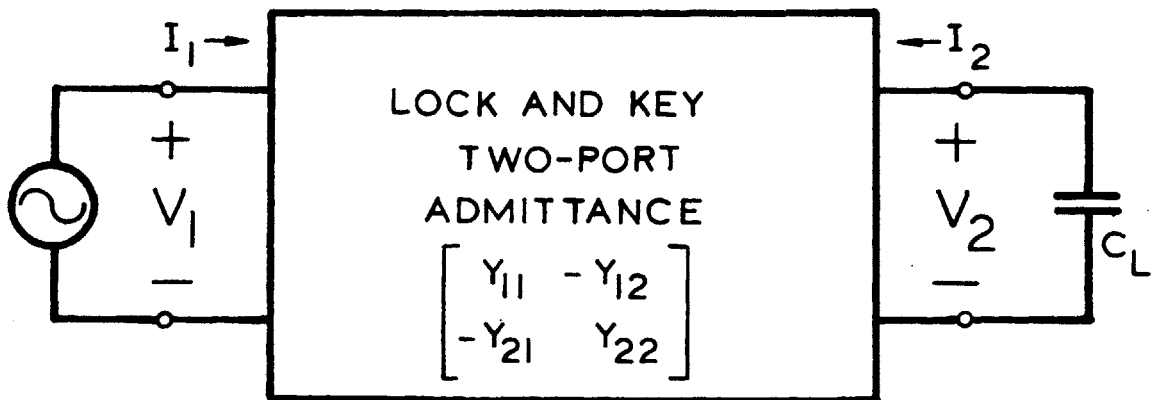


Figure 3.10 Two-Port Admittance Parameter Model of the Sensor

symmetrical and reciprocal, $Y_{11} = Y_{22}$ and $Y_{12} = Y_{21}$. The matrix equation can now be rearranged into the following:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 & -V_2 \\ V_2 & -V_1 \end{bmatrix} \begin{bmatrix} Y_{11} \\ Y_{12} \end{bmatrix} \quad [3.10.2]$$

The solution for the two-port admittance parameters are:

$$Y_{11} = (-I_1 V_1 + I_2 V_2) / (-V_1^2 + V_2^2) \quad [3.10.3]$$

$$Y_{12} = (I_2 V_1 - I_1 V_2) / (-V_1^2 + V_2^2) \quad [3.10.4]$$

If the terminal currents and voltages are known, then the two-port parameters can be determined. The complex finite difference simulation calculates the output voltage, or intrinsic response, for the unloaded lock and key, and provides half the necessary information. The currents can be evaluated by taking a surface integral around the electrodes. Figure 3.11.a shows the Gaussian surfaces around the lock and key's fingers. In the static case the integral of the electric flux through a closed surface, multiplied by the permittivity, gives the total charge contained within that boundary. In the sinusoidal steady state, the integral of the complex flux gives the current through the surface. In Figure 3.11.a these currents are

$$I_1 = \oint_{S_1} (\sigma + j\omega\epsilon') \bar{E} \cdot d\bar{S}_1 \quad [3.10.5]$$

$$I_2 = \oint_{S_2} (\sigma + j\omega\epsilon') \bar{E} \cdot d\bar{S}_2 \quad [3.10.6]$$

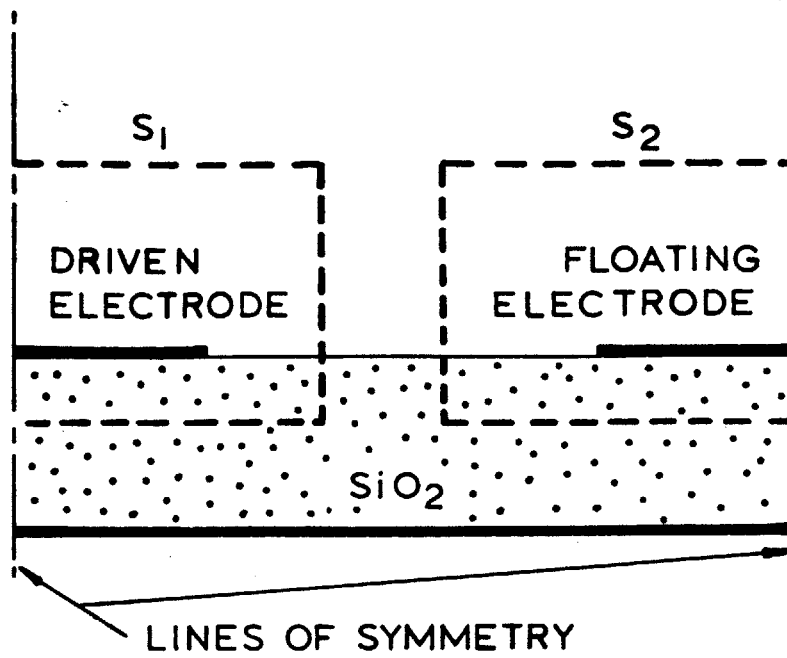


Figure 3.11.a Surface Integrals around Lock and Key Electrodes

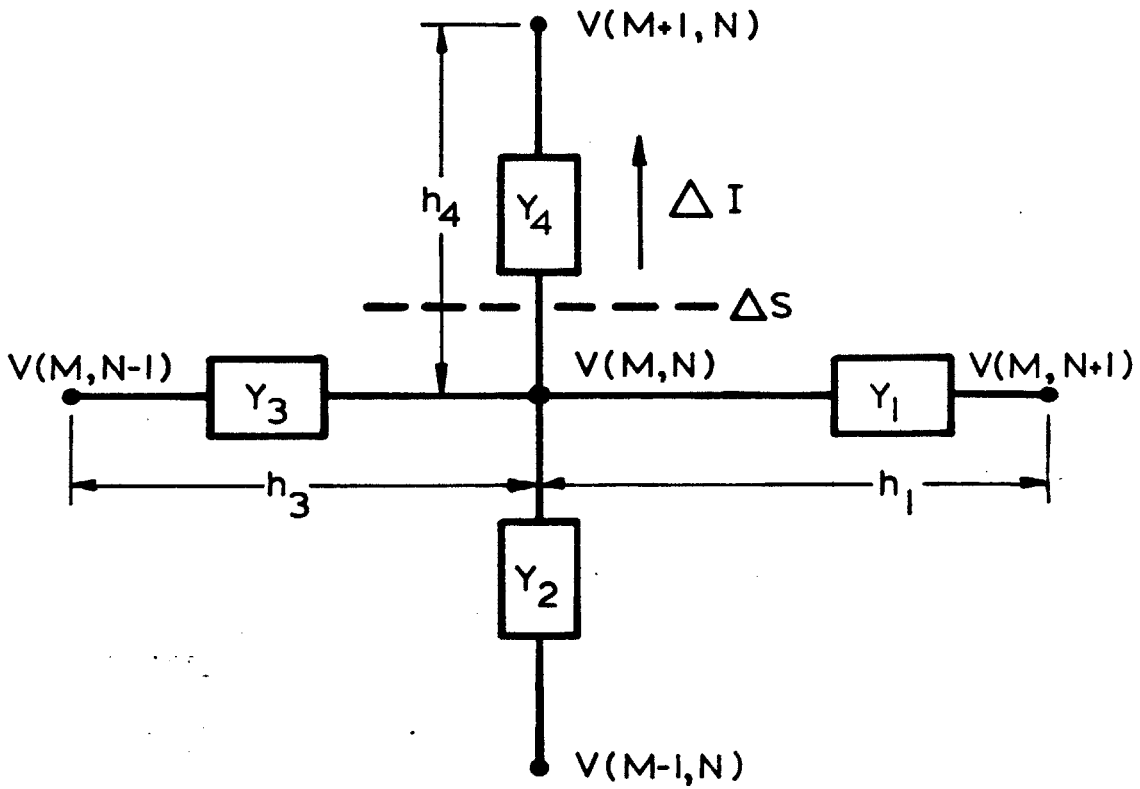


Figure 3.11.b Discretized Surface Integral used for Finite Difference Grids

The circuit analogy of Figure 3.11.b shows how these surface integrals can be calculated from knowledge of the potential field, after solution by finite differences. Given two nodes (M,N) and (M+1,N), the admittance element connecting these nodes is the same as that used in formulating the finite difference equations:

$$Y = \frac{(\sigma + j\omega\epsilon') (h_1/2 + h_3/2)}{h_4} \quad [3.10.7]$$

The current passing through the surface ΔS between these nodes is therefore:

$$I = \frac{(V(M,N) - V(M+1,N)) (\sigma + j\omega\epsilon') (h_1/2 + h_3/2)}{h_4} \quad [3.10.8]$$

which, in the limit of a differential surface, becomes

$$dI = (\sigma + j\omega\epsilon') \bar{E} \cdot \bar{dS} \quad [3.10.9]$$

Summation of all ΔI 's gives the total current through the closed surface. In this way the simulation program determines the terminal currents for the lock and key. Equations [3.10.3] and [3.10.4] then yield the two-port parameters for the matrix equation [3.10.1] and the π -equivalent model of Figure 3.12.

The π -equivalent model shows that the unloaded, intrinsic lock and key output response is

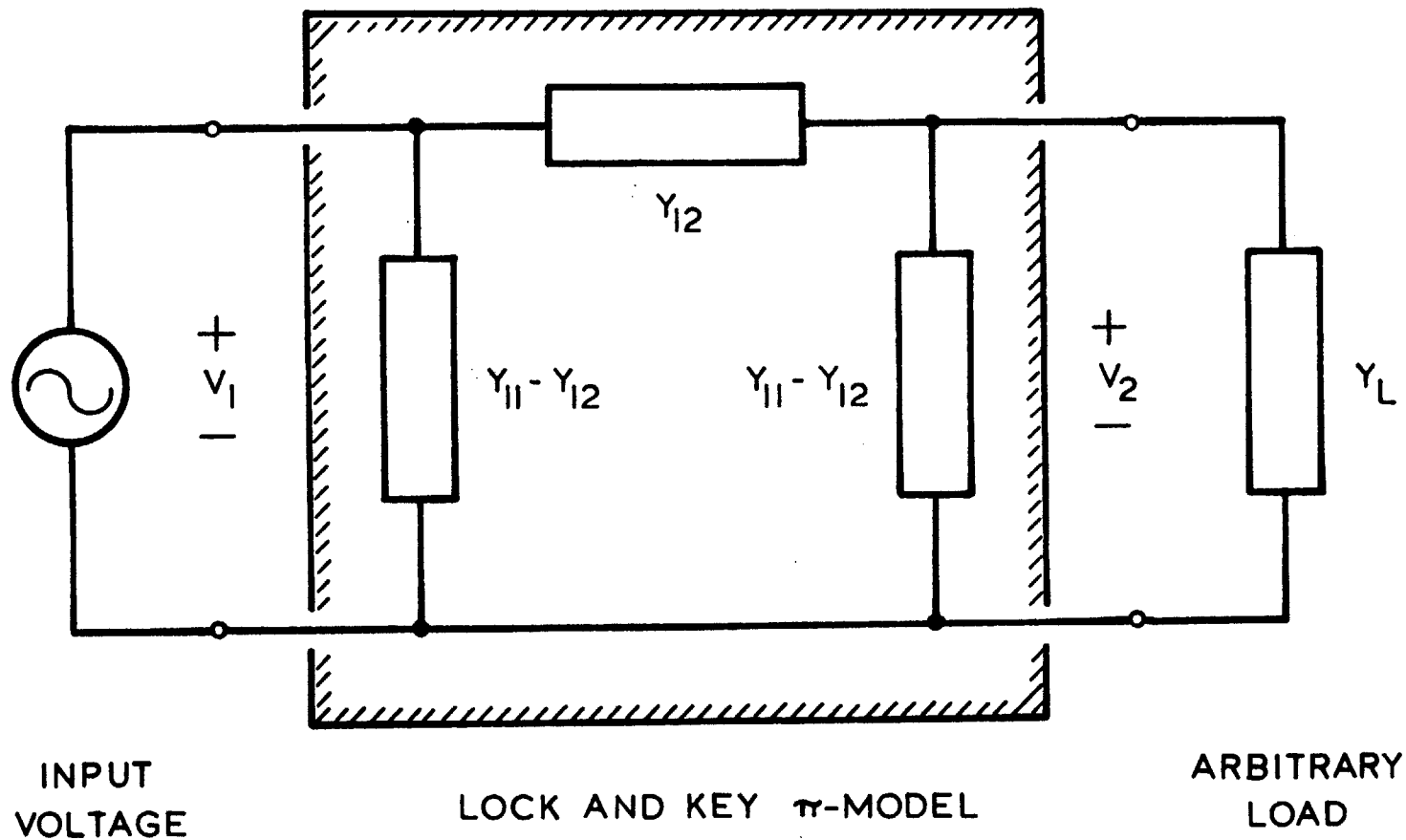


Figure 3.12 Pi-Equivalent Model of the Lock and Key

$$\frac{V_2}{V_1} = \frac{Y_{12}}{Y_{11}} \quad [3.10.10]$$

With an arbitrary load Y_L , the response becomes:

$$\frac{V_2}{V_1} = \frac{Y_{12}}{Y_{11} + Y_L} \quad [3.10.11]$$

3.11 Effect of Upper Boundary Position

Before a simulation with the finite difference program can validly model an electrode pair with a semi-infinite medium above it, the upper boundary must be situated so the mirrored ground plane exerts negligible influence. When the gain and phase of the floating electrode was calculated for several values of permittivity and loss factor, with upper boundary height above the electrodes as a parameter, it was found that when this height exceeds approximately 2.25 finger widths, corresponding to a mirrored ground plane at twice that separation, additional increases in height produce no change in output response. Figure 3.13 shows how the intrinsic gain of an uncoated lock and key varies with upper boundary position. All sensors used in experiments had W/H ratios within the two limits that are illustrated. Consequently, in the simulation program this boundary has a default height of 2.25 W

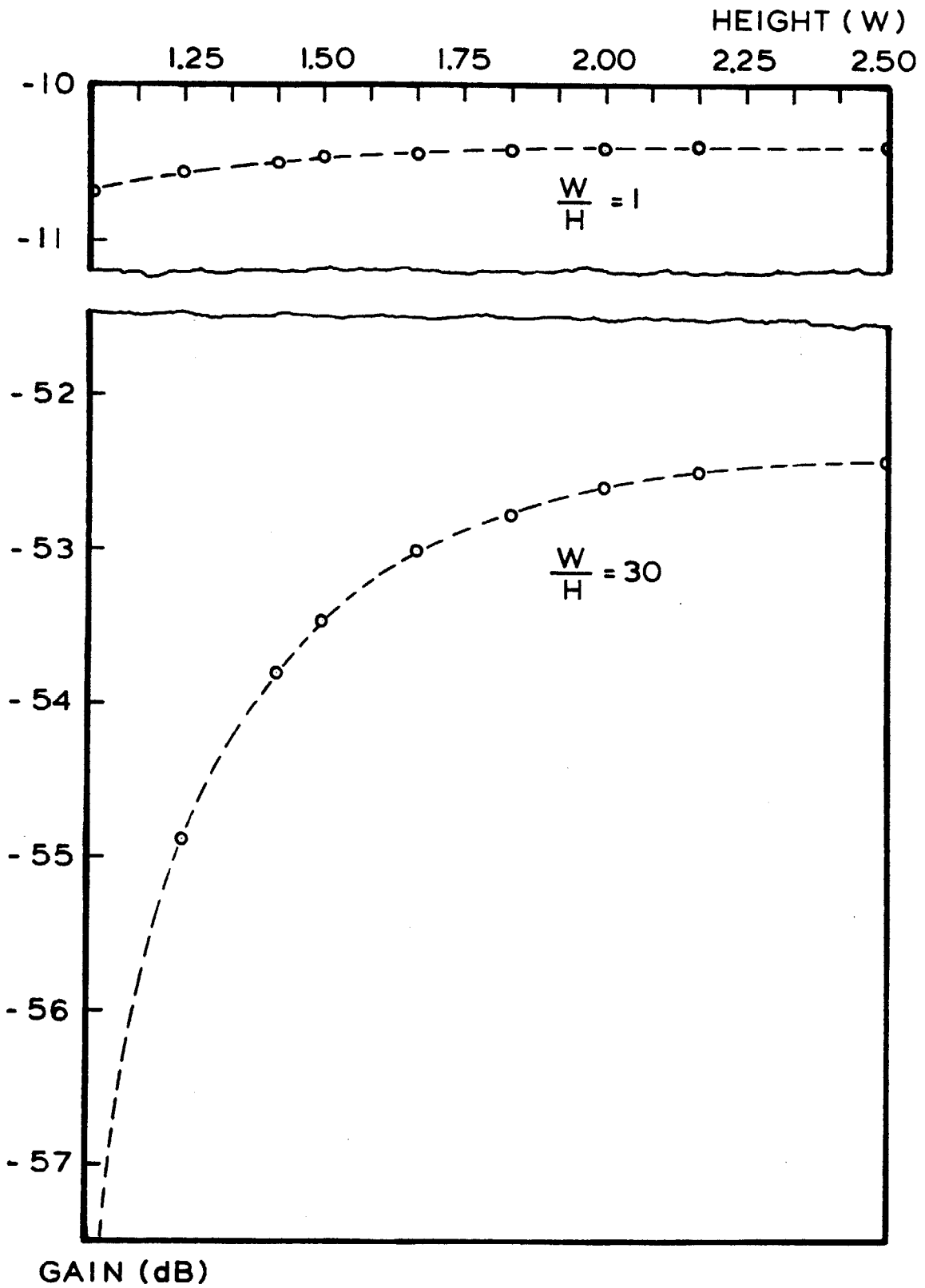


Figure 3.13 Intrinsic Gain in Air of the Lock and Key as a Function of Upper Boundary Position in Simulation

above the electrodes, i.e. 28 microns, because the electrodes are scaled to be 12.5 microns wide.

3.12 Effect of Relaxation Parameters

The simulation program was run with the relaxation parameter fixed at different values for a lock and key with $W/H = 12.5$ and a dielectric semi-infinite medium with a permittivity and loss factor of unity. The grid was initialized to zero everywhere so each run started from the same set of conditions. The results typify the dependence of convergence time on α . When the sum of relative errors for all nodes is plotted as a function of iteration, it becomes apparent that the number of iterations required for convergence is quite sensitive to the particular value of this relaxation parameter, and that an optimum value should be known to at least the second decimal place. Varying α from 1.6 to 1.8 decreases computing time by sixty percent. Further increasing α to 1.9 actually increases the number of iterations required. Maintaining α constant, however, may cause the residues to oscillate under certain conditions. Continually adjusting α as described in Section 3.8 not only guarantees convergence in all cases, but also, as shown in Figure 3.14, can further reduce the number of iterations required for solution.

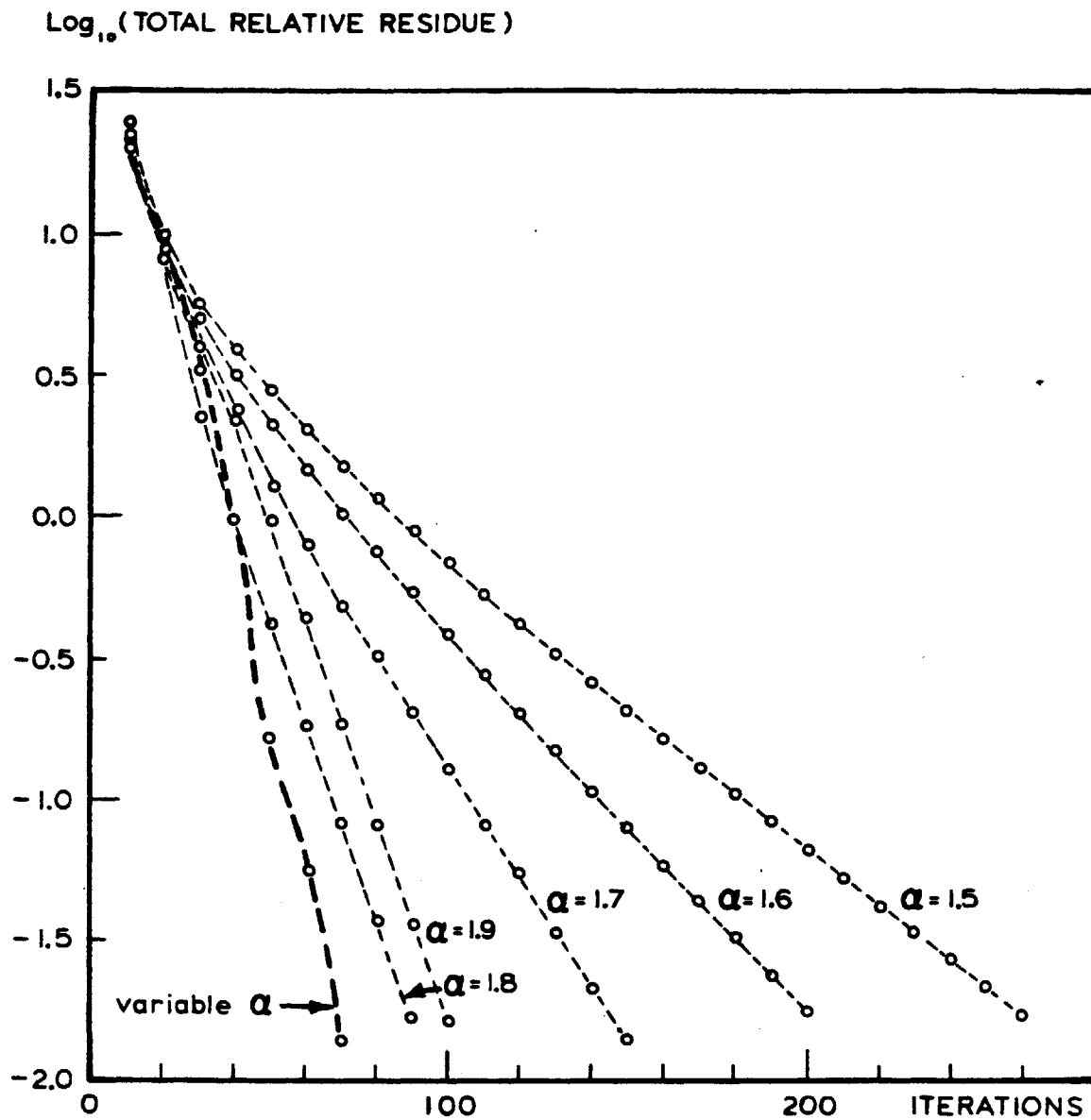


Figure 3.14 Residue Behavior for Different Relaxation Parameters

If the magnitude of the normalized residue at each node is obtained, and converted to a density of points which can be plotted around that particular node, in a two dimensional mapping, then the progress of algorithm convergence can be observed. A subroutine has been written to perform this function, where the density of points decreases with the logarithm of the normalized residue. A clear area indicates that the relative magnitude of the residue about the node is less than 0.0001, and that the solution has converged there. A sequence of plots for a typical finite difference calculation is shown in Figure 3.15.a-d. Interestingly, the region where the solution has converged propagates in a "wavefront" from the area where the potentials are most defined, that is, from the corner where the driven gate and ground plane potentials, acting as Dirichlet boundary conditions, cause rapid determination of potential values in their neighborhood.

3.13 Results of Simulation

The program developed to simulate the lock and key can be instructed to calculate the response with either the permittivity or loss factor of the semi-infinite medium constant, and the other parameter incremented by steps along a range, generating contours of either constant permittivity or loss factor. Figure 3.16 shows such a

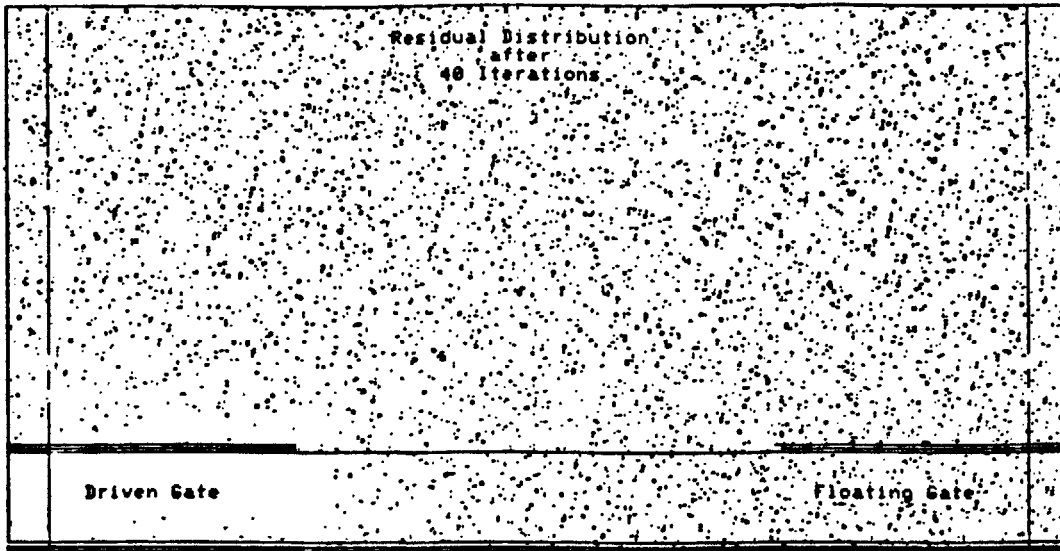


Figure 3.15.a Residue Distribution after 40 Iterations

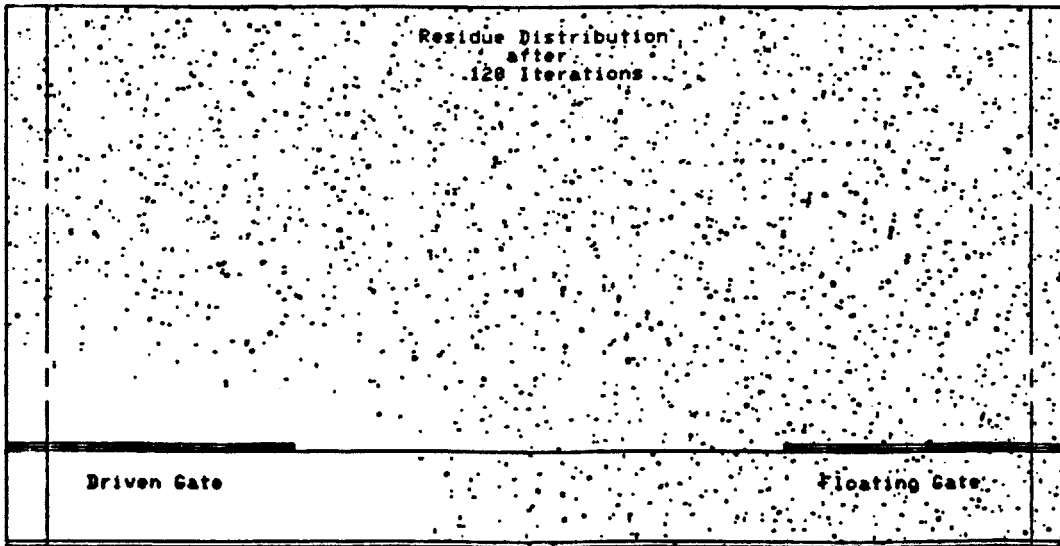


Figure 3.15.b Residue Distribution after 120 Iterations

set of calibration curves for a sensor with $W/H = 12.5$ and an FET load of 1.6 picofarads.

It can be seen that the sensor response, as calculated, behaves as expected from the simplified lumped element model of Figure 2.3. With an uncoated lock and key, the gain is minimized and the phase is zero. Similarly, if the semi-infinite region is lossless, the resulting voltage division remains purely capacitive, and pure dielectrics with permittivities greater than unity increase the device gain without introducing phase shift.

If, however, the semi-infinite medium is lossy, then the lock and key output develops negative phase relative to the input, with an accompanying increase in gain. This response is expected by analysis of the lumped element model. In the extreme case of a highly conductive resin, the electrodes are effectively shorted, and the sensor gain is unity with zero phase shift.

On a purely qualitative basis, then, the results of complex finite difference modeling yield the expected lock and key responses not only in the limits of lossless and conductive mediums, but also in the intermediate case of a resistive material, where the loss factor, and progression of the output response along a contour of constant permittivity, are continuous functions of frequency.

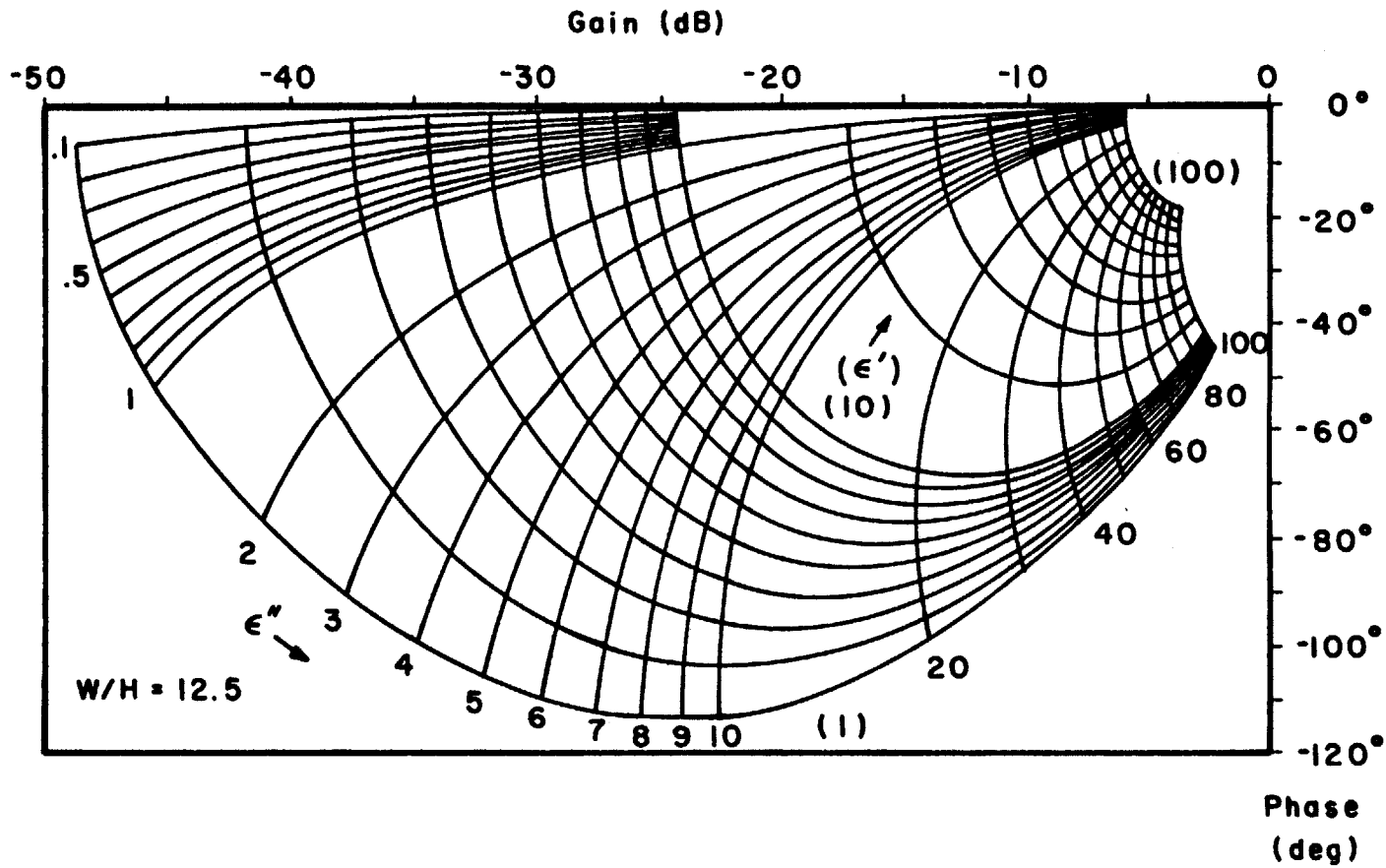


Figure 3.16 Calibration Curves for the Lock and Key with an FET Load of 1.6 pF

Figure 3.17 plots the electrode capacitances, as defined in Figure 2.3, for the uncoated lock and key as a function of the geometric variable W/H . It can be seen that the electrode capacitance to ground cannot be described by the parallel plate equation, and that for W/H less than 10, this capacitance can be several times greater than for parallel plates. Both C_{11} and C_{12} , the electrode capacitance to ground and the inter-electrode capacitance, are shown, and can be used with the model of Figure 2.3 to calculate the intrinsic lock and key gain. Knowledge of the FET load then makes possible calculation of the gain for the uncoated floating gate CFT sensor.

When electric field is computed from equations [3.5.1] and [3.5.2], it is possible to observe how electric field lines depend on loss factor. Likewise, interface charge can be calculated from equation [3.5.3]. Since all quantities in the simulation are represented as phasors, the spatial components of electric field have a sinusoidal time dependence. If the real part is extracted, then the result is the instantaneous field at the moment when the driven gate voltage is maximum. The field vectors of Figure 3.18.a then correspond to the direction of current flow at that time, and show that current travels away from the driven electrode in a highly two-dimensional manner. Figure 3.18.a is a map of the real part of electric field

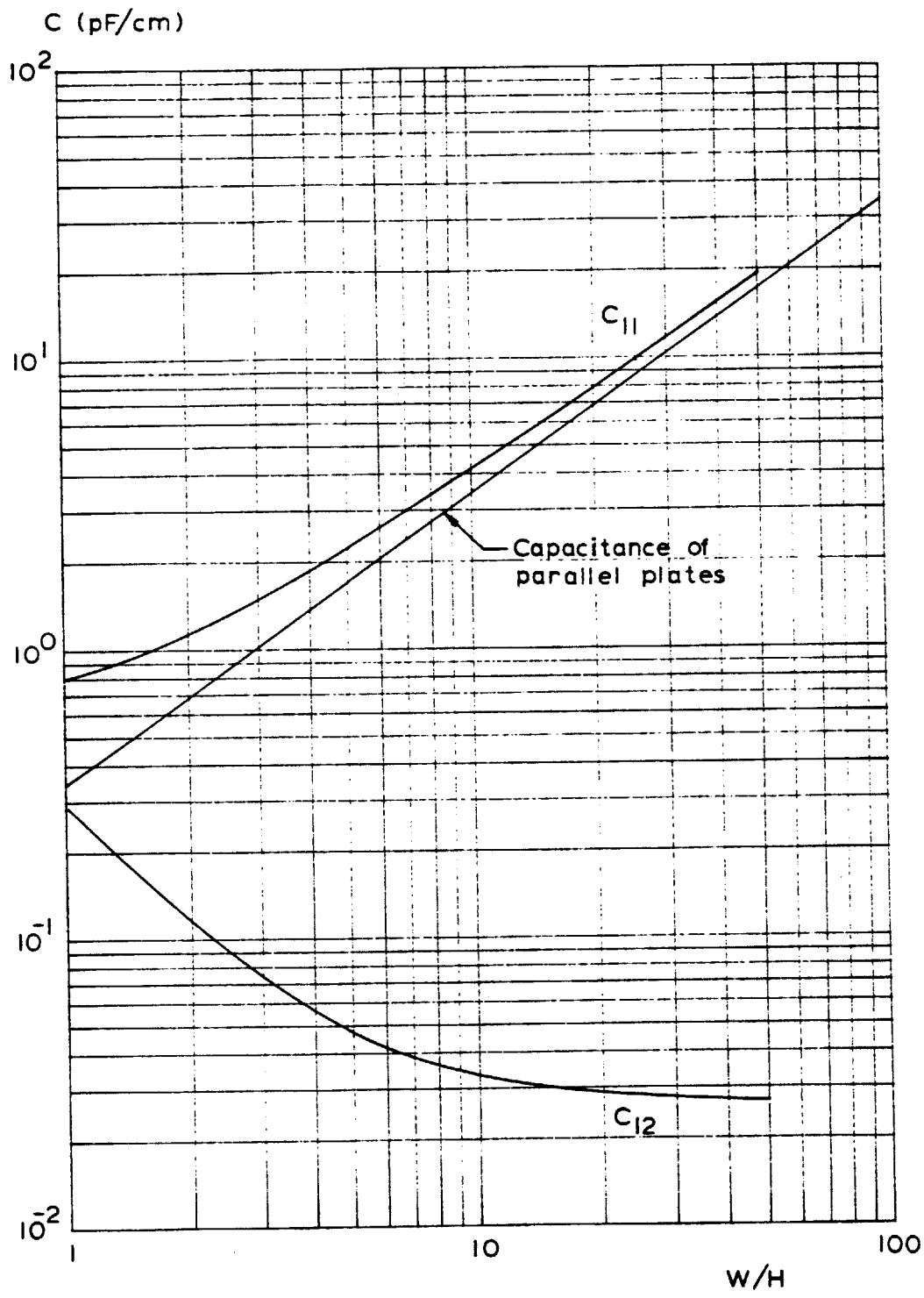


Figure 3.17 Electrode Capacitances of the Lock and Key in Air

for an uncoated lock and key, with the length of the vector proportional to the logarithm of the magnitude of the field. The inter-electrode coupling in this case is purely capacitive, and charge moves in the form of displacement current. Figure 3.18.b shows charge on the upper surface of the electrodes. For visibility, a charge phasor has zero phase in the 12 o'clock position and positive phase in the counterclockwise direction. The charge phasor, like the field vector, has a length proportional to the logarithm of its magnitude.

If charge on top of the driven electrode is considered positive, then the 180° phase of charge on top of the floating electrode may be interpreted as negative. This polarity is consistent with idea of the lock and key as a planar capacitor, for the upper surface of the electrodes, as two facing plates, should have opposite charge. As calculated, in this situation with no loss, no charge exists at all along the dielectric interface.

The sequence of Figures 3.19-3.21 depicts how the real part of the electric field changes while the permittivity of the semi-infinite medium is maintained at unity and the loss factor is increased from 1 to 100. The insulator beneath the electrodes is silicon dioxide, and is modeled with a loss factor of 0.0 and a permittivity of 3.9. The corresponding gain and phase of the floating

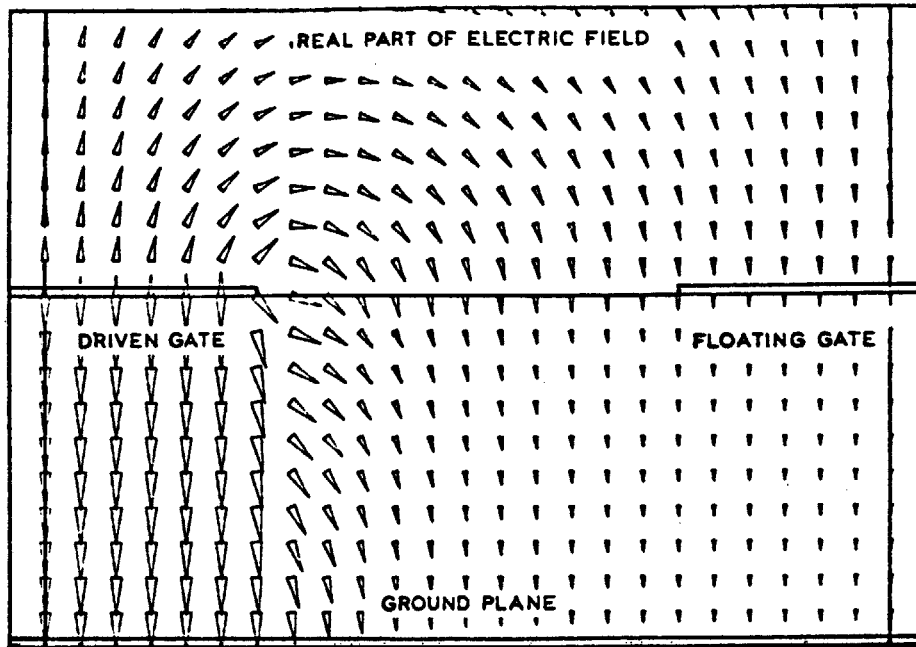


Figure 3.18.a Electric Field; Permittivity of Semi-Infinite Region = 1.0,
Loss Factor = 0.0

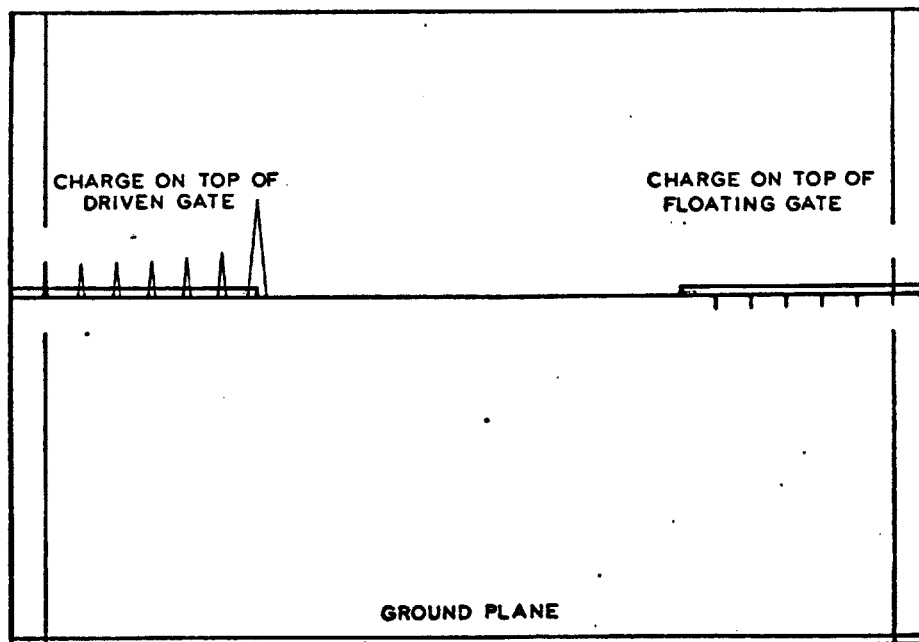


Figure 3.18.b Interface charge on Top of Electrodes, Same Conditions
as Figure 3.18.a

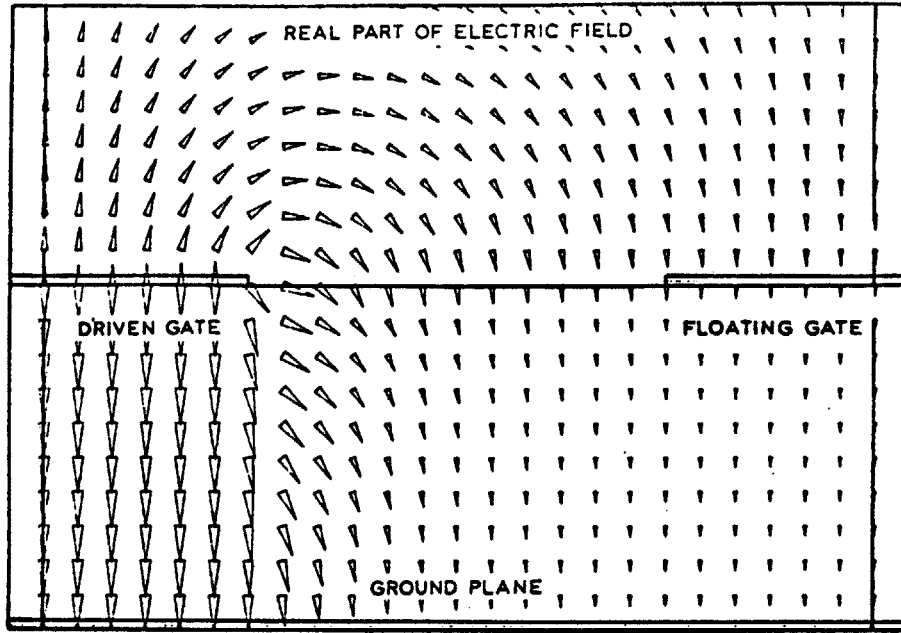


Figure 3.19.a Electric Field; Permittivity of Semi-Infinite Region = 1.0, Loss Factor = 1.0

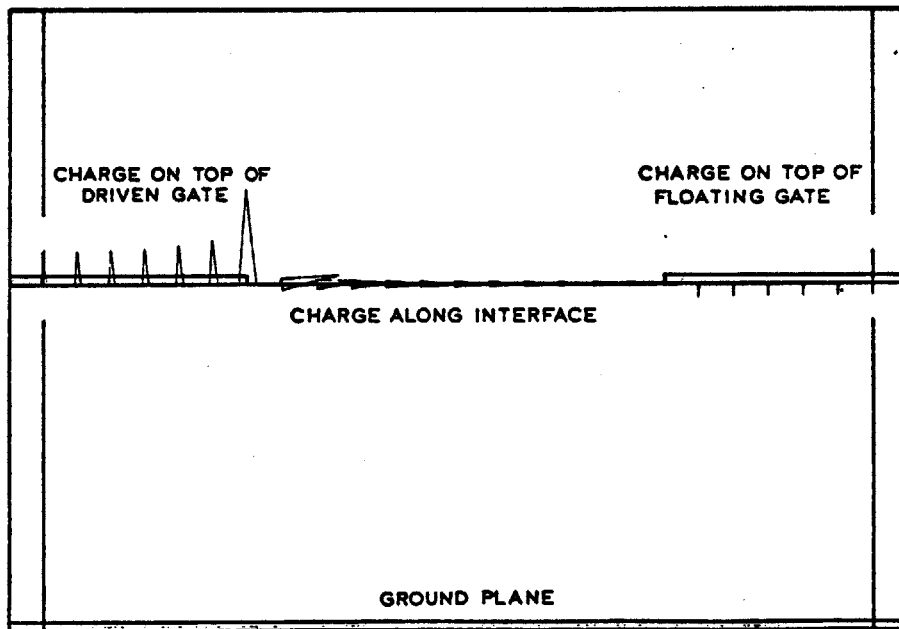


Figure 3.19.b Interface Charge, Same Conditions as Figure 3.19.a

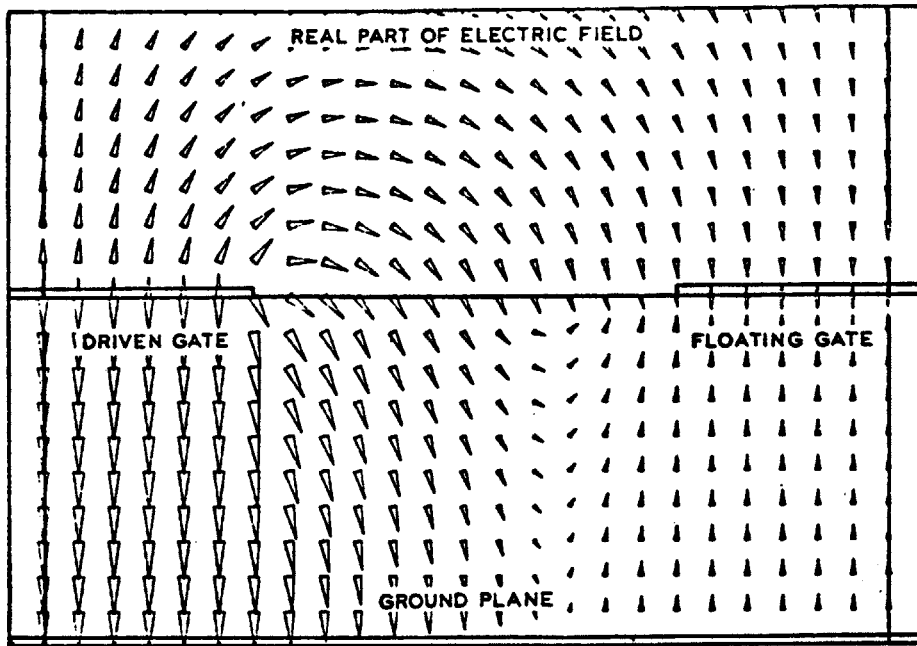


Figure 3.20.a Electric Field; Permittivity of Semi-Infinite Region = 1.0,
Loss Factor = 10.0

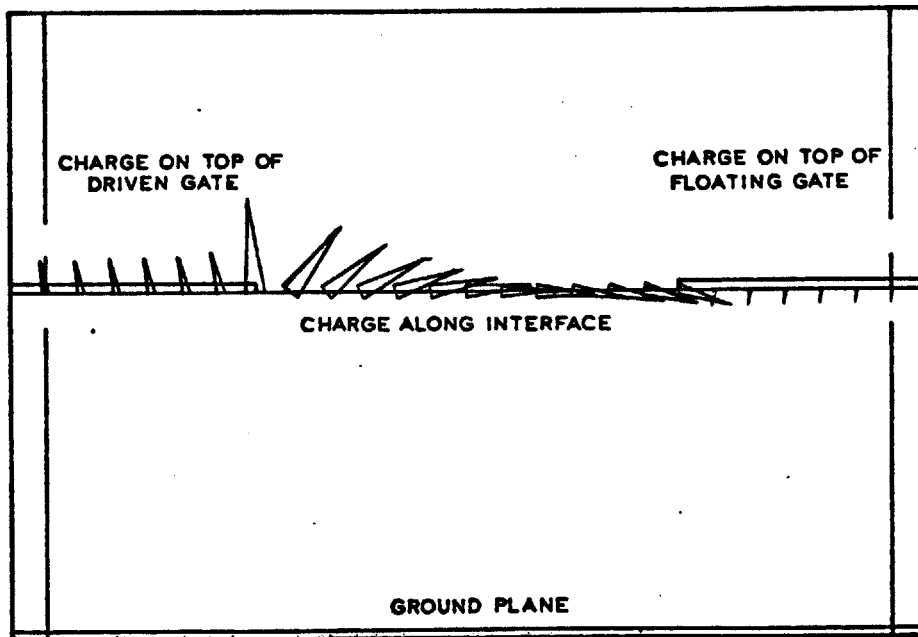


Figure 3.20.b Interface Charge, Same Conditions as Figure 3.20.a

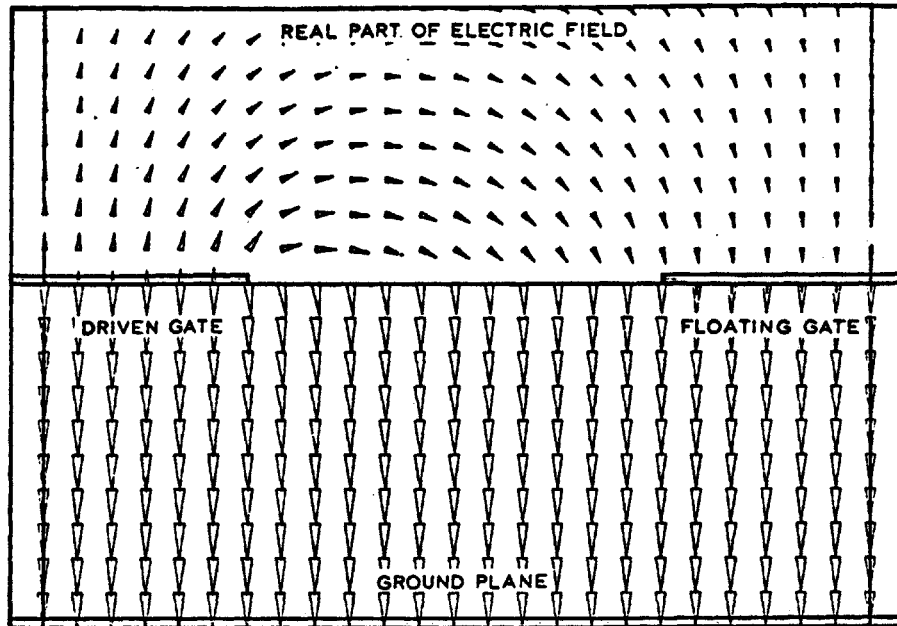


Figure 3.21.a Electric Field; Permittivity of Semi-Infinite Region = 1.0,
Loss Factor = 100.0

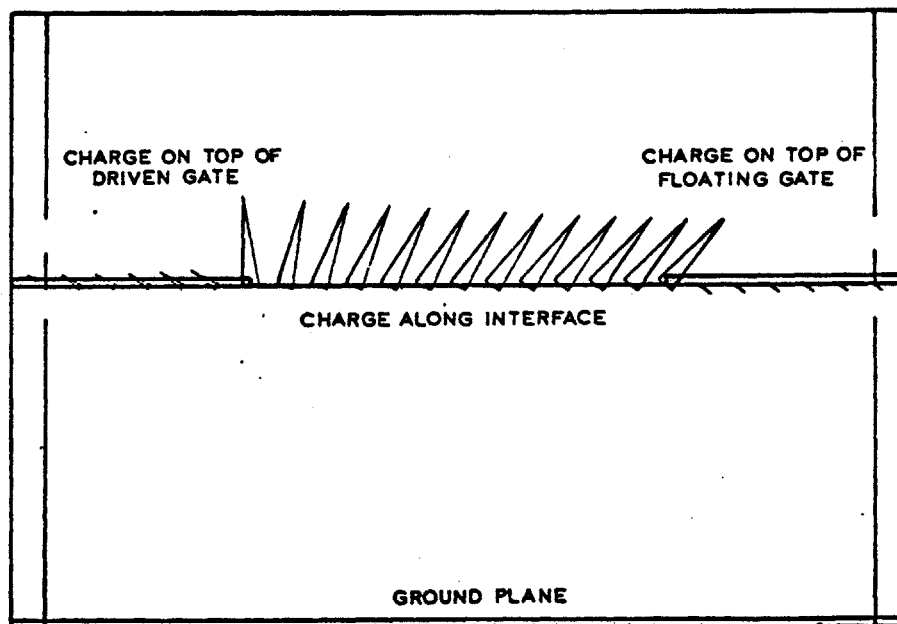


Figure 3.21.b Interface Charge, Same Conditions as Figure 3.21.a

gate can be determined from the calibration curves of Figure 3.16, for the same geometry was used in the simulations.

Interface charge does not appear until the first introduction of loss, and when the loss is small, this charge is -90° out of phase with the driven gate charge. As the loss grows larger, the electric field draws closer to the dielectric interface. The interface charge not only grows in magnitude, but also begins to shift toward the direction of less negative phase, with a resultant increase in its real component.

Interestingly, in Figure 3.20.a, for a loss factor of 10, the electric field in the silicon dioxide actually reverses direction in going from the driven to the floating electrode. This phenomenon should be expected to occur whenever the output phase is more negative than -90° , and as can be seen in Figure 3.16, for the particular set of parameters used, the phase of the lock and key response is approximately -100° . The floating gate voltage has lagged so far behind the input that the real part has become negative. Physically, the time constant of the semi-infinite medium delays the charge transfer, and charge from one cycle is still flowing from the floating electrode as charge from the next cycle begins to arrive.

Finally, for very large loss, the semi-infinite medium has become more resistive than capacitive. Consequently, the driven and floating electrodes become strongly coupled, with only a small phase shift between them. In a sense, the electrodes begin to behave as if they are shorted together, and the lossy medium above the interface can be considered a single conductor, or the upper plate of a capacitor. As shown in Figure 3.21.a, the electric field in the semi-infinite medium is still very two-dimensional, but predominately confined to the area immediately above the interface. The field lines below the interface, however, are straight not only beneath the electrodes, but also in the region between them, as they would be between a pair of infinite parallel plates.

CHAPTER 4 EXPERIMENTAL WORK

4.1 Introduction

In order to verify the results of two dimensional simulation, it is necessary to correlate data from electrode structures of different geometry. Since the important parameter affecting the lock and key intrinsic--or unloaded--response is the width to height ratio, W/H , the floating gate CFT sensor has been redesigned to allow selection of electrode height during fabrication, without affecting other portions of the device.

Although it is possible to vary electrode separation from the ground plane simply by growing field oxides of different thicknesses, the maximum practical thickness of one micron severely limits the range of W/H which can be obtained. The new sensor design is a double level metal structure which employs polyimide as an additional insulating layer between the electrodes and thermal oxide. This chapter presents the experimental device design and discusses the pertinent issues involved with the use of polyimide in this application, particularly the problem of fabricating inter-level contacts. Device calibration and experimental procedure are also discussed.

4.2 Polyimide as an Inter-level Insulator

Polyimide is a polymeric material designed for use in semiconductor and thin-film hybrid electronic fabrication. As a coating, it acts as an insulating layer for passivation or multilevel metallization. Since polyimide is applied as a viscous liquid and then spun, it provides excellent step coverage and layer uniformity across a wafer. The film can be selectively etched and, when fully cured, is mechanically tough. The device fabrication for this thesis used ultra-pure Du Pont Polyimide 2555, which has a lower viscosity and solid content than the previous formulations. Fully cured PI-2555 has the properties outlined on Table I [41].

Partially cured polyimide can be patterned with dilute alkaline solutions, and when a positive photoresist such as AZ1350-J is developed, etching of polyimide occurs simultaneously. Wet etch techniques, however, leave a highly resistive film, or "invisible shield," which causes open contacts in the vias of interlayer metal connections.

Day and Senturia [42] have investigated this problem in polyimide patterned with oxygen plasma. Auger analysis in conjunction with compositional depth profiling was used to determine the surface characteristics of plasma-etched vias, and led to the conclusion that the plasma deposits

TABLE I
 PROPERTIES OF POLYIMIDE 2555 [41]

<u>Physical</u>	<u>PI-2555</u>
Tensile Strength (Ultimate)	19,000 psi (1.31 X 10 ⁸ pascal)
Elongation	10%
Density	1.39 gm/cm ³
Flexibility	180° bend, no cracks
<u>Thermal</u>	
Melting Point	None
Weight Loss @ 316 °C in Air after 300 Hrs.	4%
Final Decomposition Temp.	560 °C
Coefficient of Thermal Expansion	4.0 X 10 ⁻⁵ / °C
Coefficient of Thermal Conductivity	3.5 X 10 ⁻⁴ cal/cm-sec °C
<u>Electrical</u>	
Dissipation Factor (1 KHz)	.002
Dielectric Strength	4000 volts/mil
Volume Resistivity	10 ¹⁶ ohm-cm
Surface Resistivity	10 ¹⁵ ohm-cm
Dielectric Constant (nominal)	3.5

an etch-resistant carbonaceous film in the contact areas and produces an abnormally thick aluminum oxide layer on the first level metal surface. This invisible shield can be removed by a low pressure plasma in the range of 50 mTorr, followed by chemical thinning of the aluminum oxide in buffered hydrofluoric acid.

Wet etching does not deposit a carbonaceous film, but instead simply leaves a polyimide residue on the first level metal surface [43]. The same low pressure plasma treatment, followed by a buffered HF etch, will remove this residual layer.

4.3 Sensor Design and Fabrication

For the purposes of this thesis the floating gate CFT was redesigned to incorporate the following features:

1) Full coverage of source and drain metal with polyimide.

Complete passivation of the device is now possible by coating the bond wires with an insulating material, to eliminate the source of positive phase shift identified by Sheppard.

2) Guard rings surrounding source and drain metal.

The guard rings maintained at constant substrate potential will prevent or reduce stray surface currents that can affect measurements in thin film applications.

- 3) Probe pads for capacitance measurements of gate and field oxide thicknesses.
- 4) Repositioning of the reference FET to align its major axis with that of the CFT. Thus small misalignments during photolithography will affect the geometry of each transistor in the same way.
- 5) An on-chip diode temperature sensor. Temperature can be measured by monitoring the diode junction voltage at a constant current.
- 6) Interchangeable metal masks. A single-level metal pattern includes the lock and key with all other interconnections and metal features. A double-level metal pattern places the transistor gates, guard rings, source and drain leads and bond pads on the first level; the lock and key, additional guard rings and bond pads on the second level.

The metal gate NMOS process developed by Garverick was modified to include a field implant, allowing the use of low conductivity wafers. The fabrication sequence of a sensor using double-level metal and polyimide is illustrated in Figure 4.1.a-h.

- a) After the growth of approximately 100 \AA of dry oxide on a 10-40 ohm-cm wafer with 100 crystalline orientation,

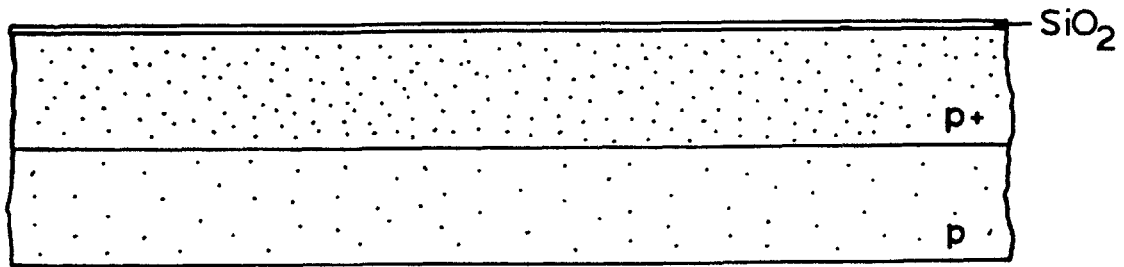


Figure 4.1.a Growth of 100 Å Oxide, Implant and Drive-in of Boron

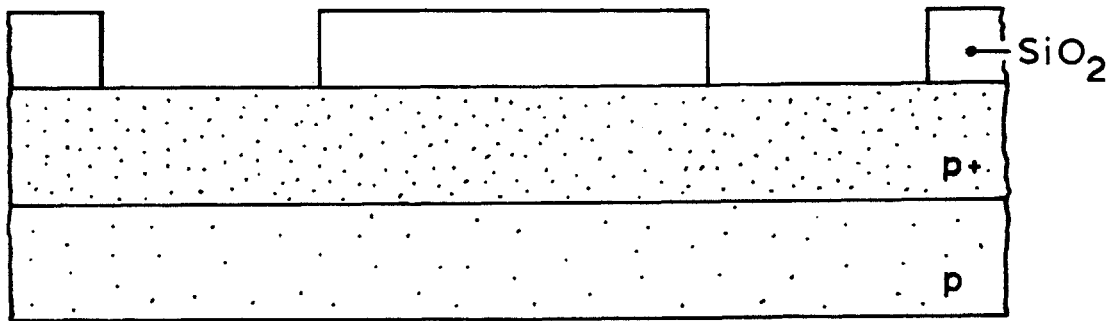


Figure 4.1.b Growth of Field Oxide, Definition of Source-Drain Regions

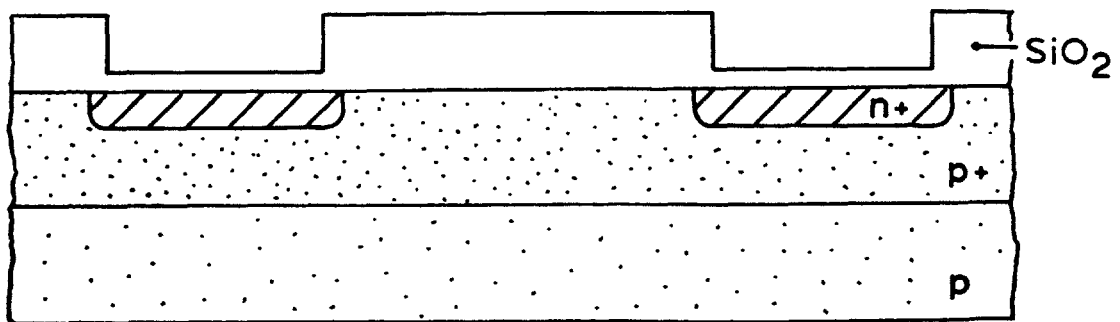


Figure 4.1.c Arsenic Implant, Oxide Growth and Implant Drive-in

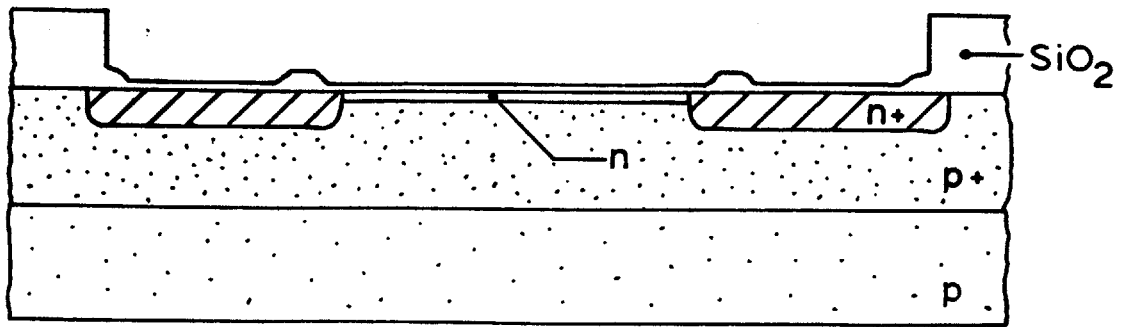


Figure 4.1.d Gate and Contact Regions Defined and Etched, Gate Oxide Grown, Implant and Anneal of Phosphorus

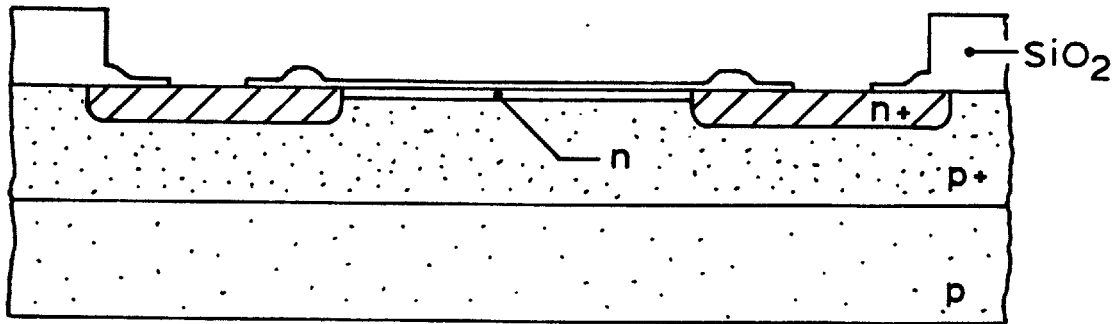


Figure 4.1.e Contact Areas Defined and Etched

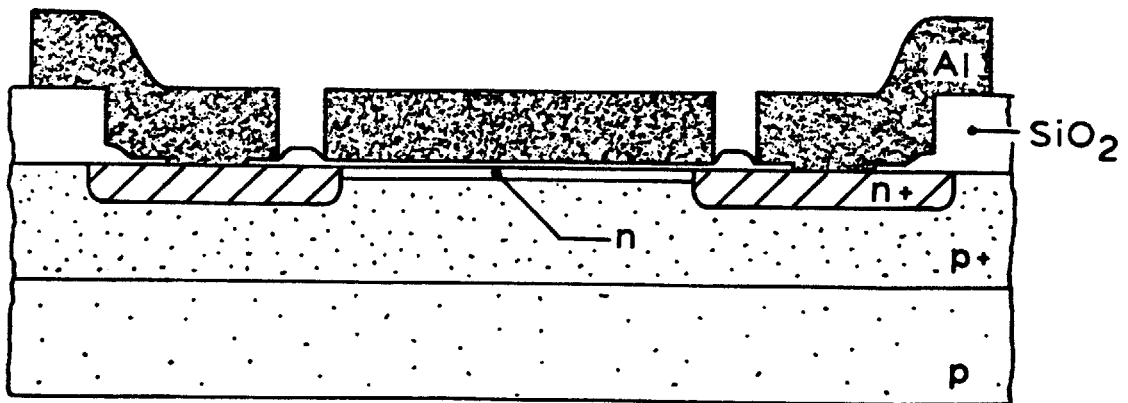


Figure 4.1.f First-level Aluminum Deposited and Patterned

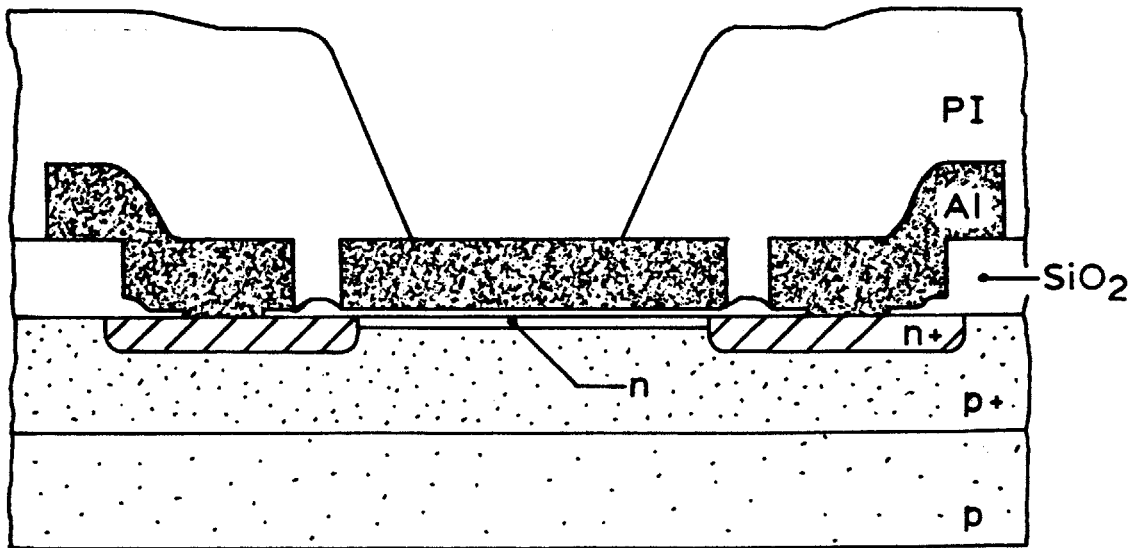


Figure 4.1.g Polyimide Deposited, Partially Cured, and Vias Etched

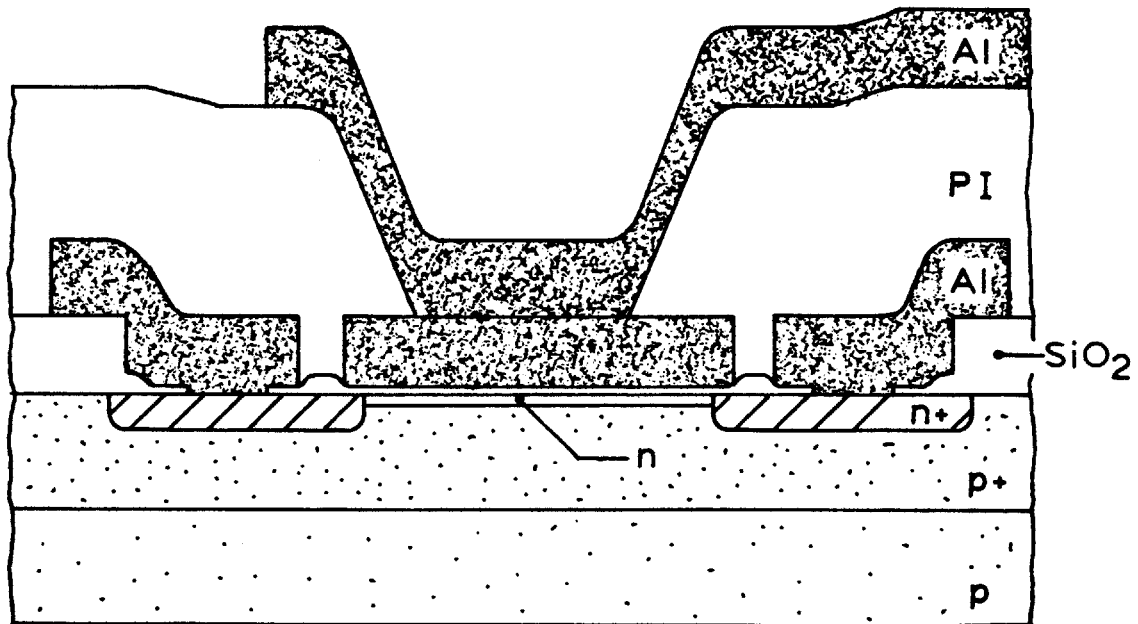


Figure 4.1.h Second-level Aluminum Deposited and Patterned

a boron field implant is performed to increase the surface layer conductivity. Following the drive-in and annealing steps, this high conductivity region, extending about 0.5 microns into the substrate, results in a high positive field threshold to avoid inadvertent field inversion. In addition, the precision with which specified doses can be implanted permits greater wafer-to-wafer field uniformity and smaller deviation in the transistor threshold voltage.

b) Approximately 0.75 microns of wet oxide, and then a final dry oxide layer are grown. Negative photoresist is applied, and the source, drain and diode moat regions are defined with the diffusion mask. Oxide from the diffusion areas is etched with buffered HF.

c) A high dose arsenic implant creates n+ type source and drain regions. A thin wet oxide layer is grown to prevent dopant out-diffusion during the subsequent anneal and drive-in process.

d) Negative resist is applied, the gate and contact regions are defined with the thin oxide mask, and then etched with buffered HF. Subsequent growth of a 1000 Å dry oxide layer forms the gate oxide. An additional application and patterning of positive photoresist, with the contact mask, protects the contact cuts and prevents the formation

of p-n junctions from the channel implant. A phosphorous channel implant is performed, and then the implant is annealed.

e) Negative photoresist is applied, and patterned with the contact mask. Contact areas are defined and etched with buffered HF.

f) The first-level aluminum is deposited. Positive photoresist is applied and patterned with the first-level metal mask. The aluminum is defined with a phosphoric-acetic-nitric acid etch.

g) Polyimide is applied and partially cured. Positive photoresist is applied, patterned with the via mask, and developed. The polyimide is simultaneously etched to form the vias which will connect first and second level metal. The photoresist is stripped in acetone.

h) The invisible shield in the vias is treated with low pressure oxygen plasma and a subsequent etching in buffered HF. The second-level metal is deposited. Positive photoresist is applied. The metal is defined with the second-level metal mask and etched. It is necessary to have the bond pads on both first- and second-level metal, with a contact area through the polyimide. Otherwise, etching of the first-level bond pads will occur. Experiments

during the course of this work demonstrated that it is not possible to bond to pads resting on polyimide, perhaps because the plastic resiliency absorbs the ultrasonic energy from the bonder.

Devices were fabricated in the MIT Microelectronics Laboratory with field oxide thicknesses of 0.45 and 0.75 microns. Texas Instruments also made single-level metal devices with 0.85 microns of field oxide.

After the application of polyimide and the second-level metal, four types of devices were available: single-level metal sensors with 0.45 and 0.85 microns of field oxide, and double-level metal sensors with 0.75 microns of field oxide and either 0.91 or 1.40 microns of polyimide.

Figure 4.2.a is a microphotograph of a sensor with the lock and key patterned on single-level metal. Figure 4.2.b is a microphotograph of the sensor with double-level metal and a polyimide/oxide insulating layer. The dark areas in the metal of Figure 4.2.b correspond to portions of first-level metal, exposed by vias in polyimide, which were subjected to the invisible shield removal treatment. The granular appearance results from aluminum oxide thinning with HF, which preferentially attacks aluminum along the grain boundaries and leaves a roughened surface.

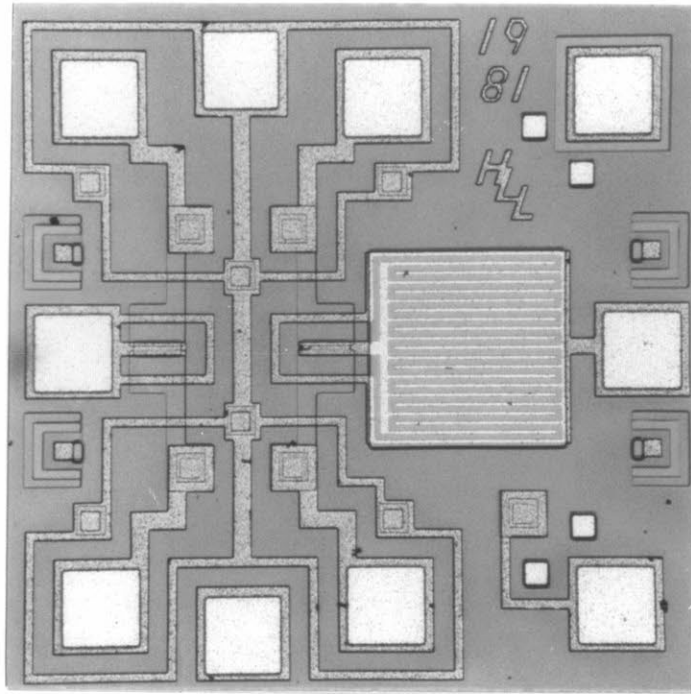


Figure 4.2 a. Microphotograph of Sensor with Single-level Metal Design (50 X)

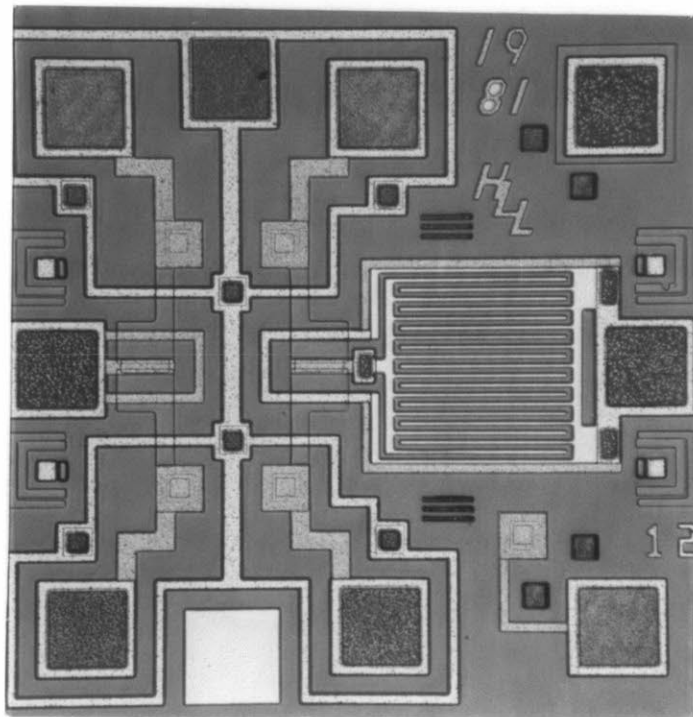


Figure 4.2 b. Microphotograph of Sensor with Double-level Metal Design (50 X)

The scanning electron microscope photograph of Figure 4.3 highlights the second-level metal on top of the polyimide. The contact pad connected to the floating gate electrode is clearly visible, and shows how electrical connection is made through a via to the gate of the transistor. Figure 4.4.a is an SEM microphotograph of this contact area at 1,200 X magnification. The smooth second-level metal around the contact cut is in contrast with the roughened area of the contact itself, which is second-level metal conforming to the chemically attacked surface of the first level.

Apparently the polyimide prebake step should have been longer than the 60 minutes used during fabrication of this device, for the polyimide etched very quickly, leaving a sharp step at the edge of the contact cut. Polyimide which has been cured somewhat longer would have a definite slope, or bevel, instead, and would provide smoother step coverage. The SEM microphotograph of Figure 4.4.b is an extreme close-up of the contact cut edge at 10,000 X magnification. The second-level metal is ragged at the step, and shows the cusping typical of coverage over large, sharp steps. Aluminum is thinnest there, and is a site of possible contact failure. In these devices, however, breakage should not be a problem with the low currents directed into the floating gate, for the use of

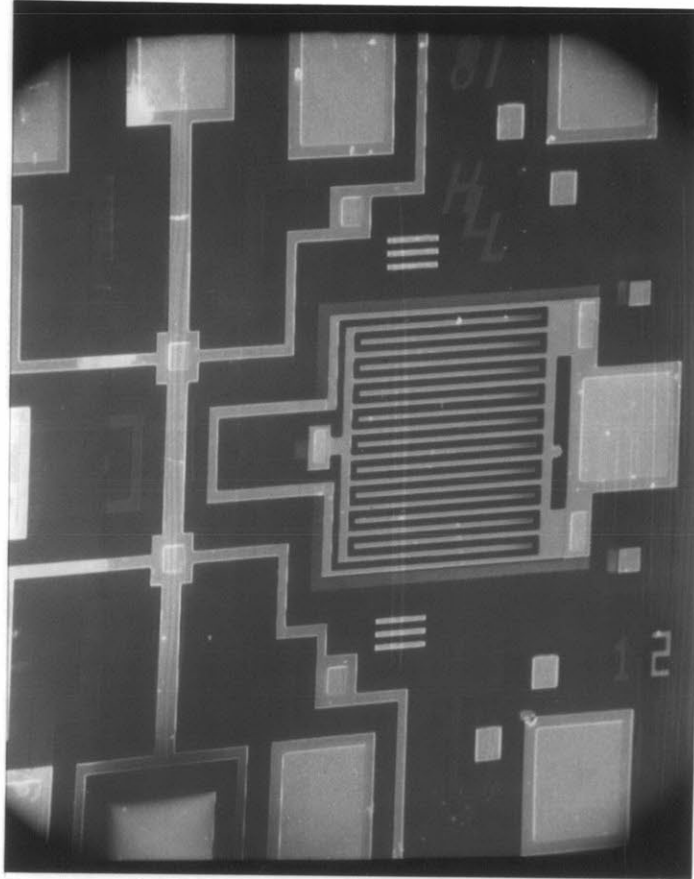


Figure 4.3 Electron Microphotograph of Sensor with Double-level Metal Design

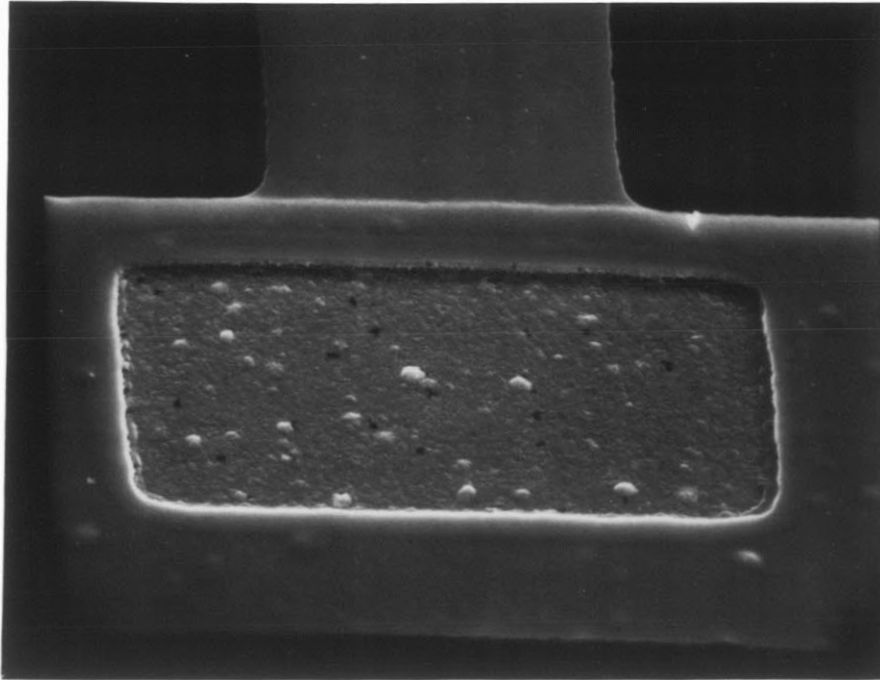


Figure 4.4 a. Electron Microphotograph of Via through Polyimide and Connection of Second-level Metal to the Floating Gate (1,200 X)

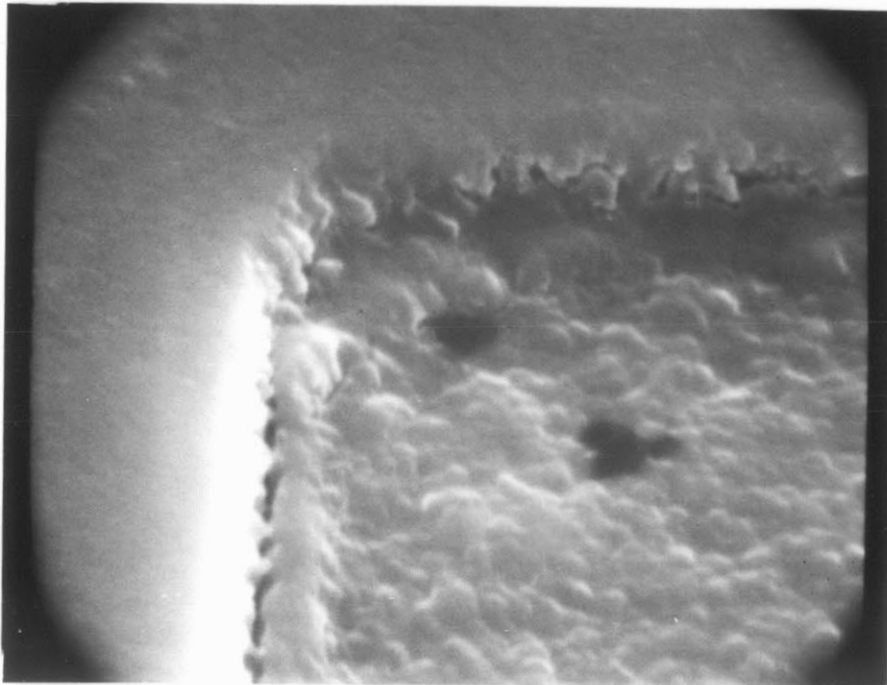


Figure 4.4 b. Electron Microphotograph of Second-level Metal at Via Edge (10,000 X)

sinusoidal AC signals centered at 0 V avoids electromigration. Also, because the sensor is employed in resin cure monitoring and later, occasional in-situ probing, it does not operate for long periods of time, and has only a relatively short requirement for useful device life.

4.4 Sensor Characterization

Only four quantities are necessary to simulate the uncoated lock and key. They are 1) ϵ_2' , the permittivity and σ_2 , the conductivity of the insulating layer; 2) W/H, the ratio of electrode width to electrode height above the ground plane; 3) M, the length of the meander between electrodes; and 4) C_L , the load capacitance.

Since polyimide has a typical dielectric permittivity of 3.5, for simplicity it is assumed that the overall permittivity of the composite oxide/polyimide field is 3.9, or that of oxide alone. According to simulation results, when the insulator has a dielectric constant of 3.5, the response of an uncoated lock and key is about 1 dB, or 12% greater than when the insulator has a dielectric constant of 3.9. A correct value for the effective permittivity of the composite field will be somewhere between that of polyimide and silicon dioxide, and can be modeled as capacitances of two different dielectric constants in series. Assuming this effective permittivity is 3.7, the

simulation calculates the response of an uncoated lock and key to be only 0.5 dB, or 6%, greater than a pure silicon dioxide field.

Field oxide thickness was determined with a Sloan Dektak by measuring the step from the top of the field region to bare silicon in the scribe line. Total insulator thickness was measured in the same way after deposition and full cure of the polyimide. Since the electrode finger width is fixed by the photolithographic mask pattern, the W/H ratio can be calculated.

The length of the meander, M , between electrodes is defined to be the length, measured in the center of the 12.5 micron gap which separates the floating and driven gate. The extra length where the meander turns a corner accounts in a rough way for the small coupling at the ends of the electrodes, which is estimated to be about 5% of the total.

The load capacitance is determined by the parallel plate capacitor equation applied to the FET gate. This calculation requires knowledge of the gate oxide thickness, the gate metal area and the geometry of the entire electrode. Table II lists the quantities used to simulate sensor behavior, and obtain the theoretical intrinsic gain for the four types of devices used in experiments for this work.

TABLE II
SENSOR GEOMETRY

Type of Sensor	A	B	C	D	<u>Units</u>
<u>Field</u>					
SiO ₂ Thickness	0.45	0.85	0.75	0.75	μm
PI Thickness	0.00	0.00	0.91	1.40	μm
Total Thickness (H)	0.45	0.85	1.66	2.15	μm
Permittivity	3.9	3.9	3.9	3.9	
<u>Electrode</u>					
Width	12.5	12.5	12.5	12.5	μm
W/H	27.8	14.5	7.5	5.8	
Meander Length (M)	0.5	0.5	0.5	0.5	cm
<u>Transistor</u>					
Gate Oxide Thickness	820	1150	820	820	Å
Area over Gate Oxide	4.8 X 10 ⁻⁵	4.8 X 10 ⁻⁵	4.8 X 10 ⁻⁵	4.8 X 10 ⁻⁵	cm ²
Floating Gate Area Excluding Fingers	4.8 X 10 ⁻⁵	4.8 X 10 ⁻⁵	8.0 X 10 ⁻⁵	8.0 X 10 ⁻⁵	cm ²
Permittivity	3.9	3.9	3.9	3.9	

4.5 Data Extraction

With only the dielectric permittivity of the field, and W/H , the finite difference simulator can calculate for a specific value of resin permittivity and loss factor the two-port admittance parameters of the intrinsic, unloaded lock and key. For purposes of data extraction, a table of admittance parameters is generated for a range of ϵ' from 2^0 to $2^{8.5}$, and ϵ'' from 2^{-6} to $2^{9.5}$. Both the permittivity and loss factor of the semi-infinite medium are incremented by a factor of $2^{1/2}$, resulting in 18 values of ϵ' and 32 values of ϵ'' .

Once the table of admittance parameters is obtained for the intrinsic lock and key, it can be used to calculate the response of a particular electrode configuration with its load. Since the parameters are stored as picofarads/centimeter or mhos/centimeter of meander, the meander length is required to scale these admittances properly. The effect of the load is then calculated as described in section 3.10.

A new table is subsequently generated, with indices which identify the values of permittivity and loss factor, and stored data which are the corresponding gain and phase of the sensor response. A different admittance parameter table can be generated for each type of sensor which has

been fabricated, and converted as just described. An interpolation routine can then search the appropriate table and extract ϵ' and ϵ'' from raw gain-phase data.

4.6 Experimental Procedure

The experiments performed for this thesis were designed to ascertain the accuracy of calibration from look-up tables generated by the simulation program. Agreement between sensors with different geometries would indicate that the quantities being extracted are material properties of the semi-infinite medium, and that the variable of electrode configuration is accounted in the calibration.

The four types of devices fabricated for this work varied only in the insulator thickness beneath the lock and key. Insulator thicknesses were 0.45, 0.85, 1.66 and 2.15 microns. With an electrode width of 12.5 microns, the W/H ratios were 27.8, 14.7, 7.5 and 5.8, and represented a wide choice of geometries.

The gain and phase response of the four types of sensors were measured over a range of frequencies with different lossless and lossy dielectrics. Permittivity calibration was performed with air, clear RTV silicone rubber, cured polyimide, cured DGEBA/MPDA resin, and DGEBA in the form of commercial products DER 332 and Epon 828. These dielectrics have known permittivities that were

compared with the values obtained from the sensor. Loss factor calibration was performed by measuring the frequency dependence of ϵ'' for DER 332 and Epon 828, to determine the agreement between different device geometries. In addition, the cure of a resin was monitored to obtain information for comparison across several orders of magnitude of permittivity and loss factor.

The resin used in the cure experiment of this thesis was Dow DER 332, which is diglycidyl ether of bisphenol-A, or DGEBA. Its epoxide equivalent weight is 176. The curing agent was meta-phenylene diamine, or MPDA, with an equivalent weight of 27. Stoichiometric amounts of the two substances were melted separately on a hot plate at about 60 °C, mixed together and cooled rapidly to prevent reaction. The DGEBA/MPDA mixture was stored in a refrigerator and used within two days of mixing. This resin/amine system was selected because it is well characterized, and because it appears to obey a simple Debye model up to gelation.

The epoxy cure was monitored with the automated system developed by Sheppard, with the resin in an oven set at 80 °C. Four devices, each with a different field insulator thickness, were used. The same Analog Devices AD 590 PTAT temperature sensor was employed in each case to monitor oven temperature. To determine if the device was working

properly, the gain and phase of each CFT was measured at seven different frequencies before the start of the experiment. A small amount of DGEBA/MPDA mixture was placed on each device, and the measurement program was initiated. The gain and phase of the CFT response were measured at 1, 3, 10, 30, 100, 300 and 1000 Hz, and were stored on cassette tape for later analysis.

CHAPTER 5 EXPERIMENTAL RESULTS

5.1 Introduction

This chapter presents the results of experiments designed to verify the finite difference simulation of the floating gate CFT sensor. Correct calibration is essential for interpretation of raw gain-phase data as dielectric permittivity and loss factor, and is the first step toward understanding how changes in the electrical properties of curing resins can be related to specific chemical processes.

The transistors fabricated in the MIT Microelectronics Laboratory have been characterized, and their offsets and mismatches have been assessed. The four types of sensors used in experiments have W/H ratios of 5.8, 7.5, 14.7 and 27.8. As will be shown, the gains of uncoated devices agreed excellently with theoretical expectations.

Two major parasitic effects can affect data obtained with the sensor. The first originates from a stray conductive path to ground, identified by Sheppard, and causes positive phase shift in the early part of cure when the resin is highly conductive. Complete passivation of the sensor eliminates this problem. The second parasitic effect is a large substrate resistance which, in conjunction with the body effect of the transistors, is the source of

positive phase shift when the floating gate signal is very small. This effect is related to the substrate sheet resistance and has sufficient consistency from device to device to allow its removal from gain-phase information with appropriate data processing.

Preliminary tests of the on-chip temperature sensor indicates that it can be useful as a thermometer over at least the range from 20 °C to 150 °C.

Permittivity and loss factor measurements with all four types of CFT sensors were made for a number of dielectric materials, and were consistent over the range of W/H represented by the four devices. An experiment was performed to monitor the cure of the DGEBA/MPDA system, and again the correlation of extracted permittivity and loss factor between all types of devices was good.

Since the gain offset of the sensors was assessed to be approximately ± 0.2 dB, a consistently observed offset from the origin of -1 dB in the DGEBA/MPDA cure trajectory was determined not to be an artifact of the measurement technique, but instead is a real feature of the curing resin. Evidence from the literature [23],[24] indicates that electrode polarization and discharge can produce a blocking layer at the electrode-resin interface, and that this phenomenon causes the apparent measured permittivity and loss factor to have a frequency dependence which obeys

the Debye dielectric dispersion equations with a single relaxation time.

5.2 Transistor Characterization

The transistors for the floating gate CFT sensors were fabricated on low conductivity, 10-40 ohm-cm wafers. These wafers had received an initial field implant to create a high conductivity surface region. The process was modeled by the SUPREM process simulator [44] with measured and calculated results compared in Table III. Certain parameters in the SUPREM program were customized by Hamilton [45] to reflect the particular linear and parabolic growth rates observed in the furnaces of the Microelectronics Laboratory. When used in the process simulation with an interface charge density of 1.0×10^{11} , these adjusted parameters yielded good agreement between the measured and calculated transistor characteristics.

The sensors with a field oxide thickness of 0.85 microns were fabricated by Texas Instruments. Their transistor parameters are not listed in Table III because the process schedule was not known, and a comparison with theoretical results is not possible.

Notably, devices fabricated with 0.75 microns of field oxide have thresholds of -3.7 volts, while those fabricated with only 0.45 microns of field oxide have

TABLE III

TRANSISTOR PARAMETERS

<u>Field Thickness</u>	0.45 m (Measured)	0.45 m (SUPREM)	0.75 m (Measured)	0.75 m (SUPREM)	<u>Units</u>
Q_{SS}	----	10^{11}	----	10^{11}	cm^{-2}
t_{ox} (Gate)	820	845	820	845	\AA
t_{ox} (Field)	0.45	0.42	0.75	0.77	μm
V_{th} (Field)	----	16.19	----	22.97	V
R_{SH}	----	1.6	----	2.0	$\text{K}\Omega/\text{Square}$
K' (Gain Factor)	6.5	----	8.2	----	$\mu\text{A}/\text{V}^2$
V_{th}	-2.18	-2.36	-3.67	-3.71	V
γ (Body Effect)	2.16	3.16	2.15	2.90	$\text{V}^{1/2}$
ϕ_B	0.6	0.7	0.7	0.7	V

higher thresholds of -2.2 volts. The only difference in the processing schedule was the period of wet oxidation to produce the necessary oxide thickness. The shorter growth time for the 0.45 micron devices resulted in less total boron segregation from the substrate into the silicon dioxide. Consequently, substrate sheet resistance is greater than for the 0.75 micron devices. Since the 0.45 micron sensors have a higher surface boron concentration, the prescribed phosphorus implant created transistors which have fewer n-type carriers in the channel. Those transistors which have thicker field oxides, because they have a lower surface boron dopant level, received proportionally greater compensation for the same channel implant dose, and therefore have channels with greater n-type doping, and more negative threshold voltages.

Typical transistor drain-source currents are plotted in Figure 5.1 as a function of gate-source voltage. Two I-V characteristics are shown, with V_{DS} constant at 0.01 volts and V_{BS} varied as a parameter from 0 to -5 volts in -1 volt increments. The devices represented were selected at random from different areas of the same wafer. Field oxide thickness was 0.75 microns. It can be seen that considerable variation in transistor parameters can occur between arbitrary devices. Figure 5.2 shows the I-V characteristics for a particular floating gate CFT

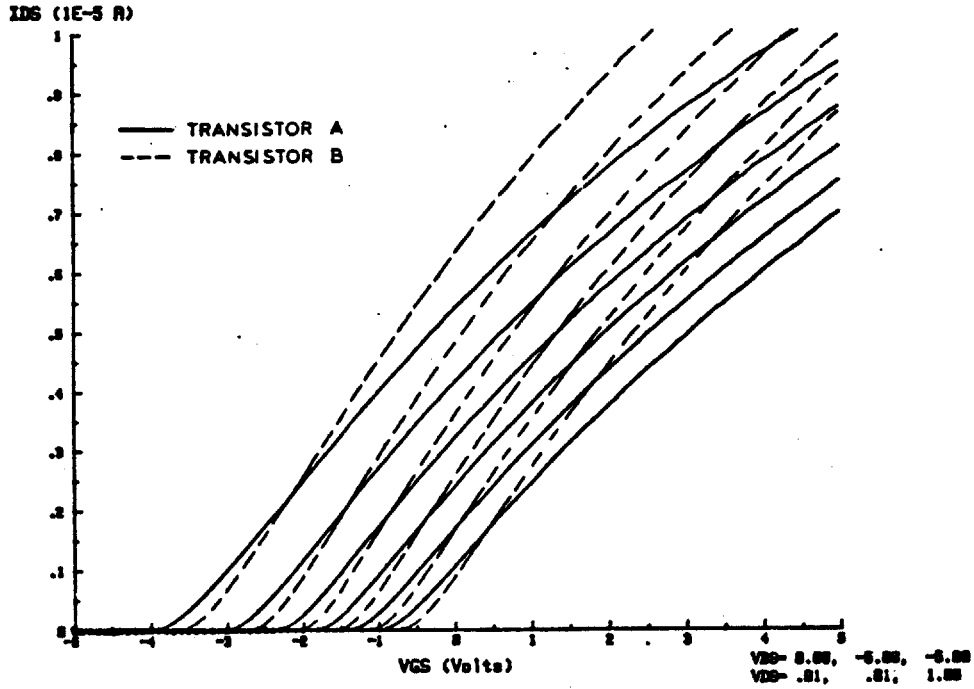


Figure 5.1 $I_{DS}-V_{GS}$ Characteristics for Typical Unmatched Transistors, Parameterized with Respect to V_{BS} from 0 V to -5 V

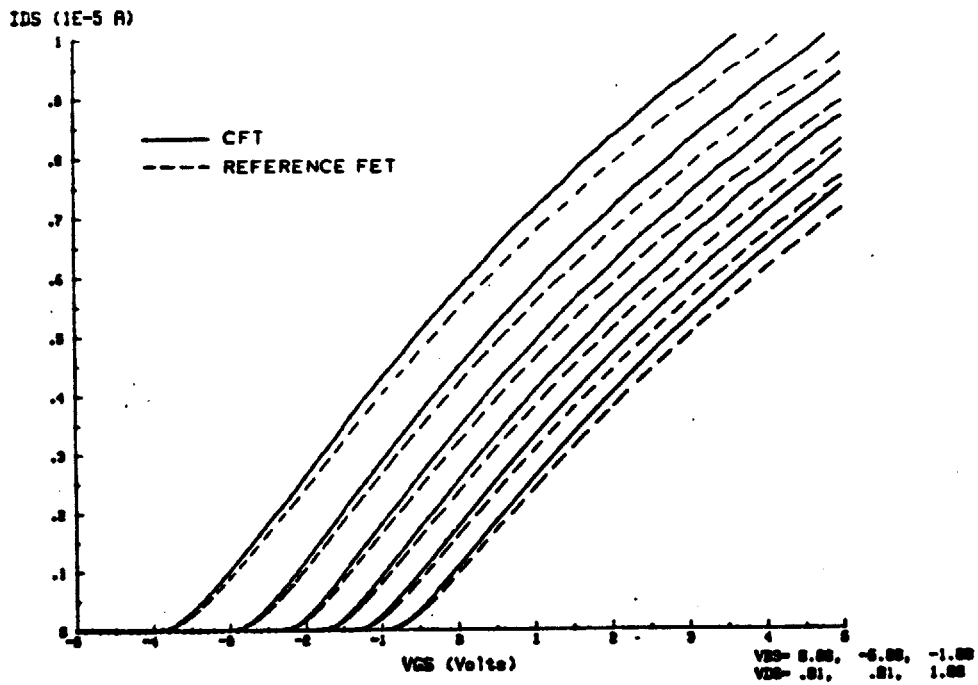


Figure 5.2 $I_{DS}-V_{GS}$ Characteristics for Typical Matched Transistors, Parameterized with Respect to V_{BS} from 0 V to -5 V

and its associated reference FET. The matching of transistor parameters is much better, and is the basis of the sensor's buffering ability.

For matched transistors, the DC voltage offset, the difference in gate voltages required to produce identical drain-source currents, is approximately 300 mV. More importantly, since the sensor operates with AC signals, the small-signal transconductances of matched devices differ from one another only by about two percent.

When the lock and key electrodes are shorted together, and the sensor is connected into the feedback circuit, the reference FET gate voltage ideally should be 0 dB relative to the CFT gate. Tested this way, the sensors fabricated in the MIT microelectronics laboratory show gain offsets in the range of ± 0.2 dB, with only one instance of an offset as large as -0.4 dB. The sensors fabricated by Texas Instruments exhibited very consistent gain offsets no greater than ± 0.1 dB. Thus the gain error of these resin cure sensors may be considered with good probability to be no more than ± 0.2 dB. In all cases, for devices tested as described, the phase offset was 0.0 degrees.

5.3 Sensor Characterization

With the geometrical quantities presented in Table III, it is possible to calculate the theoretical gain in air for each of the four types of CFT sensors. These devices have W/H ratios of 5.8, 7.5, 14.7 and 27.8. Fifteen sensors of each type were mounted on headers with silver filled epoxy and bonded with aluminum wire. The gain and phase for frequencies 1, 3, 10, 30, 100, 300 and 1000 Hz were measured for all uncoated devices in each group. A parasitic effect, which will be discussed later, caused positive phase shifts in the measurements. This effect, however, was removed after analysis of the problem revealed its cause. The gain recorded for each device was that obtained by data processing to compensate for the positive phase shift.

The average sensor gain for each group is compared with theoretical results in Table IV, and in all cases agreement is excellent.

5.4 Positive Phase Shift at the Beginning of Cure

Sheppard has observed in the early stages of resin cure that the sensor exhibits a positive phase shift and an attenuation which can be very severe. At the beginning of cure the resin is highly conductive and should short

TABLE IV
SENSOR PARAMETERS

<u>Type of Sensor</u>	A	B	C	D	<u>Units</u>
W/H	27.8	14.7	7.5	5.8	
ϵ_2' (Field)	3.9	3.9	3.9	3.9	
C_{11}	10.74	5.88	3.22	2.58	pF/cm
C_{12}	0.0280	0.0310	0.0370	0.0420	pF/cm
M	0.5	0.5	0.5	0.5	cm
C_{11}^* (C_{11} X M)	5.37	2.94	1.61	1.29	pF
C_{12}^* (C_{12} X M)	0.0140	0.0155	0.0185	0.021	pF
Intrinsic Gain ¹	-51.6	-45.7	-38.7	-35.7	dB
C_L	2.41	1.65	2.21	2.17	pF
Loaded Gain ²	-54.9	-49.6	-46.3	-44.4	dB
Experimental Gain ³	-54.9	-49.4	-46.4	-44.9	dB

1. Intrinsic Gain = $20 \log_{10} (C_{12} / [C_{11} + C_{12}])$

2. Loaded Gain = $20 \log_{10} (C_{12}^* / [C_{11}^* + C_{12}^* + C_L])$

3. Experimental Gain is averaged over measurements with 15 devices of each type.

the floating and driven gates together, with resulting measurements of 0 dB and 0 degrees phase. By identifying a stray conductive path from the driven gate, through the resin, to ground, Sheppard has explained this positive phase shift with the insertion of a lead network in the model of CFT operation. Figure 5.3.a illustrates the components of this lead network at the input port of the π -equivalent model for the sensor. Through exposed bond pads and wires, the stray conductive path to ground shunts part of the signal from the driven gate, consequently reducing the current reaching the floating gate, and decreasing the gain and causing positive phase. If all parts of the sensor were passivated, leaving only the lock and key exposed, this stray path and the positive phase shift should be eliminated.

As an experiment, a mounted sensor was passivated with polyimide covering the bond pads. After polyimide was fully cured, the bond wires were coated with RTV silicone rubber. This fully passivated chip left only the lock and key open to contact with resin. When uncured polyimide, which is highly conductive, was applied to the lock and key, the sensor showed negligible positive phase shift, and at high frequencies showed the expected negative phase that accompanies decreasing loss factor. When uncured polyimide was applied only onto the die of an

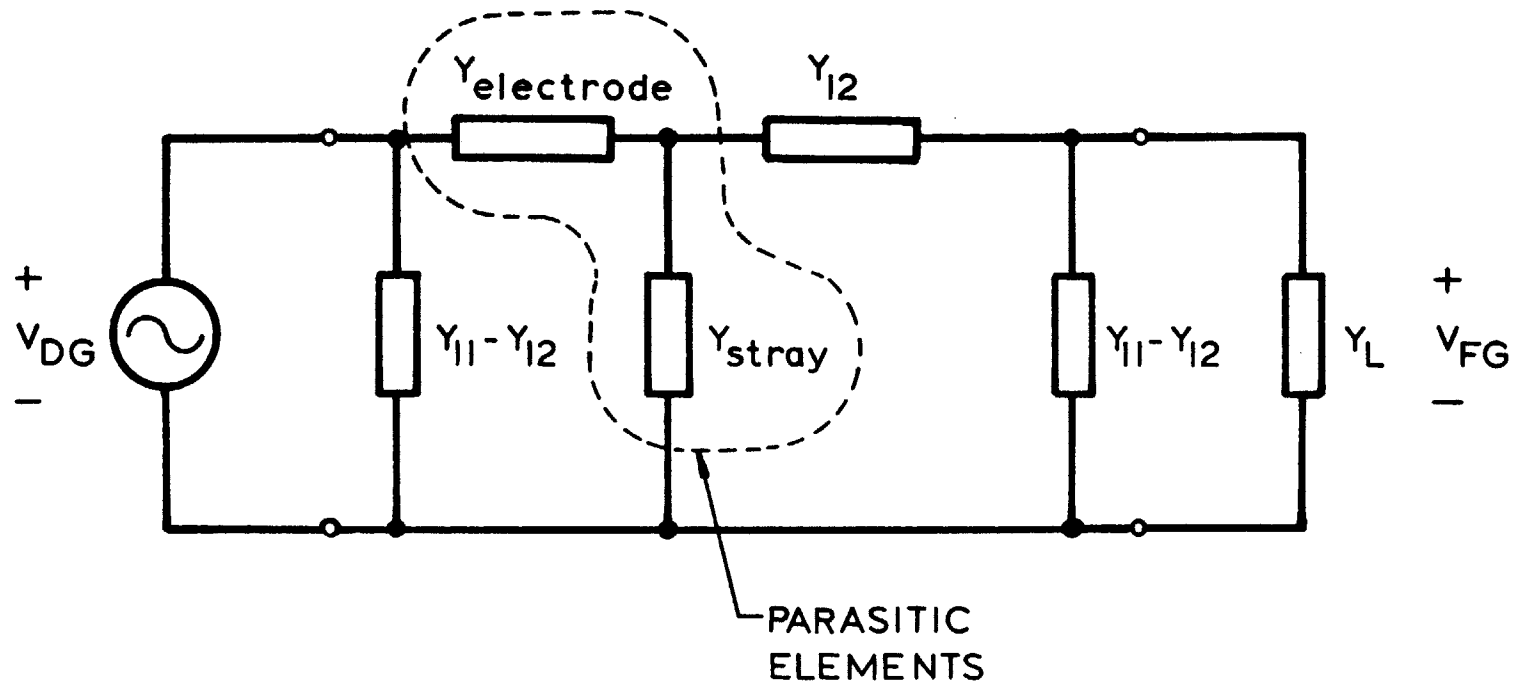


Figure 5.3.a Parasitic Elements Causing Positive Phase, Inserted in the Lock and Key Two-Port Admittance Model

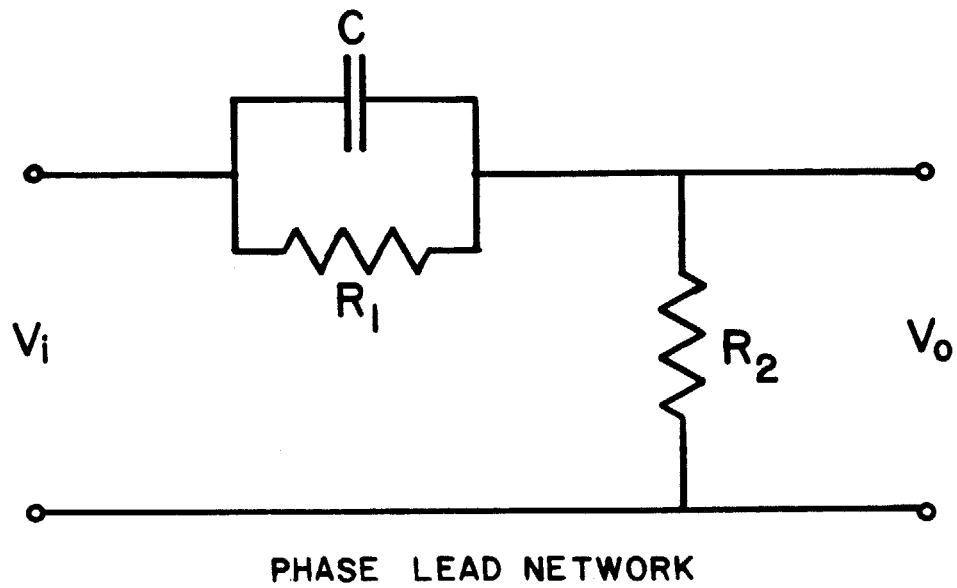


Figure 5.3.b Lead Network Elements

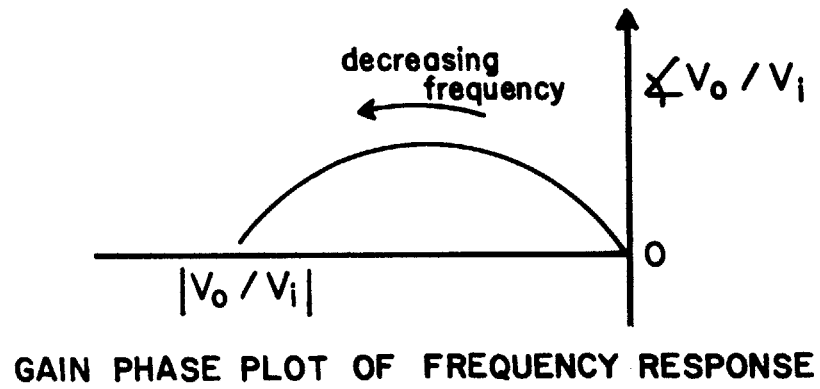


Figure 5.3.c Gain-Phase Response of Lead Network

unpassivated sensor, positive phase shift appeared. When more polyimide was added so it dripped onto the header, the positive phase increased, and the signal attenuation became worse. These results, Figure 5.4, demonstrate not only that the positive phase shift at the beginning of cure was correctly identified by Sheppard, but also that it is highly dependent on the amount of ground contact through the medium of the resin.

5.5 Positive Phase Shift at Low Gain

Measurements of the gain of an uncoated sensor reveals an anomalous positive phase shift which is unaccounted by either the lumped element model of Figure 2.3 or the lead network of Figure 5.3.a. In this case, because there is no conductive medium between the driven and floating electrodes, all coupling is capacitive, and the voltage of the floating gate should be in phase with the input signal. The observed positive phase shift at low gain has the following well defined and reproducible characteristics:

- 1) The amount of positive phase is directly proportional to the signal frequency. This neglects a residual low frequency positive phase which will be discussed later.

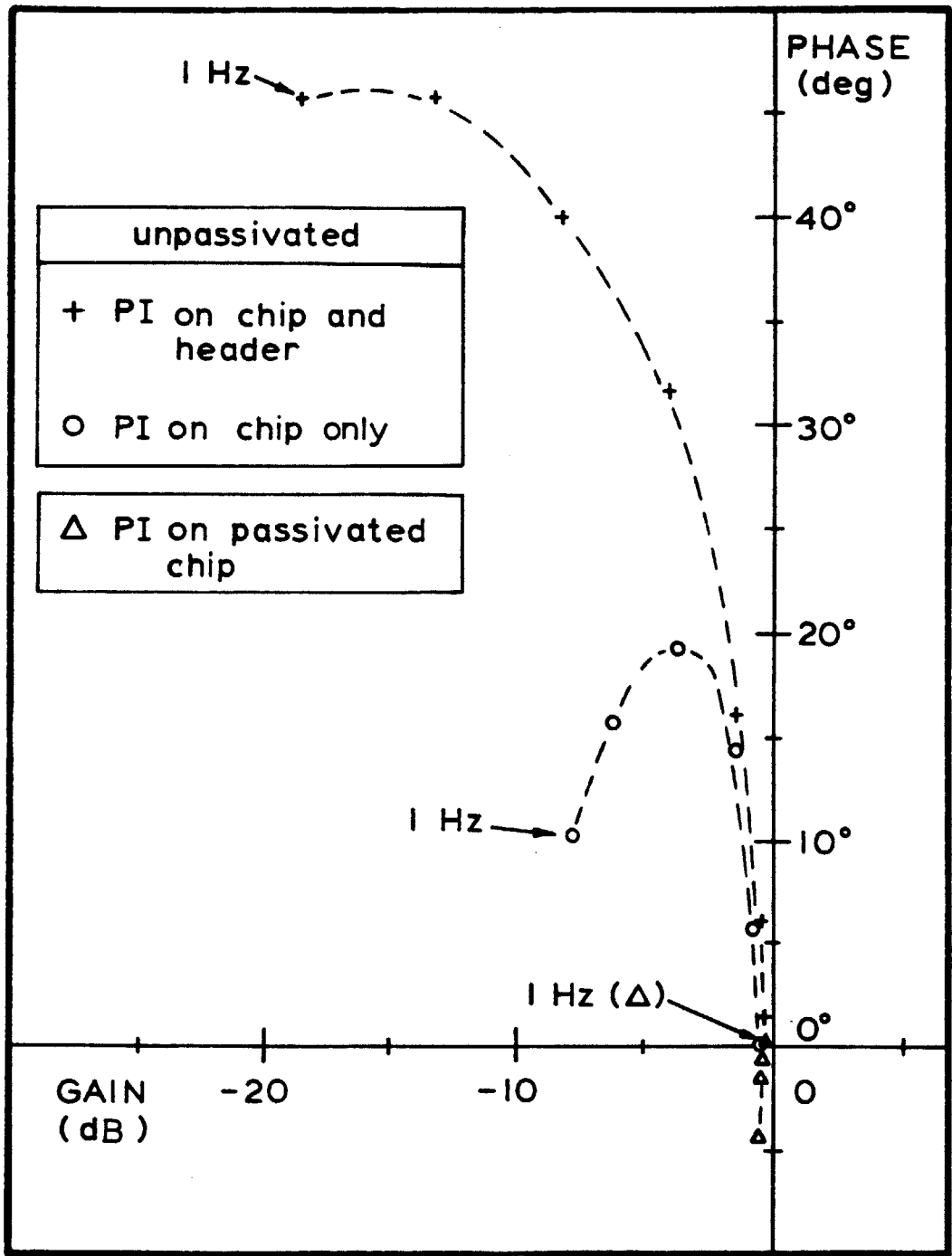


Figure 5.4 Gain-Phase Response of Passivated and Unpassivated Sensors Coated with Uncured Polyimide

- 2) Large positive phase shifts are associated with increases in gain.
- 3) At a given frequency, devices with thicker total dielectric beneath the lock and key show lesser positive phase.
- 4) Under conditions of greater gain, such as when the sensor is coated with a lossless dielectric, the positive phase still exists, but is smaller than for the uncoated device.
- 5) The resistance between two substrate pads on adjacent, connected die is approximately 3 kilohms.

It is possible that spurious signals are coupled into the transistor by the portion of the driven gate guard ring that overlaps the source-drain regions. This was tested by severing the guard ring from the rest of the driven gate with a laser trimmer. When the isolated guard ring is grounded by a bond wire to the substrate pad, no driven gate signal can couple into the transistor source or drain. When tested, however, the positive phase remained.

Consideration of the fact that the substrate sheet resistance, as calculated by SUPREM, is on the order of kilohms, and that the transistors have very large body effects, another explanation, attributed to Senturia [46], is suggested.

Operation of this sensor with its reference FET relies on the matching of transistor characteristics and the cancellation of common mode effects. Since a certain capacitive coupling exists between the gate of a transistor and the substrate, due to bond pads and other metal structures, if the gates of the two transistors have different geometries because of attached electrodes, bond pads and interconnects, the coupling to the substrate is different and can be the origin of differential signals. The large area of the lock and key therefore provides the opportunity to induce charge capacitively into the silicon beneath it, charge which is not matched by the reference FET.

If the high substrate sheet resistance is modeled as a parasitic resistance on the order of kilohms, then the capacitive coupling from the lock and key produces a current which flows to ground through this resistance and modulates the substrate potential of the CFT. The large transistor body effect amplifies this signal in the form of a back-gate transconductance, and adds a current component which is $+90^\circ$ out of phase with the current controlled by the gate transconductance. Figure 5.5.a illustrates the elements of this model. The differential signal which causes positive phase comes from the total capacitance to ground of the driven gate with its bond pad, electrodes and guard rings. All these have a potential with an

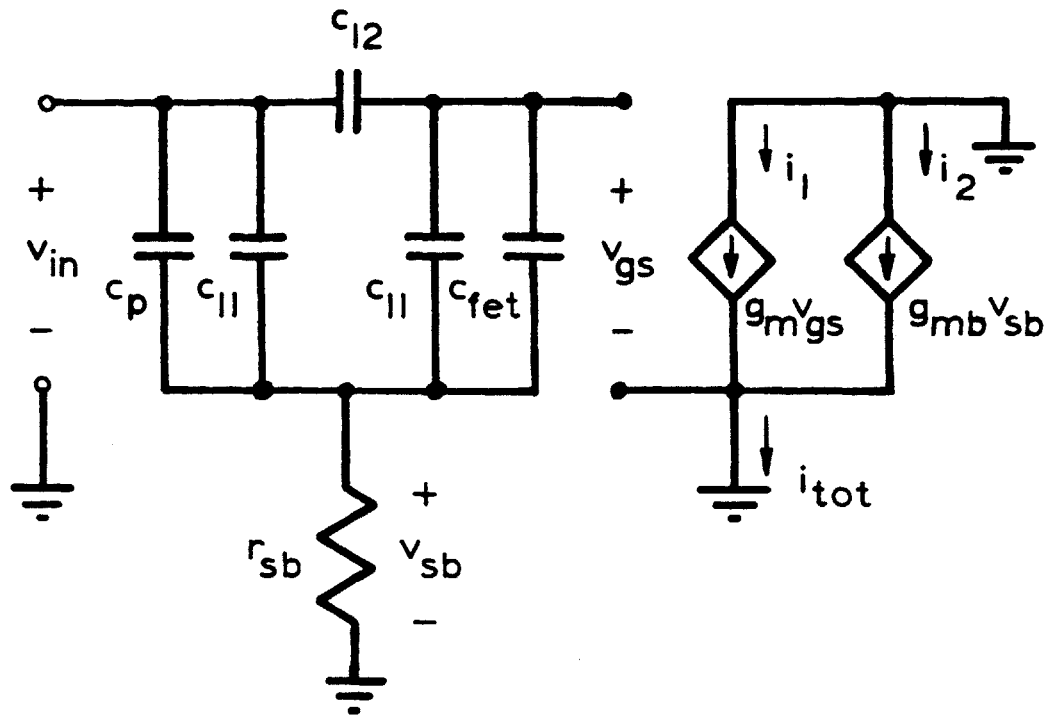


Figure 5.5.a Elements Modeling Positive Phase Shift Due to Body Effect

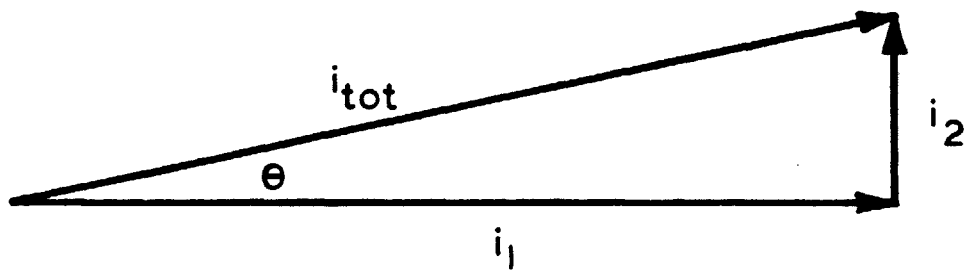


Figure 5.5.b Vector Addition of Currents to Produce Positive Phase Components

amplitude of 1 volt, while the bond pad and guard ring of the reference FET carry only the much smaller floating gate voltage.

Analysis of this model proceeds with the simplifying assumption that

$$v_{gs} = \frac{c_{12}}{c_{11} + c_{12} + c_{fet}} \quad [5.4.1]$$

This equality is valid because $r_{sb} \ll 1/\omega (c_{11} + c_p)$ at the frequencies of interest, where c_p is the extra capacitance to ground associated with the pad and all other metal portions of the driven gate, other than the electrodes themselves. The voltage division at the substrate node is so small that v_{gs} is essentially unaffected. The gate transconductance current therefore is

$$i_1 = g_m \left(\frac{c_{12}}{c_{11} + c_{12} + c_{fet}} \right) \quad [5.4.2]$$

Since $c_{12} \ll c_{11}$, the current component through c_{12} may be neglected in calculating v_{sb} , and

$$v_{sb} = \frac{j\omega r_{sb} (c_{11} + c_p)}{1 + j\omega r_{sb} (c_{11} + c_p)} \quad [5.4.3]$$

Therefore

$$i_2 = g_{mb} \left(\frac{j\omega r_{sb} (c_{11} + c_p)}{1 + j\omega r_{sb} (c_{11} + c_p)} \right) \quad [5.4.4]$$

At the frequencies of interest, less than or equal to 1000 Hz,

$$\omega r_{sb} (c_{11} + c_p) \ll 1 \quad [5.4.5]$$

and

$$i_2 \approx g_{mb} (j\omega r_{sb} (c_{11} + c_p)) \quad [5.4.6]$$

The two current components i_1 and i_2 may be treated as vectors, and their sum is

$$i_{tot} = g_m \left[\left(\frac{c_{12}}{c_{11} + c_{12} + c_{fet}} \right) + \lambda j\omega r_{sb} (c_{11} + c_p) \right] \quad [5.4.7]$$

Where $g_{mb} = \lambda g_m$, and λ is a constant relating the body effect transconductance g_{mb} to the gate transconductance g_m . The magnitude of the total current is then:

$$\left| i_{tot} \right| = g_m \left[\left(\frac{c_{12}}{c_{11} + c_{12} + c_{fet}} \right)^2 + \left(\lambda \omega r_{sb} (c_{11} + c_p) \right)^2 \right]^{1/2} \quad [5.4.8]$$

and the phase is

$$\angle i_{tot} = \tan^{-1} \left[\frac{\lambda \omega r_{sb} (c_{11} + c_p)}{c_{12} / (c_{11} + c_{12} + c_p)} \right] \quad [5.4.9]$$

The phase is positive and has behavior which agrees with observations 1-4. It is now possible to calculate the resistance r_{sb} required by this model to produce the experimental phase shifts. When this is done, with the

calculated quantities of Table V, r_{sb} has values from 4.6 kilohms to 7.5 kilohms, of the same order as the resistance reported in observation 5.

This parasitic resistance should be proportional to the substrate sheet resistance, and indeed r_{sb} is smaller for the 0.45 micron field oxide devices than for the 0.75 micron devices. The ratio of parasitic resistances for these two types of sensors is 0.75. SUPREM simulations for the devices gives sheet resistances whose ratio is 0.80. The implication is strong that this parasitic substrate resistance, in conjunction with the transistor body effect, causes the positive phase seen at low gain.

Since this phase shift has well behaved characteristics defined by the sensor geometry and transistor electrical parameters, it is possible to calculate the i_2 current vector introduced into the data at any given frequency. This component can then be removed from the data by vector subtraction. Software has been written to perform this task, and all data presented in this thesis has been processed to eliminate the parasitic phase.

5.6 Surface Conductivity on the Sensor

Even when phase shift due to the body effect is taken into account, a residual positive phase still affects low frequency measurements. According to the model of Figure

TABLE V
POSITIVE PHASE PARAMETERS

<u>Type of Sensor</u>	A	B	C	D
W/H	27.8	14.7	7.5	5.8
Field Oxide	0.45 um	0.85 um	0.75 um	0.75 um
$C_{11} \times M$ (C_{11}^*)	5.37 pF	2.94 pF	1.61 pF	1.29 pF
Area of 1st-Level Metal, Excluding Fingers (A_{P1})	9.71×10^{-4} cm ²	9.71×10^{-4} cm ²	1.36×10^{-3} cm ²	1.36×10^{-3} cm ²
Area of 2nd-Level Metal, Excluding Fingers and Overlap over 1st-Level (A_{P2})	-----	-----	2.77×10^{-4} cm ²	2.77×10^{-4} cm ²
Capacitance of 1st-Level Metal (C_{P1})	7.46 pF	3.95 pF	6.27 pF	6.27 pF
Capacitance of 2nd-Level Metal (C_{P2})	-----	-----	0.58 pF	0.45 pF
($C_{11}^* + C_{P1} + C_{P2}$)	12.8 pF	6.9 pF	8.5 pF	8.0 pF
λ	1.3	1.3	1.3	1.3
θ (1000 Hz)	15°	7°	5°	4°
$\lambda 2\pi r_{sb} (c_{11} + c_p)^1$	4.8×10^{-7} sec	4.2×10^{-7} sec	4.2×10^{-7} sec	3.9×10^{-7} sec
r_{sb}	4.6 K Ω	7.5 K Ω	6.1 K Ω	6.1 K Ω

$$\frac{R_{SH} \text{ (0.45 um Field Oxide)}}{R_{SH} \text{ (0.75 um Field Oxide)}} \text{ from SUPREM} = \frac{1.6 \text{ K}\Omega}{2.9 \text{ K}\Omega} = 0.80$$

$$\frac{r_{sb} \text{ (0.45 um Field Oxide)}}{r_{sb} \text{ (0.75 um Field Oxide)}} \text{ from DATA} = \frac{4.6 \text{ K}\Omega}{6.1 \text{ K}\Omega} = 0.75$$

$$1. \quad (c_{11} + c_p) = (C_{11}^* + C_{P1} + C_{P2})$$

5.5.a, if the phase shift at 1000 Hz is 7 degrees, it decreases linearly with frequency, and at 1 Hz should be 0.007 degrees. In the range from 1 to 100 Hz, however, the positive phase is still approximately 1 to 3 degrees. Under conditions of higher humidity, this phase increases to as much as 14 degrees at 1 to 3 Hz, and decreases to about 1 degree at higher frequencies.

These observations can be explained with the surface conduction model of Figure 5.6.a. The 1 volt signals at the driven gate generates electric fields on the order of 10,000 volts/cm, which can be coupled strongly to any surface conductance on the chip. This conductance can originate from contamination, thin films remaining after device fabrication and wet etching, or simply the inherent surface conductivity of silicon dioxide or polyimide. Charge flow across the surface can then be coupled capacitively into the CFT source as a current which has positive phase relative to the source-drain current. The guard ring around the source pad enters the model as a point which allows a resistive shunt to ground. Although the system is distributed, a lumped element model should provide understanding of the mechanism involved.

The additional current described by the model is

$$I_3 = \frac{sC_3 (R_1 \parallel R_2)}{sC_3 (R_1 \parallel R_2 + R_3) + 1} V_{DG} \quad [5.6.1]$$

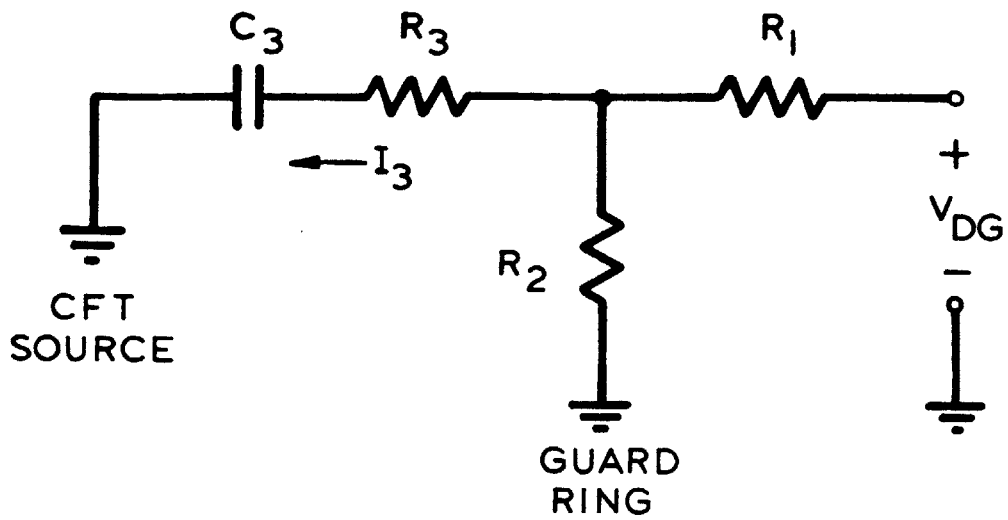


Figure 5.6.a Elements Modeling Residual Low Frequency Positive Phase

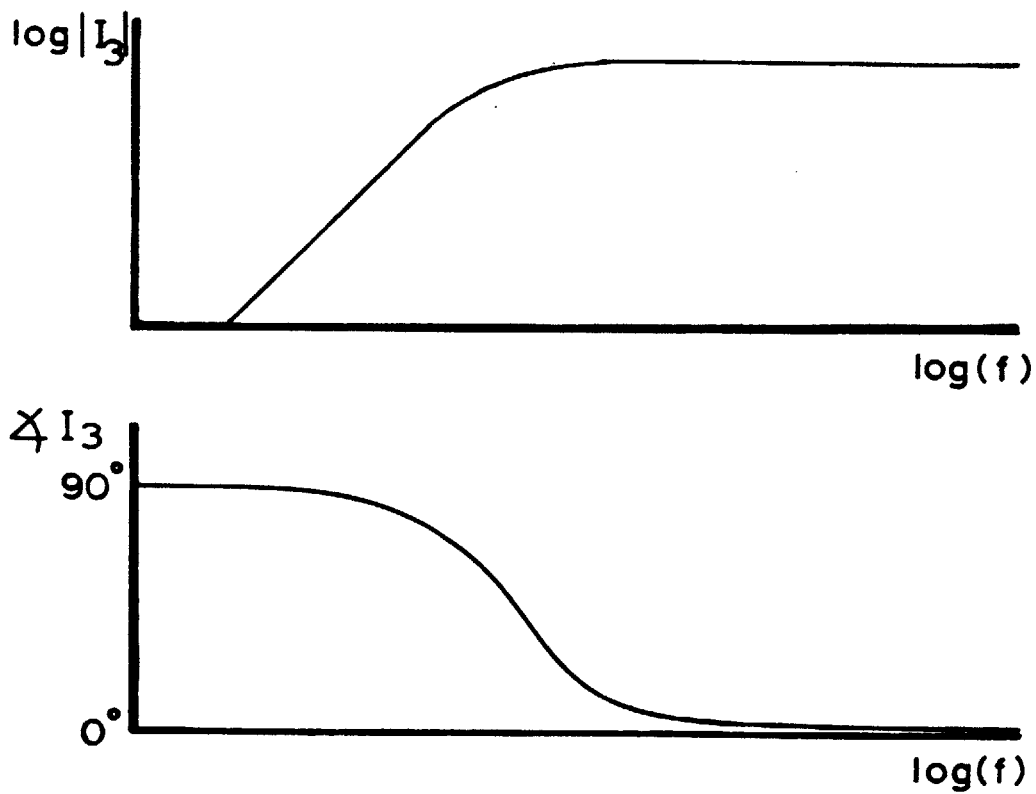


Figure 5.6.b Frequency Response of Model of Figure 5.6.a

with magnitude

$$\left| I_3 \right| = \frac{\tau_1 \omega}{(1 + (\tau_2 \omega)^2)^{1/2}} \quad [5.6.2]$$

and phase

$$\angle I_3 = 90^\circ - \tan^{-1} \omega \tau_2 \quad [5.6.3]$$

Where $\tau_1 = (R_1 \parallel R_2) C_3$

$$\tau_2 = (R_1 \parallel R_2 + R_3) C_3$$

The actual positive phase contributed by this spurious current can be calculated by vector addition to the source-drain current. Assuming that with a fixed surface geometry this stray component is constant at a given frequency, then it produces smaller phase shifts in devices with larger gains, for the zero-phase current vector is relatively larger than for a device with lesser gain, while the current I_3 remains the same. This relation is observed consistently over the range of W/H represented by the sensors which have been fabricated. This model also explains the decrease in positive phase with increasing frequency. Also, because surface conductivities are often moisture sensitive and increase with humidity, equations [5.6.2] and [5.6.3] indicate that the resulting greater surface conductances will in fact create larger phase shifts. Figure 5.7 plots an experimental example of large low frequency positive phase at high humidity, and compares

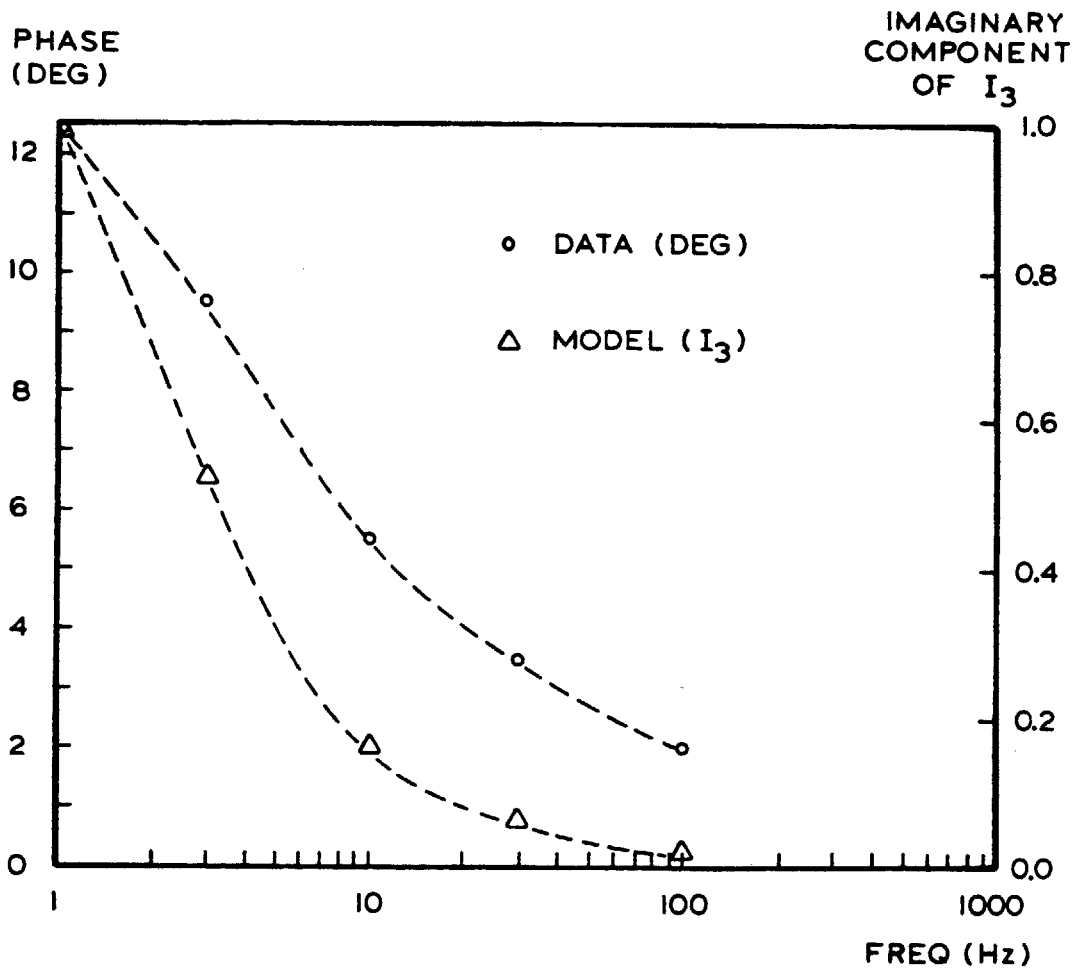


Figure 5.7 Imaginary Component of Current from Residual Positive Phase Model, Compared with Example of High Positive Phase at High Humidity

it to the imaginary component of the stray current given by the model. Time constants for the model have been chosen to show behavior similar to the data.

An additional contribution to this residual phase shift comes from the gain/phase meter, for at signal levels characteristic of uncoated devices, -55 dB to -45 dB, it has an accuracy of ± 2 degrees [47]. When measuring the phase of a resistive voltage divider whose gain was in this range, the gain/phase meter registered a phase of +1.5 degrees at 1 Hz.

Under high humidity, gain-phase measurements of uncoated sensors passivated with polyimide show moisture sensitive behavior. Typically, as frequency decreases, the data describe a bowed trajectory with negative phase and increased gain, as shown in Figure 5.8. When heated to about 100 °C, the passivated devices return to their ideal state where the gain is fixed at the theoretically calculated value. Upon cooling the sensor to room temperature, the data slowly return to a trajectory. Devices which have no polyimide do not have a trajectory, only the frequency independent gain expected of a bare sensor.

It is possible that the polyimide etch step leaves a residual contaminant between the fingers of the lock and key. This film could absorb water from a humid environment, with an accompanying decrease in sheet resistance.

Sensors demonstrating this moisture sensitivity were etched in a low pressure, 50 mTorr, oxygen plasma for 15 seconds. After subsequent annealing at 400 °C, to remove damage in the transistors caused by the plasma and radiation, the moisture sensitivity still remained. In addition, the trajectory followed by the sensor was the same before and after plasma etching.

Examination of the passivation layer shows that the edge of the opening around the lock and key crosses both the driven and floating gate metal at the transistor guard ring (See Figure 4.2.a.). A stray surface conduction path exists along this edge, and under high humidity it could shunt sufficient current to cause the sensor response to follow a trajectory. In this case, the moisture sensitivity of the sensor would be unaffected by plasma etching, for a residual film would not be the cause, and the driven and floating gates would always remain bridged by the rim of the passivation cut.

The sensors fabricated with double-level metal and a layer of polyimide beneath the lock and key also show moisture sensitivity. Figure 5.8 compares the humidity dependent trajectory of a 0.85 micron device with a polyimide overglass layer, to that of a 1.66 micron device with polyimide beneath the lock and key. The fundamental differences in these two trajectories imply that different

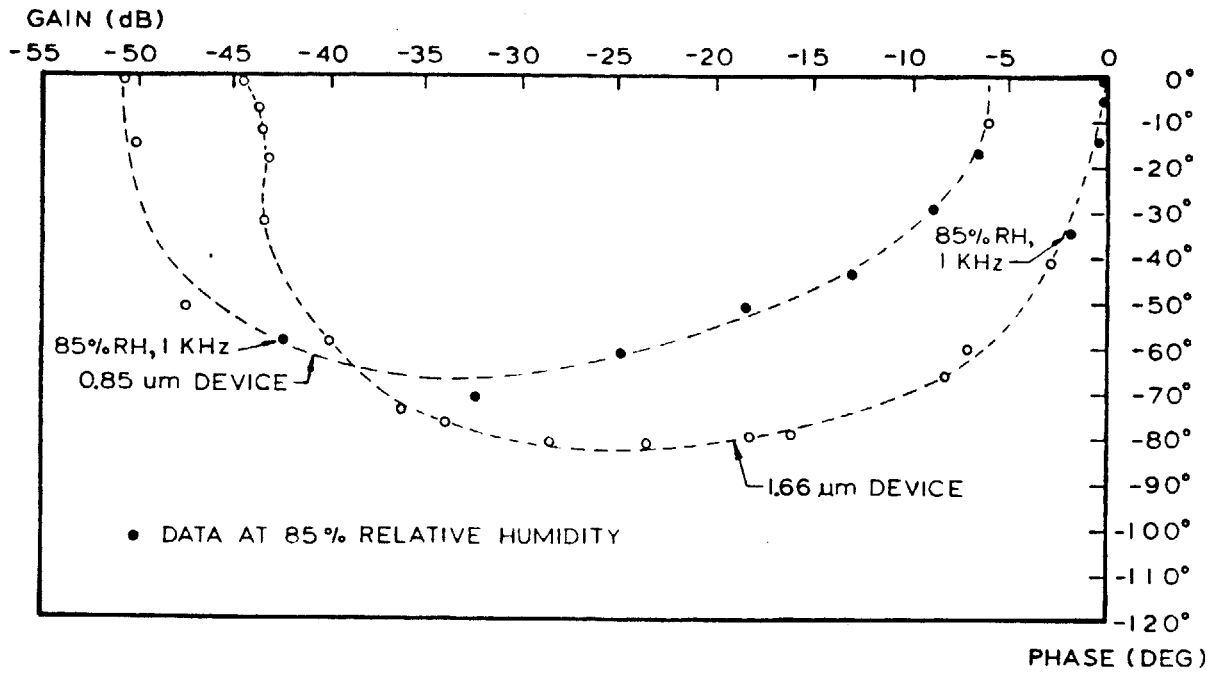


Figure 5.8 Humidity Sensitive Trajectory of a 0.85 Micron Sensor with Polyimide Passivation, Compared to Trajectory of a 1.66 Micron Sensor

conduction paths are responsible. Quantitatively, the 0.85 micron device is much less sensitive than the 1.66 micron device. Measurements were taken in the same environment with 85% relative humidity and, as shown in Figure 5.8, the 0.85 micron sensor had a gain of only -33 dB at 1000 Hz while the 1.66 micron device had a gain of -2 dB. Even when the different dielectric thicknesses beneath the lock and key are taken into account, the 0.85 micron device must have a significantly smaller conductance between the driven and floating gate than does the 1.66 micron device. If the single-level metal design has a residual polyimide film between its lock and key fingers, it should have the same area as the polyimide of the double-level design, and probably a similar surface conductance.

One significant qualitative difference between the trajectories of the two designs is the low frequency limit in gain. The 1.66 micron sensor has moisture sensitive behavior characteristic of the thin conductive films studied by Garverick [6] and Davidson [48],[49]; at high humidities or low frequencies, the data go through the origin of gain-phase space. Under these conditions the electrodes are shorted together by the high loss factor of the conductive film. The single-level metal design, however, has a trajectory that intercepts the gain axis

at -6 dB. This offset cannot be caused by a blocking layer capacitance between the electrodes and a possible thin film. Assuming such a blocking layer has a permittivity of 4.0 and the same area as the lock and key's fingers, the necessary thickness is about 0.3 microns, which is too great for either an aluminum oxide barrier or residual polyimide contamination.

When the floating gate of the 0.85 micron device was charged, and the driven gate was maintained at the floating gate potential, to act as guard ring, the floating gate charge still leaked away to ground. In another experiment, the steady state floating gate voltage was measured after positive voltage steps were applied to the driven gate. Ideally, current flow across any conductive path between the two would equalize the electrode voltages; yet, the floating gate did not charge-up to the the driven gate voltage. Instead, it reached a constant value which was roughly 70 % to 80 % less than expected, and suggested the presence of voltage division.

In a final experiment, negative voltage steps were applied to the driven gate. The floating gate voltage in this case decreased, but attained steady state values which were greater than the DC potential on the driven gate, suggesting a charge storage effect which interferes with complete conduction between the two electrodes.

It is important, therefore, to avoid stray surface conduction both between the driven and the floating gates, and between the floating gate to ground, for these paths prevent the floating gate from maintaining a true floating potential. With the exception of the charge storage effect, the experimental observations can be explained with the model of Figure 5.9. For the uncoated lock and key, the inter-electrode capacitance is C_{12} . The stray inter-electrode conductance, $G_A = 1/R_A$, is due to polyimide along the rim of the passivation cut connecting the driven and floating gate. The capacitance to ground, $C_{11} + C_L$, is the electrode capacitance to ground, plus the transistor gate capacitance. The stray conductance to ground, $G_B = 1/R_B$, arises from the surface conductive path that runs from the edge of the passivation cut, across the polyimide surface, to the substrate bond pad. Although the model has lumped elements and cannot be expected to describe the distributed nature of the problem, it has overall behavior which is similar to the observed moisture sensitive trajectory.

At low frequency the admittances are primarily conductive, and the stray conductivity across the polyimide surface shunts some of the current which would otherwise charge the floating gate. The resulting voltage divider explains the offset on the gain axis at low frequency and

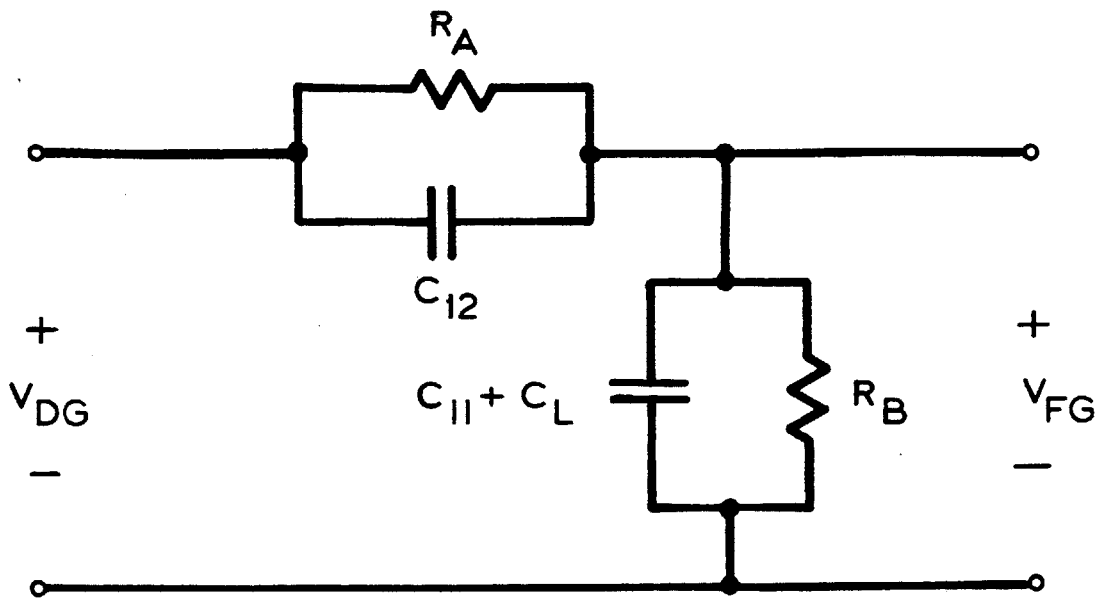


Figure 5.9 Lumped Element Model of Sensor with Humidity Dependent Components R_A and R_B to Represent Polyimide Surface Resistance

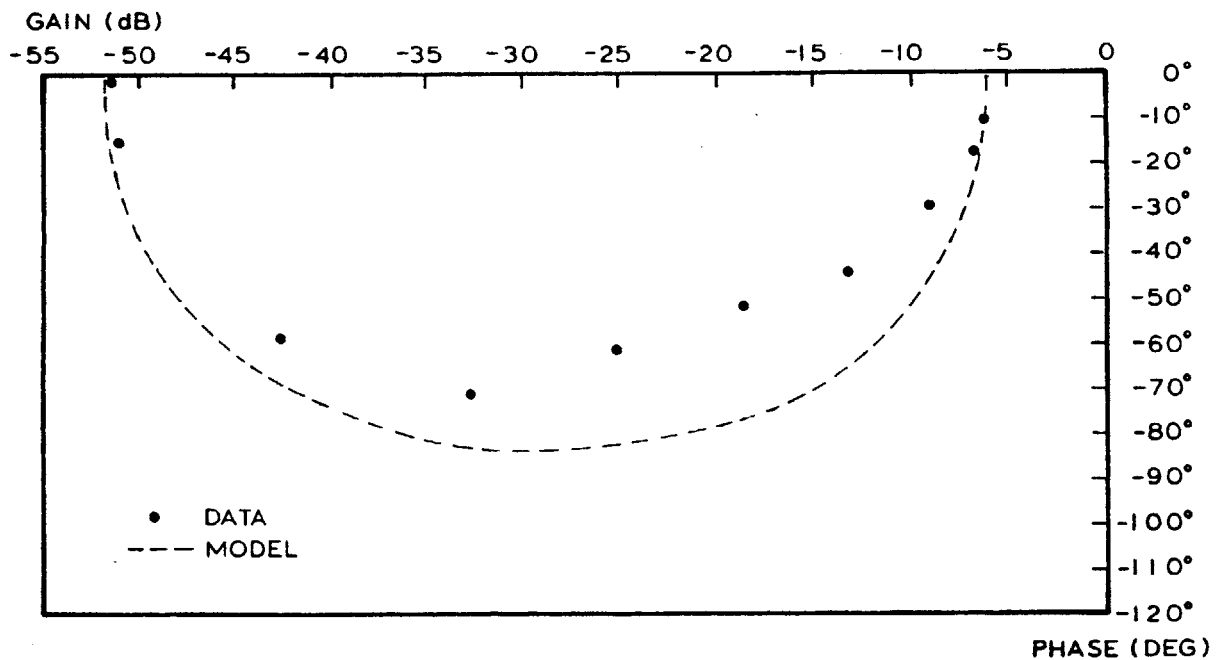


Figure 5.10 Trajectory of Model of Figure 5.9, with Data from a 0.85 Micron Sensor

high loss. At high frequency the voltage divider is capacitive, and the sensor has the gain expected for an uncoated lock and key. At intermediate frequencies the output voltage has negative phase, and with increasing loss varies smoothly between the two limiting cases. The transfer function for this model is

$$\frac{V_{FG}}{V_{DG}} = \frac{\beta (1 + j\alpha C_{12})}{1 + j\alpha\beta (C_{11} + C_L + C_{12})} \quad [5.6.4]$$

with magnitude

$$\left| \frac{V_{FG}}{V_{DG}} \right| = \frac{\beta (1 + (\alpha C_{12})^2)^{1/2}}{(1 + (\alpha\beta (C_{11} + C_L + C_{12}))^2)^{1/2}} \quad [5.6.5]$$

and phase

$$\angle \frac{V_{FG}}{V_{DG}} = \tan^{-1} \alpha C_{12} - \tan^{-1} (\alpha\beta (C_{11} + C_L + C_{12})) \quad [5.6.6]$$

where

$$\alpha = \omega R_{12}$$

$$\beta = R_{11} / (R_{11} + R_{12})$$

By properly choosing β to produce the observed offset near the origin, and then varying α , the transfer function follows the path shown in Figure 5.10. The actual trajectory of the 0.85 micron device is also plotted for comparison. It is uncertain whether this surface conduction parasitic will affect the device's ability to measure

dielectric properties, for, when used, the sensor is immersed completely in the sample, and may be effectively passivated from ambient humidity.

5.7 On-chip Temperature Sensing

If a particular curing process is exothermic, the heat generated may dissipate slowly through the bulk of large resinous volumes. Hot spots can form which will in turn affect the local rate of reaction. In studying resin cures, knowledge of the local temperature history is important, and a diode for use as a temperature sensor has been incorporated into the chip design. It is fabricated with the source-drain implant step and has an area of 4 square mils.

To first order, the diode junction voltage at a fixed current varies with a slope of $-2.3 \text{ mV}/^{\circ}\text{C}$. This quantity is determined by the thermodynamics of the diode equation, and is unaffected by variables such as junction area or doping distribution.

The circuit of Figure 5.11 is used in conjunction with this diode to measure temperature. A feedback loop consisting of an n-channel MOSFET, a resistor and an operational amplifier maintains constant current through the diode. Readings of the junction voltage are buffered through a unity gain follower and amplified with a gain-block.

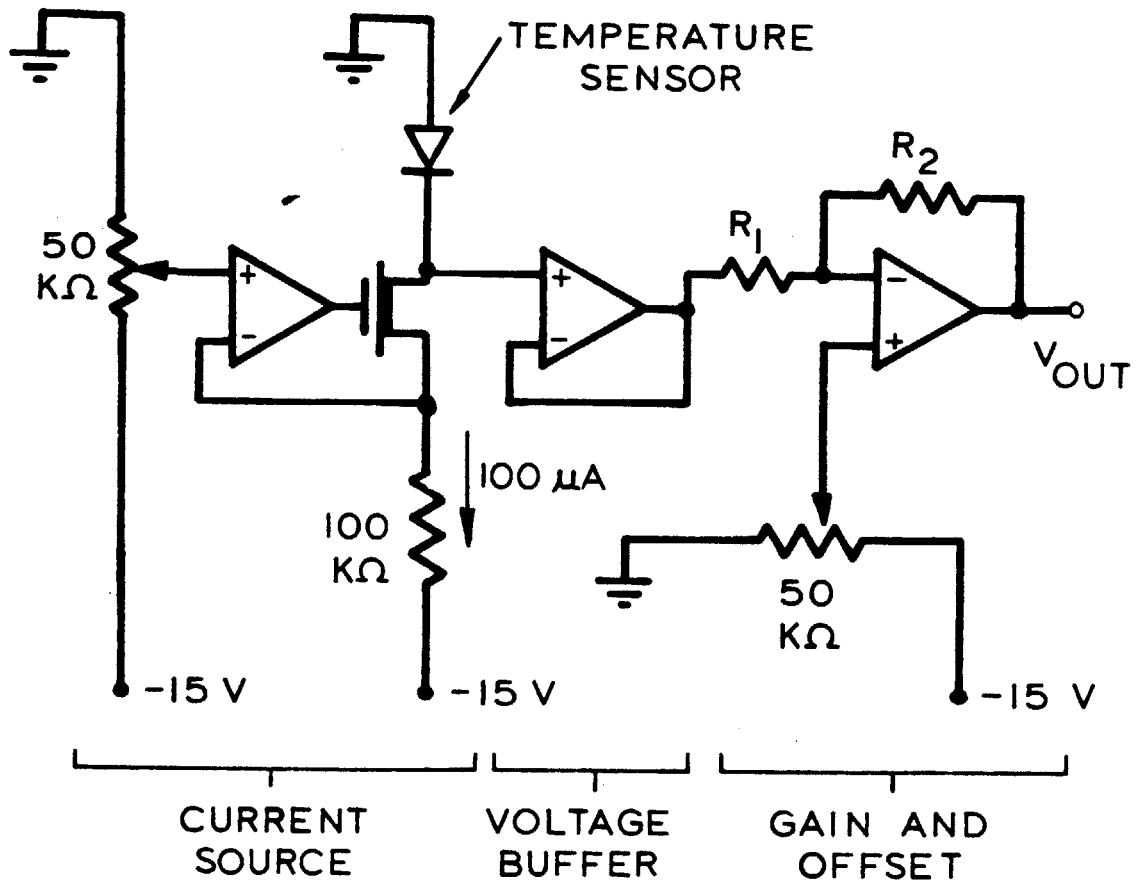


Figure 5.11 Temperature Sensor Circuit

Voltage offset in the gain stage adjusts the output level before processing by the data acquisition system.

During temperature sensing, diode current is set at 100 microamps for low power dissipation. Figure 5.12.a is a typical plot of junction voltage versus temperature. The slope is $-2.3 \text{ mV}/^{\circ}\text{C}$, and is very consistent from device to device. When the junction voltage is properly scaled and offset, a direct reading of temperature is possible. Figure 5.12.b is a plot of temperature, as measured by the diode, versus a standard Celsius mercury thermometer. Over the range from 20°C to 150°C the two agree very well, with only a maximum deviation of 2 degrees. This preliminary test indicates that the temperature sensor has immediate utility within the limitations of this uncertainty. Further, when the diode calibration includes an assessment of second order effects, the temperature sensor can be an accurate monitor of in-situ thermal events.

5.8 Permittivity Measurements

Experiments were performed to test the agreement of permittivity measurements made by the four types of sensors. Lossless dielectric materials were applied to the devices, and the gains were measured. The dielectrics used were Epon 828, DER 332, DGEBA/MPDA, Polyimide 2555 and RTV

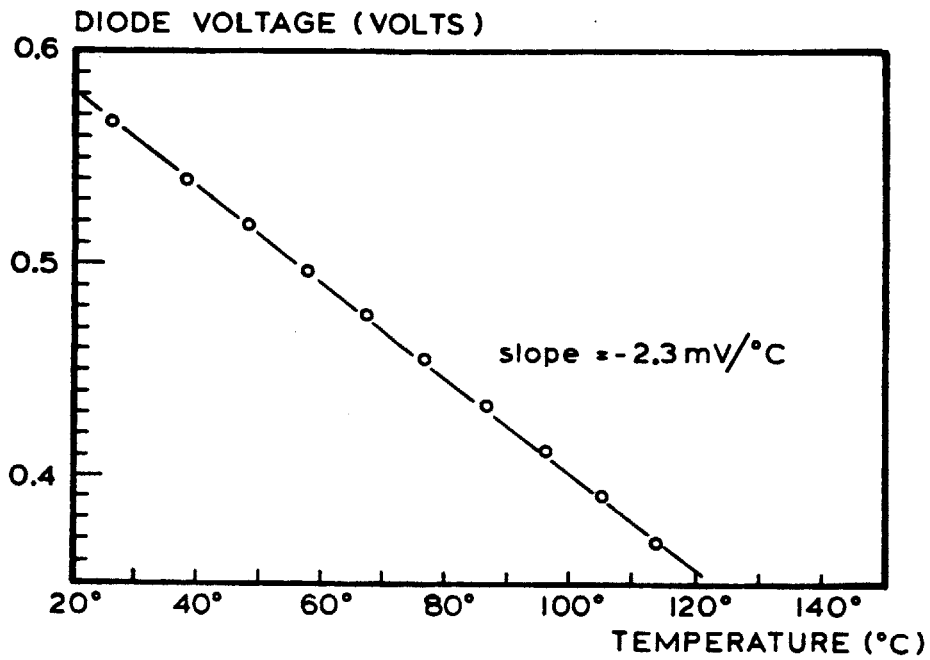


Figure 5.12.a Diode Voltage versus Temperature

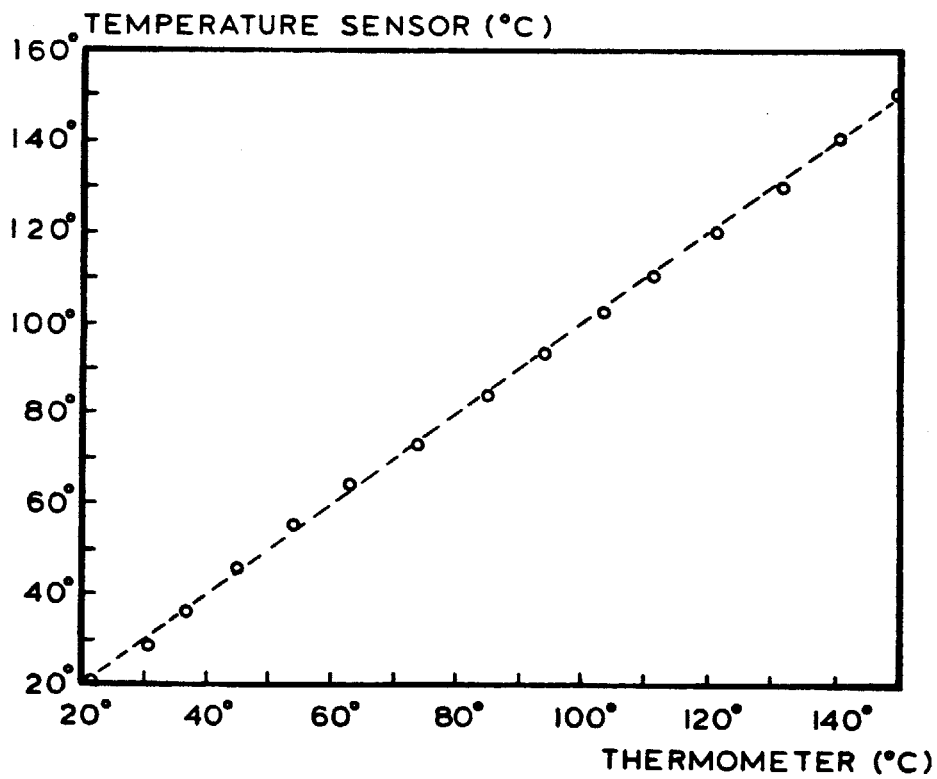


Figure 5.12.b Temperature Sensor Reading versus Mercury Thermometer

clear silicone rubber. Both the DGEBA/MPDA and the polyimide were applied in the liquid uncured state, and then fully cured before measurement. The Epon 828 and DER 332 actually have some bulk conductivity, but the data obtained at 1000 Hz were on or close to the gain axis, and therefore corresponded to only a small perturbation from zero loss factor.

Since the dielectrics were effectively lossless at the highest frequencies used, 1000 Hz, the data show no phase except the parasitic effects previously discussed. Figure 5.13 compares the permittivities extracted from the raw data for each of the substances tested. Agreement between all devices is good, with some scatter in results of approximately 10%, at worst. Table VI compares the extracted permittivities, averaged from the four devices, with values expected for the various dielectrics. The correlation for each material is good.

The permittivity of RTV was not listed in any available reference, but the CRC Handbook of Chemistry and Physics reports the permittivity of generic silicone rubber to be in the range of 3.12 to 3.3, which may not apply to the specific type of RTV used. Nevertheless, the RTV data is close to what would be expected. The large scatter in the results for RTV may be due to its extremely viscous nature; the necessary complete contact of the silicone

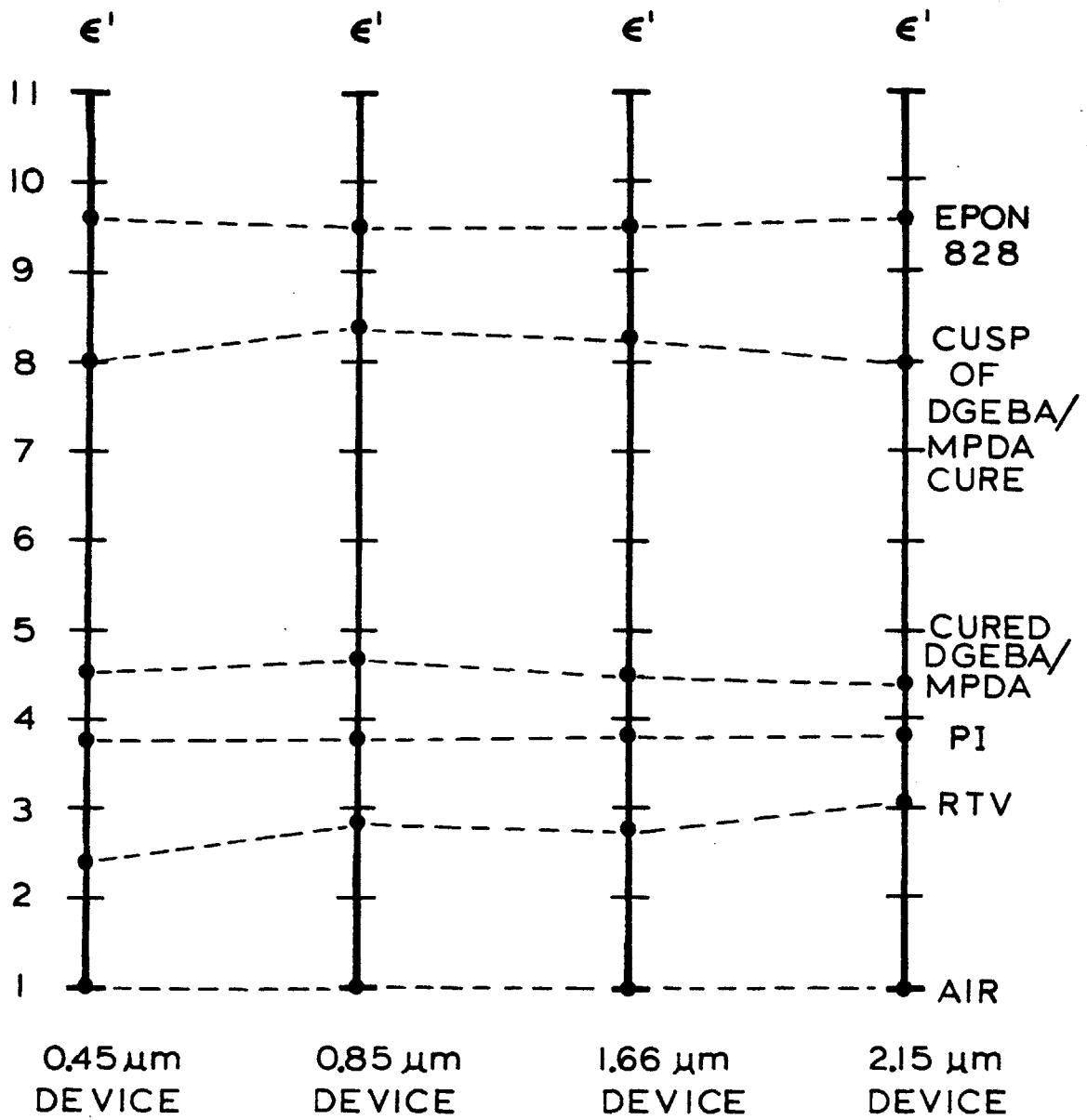


Figure 5.13 Permittivities of Various Dielectrics as Measured with Different Sensor Geometries

TABLE VI
AVERAGE EXTRACTED PERMITTIVITIES

<u>Dielectric</u>	<u>Average ϵ_1' from Sensor</u>	<u>Expected ϵ_1'</u>
Air	1.0	1.0
Clear RTV	2.8 ± 0.3	3.12 - 3.3 [i]
Polyimide 2555	3.8 ± 0.04	3.5 [ii]
Cured DGEBA/MPDA	4.6 ± 0.14	4.6 [iii]
Epon 828	9.6 ± 0.1	10 ± 0.4
DER 332	9.5 ± 0.1	10 ± 0.4

Sources

- [i] CRC Handbook of Chemistry and Physics
- [ii] Du Pont Information Bulletin [41]
- [iii] Acitelli et al. [12]

rubber to the lock and key electrodes may not have been achieved.

5.9 Loss Factor Measurements

The Epon 828 and DER 332 both have certain bulk conductivities, and allow the determination of a good range of loss factors simply by varying the measurement frequency. DER 332 is the commercial name for the DGEBA resin cured in the experiments for this thesis. Since Epon 828 is a purified form of DGEBA which is used as a calibration dielectric, it should be less conductive than DER 332.

After each liquid was applied, the gain and phase for all four types of devices were recorded for frequencies from 1 to 1000 Hz. Loss Factors were extracted with an interpolation routine using look-up tables generated by finite difference simulation. The results are shown on Figure 5.14. Both materials were found to have the same permittivity of approximately 9.5, as expected, and all four types of devices measured the loss factors with excellent agreement.

If the dissipation in a medium is dominated by a bulk, frequency independent conductivity, then loss factor is inversely proportional to frequency. A measurement at 10 Hz should yield a loss factor ten times less than one

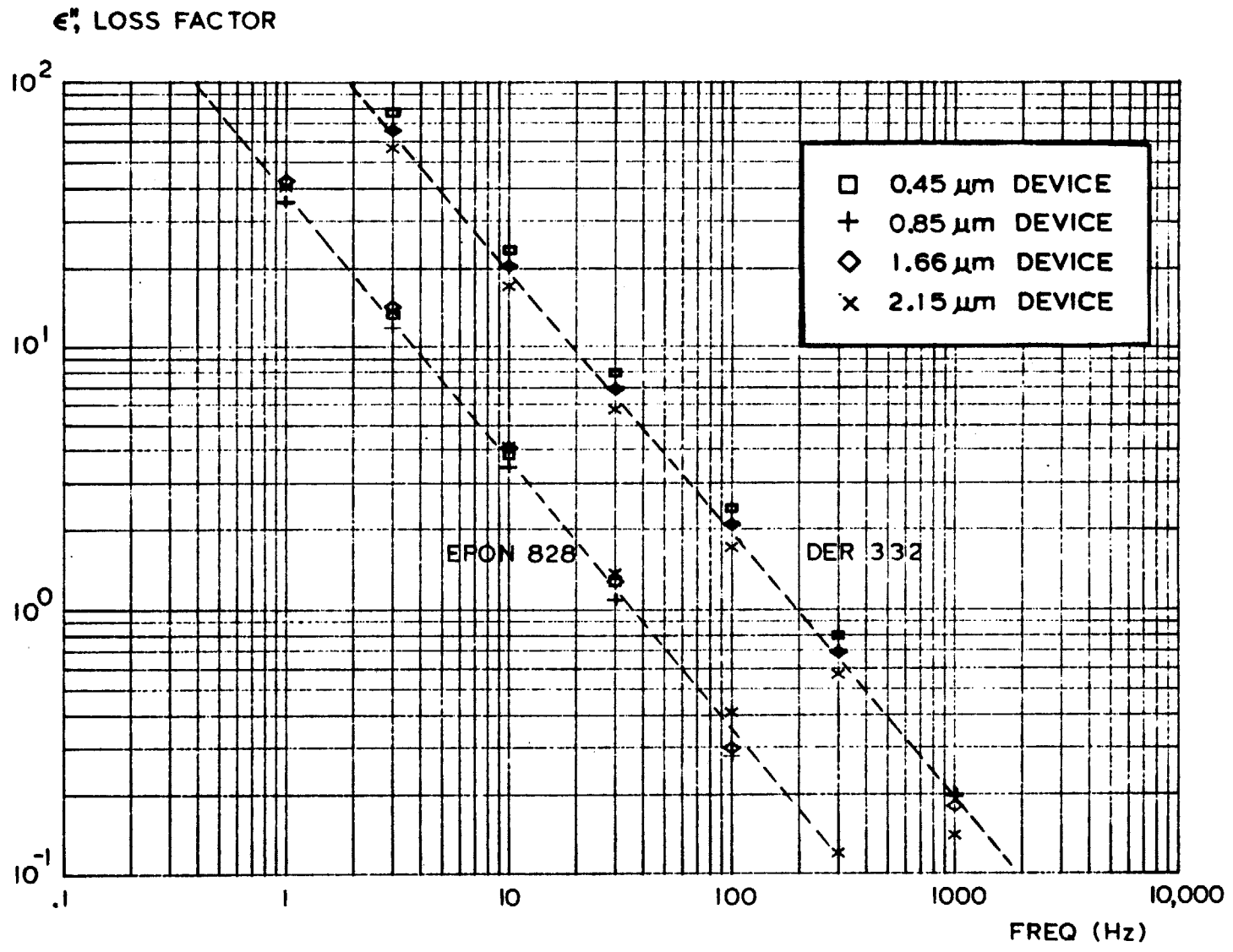


Figure 5.14 Loss Factor vs. Frequency as Measured with Different Sensor Geometries

at 1 Hz, and 10 times greater than one at 100 Hz. This proportionality is seen in the data, and the corresponding bulk conductivities are $2.15 \times 10^{-11} \Omega^{-1} \text{cm}^{-1}$ for Epon 828 and $1.16 \times 10^{-10} \Omega^{-1} \text{cm}^{-1}$ for DER 332. As previously discussed, the Epon 828 is less conductive than the DER 332.

5.10 Resin Nonlinearity

The validity of the two dimensional simulation used for sensor calibration relies on the assumption that the resin-electrode system is linear, that the transfer function from the driven to the floating gate does not depend on signal magnitude. To test for nonlinearity, uncured DGEBA/MPDA was placed on a device and cured at 60°C for 70 minutes, to allow a large portion of the cure trajectory to be traced with the frequencies from 1 to 1000 Hz. To reduce the effect of any curing that may occur between measurements, the gain and phase were recorded with input amplitudes of 0.01, 0.1 and 1.0 volts for a single frequency before proceeding to the next one. This procedure was repeated with amplitudes of 1.0, 5.0 and 10.0 volts. Table VII presents the data. Since the experiment showed no dependence on amplitude from 0.1 to 5 volts, it may be concluded that the system is linear for incremental signals in this range. The data for a 10 volt amplitude differ from those for smaller amplitudes, possibly indicating

TABLE VII

RESIN LINEARITY DATA

DGEBA/MPDA resin was partially cured at 60 °C for 70 minutes. The following data are the floating gate signals for various driven gate voltage amplitudes.

Driven Gate Amplitude	1.0 V		0.1 V		0.01 V	
	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)
Frequency						
1	-1.0	+2.3	-0.9	+2.1	-0.9	+2.7
3	-1.0	-4.7	-1.0	-4.5	-0.9	-4.0
10	-1.5	-18.5	-1.4	-18.5	-1.5	-16.1
30	-3.9	-43.6	-3.9	-43.8	-4.0	-41.0
100	-11.6	-71.9	-11.8	-71.8	-12.2	-64.7
300	-21.1	-66.2	-21.5	-65.1	-18.2	-39.2
1000	-26.9	-31.7	-27.4	-30.6	-----	-----

TABLE VII

(cont.)

Driven Gate Amplitude	1.0 V		5.0 V		10.0 V	
	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)	Gain (dB)	Phase (deg)
Frequency						
1	-0.6	-3.2	+0.3	+2.0	+1.6	-0.6
3	-1.1	-13.8	-0.3	-12.7	+1.1	-12.5
10	-3.0	-37.9	-3.0	-38.1	-0.5	-35.4
30	-8.5	-65.4	-8.4	-64.5	-8.1	-62.3
100	-18.8	-68.7	-18.4	-66.4	-18.5	-58.9
300	-24.4	-41.9	-24.8	-39.6	-23.1	-29.1
1000	-27.9	-15.0	-27.2	-14.6	-24.5	-9.3

the appearance of nonlinear effects. These deviations may also be caused by the input range limitations of the electronic circuits. Similarly, the deviations in data with the 0.01 volt driving signal can be attributed to the low-level sensitivity limitation of the gain-phase meter.

5.11 Curing of the DGEBA/MPDA System

A test of all four types of sensors was performed by monitoring the complete cure of the DGEBA/MPDA resin/amine system. This particular material was chosen because it is a well characterized commercial resin. The cure trajectory, as interpreted from earlier experiments [8], spans several orders of magnitude in both permittivity and loss factor, therefore allowing the probing of a large portion of $\epsilon' - \epsilon''$ space with a single experiment. Agreement over this range among all electrode configurations used would strongly indicate that the results of device simulation are correct, that the lock and key geometry is properly taken into account, and that a material property of the resin is being measured. Previous work by Sheppard showed that curing DGEBA/MPDA traces a trajectory whose path is independent of frequency or time. This behavior means the Cole-Cole plot of its cure is a single curve, with time removed as an experimental variable.

The resin was prepared by heating the DGEBA and MPDA in separate pans at 60 °C. They were mixed in a ratio of 6.44:1.0::DGEBA:MPDA by weight and immediately stored in a refrigerator to impede further reaction. All cure experiments occurred within three days of mixing.

Before application of the resin, each of the four types of sensors were passivated as well as possible with polyimide coating the bond pads and RTV silicone rubber covering the bond wires. Only the lock and key was exposed. A small quantity of resin was then placed on the lock and key and cured at 80 °C in a nitrogen ambient. The automated data acquisition system recorded raw gain-phase data on both paper tape and a cassette cartridge. Temperature was measured with an Analog Devices PTAT and also recorded. For comparison, the experiment was later repeated at 60 °C with unpassivated devices.

Figures 5.15.a-d show the raw data obtained from each of the four passivated devices. All the gain-phase trajectories are essentially the same in form, with a large parabolic-like curve, a cusp on or near the gain axis, and a smaller secondary curve which is traced near the end of cure. Figures 5.15.a and 5.15.b, for the 0.45 and 0.85 micron devices, respectively, both show a twinned secondary curve which does not appear in data from the other sensors. This structure is caused by the parasitic

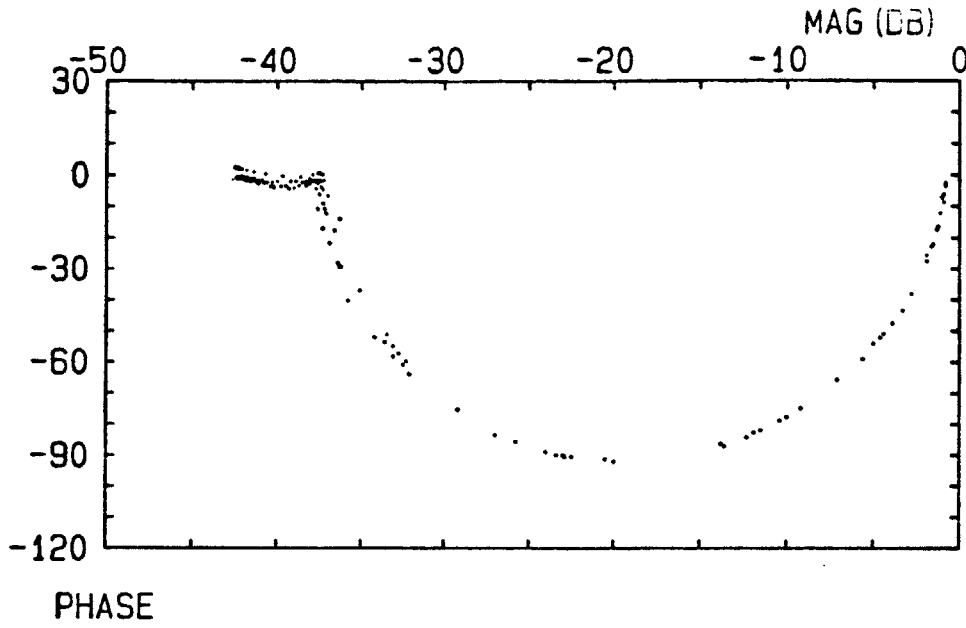


Figure 5.15.a Raw Gain-Phase Data Obtained with the 0.45 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

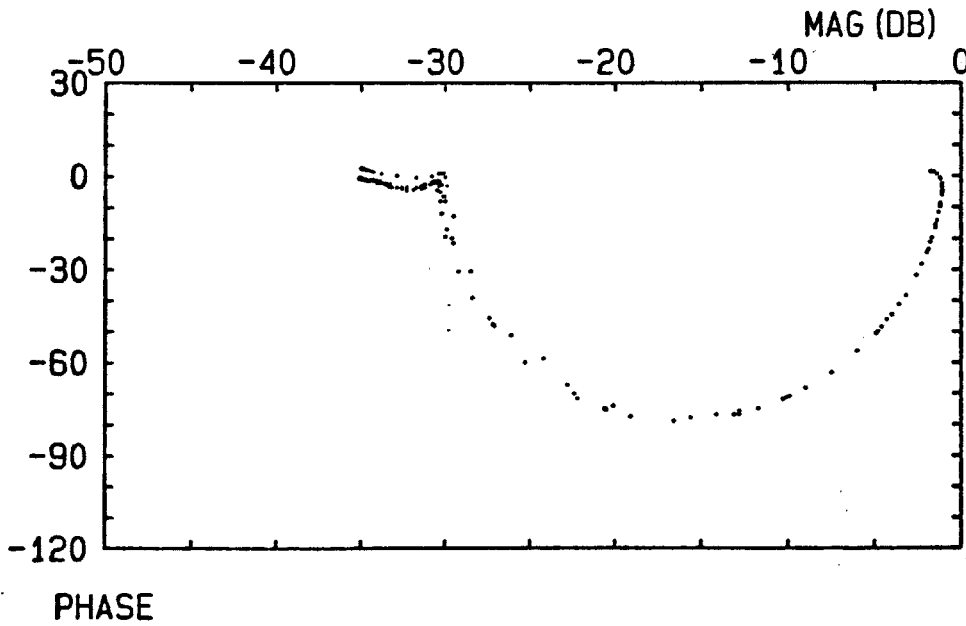


Figure 5.15.b Raw Gain-Phase Data Obtained with the 0.85 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

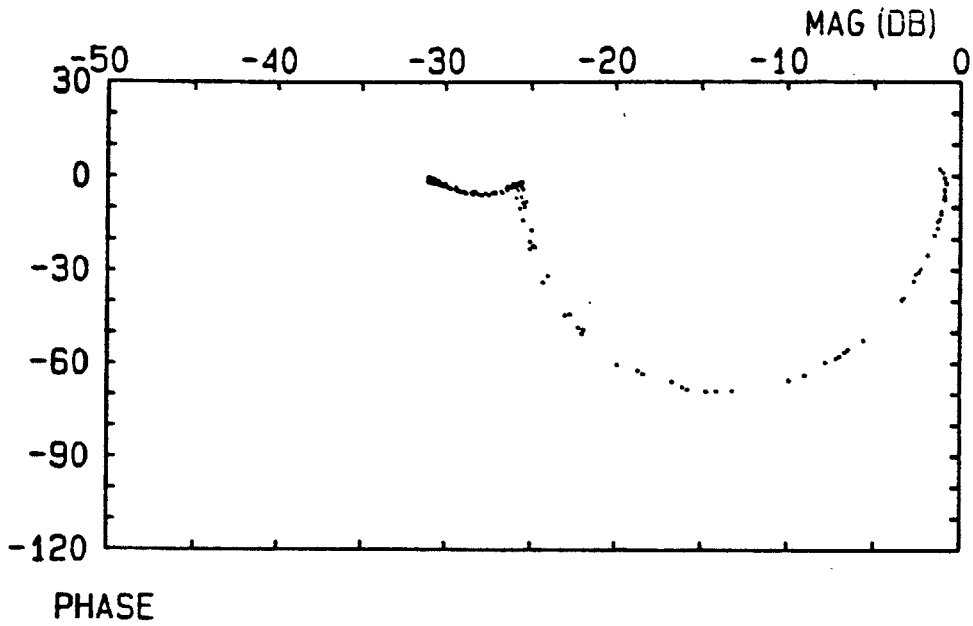


Figure 5.15.c Raw Gain-Phase Data Obtained with the 1.66 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

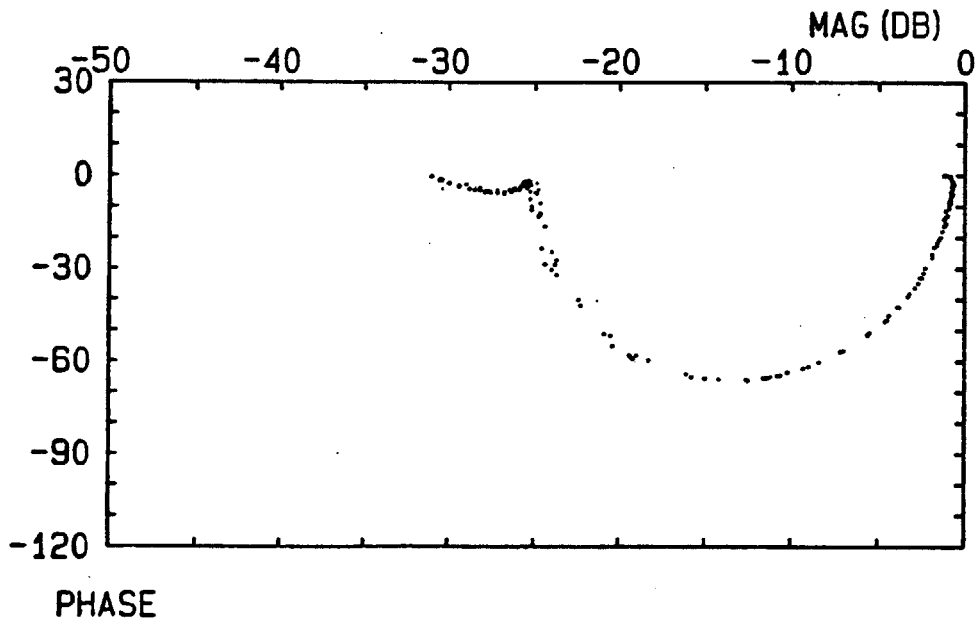


Figure 5.15.d Raw Gain-Phase Data Obtained with the 2.15 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

substrate resistance that produces positive phase at low gain. The upper curve of each pair corresponds to data taken at 1000 Hz, which would be expected to show the greatest positive phase. Data for all lower frequencies trace the lower curve. The 1.66 and 2.15 micron sensors do not show this artifact because they exhibit much less positive phase than the devices with thinner dielectric beneath the lock and key.

Figure 5.16.a shows the gain-phase trajectory for an unpassivated 0.85 micron device and a resin cure at 80 °C. Figure 5.16.b shows the trajectory for a passivated device of the same type, and a resin cure also at 80 °C. Although the passivation was largely successful, reducing the positive phase at the beginning of cure to only 4°, from 20° for an unpassivated device, the phase shift was not entirely eliminated. Later inspection of the sensor revealed that the resin reacted with the RTV, and may have exposed a stray conductive path to ground. Nevertheless, because this opened pathway would have much less area than a completely unpassivated chip, the positive phase was considerably reduced, and should not significantly affect the cure trajectory.

The extracted values of permittivity and loss factor for points along the trajectory's main curve, for all four devices monitoring the 80 °C cure, are presented in Figure

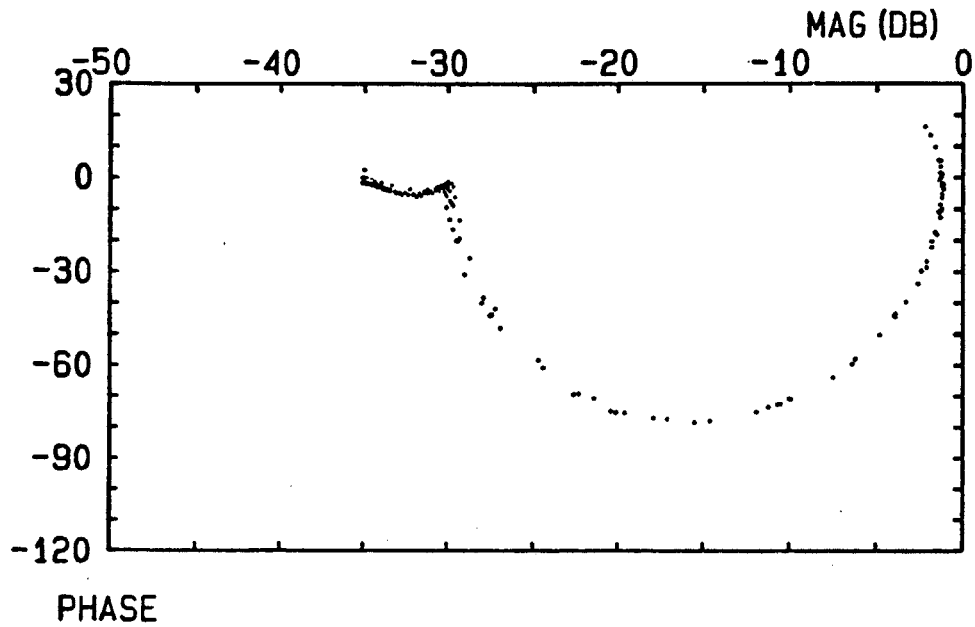


Figure 5.16.a Raw Gain-Phase Data Obtained with an Unpassivated 0.85 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C. Note +20° Phase

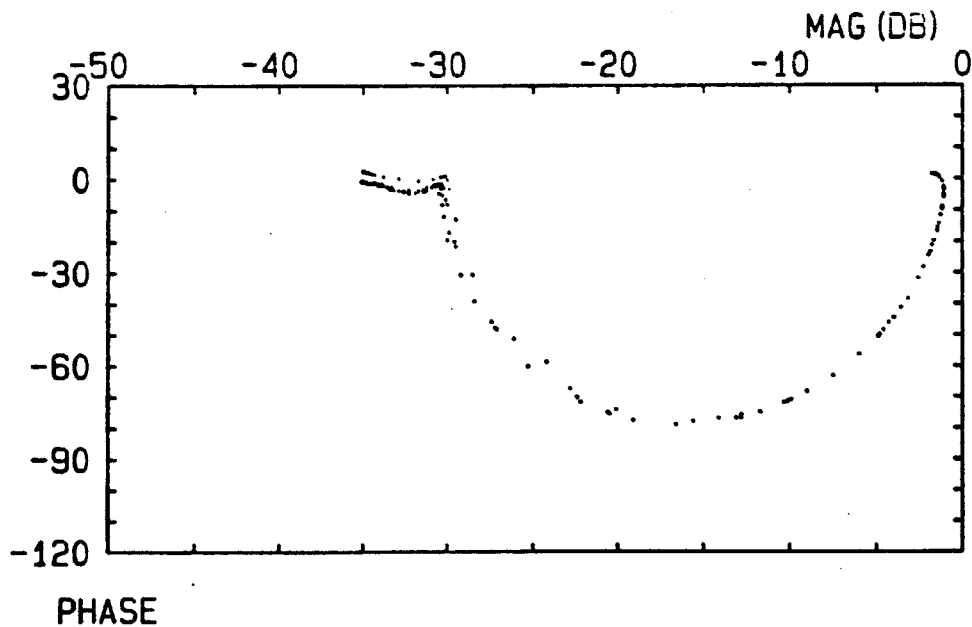


Figure 5.16.b Raw Gain-Phase Data Obtained with a Passivated 0.85 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C. Note +4° Phase

5.17 as Cole-Cole plots on logarithmic axes. One of the factors affecting the reliability of measurements is the compression of constant permittivity contours near the origin, as can be seen in Figure 3.16. When the resin is highly conductive at the beginning of cure, any gain offset or spurious noise can produce small shifts in the location of a data point in gain-phase space, in turn causing large deviations in interpolated values of permittivity. This consequence is most easily seen in the Cole-Cole plot of data from the 0.45 micron device. At high loss factors the permittivity obtained from this particular sensor is half the permittivity obtained from the other devices. The 0.85, 1.66 and 2.15 micron devices, however, show good agreement among each other in the region of high loss factor.

The measured permittivities at loss factors less than 40, though, do not show especially good agreement in this series of experiments. The permittivity at the cusp of the cure trajectory varies from 6.5 to 8.0, a disagreement greater than ten percent. Figure 5.18 shows the Cole-Cole plot for data in this region of the cure trajectory. The discrepancy may be caused by the reaction that took place between the DGEBA/MPDA and the RTV. Since the silicone rubber had a dielectric permittivity of about 3, if some mixing of components took place, then it would be expected

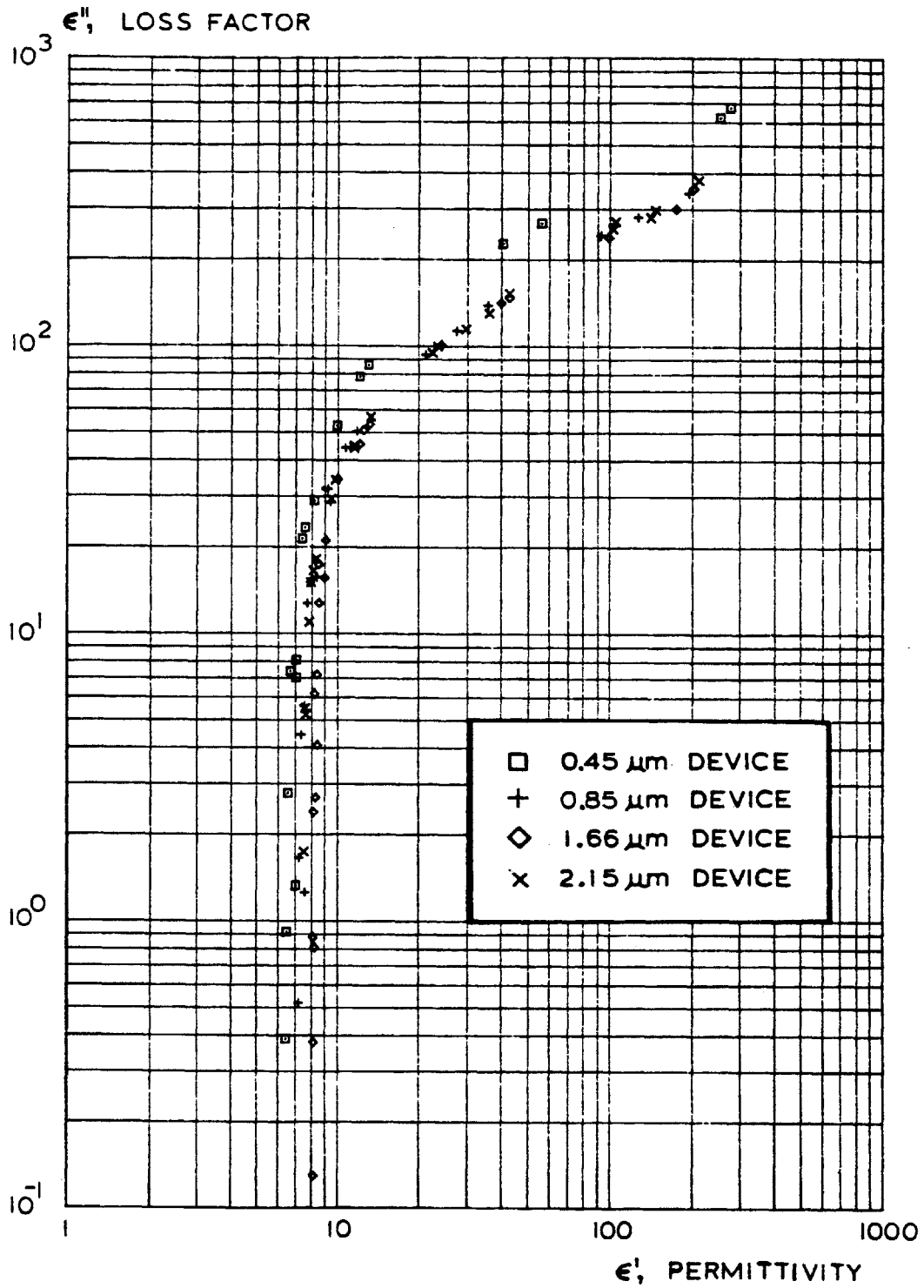


Figure 5.17 Cole-Cole Plot of Data Obtained with All Sensor Geometries for the DGEBA/MPDA Cure at 80°C

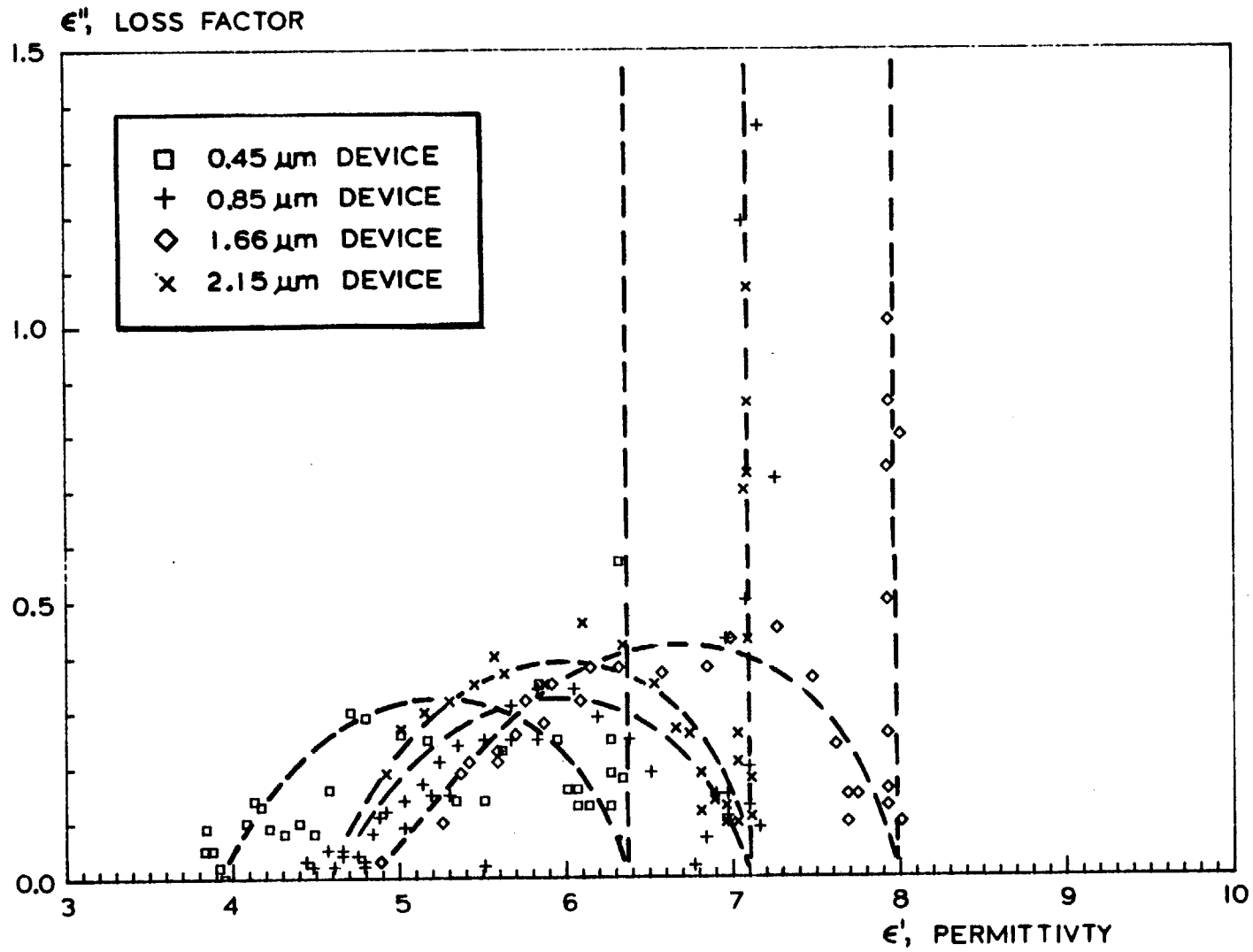


Figure 5.18 Cole-Cole Plot of Data Near End of Cure, Obtained with all Device Geometries for the DGEBA/MPDA Cure at 80°C

that the contaminated resin should have a lower permittivity than pure DGEBA/MPDA.

In contrast, the resin cures performed at 60 °C, without RTV passivation, yielded excellent agreement in measuring the same permittivity of 8.0 at the cusp; however, the stray conduction path to ground introduced offsets in the trajectory at the beginning of cure. Consequently, the extracted dielectric information do not show good agreement between devices at high loss factors. Figure 5.19 shows the Cole-Cole plot for the main curve, as extracted from data from the four types of devices used. As can be seen, the disagreement at high loss factor is significant. Figure 5.20 shows the Cole-Cole plot near the cusp. There the agreement among all devices is very good, and collected dielectric information from all sensors form a single curve. Sheppard [8] has interpreted the dielectric behavior in this region near the end of cure as dipolar orientation with a distribution of relaxation times.

For both the 80 °C and 60 °C cures, the twin curves observed in gain-phase data near the end of cure become, after correction for positive phase, single curves in $\epsilon' - \epsilon''$ space. This corrected data for passivated devices and the 80 °C cure, though, do not agree well

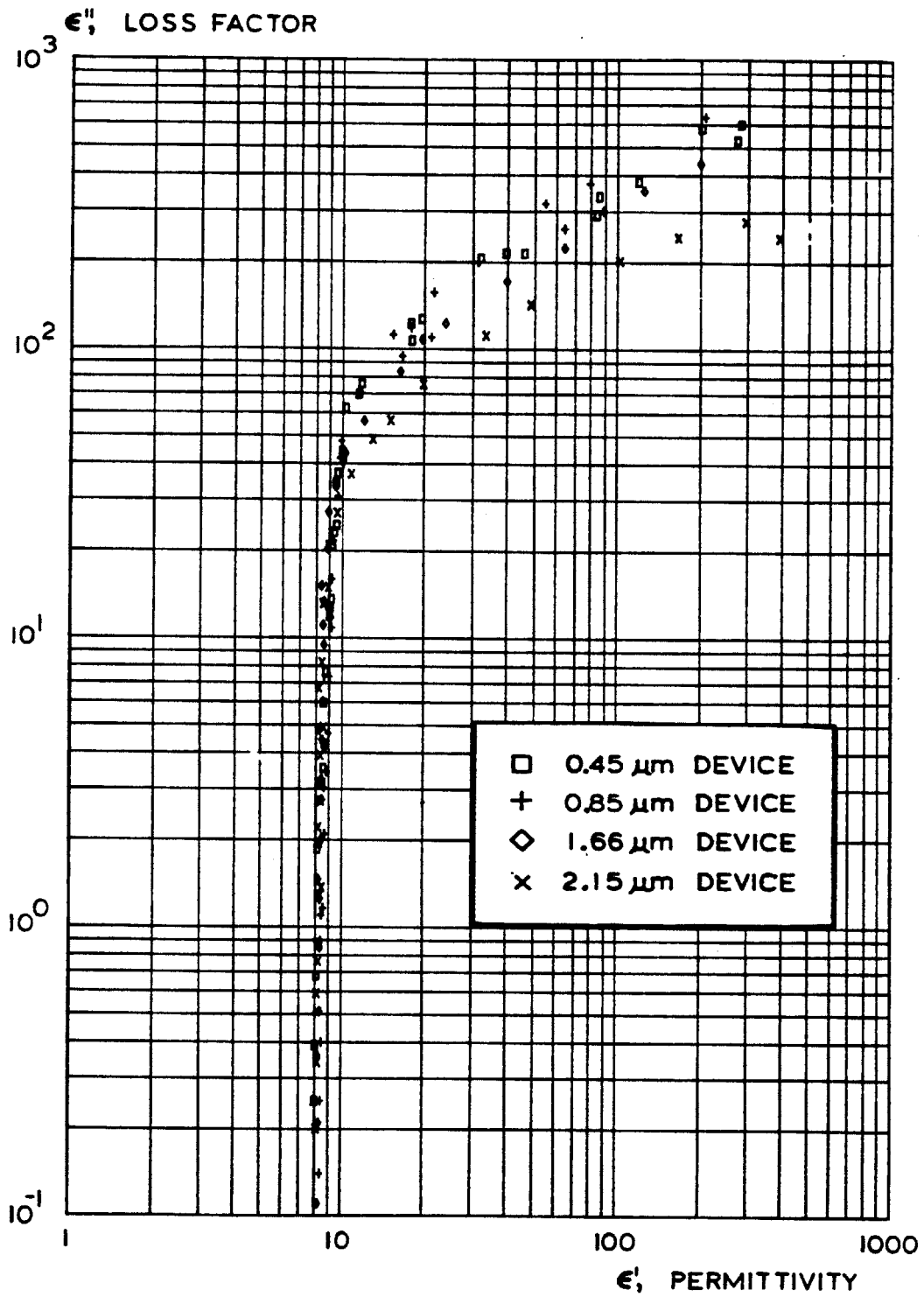


Figure 5.19 Cole-Cole Plot of Data Obtained with All Sensor Geometries for the DGEBA/MPDA Cure at 60°C

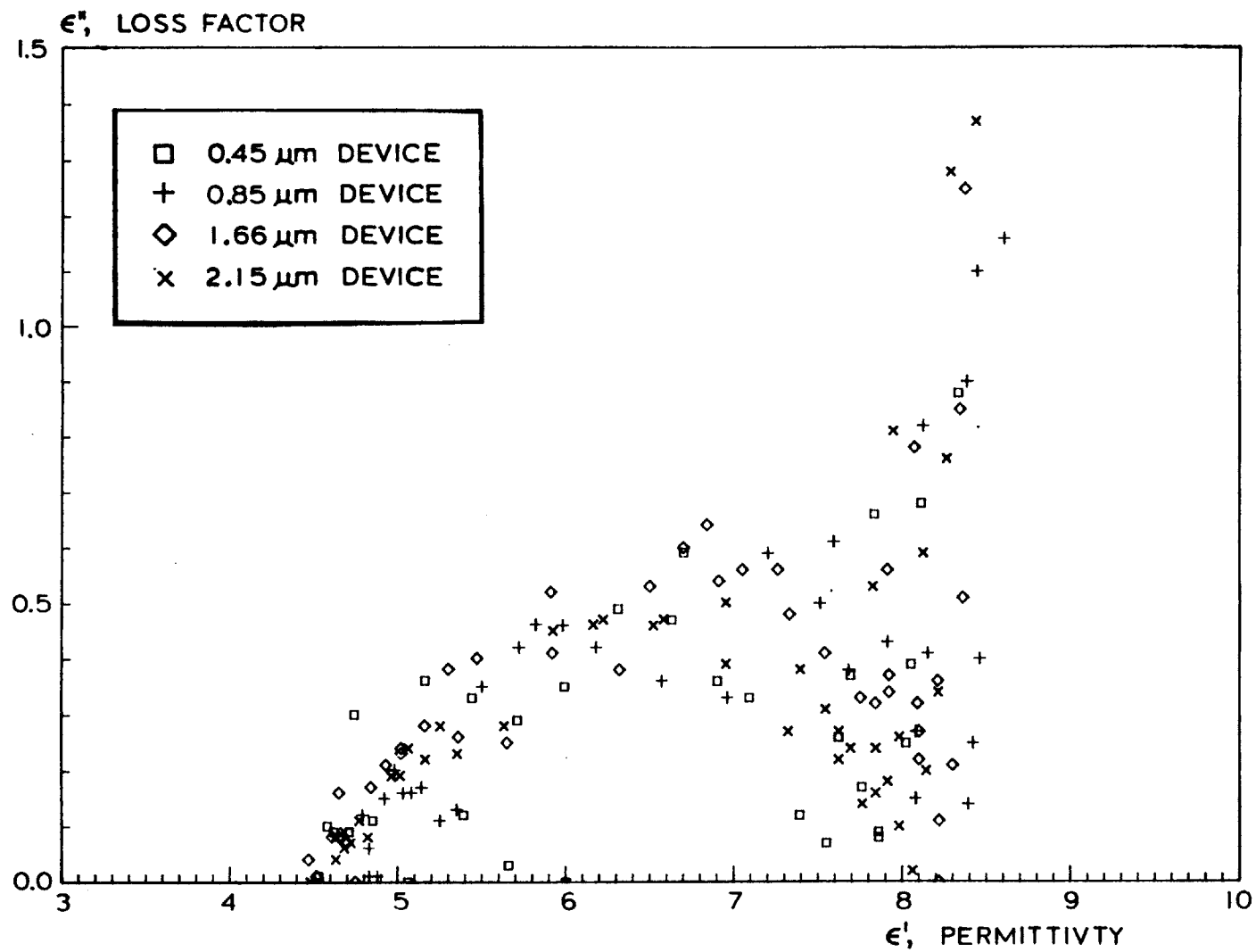


Figure 5.20 Cole-Cole Plot of Data Near End of Cure, Obtained with all Device Geometries for the DGEBA/MPDA Cure at 60°C

among the four sensors because of the possible RTV contamination.

To summarize the data obtained from experiments observing complete resin cures, the passivated devices gave consistent measures of permittivity and loss factor at the beginning of cure, when the resin permittivity is high and not likely to be affected by reaction with RTV. Near the end of cure the reaction products may have contaminated the resin and introduced errors. Unpassivated devices did not give consistent results near the beginning of cure because of large positive phase shifts resulting from stray conduction to ground, but they do agree very well with each other at the end of cure because the resin is uncontaminated. Therefore it may be concluded that sensor calibration can be obtained by the finite difference simulation, and that the effects of different electrode geometries can be taken into account when extracting permittivity and loss factor from gain-phase data.

When bulk conductivity is calculated from the loss factor, and its time dependence is obtained, it becomes possible to see structure which may be useful in evaluating the state of cure. Figure 5.21 shows ϵ'' extracted from a 0.85 micron device for a cure at 60 °C. The loss factor is inversely proportional to frequency for the times these data represent. This indicates either the frequencies

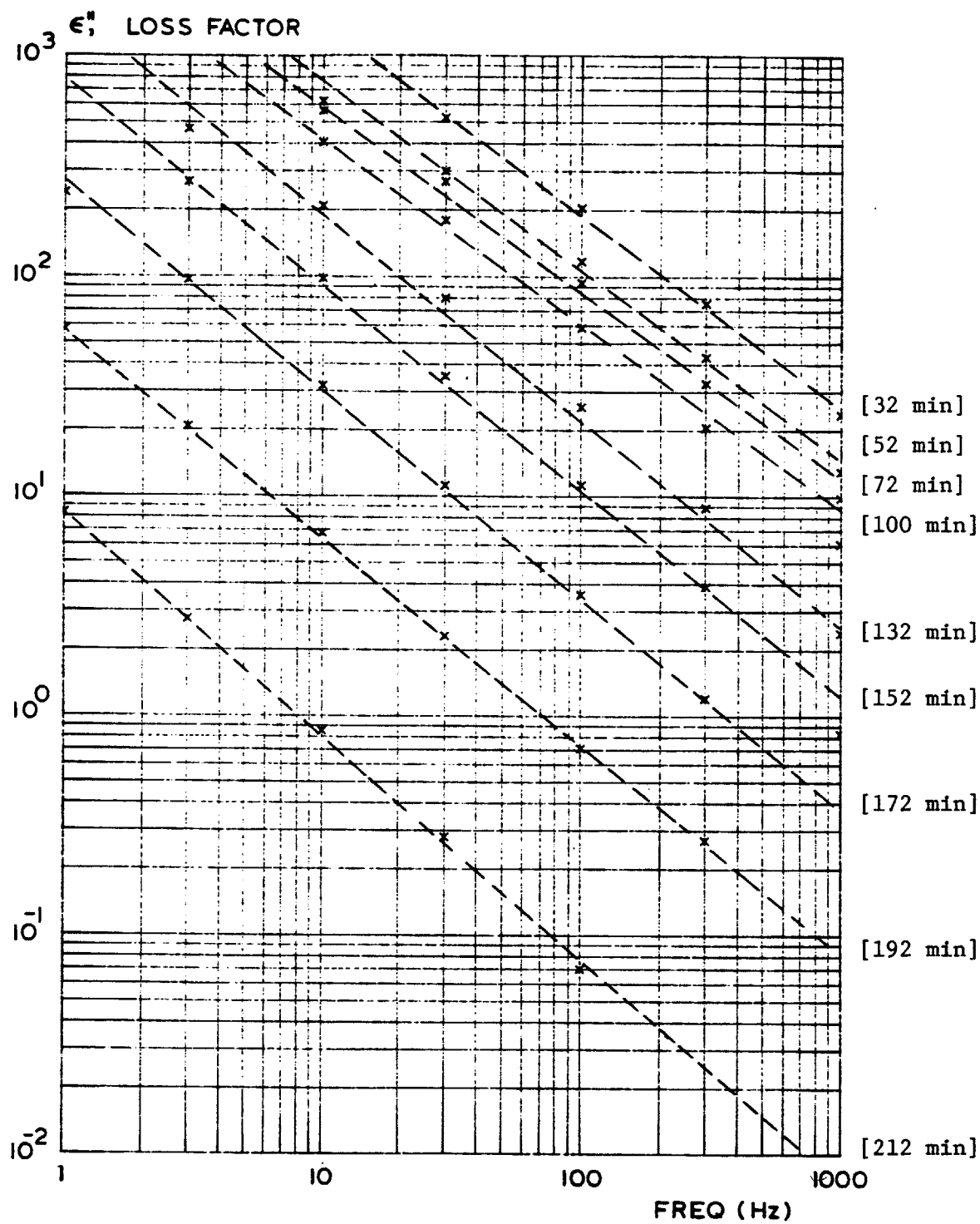


Figure 5.21 Loss Factor vs. Frequency for Curing DGEBA/MPDA at 60°C, Parameterized with Respect to Time

used were always much greater than that at which dipole orientation shows a loss peak; or the loss is dominated by a bulk, frequency independent conductivity.

Figure 5.22 shows the time dependence of a low frequency bulk conductivity obtained from these data, and compares it with DC conductivity data by Acitelli et al. [50], which was taken with parallel plate current measurements at 52 °C. The plot in both cases, on log-log scales, has two distinct slopes, with the knee of the plot attributed to the onset of gelation [50]. As measured by the CFT sensor, the time to gelation is about 60% of that obtained from DC parallel plate data at a slightly lower temperature. The agreement in slopes, though, is excellent for the conductivity after gelation. The difference in the time to gelation can be attributed entirely to the activation energy of the cure process. As reported by Senturia et al. [9], it is 11.5 Kcal/mole, which agrees with viscosity data in the literature [51]. Also, if bulk conductivity is presumed to be inversely proportional to viscosity in curing DGEBA/MPDA, then the shift in conductivity data after gelation, between the two curves of Figure 5.22, may be explained by this same activation energy.

With this correspondence between the low frequency bulk conductivity, as measured with the CFT sensor, and the DC conductivity, as measured with parallel plates,

CONDUCTIVITY ($\Omega^{-1}\text{cm}^{-1}$)

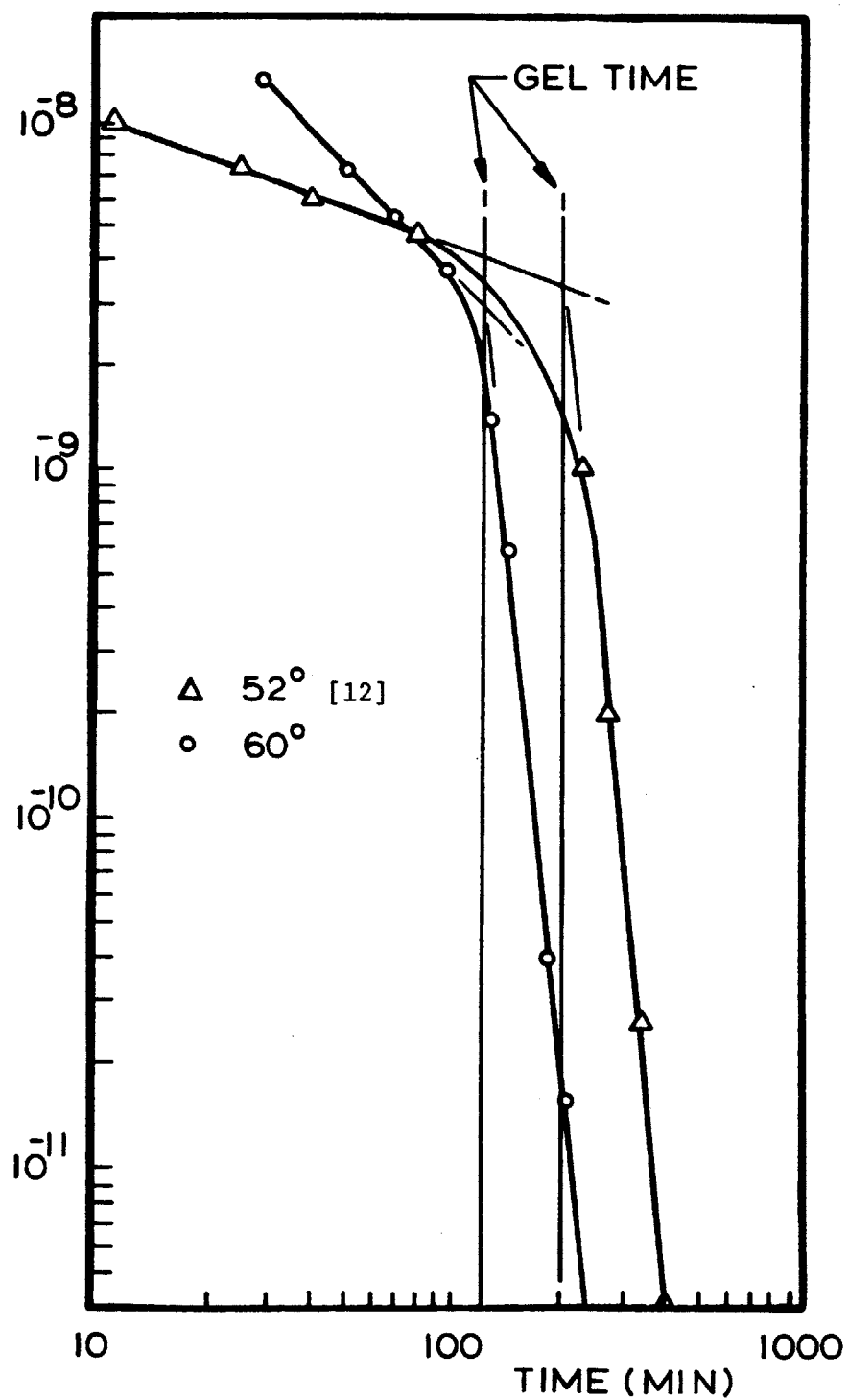


Figure 5.22 Bulk Conductivity vs. Time for Curing DGEBA/MPDA at 60°C and 52°C. Data at 52°C by Acitelli et al. [12]

one must conclude that the CFT is measuring the same type of conductivity that the DC parallel plate experiment did during the early part of cure after the onset of gelation. It may also be concluded that the electrical properties of the resin at this stage are dominated by bulk conductivity, with no visible evidence of a frequency dependent, AC conductivity arising from dipolar relaxation.

Actelli et al. report that as cure proceeds, the DC conductivity continues to decrease monotonically until it levels-out at $4 \times 10^{-16} \Omega^{-1} \text{cm}^{-1}$. The Cole-Cole plots of Figures 5.18 and 5.20, though, explicitly indicate the presence of a loss peak near the end of cure. This feature has no analog in the DC conductivity data, and behaves in a manner described by the modified Debye dielectric dispersion equations with a distribution of relaxation times. In this case, the permittivity and loss factor obtained with AC measurements represent information unavailable with DC techniques.

Clearly, in the early stages of cure, the dominant change in the dielectric characteristics of DGEBA/MPDA is a simple reduction in the bulk conductivity. When this conductivity has decreased sufficiently, the loss factor becomes small enough to reveal the AC dielectric behavior due to dipole relaxation.

All these results suggest that the CFT sensor can be useful in monitoring the cure of resins and other materials, and that the calibration method developed in this work allows the extraction of dielectric information which can be independently verified by, and agrees with, other cure monitoring techniques. In addition, the AC properties measured with microdielectrometry yield information about dipole relaxation that cannot be obtained with DC methods alone.

5.9 Gain Offset at the Beginning of Cure

A feature apparent after examination of the cure trajectories for the DGEBA/MPDA system is a consistent gain offset from the origin of approximately -1 dB at the beginning of cure. This offset has appeared in almost every cure with all four types of devices used. Since the inherent gain offset of the CFT sensors is about + 0.2 dB, the much larger observed offset cannot be an artifact of uncertainties in measurement, but must be a real phenomenon.

This behavior can be explained with the Debye dipole relaxation model, in which a Cole-Cole plot of loss factor versus permittivity describes a semi-circle. A dielectric material then has two conditions with zero loss factor, one at frequencies much higher than $1/\tau$, when the dipoles

have no time to reorient themselves in the electric field, and the second at frequencies much lower than $1/\tau$.

Figures 5.23.a-d compare the best fit Debye model, plotted in gain-phase space, with the raw data from the 80 °C cure. The Debye equations describe the data fairly well for each of the four types of sensors. At low frequencies, when the loss factor presumably goes to zero, the uncured resin appears to be a lossless dielectric with a very high permittivity. Therefore the corresponding gain-phase point shows negative gain and the zero phase indicative of pure capacitive coupling. Even the data taken at one time over a range of frequencies can be fit well by a single relaxation time, as shown in Figure 5.24. According to the model, the permittivity and loss factor distribution for one relaxation time across a range of frequencies is no different than for one frequency and a range of relaxation times, for dielectric properties are determined by the product of both. Figure 5.25 shows the Cole-Cole plot of the DGEBA/MPDA resin cured at 80 °C. The data are from the 0.85 micron sensor. To extract dielectric information from data near the origin, an extended look-up table was specially generated for this device. With it, the maximum permittivities and loss factors that can be determined are both 4096, and exclude only a $-0.1 \text{ dB} \times 1^\circ$ region about the origin of gain-phase space. The results form

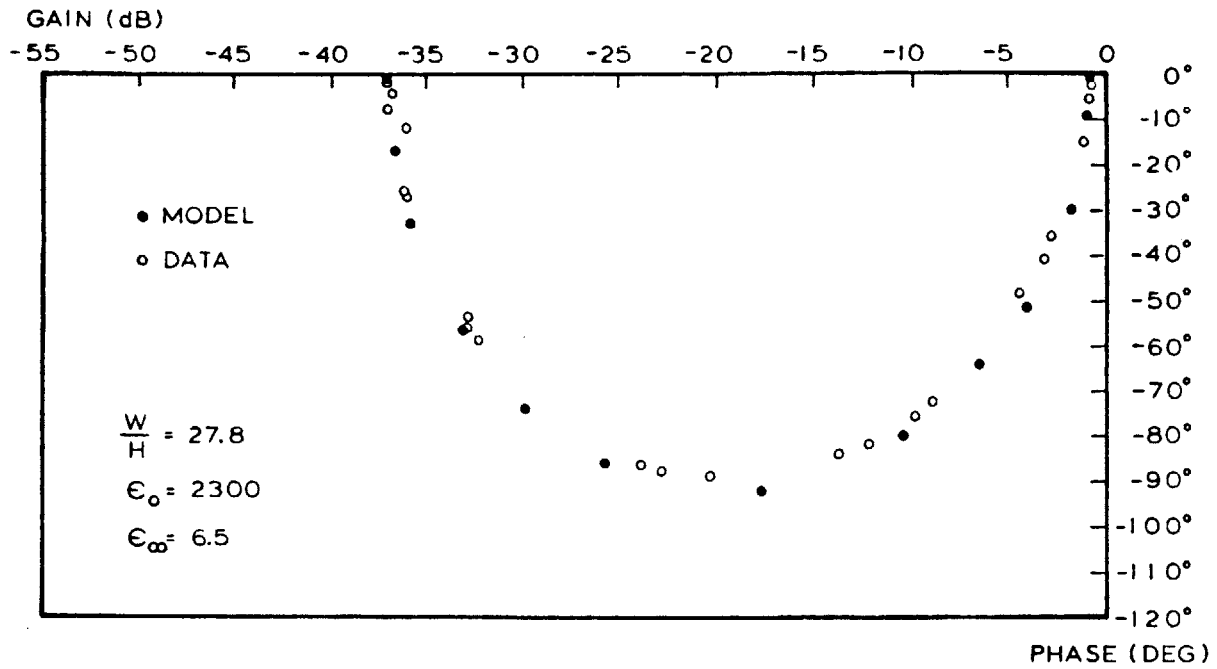


Figure 5.23.a Best Fit Debye Model to Data Obtained with the 0.45 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

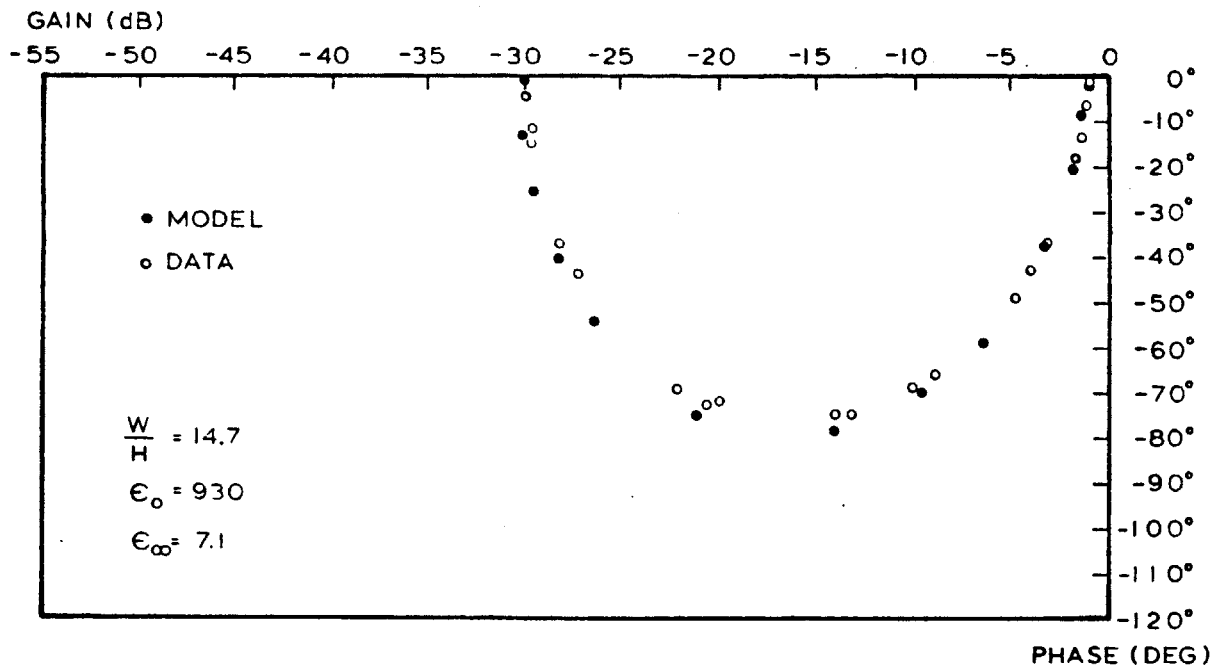


Figure 5.23.b Best Fit Debye Model to Data Obtained with the 0.85 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

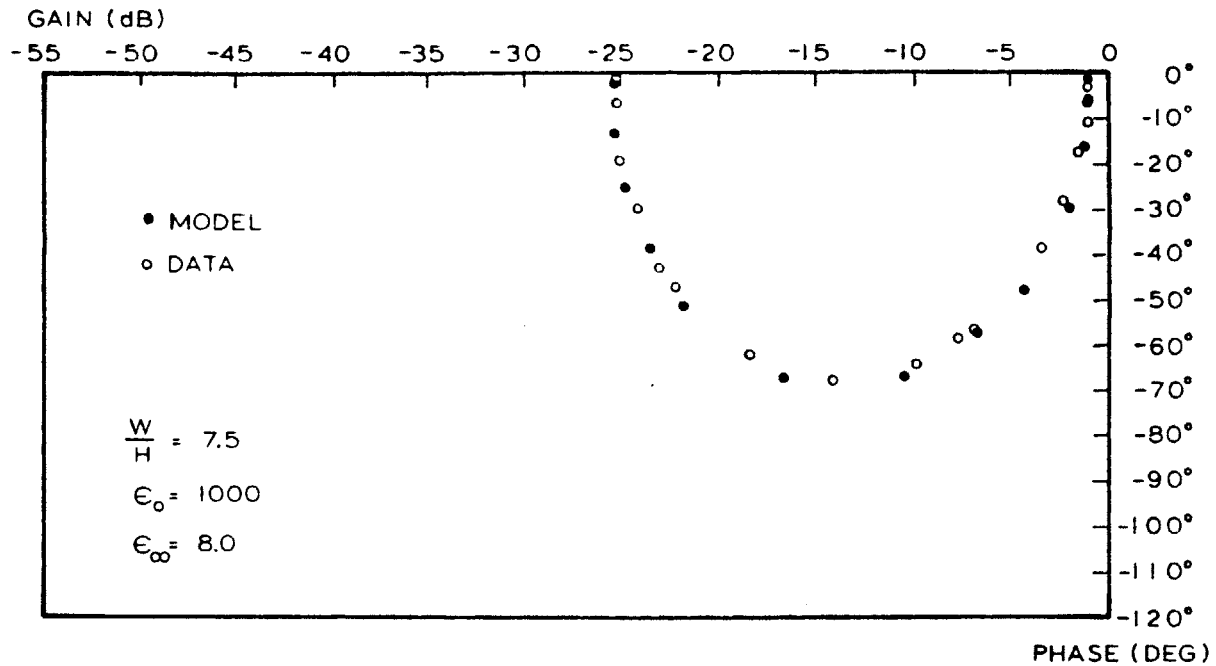


Figure 5.23.c Best Fit Debye Model to Data Obtained with the 1.66 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

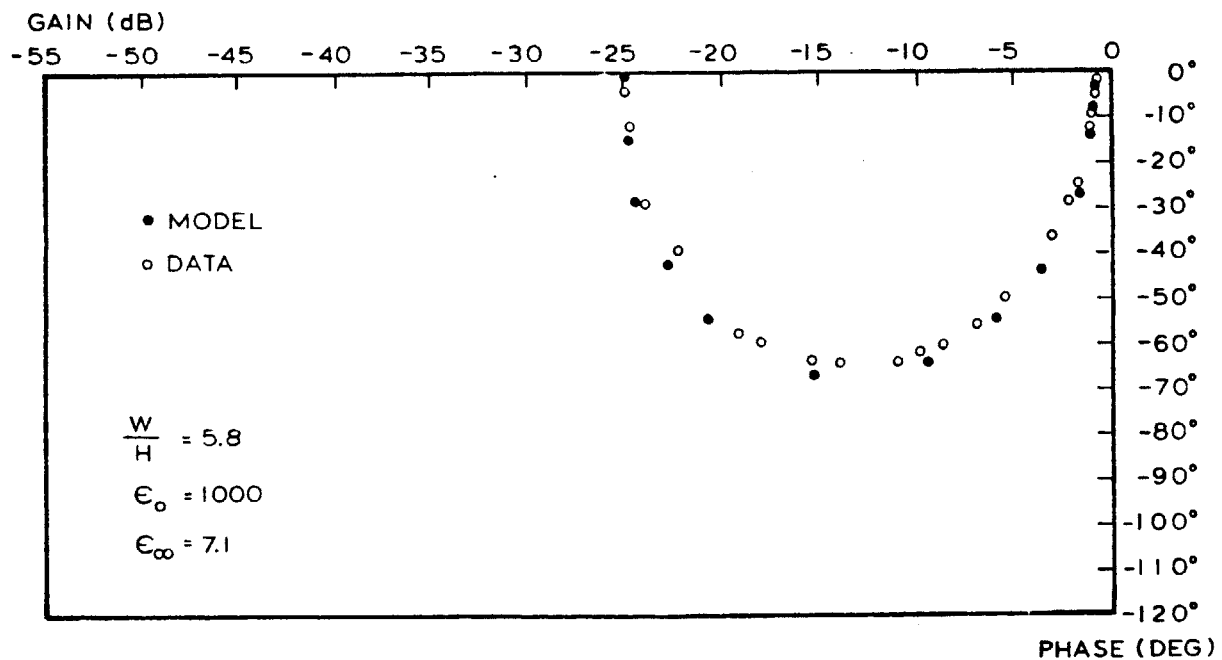


Figure 5.23.d Best Fit Debye Model to Data Obtained with the 2.15 Micron Sensor Geometry for the DGEBA/MPDA Cure at 80°C

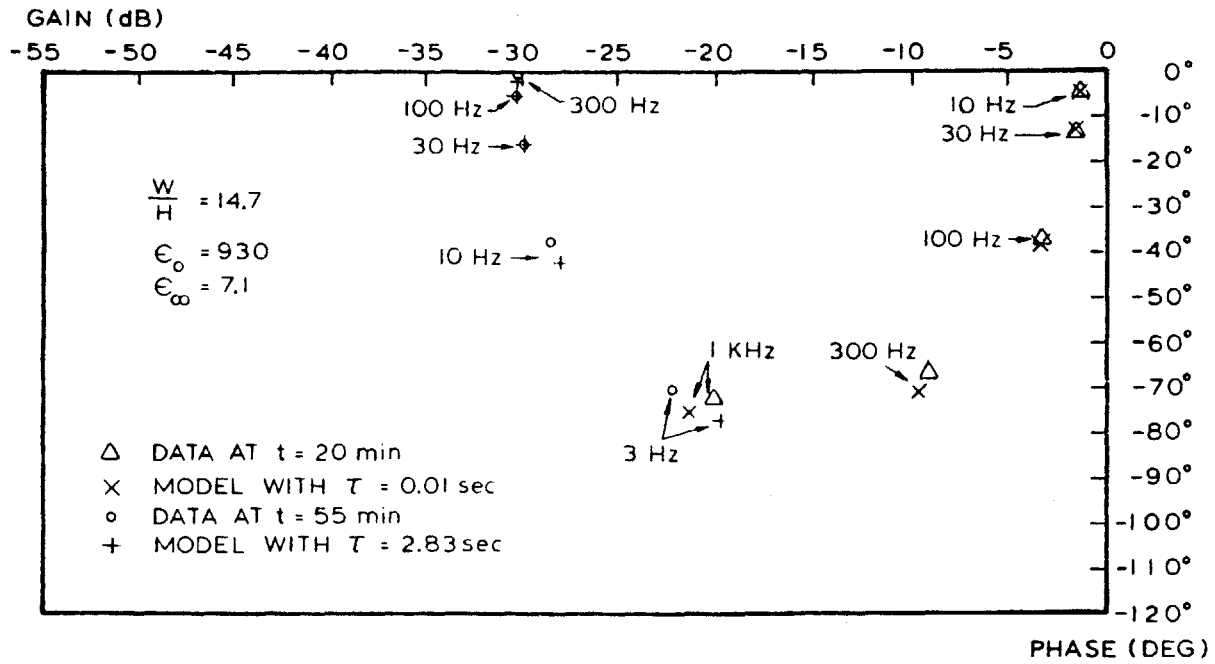


Figure 5.24 Comparison of Debye Model at Two Relaxation Times with Data Obtained at Two Times for the DGEBA/MPDA Cure at 80°C

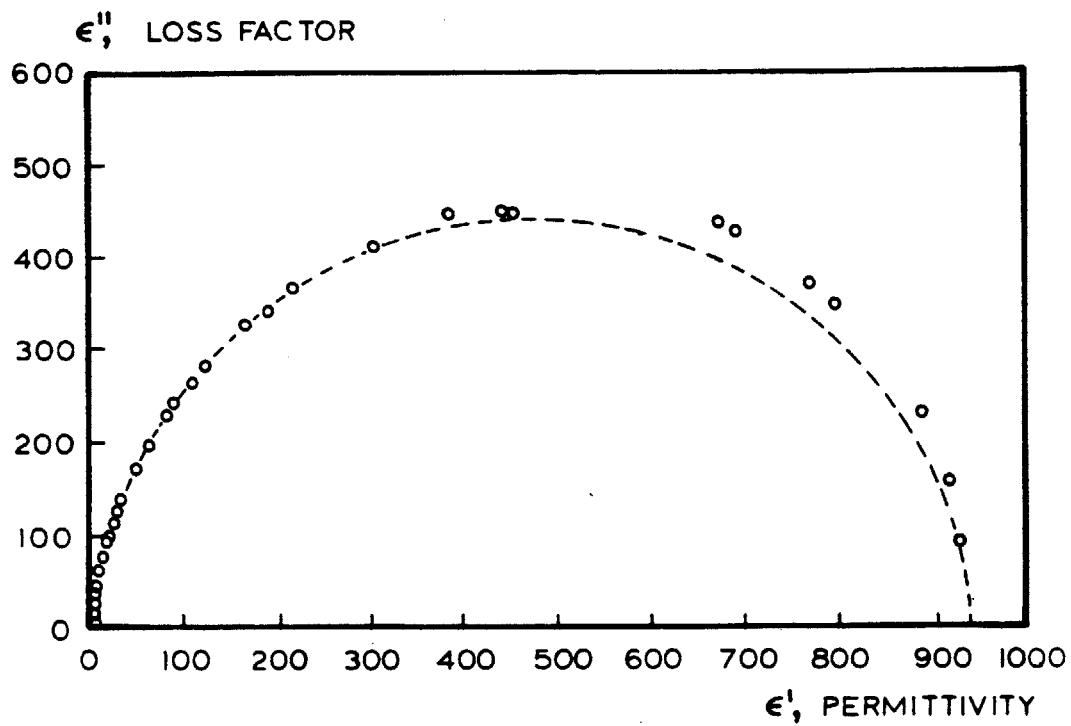


Figure 5.25 Cole-Cole Plot of Data Extracted with Extended Look-up Tables. Data was Obtained for 0.85 Micron Geometry Sensor for DGEBA/MPDA Cure at 80°C

a definite semi-circle as required by the Debye model. Figure 5.26 shows the Cole-Cole plot on log-log scales for comparison with previously presented data.

One argument, however, suggests that the gain offset cannot be explained by dipolar relaxation. The permittivities of 900 to 2000 required to fit the data at the beginning of cure appear too high for the estimated maximum number of dipoles in a unit volume of resin. In addition, when uncured polyimide was placed on a fully passivated device, the gain offset was only -0.3 dB, implying an even greater permittivity on the order of 10,000.

As shown by Acitelli, the curing DGEBA/MPDA resin has a significant bulk conductivity which is completely omitted in a Debye dipole relaxation model. This fact alone renders the Debye model invalid as the sole explanation of the gain offset, for both the frequency-dependent AC conductivity and frequency-independent bulk conductivity must be included in the loss factor. Therefore, at low frequencies the bulk conductivity term would dominate, for in this regime the Debye model contributes little or no loss from dipole orientation.

Given the assumption of a bulk conductivity in addition to dipole orientation, then at the start of cure the lock and key's fingers must be shorted together, and the cure trajectory must begin at the origin of gain-phase space.

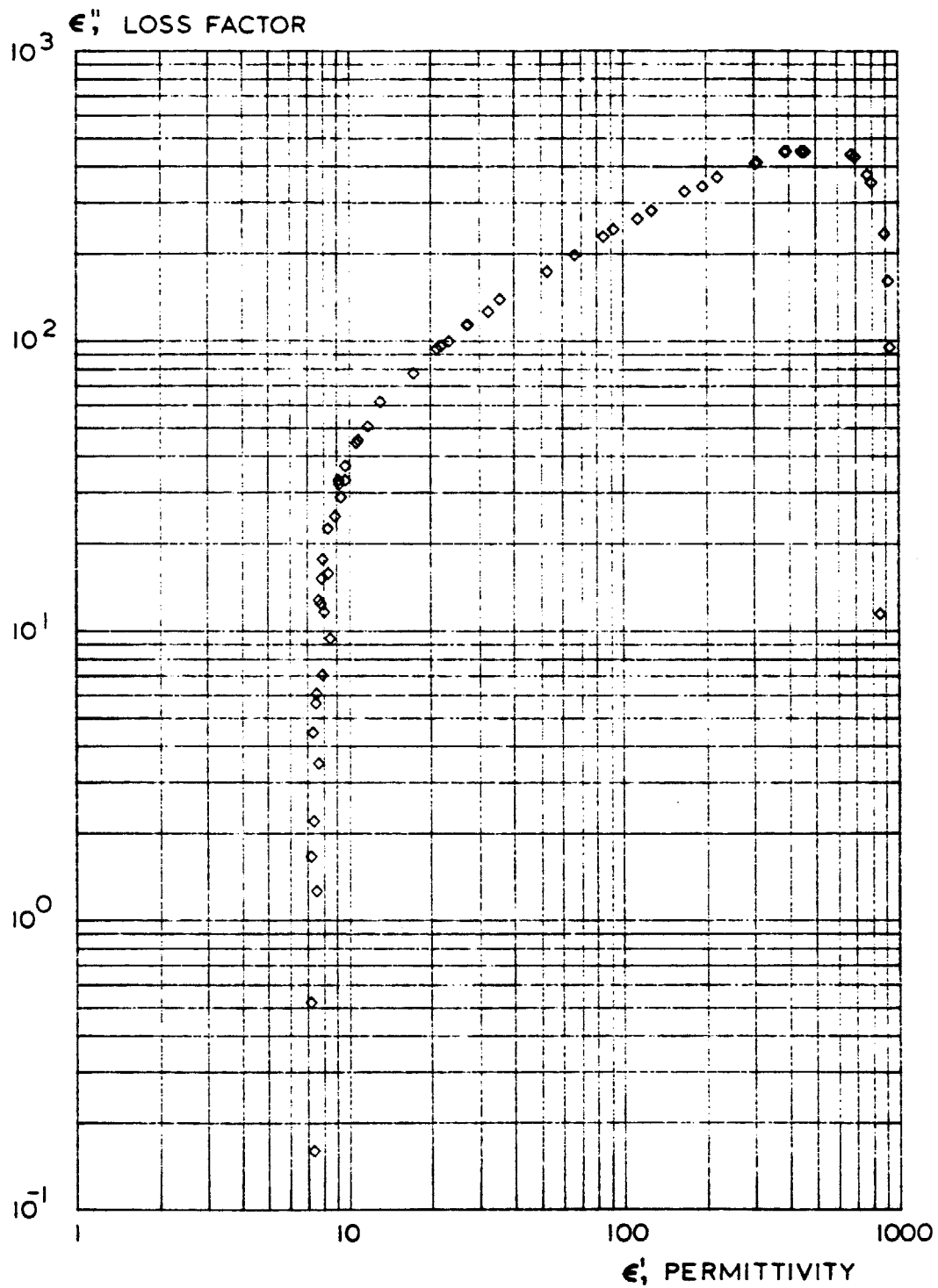


Figure 5.26 Cole-Cole Plot on Logarithmic Axes of Data Extracted from Extended Look-up Tables. Data was Obtained with 0.85 Micron Sensor Geometry for DGEBA/MPDA Cure at 80°C

Since the -1 dB offset near the origin is a reproducible effect, it motivates a refinement of the model for the resin-electrode system. Clearly, inclusion of a blocking layer capacitance, as in Figure 5.27.a, will explain the experimental gain offset in cure trajectories. When the resin has been freshly mixed and is highly conductive, the lock and key electrodes are coupled to each other through this capacitance C_{BL} , which then determines the voltage division at the floating gate and produces a non-zero, negative gain at high loss factors.

Calculation with the voltage division law reveals that a total blocking layer capacitance between 30 and 60 pF is necessary to explain the various experimental gain offsets. Assuming this capacitance has the area of the electrode fingers and a permittivity of 7.0, then the blocking layer thickness must be between 1000 and 450 angstroms.

This thickness is too great to be caused by either a native aluminum oxide or residual polyimide layer. Also, the data from passivated sensors with uncured polyimide show an offset of only -0.3 dB, suggesting that the gain offset is material dependent.

Interestingly, the blocking layer thickness is in the range of those for typical semiconductor space-charge

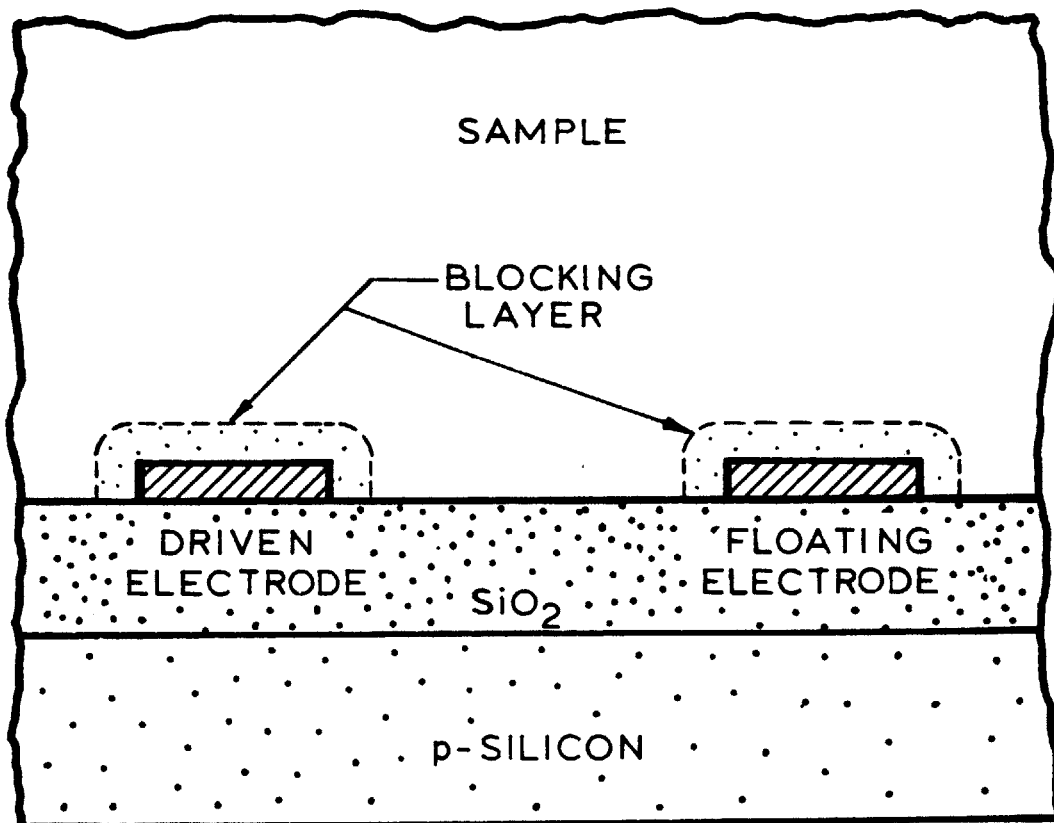


Figure 5.27.a Illustration of Space-Charge Blocking Layer around Lock and Key Electrodes

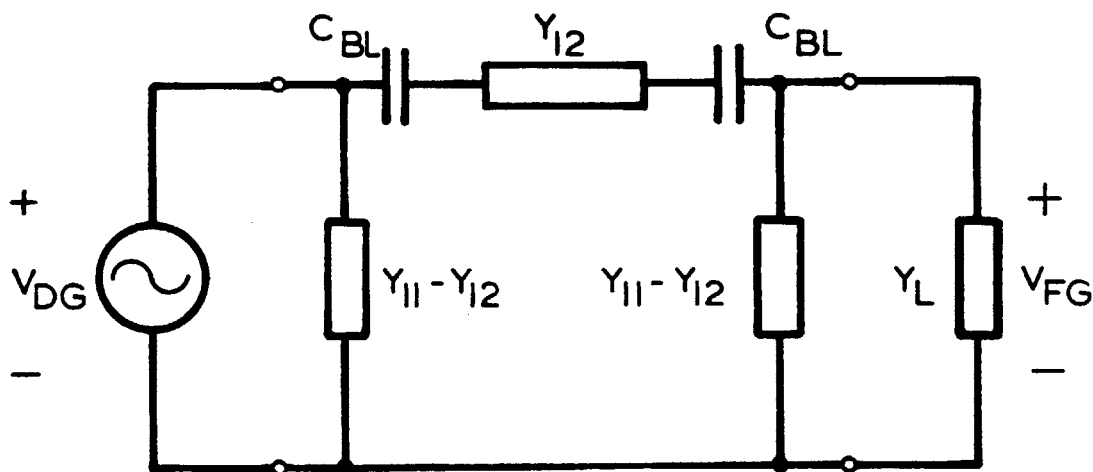


Figure 5.27.b First-order Model of Blocking Layer Inserted in Sensor Admittance Model

layers, raising the possibility that the electrode blocking layer has a similar origin.

The space-charge region width is closely related to the Debye screening length and determines the small signal capacitance of the layer. Uncured polyimide is much more conductive than than uncured DGEBA/MPDA and should have a shorter Debye length. Consequently, it should have a thinner space-charge layer, a proportionally greater blocking layer capacitance and a smaller gain offset--which is observed.

When a blocking layer capacitance is added to the π -equivalent model, as in Figure 5.27.b, and given an empirical value to reproduce the offset of each particular experiment, the look-up tables can be recalculated. In a strict sense, this added capacitance cannot accurately model the blocking layer, for no attempt has been made to incorporate any frequency-dependence in it, nor have the lock and key's two-port admittance parameters been properly recalculated to include a blocking layer and its effect on the electric field distribution. This model is only a first-order attempt to observe the behavior of a lock and key with this additional component. Extraction of the permittivity and loss factor from the new calibration tables yields the plot of Figure 5.28 for the DGEBA/MPDA cure at 80 °C with the four types of sensors. The agreement

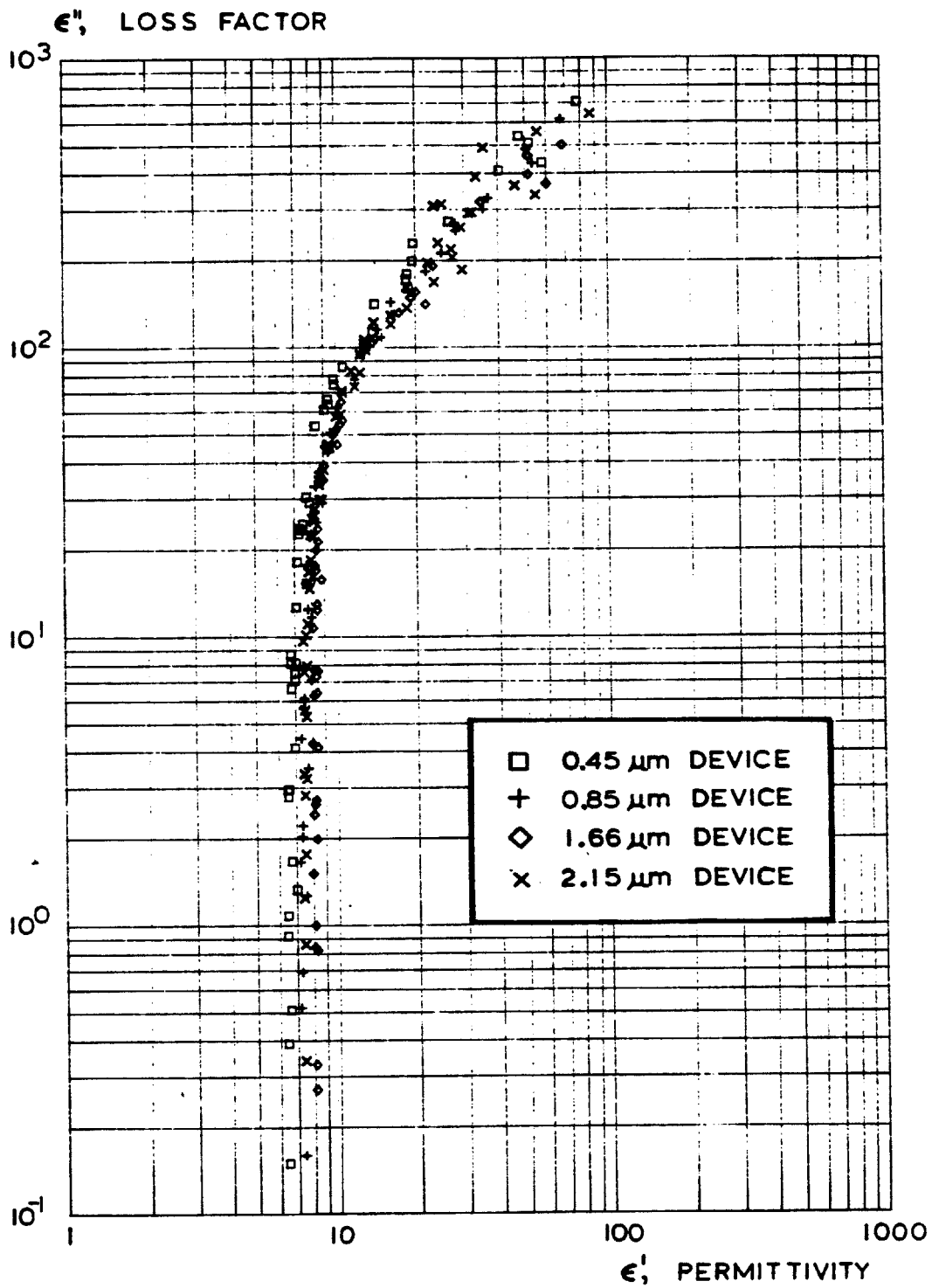


Figure 5.28 Data, after Correction for Blocking Layer in Figure 27.b, for all Sensor Geometries for DGEBA/MPDA Cure at 80°C

between devices at high loss factors has improved significantly, while the data at low loss factor are unaffected. Figure 5.29 shows both the original Cole-Cole plot of the cure, and a corrected one for the 0.85 micron device. These data were obtained with the extended look-up tables generated for this particular geometry. The Debye model semi-circle has become a trajectory where the loss factor progresses smoothly and monotonically from a high value at the beginning of cure to a low one at the end. This result is consistent with the observation that the resin has a bulk conductivity which decreases with cure. Figure 5.30 shows the Cole-Cole plots on logarithmic scales, for comparison with earlier data.

Analyses of space-charge effects at electrode-electrolyte interfaces [24],[35],[36] have included considerations of electrode polarization, ionic discharge, capacitive and rectifying blocking layers, and carrier mobilities and frequency dependences. It has been found that when the medium is highly conducting and assumed homogeneous, the experimentally measured dielectric permittivities increase enormously at low frequencies.

The theory of AC space-charge polarization effects, developed by Macdonald [24], shows that this apparent dielectric information can be highly misleading when electrode blocking layers are not included in models of

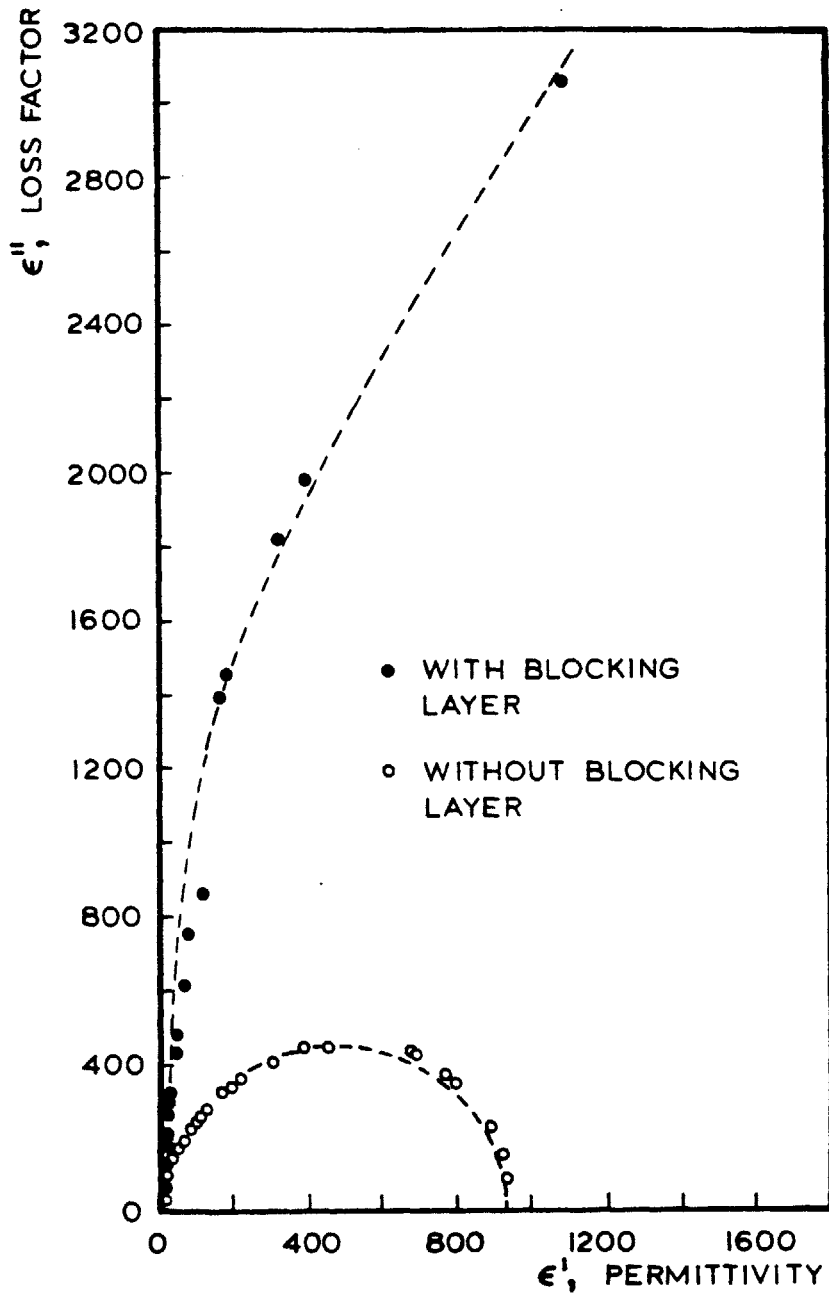


Figure 5.29 Comparison of Data for DGEBA/MPDA Cure at 80°C with and without Correction for Blocking Layer of Figure 5.27.b.

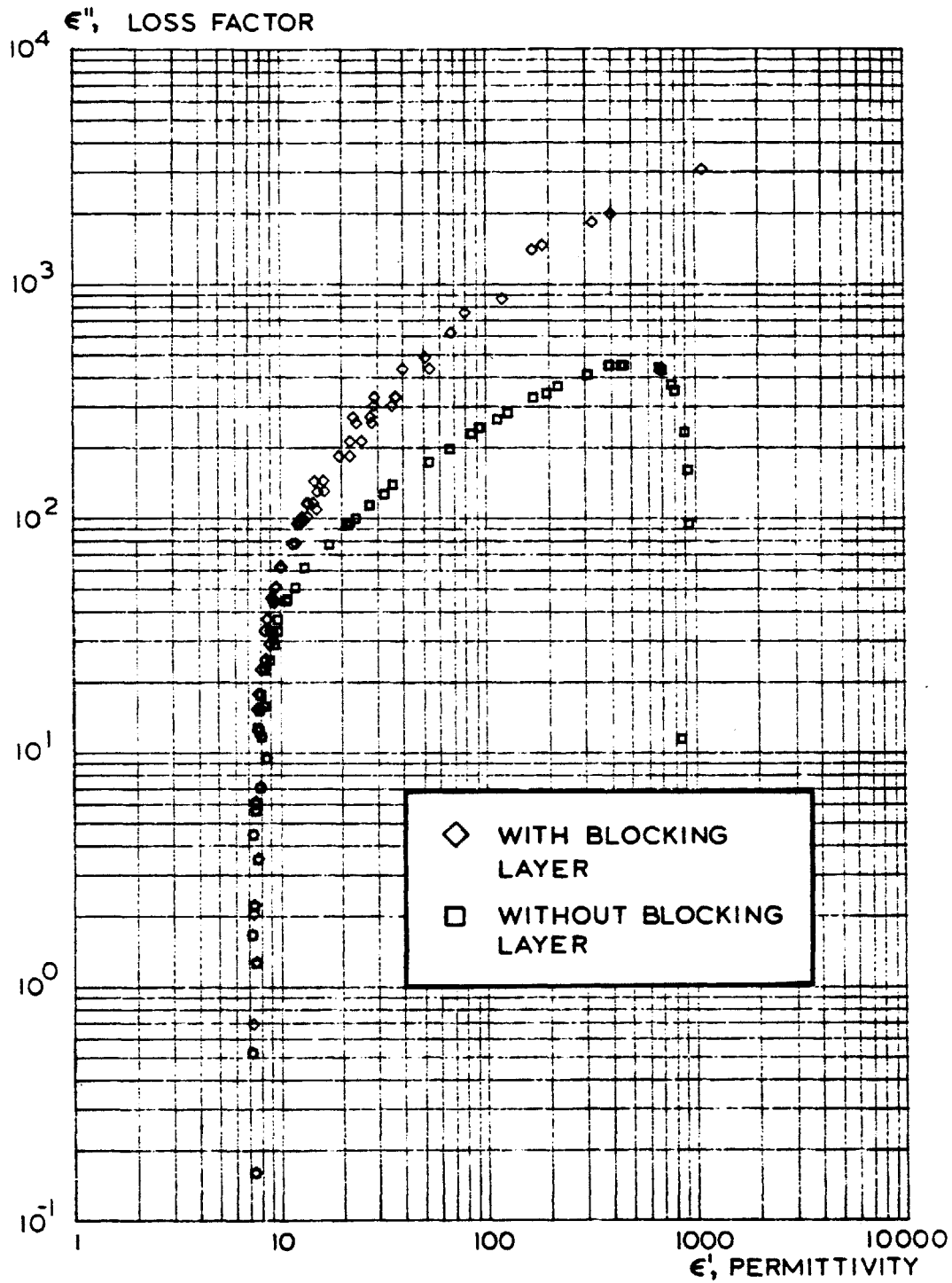


Figure 5.30 Comparison of Data for DGEBA/MPDA Cure at 80°C with and without Correction for Blocking Layer of Figure 5.27.b, Plotted on Log-Log Scales

electrolytic systems. He has determined that under certain conditions the apparent permittivity and loss factor vary with frequency according to the Debye dielectric dispersion equations with a single relaxation time--although the mechanism is not dipole orientation. Specifically, the Debye equations describe cases where a) charge carriers of only one sign are mobile, with arbitrary recombination time; b) charge carriers of both signs are mobile, with the same mobility and arbitrary recombination time; and c) charge carriers of both signs are mobile with unequal mobilities and very short recombination times.

His results depend on the RMS Debye length:

$$L_D = \sqrt{2 D \tau_D} \quad [5.9.1]$$

where D = diffusion coefficient for free charges, and

$\tau_D = \epsilon / \sigma$, the dielectric relaxation time.

The space-charge layer series capacitance is inversely proportional to this Debye length.

In an extremely simplified manner, the frequency dependence of the blocking layer, and also the observed permittivity and loss factor, may be explained with the finite mobility of free charged species. At the beginning of cure, when the viscosity is low, and the conductivity and diffusivity are high, the RMS Debye length is small. As the viscosity increases with extent of cure, the RMS

Debye length increases also. At a given stage, high frequencies do not allow sufficient time for complete formation of the blocking layer, for the mean distance a carrier can travel during a half cycle has become shorter. The electrode blocking capacitance therefore decreases at greater frequencies. It also decreases with the extent of cure because blocking layer thickness has increased.

For a certain bulk permittivity and conductivity, then, the effect is to add a frequency dependent capacitance in series between the electrode and the resin. With increasing frequency, the blocking layer capacitance becomes smaller and reduces the total inter-electrode admittance. The signal at the floating gate becomes correspondingly attenuated, and negative phase develops from the equivalent parallel capacitance and conductance of the bulk resin.

This explanation, while crude and very qualitative, elucidates the relationship between viscosity and conductivity, and how they give rise to an apparent permittivity and loss factor which can still be useful in evaluating the state of cure in a resin--even though the measured dielectric properties may be very different than the actual ones. The model also clarifies why the frequency dependence of the permittivity and loss factor can be interpreted with the Debye equations, although they are not physically

relevant, to yield an artificial quantity--the relaxation time--which reflects the nature of the resin at a particular moment.

It appears that an interfacial region between the electrodes and resin can account for discrepancies in dielectric information between different devices when a gain offset is is involved. The presence of such a blocking layer, though, has not been experimentally verified, and could be a subject for additional investigation.

CHAPTER 6
CONCLUSIONS

6.1 Summary of Results

When used as a monitor of curing resins, the floating gate CFT sensor has several advantages over conventional parallel plate techniques. Its planar electrode geometry is fixed and unaffected by pressures which may be encountered in a manufacturing environment, and because the device is an integrated circuit, it is small and may be placed unobtrusively in an object being assembled, or employed to study samples weighing only milligrams. On-chip transistor amplification extends the usable frequencies down to at least 1 Hz for greater sensitivity to dielectric changes farther into cure.

A generalized method of two-dimensional finite difference simulation has been developed and applied toward the study of the lock and key structure. By representing potentials as phasors, it is possible to calculate the sinusoidal steady state behavior in a lossy dielectric medium. Numerically computing the surface integral of the electric field around the electrodes yields two-port admittance parameters for the lock and key, which in turn are used to account for capacitive loading by the FET on the floating electrode. After generation of a look-up

table for responses over a range of permittivity and loss factor, an interpolation routine enables extraction of quantitative dielectric information from raw gain-phase data.

A double-level metal process employing polyimide has been developed and used to fabricate sensors for resin-cure experiments. Polyimide acts as the insulating layer between first and second level aluminum, and increases the lock and key height above the substrate in the double-level design.

The sensor itself has been redesigned to exploit this process and to include several improvements which increase its reliability and versatility. Lock and key height above the ground plane may be selected during fabrication by adjusting the polyimide layer thickness. The transistors have been repositioned for greater matching, with a consequent reduction in the sensor gain offset to ± 0.2 dB. A diode temperature sensor has also been incorporated on the chip to permit in-situ temperature measurements.

Experiments were conducted with device geometries having electrode width to height ratios, W/H , of 5.8, 7.5, 14.7 and 27.8. These sensors were used to monitor the cure reaction of the DGEBA/MPDA resin/amine system. The permittivities and loss factors obtained from these experiments showed good agreement among all devices, and demon-

strated that dielectric properties of materials can be extracted from gain-phase measurements, with of sensor geometry properly taken into account.

Since the calibration curves were calculated by two dimensional simulation, and because the major variable was only the different W/H ratios, it is possible to verify the simulation as able to model electrode systems with arbitrary loss.

When the time dependence of the low frequency conductivity for curing DGEBA/MPDA was compared with published data, it was established that the dielectric properties early in cure were dominated by a bulk, frequency independent conductivity, and that this quantity was being measured by the microdielectrometer. Later in cure, measurements with the sensor revealed dipolar relaxation not visible with DC techniques. Therefore, it has been concluded that the DGEBA/MPDA system undergoes an initial decrease in bulk conductivity until the loss factor has been reduced enough to observe the effects of dipole orientation. Afterwards, the dipolar relaxation times can be seen to increase until the end of cure.

Preliminary tests of the temperature sensor have determined it to be accurate to within 2 °C over at least the range from 20° C to 150° C. Complete calibration,

though, cannot be achieved until additional comparisons are made against an accurate temperature standard.

A parasitic substrate resistance, acting in conjunction with the large body effect of the transistors, was identified as the source of positive phase shift seen at low gains. In addition, smaller positive phase shifts occurring in low frequency, low gain measurements were observed and modeled by stray surface conduction with capacitive coupling from the driven electrodes to the CFT source. A surface phenomenon, this parasitic low frequency phase shift is moisture sensitive and varies with ambient humidity.

The polyimide overglass layer has been identified as the cause of moisture sensitive behavior in the response of the sensor in air. Under conditions of high humidity, the gain-phase points describe a trajectory with negative phase similar to thin film behavior. Sensors made with lock and keys on top of a polyimide layer also demonstrate this trajectory.

A gain offset from the origin of approximately -1 dB has been consistently observed in the cure trajectories of the DGEBA/MPDA system. This effect could not originate from transistor mismatching because sensors with shorted lock and keys show offsets in the range of only ± 0.2 dB. Therefore the offset must be a real phenomenon.

Since the presence of a bulk conductivity has already been established, the cure trajectory should go through the origin, for at high loss or low frequencies the lock and key electrodes are effectively shorted together. Experimental evidence indicates that the -1 dB offset is caused by a blocking layer at the electrode-resin interface, and not by simple dipolar relaxation as modeled by Debye. The Debye equations neglect DC and bulk conduction, and these have been determined to exist in the DGEBA/MPDA system. The capacitance necessary to produce the observed offset requires a blocking layer approximately 450 to 1000 angstroms thick. This value is too large for a native aluminum oxide or residual polyimide layer, but is a reasonable thickness for a space-charge layer. The literature indicates that blocking layers do form in media having high conductivities and free carrier concentrations, and that in such cases the frequency dependence of measured permittivities and loss factors follow the Debye dielectric dispersion equations with a single relaxation time. Consequently, a blocking layer capacitance arising from interfacial effects, such as electrode polarization and discharge, has been proposed to explain the gain offset at the beginning of cure, and the apparent Debye relationship of the cure trajectory.

6.2 Factors Determining Sensor Performance

The results of experiments designed to verify sensor calibration not only showed that dielectric permittivity and loss factor can be extracted from gain-phase data, but also demonstrated that the floating gate CFT sensor can be calibrated on the basis of its physical geometry alone. Knowledge of its W/H ratio, meander length, field permittivity, and transistor gate load capacitance is sufficient to determine sensor response in a semi-infinite medium with an arbitrary permittivity and loss factor.

On an idealized level, then, optimizing sensor design simply involves increasing the lock and key gain by reducing the W/H ratio. A double-level process similar to the one described in Chapter 4 would accomplish this goal. Increased gain, however, has no qualitative advantage other than providing a stronger signal for the data acquisition system. One possible disadvantage of too much gain is decreased resolution in distinguishing progression along the cure trajectory, for the entire trajectory would span a narrower dynamic range than for a device with lower gain. This limitation is imposed by the resolution of the gain-phase meter, which has a precision to only one decimal place in both gain and phase. Another possible disadvantage of greatly increased lock and key gain is decreased resolution

of permittivity at high loss factors. The crowding of permittivity contours near the origin of gain-phase space becomes even more severe under this condition, although uncertainties in the magnitude of gain offsets at the beginning of cure may render suspect all data in this region, regardless.

Sensor performance is not governed solely by idealities, but has a sensitivity to the various parasitic effects described in Chapter 5. In designing an optimized sensor, four distinctive problems must be addressed:

1) The stray conductive path to ground. Positive phase shift at the beginning of cure is the most significant parasitic because it has been seen to be as great as $+45^{\circ}$ and -17 dB from the origin, representing considerable distortion of the cure trajectory. Complete passivation of the chip, leaving only the lock and key exposed, will eliminate this stray path. The design of a chip carrier is pertinent to this issue, and necessitates proper layout of bond pads on the chip to facilitate passivation.

2) The substrate resistance. Positive phase at low gain can be corrected with data processing, but should also be eliminated with symmetrical transistor layout. In this way current flow through the substrate resistance will

modulate the substrate potential and body effect current of both field effect transistors in the same manner.

3) The stray conductance on polyimide overglass layers.

This parasitic appears only under high humidity with chips having polyimide passivation, but can seriously affect thin-film, humidity sensitive applications of the sensor. Not clear is its effect when the sensor is implanted in a bulk sample, although the sample may effectively passivate the device from the ambient. This problem can be avoided entirely by making any overglass cut completely surround the driven gate, with no crossover to provide stray conductive paths to the floating gate.

4) The surface conductance between the driven gate and CFT source. Low frequency positive phase appears to be caused by surface or interface conduction along the top of the sensor chip. Consequently, it may be impossible to eliminate completely. It should be reduced, though, by a layout which increases the length of the resistive path from the driven gate to the CFT source. A sensor with higher gain would have less positive phase of any origin because the quadrature current would be relatively smaller than the in-phase signal.

To enable consistent calibration from the same look-up table, uniformity between devices from the same wafer is highly desirable. An optimized design should reduce the sensor's sensitivity to normal processing variations in gate and field oxide thicknesses. This objective requires a small W/H ratio and an FET gate capacitance which is small compared to the total lock and key capacitance to ground. Absolute variations in insulator thickness beneath the lock and key then cause lesser relative variations in W/H, and uncertainties in gate capacitance only affect an FET that is already small.

Figure 6.1 shows a set of design curves illustrating the relationship between sensor gain in air, and electrode height above the substrate. The electrodes are assumed to be 12.5 microns wide and resting on a silicon dioxide insulator. The curves are parameterized with respect to the load on the floating electrode, expressed as a fraction of the total electrode capacitance to ground. Figure 6.2 shows the design curves relating sensor gain in air to additional load capacitance, parameterized with respect to electrode height above the ground plane.

It is possible to reduce the gate area until it is no longer a substantial influence on the lock and key, but this may decrease transconductance to the point where the transistor cannot drive its cable to the interface

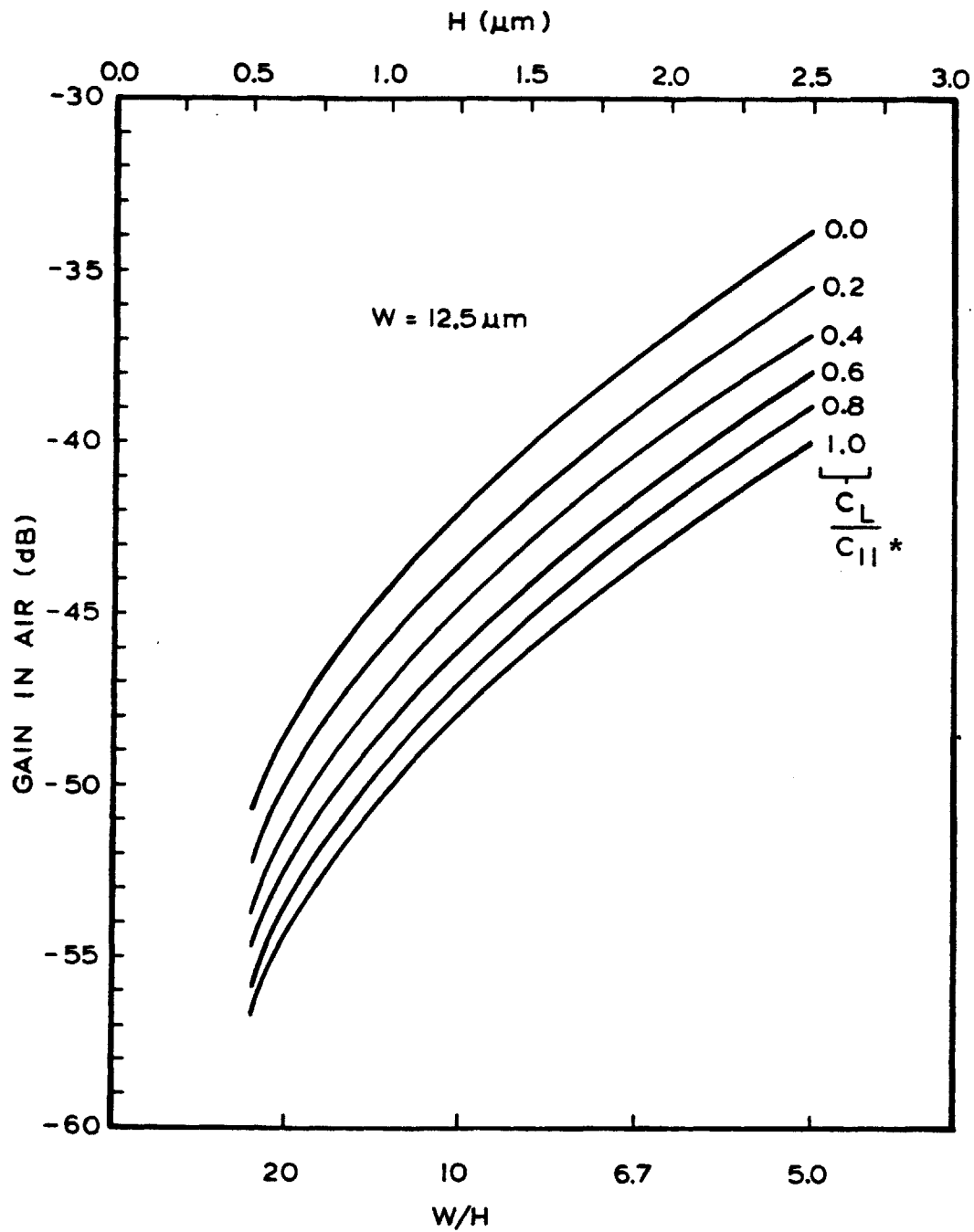


Figure 6.1 Lock and Key Gain in Air versus Electrode Height, Parameterized with Respect to Capacitive Load C_L

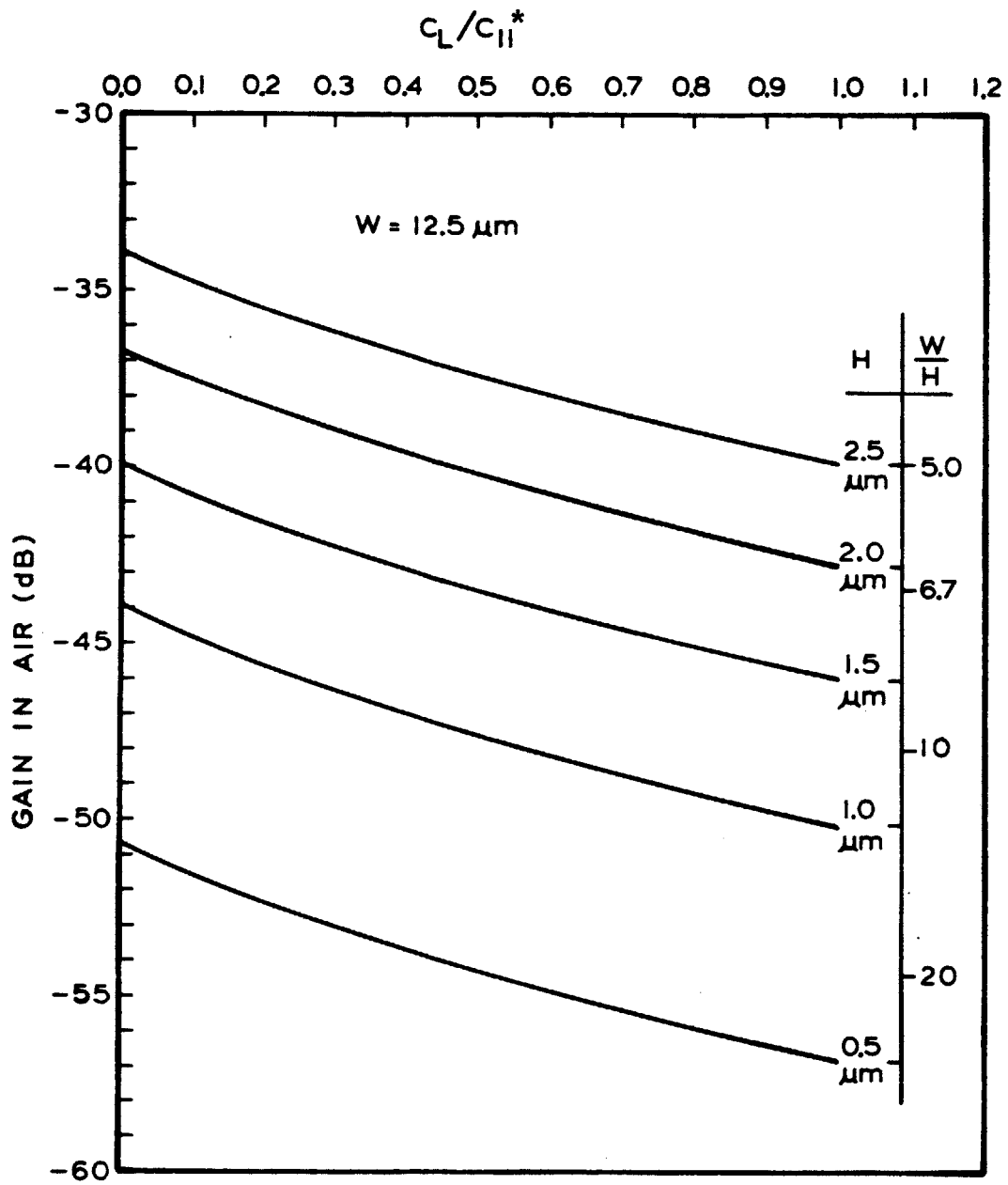


Figure 6.2 Lock and Key Gain in Air versus Capacitive Load, Parameterized with Respect to Electrode Height

circuit. The pole location of the reference FET source node is important for stability in the comparator feedback loop, and should be at a frequency as high as possible for sensor operation without phase shift from the interface circuit. An optimized sensor therefore should have a wide transistor for high transconductance. It then must have a large area lock and key to increase gain toward its intrinsic limit, and decrease sensitivity to the correspondingly larger gate capacitance.

6.3 An Optimized Device Design

An optimized resin cure sensor has been designed with considerations of parasitic elements, device-to-device uniformity and circuit performance. The sensor layout is illustrated in Figure 6.3, and is intended for use with a standard silicon gate NMOS process. The fabrication steps are: 1) n+ diffusion, 2) polysilicon, 3) depletion implant, 4) contact cut, 5) metal and 6) overglass. The specifications for a process will vary from one fabrication line to another, but the typical parameters of Table VIII have been assumed. Of the quantities listed, only the total oxide thickness between metal and substrate will significantly determine sensor gain. A calibration table tailored to the fabricated devices can be generated once the geometry has been measured.

TABLE VIII
TYPICAL NMOS PROCESS PARAMETERS

BV_{DSS}	20 V
K' ($\mu C/2$) Linear Region	10-12 $\mu A/V^2$
γ (Body Effect)	0.7-0.9 $V^{1/2}$
V_{TDO}	-3 to -4 V
Field Threshold V_{TF} (Poly)	15 V
V_{TF} (Metal)	20 V
Diffusion Sheet Resistance	13-30 ohms/square
Polysilicon Sheet Resistance	15-50 ohms/square
Oxide Encroachment	0.8-1.0 micron
Diffusion Junction Depth	1.3 microns
Gate Oxide Thickness	850-900 Å
Field Oxide Thickness (Including Deposited Oxide)	1.4-1.7 microns
Capacitances (10^{-4} pF/ μm^2)	
Gate Oxide	3.6-4.1
Diffusion Junction (Zero Bias)	1.4-1.8
Poly to Substrate	0.43-0.5
Metal to Diffusion	0.3-0.4
Metal to Substrate	0.2-0.25

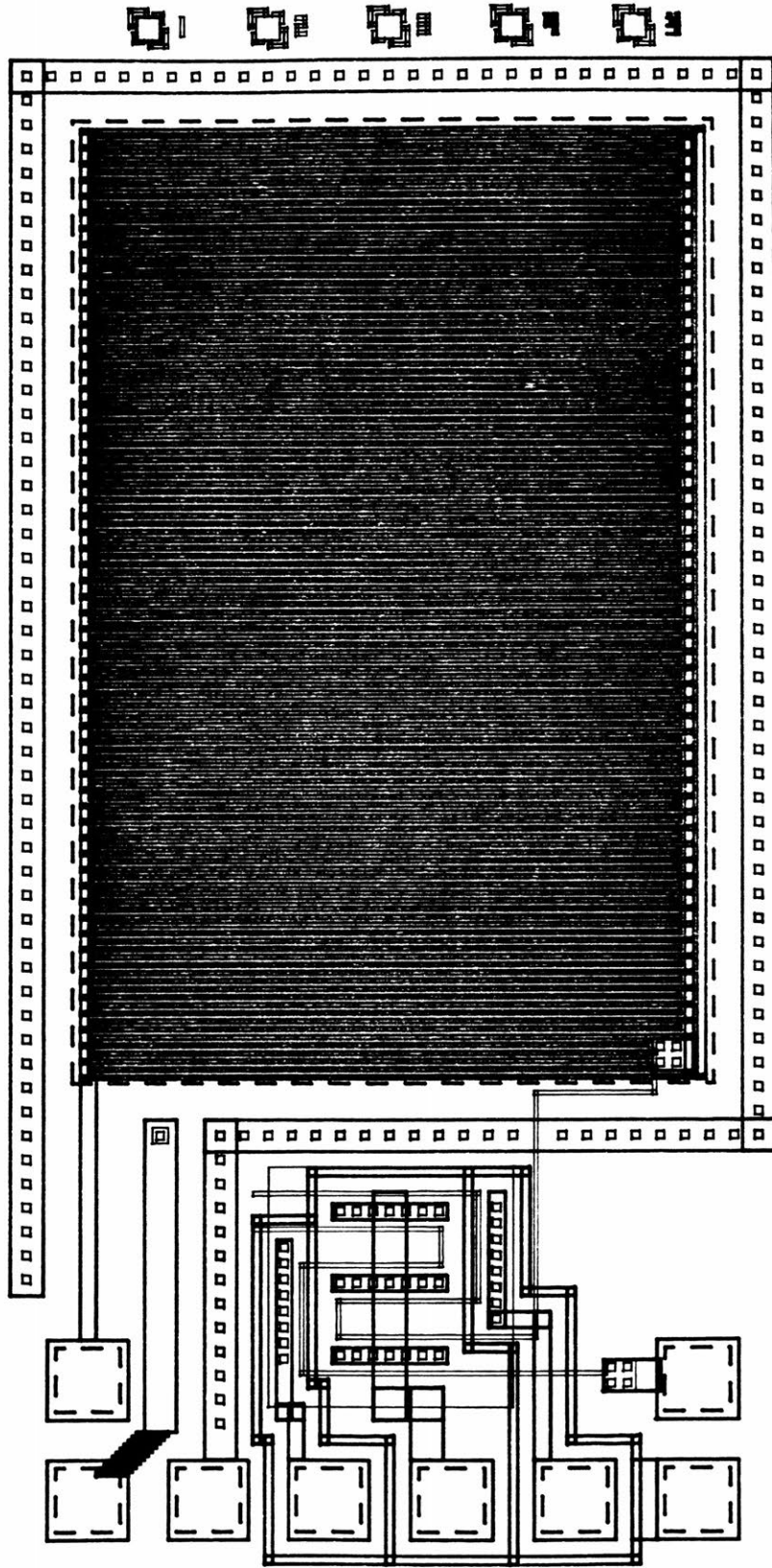


Figure 6.3 Layout of Optimized Sensor Design

The design rules developed by Mead and Conway [52] have been used with a minimum feature size, λ , of 8 microns. Silicon gate NMOS technology was chosen because it allows the fabrication of sensors with readily available techniques. The deposited CVD oxide layer, after polysilicon definition, increases total field oxide thickness beneath the electrodes to a maximum of about 2 microns. Thermally grown oxides, used alone, are limited to about 1 micron. In addition, because the transistor gates lie beneath oxide, they are well passivated and do not require guard rings, enabling more compact configurations. Self-aligned gates greatly reduce overlap capacitances which increase loading of the lock and key, and with only depletion devices on a wafer, the depletion mask step can be eliminated from the process flow.

Use of a diffusion moat mask in NMOS fabrication prevents field implantation of transistor channel regions, consequently producing good field thresholds without large body effects.

The optimized design has the following features:

- 1) A large area lock and key. The FET gate capacitance is only 5% of the electrode capacitance to ground. A variation of 10% in gate capacitance becomes a variation of only 0.05% in the load, and should not detectably affect

sensor gain. As a result, sensor gain is close to the intrinsic value, and one cause of gain uncertainty is eliminated.

2) Wide, serpentine transistors. The common centroid geometry causes first order cancellation of processing variations, threshold and gain mismatches. The positive phase shift due to substrate potential modulation should disappear because the substrates of both the CFT and the reference FET are affected in the same way.

3) Bond pads at one end of the chip. Complete passivation of the sensor is facilitated because the overglass layer exposes only the lock and key, and the bond pads. The pads and bond wires can then be coated with a passivant applied at only one end of the chip, with minimal risk of also coating the lock and key.

4) Distributed substrate contacts. The substrate contacts have been distributed around the lock and key to reduce substrate potential modulation which causes positive phase shift. This modulation is a hazard because the large area lock and key has a correspondingly great capacitive coupling to the ground plane. Collection of the resulting substrate currents is essential for elimination of positive phase.

5) Guard rings. Guard rings have been included to reduce capacitive coupling between the driven gate and the CFT source. To reduce stray capacitance further, the pads themselves have been arranged so cables carrying signals alternate with cables that are AC grounds.

6) Temperature sensor. A diode temperature sensor has been incorporated in the design for in-situ measurements.

6.4 Direction of Future Work

As a result of this thesis, it has been demonstrated that the floating gate CFT sensor can be calibrated solely on the basis of its geometry, that not only the transfer function of the lock and key can be simulated, but also its admittance parameters derived and the effect of an arbitrary load properly weighted and taken into account. Further work should involve fabrication of the optimized design presented, with development of a compatible package. The possible existence of a depletion layer between the electrodes and resin, and its effect on dielectric measurements are also interesting avenues for research. The sensor has potential applications in microprocessor based process control for the cure of resins and graphite-fiber composites. Therefore its usefulness in a heterogeneous medium could be investigated. The preliminary observations

of polyimide moisture sensitivity could be expanded to examine the potential of polyimide humidity sensors, or to study the more fundamental issues of surface conductance on polyimide; the double-level process developed in this thesis is inherently suited for such work.

The generalized finite difference simulation could be applied in the study of different electrode configurations, and may also have use in modeling other lossy systems. It can be modified, for example, to simulate thin-film behavior of the lock and key for moisture or gas sensing. The effect of different film thicknesses could be determined. Also, for more detailed device modeling, the finite thickness of the metal electrodes should be incorporated into any further modifications of the program. Finally, much work remains in the areas of more efficient algorithms and the simulation of nonlinear systems.

APPENDIX A

GENERAL FINITE DIFFERENCE EQUATIONS

I. General Finite Difference Formula for Potential:

$$V_o = \frac{\frac{V_1}{h_1(h_1 + h_4)} + \frac{\frac{\epsilon_2^*}{\epsilon_1^*} V_2}{h_2 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)} + \frac{V_3}{h_3(h_1 + h_3)} + \frac{V_4}{h_4 \left(\frac{\epsilon_2^*}{\epsilon_1^*} h_2 + h_4 \right)}}{\frac{1}{h_1 h_3} + \frac{1}{h_2 h_4} \left(\frac{\frac{\epsilon_2^*}{\epsilon_1^*} h_4 + h_2}{h_4 + \frac{\epsilon_2^*}{\epsilon_1^*} h_2} \right)}$$

II. X and Y Components of Electric Field:

$$E_{x0} = -\frac{1}{2} \left(\frac{V_1 - V_o}{h_1} + \frac{V_3 - V_o}{h_3} \right)$$

$$E_{y0} = -\frac{1}{2} \left(\frac{V_4 - V_o}{h_4} + \frac{V_2 - V_o}{h_2} \right)$$

III. Interface Charge:

$$Q_I = - \left[\frac{V_1 - V_o}{h_1} \left(\frac{\epsilon_1' h_4 + \epsilon_2' h_2}{2} \right) + \frac{V_2 - V_o}{h_2} \left(\epsilon_2' \left(\frac{h_1 + h_3}{2} \right) \right) \right. \\ \left. + \frac{V_3 - V_o}{h_3} \left(\frac{\epsilon_1' h_4 + \epsilon_2' h_2}{2} \right) + \frac{V_4 - V_o}{h_4} \left(\epsilon_1' \left(\frac{h_1 + h_3}{2} \right) \right) \right]$$

APPENDIX B

SUPREM SIMULATION OF DEVICE FABRICATION

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***

```
1....TITLE      *****MODEL OF FIELD REGION FOR 0.75 UM CFT*****
2....GRID       DYSI=0.01, DPTH=2.0, YMAX=4.0
3....SUBS       ORNT=100, ELEM=B, CONC=1E15
4....MODEL      NAME=SPM1, GATE=AL, QSSQ=1.0E11, CBLK=0
5....MODEL      NAME=WET1, LRTE=3.6E6, LREA=2.18, PRTE=17.62, PREA=.96, PRES=1
6....COMM       *****THIN OXIDE GROWTH*****
7....STEP       TYPE=OXID, TIME=15, TEMP=1100, MODL=DRYO
8....COMM       *****BORON FIELD IMPLANT*****
9....STEP       TYPE=IMPL, ELEM=B, DOSE=1.5E13, AKEV=190
10....COMM      *****DRIVE-IN WITH NEUTRAL AMBIENT*****
11....STEP      TYPE=OXID, TIME=70, TEMP=1100, MODL=NITO
12....COMM      *****FIELD OXIDE GROWTH*****
13....STEP      TYPE=OXID, TIME=120, TEMP=1100, MODL=WET1
14....STEP      TYPE=OXID, TIME=10, TEMP=1100, MODL=DRYO
15....STEP      TYPE=OXID, TIME=20, TEMP=1000, MODL=WET1
16....STEP      TYPE=OXID, TIME=40, TEMP=1100, MODL=DRYO
17....PRINT     HEAD=Y
18....PLOT      TOTL=Y, CMIN=14, NDEC=7, WIND=2
19....STEP      TYPE=OXID, TIME=10, TEMP=1100, MODL=NITO, MODL=SPM1
20....END
```


*****MODEL OF FIELD REGION FOR 0.75 UM CFT*****
 STEP Δ 8

NEUTRAL AMBIENT DRIVE-IN

TOTAL STEP TIME = 10.0 MINUTES
 INITIAL TEMPERATURE = 1100.00 DEGREES C.
 OXIDE THICKNESS = .7740 MICRONS

	± OXIDE	± SILICON	±	± SURFACE	±
	± DIFFUSION	± DIFFUSION	± SEGREGATION	± TRANSPORT	
	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	±
BORON	± 2.09720E-07	± 8.90330E-04	± .66145	± 1.31132E-02	±

SURFACE CONCENTRATION = 6.140980E+16 ATOMS/CM³

GATE MATERIAL = ALUMINUM SILICON UNDER GATE = P - TYPE
 OXIDE THICKNESS = 7739.9 ANG. CAPACITANCE/AREA = 4.46E-05 PF/UM²
 INTERFACE CHARGES = 1.00E+11 CM-2 INTF CHARGE VOLT. = -.4E+01 VOLTS
 FLATBAND VOLTAGE = -4.541 VOLTS
 /VSB/ 0.00 .50 1.00 1.50 2.00 3.00 4.00 5.00 6.00 7.00 10.00 15.00
 VTHR 22.97 31.40 38.18 44.01 49.22 58.39 66.39 73.57 80.16 86.27 102.57 125.24
 XDPL .13 .16 .19 .22 .24 .28 .32 .35 .38 .41 .48 .58

JUNCTION DEPTH	±	SHEET RESISTANCE
	±	1987.47 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE = 7.318580E+12 IS 47.4 % OF TOTAL
 SILICON CHARGE = 8.099610E+12 IS 52.5 % OF TOTAL
 TOTAL CHARGE = 1.541820E+13 IS 100. % OF INITIAL
 INITIAL CHARGE = 1.541820E+13

CHEMICAL CONCENTRATION OF BORON

OXIDE CHARGE = 7.318580E+12 IS 47.4 % OF TOTAL
 SILICON CHARGE = 8.099610E+12 IS 52.5 % OF TOTAL
 TOTAL CHARGE = 1.541820E+13 IS 100. % OF INITIAL
 INITIAL CHARGE = 1.541820E+13

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***

```
1....TITLE      *****MODEL OF CHANNEL REGION FOR 0.75 UM CFT*****
2....GRID      DYSI=0.01, DPTH=1.0, YMAX=2.0
3....SUBS      ORNT=100, ELEM=B, CONC=1E15
4....MODEL      NAME=SPM1, GATE=AL, QSSQ=1.0E11, CBLK=0
5....MODEL      NAME=WET1, LRTE=3.6E6, LREA=2.18, PRTE=17.62, PREA=.96, PRES=1
6....COMM      *****THIN OXIDE GROWTH*****
7....STEP      TYPE=OXID, TIME=15, TEMP=1100, MODL=DRYO
8....COMM      *****BORON FIELD IMPLANT*****
9....STEP      TYPE=IMPL, ELEM=B, DOSE=1.5E13, AKEV=190
10....COMM      *****DRIVE-IN WITH NEUTRAL AMBIENT*****
11....STEP      TYPE=OXID, TIME=70, TEMP=1100, MODL=NITO
12....COMM      *****FIELD OXIDE GROWTH*****
13....STEP      TYPE=OXID, TIME=120, TEMP=1100, MODL=WET1
14....STEP      TYPE=OXID, TIME=10, TEMP=1100, MODL=DRYO
15....STEP      TYPE=OXID, TIME=20, TEMP=1100, MODL=WET1
16....STEP      TYPE=ETCH, TEMP=100
17....COMM      *****GATE OXIDE GROWTH*****
18....STEP      TYPE=OXID, TIME=40, TEMP=1100, MODL=DRYO
19....STEP      TYPE=OXID, TIME=10, TEMP=1100, MODL=NITO
20....STEP      TYPE=IMPL, DOSE=2.5E12, AKEV=90, ELEM=P
21....PRINT      HEAD=Y
22....PLOT      TOTL=Y, CMIN=14, NDEC=7, WIND=0.5, IDIV=Y
23....STEP      TYPE=OXID, TIME=20, TEMP=950, MODL=NITO, MODL=SPM1
24....END
```

*****MODEL OF CHANNEL REGION FOR 0.75 UM CFT*****
 STEP Δ 11

NEUTRAL AMBIENT DRIVE-IN

TOTAL STEP TIME = 20.0 MINUTES
 INITIAL TEMPERATURE = 950.000 DEGREES C.
 OXIDE THICKNESS = 8.4553E-02 MICRONS.

	± OXIDE	± SILICON	±	± SURFACE	±
	± DIFFUSION	± DIFFUSION	± SEGREGATION	± TRANSPORT	
	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	±
BORON	± 5.40472E-09	± 2.55660E-05	± .24457	± 1.00231E-03	±
PHOSPHORUS	± 1.72790E-07	± 1.91820E-05	± 10.000	± 5.68350E-03	±

SURFACE CONCENTRATION = -2.285452E+17 ATOMS/CM_{p3}

GATE MATERIAL = ALUMINUM SILICON UNDER GATE = N - TYPE
 OXIDE THICKNESS = 845.5 ANG. CAPACITANCE/AREA = 4.08E-04 PF/UM2
 INTERFACE CHARGES = 1.00E+11 CM-2 INTF CHARGE VOLT. = -.4E+00 VOLTS
 FLATBAND VOLTAGE = -1.425 VOLTS

/VSB/	0.00	.50	1.00	1.50	2.00	3.00	4.00	5.00	6.00	7.00	10.00	15.00
VTHR	-3.71	-2.97	-2.36	-1.84	-1.37	-.56	.16	.82	1.44	2.02	3.60	5.84
XDPL	.22	.25	.27	.29	.31	.35	.38	.41	.44	.46	.53	.63

JUNCTION DEPTH	±	SHEET RESISTANCE
9.956040E-02 MICRONS	±	8771.76 OHMS/SQUARE
	±	2434.84 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE = 5.382710E+11	IS	6.44	% OF TOTAL
SILICON CHARGE = 7.808752E+12	IS	93.5	% OF TOTAL
TOTAL CHARGE = 8.347023E+12	IS	99.5	% OF INITIAL
INITIAL CHARGE = 8.380714E+12			

CHEMICAL CONCENTRATION OF BORON

OXIDE CHARGE = 5.322504E+11	IS	6.85	% OF TOTAL
SILICON CHARGE = 7.227730E+12	IS	93.1	% OF TOTAL
TOTAL CHARGE = 7.759980E+12	IS	100.	% OF INITIAL
INITIAL CHARGE = 7.760010E+12			

CHEMICAL CONCENTRATION OF PHOSPHORUS

OXIDE CHARGE = 6.905844E+11	IS	27.6	% OF TOTAL
SILICON CHARGE = 1.809800E+12	IS	72.3	% OF TOTAL
TOTAL CHARGE = 2.500381E+12	IS	99.9	% OF INITIAL
INITIAL CHARGE = 2.500850E+12			

*****MODEL OF CHANNEL REGION FOR 0.75 UM CFT*****

DEPTH (UM) ± ± ± ± ± ± ± ±

DEPTH (UM)	14	15	16	17	18	19	20	21
-.08	*							
	±	±	± *	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	± *	±	±	±	±	±
	±	±	± *	±	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
0.00				*	*			
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	± *	±	± *	±	±	±	±
	±	±	± *	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
.20				*				
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
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	±	±	±	± *	±	±	±	±
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.40				*				
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.60				*				
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	±	±	±	± *	±	±	±	±
	±	±	±	± *	±	±	±	±
.80				*				

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***

```
1....TITLE      *****MODEL OF FIELD REGION FOR 0.45 UM CFT*****
2....GRID      DYSI=0.01, DPTH=2.0, YMAX=4.0
3....SUBS      ORNT=100, ELEM=B, CONC=1E15
4....MODEL      NAME=SPM1, GATE=AL, QSSQ=1.0E11, CBLK=0
5....MODEL      NAME=WET1,LRTE=3.6E6,LREA=2.18,PRTE=17.62,PREA=.96,PRES=1
6....COMM      *****THIN OXIDE GROWTH*****
7....STEP      TYPE=OXID, TIME=15, TEMP=1100, MODL=DRYO
8....COMM      *****BORON FIELD IMPLANT*****
9....STEP      TYPE=IMPL, ELEM=B, DOSE=1.5E13, AKEV=190
10....COMM     *****DRIVE-IN WITH NEUTRAL AMBIENT*****
11....STEP     TYPE=OXID, TIME=70, TEMP=1100, MODL=NITO
12....COMM     *****FIELD OXIDE GROWTH*****
13....STEP     TYPE=OXID, TIME=30, TEMP=1100, MODL=WET1
14....STEP     TYPE=OXID, TIME=10, TEMP=1100, MODL=DRYO
15....STEP     TYPE=OXID, TIME=20, TEMP=1000, MODL=WET1
16....STEP     TYPE=OXID, TIME=40, TEMP=1100, MODL=DRYO
17....PRINT    HEAD=Y
18....PLOT     TOTL=Y, CMIN=14, NDEC=7, WIND=2
19....STEP     TYPE=OXID, TIME=10, TEMP=1100, MODL=NITO, MODL=SPM1
20....END
```

*****MODEL OF FIELD REGION FOR 0.45 UM CFT*****
 STEP A 8

NEUTRAL AMBIENT DRIVE-IN

TOTAL STEP TIME = 10.0 MINUTES
 INITIAL TEMPERATURE = 1100.00 DEGREES C.
 OXIDE THICKNESS = .4157 MICRONS

	± OXIDE	± SILICON	±	± SURFACE	±
	± DIFFUSION	± DIFFUSION	± SEGREGATION	± TRANSPORT	
	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	± COEFFICIENT	±
BORON	± 2.09720E-07	± 8.90330E-04	± .66145	± 1.31132E-02	±

SURFACE CONCENTRATION = 9.831750E+16 ATOMS/CM²

GATE MATERIAL = ALUMINUM SILICON UNDER GATE = P - TYPE
 OXIDE THICKNESS = 4157.4 ANG. CAPACITANCE/AREA = 8.30E-05 PF/UM²
 INTERFACE CHARGES = 1.00E+11 CM-2 INTF CHARGE VOLT. = -.2E+01 VOLTS
 FLATBAND VOLTAGE = -2.878 VOLTS

/VSB/	0.00	.50	1.00	1.50	2.00	3.00	4.00	5.00	6.00	7.00	10.00	15.00
VTHR	16.19	21.85	26.44	30.37	30.20	40.05	45.46	50.33	54.79	58.93	70.00	85.42
XDPL	.10	.13	.15	.18	.19	.23	.25	.28	.30	.32	.38	.46

JUNCTION DEPTH	±	SHEET RESISTANCE
	±	1580.44 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE =	4.342204E+12	IS	28.1	% OF TOTAL
SILICON CHARGE =	1.109621E+13	IS	71.8	% OF TOTAL
TOTAL CHARGE =	1.543841E+13	IS	100.	% OF INITIAL
INITIAL CHARGE =	1.543840E+13			

CHEMICAL CONCENTRATION OF BORON

OXIDE CHARGE =	4.342204E+12	IS	28.1	% OF TOTAL
SILICON CHARGE =	1.109621E+13	IS	71.8	% OF TOTAL
TOTAL CHARGE =	1.543841E+13	IS	100.	% OF INITIAL
INITIAL CHARGE =	1.543840E+13			

*****MODEL OF FIELD REGION FOR 0.45 UM CFT*****
 CONCENTRATION (LOG ATOMS/CC)

DEPTH (UM)	14	15	16	17	18	19	20	21
-.42	*			*				
	±	±	±	±*	±	±	±	±
	±	±	±	±*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	±*	±	±	±	±
	±	±	±	±*	±	±	±	±
0.00				*				
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	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
.50				*				
	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
1.00				*				
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
1.50				*				
	±	±	±*	±	±	±	±	±
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	±	±	*	±	±	±	±	±
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	±	±	*	±	±	±	±	±
	±	±	*	±	±	±	±	±
2.00			*	±	±	±	±	±

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***

```
1....TITLE      *****MODEL OF CHANNEL REGION FOR 0.45 UM CFT*****
2....GRID      DYSI=0.01, DPTH=1.0, YMAX=2.0
3....SUBS      ORNT=100, ELEM=B, CONC=1E15
4....MODEL     NAME=SPM1, GATE=AL, QSSQ=1.0E11, CBLK=0
5....MODEL     NAME=WET1, LRTE=3.6E6, LREA=2.18, PRTE=17.62, PREA=.96, PRES=1
6....COMM      *****THIN OXIDE GROWTH*****
7....STEP      TYPE=OXID, TIME=15, TEMP=1100, MODL=DRYO
8....COMM      *****BORON FIELD IMPLANT*****
9....STEP      TYPE=IMPL, ELEM=B, DOSE=1.5E13, AKEV=190
10....COMM     *****DRIVE-IN WITH NEUTRAL AMBIENT*****
11....STEP     TYPE=OXID, TIME=70, TEMP=1100, MODL=NITO
12....COMM     *****FIELD OXIDE GROWTH*****
13....STEP     TYPE=OXID, TIME=30, TEMP=1100, MODL=WET1
14....STEP     TYPE=OXID, TIME=10, TEMP=1100, MODL=DRYO
15....STEP     TYPE=OXID, TIME=20, TEMP=1100, MODL=WET1
16....STEP     TYPE=ETCH, TEMP=100
17....COMM     *****GATE OXIDE GROWTH*****
18....STEP     TYPE=OXID, TIME=40, TEMP=1100, MODL=DRYO
19....STEP     TYPE=OXID, TIME=10, TEMP=1100, MODL=NITO
20....STEP     TYPE=IMPL, DOSE=2.5E12, AKEV=90, ELEM=P
21....PRINT    HEAD=Y
22....PLOT     TOTL=Y, CMIN=14, NDEC=7, WIND=0.5
23....STEP     TYPE=OXID, TIME=20, TEMP=950, MODL=NITO, MODL=SPM1
24....END
```

*****MODEL OF CHANNEL REGION FOR 0.45 UM CFT*****
 STEP Δ 11

NEUTRAL AMBIENT DRIVE-IN

TOTAL STEP TIME = 20.0 MINUTES
 INITIAL TEMPERATURE = 950.000 DEGREES C.
 OXIDE THICKNESS = 8.4553E-02 MICRONS

	± OXIDE ± DIFFUSION ± COEFFICIENT	± SILICON ± DIFFUSION ± COEFFICIENT	± ± ±	± SEGREGATION ± COEFFICIENT	± SURFACE ± TRANSPORT ± COEFFICIENT	±
BORON	± 5.40472E-09	± 2.55660E-05	±	.24457	± 1.00231E-03	±
PHOSPHORUS	± 1.72790E-07	± 1.91820E-05	±	10.000	± 5.68350E-03	±

SURFACE CONCENTRATION = -2.055003E+17 ATOMS/CM³

GATE MATERIAL = ALUMINUM SILICON UNDER GATE = N - TYPE
 OXIDE THICKNESS = 845.5 ANG. CAPACITANCE/AREA = 4.08E-04 PF/UM²
 INTERFACE CHARGES = 1.00E+11 CM-2 INTF CHARGE VOLT. = -.4E+00 VOLTS
 FLATBAND VOLTAGE = -1.406 VOLTS
 /VSB/ 0.00 .50 1.00 1.50 2.00 3.00 4.00 5.00 6.00 7.00 10.00 15.00
 VTHR -2.36 -1.55 -.89 -.31 -.39 1.20 2.09 2.91 3.68 4.40 6.36 9.15
 XDPL .18 .20 .22 .24 .25 .28 .31 .33 .35 .37 .43 .51

JUNCTION DEPTH	±	SHEET RESISTANCE
8.420850E-02 MICRONS	±	10843.4 OHMS/SQUARE
	±	1938.85 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE = 5.954602E+11 IS 5.74 % OF TOTAL
 SILICON CHARGE = 9.773110E+12 IS 94.2 % OF TOTAL
 TOTAL CHARGE = 1.036860E+13 IS 100. % OF INITIAL
 INITIAL CHARGE = 1.036714E+13

CHEMICAL CONCENTRATION OF BORON

OXIDE CHARGE = 8.434370E+11 IS 7.99 % OF TOTAL
 SILICON CHARGE = 9.701260E+12 IS 92.0 % OF TOTAL
 TOTAL CHARGE = 1.054470E+13 IS 99.9 % OF INITIAL
 INITIAL CHARGE = 1.054474E+13

CHEMICAL CONCENTRATION OF PHOSPHORUS

OXIDE CHARGE = 6.905844E+11 IS 27.6 % OF TOTAL
 SILICON CHARGE = 1.809800E+12 IS 72.3 % OF TOTAL
 TOTAL CHARGE = 2.500381E+12 IS 99.9 % OF INITIAL
 INITIAL CHARGE = 2.500850E+12

*****MODEL OF CHANNEL REGION FOR 0.45 UM CFT*****

DEPTH (UM) ± ± ± ± ± ± ± ±

DEPTH (UM)	14	15	16	17	18	19	20	21
-.08	*			*				
	±	±	±	±	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
0.00				*				
	±	±	±	±	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
.20				*				
	±	±	±	±	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
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.40				*				
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
.60				*				
	±	±	±	±	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
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	±	±	±	*	±	±	±	±
	±	±	±	*	±	±	±	±
.80				*				

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***

```
1....TITLE      *****MODEL OF ARSENIC DOPED SOURCE-DRAIN REGION*****
2....GRID      DYSI=0.01, DPTH=2.0, YMAX=4.0
3....SUBS      ORNT=100, ELEM=B, CONC=1E15
4....MODEL     NAME=WET1,LRTE=3.6E6,LREA=2.18,PRTE=17.62,PREA=.96,PRES=1
5....COMM      *****THIN OXIDE GROWTH*****
6....STEP     TYPE=OXID, TIME=15, TEMP=1100, MODL=DRYO
7....COMM      *****BORON FIELD IMPLANT*****
8....STEP     TYPE=IMPL, ELEM=B, DOSE=1.5E13, AKEV=190
9....COMM      *****DRIVE-IN WITH NEUTRAL AMBIENT*****
10....STEP    TYPE=OXID, TIME=70, TEMP=1100, MODL=NITO
11....COMM    *****FIELD OXIDE GROWTH*****
12....STEP    TYPE=OXID, TIME=120, TEMP=1100, MODL=WET1
13....STEP    TYPE=OXID, TIME=10, TEMP=1100, MODL=DRYO
14....STEP    TYPE=ETCH, TEMP=100
15....COMM    *****SOURCE-DRAIN ARSENIC IMPLANT*****
16....STEP    TYPE=IMPL, ELEM=AS, DOSE=8E15, AKEV=100
17....COMM    *****OXIDE GROWTH*****
18....STEP    TYPE=OXID, TIME=20, TEMP=1000, MODL=WET1
19....STEP    TYPE=OXID, TIME=40, TEMP=1100, MODL=DRYO
20....PRINT   HEAD=Y
21....PLOT    TOTL=Y, CMIN=14, NDEC=7, WIND=2
22....STEP    TYPE=OXID, TIME=10, TEMP=1100, MODL=NITO
23....END
```

*****MODEL OF ARSENIC DOPED SOURCE-DRAIN REGION*****
 STEP Δ 10

NEUTRAL AMBIENT DRIVE-IN

TOTAL STEP TIME = 10.0 MINUTES
 INITIAL TEMPERATURE = 1100.00 DEGREES C.
 OXIDE THICKNESS = .2508 MICRONS

	± OXIDE ± DIFFUSION ± COEFFICIENT	± SILICON ± DIFFUSION ± COEFFICIENT	± SEGREGATION ± COEFFICIENT	± SURFACE ± TRANSPORT ± COEFFICIENT
BORON	± 2.09720E-07	± 8.90330E-04	± .66145	± 1.31132E-02
ARSENIC	± 1.18401E-08	± 1.22584E-04	± 10.000	± 4.47011E-02

SURFACE CONCENTRATION = -1.217672E+20 ATOMS/CM³

JUNCTION DEPTH	±	SHEET RESISTANCE
.863824 MICRONS	±	15.4903 OHMS/SQUARE
	±	6390.24 OHMS/SQUARE

NET ACTIVE CONCENTRATION

OXIDE CHARGE = 2.315500E+15	IS	28.4	% OF TOTAL
SILICON CHARGE = 5.820000E+15	IS	71.5	% OF TOTAL
TOTAL CHARGE = 8.135500E+15	IS	100.	% OF INITIAL
INITIAL CHARGE = 8.113143E+15			

CHEMICAL CONCENTRATION OF BORON

OXIDE CHARGE = 9.790570E+11	IS	11.6	% OF TOTAL
SILICON CHARGE = 7.447820E+12	IS	88.3	% OF TOTAL
TOTAL CHARGE = 8.426871E+12	IS	99.9	% OF INITIAL
INITIAL CHARGE = 8.427112E+12			

CHEMICAL CONCENTRATION OF ARSENIC

OXIDE CHARGE = 2.316480E+15	IS	28.1	% OF TOTAL
SILICON CHARGE = 5.910103E+15	IS	71.8	% OF TOTAL
TOTAL CHARGE = 8.226580E+15	IS	99.9	% OF INITIAL
INITIAL CHARGE = 8.226640E+15			

*****MODEL OF ARSENIC DOPED SOURCE-DRAIN REGION*****
 CONCENTRATION (LOG ATOMS/CC)

DEPTH (UM)	14	15	16	17	18	19	20	21
-.25	*				*			
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
0.00						*	*	
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
.50							*	*
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
1.00								
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
1.50								
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
2.00								
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±
	±	±	±	±	±	±	±	±

APPENDIX C

DETAILED MASK LAYOUT OF EXPERIMENTAL CHIP

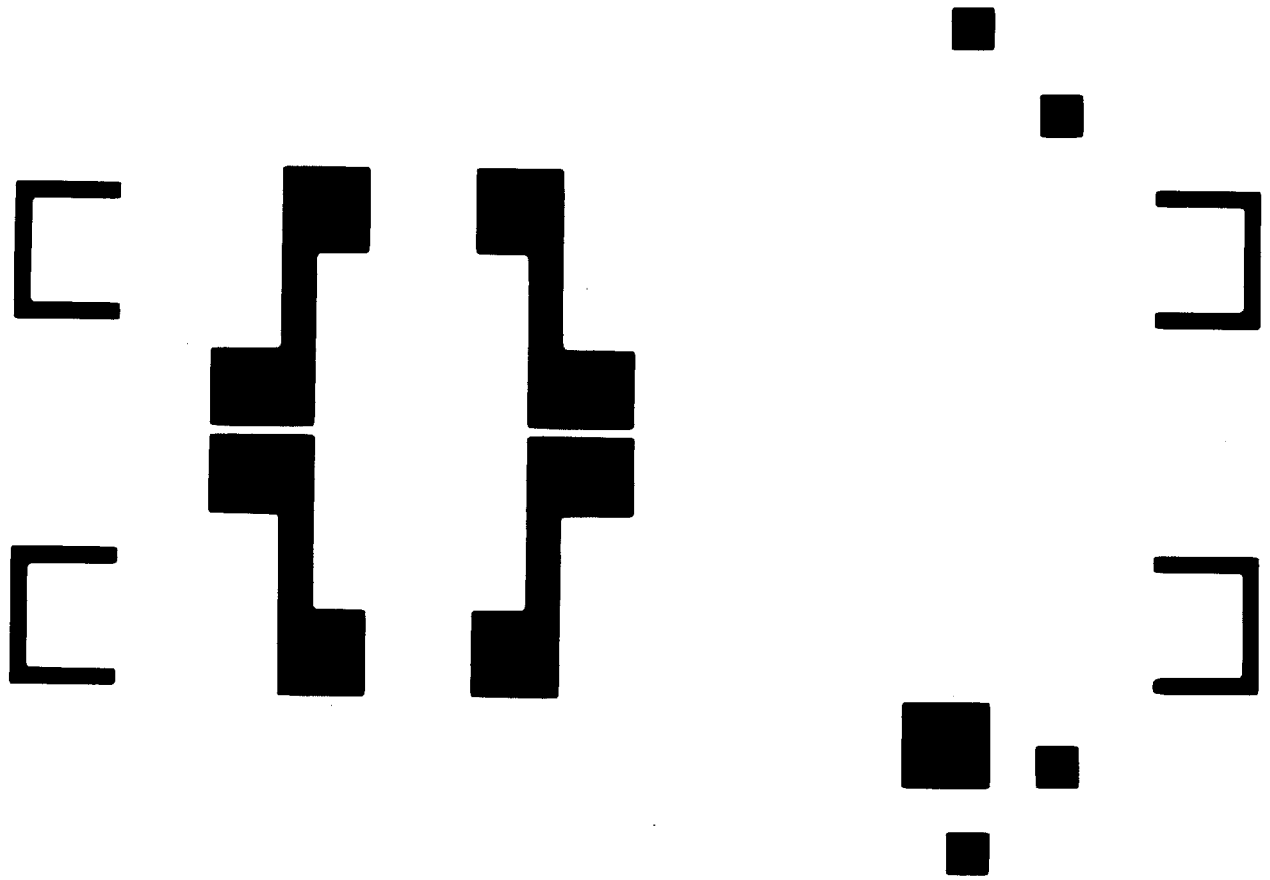


Figure C.1 Source-Drain Mask (Mask 1) Approximately 90 X

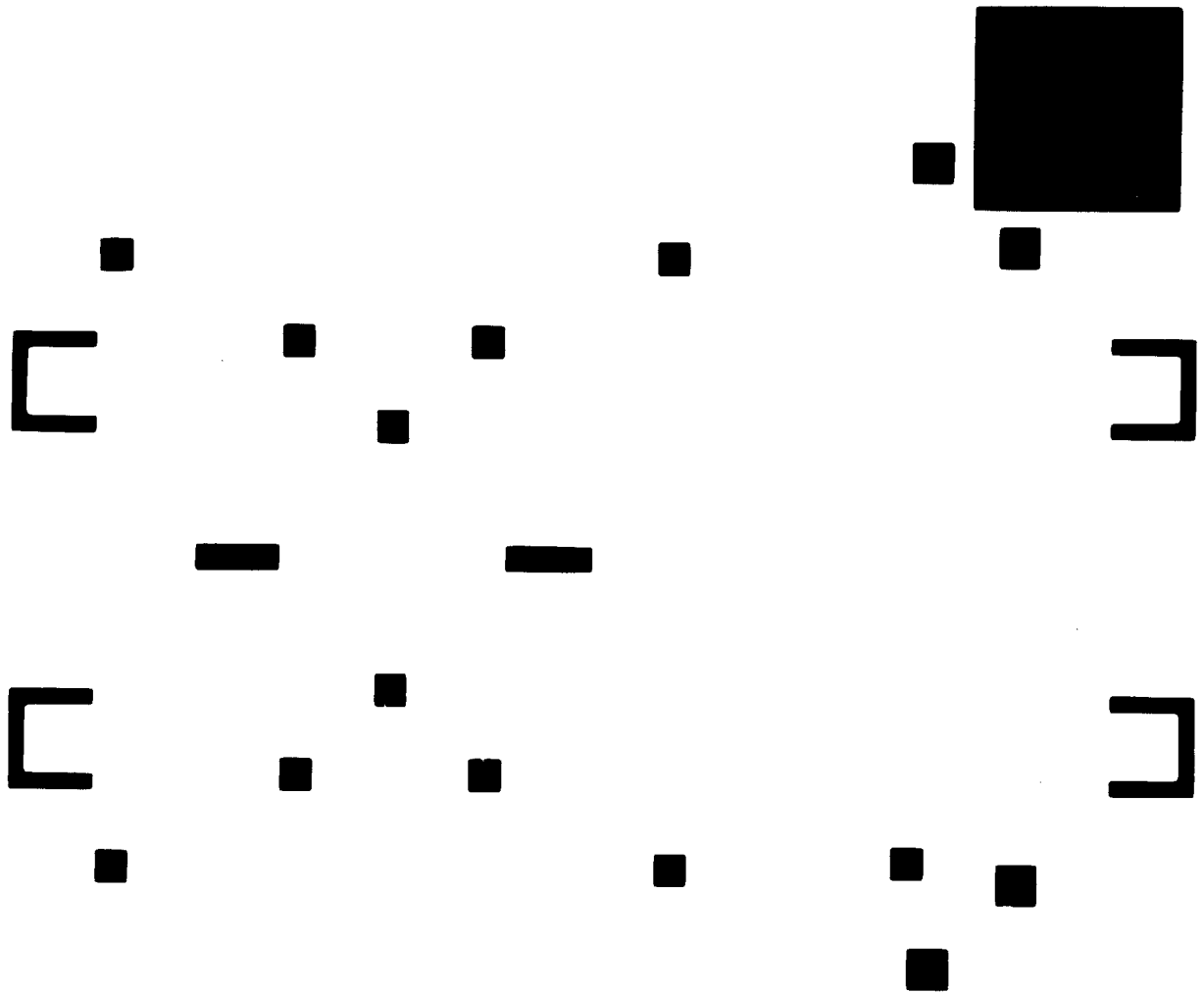


Figure C.2 Thin Oxide Mask (Mask 2) Approximately 90 X

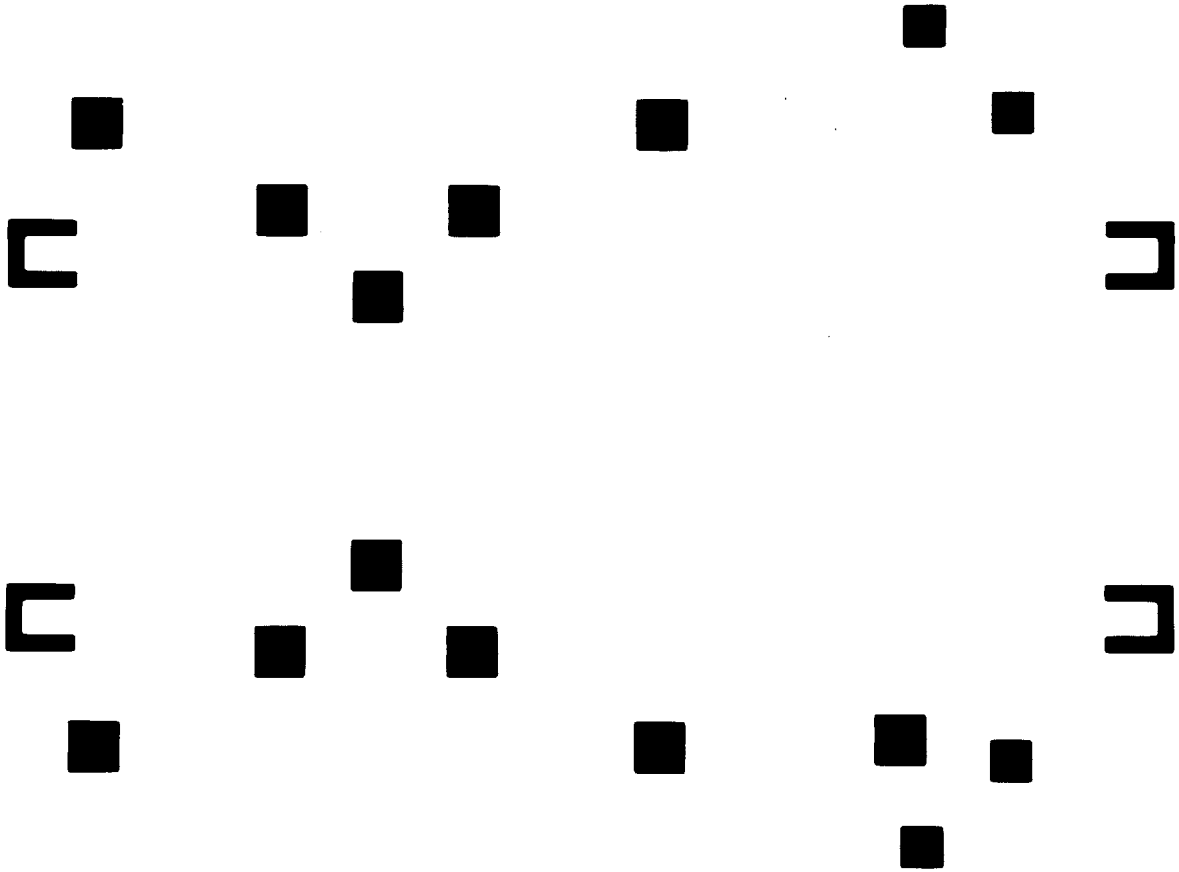


Figure C.3 Contact Cut Mask (Mask 3) Approximately 90 X

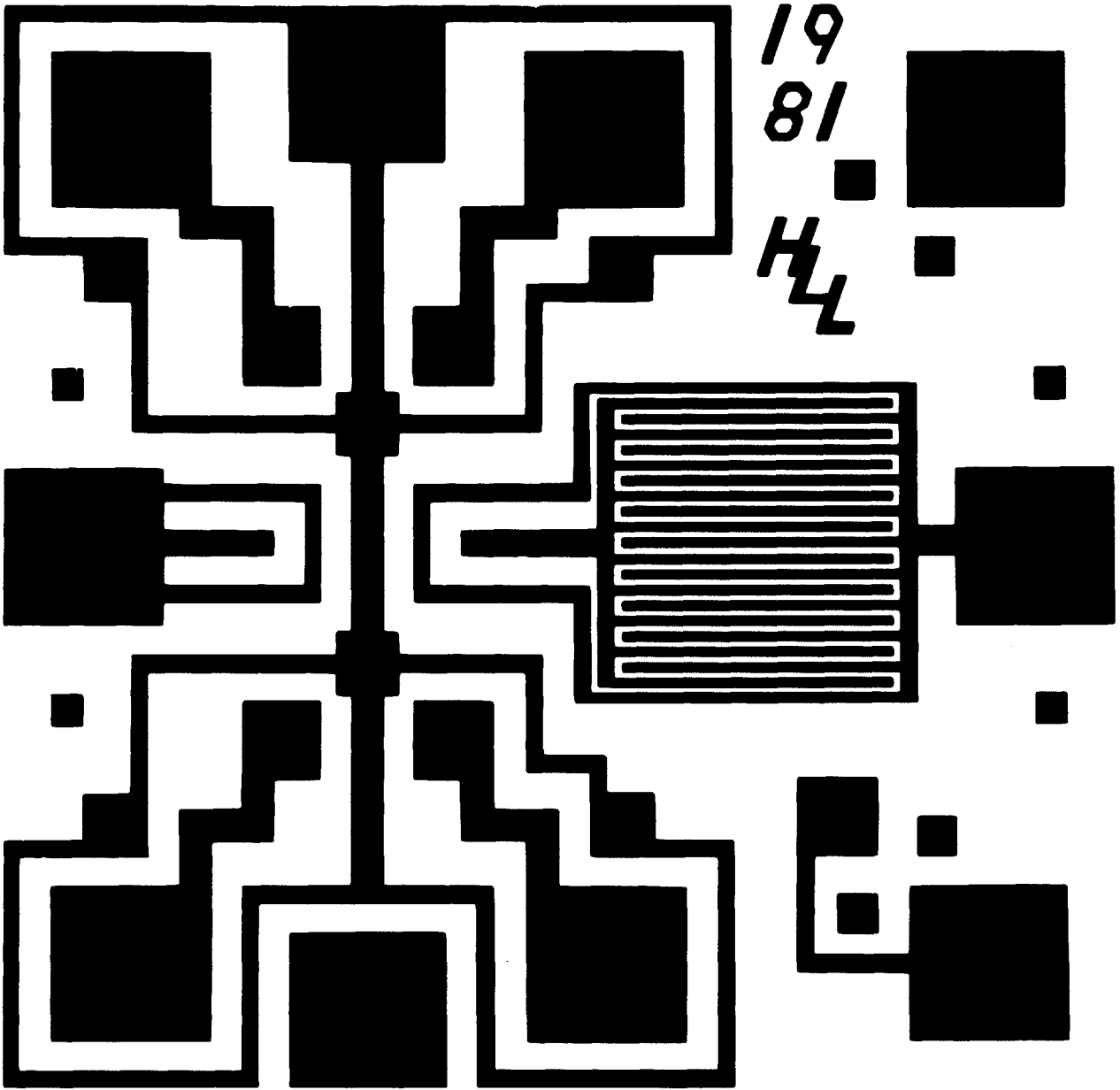


Figure C.4 Metal Mask, Single-level Metal Design (Mask 4A)
Approximately 90 X

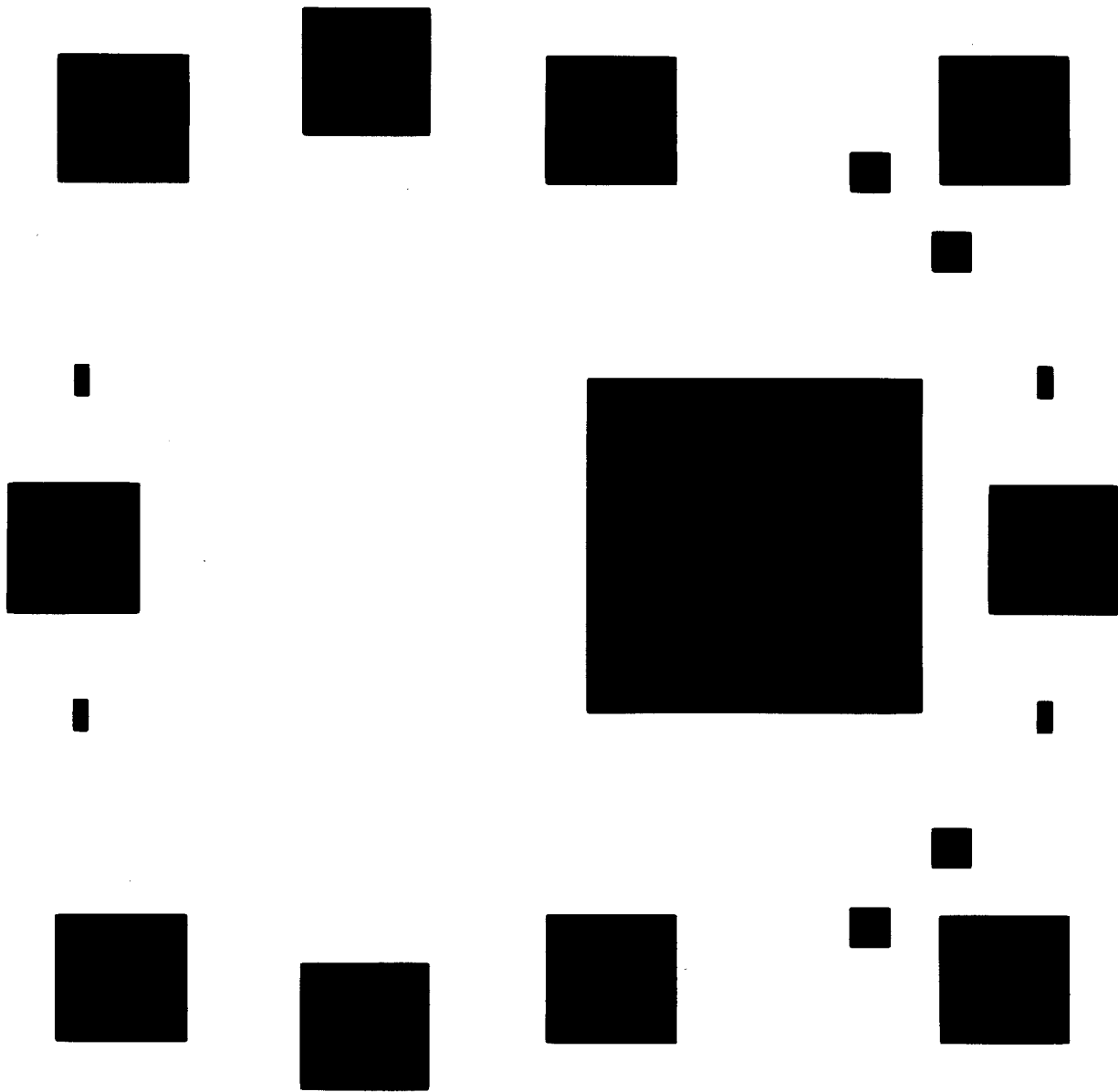


Figure C.5 Passivation Mask, Single-level Metal Design (Mask 5A)
Approximately 90 X (Actual Mask has Opposite Polarity)

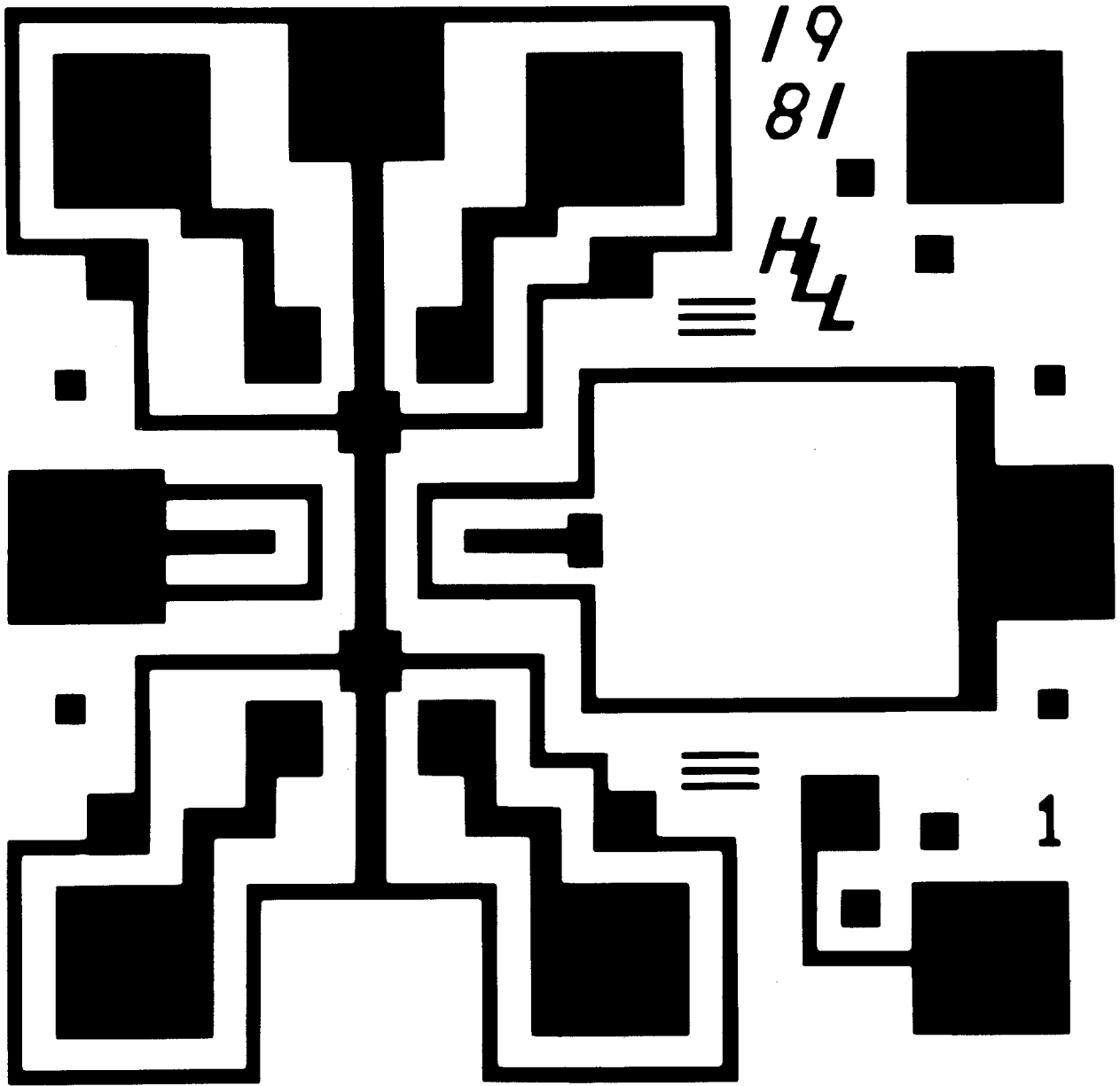


Figure C.6 First-level Metal Mask, Double-level Metal Design
(Mask 4B Metal 1) Approximately 90 X

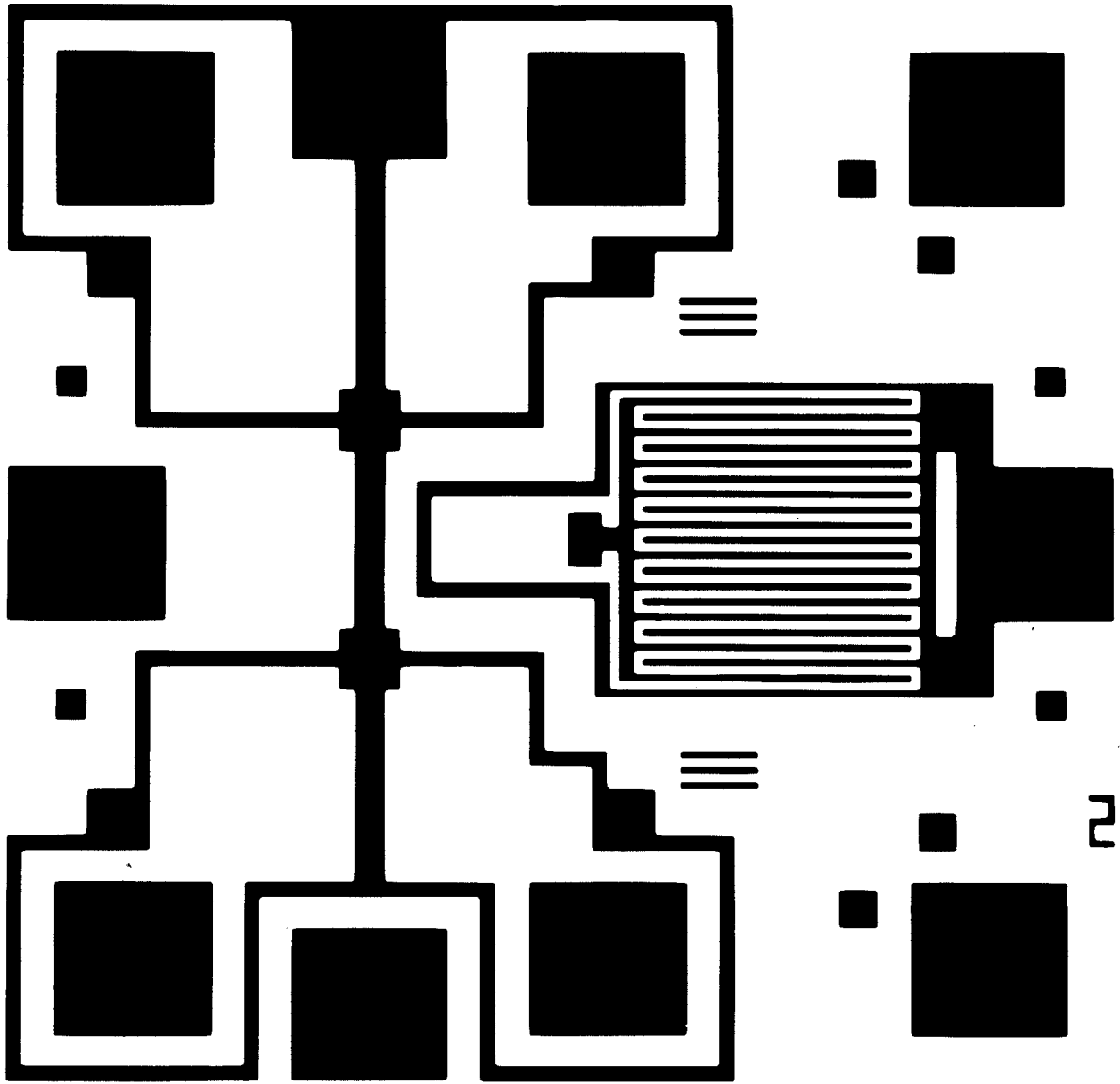


Figure C.7 Second-level Metal Mask, Double-level Metal Design
(Mask 4B Metal 2) Approximately 90 X

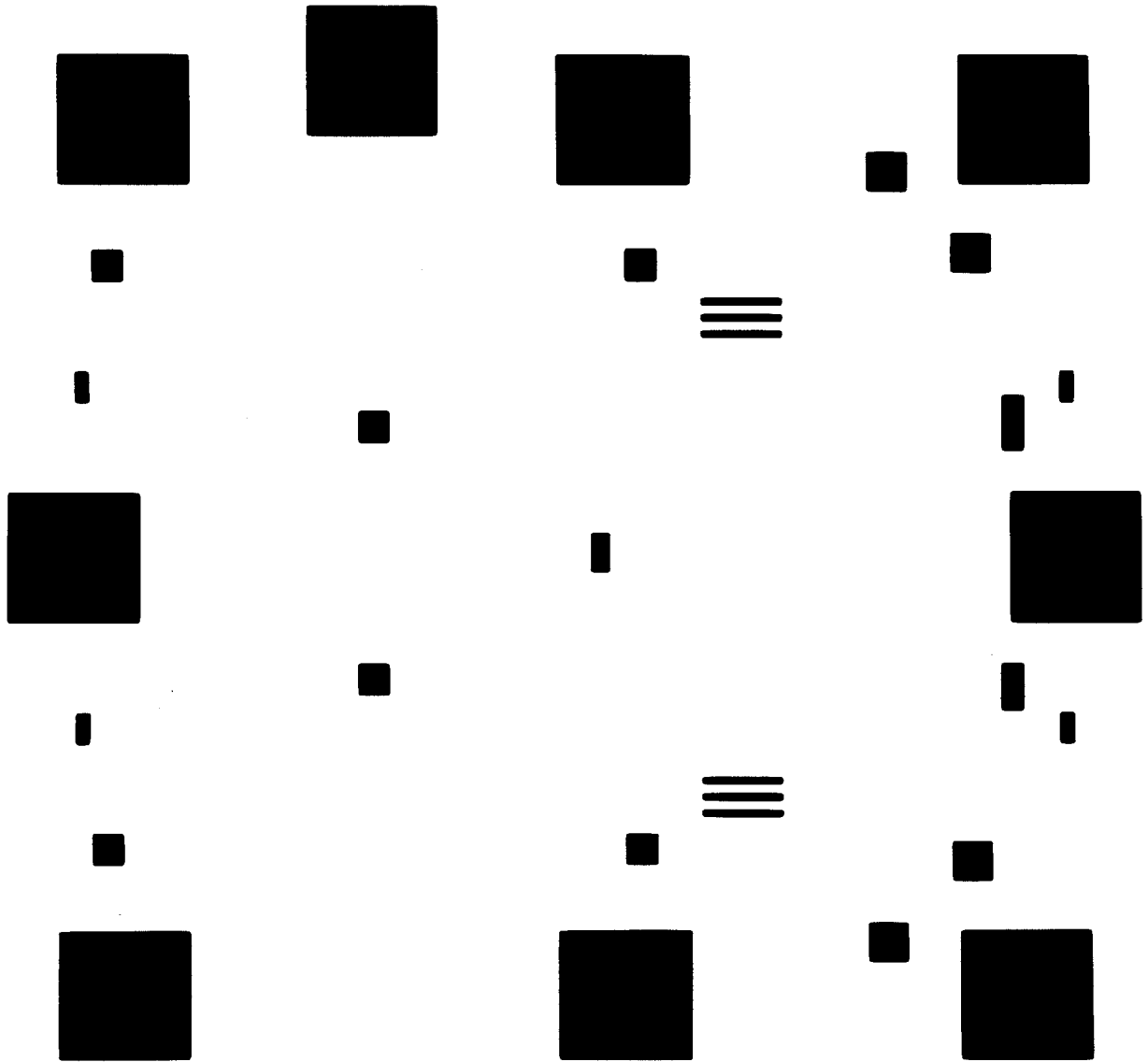


Figure C.8 Via and Passivation Mask, Double-level Metal Design
(Mask 5B Passivation) Approximately 90 X (Actual
Mask has Opposite Polarity

APPENDIX D

POLYIMIDE FILM THICKNESS VS. SPIN SPEED

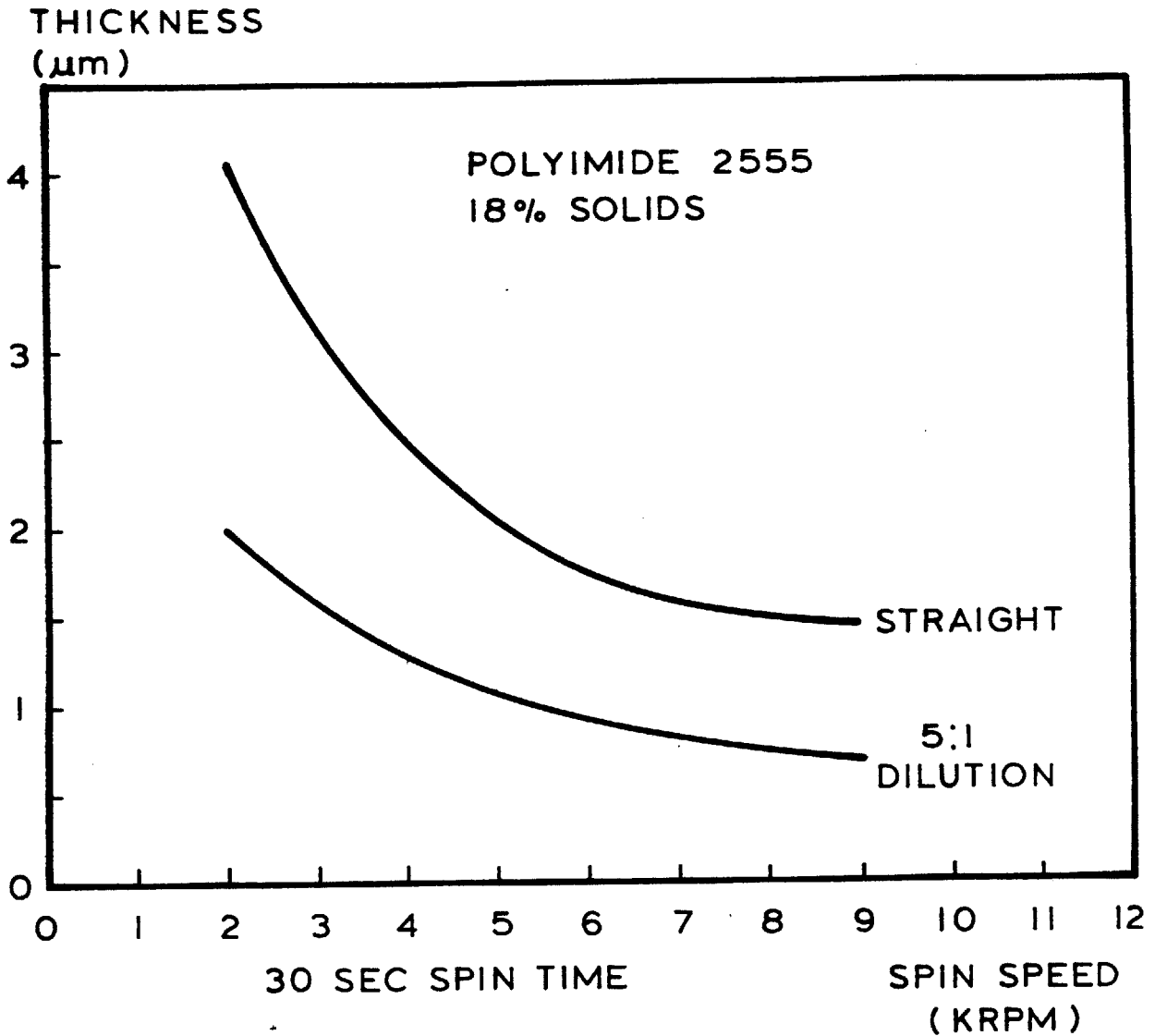


Figure D.1 Thickness of Cured Polyimide 2555 versus Spin Speed

APPENDIX E

FABRICATION PROCEDURE FOR EXPERIMENTAL CHIP

- b. Air dry 15 min
 - c. Pre-bake 30 min 90 °C
 - d. Expose 15 sec on Cobilt aligner with Thin Oxide mask
 - e. Develop 1 min with KTFER developer, dry
 - f. Post-bake 30 min 180 °C
 - g. Etch About 8 min--check after 6--in buffered HF, rinse
 - h. Strip in hot A-20 for 5 min, rinse, blow dry
9. Gate Oxide Growth
- a. RCA clean
 - b. Dry O2 40 min 1100 °C
 - c. N2 10 min 1100 °C
10. Channel Implant Photolithography
- a. Spin on Shipley B positive resist 15 sec 3000 RPM
 - b. Pre-bake 2.5 min 90 °C
 - c. Repeat steps 10 a. and 10 b.
 - d. Expose 15 sec on Cobilt aligner with Contact mask
 - e. Develop 25 sec with Shipley B developer, rinse
 - f. Post-bake 30 min 180 °C
11. Channel Implant
- a. Species: Phosphorus
 - b. Dose: 2.5 E12
 - c. Energy: 90 Kev
12. Channel Implant Anneal
- a. Strip resist in hot A-20 for 5 min, rinse, blow dry
 - b. RCA clean
 - c. N2 20 min 1000 °C
13. Contact Photolithography
- a. Spin on Kodak 747 negative resist 15 sec 6000 RPM
 - b. Air dry 15 min
 - c. Pre-bake 20 min 90 °C
 - d. Expose 15 sec on Cobilt aligner with Contact mask
 - e. Develop 1 min with KTFER developer, blow dry
 - f. Post-bake 30 min 180 °C
 - g. Etch About 2 or 3 min in Buffered HF, rinse
 - h. Strip in hot A-20 for 5 min, rinse, blow dry
14. Aluminum Deposition--use E-beam evaporator
15. Metallization Photolithography
- a. Spin on Shipley J positive resist 20 sec 6000 RPM

- b. Air dry 15 min
- c. Pre-bake 20 min 90 °C
- d. Expose 15 sec on Cobilt aligner with Metal mask
- e. Develop 20 sec with Shipley J developer, rinse
- f. Etch In PAN etch, rinse
- g. Strip resist with acetone

(Use of Metal Mask 4A will produce the single-level CFT)

(Use of Metal Mask 4B 1 will produce the first-level of the double-level CFT)

16. Aluminum Sinter

- a. Rinse in RT2 10 min 90 °C
- b. Alloy in Forming Gas 20 min 400 °C

17. Polyimide Application and Photolithography

- a. Rinse
 - i. Trico 5 min 90 °C
 - ii. Methanol 5 min 90 °C
- b. Spin on surface promoter 10 sec 3000 RPM
- c. Spin on polyimide 30 sec--See Appendix D for spin speeds
- d. Bake 40 min 90 °C
- e. Spin on Shipley J positive resist 30 sec 6000 RPM
- f. Air dry 15 min
- g. Pre-bake 20 min 90 °C
- h. Expose 15 sec on Cobilt aligner with Passivation mask
- i. Develop 20 sec with Shipley J developer
- j. Strip resist with acetone

(Use of Passivation Mask 5A will produce the overglass for the single-level CFT)

(Use of Passivation Mask 5B will produce the overglass and vias for the double-level CFT)

18. PI Cure

- a. 30 min 200 °C
- b. Ramp 8 °C/min to 390 °C
- c. 60 min 390 °C

Fabrication of the single-level CFT ends here.

Fabrication of the double-level CFT continues.

19. Via Treatment

- a. Rinse in acetic acid 1 min
- b. Rinse in DI H2O 1 min

- c. Plasma Etch 50 mTorr 60 sec
- d. Rinse in Buffered HF 10 sec

20. Second-level Aluminum Deposition--Same as Step 14

21. Second-level Metal Patterning--Same as Step 15

22. Aluminum Sinter

a. Rinse

- i. Trico 5 min 90 °C
 - ii. Acetone 5 min 90 °C
 - iii. DI H2O 5 min, blow dry
- b. Alloy in N2 15 min 400 °C, leave in end of tube
an additional 5 min before removing.

APPENDIX F

DETAILED MASK LAYOUT FOR OPTIMIZED SENSOR DESIGN

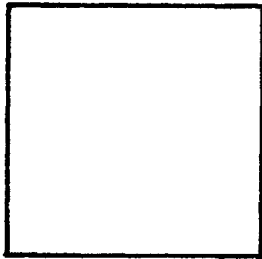


Figure F.1 Diffusion Mask for Optimized Sensor Design

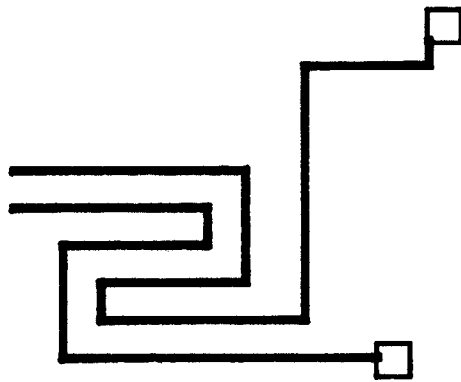


Figure F.2 Polysilicon Mask for Optimized Sensor Design

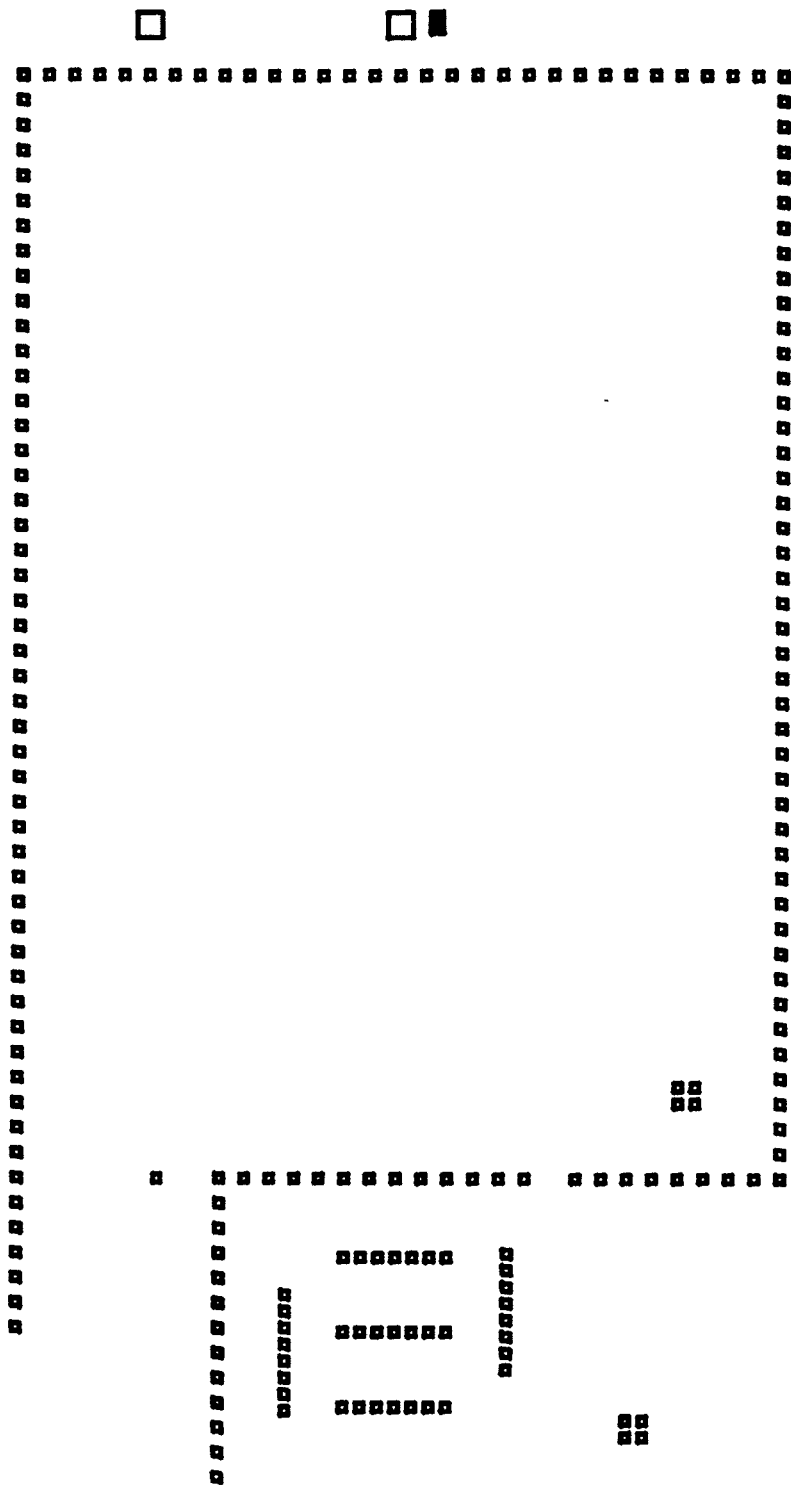


Figure F.3 Contact Mask for Optimized Sensor Design

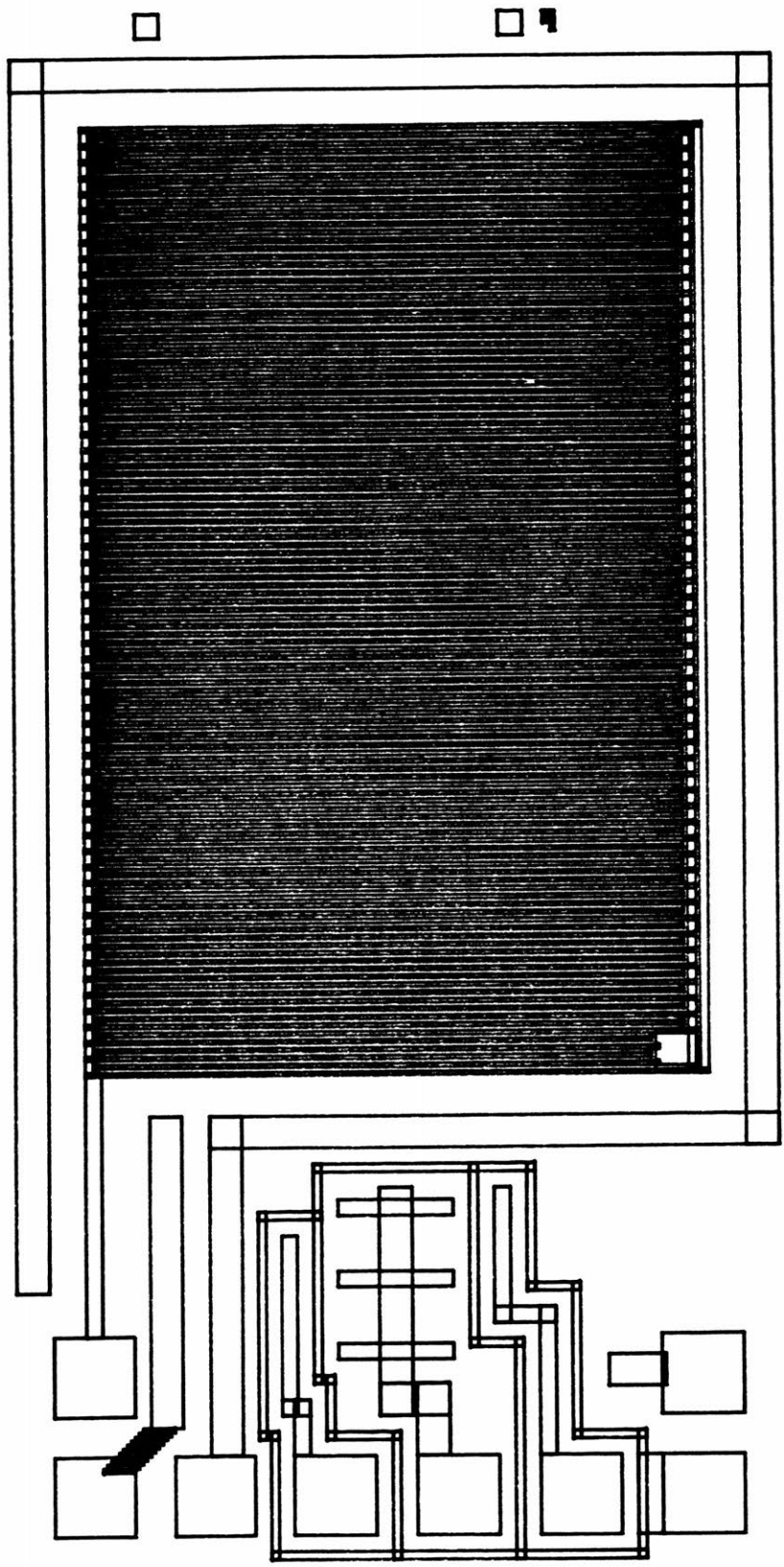


Figure F.4 Metal Mask for Optimized Sensor Design

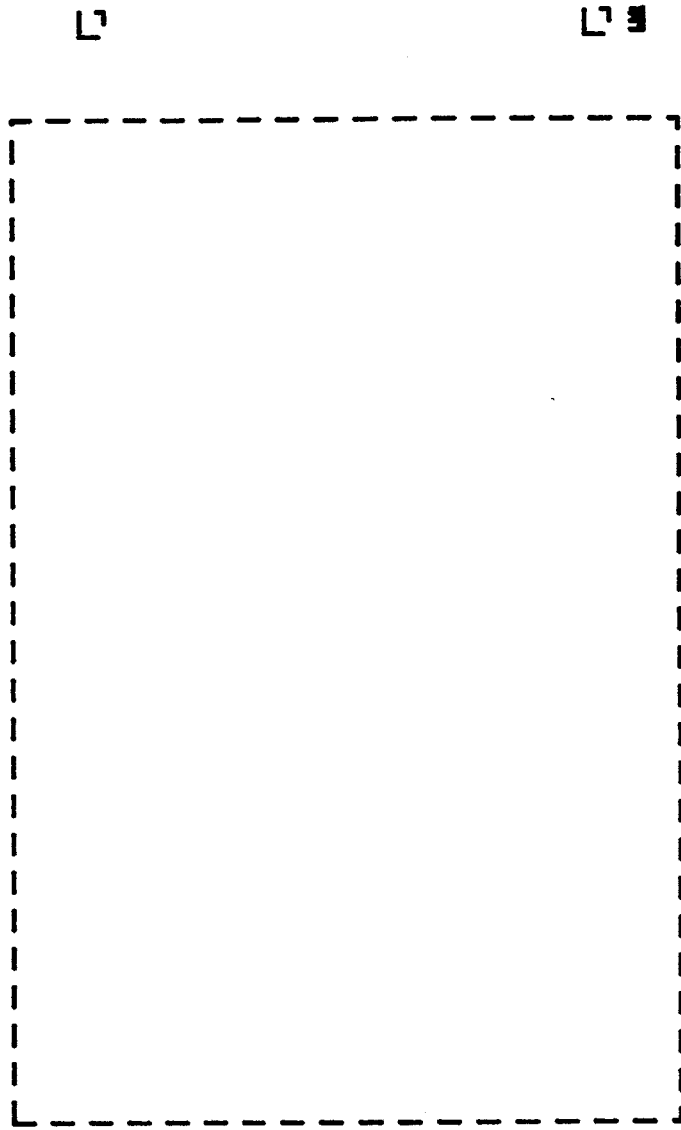


Figure F.5 Passivation Mask for Optimized Sensor Design

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