Low Voltage, Low Power CMOS Operational Amplifier Design for Switched Capacitor Circuits

by

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B.S., Georgia Institute of Technology (1996)

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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Abstract

The increasing demand for circuits with low voltage operation and low power consumption is being driven by smaller submicron technologies and the increasing market for portable, battery-operated electronic systems. These goals present many circuit design challenges, particularly in the analog domain. This thesis presents the design and implementation of a high performance 1.8V CMOS operational amplifier with <100μW power consumption and large signal-to-noise ratio for use in switched capacitor circuits. Key features include a fully differential two-stage topology with cascoded first stage to boost gain, a replica tail design to provide constant tail current, and a common mode feedback circuit to set output common mode voltage.

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Title: Professor of Electrical Engineering

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CHAPTER 1

Introduction

The increasing demand for circuits with low voltage operation and low power consumption is being driven by smaller submicron technologies and the exploding market for portable, battery-operated electronic systems [1, 2]. Smaller geometries require lower supply voltages to prevent a high electric field which can cause device breakdown and degrade reliability. Feature scaling also results in a lower allowable power dissipation per device in order to maintain constant power consumption per unit area as device densities increase. For portable electronic systems low voltage is desirable since it translates to fewer batteries which minimizes size and weight. However, low power consumption is also needed in these applications to ensure reasonable battery lifetime.

This demand for low voltage supply and low power consumption presents challenges in circuit design, particularly in the analog domain. In analog circuit design, operational amplifiers are the core building blocks and often are the primary bottleneck in circuit performance. Unlike digital circuits where power consumption reduces proportional to the square of the supply voltage, in operational amplifiers lower voltage actually increases power consumption [3] when performance is held constant. Another opamp design challenge that arises under low voltage operation is lower transistor drive availability, which decreases device speed. Reduced dynamic range is yet another problem [4] since the supply voltage is reduced while the noise floor remains unchanged for same sized capacitor values.

While one possible solution to low voltage, low power analog circuit operation is use of low threshold voltage mosfets, these devices have drawbacks. Although low Vt transistors reduce some disadvantages introduced by low power supplies [5], the decrease in channel doping causes subthreshold current leakage during the normally off state, which degrades circuit performance [6]. Also, low threshold transistors have higher output conductance which translates to lower gain. Finally, the multiple mask requirement when integrating with standard Vt devices becomes expensive.

Thus, the goal of this research is to tackle these challenges and design a high performance low voltage and low power operational amplifier using a standard CMOS process.

1.1 Thesis Objective

The objective of this research is to design a low voltage, low power CMOS operational amplifier with high performance for use in medium to low frequency switched capacitor circuits such as filters and A/D converters. The key criteria for the project is to operate within +/- 0.9V power supply and achieve large signal-to-noise ratio while maintaining ≤100μW power consumption, ≤100ns settling time, and reasonable gain. Table 1-1 shows the full detailed specifications. The opamp drives a capacitive load of 200fF. This thesis presents the amplifier circuit that has been designed, simulated and fabricated on a chip.

Performance Parameter	Design Goal
Swing (>20% inc. gain)	close to rails
Total Power	< 100μW
0.1% Settling Time	< 100ns
Slew Rate	> 12V/μs
Gain (DC)	> 10K (80dB)
Phase Margin	> 60°
Unity Gain Frequency	> 15MHz
CMRR	max
PSRR +	max
PSRR -	max
Input Referred Offset	< 10mV
Input Referred Noise	64.5 nV/$\sqrt{Hz}$

Table 1-1: Opamp Design Specifications

1.2 Thesis Motivation

Improvements in processing have pushed scaling of device dimensions persistently over the past years and as shown in Figure 1-1 [7], this pattern is expected to continue in the future. The main drive behind this trend is the resulting reduction in IC production cost since more components on a chip are possible. While smaller geometries have other benefits such as lower parasitic capacitances and increased transconductance which yields higher speed, these devices are subject to reliability problems unless voltage is scaled as well. Scaling lengths, widths, and other dimensions alone result in high field effects such as hot carrier degradation and lower breakdown values. Therefore, voltage supply must decrease as transistor dimensions decrease. Figure 1-2 [7] depicts this reduction of voltage supply over the last few years and its continuing trend predicted for the future.

In addition to device scaling, the increasing portable electronics market is also encouraging low voltage and low power circuitry since this would reduce battery size and weight and enable longer battery lifetime.

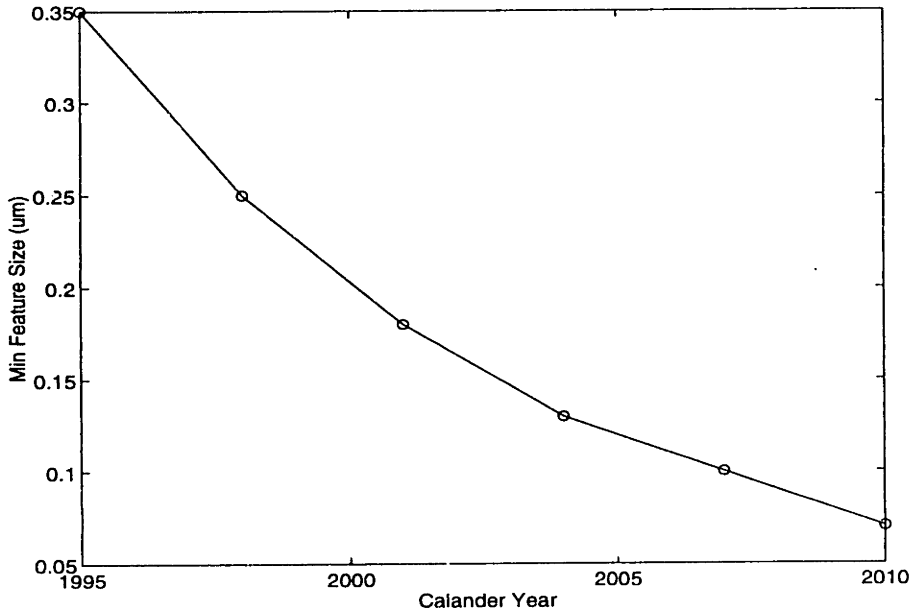


Figure 1-1: MOS Device Dimension Scaling Trends [7]

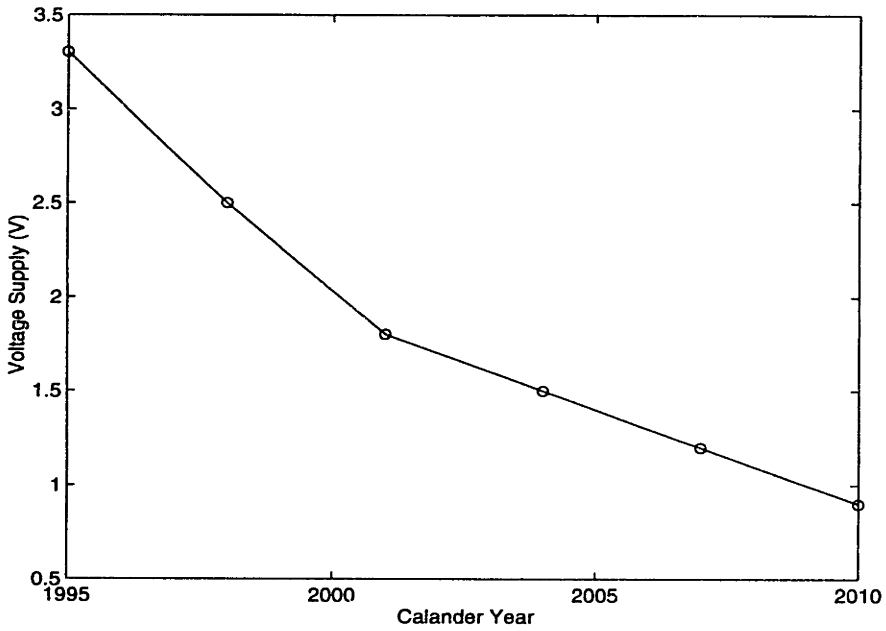


Figure 1-2: Voltage Supply Trends [7]

In the digital domain, the continual reduction in supply voltage is beneficial since it is an effective way to reduce power consumption. Decrease in voltage translates to decrease in power, leading to an optimum energy-delay product [8]. In analog circuits, however, power consumption increases when voltage is decreased. This is because power consumption at a given temperature is determined by the signal-to-noise ratio (SNR) at a given frequency. Assuming the fundamental thermal noise limit, Equation 1.1 shows that decreasing voltage supply directly reduces output swing, which reduces the SNR.

$$SNR \propto \frac{swing}{\sqrt{\frac{kT}{C}}} \tag{1.1}$$

If SNR given in Equation 1.1 and settling time given in Equation 1.2 are held constant, it is evident that more current would be needed to get the same performance, which results in increased power consumption.

$$\tau_s \propto \frac{C}{g_m} \propto \frac{C(V_{GS}-V_T)}{I} \tag{1.2}$$

The primary motivation for this thesis, therefore, arises from the high demand and challenge of designing a high performance low voltage and low power analog circuit, particularly operational amplifiers. This research focuses on switched capacitor applications since it is an analog CMOS circuit technique for sampled-data applications which yields good results in low and medium frequency applications [4].

The specifications for the high performance low voltage, low power opamp given in Table 1-1 were chosen so that the amplifier would be useful for general A/D converter and filter applications [9]. The voltage supplies were based on the Nickel Cadium (NiCd) battery system since it remains to be the mainstay of small secondary batteries [10]. Specifically, +/-0.9V supplies were used because the NiCd battery decays down to 0.9V at the end of its lifetime [11]. Thus the opamp would function even when the battery cells reach the end of their lifetime. The 200fF capacitive load was chosen as a reasonable starting point. Note that this value can be increased, however, other specifications would have to change because more power would be consumed for the same performance since current must scale accordingly.

1.3 Thesis Organization

This thesis will begin with the general approach taken to evaluate architecture trade-offs in Chapter 2. Then the operational amplifier design will be discussed in detail in Chapter 3. Next, simulation results are analyzed in Chapter 4. Finally, the chip layout is presented in Chapter 5 and conclusions are drawn in Chapter 6.

CHAPTER 2

Low Voltage, Low Power Operational Amplifier Design Approach

As mentioned in Chapter 1, the operational amplifier is often the primary bottleneck in performance for switched capacitor circuits. Thus choosing the best opamp architecture suited for a particular application is critical. In this research, the approach taken to design the high performance low voltage, low power operational amplifier was first to examine existing architectures which are able to operate under such conditions. The primary concern is that the number of mosfet devices in each stage must be able to fit within the supply rails and operate in the saturation regime. Therefore opamp designs such as the Class AB which are traditionally used for high performance applications are not a valid choice for low voltage supplies because they do not meet the previously stated criterion.

Three topologies that are viable choices for low voltage operation are the output folded cascode, telescopic, and basic two-stage. In order to correctly evaluate and choose the best architecture based on topology trade-offs, the application of the circuit must be kept in mind. For this research project the highest priority was given to maximizing signal-to-noise ratio given in Equation 1.1 while meeting the gain, settling time, and power specifications.

The second part of the design approach was to analyze noise contributions of switched capacitor circuits. In section 2.2, the noise due to switches and noise due to the operational amplifier are discussed in detail.

2.1 Existing Architecture Analysis

The output folded cascode, telescopic, and basic two-stage amplifier designs are shown in Figures 2-1, 2-2, and 2-3 respectively. Note that all topologies are fully differential since the opamp must reject supply and substrate noise. This type of structure also offers higher swing, higher common mode rejection ratio, and lower clock feedthrough noise (since it appears as a common mode signal) compared to its single-ended counterpart. A fully

differential circuit requires a common mode feedback circuit to set its output common mode voltage, but for simplicity this is not shown in the figures. In order to chose the best architecture for the given application, gain, speed, power, and output swing trade-offs are analyzed.

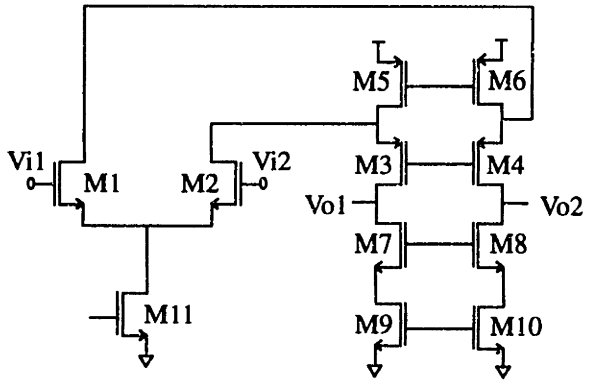


Figure 2-1: Output Folded Cascode Architecture

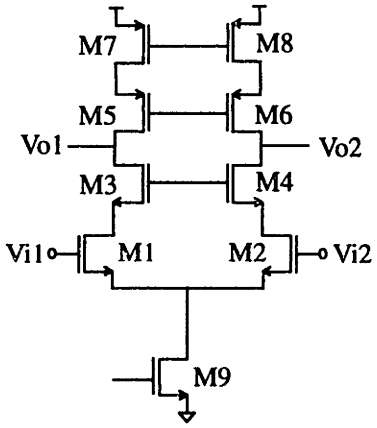


Figure 2-2: Telescopic Architecture

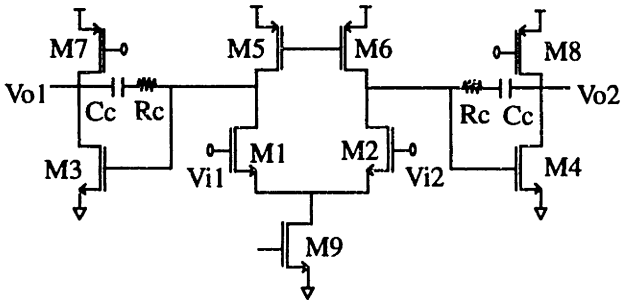


Figure 2-3: Basic Two-Stage Architecture

2.1.1 Output Folded Cascode

Gain

In analyzing the output folded cascode, it is evident that the low frequency voltage gain is the input transconductance times the output resistance. Since the output resistance is a parallel combination of cascode circuits, the overall gain is given by $g_{m1,2}(g_{m7,8}ro_{7,8}ro_{9,10}//g_{m3,4}ro_{3,4}(ro_{1,2}//ro_{5,6}))$, which is effectively on the order of $(g_m ro)^2$. The notation $g_{mx,y}$ and $ro_{x,y}$ represents the transconductance and output resistance, respectively, of x or y.

Speed

The unity gain frequency for this architecture is determined by the input transconductance over the load capacitance, or $g_{m1,2}/C_L$. The lowest frequency nondominant pole is determined by the output stage pmos cascode transconductance over the sum of the parasitic capacitances seen at its source, i.e. $g_{m3,4}/C_p$. The location of this nondominant pole is important since it determines the maximum unity gain frequency obtainable with reasonable phase margin (stability). For the output folded cascode, this nondominant pole is not extremely high in frequency since the transconductance is that of a pmos, which is lower than the transconductance of an nmos. Also, the C_p here is determined by a total of three transistors.

Power

In this topology, typically similar amounts of current are run through each stage. If equal currents, I, are run through each stage of the output folded cascode, the power consumed becomes 2*I*Vsupply where Vsupply is taken to be Vdd-Vss, or 1.8V in this case.

Output Swing

The swing of this architecture is limited by the cascoded transistors in the output stage. Assuming all devices are in the saturation regime, the differential output swing for this topology is 2*Vsupply - (8Vds,sat+4Vmargin). Vds,sat is the minimum drain to source voltage needed to saturate the transistor. Usually, this value is about 200mV. Vmargin is the extra voltage designed in to ensure transistor saturation even if process variations that change threshold voltages exist. Typically, this value is about 100mV. Thus differential output swing for the folded cascode topology is roughly 1.6V, or about 44% of twice the supply voltage.

2.1.2 Telescopic

Gain

For the telescopic configuration, the gain is approximately $g_{m1,2}(g_{m5,6}ro_{5,6}ro_{7,8}//g_{m3,4}ro_{3,4}ro_{1,2})$. This performance parameter, as in the previous topology, is on the order of $(g_m ro)^2$, since the stage is cascoded.

Speed

The strength of the telescopic architecture is high unity gain frequency for given power consumption. Like the output folded cascode, the unity gain frequency is $g_{m1,2}/C_L$. However, the nondominant pole is at a much higher frequency than that of the previous architecture. This is because the nondominant pole is determined by the transconductance of the nmos device above the input transistor divided by the sum of the parasitic capacitances seen at its source, expressed as $g_{m3,4}/C_p$. This value is higher since the nmos has a higher transconductance value than a pmos, and also a smaller sum of parasitic capacitance is seen at this node because only two transistors are connected below it.

Power

As the single stage architecture intuitively suggests, it consumes the least power of all three topologies in this discussion. The power consumed in the telescopic opamp is I*Vsupply assuming current I is running through the stage.

Output Swing

The weakness of this architecture is low output swing. For this topology, differential output swing is given by 2*Vsupply-(10Vds,sat+6Vmargin) where, as mentioned previously, Vmargin is an excess voltage designed in to ensure device saturation. Using the typical Vds,sat and Vmargin values mentioned before, this results in approximately 1V, assuming all devices are in saturation. This differential output swing value only represents about 28% of twice the available voltage supply. Also note that the common mode output swing is asymmetric for this topology since it is a single-stage cascode amplifier with no level shifting. This maybe a disadvantage in certain applications.

2.1.3 Basic Two-Stage

Gain

Finally, in analyzing the basic two-stage, the gain is comparable to that of the folded cascode and the telescopic architectures, which are on the order of $(g_m r_o)^2$. It has two gain stages and the total is given by $g_{m1,2}(ro_{1,2}//ro_{5,6})g_{m3,4}(ro_{3,4}//ro_{7,8})$.

Speed

The unity gain frequency for this architecture is $g_{m1,2}/C_C$ where the transconductance is that of the input transistor. The nondominant second pole, which determines the maximum unity gain with stable feedback, is roughly $g_{m3,4}/C_L$ where the transconductance comes from the nmos in the second stage. Note that the maximum unity

gain frequency for this architecture is much lower than the output folded cascode or telescopic amplifiers.

Power

The power consumed for this two stage topology is somewhat higher than the previous opamps discussed because the second stage generally has a higher current level than the first stage. The power dissipated, then, is equal to slightly > 2*I*Vsupply assuming the first stage has current I and the second stage has a slightly larger current.

Output Swing

The strength of the two stage opamp design is the near rail to rail output swing. For this architecture, differential output swing limited by just two transistors in each output stage, and is given by 2*Vsupply - (4Vds,sat). The resulting value for this case is 2.8V or roughly 78% of twice the supply range, which is superior to the other two topologies.

2.2 Noise Analysis

While gain, speed, power, and output swing are important performance parameters, it is equally important to understand how noise figures into these designs. As mentioned previously, one analog circuit design challenge under low voltage operation is the severe reduction in opamp dynamic range due to decreased output swing. Another factor which contributes to dynamic range is the electronic noise seen at the output.

The three major noise sources in solid-state devices are shot noise, flicker noise, and thermal noise [13]. Shot noise comes from the randomness of density and velocity of charge carriers crossing a given surface in a conductor. This value is fairly significant for subthreshold-operated devices, but tends to be minimal for strongly inverted devices since in a conducting MOSFET channel the charge density is high and electric field is relatively low. Flicker noise arises when the extra electron energy states at the boundary of Si and SiO_2 trap and release electrons from the channel. This type of noise can be minimized with circuit cancelation techniques, so it is generally not significant when compared to

thermal noise. Thermal noise results from the random thermal motions of charged particles, and this type of noise is dominant in many circuits, particularly when the devices are operated in strong inversion.

For switched capacitor circuits, noise comes from primarily two sources, switches and the operational amplifier. In order to analyze these two noise sources, consider Figure 2-4, which shows a typical configuration used for data converters.

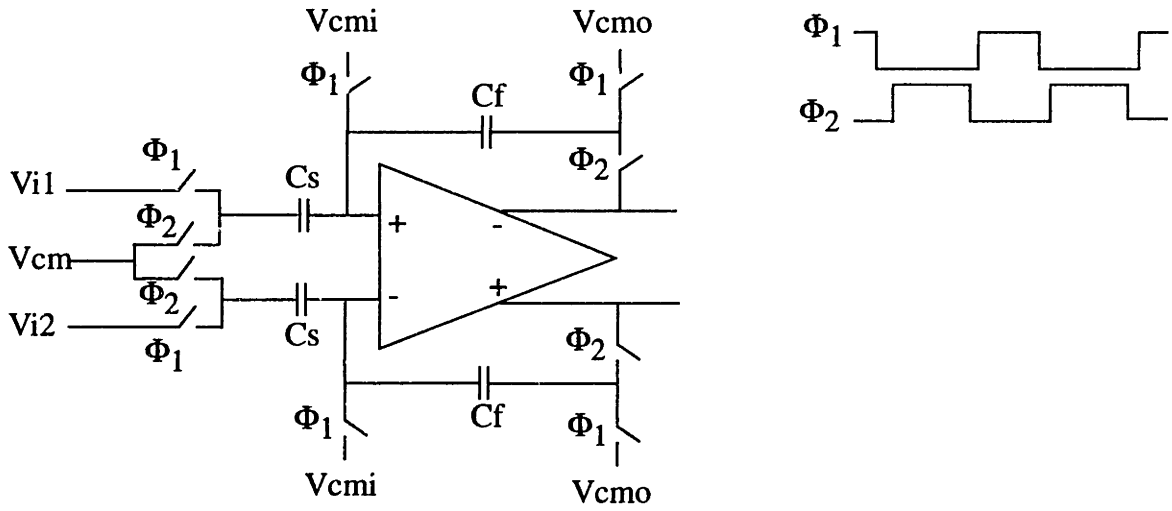


Figure 2-4: Typical Switched Capacitor Circuit

2.2.1 Switches

Integrated circuit components such as switches contribute to noise in the following manner. Since noise is random, the best way to represent it is in terms of power spectral density, S(f), or spot mean-square voltage, $\overline{v_n^2}$. Equations 2.1-2.3 define these two representations for voltage. Note that the power spectral density is the Fourier transform of the autocorrelation function, R(τ).

$$S_v(f) \equiv \int_{-\infty}^{\infty} R_v(\tau)\, e^{-j2\pi f} d\tau \tag{2.1}$$

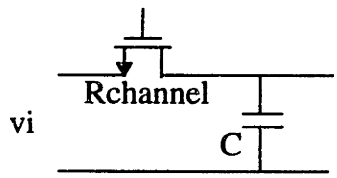
$$R_v(\tau) \equiv \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} v_n(t)\, v_n(t+\tau)\, dt \tag{2.2}$$

$$\overline{v_n^2} = \int_0^\infty S_v(f)\,df = 2S_v(f)\,\Delta f \tag{2.3}$$

To analyze the noise contribution due to switches, the transfer function must be evaluated since the noise will be shaped by this value. An alternative way to define the spot mean-square voltage is shown in Equation 2.4, where $\overline{v_{on}^{2'}}$ is the mean-square voltage and H(f) is the transfer function.

$$\overline{v_{on}^{2'}} = \int_0^\infty |H(f)|^2 \frac{\overline{v_n^2}}{\Delta f} df \tag{2.4}$$

Figure 2-5 shows the equivalent circuit and transfer function for each periodically sampled capacitor of Figure 2-4. When the switch is on, there is a finite resistance in the device channel which leads to thermal noise. When each switch is turned off, this noise is essentially stored on the respective capacitor.



$$H(f) = \frac{1}{1 + j2\pi f R_{channel} C}$$

Figure 2-5: Periodically Sampled Capacitor

To calculate the total noise power, Rchannel can be modeled as having a noise source in series with a power source equal to the Johnson (thermal) noise 4kTRΔf [14]. Thus, as Equation 2.5 shows, the integral evaluation of the contribution of switch noise has a mean squared output noise voltage value of KT/C.

$$\overline{v_{on}^{2'}} = \int_0^\infty \left(\frac{4kTR}{1 + (2\pi f RC)^2} \right) df = \frac{kT}{C} \tag{2.5}$$

A direct ramification of this is that switch noise is independent of Rchannel, and the only way to reduce it is to have a larger sampling capacitor. In addition to switches, the opamp also contributes to noise, as shall be analyzed in the next subsection.

2.2.2 Operational Amplifier

A similar noise analysis can be performed on the operational amplifier's contribution to noise. Figure 2-6 shows a simplified single-ended opamp in closed loop configuration with feedback capacitor Cf, sampling capacitor Cs, and parasitic capacitance Cp.

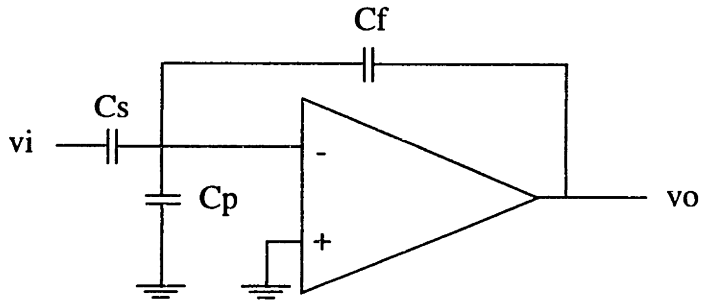


Figure 2-6: Thermal Noise Due To Opamp

The transfer function for the figure above is shown in Equation 2.6 where A(f) is the gain expressed in Equation 2.7 assuming single pole rolloff with gain G_mR, and β is the feedback factor shown in Equation 2.8.

$$H(f) = \frac{A(f)}{1 + A(f)\beta} \tag{2.6}$$

$$A(f) = \frac{G_m R}{1 + j2\pi frC} \tag{2.7}$$

$$\beta = \frac{C_f}{C_f + C_s + C_p} \tag{2.8}$$

Assuming noise is dominated by the two saturated input transistors in strong inversion, the two-sided input-referred noise spectral density is shown in Equation 2.9. The variable 'm' in this equation represents the excess noise factor from other devices, which is a ratio of transconductances and is dependant on opamp architecture [15].

$$S_i(f) = \frac{16mKT}{3g_m} \tag{2.9}$$

Table 2-1 shows the expressions for the three topologies discussed in the previous sections, where g_{mi} is the transconductance of one of the input transistors. From this table, it is evident that the excess noise factor is slightly worse for the output folded cascode compared to that of the telescopic or two-stage since it has two load stages.

Topology	Excess Noise Factor 'm'
Output Folded Cascode	$1 + \frac{g_{mload1}}{g_{mi}} + \frac{g_{mload2}}{g_{mi}}$
Telescopic	$1 + \frac{g_{mload}}{g_{mi}}$
Simple Two-Stage	$1 + \frac{g_{mload}}{g_{mi}}$

Table 2-1: Excess Noise Factor for Various Opamp Topologies [15]

Using the definition for mean-square voltage, the resulting noise contribution due to the opamp (see Appendix A.1) is expressed in Equation 2.10.

$$\overline{v_{on}^2} = \int_{-\infty}^{\infty} |H(f)|^2 S_i(f)\, df = \frac{16mKT}{6\beta C} \tag{2.10}$$

This result shows that opamp noise is inversely proportional to capacitance as expected, and is inversely proportional to the feedback factor.

2.3 Evaluating Trade-offs

Each of the above topologies offers advantages and disadvantages as seen in Table 2-2. Choosing an architecture based on these trade-offs critically depends on which specifications are significant for the particular circuit application. For this thesis, the most important opamp design goal is to maximize signal-to-noise ratio, which is proportional to output swing assuming noise is dominantly thermal and approaches the fundamental limit. This goal should be achieved while meeting the gain, power, and settling time limitations.

Topology	Gain	Speed	Power Consumed	Differential Output Swing	Excess Noise Factor 'm'
Folded Cascode	$\sim(g_m r_o)^2$	g_m/C_L	2*I*Vsup	2*Vsup - 8Vds,sat - 4Vmargin	$1+\frac{g_{mload1}}{g_{mi}}+\frac{g_{mload2}}{g_{mi}}$
Telescopic	$\sim(g_m r_o)^2$	g_m/C_L	I*Vsup	2*Vsup - 10Vds,sat - 6Vmargin	$1+\frac{g_{mload}}{g_{mi}}$
Basic Two-Stage	$\sim(g_m r_o)^2$	g_m/C_C	slightly > 2*I*Vsup	2*Vsup - 4Vds,sat	$1+\frac{g_{mload}}{g_{mi}}$

Table 2-2: Architecture Analysis Summary

The first observation to note from Table 2.1 is that the gain of the architectures are all on the same order, so it is not a deciding factor in choice of topology. Also, since the settling time of ≤100ns for this project is not extremely fast, the advantage of speed in the telescopic opamp is not significant. For a given feedback factor and capacitance, the two-stage and telescopic opamp architectures have lower thermal noise contributions resulting from less number of load devices.

Since the goal, as stated earlier, is to maximize output swing while meeting gain, power, and speed specifications, the basic two-stage architecture was determined as the best choice for this project. Although it consumes slightly more power than the telescopic and the folded cascode topologies, it was believed and later proven to be true that if designed properly, this opamp would consume ≤100μW of power.

CHAPTER 3

Overview of Operational Amplifier Design

Based on the trade-offs and evaluation goals described in Chapter 2, the basic two-stage was determined to be the best choice of topology for a high performance low voltage, low power opamp in low to medium frequency switched capacitor applications. The analysis revealed several advantages and disadvantages. In summary, this architecture has excellent differential output swing, reaching within 4Vds,sat's of twice the supply voltage. The excess noise factor is relatively low, and the gain is moderate. Two design constraints that should be carefully considered with this type of opamp, however, are speed and power consumption.

The proposed opamp has some features that have been added to the simple two-stage topology which improve performance. Figures 3-2 and 3-3 show the proposed opamp schematic and bias circuit respectively. The three highlighted boxes show the main modifications. One addition is cascode transistors, which increases gain without sacrificing output swing or speed. This circuit, however, reduces the common mode input range. This problem is alleviated by the implementation of a replica tail [5, 12], which provides a constant tail current source for the opamp over an extended range of input common mode voltages. Another addition for this fully differential structure is the switched capacitor common mode feedback circuit, which sets the output common mode value. Finally, the bias voltages for the opamp are generated through a bias circuit.

3.1 Simple Two-Stage Architecture in Detail

In order to exploit the strengths and improve the weaknesses of the simple two-stage topology, it is important to analyze the circuit in further detail. Figure 3-1 shows the half-circuit small signal model for this architecture. Note that this is a simplified model in which subscripts 1 and 2 refer to the first stage and second stage, respectively. Thus, translating the right half of Figure 2-3: $Gm1=gm_2$, $R1=ro_2//ro_6$, $C1=C_{parasitic}$ at the drain of M2, $R2=ro_8//ro_4$, and $C2=C_{load}$.

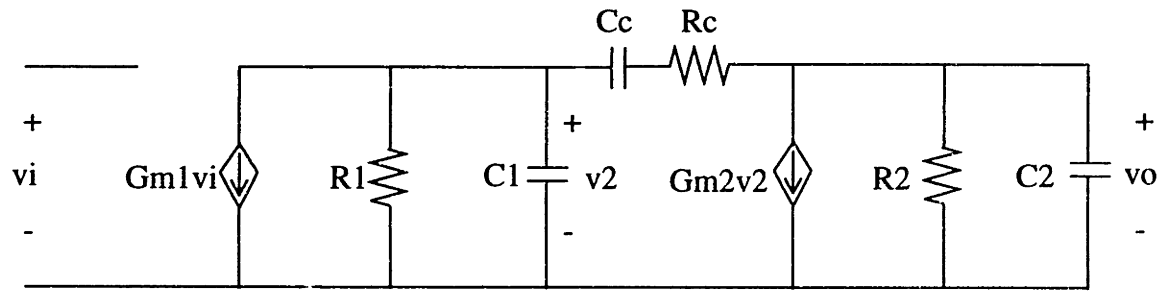


Figure 3-1: Half-Circuit Small Signal Model for Basic Two-Stage Circuit

3.1.1 Gain

From the schematic, it is clear that the dc gain is the first stage transconductance times its output resistance multiplied by the second stage transconductance times its output resistance, as expressed in Equation 3.1. Since the output resistance in each stage is proportional to the device length, shown in Equation 3.2, one way to increase gain is use the same number of devices but increase the gate length. However, this significantly degrades the opamp settling time. Since it was already determined the speed of this opamp topology is fairly slow, increasing gate length to improve gain should be avoided.

$$A_{dc} = Gm_1 R_1 Gm_2 R_2 \tag{3.1}$$

$$r_o = \frac{1}{\lambda I_D} \propto \frac{L}{I_D} \tag{3.2}$$

3.1.2 Speed

The first pole of this system is pushed to low frequency due to the Miller Multiplied (see appendix A.2) compensation capacitor, which is across the second gain stage. Equation 3.3 shows the approximate location of this first pole. The unity gain frequency (UGF) can be approximated as the dc gain times the first pole for a single pole rolloff system. Thus, the UGF reduces to Equation 3.4. The second pole in this system is moved to a higher frequency as a result of the shunt feedback. Equation 3.5 shows the resulting approximate

location. Note that the second pole location should be designed about two to three times higher than the UGF to ensure proper stability and reasonable phase margin. The compensation resistor Rc is used to cancel the zero caused when the compensation capacitor Cc shorts at high frequency and converts the second stage nmos transistor, M4, to a diode-connected configuration. Thus compensation resistor should approximately take on the value of $1/Gm_2$.

$$P1 \cong \frac{-1}{(Gm_2R_2)\,CcR_1} \tag{3.3}$$

$$UGF = A_{dc}P1 \approx \frac{Gm_1}{Cc} \tag{3.4}$$

$$P2 \approx \frac{-Gm_2}{C_2} \tag{3.5}$$

Taking these poles and zeros into account, the settling time can be determined as inversely proportional to the unity gain frequency times the feedback factor, as shown in Equation 3.6. Here C_f is the feedback capacitor, C_s is the sampling capacitor, and C_p is the parasitic capacitor.

$$\tau_{settling} = \frac{1}{UGF}\frac{Cf + Cs + Cp}{Cf} \tag{3.6}$$

Another parameter that affects speed is slew rate, which is the current over capacitance as shown in Equation 3.7. In the two-stage topology specifically, the input stage current charging the compensation capacitor sets one slew limit while the output stage charging the load capacitor and compensation capacitor sets another slew limit. The slew rate is determined by the smaller of the two slew limits. Thus one evident trade-off is between power and speed. If current is increased for a given capacitance, the unity gain frequency and other poles are shifted out and slew rate is larger. This increase in speed, however, is only achieved if power consumption is increased.

$$slewrate = \frac{I}{C} \tag{3.7}$$

3.1.3 Input Device Polarity

All architectures analyzed thus far were shown with nmos input transistors. It is important to analyze if this is always the best way to implement the opamp. As discussed previously, the two-stage topology second pole location is determined by the second stage g_m. Since this second pole is unaffected by pmos input devices, performance is not significantly compromised. Pmos devices would also be beneficial if the input signal level is low in the system of interest. Also, if the circuit is implemented in an n-well process, the pmos device is more controlled since the threshold voltage is not a function of the source to bulk voltage.

However, nmos input devices are often chosen for many reasons. The conducting channel in an nmos transistor contains electrons which have approximately three times the mobility of the holes which form the conducting pmos channel. So for the same g_m performance, area would be saved using the nmos device. The reduced area also results in lower input capacitance, which translates to faster settling time. Also, for the same transconductance and a given size, lower current and thus less power consumption is possible with the nmos transistor.

3.1.4 Common Mode and Power Supply Rejection Ratios

The common mode rejection ratio (CMRR), positive power supply rejection ratio ($PSRR_{plus}$), and negative power supply rejection ratio ($PSRR_{minus}$) for a fully differential structure are given in Equations 3.8, 3.9, and 3.10 respectively. Note that the first subscript represents the ac input and the second subscript is the measured output, where d=differential, c=common, plus=positive power supply, and minus=negative power supply.

$$CMRR = \frac{A_{d,d}}{A_{c,d}} \tag{3.8}$$

$$PSRR_{plus} = \frac{A_{d,d}}{A_{plus,d}} \tag{3.9}$$

$$PSRR_{minus} = \frac{A_{d,d}}{A_{minus,d}} \tag{3.10}$$

Rejecting common mode signals is important since the goal is to amplify differential signals only. The CMRR is ideally infinite for any fully differential structure assuming no mismatch between devices. In reality, however, process mismatch is unavoidable so CMRR is finite.

Power supply rejection is important if analog and digital systems exist on one chip with the same power supply. Also, analog circuits such as switched capacitor circuits can themselves generate noise in the supply resulting from transient currents. The PSRR for a two-stage is worse for the negative rail than the positive supply since the second stage output nmos will be diode-connected by the compensation capacitor at higher frequency. Thus, the poles of $A_{d,d}$ and $A_{minus,d}$ do not roll off together. An important note is that the $PSRR_{minus}$ is better in other topologies such as the telescopic and output folded cascode compared to this architecture because their compensation capacitors terminate to ground.

One way to improve CMRR and PSRR is to have a constant opamp tail current source with a large output resistance. This near-ideal current source would reduce the affect of variations in common mode input and power supplies. The resulting reduced common mode gain and lower power supply gain improves both rejection ratios.

3.2 Proposed Design

Figures 3-2 and 3-3 show the proposed opamp design and the bias circuit respectively. The three highlighted boxes in Figure 3-2 show the main modifications of cascode transistors, replica tail, and common mode feedback applied to the simple two-stage architecture with nmos inputs. These circuits are discussed in further detail in the following subsections.

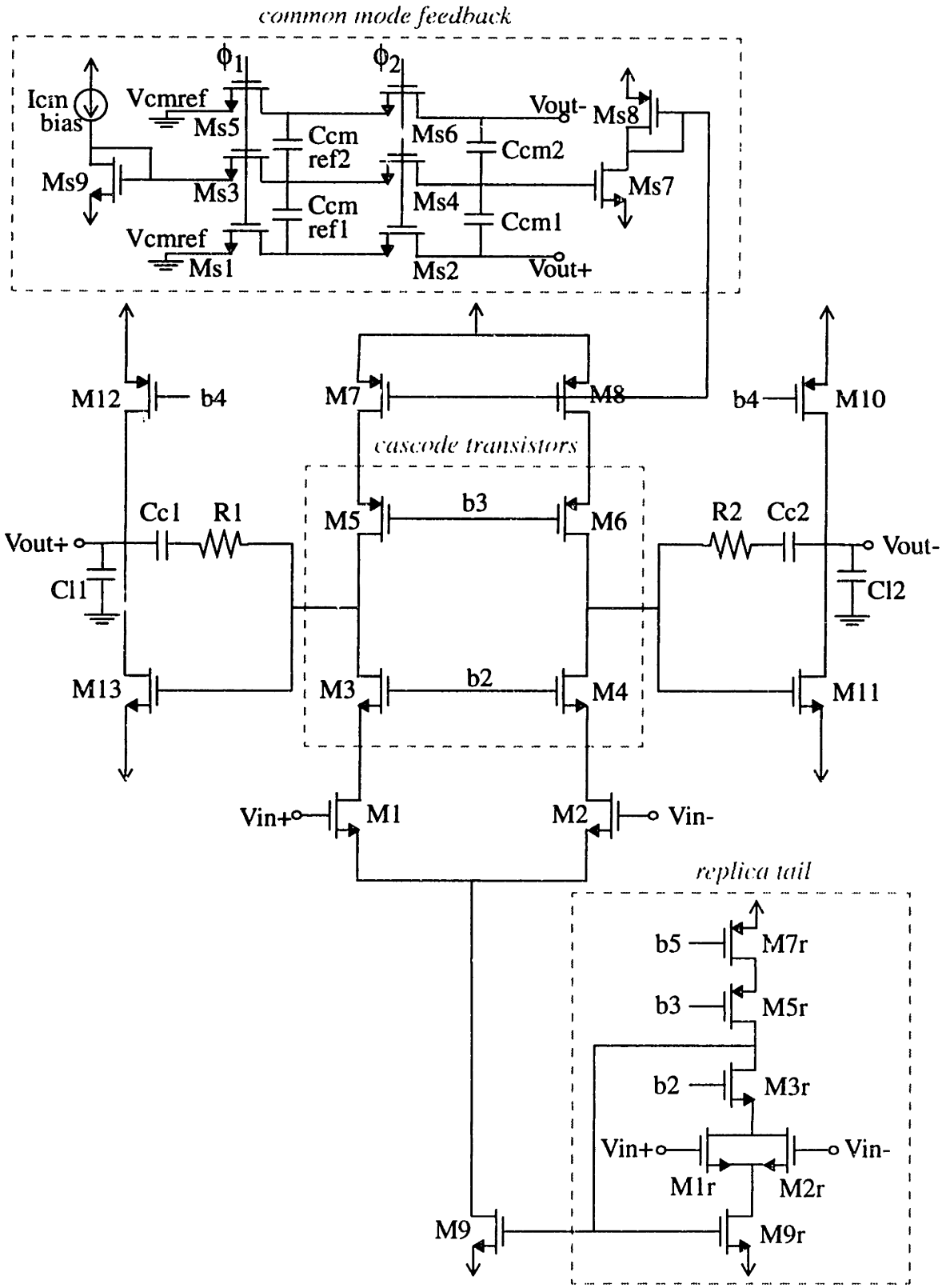


Figure 3-2: Proposed Opamp Schematic

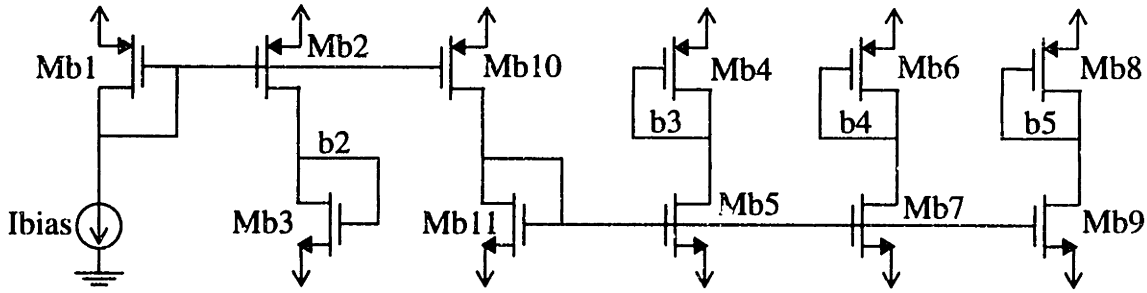


Figure 3-3: Bias Circuit

3.2.1 Cascode Circuits

As mentioned previously, one way to improve gain in the two-stage is to increase gate lengths of the devices. At first this may seem attractive since no additional transistors are required which saves area, and no extra bias voltages need to be generated. This increase in length, however, slows down the opamp significantly.

A better approach is to increase the output resistance of the first stage by adding cascode devices, as shown in the proposed opamp design in Figure 3-2. The output resistance r_o becomes $g_m r_o^2$, where the cascode provides a boost of $g_m r_o$. It is important to note that if the cascodes were added to the second stage, gain would be improved by the same value, but the differential output swing would be compromised by 4Vds,sat+2Vmargin, or approximately 28% of twice the available voltage supply. Thus by placing the cascode in the first stage, the opamp has increased gain without sacrificing speed nor differential output swing. The penalty of having cascodes in the first stage, however, is decreased common mode input range. In the next section a circuit will be described that alleviates this problem.

3.2.2 Replica Tail

From the analysis in section 3.1.4, it was seen that a constant tail current source with high output resistance is desirable since it approximates an ideal current source which

translates to better opamp performance, improved common mode rejection ratio, and higher power supply rejection ratio. Such a source would also increase input common mode range since the current would remain constant even if the input transistors' source voltage varies significantly. This concept is implemented in what is presented here as the replica tail.

Figure 3-2 highlights the replica tail circuit implemented in the proposed opamp design. To begin analysis, the first observation is that there are three transistors in the main opamp half-circuit (M9, M1, M3 or M9, M2, M4) from the -0.9V Vss rail to the first stage output, designed nominally at 0V. This means that the tail transistor M9 is operating in saturation but is towards the edge of triode. The problem then, is that if there is a variation in voltage at the drain of M9, the current will be strongly Vds-dependent as the device enters the triode region. As this Vds-dependent current changes, g_m also changes which adversely affects performance. The replica tail alleviates this problem.

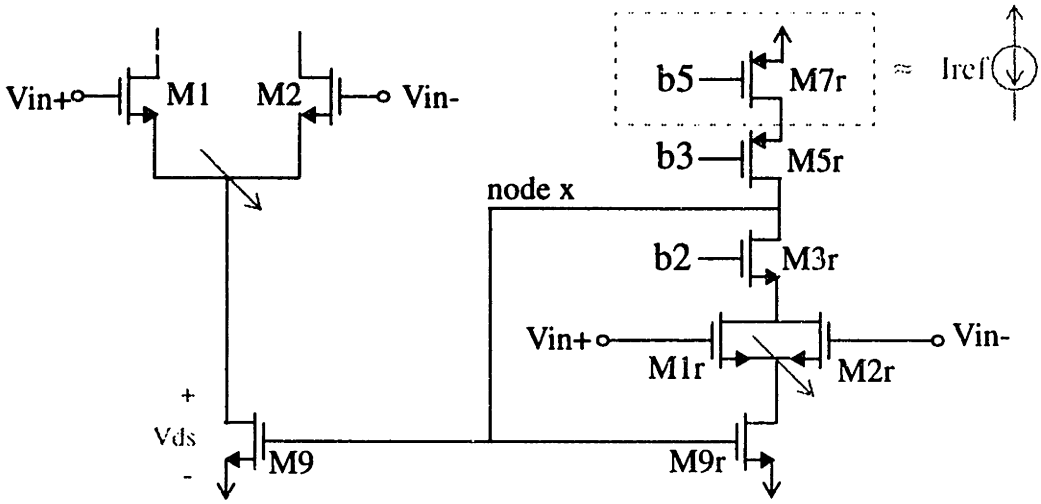


Figure 3-4: Replica Tail Concept

Figure 3-4 shows the replica tail circuit and part of the first stage in the opamp. The main concept of this feature is to adaptively change the bias voltage at the gate of M9, labeled 'node x', to provide constant current even when the drain voltage of M9 varies [5, 12]. In the implementation presented here, the W/L ratios between the replica tail and the main opamp are the same. The gates of the input devices M1r, M2r and devices M9r, M3r,

M5r of this replica tail are connected respectively to the main opamp (as shown in Figure 3-2). The device M7r is not connected to the main opamp and can be thought of as an ideal current source which sets the current down the replica tail. For purely differential signals, the circuit has no functional affect on the opamp, assuming no mismatch. For common mode signals, however, the circuit acts as a third input in the following manner.

Suppose a common mode signal is applied to the main opamp such that the drain voltage of M9 reduces, forcing the transistor into triode operation. If the gate of M9 was simply biased by a constant voltage, the tail current would be governed by this drain to source voltage. With the replica tail, however, the common mode signal is applied to the replica tail input transistors as well. Therefore the same reduction at the drain of M9 is present at the drain of M9r. Since the current source provided by M7r must flow through the replica tail, the voltage at 'node x' will adaptively bias itself to support this current. Since 'node x' is connected in a current mirror fashion to the gate of M9, the result is that the replica tail will compensate for any change in M9 drain voltage. Thus the current running through M9 will be the current running through M9r multiplied by the W/L ratio between the two devices (unity in this case), regardless of drain voltage. Effectively, this circuit expands the common mode input range which was restricted previously by the addition of cascode circuits. Figure 3-5 shows the improvement in input common mode range as a result of the replica tail circuit. Specifically, simulations show that a constant current is maintained even when just a few millivolts are placed across the drain and source of the tail transistor.

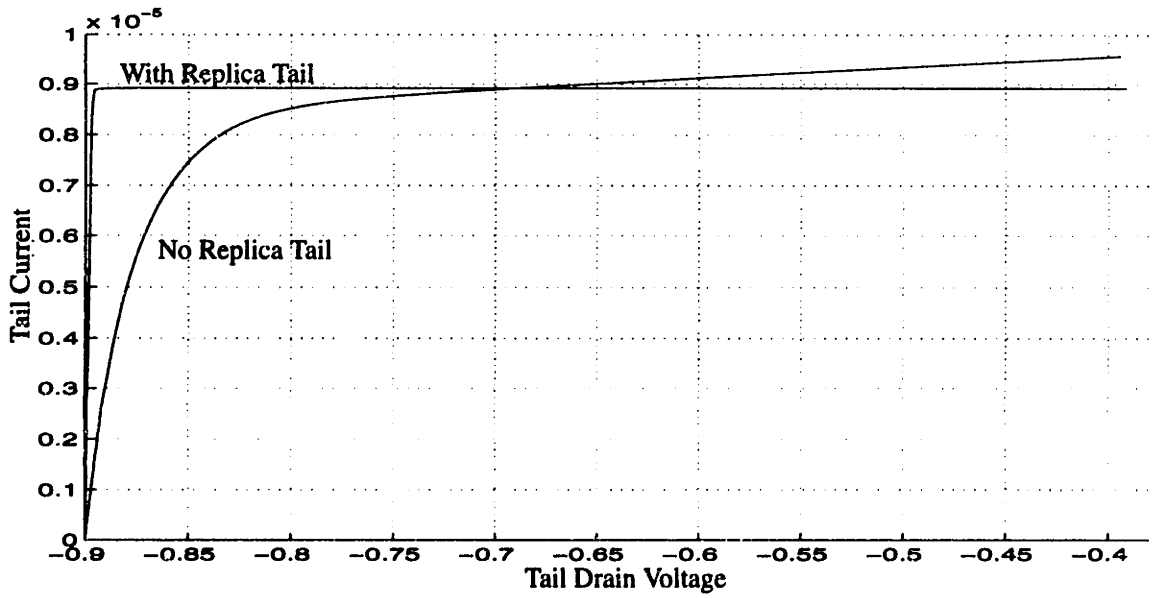


Figure 3-5: Simulation of Extended Input Common Mode Range Due to Replica Tail

Other advantages of the replica tail are seen by examining the increase in effective output resistance of M9. This circuit improves the tail resistance from just ro9 to ro9 multiplied by the open loop gain of the replica tail. Specifically, Equation 3.11 shows the new increased value of output resistance, ignoring minor source degeneration from the intrinsic resistance of tail transistor M9.

$$R_{tail} = r_{09}\left[g_{m2r}\left(\left(g_{m5r}r_{05r}r_{o7r}\right) \parallel \left(g_{m3r}r_{03r}g_{m2r}r_{02r}r_{o9r}\right)\right)\right] \times \frac{g_{m9}}{g_{m2}} \qquad (3.11)$$

This increased impedance improves common mode rejection ratio since a common mode signal will now generate a minimal variation in common mode current. The higher resistance also improves negative power supply rejection ratio because change in the rail will have less of an affect on the tail current. An intuitive way to see this is that just as the replica tail compensates for change in voltage at the drain of M9, the circuit will also adaptively change 'node x' to support the current set by M7r when the negative rail is varied.

Another important feature of this replica tail circuit is that the transistor widths and current flow can be scaled to reduce power consumption and area. The current through M9 would then be the value of the current through M9r multiplied by the scaling factor. This

scaling, however, would reduce opamp performance since the transconductance of the input replica devices would decrease, leading to lower frequency poles.

One issue to note is that when physically laying out these transistors, there is mismatch between devices. This mismatch can translate differential signals to common mode signals, and vice versa. The result is that the replica tail circuit does not provide as significant an improvement. However, even with mismatch on the order of 0.02μm for device gate lengths and 1mV threshold voltage offset per transistor, the replica tail improves performance compared to having just a simple bias voltage placed at the tail transistor [16].

3.2.3 Common Mode Feedback

For fully differential topologies, it is important to set and maintain the common mode output voltage. The local common mode feedback circuit for this opamp, highlighted in Figure 3-2, is implemented using switched capacitors.

This common mode feedback circuit uses capacitors to store voltages transferred via pass gates (single transistors) during non-overlapping clock cycles. In the schematic, the output common mode voltage is set by Vcmref. Since the output stage of the opamp consists of two transistors, Vcmref was set to ground to maximize output swing (exactly between the positive and negative supply rails). The voltage at gate Ms9 is set to support current Icmbias, which is the nominal current desired through M7 and M8. During the first clock phase ϕ_1, Vcmref minus the gate voltage of Ms9 is placed upon Ccmref. On the opposite clock phase ϕ_2, the difference between this voltage and the actual output common mode voltage is placed across Ccm. This difference drives the inverting stage Ms7 and Ms8, which appropriately adjusts the gate bias of M7 and M8. The transistors Ms7 and Ms8 provide the proper inversion since the two stage architecture is noninverting. As the two clocks continuously operate, the output common mode voltages are set and maintained to Vcmref.

The switches Ms1-Ms6 were sized small enough to reduce charge injection and parasitic capacitance but large enough to allow current to pass through when they are

turned on. The W/L ratio was simulated and chosen such that the RC time constant was small enough to settle within the desired time. The switches were driven by a voltage higher than the available supply because 0.9V is very close to the threshold voltage (~.75V for nmos), thus the transistor would only weakly turn on. This structure implemented pass gates instead of complimentary gates (one pmos transistor and one nmos transistor connected in parallel) because it has a lower resistance, thus the 1/RC pole would be higher in frequency. Also, bootstrapping of the pmos device is not possible because in an nwell process this would reverse bias device diodes.

It should be noted that the switched capacitor circuit was chosen over the continuous version [17] for several reasons. The continuous method first has the disadvantage of mosfet nonlinearity. Also, the devices in this circuit reduce output swing as well as take up large area. Another disadvantage is that large resistor values would be needed considering the output load. This introduces a low frequency pole, so a capacitor would have to be added in parallel to introduce a zero for pole cancelation. This capacitor, in turn, would reduce settling time.

3.2.4 Bias Circuit

Figure 3-3 shows the bias circuit used for this opamp design. Due to the restricted supply voltage, the bias voltages were generated using pairs of an nmos transistor and a pmos transistor with one device diode connected (Mb2 and Mb3; Mb4 and Mb5; Mb6 and Mb7; Mb8 and Mb9). The appropriate polarity transistor was diode-connected to provide the bias voltage which tracks the main opamp device. This enables a high swing circuit with biases generated at low impedance points. Generating biases at low impedance nodes are advantageous because a small change at these points will not result in a large gain and cause significant deviation from designed voltages.

One important note is that most of the W/L ratios were sized such that the g_m was large enough to drive the circuit capacitance. The exception to this was transistor Mb3, which had to generate a fairly large negative voltage. Since current had to be conserved to

save power, the sizing of this transistor was forced to have a large gate length and small width. However, this is not a significant problem since it drives a cascode device.

CHAPTER 4

Simulation Results

Simulations using HSPICE and MATLAB were performed throughout the design process to validate and optimize opamp performance. The process used was characterized in a level 13 HSPICE model file. The next sections show simulation plots and discuss the results of the proposed opamp design described in Chapter 3.

4.1 Simulations

The following figures show the simulation results of the proposed opamp design. The output swing (defined here as a 20% change in incremental gain) was very large, reaching within two Vds,sat's of the rails. Specifically, simulations in Figure 4-1 show a differential output swing of +/- 1.54V. The 0.1% settling time for a 600mV step input, or 1/3 the supply voltage, was about 65ns as shown in Figure 4-2. The total power consumption of this design was approximately 95μW. As Figure 4-3 depicts, the dc gain attained was approximately 85K with a phase margin of 61° at a unity gain frequency of 41MHz. Figure 4-4 shows the common mode rejection ratio was about 69dB while the positive and negative power supply rejection ratios were approximately 46dB.

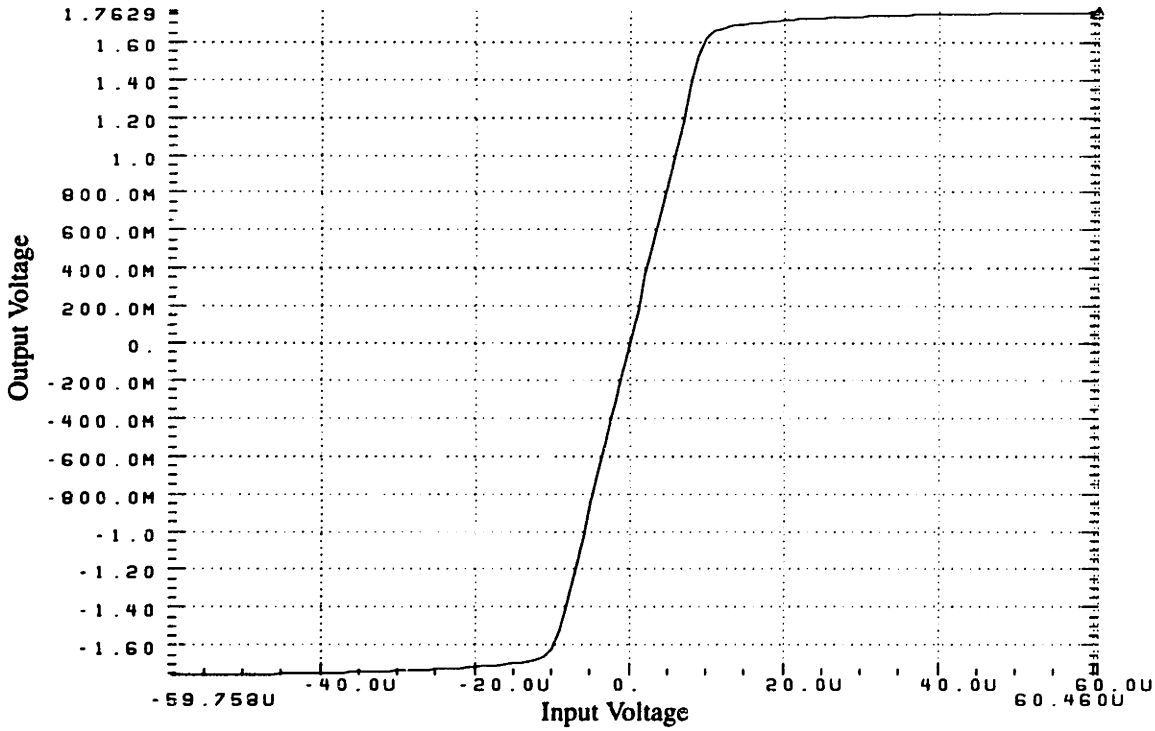


Figure 4-1: Output Swing Simulation

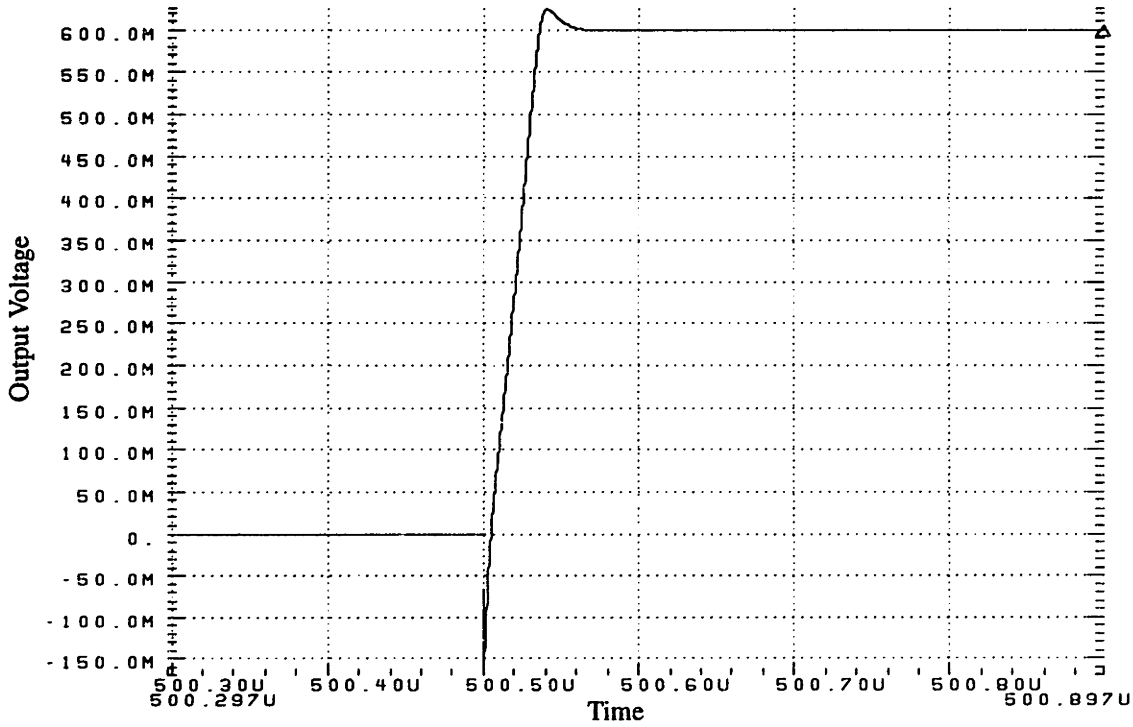


Figure 4-2: Settling Time Simulation

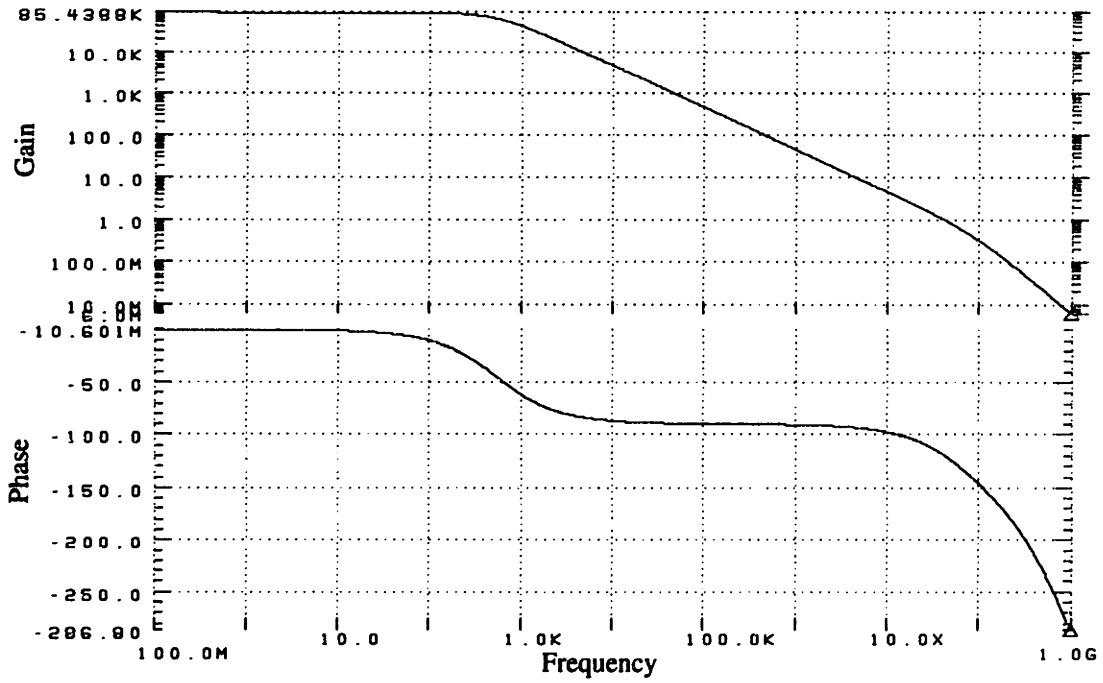


Figure 4-3: Gain, Phase Margin, and Unity Gain Frequency Simulation

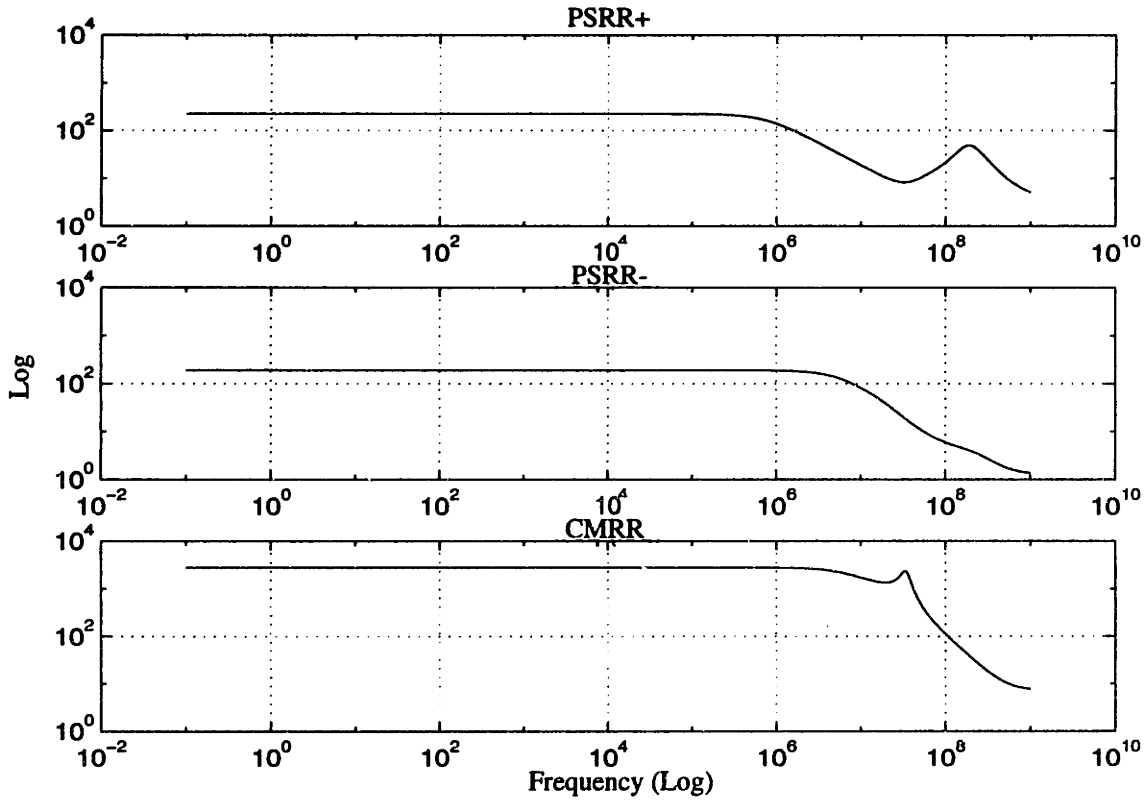


Figure 4-4: PSRR+, PSRR-, CMRR Simulations

4.2 Discussion

Below, Table 4-1 shows the summary of design goals and simulation results.

*Technology: 0.6μm CMOS
*Power Supply: 1.8V

Performance Parameter	Design Goal	Simulation Results
Swing (>20% inc. gain)	close to rails	+/- 1.54V
Total Power	< 100μW	95.29μW
0.1% Settling Time	< 100ns	65.1ns
Slew Rate	> 12V/μs	28.0V/μs (down) 34.7V/μs (up)
Gain (DC)	> 10K (80dB)	85.44K (98.6dB)
Phase Margin	> 60°	61.1°
Unity Gain Frequency	> 15MHz	41.48MHz
CMRR	max	69.0dB
PSRR +	max	46.92dB
PSRR -	max	45.65dB
Input Referred Offset	< 10mV	-12.82mV
Input Referred Noise	64.5 $nV/\sqrt{Hz}$	[1]68.36$nV/\sqrt{Hz}$

1 - Hand Calculated Using Equation 2.10

Table 4-1: Summary of Design Goals and Simulation Results

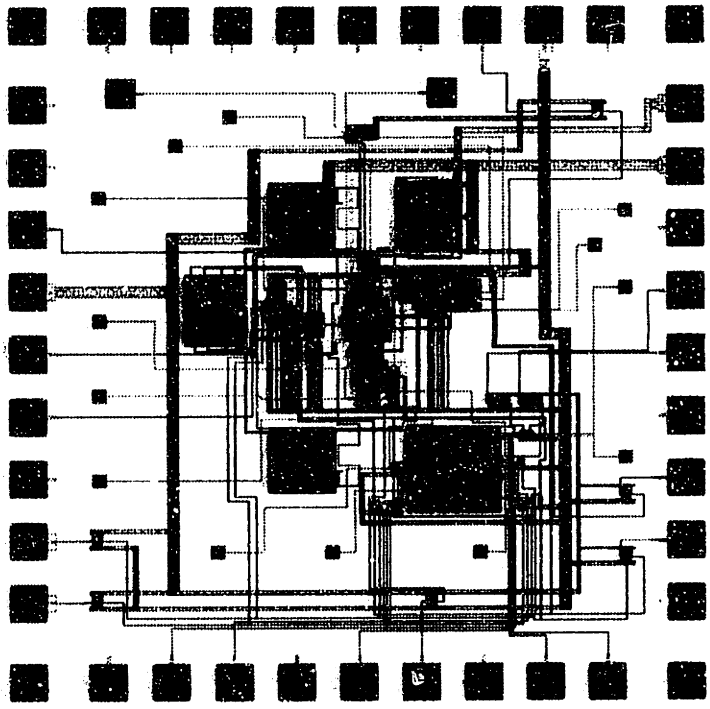
Overall, the proposed opamp design has very good results for operating off of 1.8V and consuming only 95μW of power. The simulation results meet the design goals in nearly all the performance parameters. As expected, the opamp has very large differential output swing, representing approximately 86% of twice the power supply. The circuit also has ample gain and a high unity gain frequency. While the input offset and noise was slightly beyond the design goal, the deviation is not significant. Also, these goals could be met by trading off performance in other parameters. The simulation results prove this opamp is well-suited for medium to low frequency switched capacitor applications.

CHAPTER 5

Chip Layout

A 10x version of the proposed opamp circuit was laid out in Cadence in the 0.6um nwell triple metal single poly HP process from MOSIS. A larger version of the opamp design was used in layout since driving larger capacitors enables easier testing. The layout of this chip is shown in Figure 5-1. The silicon area used for this 10x version was approximately 2.5mm by 2.5mm.

The opamp configuration implemented many switches which controlled closed loop mode, feedback voltage refreshing mode, and output shorting mode among others. The switches were implemented using nmos pass gates. The gate voltage is boosted since a Vdd of 0.9V would not be sufficient to turn the transistor on. Inverters were used to buffer digital paths, and the outputs of the opamp were sent through unity gain source follower buffers since they had to drive large pin capacitances.



*Technology: 0.6µm CMOS
*Power Supply: 1.8V
*Die Size: 2.5mm x 2.5mm
(10x Version)

Figure 5-1: Layout of Opamp Chip

5.1 General Techniques

In contrast to many digital circuits where transistors are automatically generated in layout, in the analog domain custom layout is crucial. Improper layout can lead to significant mismatches and parasitic capacitances which would ruin sensitive analog nodes and degrade circuit performance.

5.1.1 Transistors

The layout of large width transistors were implemented using the folding technique, which reduces junction capacitance significantly. This comb technique not only improves speed but it saves area as well. In order to avoid asymmetry and mismatch of transistors due to the angle of ion implantation, the common centroid configuration was also incorporated. This type of layout configuration removes the first order gradients in gate length and width as well as in threshold voltages. Another feature included shielding in metal three of sensitive nodes, like the common mode input node in the first stage located at the gates of M7 and M8.

5.1.2 Resistors

The resistor was first going to be implemented as an nmos with the gate tied to Vdd. This has the advantage of tracking the performance of the output nmos transistor, which determines the maximum unity gain frequency with reasonable phase margin. However, since the technology was an nwell process, the backbias from source to bulk in the nmos would increase threshold such that an unreasonably large device would be required to get the desired resistor value. Thus, a polysilicon resistor, which has low leakage current, low parasitic capacitance, and good matching was used. A meander layout was used since a fairly large L was required. To optimize matching, the right angled corners were avoided.

5.1.3 Capacitors

For linear capacitors, the structure implemented was metal two and poly forming one plate, and metal one forming the other plate. For optimum matching a square geometry was used. If the capacitor had one plate terminated to ground, the metal two-poly plate was used since this would also terminate parasitic capacitances seen at the bulk or well. Again, common centroid was used for matching capacitors.

CHAPTER 6

Conclusions

A high performance, low voltage, low power CMOS operational amplifier has been designed. The two-stage architecture was found to be the best topology for the given specifications, primarily since it has large differential output swing compared to other architectures. Operating with 1.8V power supply, the opamp consumes less than 100μW of power and has a large signal-to-noise ratio.

One of the main features is the implementation of a replica tail circuit which adaptively biases the tail transistor to provide constant current. Simulations show that this circuit enhances the common mode input range, improves CMRR and PSRR-, and improves overall performance.

Simulated results enable use of this opamp in a 12-bit pipeline A/D converter at 6MHz and 16-bit delta-sigma A/D converter at 20kHz, which include applications such as scanners and audio systems.

APPENDIX A

A.1 Operational Amplifier Thermal Noise Analysis

Based on Equations 2.6-2.10 which express the operational amplifier gain, feedback factor, transfer function, and input-referred noise spectral density, the mean-square voltage can be easily calculated. The following shows the analysis for the two-stage opamp architecture:

$$H(f) = \frac{A(f)}{1 + A(f)\beta} = \frac{G_{m1}R_1G_{m2}R_2}{1 + j2\pi f G_{m2}R_2C_cR_1 + G_{m1}R_1G_{m2}R_2\beta} \tag{a.1.1}$$

$$|H(f)|^2 = \frac{(G_{m1}R_1G_{m2}R_2)^2}{(1 + G_{m1}R_1G_{m2}R_2\beta)^2 + (2\pi f G_{m2}R_2C_cR_1)^2} \tag{a.1.2}$$

$$\overline{v_{on}^{2'}} = \int_{-\infty}^{\infty} |H(f)|^2 S_i(f)\,df = \frac{32mKT}{3G_{m1}} \int_0^{\infty} \frac{\dfrac{(G_{m1}R_1G_{m2}R_2)^2}{(2\pi G_{m2}R_2C_cR_1)^2}}{\dfrac{(1 + G_{m1}R_1G_{m2}R_2\beta)^2}{(2\pi G_{m2}R_2C_cR_1)^2} + f^2} df \tag{a.1.3}$$

Using the following identity, where the substitution of variable made was f=ytanθ:

$$\int_0^{\infty} \frac{x}{y^2 + f^2} df = \frac{\pi x}{2y} \tag{a.1.4}$$

The result becomes:

$$\overline{v_{on}^{2'}} = \frac{16mKT}{6\beta C} \tag{a.1.5}$$

A.2 Miller Approximation

In many amplifiers, an approximation of impedance can be made which makes analysis of frequency response simpler. The effect is called Miller Multiplication, and it refers to the effective value of a component as seen from the input port. For example, Figure A-1 shows a capacitor, nominal value C, across an inverting amplifier with gain A. It is clear that

$$Ix = \frac{Vx - Vo}{\frac{1}{Cs}} \qquad \text{(a.2.1)}$$

and by definition

$$Vo = A\,(Vplus - Vminus) = -AVx \qquad \text{(a.2.2)}$$

thus

$$\frac{Vx}{Ix} = \frac{1}{(1 + A)\,Cs} \qquad \text{(a.2.3)}$$

In other words, the effective capacitance, C_M, seen from the input port becomes Miller Multiplied.

$$C_M = (1 + A)\,C \qquad \text{(a.2.4)}$$

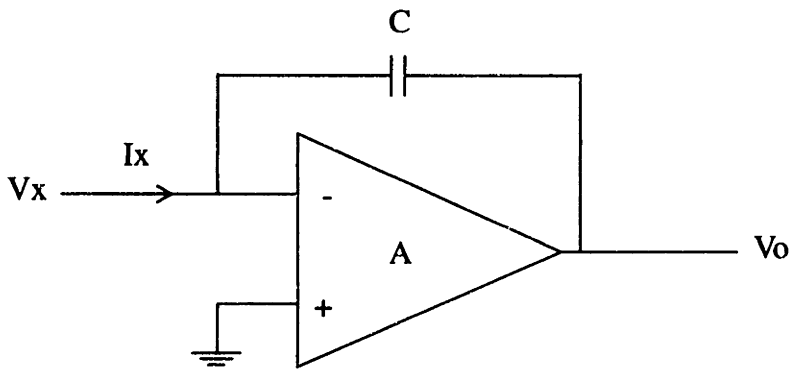


Figure A-1: Miller Approximation

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