Active Sensing in Silicon-based MEMS Resonators

by

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Abstract

Microelectromechanical resonators are advantageous over traditional LC tanks and off-chip quartz crystals due to their high quality factors, small size and low power consumption. FET-sensing has been demonstrated in resonant body transistors (RBTs) to reach an order of magnitude higher frequencies than possible with passive resonators due to the greater sensing efficiency of FET sensing over traditional mechanisms such as capacitive or piezoelectric sensing. This thesis explores FET-sensing in Si-based MEMS resonators with dielectric and piezoelectric materials for design of fully unreleased CMOS-integrated resonators for multi-GHz frequency applications.

Monolithic integration of Si-based MEMS resonators into CMOS is critical for commercial applications due to reduced size, weight and parasitics. A vast majority of CMOS-integrated resonators require a release step to freely suspend their vibrating structures, necessitating costly, complex encapsulation methods. This thesis proposes the development of fully unreleased resonators in CMOS using acoustic confinement structures, which may be realized without any post-processing or packaging. These dielectrically driven, FET-sensed resonators may be fabricated at the transistor-level of a standard CMOS process, and are demonstrated upto 11.1 GHz with quality factors (Q) up to 252 with footprints of less than $5\,\mu m \times 7\,\mu m$ with temperature coefficients of frequency (TCF) < 3 ppm/K.

While electrostatic resonators have been primarily explored in this work due to the availability of such dielectric materials in a standard CMOS stack, piezoelectric materials remain popular in commercial MEMS resonators for their high electromechanical coupling factors. Recent years have seen a push towards integration of piezoelectric materials into standard CMOS for switching and memory applications. This work explores the performance improvements arising from the integration of CMOS-ready piezoelectric materials such as AlN into a resonant body transistor. This is shown to improve transduction efficiency for low insertion losses at multi-GHz frequencies, for applications in communications to microprocessor clocking.

Thesis Supervisor: Dana Weinstein
Title: Associate Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

Microelectromechanical (MEMS) resonators are advantageous over traditional LC tanks, off-chip quartz crystals, and surface acoustic wave (SAW) devices due to their high quality factors (Q), small size and low power consumption in applications such as communications, navigation, microprocessor clocking, and inertial sensors etc. These MEMS resonators can be driven and sensed using a variety of transduction mechanisms including electrostatic [5], piezoelectric [6], thermal [7], optical etc.

Silicon has been keenly studied as the material of choice for the design of MEMS resonators due to its abundance and inexpensiveness, and due to the development of batch-fabricated, standardized integrated circuit (IC) technologies driven by Moore's law. The availability of high purity Si, and the development of thin film and lithographic microfabrication techniques result in extremely small but high-precision mechanical structures with excellent mechanical properties [8]. For high frequencies of operation, especially beyond the 100 s of MHz range, Si as a material exhibits a relatively high intrinsic $f.Q$ limit with orientation $< 100 >$ as compared to materials such as quartz, AlN and routing metals [9] (see appendix A). This high $f.Q$ limit may be explained by the fact that since Si is a semiconductor, acoustic losses due to phonon-electron interactions are minimized as compared to metals and the crystallinity of Si leads to low losses at grain boundaries which result in materials such as AlN. As a result, Si has been widely incorporated into both dielectric and piezoelectric resonators for Q-boosting and improvement in power handling capability which

is discussed further in chapter 5.

This thesis explores such Si-based MEMS resonators using dielectric and piezoelectric transduction mechanisms with active sensing for scaling to high frequencies. To this end, the motivation for scaling to multi-GHz frequencies with some potential applications are discussed. Following this, the limitations of traditional MEMS transduction mechanisms for frequency scaling are considered which leads to the need for a more efficient transduction mechanism such as active sensing using field effect transistors (FETs). We then discuss with the advantages of CMOS integration for FET-based transduction mechanism with an overview of the typical CMOS process and the different ways in which MEMS and RF MEMS devices have been included in a CMOS process stack to-date. Following this, the vision for the CMOS-integrated RBTs as fully unreleased devices with acoustic isolation structures formed in the standard CMOS stack is discussed. Finally, the use piezoelectric materials in place of dielectrics is explored with such FET-based sensing for further improvements in transduction efficiency for design of low impedance filters and oscillators.

1.1 The push towards multi-GHz frequencies

With the increasing pervasiveness of wireless communication technology including smartphones and personal area networks, the overcrowding of the frequency spectrum at low frequencies has seen a surge in demand for high-Q filters and oscillators that operate in the previously unexplored multi-GHz frequency regime. At the lower end of this spectrum, exploratory applications such as wireless personal area networks (WPAN) and body-area networks (BAN) around 2.4 GHz have been allocated frequency bands in previously unregulated high frequency bands, creating a need for frequency scaling of devices.

At higher frequencies, the Extremely High Frequency (EHF) band is designated between ($30-300$ GHz) in the near to far infrared regimes. Electromagnetic radiation in this band has high atmospheric attenuation due to absorption by rain and atmospheric gases, especially the $57-64$ GHz band which is attenuated due to resonance

of the oxygen molecule. While this restricts communication to short distances, it is in turn useful for secure wireless local area networks (WLAN at 60 GHz) that improve spectrum utilization efficiency through frequency band reuse. The EHF band is also useful for mm-wave imaging for concealed weapons detection as clothing and other organic materials are transparent in certain mm-wave atmospheric windows. Furthermore, specific applications such as high-definition video links for live, high-res streaming for sports events call for a continuous scaling of resonator frequencies to the multi-GHz and THz regimes.

Below we consider the different types of MEMS resonators and transduction mechanisms available and what is most amenable to frequency scaling.

1.1.1 Transduction Mechanisms in MEMS resonators

The transduction mechanisms used to actuate and sense vibrations in MEMS resonators may be broadly classified into active and passive transduction mechanisms. Passive mechanisms such as dielectric and piezoelectric transduction do not involve an active element such as a transistor or a constant current bias to the device. These are usually low-power devices that apply driving and sensing voltages to the input and output terminals. Electrostatic and piezoelectric transduction are briefly discussed below as they are two of the most popular passive transduction mechanisms relevant to this work.

Electrostatic transduction

The first of these, dielectric or electrostatic transduction employs electrostatic forces to convert energy from the electrical to the mechanical domain and vice-a-versa. Consider the simple scenario of a parallel plate capacitor with capacitance C with one plate tied to ground and the other plate biased at a DC voltage V_{DC} with a small AC signal at the desired frequency, $v_{ac}^{j\omega t}$. In this case, the driving force between the

capacitor plates is given by:

$$\begin{aligned} f_d =& \frac{1}{2}\frac{\partial C}{\partial x}(V_{DC} + v_{ac}^{j\omega t})^2 \\ =& \frac{1}{2}\frac{\partial C}{\partial x}(V_{DC}^2 + v_{ac}^{2j\omega t} + 2V_{DC}v_{ac}^{j\omega t}) \end{aligned} \tag{1.1}$$

As seen from the above equation, the DC force is required to generate and amplify the force at the frequency of the AC voltage v_{Ac} and the resulting force also has a DC component as well as a 2ω component. On the sensing side, for a DC voltage of V_{DC} applied across the plates of the resonator, the output current is given by:

$$i_{out} = V_{DC}\frac{\partial C}{\partial t} \tag{1.2}$$

Capacitive resonators have been traditionally fabricated as air-gap devices which needed extremely narrow, high-aspect ratio trenches for high electrostatic forces for actuation and sensing [10]. However, due to the fabrication difficulties associated with deep, narrow air-gaps, along with prevalent failure mechanisms such as stiction, particles lodged in gap, imperfect sidewalls etc., high-k dielectrics were explored in their place for electrostatic actuation [5]. Dielectric films not only make the fabrication easier, but also increase the mechanical driving force which is directly proportional to the relative dielectric permittivity, thus improving transduction efficiency. In such resonators, the acoustic free boundary conditions are no longer defined at the edges of the driving and sensing capacitor but the acoustic wave now extends into the dielectric material and beyond into the electrode material. A possible design tradeoff with such a design include interface imperfections, phonon-electron interactions in the conducting electrode, the stress mismatch between the thin dielectric film and the Si/PolySi body, and differing acoustic properties that may distort the resonant mode resulting in a lower Q.

Such electrostatic resonators consist either entirely of Si or PolySi with the optional dielectric film incorporated into the mechanical body, thus taking advantage of the cost-scaling of Si micromachining and the excellent mechanical properties of single

crystal silicon ($Q > 10,000$ at 1 GHz) [9]. This has led to high-Q low-cost resonators that have been extensively explored over the past two decades. The CMOS-friendly materials used in these resonators also makes them amenable to seamless integration with integrated circuit (IC) technology [11].

Piezoelectric transduction

On the other hand, resonators relying on the piezoelectric transduction mechanism incorporate piezoelectric materials such as AlN, ZnO, PZT, quartz etc. into their body, which may be excited into mechanical vibrations through the application of an AC electric field. Conversely, mechanical strain in piezoelectric materials also result in an electric displacement field and current for sensing of resonance. The details of the piezoelectric transduction mechanism are provided in appendix B.

Historically, piezoelectrically driven resonators have been preferred over electrostatic devices in commercial products due to their high electromechanical coupling coefficients resulting in a much lower insertion loss in the electrical output. One of the earliest examples of piezoelectrics used in commercial resonators is that of quartz crystals employed in microprocessor clocking circuits to generate high-Q resonance. At present, for frequencies of operation < 10 GHz, piezoelectric resonators (first SAW and now film bulk acoustic resonators or FBARs) have been successfully implemented in custom MEMS-only or MEMS-last processes which can then be wire-bonded to interfacing circuitry such as Avago's FBAR technology [12].

One of the key issues with piezoelectric devices such as FBARs is the inability to manufacture devices with several different resonance frequencies on a single chip as the frequency is determined by material thicknesses, and the inherently low Q of piezoelectric materials [9]. As a solution to the former, recent years have seen numerous examples of contour-mode piezoelectric resonators with lithographically defined frequency. In response to the latter problem of low Q of piezoelectric resonators, efforts have been made to fabricate Si-based piezoelectric resonators to boost the Q of the overall device which is now dominated by Si [6]. Another key problem with piezoelectric resonators is that several piezoelectric materials such as quartz, PZT

etc. are not amenable to CMOS integration due to the possibility of contamination of the front end of line materials or manufacturing difficulties. However, the excellent transduction efficiency and minimal insertion loss demonstrated by these devices allow for a commercially viable multi-chip solution, in spite of parasitics that invariably arise due to the presence of wire-bonding.

Both capacitively and piezoelectrically driven and sensed passive resonators may be modeled using a simple Butterworth-Van-Dyke model provided in appendix C (Fig. 1-1(b)).

1.1.2 Frequency scaling of passive resonators

Passive transduction schemes such as electrostatic or piezoelectric transduction have been traditionally used in the majority of MEMS resonators to date. However, as resonators scale to higher frequencies, the out-of-band rejection of the signal with respect to the feedthrough can be severely compromised, and cannot simply be mitigated by subsequent amplifier stages.

To illustrate this effect, we consider a dielectrically driven and sensed resonator with a resonant length L whose geometry can be realized using FEOL fabrication in an SOI CMOS process (Fig. 1-1(a)). The resonator's equivalent electrical circuit may be represented by a simple Butterworth Van Dyke (BVD) model (Fig. 1-1(b)) using an RLC branch and feedthrough parasitics. The drive and sense capacitors are modeled by C_0. This model has been traditionally used to model passive MEMS resonators and is included in appendix C.

For simplicity, we assume that all other dimensions (such as W), materials, the quality factor Q and the feedthrough capacitance C_f of such a device remain constant while only the length of the resonant cavity L changes as $1/f$ where f is the resonance frequency. Thus the shunt capacitor C_0 also reduces as $1/f$ since the non-resonant dimension is held constant. The motional resistance R_m scales as $W/C_0^2 f^2$ where W is the non-resonant dimension and hence remains constant with frequency in this configuration. Meanwhile the impedances of C_m and L_m cancel at resonance. Under these assumptions, the expected out-of-band rejection of the voltage gain from input

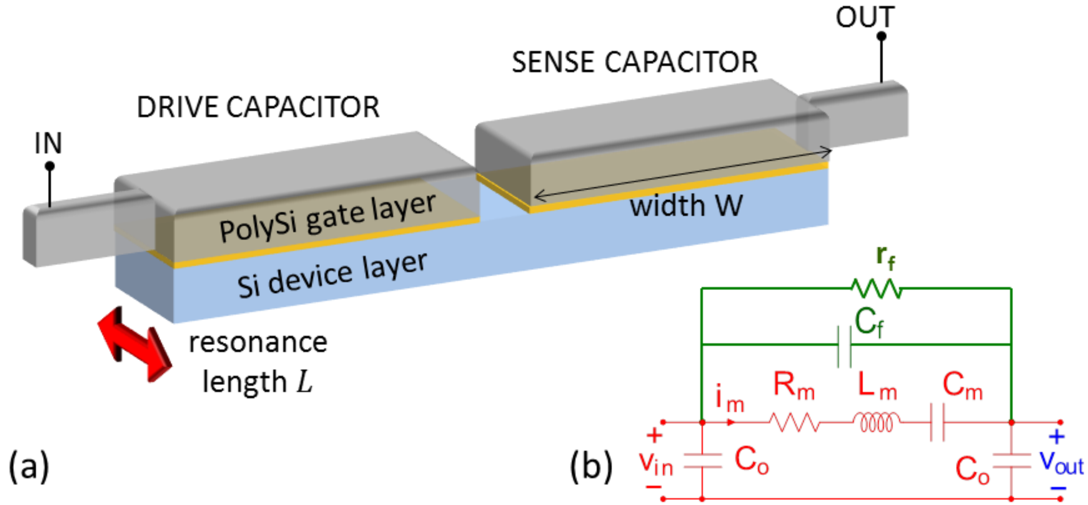

Figure 1-1: (a) Schematic of passive resonator driven and sensed capacitively with a resonance dimension L. (b) Small signal model of passive resonator showing motional RLC branch, shunt capacitors C_0 and feedthrough modeled by C_f.

to output reduces from $> 10\,\text{dB}$ at 100 MHz and to $> 0.1\,\text{dB}$ at 10 GHz. For such resonators, an in-line amplifier stage would indiscriminately amplify the resonance signal along with the feedthrough, thus providing no improvement in the out-of-band rejection.

One method to improve the out-of-band rejection of the resonator is by keeping the drive and sense area of such resonators constant with frequency by scaling the non-resonant dimension $W \propto f$ to retain the same effective shunt capacitance C_0. This leads to the overall feedthrough capacitance remaining constant at $C_0/2 \parallel C_f$ while R_m now scales as $1/f$, leading to a constant out-of-band rejection across frequencies for a standalone device. However, in system level integration, such resonators interface with driving and sensing CMOS circuits with an associated input and output impedance. At high frequencies, these large shunt capacitors C_0 result in large signal being shunted to ground through such low impedance capacitive paths. This results in strict constraints on the input and output impedances of interfacing circuits, which increases overall power consumption.

1.1.3 The Need for Active Sensing

While C_0 may be constrained by interfacing circuits, active sensing provides one solution to overcome the limits of out-of-band rejection by utilizing a more efficient transduction mechanism to amplify the mechanical signal before the presence of parasitics. In active resonant devices, an active element such as a transistor is usually provided to generate a current through the device which either excites vibrations or senses them. For instance, in thermally actuated resonators, a constant current running between two terminals of the device causes resistive heating and the resultant thermal expansion may be used to actuate mechanical resonance [13]. On the sensing side, mechanisms such as piezoresistivity may be used to sense vibrations in resonators as the strain in the device causes a change in electron mobility and modulates the DC current through it [7]. The phenomenon of piezoresistivity is discussed in detail in appendix D.

The small signal equivalent circuit of a capacitively driven, piezoresistively sensed resonator is provided in Fig. 1-2 , consisting of a 1-port passive BVD model and a modified transistor pi-model. The drive capacitor is represented by C_0 while the RLC components model the mechanical mass-spring-damper system of the resonator. The piezoresistive sensing is represented by a transconductance g_α. The integration of such an electromechanical amplification element into the resonant cavity enables improvement in the out-of-band rejection of the signal before the contribution of feedthrough parasitics modeled by the C_f and r_f. This model will be further developed in §2.4.

Two types of piezoresistive sensing mechanisms may be considered for Si-based resonators in a standard CMOS process. The first involves piezoresistive sensing using a resistive element [14] while the second involves piezoresistive sensing using a FET.

A detailed analysis of the performance of the FET-sensing versus resistive mechanisms in terms of gain and noise performance was carried out by Bichoy Bahr and included in [15]. Some important results from this analysis are discussed here.

We first consider a resonant structure which is sensed using a current path defined inside the resonant body. Mechanical strain at resonance piezoresistively modulates

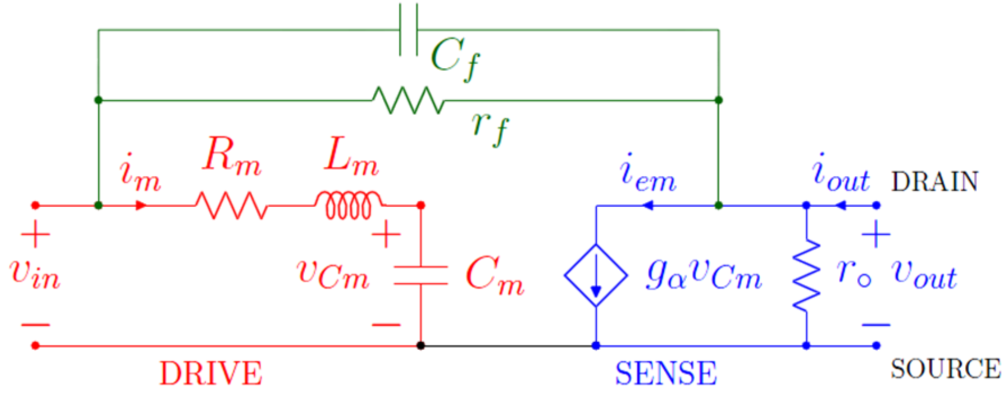

Figure 1-2: Small signal model of the RBT consisting of an RLC branch modeling the mechanical resonant system (red) and a modified transistor small signal model (blue). Lumped feedthrough parasitics (green) are modeled by C_f and r_f.

the resistivity in the current path. The stress and strain are both proportional to the resonator excitation voltage v_{in}. For a Si-based bulk acoustic resonator operating around 10 GHz, the sensing resistance R is limited to a few hundred ohms due to the length of resonant cavity.

Two techniques are considered to detect the piezoresistive modulation: *a*) constant current bias *b*) a Wheatstone bridge

- The simplest method to detect the variation in the sensing resistance is to bias it with constant current I as shown in Fig. 1-3(a) which gives a voltage gain A_v of:

$$A_v = IRg_R \tag{1.3}$$

  and an input referred noise PSD is considered.

$$\overline{v_{in}^2} = \frac{\overline{v_{on}^2}}{|A_v|^2} = \frac{4k_BT}{I^2 g_R^2 R} \tag{1.4}$$

  From 1.3 and 1.4, the low voltage gain and high noise of such an implementation is limited by the value of the sensing resistor which may not be increased arbitrarily due to area and noise considerations. Such a configuration can be considered as an equivalent current source with very small output re-

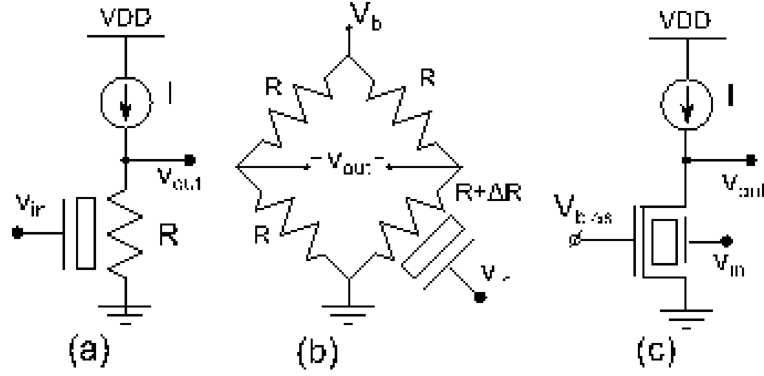

Figure 1-3: Schematic showing biasing scheme for (a) Resistively sensed resonator, (b) Wheatstone bridge configuration for piezoresistive sense transducer, and (c) FET sensed resonator. In all cases, the device is biased at a total DC current I and driven using a small AC voltage v_{in}.

sistance, which makes current sensing by a trans-impedance amplifier (TIA) a non-feasible solution due to the small input impedance required. Furthermore, the small resistance also restricts the DC operating point of the output node to be close to ground, presenting a limitation for the direct coupling of subsequent amplification stages.

- On the other hand, in a Wheatstone bridge configuration show in Fig. 1-3(b) shows an implementation of Wheatstone bridge, biased at V_b, the voltage gain A_v of which is given by:

$$A_v = \frac{1}{4} V_b g_R = \frac{IR}{4} g_R \tag{1.5}$$

where the total current consumption of the bridge $I = V_b/R$ has been used. Again, the input referred noise PSD is given by:

$$\overline{v_{in}^2} = \frac{\overline{v_{on}^2}}{|A_v|^2} = \frac{64 k_B T R}{V_b^2 g_R^2} = \frac{64 k_B T}{I^2 g_R^2 R} \tag{1.6}$$

Comparing 1.3 and 1.4 with 1.5 and 1.6, it becomes clear that, for the same bias current, the voltage gain of the Wheatstone bridge sensing is lower than the constant current biasing scheme of Fig. 1-3(a) and the $\overline{v_{in}^2}$ is higher.

An alternative to the approach above is the use of FETs for sensing of acoustic

vibrations. FET sensing relies on piezoresistivity as the dominant effect to modulate the mobility of carriers along the channel and result in a small signal output current. Secondary contributions to the current modulation include modulation in channel length, threshold voltage, gate capacitance and electrostriction are omitted for simplicity from the small signal model presented in Fig. 1-2 and will be discussed in section 2.4.

Consider a resonator with the same geometry as that of the resistive sensing resonator with the only variation being that of sense transducer. Mechanically, this device behaves identically to the resistively-sensed device and strain induced at resonance is related to the input voltage in the same manner. The magnitude of the relative change in the FET channel mobility $\Delta\mu/\mu$ due to piezoresistance is equal to the relative change in resistivity, but with opposite sign. Thus, assuming the FET is biased in saturation, the voltage gain is given by:

$$A_v = -Ir_0 g_R \tag{1.7}$$

Given the large output resistance of the FET, for the same mechanical structure and the same bias current, FET sensing thus has a voltage gain that is r_0/R higher than its resistive counterpart. For the devices considered in this work, this ratio is as high as 200.

For short channel devices, the thermal noise coefficient $\gamma \sim 1$ and for a transconductance g_{mFET} the input referred noise voltage PSD is given as:

$$\overline{v_{in}^2} = \frac{4k_B T \gamma g_{mFET}}{I^2 g_R^2} \tag{1.8}$$

Comparing the input referred noise PSD of both FET and resistive sensing, we have:

$$\frac{\overline{v_{in}^2}|_{FET}}{\overline{v_{in}^2}|_{Res}} = \gamma g_{mFET} R \tag{1.9}$$

For typical designs, g_{mFET} is a fraction of mS, such that the input referred noise of FET sensing is much lower than that of resistive sensing. For the ABR-RBT devices

considered in this work, g_{mFET} is of the order of $500\,\mu S$, resulting in an input referred noise for the FET of only 5% that of its resistive counterpart. Additionally, the acoustic wavelengths are on the order of 100 s of nm in GHz-frequency resonators, which limits the area of the sensing resistor but does not restrict FET output resistance. This makes the FET more suitable for higher frequency implementations which incorporate shorter wavelengths.

The downside of FET sensing comes from its higher power dissipation as compared to resistive sensing. When biased in saturation, the sensor FET consumes more DC power than the resistive sensor. For the ABR-RBT described in this work, designed for a bias current of $60\,\mu A$, and a drain voltage of $500\,mV$, the FET sensing power dissipation is more than 80× larger than the resistive sensing.

1.2 Actively sensed MEMS resonators

The concept of active FET-sensing in MEMS devices has been around since Nathanson's Resonant Gate Transistor in 1967 [16]. This resonator employed a gold cantilever suspended on top of a transistor channel. The voltage applied to this cantilever served as the gate voltage of this channel and any vertical motion of the cantilever modulated the capacitance and hence the output current of the transistor.

In more recent times, FET sensing has been demonstrated in Si up to 165 MHz in a double-ended tuning fork with 2 FinFETs [17] and up to 226 MHz in Si nanowire based resonators [18]. Resonant Body Transistors (RBTs) [19], [20] with internal dielectric drive and Field Effect Transistor (FET) sensing up to 37 GHz have also been previously demonstrated (Fig. 1-4). Transistor based sensing has also been demonstrated in piezoelectric GaN-based resonators, up to 2 MHz [21] and more recently , up to 3.5 GHz as switchable GaN resonators in metal-on-metal IC technology [22]. FET-sensing has thus been shown to reach order of magnitude higher frequencies than possible with passive resonators due to the decoupling of the drive and sense transduction mechanisms.

Active sensing in non-Si materials such as carbon nanotubes (CNTs) has been

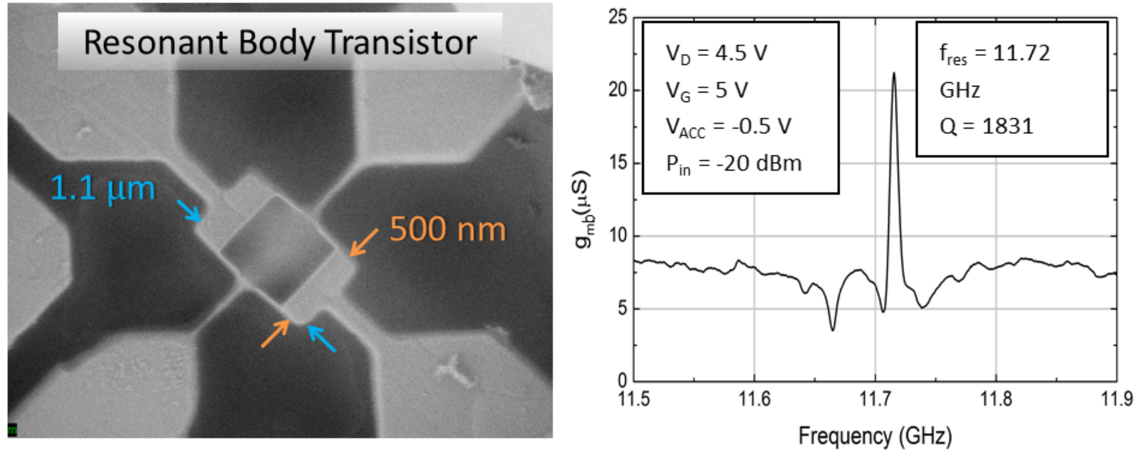

Figure 1-4: (left) Scanning electron micrograph of RBT showing gate length of 500 nm and resonant dimension $\sim 1\mu m$. (right) De-embedded frequency response of a resonant body transistor showing third harmonic resonance frequency of 11.7 GHz, with electromechanical Q of 1831 and piezoresistive transconductance of 22 μ S.

demonstrated with suspended CNT arrays used as the gate electrode for a transistor channel, known as CNT-SGFETs. Resonance frequencies of 120 MHz have been reported for biological and chemical applications such as single-molecule sensing [23]. The use of GaN high electron mobility transistors (HEMTs) with mechanically floating carbon nanostrings (NS) or CNTs serving as the floating gate have been demonstrated for detection of THz radiation modulated by mechanical resonance frequencies in the MHz or GHz range [24].

A separate class of devices with active piezoresistive sensing comprises of various geometries such as rings [25], disks [26] and bulk mode resonators [27]. Piezoresistive sensing has also been demonstrated in single-walled CNTs upto 79 MHz [28], in CMOS-MEMS resonators [29] and thermally actuated resonators up to 61 MHz [7]. Such piezoresistively sensed resonators have been employed for a variety of applications such as for gas recognition, pressure sensing [30] and biomolecular detection [26].

1.3 CMOS Integration of Vibrating Transistors

Due to the necessity of FET-sensed resonators for high-frequency operation, one direction to explore would be the design of MEMS resonators inside of the CMOS stack to access the high-performance, high-yield transistors available in the front-end-of-line (FEOL). Apart from the high yield of CMOS processes as compared to in-house, custom MEMS processes for transistor fabrication, the length scales of CMOS are also about $10-100\times$ smaller than in-house processes due to the availability of state-of-the-art tools and processes, which allow for scaling to higher frequencies. Furthermore, the integration of MEMS resonators with the CMOS stack leads to reduced parasitics from on-chip and off-chip routing for high frequency operation, smaller size and weight, and decreased power consumption by alleviating constraints for impedance matching networks [31], [32]. At present, a majority of electromechanical devices require a release step to freely suspend the moving structures. This necessitates costly complex encapsulation methods and restricts MEMS fabrication to back end-of-line (BEOL) processing of large-scale devices in CMOS. Thus, apart from the access to high-performance transistors, development of unreleased Si-based MEMS resonators in CMOS is a critical step towards seamless integration in CMOS with no post-processing or packaging.

However, such seamless MEMS-CMOS integration presents a number of challenges to the performance of the MEMS devices as well as the surrounding CMOS circuitry. Before the details of such challenges and constraints may be discussed, an overview of a typical CMOS process is presented followed by a discussion of MEMS, and specifically RF MEMS design in CMOS.

1.3.1 Overview of typical CMOS process

Due to the high cost of tools required in a state-of-the-art CMOS foundry, along with the fast turnaround times (based on Moore's law [33]), CMOS foundries have relied on process standardization and design to deliver high-yield and reliable IC technology. While several different materials and fabrication techniques are theoretically

possible in each part of the process, the customer is typically restricted to a few reliable designs for active and passive components whose reliability and functionality is guaranteed by the foundry. Whereas traditional CMOS processes have used bulk Si as a starting material, as the industry moves towards smaller devices, increased transistor capacitance and feedthrough has forced the introduction of Si on insulator (SOI) substrates. In an SOI wafer, the active or device layer is separated from the bulk or handle wafer by a layer of buried oxide (BOX) which helps to electrically isolate adjacent devices which in turn lowers the parasitic leakage capacitance and current to save power with the trade-off of increased substrate cost.

Regardless of starting substrate, a typical CMOS process is divided into two sections, the Front-End-of-Line (FEOL) and the Back-End-of-Line (BEOL) process flow. The FEOL forms the first few layers that are manufactured in a CMOS process which typically form all semiconductor devices in a circuit such as transistors (Field effect transistors or FETs and bipolar junction transistors or BJTs), diodes, resistors, capacitors (such as MOSCAPs, deep trench capacitors) etc. The BEOL includes the fabrication of metal interconnects and vias along with certain passive components such as capacitors (in the form of MIMcaps) and inductors.

The key differences between the FEOL and BEOL are in terms of the materials used and the processing temperatures that result from this material choice. As a very brief description, the typical FEOL process flow involves selection of a silicon substrate, i.e. specifying starting wafer type (bulk versus SOI), orientation, doping, wafer size, wafer flatness etc. Following this, the gate regions are typically patterned along with optional shallow trench isolation (STI) structures. This is followed by the definition of active regions, p and n wells, by ion implantation. After this step, the gate dielectric and gate polysilicon/metal are grown or deposited based on the exact materials used. The gate as well as source/drain regions are defined by ion implantation. At this stage, the transistor in itself is complete but disconnected and hence the next step is that of creating silicide to connect the gate and source/drain regions to metal interconnects. Stress liners may be deposited following this step for controlling channel mobility, especially for short channel length, high-frequency

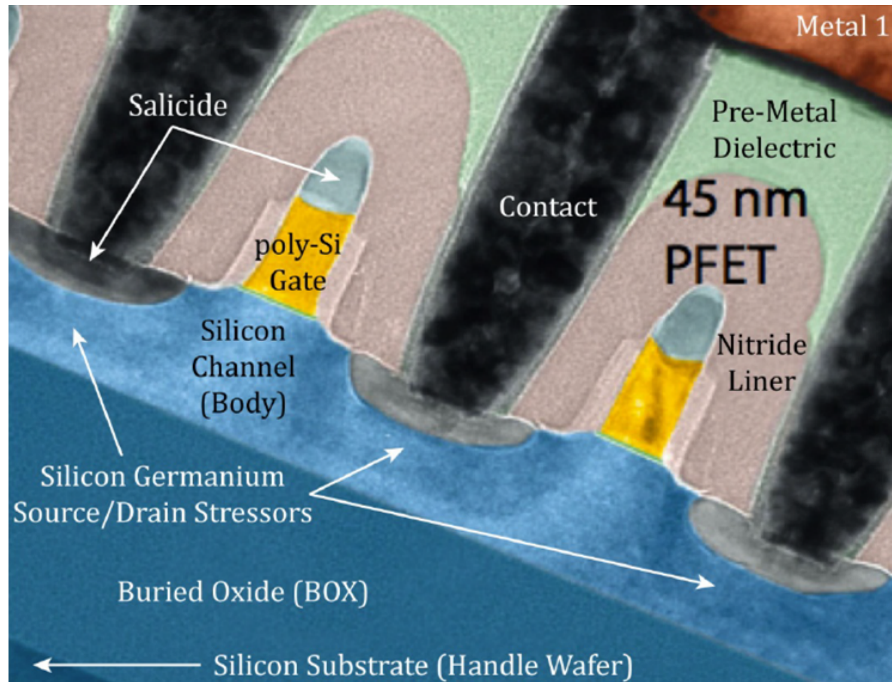

Figure 1-5: Scanning TEM of FEOL stack from IBM's 45nm SOI process showing adjacent FETs with stress liners, pre-metal dielectric, silicide and contacts. False coloring used [1].

devices. A TEM image of the FEOL stack for IBM's 45nm process is included in Fig. 1-5.

Thus, these FEOL processes typically use materials such as silicon in the device layer; silicon dioxide (or high-k dielectrics) as gate dielectric, or in electrical isolation structures such as the buried oxide (BOX) layer and STI; polysilicon/metal for FET gates; silicide for forming ohmic contacts; silicon nitride as stress liners etc. Temperatures in the FEOL typically reach $> 1000\,\mathrm{C}$ for annealing and activation of dopants, deposition of materials such as PolySi.

The final steps in a CMOS process, also called BEOL, involve the deposition and patterning of various levels of metal interconnects composed of metals such as Cu/W/Al, connected by vias or metals such as Cu/W and electrically isolated from adjacent connections by low-k dielectrics. Al has been traditionally used to form interconnects as Cu was not patternable through the traditional lithography and plasma etch processes due to the lack of volatile Cu compounds. The damascene or additive patterning process was devised to pattern Cu as it has better conductivity

than Al, thus reducing resistive losses. As part of the damascene process, efforts are made to planarize the metal to avoid problems with thickness of metal on non-planar topography, development of “opens” and difficulty with photolithography. Chemical Mechanical Polishing (CMP) is introduced and a certain level of via and metal pattern density is maintained to aid the planarization process. Processing temperatures are not increased beyond 450 C in the BEOL process flow to avoid diffusion of the metal layers. Fig. 1-6 shows a cross-sectional SEM of a typical BEOL stack.

It is worth noting here that a barrier metal layer is required to completely surround Cu interconnects to prevent diffusion of Cu into Si which may cause deep-level traps and compensate the dominant charge carrier type by annihilating free electrons or holes. While the thickness of this barrier metal often takes away the improvements in conductivity that Cu provides over Al by reducing its cross-sectional area, Cu brings an additional benefit over Al: electromigration resistance. Electromigration is the process by which ions are transported in a conductor due to momentum transfer between electrons and metal ions and is relevant in applications with high current densities. Cu has about $5\times$ the electromigration/current density limit as Al due to higher electrical and thermal conductivity and melting point.

Additional details on the CMOS process flow may be found in any standard electronics/CMOS fabrication textbook [34].

Typically CMOS foundries provide several rules (known as the design rule check or DRC) that dictate the permissible layout, pattern density, critical dimensions and overlap etc. to ensure high yields for the designed process. For instance, a typical design rule file does not allow for: a transistor to be formed on the same device “island” as a capacitor, only the source or the drain of a MOSFET to be populated with vias, changing the dimensions of provided deep trench capacitors, and removing dummy gate stacks etc. For the purposes of MEMS design, engineers often need to make such modifications based on the optimized mechanical design at the risk of unknown yields and compromised performance of the resulting design. MEMS designers typically need to provide a list of all DRC rules being violated by a particular design for foundry approval before the wafers may be processed to ensure

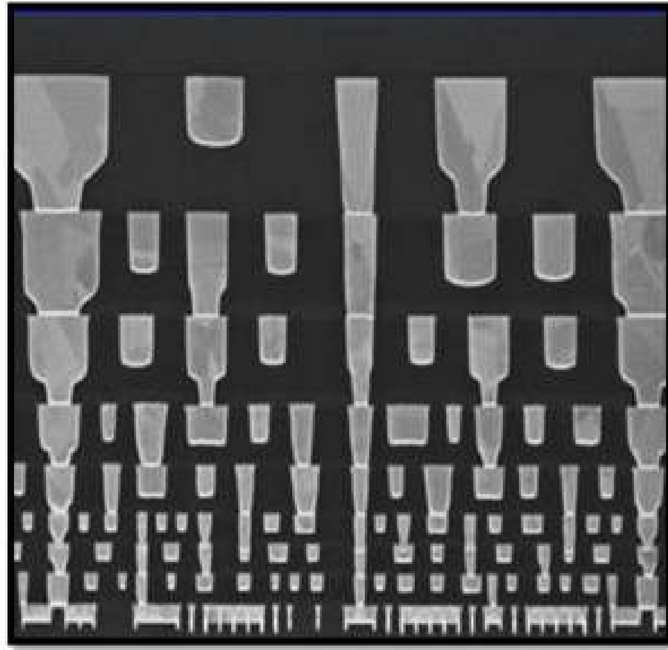

Figure 1-6: Cross-section of Intel's 32nm process BEOL stack showing metals and vias on a background of insulating dielectric. Source: Intel.

that the yield and performance compromise does not propagate across the wafer. To this end, the DRC rules most amenable to modification include changes in layout of individual transistors, vias and routing, while those least amenable to modification include changes in pattern densities and changing dimensions of deep etches which may lead to crack propagation through the wafer. It is also noted that having several DRC modifications essentially renders it pointless - in such a scenario, it is best to create an extended DRC set for the MEMS design to catch inadvertent errors in the complex MEMS designs.

1.3.2 Co-fabricating MEMS with CMOS

The integrated CMOS process flow, originally developed for electronics, has been adopted for a wide variety of MEMS devices including imagers, inertial sensors, chemical and biological sensors, actuators for switching, and filters [31]. There are several incentives for integration of MEMS with CMOS including but not limited to: reduced packaging and chip-pinout requirements, lower weight and cost as compared to multi-

chip solutions and improved shielding from electromagnetic interference. On the other hand, the drawbacks to such an integration typically present in the form of complicated manufacturing, increase process complexity, restricted material choice, lower yield and higher cost per wafer. Furthermore, integration can lead to compromised performance of both the MEMS and the electronics.

CMOS-based MEMS devices are broadly classified into two categories, MEMS-first devices and MEMS-last devices. The pros and cons of each approach are considered below with some examples.

MEMS-first devices

In some cases, the MEMS sequence, or most of it, is completed prior to the CMOS transistor and metal stack formation and is known as the MEMS-first fabrication sequence.

One of the first few devices fabricated in the FEOL stack include pressure sensors [35] and neural probes [36]. The pressure sensors were fabricated as micro-diaphragms which were released by anisotropic etching of the backside of a wafer [37]. In recent years, the availability of SOI wafers has enabled preprocessing wafers using DRIE and trench fill followed by planarization to create microstructures before sending wafers to the foundry. After the completion of the CMOS process, the microstructures are defined with a second DRIE process and the BOX is released (Fig. 1-7). In such cases, wafer acceptance by foundries may be an issue due to the substantial pre-processing. Also, with such an approach, transistors need to be protected during the final release step of the MEMS in HF or BOE.

More recently, MEMS-first devices have been released and encapsulated prior to the CMOS process flow using LPCVD oxide or PolySi films to seal release-etch holes, to achieve complete modularity [38]. However such a technique suffers from increased mask count and process complexity resulting from the fully independent MEMS process flow which does not take advantage of the CMOS foundry. Resonators encapusulated by this method have demonstrated stable performance, promising applications in timing and inertial sensing.

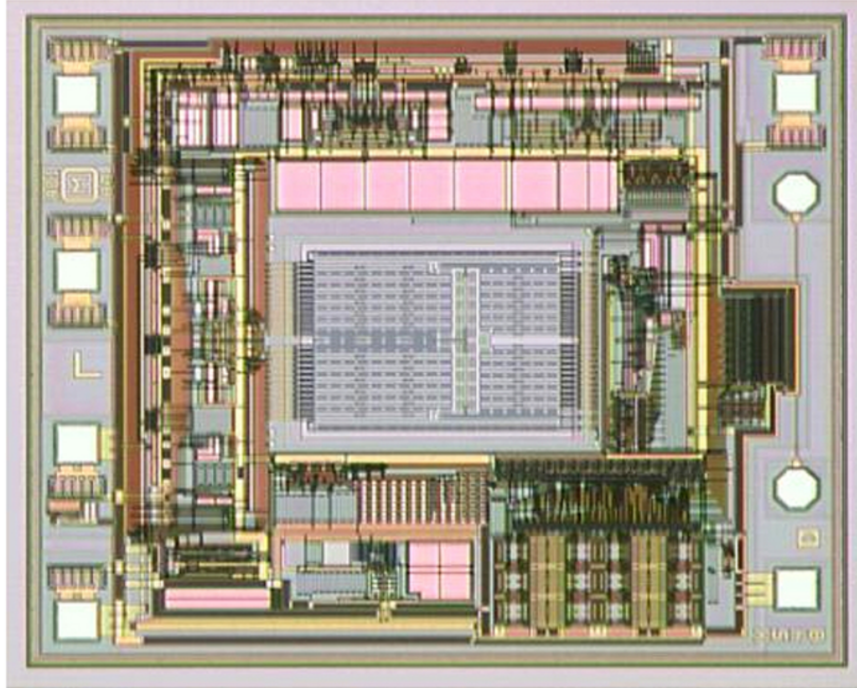

Figure 1-7: A SOI-MEMS accelerometer formed by MEMS-first creation of microstructures on an SOI substrate followed by the CMOS process flow. Source: Analog Devices Inc. [2].

Thus, MEMS-first devices are typically designed in the front-end-of-line (FEOL) stack with access to high performance materials with a high thermal budget such as silicon, polysilicon, silicon nitride, silicon oxide and high-κ dielectrics. However, the release etch typically required by such devices at the end of the CMOS process can significantly affect the performance and yield of the surrounding circuitry while increasing overall process complexity [11].

MEMS-last devices

On the other hand, MEMS-last devices are usually fabricated in the back-end-of-line (BEOL) of the process, after the transistor stack is fabricated, making the release step easier and decreasing the overall chip footprint due to vertical stacking [2]. However, inspite of its modularity, MEMS-last processes are restricted to the BEOL material stack, comprising of low-Q porous or amorphous materials such as metals and low-κ dielectrics which intrinsically have higher thermoelastic and material losses. Further-

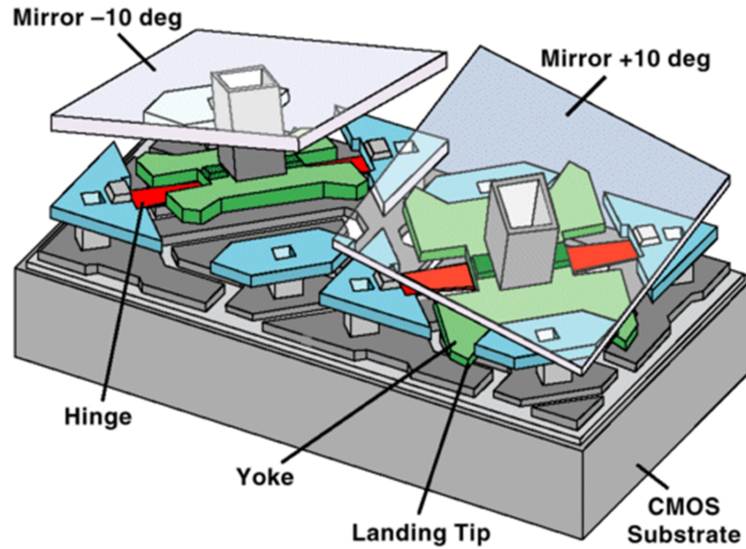

Figure 1-8: Schematic of TI's DLP showing structures in three Al layers to create a rotating mirror display. Source: http://celluloidjunkie.com/2010/03/26/texas-instruments-on-track-with-4k/.

more, the thermal budget is constrained as it has to be tolerated by the underlying electronics. While the transistors themselves can withstand thermal processing a long as the diffusion of dopants is accounted for, thermal stresses can significantly affect the resistance and electromigration limits of the metals and vias. Another constraint for BEOL processes is that conventional passivation materials such as PECVD SiN and polyimide are etched by HF, making SiO_2 unusable as a sacrificial layer. Thus, both the materials and the thermal budget limit device performance and maximum resonance frequency in MEMS-last devices.

One of the most prominent and commercially successful examples in this category of MEMS-last devices is the digital light processor (DLP) by Texas Instruments. This structure is fabricated as three layers of Al-based films for the mirror and its suspension system using resist as a sacrificial layer on top of an FEOL stack. Fig. 1-8 shows a schematic of the DLP with its hinged microstructure.

Another class of MEMS-last devices includes those fabricated on top of a complete CMOS die in a separate custom MEMS process [12], [5]. Such an approach can reduce system footprint and introduce non-CMOS materials, but is subject to increased process complexity and cost from additional masks along with the constrained thermal

budget.

1.3.3 RF MEMS in CMOS

Several RF components such as switches, high-Q inductors, variable capacitors and resonators have been integrated into CMOS in an attempt to remove off-chip bulky passives, reduce noise and scale to higher frequencies in RF architectures [39]. As one of the RF MEMS components, RF MEMS switches have been shown to have significantly better insertion loss, isolation, standby power and linearity as compared to their semiconductor counterparts such as PIN diodes and GaAs FETs [40], [41]. These are usually fabricated as post-CMOS devices in a low-temperature process and the first commercial applications have been shown by Motorola [42] and ST Microelectronics [43].

RF tunable capacitors, typically using electrothermal actuation [44], and high-Q inductors, usually as suspended structures using metallization layers [45], have also been demonstrated for applications in tunable filters, voltage-controlled oscillators (VCO) and resonators. At higher frequencies, transmission line-based resonators have been demonstrated as 37-GHz and 60-GHz multi-pole filters [46] in the form of monolithically integrated devices in a CMOS process.

The inherent resistive losses in such transmission-line based resonators limit the Q-factor as compared to mechanical resonators. Integration of mechanically vibrating resonators with CMOS was first demonstrated by Nguyen and Howe fabricated using a CMOS plus surface micromachining technology [47]. An SEM of this device along with the frequency response is included in Fig. 1-9. Since then, most CMOS-integrated designs have been in BEOL processes, focused on electrostatic actuation based on the choice of materials available in CMOS. Performance improvements have been achieved by mechanical coupling to reduce feedthrough, and reduced electromechanical gap for high-efficiency actuation.

The FBAR commercialized by Avago may also be classified as a related architecture, though it is not directly integrated into CMOS technology. These resonators are fabricated as parallel-plate capacitors with a piezoelectric layer sandwiched in between

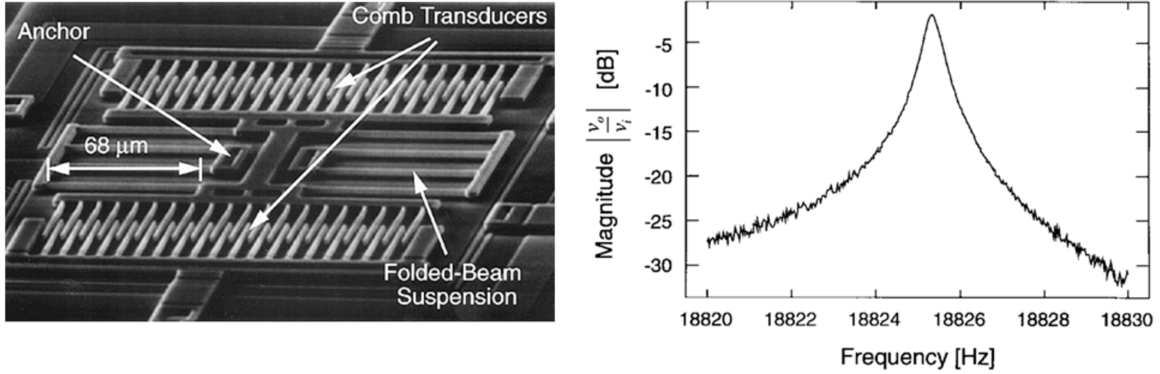

Figure 1-9: (left)SEM of CMOS-integrated MEMS resonator showing electrostatic actuation. (right) Frequency response showing $Q > 50,000$ at 18 kHz.

and are assembled in a custom MEMS-first process to interface with a CMOS-VCO [48].

At this point, it is worth discussing the design tradeoffs for RF MEMS design in FEOL versus BEOL. For a fully integrated MEMS design that utilizes CMOS materials and fabrication processes, the FEOL stack provides significantly more challenges that the BEOL stack in terms of design flexibility. Several design rules such as dimensions of transistor islands and gates, spacing and overlap between vias and source/drain regions, pattern densities, proximity of doping regions to transistors and isolation trenches, number and position of contacts etc. are tightly controlled in the FEOL to achieve best possible transistor performance in terms of speed, power and reliability. For instance 2-4 dummy gates are patterned at a fixed distance around the smallest gate length transistor to maintain pattern density in the gate layer and ensure accuracy in gate length fabrication. While these gates are electrically disconnected and do not affect transistor performance, they can affect the MEMS performance by changing the mode shape for a resonator designed in these layers. However, removing them is a design rule violation with risk to reliability of transistor performance. Thus, while several high-Q materials are available to the designer, DRC constraints severely restrict the design space in the FEOL.

As compared to the FEOL stack, the BEOL design rules are more flexible and restricted to via sizes, minimum spacing and minimum metal line widths (restricted

by both lithography and electromigration). One of the few constraints in the BEOL include the overlap between vias and metal lines as they are filled in a single step as part of the dual-damascene process. Overall, a much wider design space is available for patterning the materials in this part of the CMOS flow.

One approach to address the afore-mentioned challenges of integration is the design of MEMS resonators in FEOL CMOS which can be realized without any post-processing or packaging. The unreleased nature of these resonators avoids extra complexity and cost, with the added benefit of increased robustness in harsh environments. In this work, IBM's 32SOI process was chosen for its high f_T transistors, the manufacturability of small feature sizes down to $< 60\,\mathrm{nm}$ and the presence of the buried oxide (BOX) layer for acoustic localization of vibrations in the Si device layer.

Two constituent building blocks are required for the development of embedded high-frequency CMOS-integrated resonators: (i) A Si-based transducer operating efficiently in the GHz frequency regime, and (ii) a solid-state mechanism to confine acoustic vibrations within the resonant cavity in a completely unreleased environment using CMOS compatible materials. The above challenges are addressed by CMOS-integrated RBTs using FET-sensing with dielectric drive and FET sensing. Acoustic isolation structures are created in the form of acoustic Bragg reflectors (ABRs) and phononic crystals (PnCs).the pre-existing layers of the CMOS stack (Fig. 1-10).

1.4 Active sensing in Piezoelectric Resonators

As transistor technology continues scaling to the deep sub-μm range driven by Moore's Law, transistor threshold frequencies have increased, enabling transceiver circuitry to be designed in the tens of GHz range. The released and unreleased resonant body transistors discussed above [19], [20] have been explored in this thesis as candidates for side-by side integration with transceiver circuitry in a standard CMOS process using gate dielectrics for actuation and high-f_T FETs for sensing. However, the impedance of such devices is still orders of magnitude greater than those of piezoelectric devices due to the low transduction efficiency of electrostatic actuation as compared to

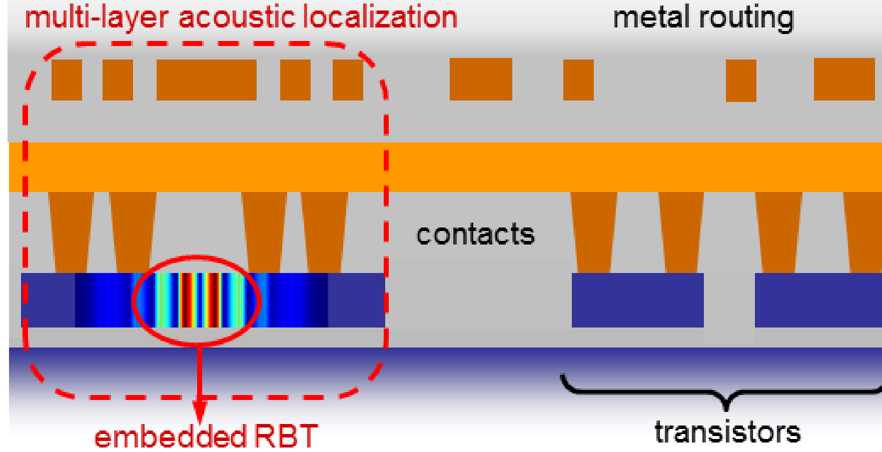

Figure 1-10: Schematic showing fully CMOS integrated resonant body transistor formed side-by-side with transistors in a standard CMOS process. Acoustic isolation is provided by pre-existing materials in the CMOS stack in the front and back-end-of-line.

piezoelectric actuation. Quantitatively, the driving forces for electrostatic actuation are $10 - 100\times$ smaller than piezoelectric driving forces for films of the same physical dimensions, being driven with the same voltage. On the sensing side, piezoelectric films induce an additional gate voltage at the FET gate which causes a modulation in the DC drain current at resonance in addition to piezoresistive sensing, further increasing the transconductance and reducing their motional impedance [49]. As a result, devices using piezoelectric transduction with active sensing have been demonstrated in the multi-GHz range with low impedance values due to the high coupling coefficients of piezoelectric materials [17], [21].

While piezoelectric materials have not been traditionally available in standard CMOS processes, recent years have seen some push in this direction for memory and switching applications and for improvements in transistor performance. One instance of this includes GLOBALFOUNDRIES which now offers an AlN on CMOS process as a BEOL process for fabrication of MEMS and other devices. IBM's Piezotronics effort uses the piezoelectronic transistor (PET) which is proposed as a device using a relaxor piezoelectric such as PMN-PT (lead magnesium niobate-lead titanate) in conjunction

with a piezoresistive material such as SmSe with a high piezoresistive coefficient [50], [51]. In operation, a voltage applied on the piezoelectric film induces a squeezing stress on the piezoresistive element, driving an insulator to metal transition by a change in conductivity spanning several orders of magnitude for switching applications.

Yet another application for CMOS integration of piezoelectric materials is that of memory applications using ferroelectric materials, called ferroelectric random access memory (FeRAM/FRAM) [52]. Ferroelectric materials such as $BaTiO_3$ and lead zirconate-lead titanate retain their polarization state after an applied electric-field is removed and this remnant polarization may be used to encode binary states in a data storage cell which has been demonstrated by shown by Texas Instruments [53] and Fujitsu [54]. More recently, ferroelectric materials have been used in negative capacitance structures stabilized by the presence of a dielectric layer with potential applications for improving transistor efficiency in the subthreshold regime [55]. Since all ferroelectric materials also show piezoelectric properties, the integration of such materials into CMOS leads to the possibility of fully CMOS-integrated piezoelectrically actuated and sensed MEMS resonators.

Since such piezoelectric materials are not commonplace in standard CMOS processes yet, the design and analysis of a piezoelectric resonant body transistors (which are architecturally similar to the devices from [19]) is explored in this work for an in-house process with potential for CMOS integration. Given the vision of CMOS-integration of these piezoelectric materials, high efficiency piezoelectric materials such as PZT which are not CMOS-friendly have not been considered in this work. Instead, the piezoelectric RBT in question is analyzed as a device that employs piezoelectric films such as AlN in the place of the dielectric in the configuration of an RBT. Some of the possible merits of such a configuration include:

- Improved drive and sense efficiency due to presence of high k_{eff}^2 piezoelectric material as compared to electrostatically driven RBT. The resulting driving forces are $10 - 100\times$ greater than those in dielectric films of similar physical dimensions.

- Such a device with sidewall piezoelectric materials will also have higher k^2_{eff} as compared to lateral drive devices due to higher value of in-plane piezoelectric coefficient. Sidewall deposition of AlN films with excellent c-axis orientation has only been demonstrated recently [56] and can be used to drive such in-plane vibrations. Overall, this results in improved R_m or insertion loss with respect to laterally driven piezoelectric devices.

- Piezoelectric resonators fabricated with loss materials such as piezoelectrics (AlN, ZnO) and electrode materials (Mo, Al) show a reduced Q factor as compared to electrostatically driven devices which use low loss Si. Piezoelectric devices which incorporate Si into the resonant cavity have been demonstrated to show improved quality factor Q and power handling capability over traditional designs [6]. This will be discussed further in chapter 5.

- High k^2_{eff} results in a large electromechanical signal in piezoelectrically transduced RBTs. These devices are hence no longer restricted to small signal behavior, allowing for non-linear behavior arising from switching of the transistor between different regimes such as cut-off, linear and saturation.

1.5 Conclusions and Overview

In conclusion, various passive transduction mechanisms such as electrostatic and piezoelectric actuation and sensing have been used in a majority of MEMS resonators to date. Such passive transduction mechanisms do not allow for scaling of these resonators to high frequencies due to the increasing parasitic feedthrough as resonator dimensions scale down for high-frequency operation. FET-sensing using resonant body transistors or RBTs, has been recently demonstrated to reach atleast an order of magnitude higher frequencies than possible with passive resonators due to the presence of a more efficient sensing mechanism in the form of piezoresistive sensing in the resonant cavity. Such RBTs may benefit from integration into a standard CMOS process to take advantage of the high-f_T, high-yield transistors for scaling to

multi-GHz frequencies.

This work focuses on the design of such CMOS-integrated RBTs envisioned as fully unreleased structures designed in the front and back-end-of-line in a CMOS stack without any modification to the process flow. A standard CMOS stack may contain materials such as dielectrics which may be used for electrostatic actuation of mechanical vibrations. Monolithic integration of such resonant body transistors into the CMOS stack is approached by designing the resonant cavity in the front-end-of-line to take advantage of the availability of transistors, and high quality, high stability, thin dielectric materials in the gate stack with small lithographic dimensions for improved frequency scaling. Acoustic confinement structures such as acoustic Bragg reflectors (ABRs) and phononic crystals (PnCs) are proposed using already available materials in the FEOL and BEOL CMOS stack to confine mechanical energy to the resonant cavity for high Q and suppression of spurious modes.

Devices fabricated in IBM's 32nm SOI technology realized without any post-processing or packaging will be demonstrated with frequencies upto 11.1 GHz with quality factors upto 252. Small signal model parameters will be extracted, and the effects of design variations and fab-induced variations on the performance of these devices in terms of input-to-output transconductance, g_m, and quality factor, Q, will be discussed. Temperature compensation arising from the complimentary temperature coefficients of $SiSiO_2$ in the resonant cavity will be experimentally and theoretically verified.

Recent years have seen a push towards integrating materials with piezoelectric properties into the CMOS stack which allow the design of improved transduction efficiency devices by using piezoelectric actuation and sensing in place of electrostatic actuation. The performance improvements in terms of effective motional impedance R_X expected from introducing piezoelectric films such as AlN into RBTs will be explored with the possibility of CMOS integration. The details of the physics of such a transduction mechanism are included with some possible designs which include mechanical coupling and differential drive and sense to obtain spurious free resonance responses with further improvements in transduction efficiency. Finally, a possible

extension of this work is discussed for performance improvements in next-generation dielectric and piezoelectric-based CMOS-RBTs for fully monolithic filter and oscillator design.

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Chapter 2

ABR-RBTs in CMOS: Design and Modeling

Monolithic integration in CMOS dramatically reduces parasitics, power consumption and footprint of MEMS resonators and allows us to leverage high performance transistors in a high-yield technology to enhance resonator efficiency for multi-GHz operation. Electrostatic transduction is the optimal choice for low-power resonators fabricated in CMOS due to restricted material selection. However, passive electrostatic resonators are subject to large feed-through capacitance, making it difficult to reach multi-GHz frequencies. The Resonant Body Transistor (RBT) addresses this obstacle by employing active FET sensing of acoustic vibrations.

Active FET sensing has superior gain and noise performance as compared to passive sensing mechanisms, while being insusceptible to cavity length restrictions imposed at high frequencies as discussed in section 1.1.3. Using the high quality of the gate dielectric, the ABR-RBTs designed here are driven electrostatically and sensed using a body-contacted analog nFET (Fig. 2-1). Realization of the RBT in CMOS technology leverages high-performance, high-yield transistors enabling RF-MEMS resonators at orders of magnitude higher frequencies than possible with passive devices.

Structurally, the drive capacitor consists of PolySi and a p-doped or n-doped single-crystal silicon (SCS) device layer acting as capacitor plates with the interfacial

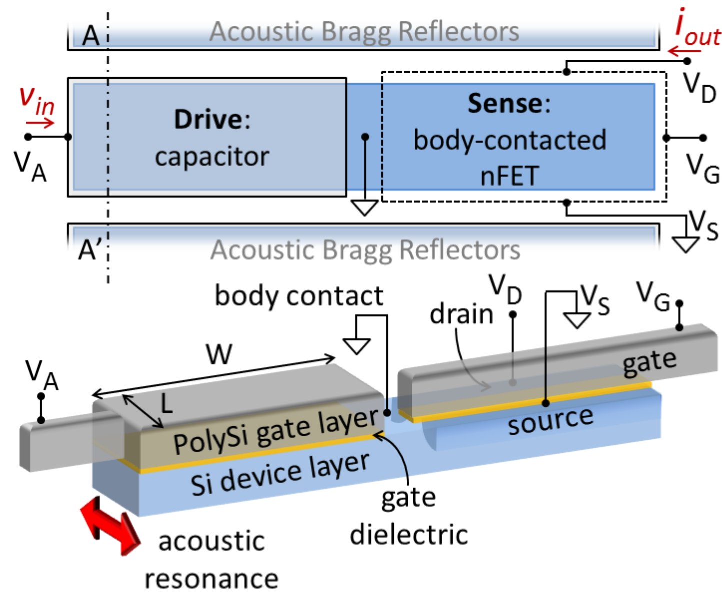


Figure 2-1: Top and 3D views of Si-based CMOS-MEMS resonator excluding acoustic Bragg reflectors (ABRs). The resonator is driven capacitively on the left, and sensed through piezoresistive modulation of the nFET drain current on the right. Details of FET layout and doping layers are not shown.

oxide layer between them. On the sense side, a foundry-provided nFET is modified to incorporate it within the resonant cavity along with the drive capacitor on the same device layer.

2.1 Acoustic Bragg Reflectors

The principle of acoustic Bragg reflectors (ABRs) is used to define the acoustic cavity of the unreleased resonators. ABRs consist of alternating materials with mismatched acoustic impedance patterned around the resonator, resulting in reflection of a majority of the acoustic energy back onto the resonant cavity. In the case of longitudinal waves, the acoustic impedance Z_{ac} is defined in terms of the elastic constant c_{11}, the acoustic velocity c_l, the effective Young's modulus of the cavity E, the Poisson ratio

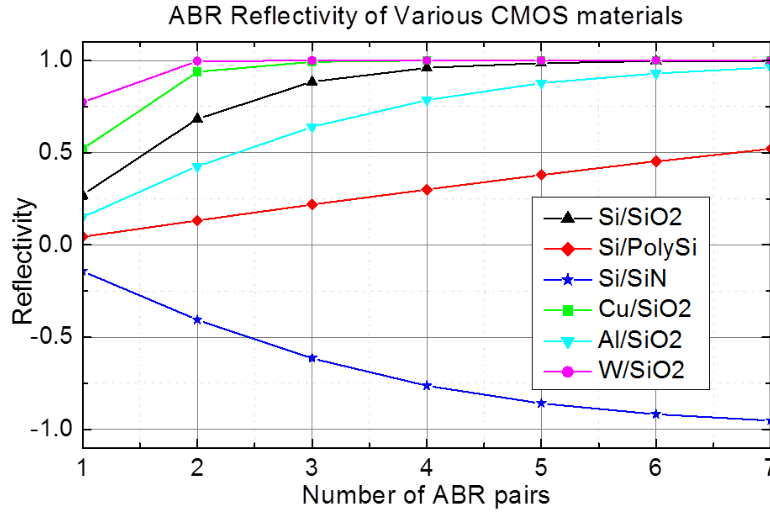


Figure 2-2: Comparison of the acoustic reflectivity of various ABR material pairs. For finite number of ABR pairs, the reflectivity increases with the number of pairs and converges to 1 or -1 rapidly for materials commonly found in CMOS.

ν and mass density ρ as

$$Z_{ac} = c_{11}/c_l = \sqrt{\frac{(1-\nu)\rho E}{(1+\nu)(1-2\nu)}} \tag{2.1}$$

The resultant reflection coefficient along any surface when each of the materials contains a quarter wavelength ($\lambda/4$) or odd multiples of a quarter wavelength at the resonance frequency is given by $R = (Z_1 - Z_2)/(Z_1 + Z_2)$. The net reflectivity increases with the number of reflecting surfaces; every pair of alternating materials can be considered one pair of ABRs. The acoustic mismatch offered by various combinations of materials from the CMOS stack is considered for the design of ABRs (Fig. 2-2).

Unreleased resonators have been previously demonstrated as solidly mounted devices using acoustic Bragg reflectors (ABRs) [57]. This concept may be extended to fully buried CMOS resonators using the BEOL layers such as routing metals and inter-metal dielectric for design of ABRs in the vertical direction. However, this scenario suffers from the following problems: (i) BEOL layer thicknesses are process-determined and are not available as a design parameter. (ii) Vertical ABRs preclude

the design of lithographically-defined resonant modes and frequencies, restricting the whole wafer to a single resonance frequency and its harmonics. (iii) High variability in BEOL layer thicknesses as compared to lithographically defined dimensions results in variable center frequency and reduced yield.

As one solution, Si/SiO_2 was chosen as the material combination for ABRs in this work as aforementioned materials occur in the Shallow Trench Isolation (STI) features offered in IBMs 32SOI technology to electrically isolate adjacent transistors. The dimensions of the STI fill are lithographically defined, allowing the design of multiple laterally confined resonant modes on a single wafer. The acoustic impedance mismatch between Si and SiO_2 is $Z_{rel} = Z_{Si}/Z_{SiO2} \sim 1.65$ and the resultant reflectivity achieved using 7 pairs of ABRs is 99.4% based on 1D analysis [58].

2.2 Design of Unreleased Resonator

In order to realize an unreleased acoustic resonator, a resonant cavity is specified using ABRs to define its boundary conditions. The resonant cavity is designed to be of length L and is formed by the gate stack consisting of the Si device layer, gate dielectric and gate PolySi. It is designed at an effective acoustic wavelength of $\lambda/2$. This is surrounded by ABRs consisting of alternate islands of SiO_2 and the gate stack, each designed at a length of $\lambda/4$ corresponding to its acoustic velocity. At resonance, longitudinal acoustic vibrations are set up in the resonant cavity and surrounding ABRs (Fig. 2-3). The eigenmode is comprised of a sinusoidal standing wave is formed in the resonant cavity which decays exponentially in the ABR region.

The first ABR is placed at a three quarter-wavelength ($3\lambda/4$) distance from the resonant cavity based on DRC restrictions. This affects the reflection solid angle and consequently the quality factor Q of the resonator. The mode shape and amplitude of vibrations U_0 of this unreleased resonator can be calculated using the model for damped vibrations in dielectrically driven released bar resonators [59]. This analogy is true under two assumptions:

- Each of the ABRs is designed at an odd multiple of a quarter wavelength. This

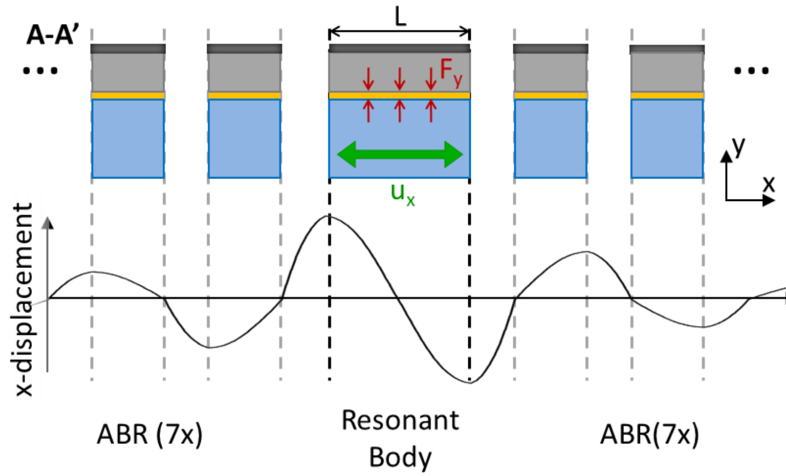


Figure 2-3: Cross section view of resonant cavity with surrounding ABRs. The capacitive force is applied along the y-axis across the gate dielectric on the drive side of the resonator. Acoustic vibrations are excited in the resonant cavity along the x-direction through the Poisson effect and decay exponentially as a function of length along the ABRs.

ensures no phase change occurs at the ABR boundary and so that it behaves like a free or fixed boundary condition.

- The aspect ratio of the structure is large, so that it can be approximated using a one-dimensional model, i.e. the wave leakage through the top and bottom is negligible.

Considering only transmission losses through ABRs in a purely 1D model, this method predicts Q around 7500 for 7 pairs of ABRs. However the small aspect ratio of the STI structures, the tapered angle of the SCS etch, reflections along the vertical direction, additional materials in the CMOS stack such as salicide, stress liners, metal contacts etc. result in distortion of the 1D mode necessitating 2D and 3D treatment for mode optimization.

In the course of design of the resonators, several structural aspects of the foundry-provided nFETs are modified. Standard FET doping layers which define the source, drain and body doping were changed to allow ABRs to be designed as close to the devices as possible. The shapes of the active device region of the SOI process and

Table 2.1: Design parameters of CMOS-MEMS RBTs fabricated in the IBM 32nm SOI CMOS process, shown in Fig. 2-1.

Parameters	Value
Length(resonance dimension) (L)	360nm
Width (W)	2.5μm
# ABR pairs	7
Device footprint (including ABRs)	3μm $\times$ 5μm
Capacitor doping	p or n-type
FET type	body contacted nFET
FET W/L	10.3

PolySi gate regions were modified to create longitudinal bar like structures for definition of the resonant cavity. The number of metal contacts was reduced to reduce distortion of the resonant mode of vibrations. A summary of the resonator design parameters is provided in Table 2.1.

A consideration for CMOS based tapeouts is the cost and turnaround times associated with every chip which limits the number of devices that may be prototyped on each chip. Typically, this number is restricted by the large probe pads (3 pads each for input and output, each pad of size $60\mu m \times 100\mu m$ with a pitch of $150\mu m$) based on RF probe specifications required for testing which restricts each run to a few devices. One way to overcome this limitation is to connect several devices in parallel between a set of input and output RF pads, with each device connected to a separate DC pad to turn one transistor ON at a time. This in theory allows for several devices to be prototyped on a single run and a thorough variation and yield analysis. However, the increased capacitive loading at the input and output due to the drive capacitors of these multiple devices cause a huge part of the signal to be shunted to ground, and appear as large feedthrough parasitics. This prevents the detection of any resonance peak and thus cannot be pursued as a viable option for optimization of these devices.

2.3 Finite Element Analysis

Based on the previous discussion, a 3D finite element analysis (FEA) of the acoustic structure including the resonant cavity and ABRs is necessary to design an optimized

resonant mode. A 3D model is constructed consisting of the handle wafer, buried oxide layer (BOX), the resonant structure capped by the stress liner and the premetal dielectric (Fig. 2-4(a)). The simulation shows the acoustic structure cut across the axis of symmetry, including the sensing FET with source/drain contacts, and the contacts to the resonator body and the driving capacitor.

The boundary condition at the top of the structure (above the FET and ABRs) was selected to be a free boundary condition. This is due to the fact that the subsequent layers are made of the low- dielectric (SiCOH) [60], which has very low acoustic impedance as compared to the materials in the acoustic cavity: Si ($Z_{Si}/Z_{SiCOH} \simeq 10.5$) and SiO_2 ($Z_{SiO2}/Z_{SiCOH} \simeq 6$). The boundary condition terminating the handle wafer was selected to be a low reflection boundary condition, to account for the large thickness of the handle wafer. This low reflection boundary condition is similar in function to Perfectly Matched Layers (PMLs), more commonly used for impedance matched boundary conditions in 2D simulations. A frequency sweep of the structure is carried out by applying a squeezing force on the dielectric between the capacitor plates. Fig. 2-4(b) and Fig. 2-4(c) show the resulting mode shape and stress plot in the longitudinal direction, respectively. The predicted resonance frequency is around 11.5 GHz for a longitudinal mode contained in the resonator and ABRs.

2.4 Small Signal Model

The small signal equivalent circuit of a capacitively driven, piezoresistively sensed resonator is provided in Fig. 1-2, consisting of a 1-port passive BVD model and a modified transistor pi-model. The drive capacitor is represented by C_0 while the RLC components model the mechanical mass-spring-damper system of the resonator. The piezoresistive sensing is represented by a transconductance g_α. The integration of such an electromechanical amplification element into the resonant cavity enables improvement in the out-of-band rejection of the signal before the contribution of feedthrough parasitics modeled by the C_f and r_f.

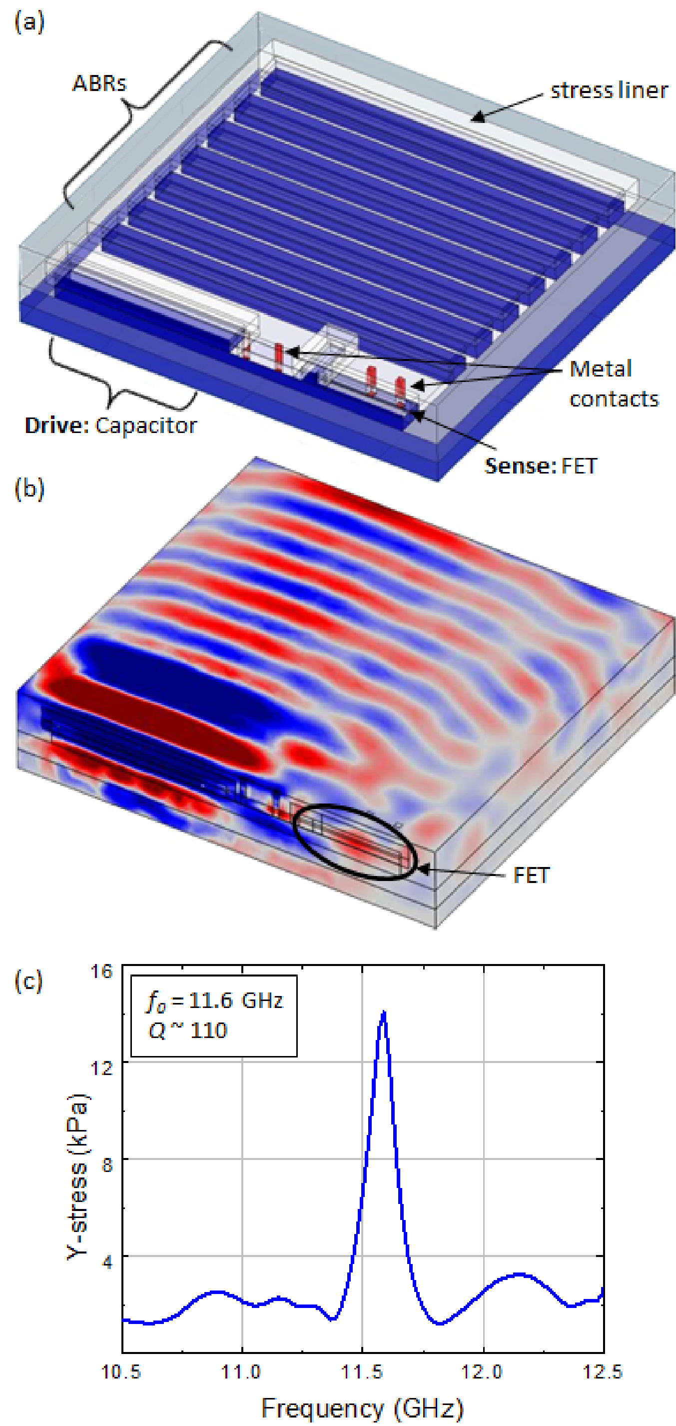


Figure 2-4: 3D Finite element analysis of unreleased RBT showing (a) symmetric half-plane of the 3D geometry of resonant cavity and ABRs, including the full FEOL stack materials starting with the handle wafer up to the first metal layer, (b) stress plot along the resonance direction, and (c) frequency response of simulated RBT derived from the integrated stress at the FET channel.

The amplitude of vibrations U_0 is obtained from the mechanical mode shape of the composite structure with a resonance frequency of ω_0 and resonance length L. The motional current i_m which is the electrical equivalent of the acoustic velocity in the mechanical lumped model, arises from the changing dimensions of the drive capacitance C_0 and its value at resonance is given by:

$$i_m = V_A \frac{dC_0}{dt} = \frac{2j\omega_0 V_A C_0 U_0}{L} \tag{2.2}$$

Thus the input current is proportional to and in phase with the velocity of acoustic vibrations. The motional RLC values may be calculated from the following equations.

$$R_m = \frac{v_{in}}{i_m} \tag{2.3}$$

$$L_m = Q\frac{R_m}{\omega_0} \tag{2.4}$$

$$C_m = \frac{1}{QR_m\omega_0} \tag{2.5}$$

On the sensing side, the electromechanical transconductance g_α represents the piezoresistive modulation of the drain current I_D at resonance. The electromechanical output current i_{em} is proportional to the relative change in mobility $\frac{\Delta\mu}{\mu}$ which in turn is related to the piezoresistive coefficient Π_{Si} and the Youngs modulus of Si, E_{Si}. This is given by:

$$i_{em} = \frac{\Delta\mu}{\mu} I_D = \frac{-\pi\Pi_{Si}E_{Si}U_0 I_D}{L} \tag{2.6}$$

Thus, this electromechanical current is proportional to the displacement in the device and is 90 degrees out of phase with the input current given in (2.2) which is in phase with the velocity of the resonator. The voltage across the motional capacitance C_m is in phase with the displacement and can be calculated from the input AC voltage v_{in} as follows.

$$V_{Cm} = v_{in}\frac{1/sC_m}{1/sC_m + R_m + sL_m} = \frac{v_{in}}{s^2L_mC_m + sR_mC_m + 1} \tag{2.7}$$

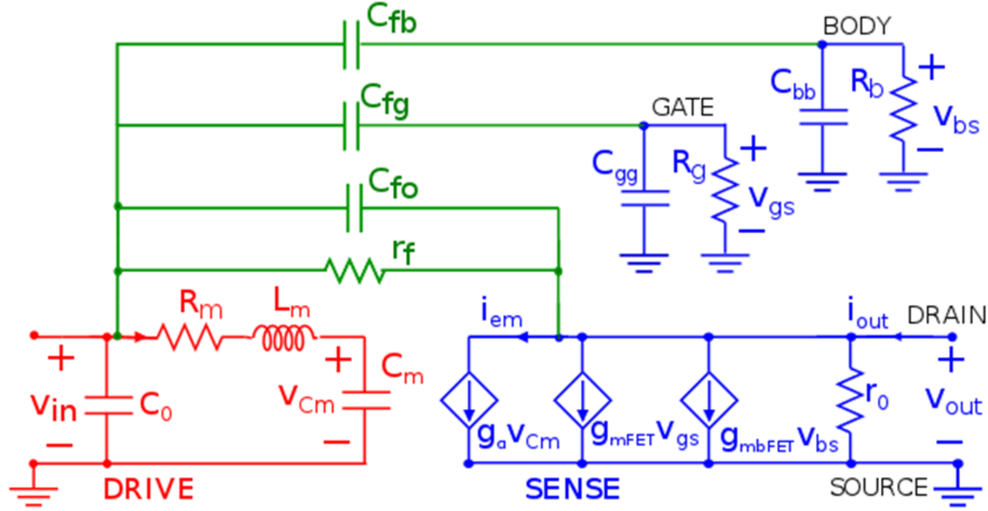


Figure 2-5: Augmented small signal model of the RBT consisting of: (1) an RLC branch modeling the mechanical resonant system (red), (2) a modified transistor small signal model (blue), and (3) detailed feedthrough parasitics (green) accounting for the direct feedthrough to drain, gate and body of the transistor.

At resonance, this is used to calculate g_α in terms of i_{em} as:

$$g_\alpha = \frac{i_{em}}{V_{Cm}} = \frac{i_{em}}{V_{Cm}} j\omega_0 R_m C_m \tag{2.8}$$

Along with the direct feedthrough from the driving capacitor to the drain of the sensing FET, capacitive coupling to the FET gate and body is also possible and this analysis was carried out by Bichoy Bahr for these devices. According to the extended small signal model in 2-5 the gate voltage resulting from this coupling can be expressed as:

$$\frac{v_{gs}(s)}{v_{in}(s)} = \frac{sR_g C_{fg}}{1 + sR_g(C_{gg} + C_{fg})} \tag{2.9}$$

where R_g is the gate bias resistance, C_{gg} and C_{fg} are the intrinsic gate capacitance and corresponding feedthrough capacitance to the FET gate from the driving capacitor, respectively. Similarly, the voltage feedthrough to the FET body can be expressed as:

$$\frac{v_{bs}(s)}{v_{in}(s)} = \frac{sR_b C_{fb}}{1 + sR_b(C_{bb} + C_{fb})} \tag{2.10}$$

where R_b is the body bias resistance, C_{bb} and C_{fb} are the body capacitance and

corresponding feedthrough capacitance, respectively. Both couplings show a high-pass response with frequency. In order to assess the magnitude of this feedthrough, 2.9 and 2.10 are better expressed in terms of the transistor cut-off frequency $_T = \frac{g_{mFET}}{C_{gg}}$. At resonance, the feedthrough expressions can be manipulated to yield:

$$\frac{v_{gs}(s)}{v_{in}(s)} = \frac{j\frac{\omega_0}{\omega_T}(g_{mFET}R_g)\frac{C_{fg}}{C_{gg}}}{1 + j\frac{\omega_0}{\omega_T}(g_{mFET}R_g)(1 + \frac{C_{fg}}{C_{gg}})} \tag{2.11}$$

$$\frac{v_{bs}(s)}{v_{in}(s)} = \frac{j\frac{\omega_0}{\omega_T}(g_{mFET}R_b)\frac{C_{fb}}{C_{gg}}}{1 + j\frac{\omega_0}{\omega_T}(g_{mFET}R_b)(1 + \frac{C_{fb}}{C_{bb}})\frac{C_{bb}}{C_{gg}}} \tag{2.12}$$

The bias resistances R_b and R_g must be small for reliable operation of the RBT. In a typical biasing configuration, the RBT FET gate may be biased through a current mirror. The gate bias resistance in this case is on the order of $\frac{1}{g_{mFET}}$, making $g_{mFET}R_g \approx 1$. Thus, we consider R_g to be limited such that:

$$g_{mFET}R_g \leq 1 \tag{2.13}$$

Moreover, R_b must be designed such that:

$$g_{mFET}R_b \ll 1 \tag{2.14}$$

We may also consider the case where the feedthrough capacitance C_{fg} and C_{fb} are both much smaller than the total gate capacitance C_{gg}, and the resonance frequency of the RBT ω_0 is much smaller than the cut-off frequency of the sensing FET ($\omega_0 \ll \omega_T$). With all these conditions satisfied, the voltage feedthrough to the gate and body of the sensing FET can be approximated as: $\frac{v_{gs}(s)}{v_{in}(s)} \approx j\omega_0 R_g C_{fg}$ and $\frac{v_{bs}(s)}{v_{in}(s)} \approx j\omega_0 R_b C_{fb}$

For a series resonance RLC, the capacitor voltage becomes jQv_{in} at resonance. Hence, the overall transconductance of the RBT, g_m, is given by:

$$g_m(j\omega_0) = \frac{i_{out}(j\omega_0)}{v_{in}(j\omega_0)} \approx -jQg_\alpha + g_{mFET}(j\omega_0 R_g C_{fg}) + g_{mbFET}(j\omega_0 R_b C_{fb}) + j\omega_0 C_{fo} + \frac{1}{r_f} \tag{2.15}$$

where g_{mbFET} represents the backgate transconductance. Rearranging this yields:

$$g_m(j\omega_0) = \frac{i_{out}(j\omega_0)}{v_{in}(j\omega_0)} \approx -jQg_\alpha + j\omega_0(g_{mFET}R_gC_{fg} + g_{mbFET}R_bC_{fb} + C_{fo}) + \frac{1}{r_f} \quad (2.16)$$

Thus, the feedthrough to the sensing FET gate and body can be lumped into a single feedthrough capacitance C_f, given by:

$$C_f = C_{fo} + g_{mFET}R_gC_{fg} + g_{mbFET}R_bC_{fb} \quad (2.17)$$

Using 2.17, the model of Fig. 2-5 reduces that of Fig. 1-2. Lumped feedthrough parasitics are represented as a parasitic capacitance C_f in parallel with a parasitic resistance r_f. The overall short circuit output current is given by:

$$i_{out}(s) = g_\alpha v_{Cm}(s) + \frac{v_{in}}{r_f} + sC_f v_{in} \quad (2.18)$$

And the overall input-to-output transconductance g_m is given by:

$$g_m = \frac{i_{out}(s)}{v_{in}(s)} = \frac{g_\alpha}{s^2L_mC_m + sR_mC_m + 1} + \frac{1}{r_f} + sC_f \quad (2.19)$$

Thus, this analysis shows that the simplified small signal model of Fig. 1-2 can be used to model the resonant body transistor including all of its parasitics. The key difference between BVD model (Fig. 1-1(b)) used for passive devices and the RBT small signal model (Fig. 1-2) is that in the case of the former, the motional impedance R_m completely determines the signal and losses at resonance whereas in the case of the latter, this is determined by the R_m and C_m along with the piezoresistive coefficient and drain current I_D. Thus the values of all of these paramaters need to be co-optimized to minimize losses and increase the small signal output current in the device at resonance. This simplified small signal model will be revisited in the following chapter and parameter values extracted for the ABR-confined CMOS-integrated RBTs. These parameters can be used in circuit simulators to model the RBT behavior for the purpose of CMOS-MEMS co-design.

Chapter 3

ABR-RBTs in CMOS: Experimental Results

Devices were fabricated by IBM and realized without any post-processing or packaging (Fig 3-1). Resonators were tested in a standard two-port configuration in a Cascade PMC200 RF probe system. SOLT calibration up to the probe tips was carried out, followed by measurement of open and short structures on the die to de-embed routing parasitics down to the first metal level. All RF measurements were carried out at room temperature with $-21.9\,\text{dBm}$ input power and $30\,\text{Hz}$ IF BW using an Agilent PNA-X $N5245A$. The overall input-to-output transconductance is obtained from the de-embedded Y parameters as per the definition for a MOSFET [61],

$$g_m = i_{out}/v_{in} = Y_{21} - Y_{12} \tag{3.1}$$

The ultimate goal for such integrated resonant devices is cofabrication with circuits in the FEOL level of a CMOS stack. The stand-alone devices fabricated here are probed using bondpads which introduce parasitics and require de-embedding. It should be noted CMOS-devices are usually designed to avoid electrostatic discharge (ESD) events at the chip level using ESD diodes shunting bondpads to the handle wafer. However, this results in an increased shunt capacitance to ground on the drive and sense ports and was thus avoided for probing standalone RBTs. Measurements

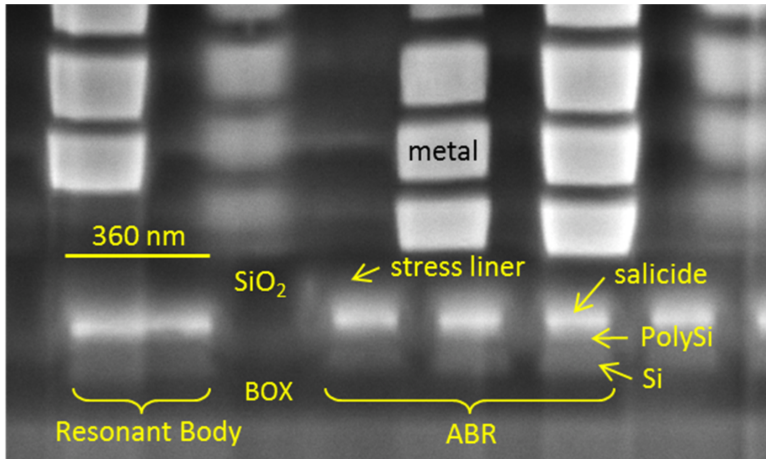


Figure 3-1: SEM of CMOS stack obtained using FIB. The resonant cavity comprised of the SCS device layer and acoustic Bragg reflectors is seen fully buried under the metal layers.

were therefore taken with continuous N_2 purge to reduce the chance of ESD-related device failure.

For DC measurements, the FET was biased at a gate voltage $V_A = 0.4V$ and a drain voltage $V_D = 0.6V$ to verify that the modified FETs showed characteristic transistor behavior (Fig. 3-2). Furthermore, the drive-capacitor voltage V_G does not affect the transistor $I_D - V_D$ curves, verifying no DC feedthrough.

Due to the modifications made to the overall FET geometry to create resonant devices, the output drain current was found to be approximately 2× lower at a given operating point as compared to a foundry-provided FET. The DC power consumed at the operating point is 35 μW.

3.1 RF Measurement

The frequency response of the input-to-output transconductance g_m of an nFET-ncap RBT is shown in Fig. 3-3. While the device layer in the region of the nFET is p-doped, the device layer defining the drive capacitor is n-doped. The device shows

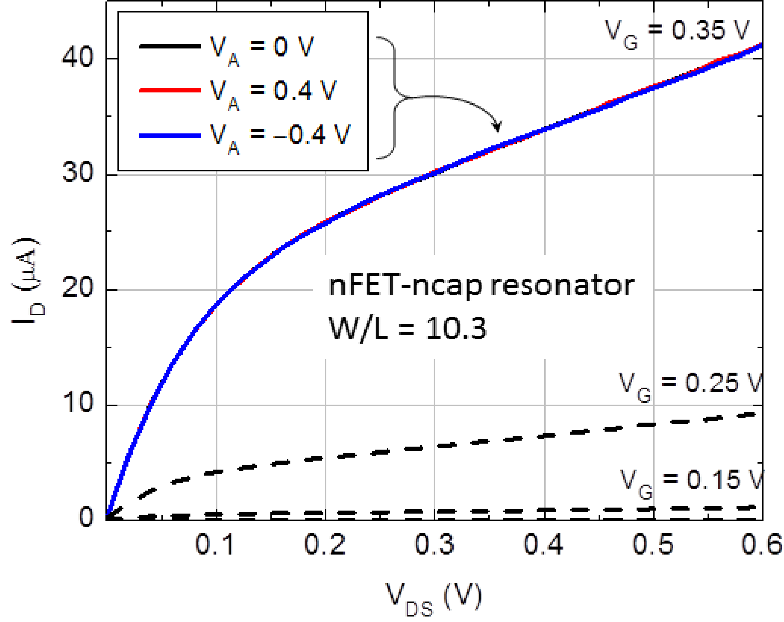


Figure 3-2: DC response of a sample device showing transistor characteristics and no dependence of drain current I_D on drive capacitor voltage V_A

a resonance frequency of 11.1 GHz with a Q of 30 extracted from full width at half maximum (FWHM). As seen in the figure, the amplitude of the resonance peak changes with the drive capacitor voltage V_A verifying the mechanical nature of the resonance peak. Similarly, the FET gate voltage V_G determines the drain current I_D, which in turn proportionally changes the electromechanical current as in (2.6).

Small signal parameters for the equivalent circuit shown in Fig. 1-2 were extracted using the data corresponding to the DC bias point of $V_A = 0.4V$ and $V_D = 0.6V$ in Fig. 3-3. The designed value of the driving capacitor C_0 was obtained from layout. The measured value of Q of 30 and resonance frequency of 11.12 GHz were used to calculate the amplitude of vibrations U_0, and to uniquely determine the parameter values for R_m, C_m and L_m and the electromechanical transconductance g_α were calculated based on the equations in section 2.4. The value of the output resistance r_0 was then determined from the Early voltage extracted from the FET DC response (Fig. 3-2) and foundry-provided nFET models. Fig. 3-4 shows a comparison of measured RF response of the nFET-ncap RBT to the response of this equivalent circuit model while Table 3.1 contains the extracted values of the small signal parameters. The

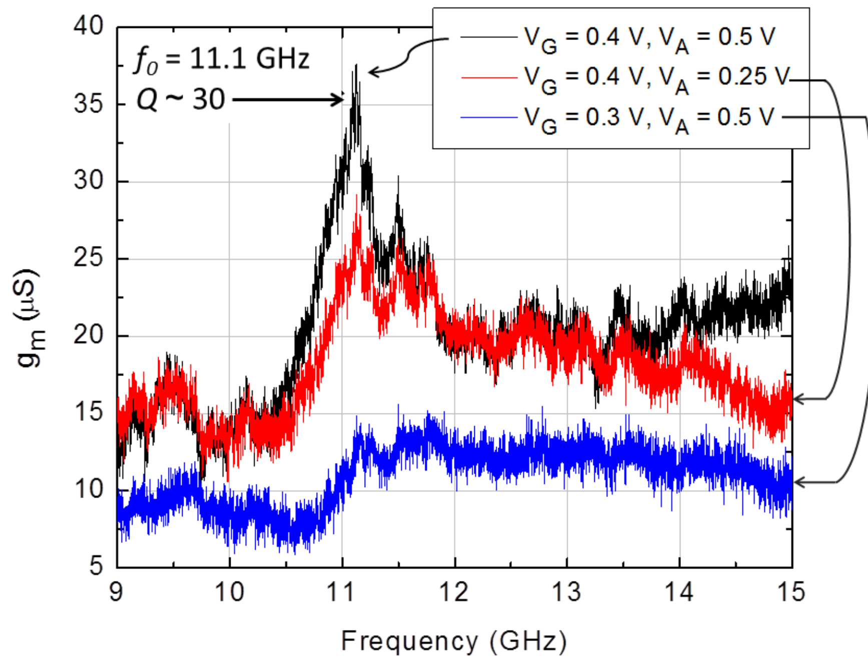


Figure 3-3: Frequency response of an nFET-ncap RBT showing a resonance frequency of 11.1 GHz with Q of 30. The drive capacitor voltage V_A modulates the gain at resonance verifying the mechanical nature of the resonance peak.

value of C_f and r_f were extracted from the broadband floor of the RF measurement. It is important to note that modeling of spurious modes requires the addition of RLC branches to the model in parallel with the existing one.

Fig. 3-5 shows the frequency and phase response of nFET -pcap device designed on the same die which demonstrates a resonance frequency of 11.54 GHz with $Q \sim 24$. The nFET-pcap device is identical to the nFET-ncap RBT whose response is included in Fig. 3-3, save for a p-type doping in the device layer below the drive capacitor instead of n-type doping. The parasitic reverse-biased diode in the nFET-ncap device increases feed-through with respect to the nFET-pcap device. Both types of RBTs are driven with n-doped or p-doped drive capacitors designed with identical geometry but show different resonance frequencies possibly due to stress liners, degenerate doping leading to differences in acoustic velocity, and fabrication differences between ntype and p-type doping which give rise to geometric differences.

In a passive resonator, the input voltage is expected to be in phase with the

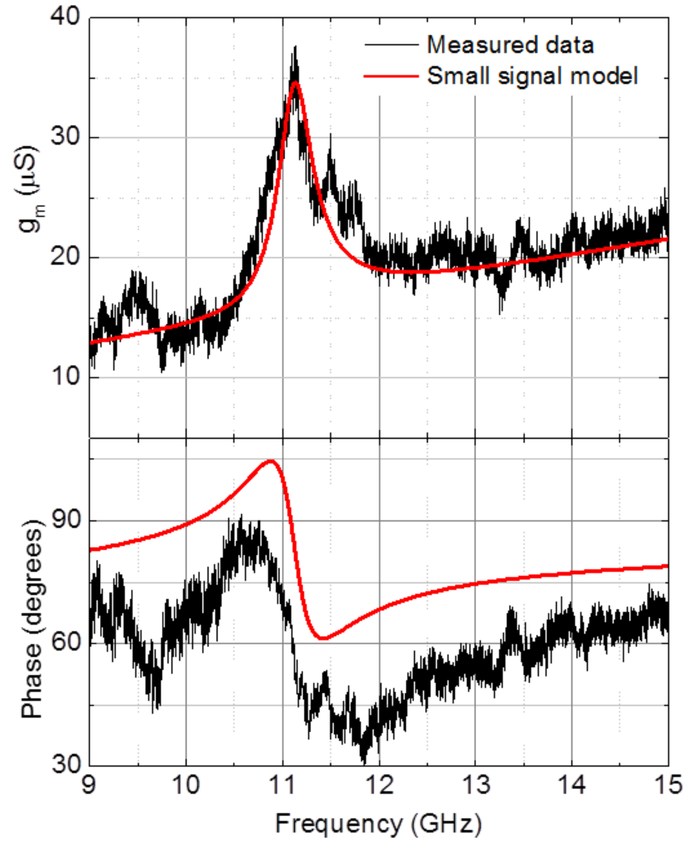


Figure 3-4: Measured response of nFET-ncap resonator at $V_A = 0.4V$ and $V_D = 0.6V$ (black) in close agreement with the equivalent small signal model (red) (Fig. 1-2). Extracted model parameters are included in Table 3.1. The model shows a good response for the primary mode, but additional spurious modes are not captured by the single LC branch. The systematic offset in the phase is the result of imperfect open/short de-embedding.

Table 3.1: Extracted small signal model paramaters for the Extracted parameters of the equivalent circuit model (1-2) of CMOS-MEMS RBTs fabricated in the 32nm IBM SOI CMOS process.

Parameters	Value
C_0	14 fF
R_m	1.1 MΩ
L_m	0.49 mH
C_m	4.2e-19 F
g_α	-0.62 μS
C_f	0.22 fF
r_f	290 kΩ
r_0	20 kΩ

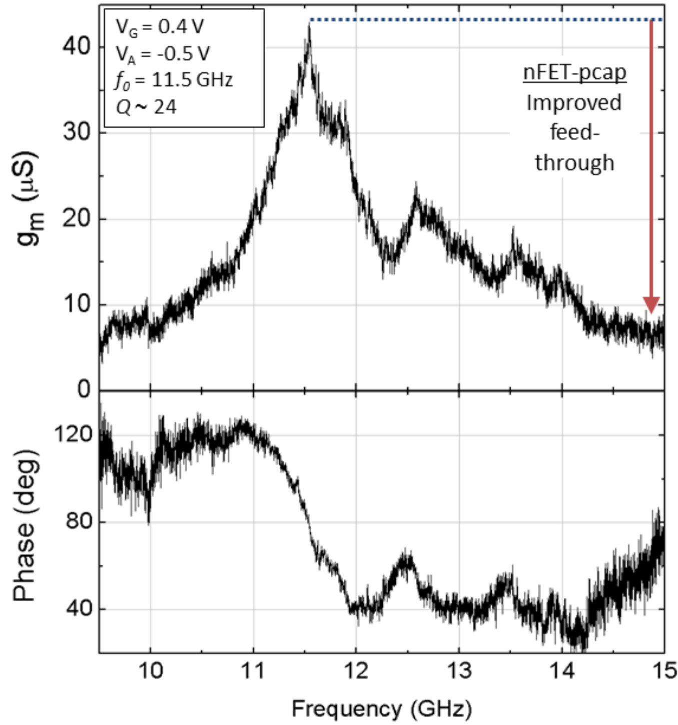


Figure 3-5: Frequency response of nFET-pcap RBT with improved feed-through relative to the nFET-ncap device. Phase at resonance agrees well with analysis ($\sim 90°$).

output current as inferred from the Butterworth-Van-Dyke model. As per the small signal-model of the CMOS-based RBTs, the output current i_{out} is in phase with the displacement in the device. Meanwhile, the input current i_{in} and voltage v_{in} are in phase with the velocity of vibrations at resonance. Hence the output current is expected to lag the input voltage by $90°$ for a positive V_A and lead by $90°$ for a negative V_A. This is confirmed by experiment in the phase plot of Fig. 3-5.

It is noted that testing at a higher DC bias current will improve the amplitude of the resonance peak with respect to the floor. This requires careful design around electromigration limits of routing metals and vias/contacts, especially in the lower metal levels to avoid burnout of metal traces. This poses a design tradeoff between maximum DC current in the RBT FET and number of contacts to the FET; increased number of contacts may act as scattering defects in the low-k dielectric near the resonant cavity distorting the mode shape.

Passive devices using electrostatic drive and sense were also implemented in this

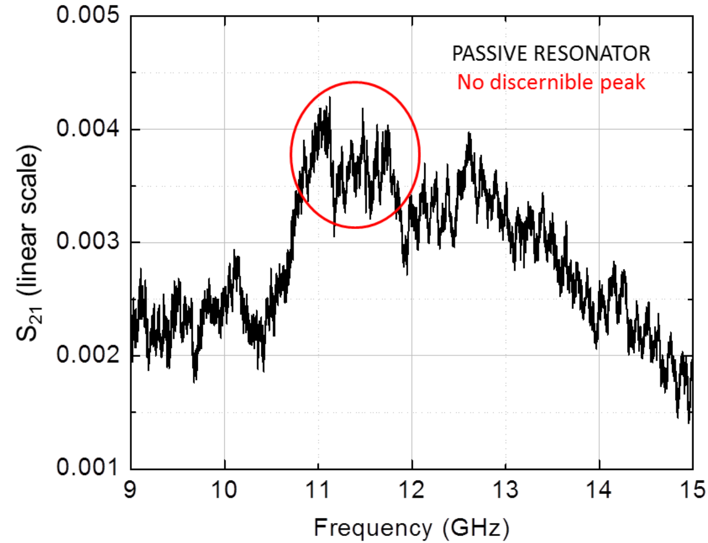
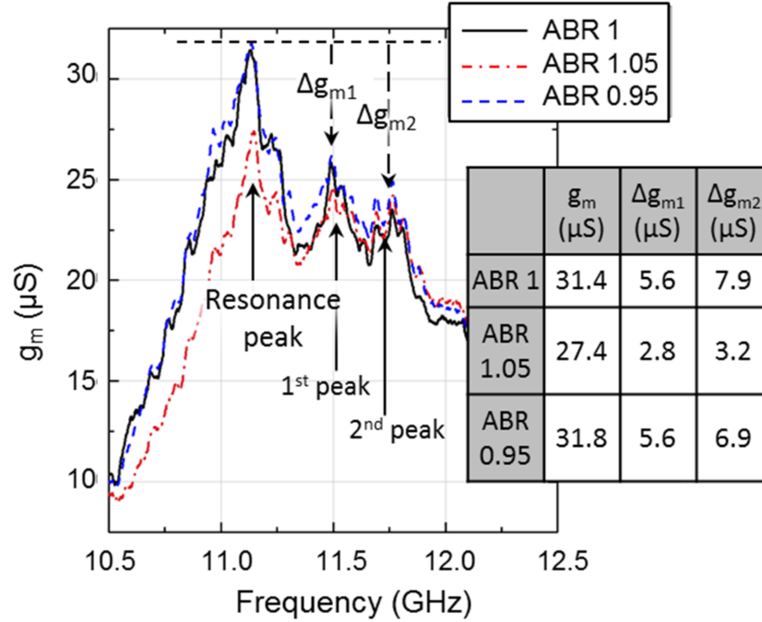


Figure 3-6: Frequency response of a passive device with pcap drive and sense, showing no discernible peak around the designed resonance frequency of 12 GHz. De-embedded S_{21} response using consistent open-short structures across active and passive devices is shown on a linear scale.

technology to compare the relative performance of passive vs. active resonators (Fig. 3-6). The geometry of the electrostatic device is similar to that of the RBT, with the FET replaced by a sense capacitor. 2-port de-embedded frequency response of the passive device shows no discernible resonance with respect to the feed-through on a linear S_{21} scale. This highlights the importance of FET sensing at the frequencies under consideration.

3.2 Effect of Acoustic Bragg Reflectors

The effect of ABRs on device performance was characterized by designing ABRs at 5% higher frequency (ABR 1.05) and 5% lower frequency (ABR 0.95) as compared to the resonance frequency. A comparison of devices with ABRs at three different frequencies is shown in Fig. 3-7. The device with ABRs at the resonance frequency shows optimized performance at resonance frequency in terms of suppression of spurious modes.



	g_m (μS)	Δg_{m1} (μS)	Δg_{m2} (μS)
ABR 1	31.4	5.6	7.9
ABR 1.05	27.4	2.8	3.2
ABR 0.95	31.8	5.6	6.9

Figure 3-7: Comparison of unreleased RBTs with identical resonant cavity length but with different ABR spacing. ABR 1 is designed at the cavity resonance frequency; ABR 1.05 is designed for 5% higher frequency, while ABR 0.95 is designed for 5% lower frequency. The resonator with ABRs designed at resonance frequency shows optimized spurious mode suppression.

As discussed in the design section, the first ABR pair had to be spaced at a $3\lambda/4$ distance from the resonator body due to DRC restrictions. Placing such pairs closer in future designs will further improve the performance of resonators with resonance frequency ABRs with respect to off-resonance ABRs.

3.3 Fabrication Variations and Yield

The yield of FETs in the process was nearly 100%, which emphasizes the merits of CMOS integration to harness the high yield of standard CMOS for MEMS fabrication. The variation in the resonance frequency of the resonators, designed with identical resonance dimensions, is around $0.1 - 0.5\%$, and is attributed to lithographic process variations. On the electrical side, such variations are in the form of the variance in the driving MOS capacitor and FET which affects the drive and sense efficiency, the gain at resonance, and electrical contribution to the total Q. On the fabrication

side, geometric or material variations from layer misalignments, sidewall slope and roughness, film thickness, stress liners, and variation in material acoustic properties affect the resonance frequency and Q.

A two-parameter model was developed by Wentao Wang to investigate the effects of lithographic fabrication variations on ABR performance in unreleased RBTs. The model sweeps the resonance frequency along with the length of the ABR Si/PolySi gate stack while keeping a constant ABR pitch. This model assumes that the ratio of the length of the gate stack (L_{Si}) to the length of the STI fill material SiO_2 (L_{SiO_2}) varies due to a systematic underetch or overetch or due to exposure variation in lithography, while the total length of one pair of ABR ($L_{Si} + L_{SiO_2}$) is held constant. Fig. 3-8 shows that under these conditions, a $\pm5\%$ variation is observed in the resonance frequency and $\pm10\%$ relative change in Q for a $\pm10\%$ variation in (L_{Si}/L_{SiO_2}).

Some of the above-noted variations may be mitigated by mechanically coupling the resonators which has been shown to improve the feed-through, suppress spurious modes, and improve gain at resonance with the tradeoff of a larger overall footprint [62], [63].

3.4 Thermal stability

Thermal stability is an important characteristic of any resonator required for reliable operation in oscillators, filters, sensors, and other communication and navigation systems. Si resonators typically exhibit temperature coefficient of frequency (TCF) of -20 to -30 ppm/K but use of materials with positive temperature coefficient of Young's modulus (TCE) such as SiO_2 has been demonstrated for thermal compensation [64]. The CMOS-integrated resonators presented here are inherently surrounded by SiO_2 in the BOX and STI fill used to define ABRs. Since the acoustic energy of unreleased resonators is contained not only within the resonant cavity but also the surrounding ABRs (Fig. 2-3), such devices are expected to show TCF compensation from the complimentary Si/SiO_2 pairing.

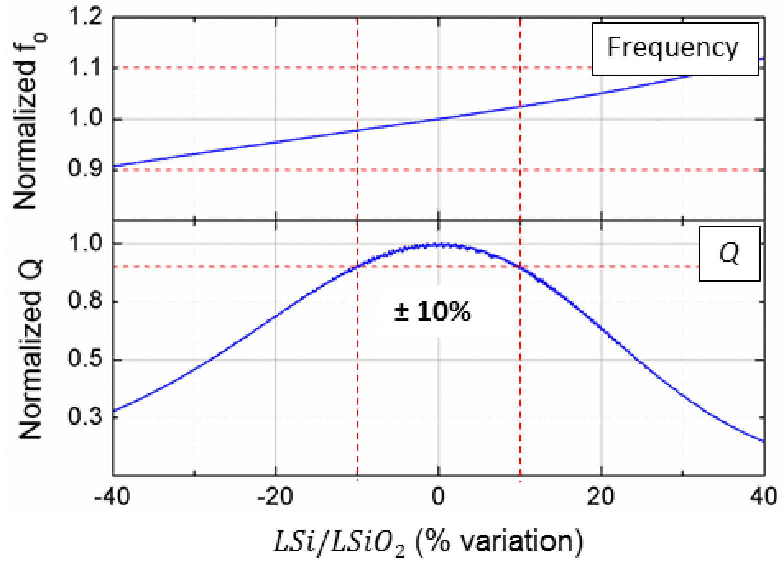


Figure 3-8: Simulated variations in normalized frequency and Q for RBT with 7 ABRs corresponding to percentage change in (L_{Si}/L_{SiO_2})). Here, L_{Si} is the length of Si-PolySi stack and L_{SiO_2} is the length of SiO_2 which together form one pair of ABR. The red lines mark ±10% of the designed values.

3.4.1 TCF Analysis

The TCF of a given resonator structure may not be simply calculated by adding the TCFs of individual materials weighted by their relative proportions in the composite structure. Instead, the TCF contribution of each material is determined by the net elastic and kinetic energy contained in it at the resonance mode. The TCF of a composite structure such as the CMOS-integrated resonator can thus be obtained using perturbation theory [65] and such an analysis was carried out for these devices by Bichoy Bahr. At resonance, the total kinetic energy K and potential energy U are equal in the resonator domain Ω. This yields:

$$\frac{1}{2}\int_{\Omega} S.c.S d\Omega = \frac{\omega^2}{2}\int_{\Omega} \rho ||u||^2 d\Omega \tag{3.2}$$

where c is elastic stiffness tensor, S is the strain field, ρ is the mass density and u is the displacement field. The notation (:) used here represents the double dot tensor product. For isotropic materials, the stiffness tensor is proportional to the Young's

modulus E and can be written as

$$c = E\tilde{c}(\nu) \tag{3.3}$$

where ν is Poisson's ratio. Perturbation theory assumes that changes in the mode shape can be neglected for small perturbations in the material properties. Changes in the strain field can also be neglected in this case. Taking the derivative of 3.2 with respect to the temperature, and neglecting any change in Poisson's ratio, it can be shown that:

$$TCF = \frac{1}{\omega}\frac{\partial \omega}{\partial T} = \frac{1}{2}\sum_{i=1}^{N}(\frac{\alpha_{Ei}U_i}{U} - \frac{\alpha_i K_i}{K}) \tag{3.4}$$

where α_{Ei} and α_i are the Young's modulus and mass density coefficients, respectively. U and K are the total strain and kinetic energy in the composite structure, respectively, while U_i and K_i are the strain and kinetic energy in the ith domain, respectively. For negligible changes in strain field, the volume of each domain is assumed to be constant and thus α_i can be assumed to be zero, leaving only Young's modulus and strain energy ratios in the equation. By virtue of the geometric complexity of the CMOS RBT, a closed form solution for the mode shape is not available. Using COMSOL Multiphysics, a finite element eigenfrequency simulation was used to find the strain energy in each domain at 298K. The resonance mode was identified as the eigenmode with highest strain energy in the sensing transistor. Table 3.2 shows the material properties for the FEOL materials used in the simulation [64], [66]. Substituting these values into 3.4, the resonator TCF is found to be +2.41 ppm/K.

To further validate the TCF results, another finite element eigenfrequency simulation is carried out at 380 K, by modifying the corresponding materials Young's modulus based on their TCEs. The eigenmode corresponding to the simulation at room temperature is identified from the mode shape and stress distribution. The TCF is then estimated from the frequency shift between the two cases. At room temperature, the simulated resonance frequency was found to be 11.51123 GHz, whereas at 380 K it rises to 11.51339 GHz. These results correspond to a TCF of +2.29 ppm/K.

Table 3.2: Temperature coefficient of Young's modulus and strain energy density of resonator materials considered for TCF simulation.

Materials	E(GPa)	α_E(ppm/K)
PolySi	160	-63.82
SiO_2	70	$+195.8$
Si nitride	260.5	-85.82

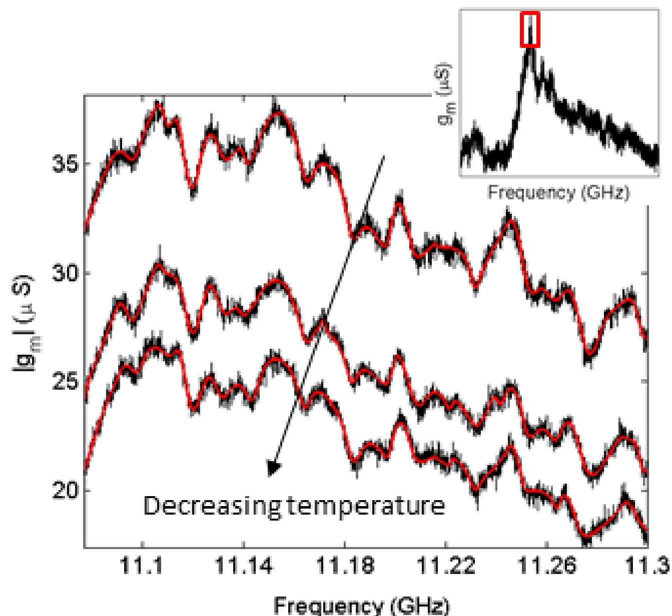


Figure 3-9: Zooming in around the measured resonance peak included in inset shows multiple spurious modes that make up the peak. Plot compares measured values of the transconductance and data fitted using rational transfer functions. Measured data shown in black, red lines show the output from the rational transfer function model.

3.4.2 TCF Measurement and Data Fitting

The temperature stability of the CMOS-MEMS resonators was measured above room temperature under N_2 purge to avoid ESD events. Devices were characterized at room temperature (298 K), 340 K and 380 K. The DC biasing conditions were the same as described in chapter 3. Ceramic-substrate calibration and on-chip de-embedding were carried out at each temperature with -21.9 dBm input power and 30 Hz IF BW. The fact that resonance peaks exist across temperatures with independent calibrations validate that they arise from the device and not from any artifacts of the RF measurement.

Due to the presence of spurious modes (from CMP fill) in close proximity to the resonance peak and the small value of the frequency shift, the TCF could not be directly extracted from g_m measurement. Numerical modeling techniques were thus automated by Zohaib Mahmood to perform temperature stability analysis.

Systems with multiple resonances in the frequency response can be modeled accurately using a rational transfer function of the form:

$$H(s) = \sum_{k=1}^{\kappa} \frac{R_k}{s - \alpha_k} + D \tag{3.5}$$

Here α_k and R_k are poles and residues respectively. κ is the total number of poles used which defines the model order. For such a model to be physically consistent, it was ensured that the complex poles appear in conjugate pairs and all the poles are stable, i.e. they have negative real part ($\Re\alpha_k < 0$). For our analysis, the model $H(s)$ minimizes the mismatch between the measured transconductance and output of the model using an optimization framework as described in [67], [68]. For the example presented here, de-embedded S-parameters of the resonator measured at the above-mentioned temperatures were used to compute the transconductance g_m.

Rational transfer functions with 22 pairs of complex conjugate poles ($\kappa = 44$) each were used to model the transconductance as a function of frequency computed for different temperatures and a high-quality fit was obtained (Fig. 3-9). Next, the smooth outputs of the models were analyzed to locate the resonant frequencies and their sensitivities to operating temperature. Temperature sensitivities of individual spurious modes are reported in terms of total frequency shift in Fig. 3-9. Error bounds were computed by analyzing the noise in measured data and the RMS error generated by the model in (3.5). It is noted that the error bounds for high-Q resonances, such as the one at 11.17 GHz, are tighter than the error bounds for low-Q resonances, such as the one at 11.19 GHz.

The complimentary TCE of Si/SiO_2 in the resonator and the surrounding ABRs results in a temperature stability TCF of 3 ppm/K (Fig. 3-10). Two different families of poles were observed those showing positive TCF indicating oxide-dominated

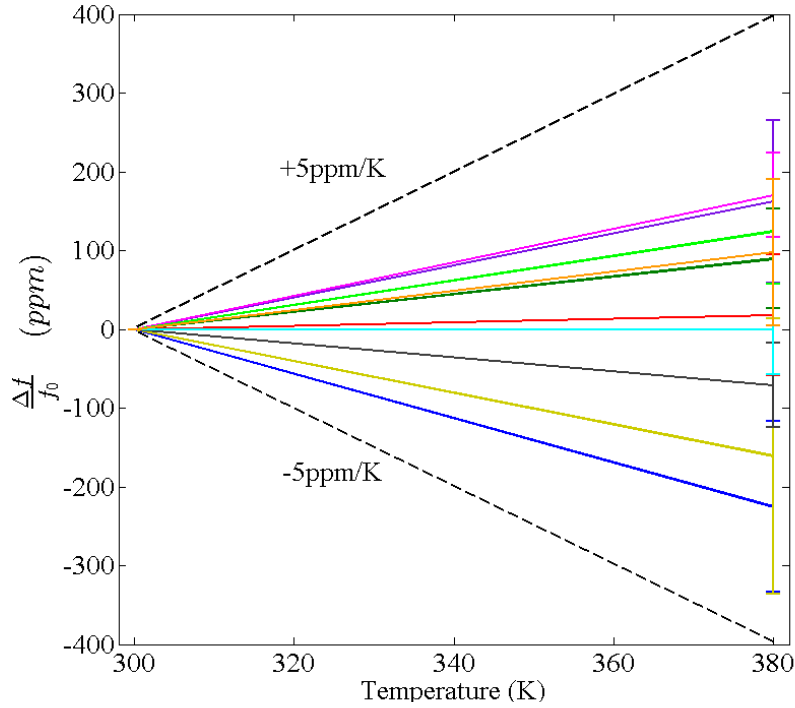


Figure 3-10: $\Delta f / f_0$ with error bars plotted against temperature. Reference lines at $\pm 5 ppm/K$ are shown.

modes and those with negative TCF showing Si-dominated modes. Some modes were observed with sub-ppm TCF, which demonstrates almost complete compensation of the thermal properties of Si by the surrounding SiO_2 . This complimentary nature of the TCE of Si/SiO_2 provides the opportunity to engineer the TCF of the resonance peak in future designs to either obtain a high TCF for design of temperature sensors or for a low TCF for oscillators and filter design.

3.5 Summary and Discussion of Performance

The first CMOS-based unreleased RBTs are demonstrated in IBM's 32SOI process with resonance frequencies above 11 GHz, Qs of $24 - 30$ and footprint of less than $3\,\mu m \times 5\,\mu m$. They are fabricated at the transistor level of the CMOS stack and are realized without the need for any post-processing or packaging. TCF compensation is shown to < 3 ppm/K due to the complimentary TCEs of Si/SiO_2 present in the

resonance cavity. The absence of a resonance peak in capacitively sensed resonators shows the importance of FET sensing for scaling to high frequencies.

The Q of the RBTs is comparable to that of CMOS-integrated LC tanks at similar frequencies. However, compared to other acoustic resonators, the Q of the first-generation CMOS-MEMS RBTs leaves room for improvement. The acoustic properties of such devices can be precisely designed and simulated if material properties and dimensions of the FEOL and BEOL stack are available. Accurate knowledge of the acoustic impedance and velocity of the SiO_2 and stress liner used as STI fill material is critical to the design of ABRs for maximum reflectivity at the desired frequency. A deviation in properties such as density, Young's modulus, and built-in stress cause a mismatch of the ABR design from the resonator at the resonance frequency, resulting in reduced gain, Q and an altered resonance frequency due to alteration of the boundary conditions forming the resonant cavity. Similarly, the dimensions, location, and processing method of the salicide contacts to the PolySi gate and the source/drain regions affect the aspect ratio and mode shape in the thickness dimension resulting in spurious modes. Several of the above-mentioned parameters and properties of the FEOL stack were unknown to the foundry or could not be disclosed resulting in compromised device performance in terms of low Q and presence of spurious modes close to the resonance peak in first-generation devices. In general, for each new technology, characterization structures such as transmission lines are required to accurately extract the different material properties for RBT optimization.

Another set of structures which strongly affect device performance are the copper layers appearing vertically above the resonator due to CMP fill generation. The resultant acoustic reflector in the vertical direction due to the acoustic mismatch between the low- dielectric and Cu layers leads to spurious modes in the thickness direction. Such layers can be excluded from future designs or patterned to create 3D phononic crystals around the resonant cavity.

Furthermore, the small aspect ratio of the acoustic isolation in the form of ABRs and the corresponding small solid angle subtended at the resonator for acoustic reflection resulted in Qs of 30 due to radiation losses into the BEOL stack and Si substrate

below.

The finite element analysis carried out on these devices shows that while the experimentally observed resonance frequency is a good match to the simulation, the non-uniformity in device structure between the drive and sense side results in small induced strains at the sensing FET at resonance. Thus the FEM emphasizes the importance of uniformity in the resonance cavity in the direction normal to the acoustic wave to to maximize mechanical strain at the sensing transducer for increased output.

Chapter 4

PnC-RBTs in CMOS

Several different approaches were considered to improve the Q and the transduction efficiency of the resonant mode as well as suppress spurious modes.

One approach that was considered to improve the aspect ratio of the isolation structures while using easily available FEOL materials was through the use of deep trench capacitors (DTcaps) used as part of the DRAM in IBM's 45nm SOI process (Fig. 4-1). However there are several problems with using the deep trench capacitors in IBM's process as part of the resonant cavity design:

- The trenches have random voids which result in imperfect and unpredictable reflections.

- The size and spacing of trenches is fixed and changing the dimensions is a serious design rule violation that can lead to propagating cracks and mechanical failure.

- The geometry and structure of the DTcaps is such that since they extend far into the handle wafer ($\sim 4\mu m$), any mode driven by the DTcaps is confined far below the sensing transducers (FETs) which are above the BOX layer.

- The DTcaps available in IBM's 45nm technology may be modeled as an RC branch with a cutoff frequency in the MHz range while the transistor dimensions mean that the resonance mode has a frequency in the GHz range. This makes the DTs unviable for electrostatic drive with FET sensing.

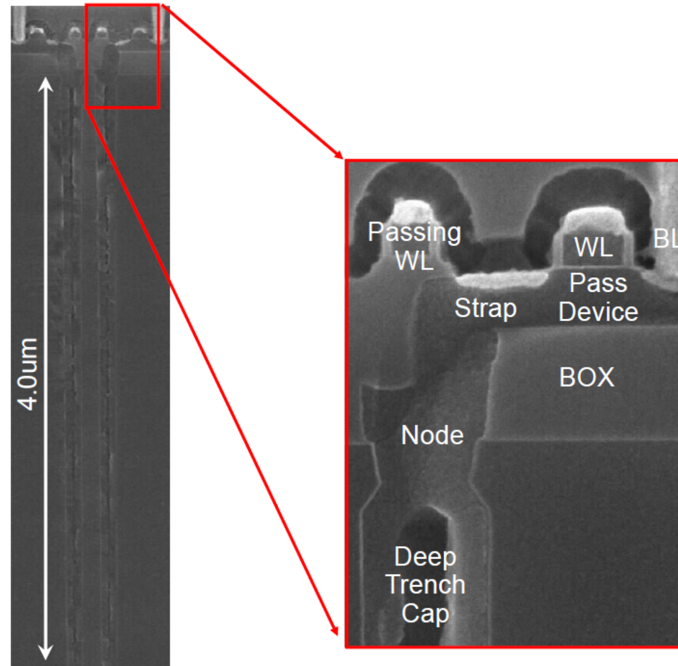


Figure 4-1: (left) Cross-section view of deep trench capacitors in IBM's 45nm SOI process showing $> 35:1$ aspect ratio. (right) Details showing the interfacing transistors along with PolySi strap connecting the capacitor through the BOX.

- If DTcaps themselves as used for electrostatic sensing, it takes away the advantages of low noise, high efficiency of FET sensing while restricting operation to MHz frequencies, which make CMOS integration itself redundant.

- Deep trenches are often unavailable in standard CMOS processes making this a specialized solution for a single process flow. When available, they are often electrically disconnected and available only as isolation structures or guard rings, which means they cannot be used for electrostatic actuation.

Given these issues, it may be concluded that DTcaps are not a viable option as actuating or sensing transducers in CMOS RBTs.

A seemingly obvious way to reduce spurious modes is by removing CMP fill that appears randomly above designed resonators by using metal exclude layers in the standard CMOS process. However there is a large acoustic impedance mismatch between the FEOL layers, typically the stress liners, silicide, and metals that lie vertically above the resonant cavity in the stack, and the porous low-k dielectric

SiCOH in the BEOL which has extremely low impedance. Finite element analysis in COMSOL shows that in a resonator which relies on capacitive drive through the gate dielectric, this leads to very high energy loss into the BEOL with very little energy getting reflected back into the FEOL where the sensing transducer is located. This results in a very low stress appearing at the channel of the sensing FET which in turn results in the disappearance of the peak and a severely reduced dynamic range. Secondly, the absence of a metal layers in the SiCOH matrix coupled with the very low impedance of the SiCOH, results in the creation of a pseudo-free boundary condition at the top of the resonator. This results to spurious modes in the thickness direction.

Thus, what is ideally desired here is a structure in BEOL which will reflect energy at the resonance frequency to improve the mechanical signal while allowing energy loss at frequencies other than the resonance frequency to suppress spurious modes. This is similar to the concept of vertical ABRs for unreleased resonators which have been previously demonstrated as solidly mounted devices using ABRs in the vertical direction for confinement of thickness modes [57]. This concept may be extended to fully buried CMOS resonators using the BEOL layers such as routing metals and inter-metal dielectric for design of ABRs in the vertical direction. However, such an implementation suffers from the following problems:

- BEOL layer thicknesses are process-determined and are not available as a design parameter.
- Vertical ABRs preclude the design of lithographically-defined resonant modes and frequencies, restricting the whole wafer to a single resonance frequency and its harmonics.
- High variability in BEOL layer thicknesses as compared to lithographically defined dimensions results in variable center frequency and reduced yield.

As one solution, a 3D acoustic reflective structure comprising a phononic crystal (PnC) (Fig. 4-2) which surrounds the resonant cavity is proposed, for better mode confinement and suppression of spurious modes as compared to first-generation devices.

Figure 4-2: Cross-section schematic of a standard CMOS stack showing phononic crystal formed using BEOL layers, encapsulating resonant cavity formed in FEOL layers.

4.1 Design of PnC in CMOS

A PnC is an acoustic structure with periodic variations in mechanical properties, which generate frequency bandgaps in which no elastic waves may propagate through the structure. Such acoustic bandgaps are formed by the diffraction and scattering of phonons at the interface between the materials making up the PnC. The location, width and rejection within such bandgaps is engineered by varying lattice types as well as the size, shapes, positions and properties of the materials constituting the PnC. PnCs have been experimentally demonstrated in a variety of materials such as Si-air [69], SiC-air [70], Si-W [71] and SiO_2 -W [72] for acoustic isolation and mirroring, as acoustic waveguides, cavities and filter coupling. Phononic bandgaps in these material systems have been demonstrated to exceed 10% of the center frequency.

Based on classical wave theory, PnC bandgaps are formed due to two different resonance conditions that prohibit acoustic propagation through the crystal, called the Mie resonance (from local standing waves formed within inclusions) and the Bragg resonance (from destructive interference of waves scattered from the inclusions) [73] (Fig. 4-3).

In a 2D representative diagram with circular "inclusion" material with radius

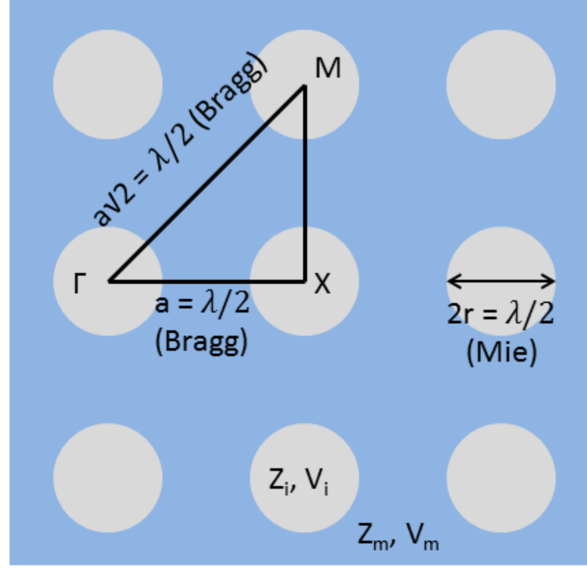


Figure 4-3: Schematic of 2D phononic crystal showing conditions for Bragg and Mie resonances which result in phononic bandgaps.

r and pitch a, with acoustic impedance Z_i and velocity V_i and an environment or surrounding material with acoustic impedance Z_m and velocity V_m, the reflection coefficient at the inclusion-environment interface is given as:

$$\Gamma^2 = (\frac{Z_i - Z_m}{Z_i + Z_m})^2 \tag{4.1}$$

and the Bragg and Mie resonance conditions along various crystal directions may be given by:

$$f(Bragg)_{\Gamma X} = f(Bragg)_{XM} = \frac{V_{avg}}{2a} \tag{4.2}$$

$$f(Bragg)_{\Gamma X} = \frac{V_{avg}}{2a\sqrt{2}} \tag{4.3}$$

$$f(Mie) = \frac{V_i}{4r} \tag{4.4}$$

where the average acoustic velocity through the crystal V_{avg} is given by:

$$V_{avg} = \pi(\frac{r}{a})^2 V_i + (1 - \pi(\frac{r}{a})^2) V_m \tag{4.5}$$

To create a wide acoustic bandgap, it is desirable to maximize scattering at in-

terfaces (4.1) and maximize the overlap of Bragg and Mie resonances to form wide and deep bandgaps (4.2), (4.4). These conditions may be satisfied by maximizing the acoustic impedance mismatch between the PnC material pairs while matching their acoustic velocities. It is also noted that filling fraction r/a must be large to restrict transmission through the surrounding material but if this becomes too high, hopping between these inclusions once again leads to increased transmission. Further details of PnC theory may be found in [74].

Thus, material pairs with high acoustic impedance mismatch such as W/SiO_2 or Cu/SiO_2 form highly reflective PnCs in which fewer repeating layers of the PnC structural unit cell are required for acoustic confinement. The high impedance mismatch also results in wide PnC bandgaps; these facilitate the design of a high-Q resonance within such bandgaps [75] and are commonly implemented in 1D ABRs [57].

Such material pairs are found in the BEOL of integrated circuit (IC) technologies as high acoustic impedance metals (such as Cu or W) surrounded by a low acoustic impedance dielectric (such as SiO_2 and low-k dielectrics like SiCOH) used for metal routing and vias. In a typical IC technology, while the thickness of metals (or vias) is fixed, the widths and lengths are lithographically defined and these may be optimized within a wide range to engineer a wide frequency bandgap for the PnC. Table 4.1 lists some common materials found in BEOL CMOS along with their acoustic impedances. Copper metallization over low-κ SiCOH background as well as tungsten over SiO_2

Table 4.1: Mechanical properties for materials in the CMOS stack

Material	ρ (kg/m^3)	c_{11} (GPa)	Z_{11} $(MRayls)$	c_{44} (GPa)	Z_{44} $(MRayls)$
Si$< 1-0-0 >$	2329	194.3	21.2	79.5	13.6
Poly-Si	2320	183	20.6	65.5	12.3
SiO_2	2200	75.2	12.9	29.9	8.11
TEOS	2160	49.4	10.3	19.7	6.5
Tungsten	19250	525	101	161	55.6
Copper	8937	190	41.2	47.0	20.5
Aluminum	2735	111.1	17.4	28.9	8.9
SiCOH	1060	3.96	2.05	1.32	1.18

are notable examples with impedance contrast ratios on the order of 19× and 17× respectively. The ability to create wide-bandgap PnCs in CMOS makes them ideal for achieving high acoustic confinement in unreleased CMOS.

In this work, the PnC defining the acoustic cavity was designed in IBM's 32nm SOI process using the first five metal layers of the BEOL stack as they have identical thicknesses. These consist of Cu surrounded by low-κ SiCOH intermetal dielectric [76]. As discussed, the Cu layers are ideal for PnC design as DRC constraints on their size and placement are sufficiently relaxed to allow engineering of a wide acoustic bandgap. FEM simulation of the unit cell shown in Fig. 4-4(a) was used to analyze and optimize the frequency response of this PnC. The size and pitch of the Cu blocks patterned over the inter-metal dielectric are 168 nm and 252 nm respectively. Bloch boundary conditions were forced in the unit cell model with k-vector scanned across the irreducible Brillouin zone of the reciprocal lattice (Fig. 4-4(b)).

This type of analysis determines every possible acoustic resonance mode that may be sustained by such a periodically repeating PnC unit cell in all directions, and thus captures the expected behavior of the PnC in all directions. The eigenfrequencies obtained at each k-vector from this simulation reveal a 3.47 GHz wide bandgap centered at 4.5 GHz (Fig. 4-4(c)). The phononic bandgap prevents transmission of mechanical energy in this range of frequencies in any direction in the PnC, from the resonant cavity outwards to the environment and from the environment inwards to the resonant cavity. In IBM's 32nm SOI process, upper metal levels have a different thickness which causes them to break the periodicity of the PnC. To simplify design, these upper metals were excluded using CMP fill exclusion layers available in the process.

4.2 Resonator Design

The foundry-provided analog nFET was chosen to drive and sense the acoustic resonator to take advantage of the high-quality, ultrathin gate dielectric and high-performance FETs available in the FEOL stack. In the ABR-only design from [15],

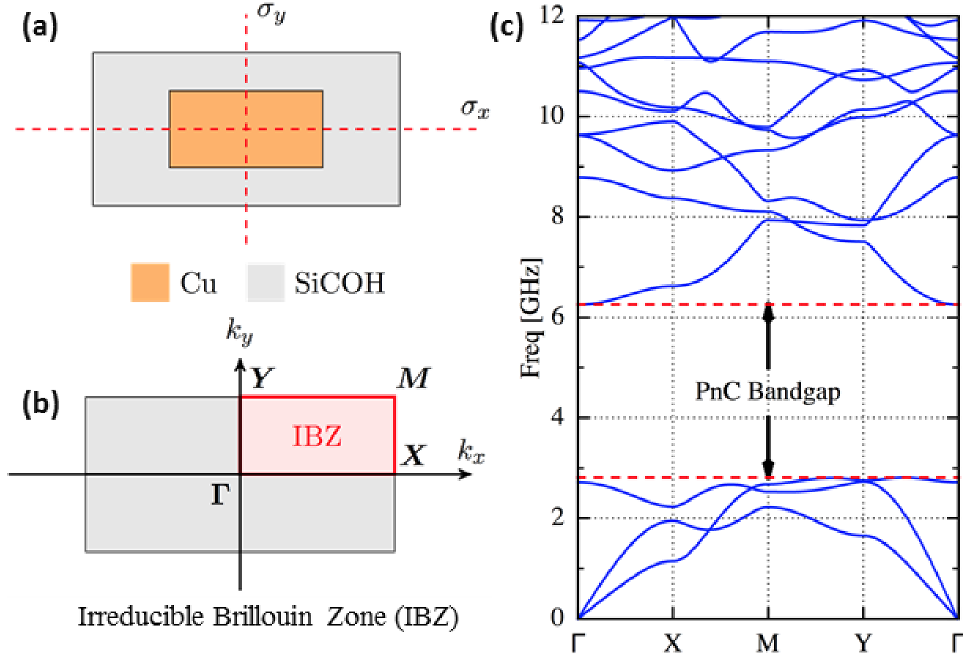


Figure 4-4: (a) Unit cell of the PnC implemented in this design (b) Irreducible Brillouin zone showing directions of k-vector scan. (c) COMSOL simulation of the PnC unit cell showing bandgap a bandgap between 2.80 GHz and 6.27 GHz.

the driving and sensing transducers each spanned half the length of the cavity (in the y-direction), resulting in an asymmetric transduction of the longitudinal mode (Fig. 4-5). In the current design, such asymmetry was avoided by configuring two nFETs as MOS capacitors (MOSCAPs) extending the entire length of the resonance cavity (in the y-direction). A single sensing nFET was placed at the center of the cavity between the two driving MOSCAPs. A floating body nFET was chosen over body-contacted structures for optimal structural continuity along the resonance cavity in the y-direction.

In operation, the two driving nFETs configured as MOSCAPs are biased into inversion. A small AC voltage is applied across the gate dielectric of the capcitors to launch acoustic vibrations into the device. At resonance, the acoustic vibrations of the resonant cavity are sensed as the piezoresistive modulation of the sensing FET drain current.

Dummy gates of the transistors included in the foundry-provided layout were left

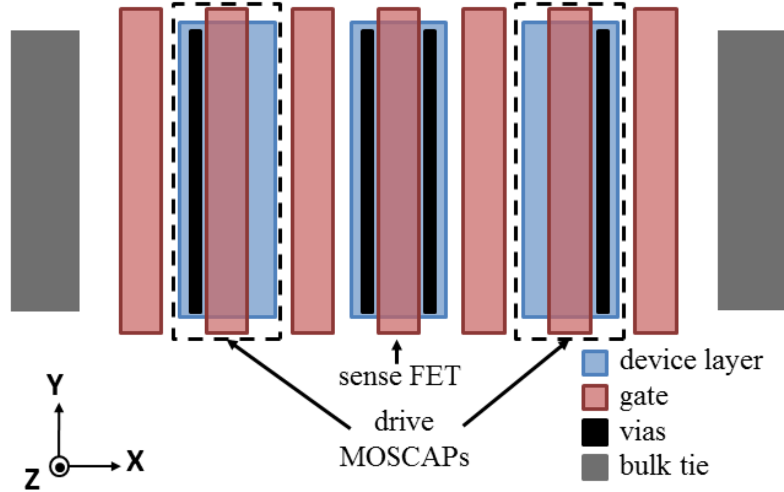


Figure 4-5: Top view of PnC resonator showing driving and sensing transistors, gates, modified contacts, first metal level and bulk ties. Metals layers are excluded for clarity of underlying structure.

unmodified to maintain uniformity of stress liner distribution within the resonant cavity and to minimize DRC violations. Adjacent transistors in the resonant cavity were positioned such that the neighboring transistors' dummy gates exactly overlapped with each other. nFets with 160 nm nominal gate length were configured with 2 μm gate width and gate-to-gate pitch of 290 nm. The overall footprint of the device $5\mu m \times 7\mu m$.

Certain parameters of the foundry-provided layout were modified for optimal confinement of the resonant mode. First, the routing for the driving and sensing gates was limited to the first metal layer to maintain the periodicity of the PnC in the higher metal levels for optimal acoustic confinement at resonance. Second, some vias from the MOSCAP source/drain regions were removed to minimize acoustic scattering points within the resonant cavity. Third, long rectangular wall-like vias spanning the width of the FET (in the y-direction) were used to uniformly reproduce the resonant structure from the 2D design in Fig. 4-5. Such vias are already offered as a fabrication option and optimized to have no effect on yield by foundries such as TSMC. In general this is the only serious DRC rule violation in the design of these second-generation PnC-RBTs as changing the via type from square to long rectangular vias does affect FEOL layers critical to transistor operation such as stress liners

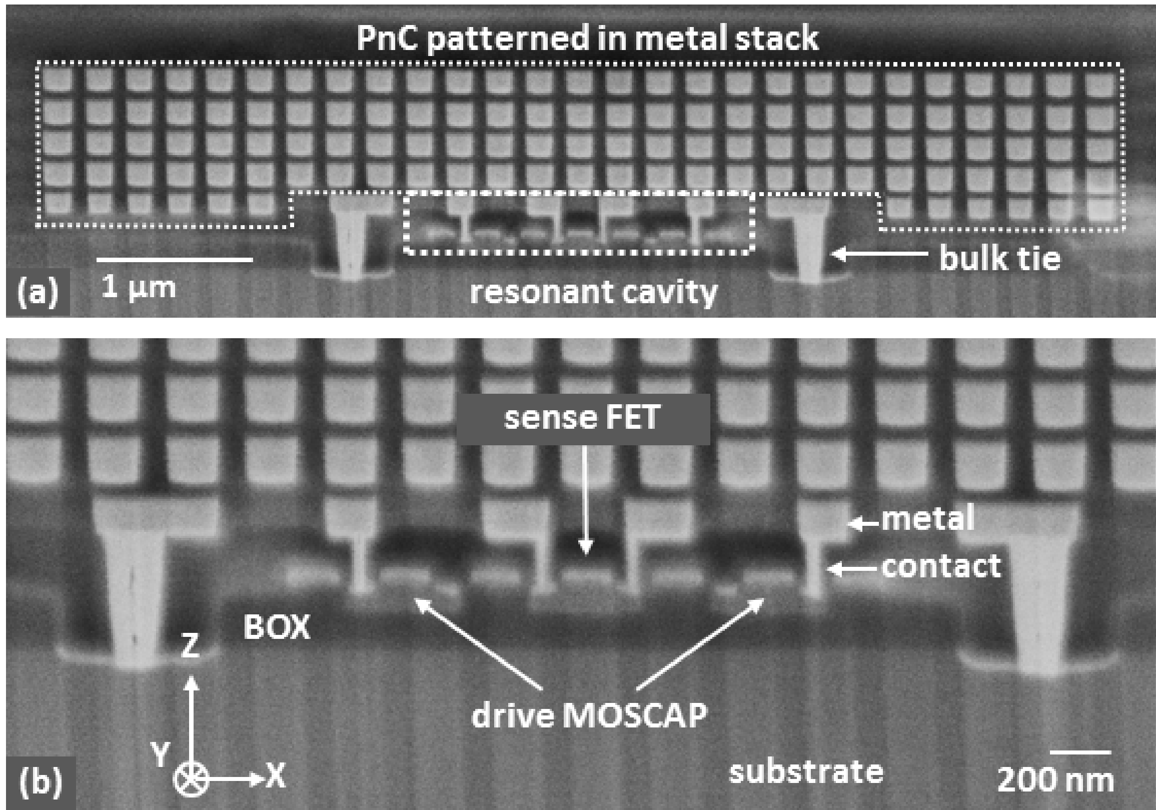


Figure 4-6: (a) Cross-section SEM of a CMOS-MEMS resonators showing PnC patterned in metal stack and FEOL resonant cavity (b) details of resonant cavity showing driving and sensing transducers.

and may adversely affect transistor function. Finally, bulk ties (vias to substrate) were included at the transistor level to optimize mode confinement in the x-direction in the FEOL of the process.

4.3 Experimental Results

The PnC-confined RBTs were fabricated by IBM and realized without any post-processing or packaging. A cross-sectional SEM of the PnC RBT is presented in Fig. 4-6.

The DC response of the sensing transistor is shown in Fig. 4-7 and exhibits expected FET performance, despite the modifications mentioned in section 4.2. The modification from foundry-provided square vias to rectangular long vias spanning the width of the gate was seen to have no effect on transistor DC performance in this

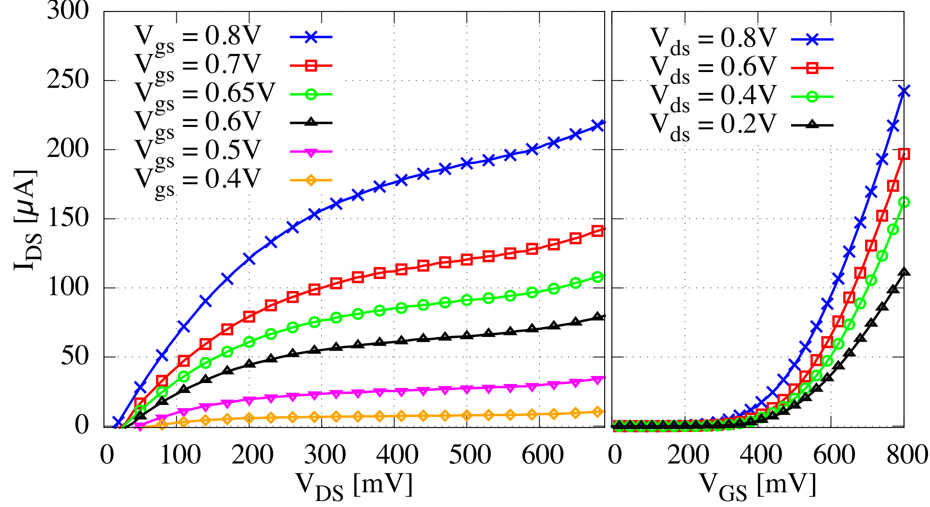


Figure 4-7: (left) $I_{DS} - V_{DS}$ characteristics and (right) $I_{DS} - V_{GS}$ of the resonator's sensing FET showing expected transistor response. In operation, the the sensing FET was biased at $V_{DS} = 0.6\,\mathrm{V}$ and $V_{GS} = 0.65\,\mathrm{V}$.

design.

For RF operation, the driving MOSCAP gates are biased in inversion at $V_A = 1\,V$ while the sensing transistor is biased in saturation with drain voltage $V_{DS} = 0.6\,V$, gate voltage $V_{GS} = 0.65\,V$, and drain current $I_{DS} = 95\,\mu A$, well within electromigration limits. This operating point has been selected to maximize the current sensitivity to relative change in channel mobility. The power dissipated by the sensing FET at its DC operating point is $57\,\mu\mathrm{W}$.

Resonators were tested in a standard two-port configuration in a Cascade PMC200 RF probe system. TRL calibration up to the probe tips was carried out at room temperature with -10 dBm input power and 2kHz IF BW with 50 averaging traces using an Agilent PNA N5225A. Devices were measured under continuous N_2 purge to reduce electrostatic discharge events. The overall input-to-output electromechanical transconductance g_m is obtained from the de-embedded Y parameters as per the definition for a MOSFET [61],

$$g_m = i_{out}/v_{in} = Y_{21} - Y_{12} \tag{4.6}$$

Devices were de-embedded using their response at $V_A = 0\,V$ on the driving MOSCAPs,

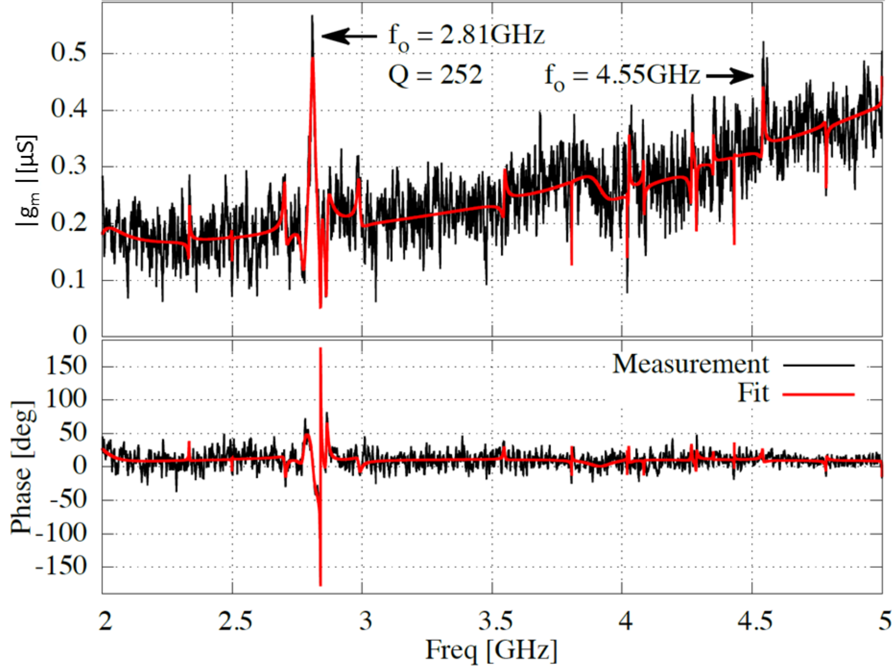


Figure 4-8: Measured mechanical transconductance $g_m = Y_{21} - Y_{12}$ of the fabricated PnC RBT. Measured frequency response of the PnC-RBT along with the fit generated using a 24-pole rational transfer function in MATLAB.

corresponding to the resonator "Off" state to suppress the mechanical mode. An 11-point running average filter is applied to the data for smoothing before fitting a rational transfer function with 24 poles to extract a Q of 252 at the 2.8 GHz resonance. The result of this fit along with the measured frequency response are plotted in Fig. 4-8. The spurious mode at 4.55 GHz corresponds to the high-frequency mode in the simulation (Fig. 4-10) but is not distinguishable above the feedthrough floor and it is intrinsically lower Q.

This design shows a 8× boost in Q over the previous generation CMOS-integrated RBTs with a 2.5× improvement in $f.Q$ product in [15] with only a 2× increase in overall footprint. The PnC RBT also shows a wide spurious-free spectral range extending up to 4.5 GHz.

The importance of design symmetry in the Z-direction maintained by using long wall-like vias instead of the standard foundry-provided square vias is evident from Fig. 4-9. Both of these measurements were obtained at the same DC operating point

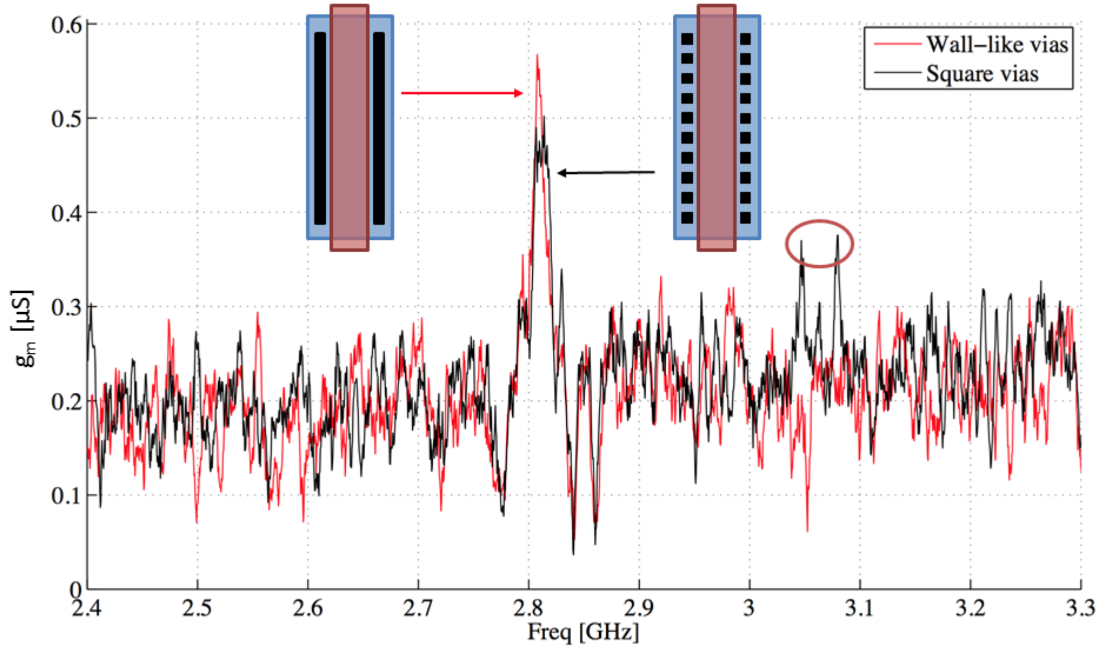


Figure 4-9: Comparative response of modified long wall-like vias used in resonator design versus regular foundry-provided square vias. The design using foundry-provided square vias shows a distorted peak with low Q along with additional spurious modes.

as in Fig. 4-8. Both RBTs were fabricated on the same die and are expected to have closely matches layer thicknesses, as justified by the exact overlap of the resonance frequency. A comparison of the plots shows that the resonant structure with the modified wall-like vias that span the entire length of the cavity for contacting the driving MOSCAPs and the sensing FET demonstrates higher amplitude and less distortion of the resonance peak. The resonant structure with square vias not only shows a distorted, low amplitude main peak, with a reduced Q of 160, but also suffers from high amplitude spurious modes close to the primary peak. It is hypothesized that the discontinuities introduced by the square vias in the Z-direction lead to scattering points within the resonant cavity which reduce the Q of the resonant peak. This also emphasizes the importance of such a Z-direction symmetric design over the ABR-RBT.

4.4 Finite Element Modeling

Mechanical properties of various materials in the CMOS stack are often unknown (for instance passivation materials such as SiCOH) or not shared by the foundry (such as details of stress liners). The experimental response of the PnC-RBT is used to perform finite element modeling in COMSOL by comparing the simulated response to the measured frequency response. The dimensions of the stack layer thicknesses as well as lithographically defined dimensions are extracted from the SEM cross-section (Fig. 4-6) of the final structure. Mechanical properties of various materials found in the FEOL and BEOL stack, such as Young's modulus, density and poisson ratio are tweaked within expected limits to obtain the best match between simulation and measurement to extract exact material properties of the stack for future designs.

The FEM simulation is carried out by using the extracted dimensions of the resonant structure and applying a small signal 26.5 MPa stress at the resonator driving gates corresponding to the calculated stress when the MOSCAPs are biased in inversion and an RF input signal of -10 dBm is applied to the driving gates. Mechanical properties were varied within a plausible range for each material to obtain a response that is well-matched to the experimental results. The resultant mode shapes and frequency response from COMSOL simulation is shown in Fig. 4-10 in good agreement with the measured frequency response of a 2.8 GHz resonator presented in Fig. 4-8. Properties of the various FEOL and BEOL materials in the structure simulated here are given in Table 4.1.

The simulated frequency response in Fig. 4-10(c) shows the average stress at the sensing FET channel. The structure exhibits two mechanical modes at 2.8 and 4.5 GHz. Both modes show good confinement of the resonant mode by the PnC with leakage restricted to the substrate. The mode at 2.8 GHz (Fig. 4-10(a)) is a PnC surface mode (decaying into PnC and substrate) and has a higher Q of 903 [77]. The mode at 4.5 GHz (Fig. 4-10(b)) penetrates less into the PnC as it is located deep inside the PnC frequency bandgap. However the increased radiation losses in the plane of the transistors leads to an overall Q reduction of this mode.

Overall, the Q from simulation is expected to be much higher than the Q from measurement for the following reasons:

- The inter-metal dielectric is a porous SiCOH ultralow-k dielectric [78] and is expected to be a significant source of viscoelastic damping [79]. However, relevant material properties could not be disclosed by the foundry or were unknown and hence viscoelastic damping was not included in the simulation which only considers radiation losses in the $x-y$ plane of the cavity.
- The simulation is a 2D plane strain approximation which does not account for the scattering along the Z-direction due to finite cavity depth as well as the abrupt termination at the ends of the MOSCAPs and FET.

4.5 Conclusion

Using some of the insights obtained from the ABR-confined 1st generation of CMOS-RBTs, acoustic isolation in the form of phononic crystals was considered for the 2nd generation of CMOS-integrated resonators. These phononic crystals are designed in the back-end-of-line of a standard CMOS process by patterning high impedance metal routing layers and vias with the low impedance passivation material to generate acoustic bandgaps that prevent the propagation of energy in certain frequency ranges. Such PnC confined RBTs show minimal performance degradation due to the minimized DRC violations in such a design, while the superior acoustic confinement in the form of PnCs results in a Q of 252 which is an $8\times$ improvement (with a $2.5\times$ improvement in $f.Q$ product) over the previous generation. A resonance peak at 2.81 GHz is demonstrated with spurious free range extending beyond 4 GHz with a footprint of $5\mu m \times 7\mu m$.

One of the only DRC rules violated in the creation of these devices includes the design of long vias that span the length of the resonant cavity (which is offered as a design option in processes such as TSMC) to ensure Z-directional uniformity. The importance of Z-direction uniformity of the resonance cavity is emphasized by the

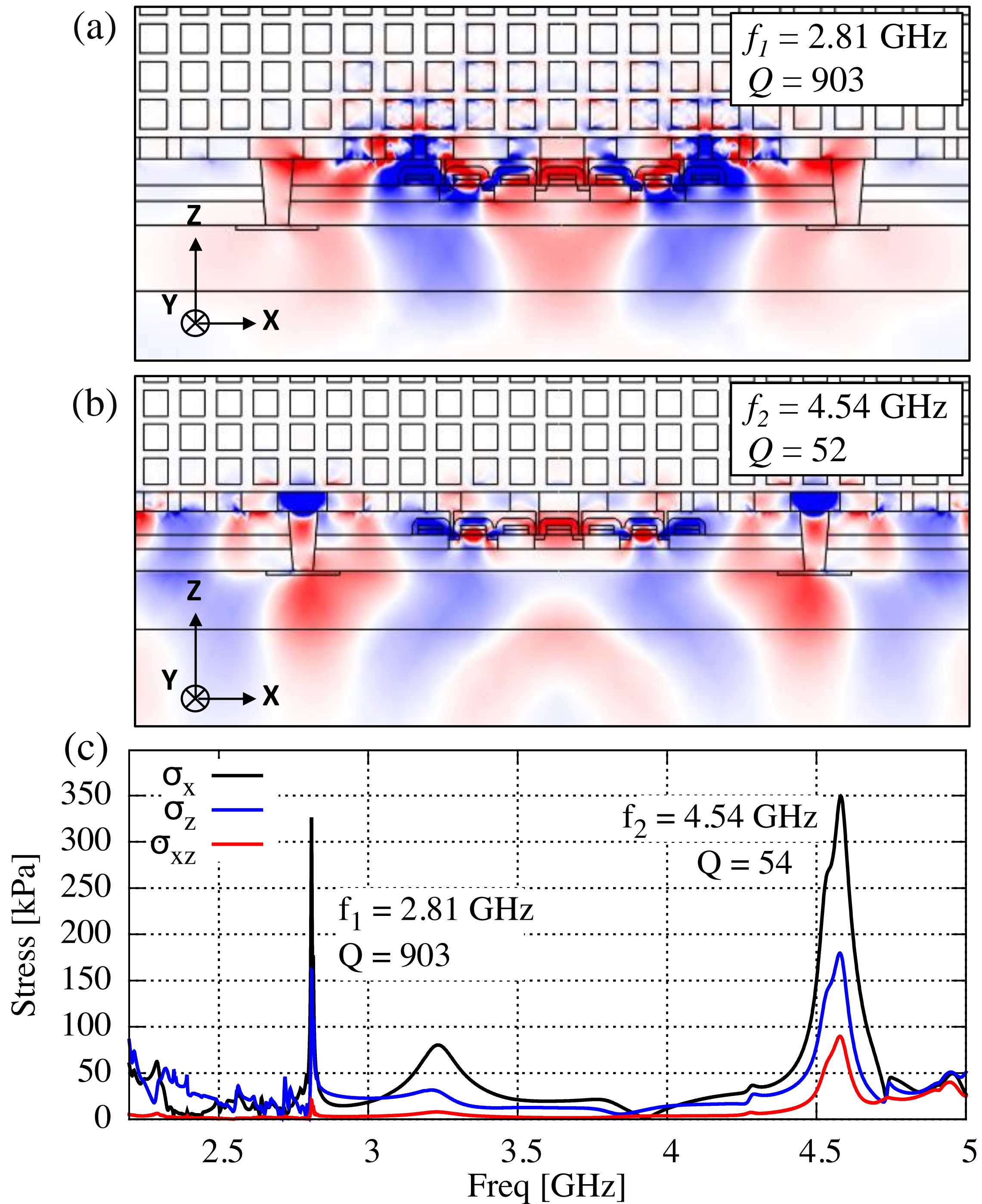


Figure 4-10: (a) X-stress at 2.81 GHz in 2D PnC-RBT structure showing Q of 903 with acoustic losses confined to substrate. (b) X-stress in resonant structure at 4.54 GHz with Q of 52 showing losses restricted to FEOL and substrate (c) Frequency response from 2D FEM COMSOL simulation of PnC resonator with resonances at 2.81 GHz (Q of 903) and 4.5 GHz.

design of a resonator with the standard IBM square vias which shows a degraded Q and presence of spurious modes close to resonance peak. Such devices may be used to reverse engineer and characterize the properties of the materials in the CMOS stack by fitting the finite element simulation response to the resonator response, thus creating a database for future designs. Performance improvements may be achieved by maintaining the uniformity of the PnC down to the resonance cavity, designing well inside the acoustic bandgap and using techniques such as differential drive and sense and mechanical coupling to improve resonator Q and parasitic feedthrough. The resonant frequency and mode may be carefully chosen to evanescently decay into the buried oxide layer and underlying handle wafer [74].

An important consideration while choosing a technology for design of a CMOS PnC is the materials available in the BEOL stack. For most technologies, the inter-metal dielectric usually provides a low acoustic impedance background for PnC design. The high-impedance material surrounded by this dielectric is in the form of either vias or routing metals. In a technology such as IBM's 32nm SOI, both routing metals and vias are comprised of high-impedance Cu surrounded by a low-impedance SiCOH$\dot{\text{T}}$he use of both routing metals and vias for PnC design provides a wide design space to optimize PnC bandgaps, leading to relaxed mechanical design constraints. However, electrical routing to the resonator is challenging in this scenario as it mechanically perturbs the interface between the PnC and the resonant cavity, affecting the boundary conditions and hence overall device performance. In this work, the vias from the drain of the driving MOSCAPs were removed, and the first layer of metal was placed off-center from the existing vias to minimally affect the mechanical structure of the PnC.

On the other hand, some IC technologies use routing metals with acoustic impedance comparable to that of the inter-metal dielectric such as Al surrounded by $SiO_2\dot{\text{I}}$n this case, the routing metals negligibly affect the PnC dispersion characteristics and the PnC is solely designed using the high-impedance vias (such as tungsten or copper), if available. For such technologies, the electrical routing to the resonator does not interfere with the PnC mechanical design and there are no severe impediments to

electrical routing to the resonator. However, the mechanical design of a PnC with wide frequency bandgaps is challenging as it is restricted by the lack of flexibility in via dimensions.

Chapter 5

The Piezoelectric RBT

In the previous chapters, we explored CMOS-integrated resonators employing FET-based sensing to realize small-footprint, high-Q, fully unreleased MEMS resonators. These solid-state devices require no post-processing or packaging and can be integrated with IC circuits with minimal parasitics due to their fabrication at the transistor level of the CMOS stack.

However, these CMOS-integrated RBTs have certain performance limitations based on the materials and the transduction mechanisms available in the standard CMOS stack. Dielectric transduction with Si-based resonators, is usually less efficient as a driving mechanism as compared to mechanisms such as piezoelectricity, resulting in $10 - 100\times$ smaller driving forces for the same voltage applied across a dielectric film of the same physical dimensions as compared to a piezoelectric film. This results in a small output signal and high motional impedance R_m (Fig. fig. C-1), which leads to high insertion losses in filters, and difficulty in designing a feedback loop for oscillators. Furthermore, since high transduction efficiency for a dielectric based drive is usually dependent on utilization of thin films, the power handling capacity of these devices is correspondingly low.

Exploration of piezoelectric materials for actively-sensed resonators is an attractive direction due to the high transduction efficiency, also expressed by the performance metric k_{eff}^2 (appendix B) for piezoelectric devices resulting in low insertion losses measured in such devices. Furthermore, due to the manufacturing difficulties

in depositing thin piezoelectric films with minimal leakage and good piezoelectric properties, these usually have thicknesses on the order of 100 s of microns, improving their power-handling capacity.

In the past, several piezoelectric materials such as quartz, ZnO, AlN and PZT have been chosen for use in a microdevices based on their unique properties for the desired application [3]. For instance, lead zirconate titanate (PZT) is a piezoelectric material with extremely high coupling coefficients, making it attractive for macroscale sensors and actuators [80]. Crystalline quartz has also been extensively explored and commercialized for timing applications as quartz has a very low temperature coefficient of frequency resulting in highly reliable resonators [81]. Piezoelectrics such AlN and ZnO have relatively weak coupling coefficients (Table 5.1) but they have high quality factors that make them especially suitable for high frequency resonators [82], [83].

Piezoelectric devices have been traditionally designed and fabricated with piezoelectric films such as AlN deposited on the top surface of the resonant structure. One category of such devices includes thickness mode resonators such as FBARs which utilize the e_{33} coefficient to drive and sense vibrations. For most materials the e_{33} coefficient is greater than the e_{31} coefficient (Table 5.1), making longitudinal transduction more efficient. However, FBARs are restricted to a single resonance frequency and its harmonics per wafer. Such thickness mode FBAR devices also require extremely thin films to scale to higher frequencies which makes manufacturing difficult and films leaky. Furthermore, the large sensing area required for high signal out-

Table 5.1: Comparison of piezoelectric coupling coefficients of common piezoelectric materials [3].

Material	e_{31} (C/m^2)	e_{33} (C/m^2)
AlN	-0.48	1.55
ZnO	-0.61	1.14
PZT-4	-5.2	15.1
PZT-5A	-5.4	15.8
Quartz	NA	0.17

put proportionally increases the device footprint which is undesirable for electronic components.

Another category of piezoelectric devices is the thin film-piezoelectric on Si (TPoS) resonators which utilize the transverse piezoelectric coefficient e_{31} of a material such as AlN to induce lateral vibrations by squeezing the piezoelectric film in the vertical direction. Enhanced power handling and Q-boosting has been demonstrated in these devices by inclusion of Si into the resonant cavity [84]. The Q-boosting of Si based piezoelectric resonators may be understood based on the higher theoretical Q limits in Si as compared to piezoelectrics such as AlN, which are $2 - 3\times$ higher in the case of Siat low frequencies, and more than an order of magnitude higher above GHz frequencies [9].

Power handling is a measure of the amount of power that may be delivered or applied to a resonator before giving rise to nonlinearities. In piezoelectric resonators, the primary source of this nonlinearity is the non-linear spring constant, which leads to a dependence of the resonance frequency on vibration amplitude and leads to noise and distortion in the output signal. The nonlinearity limitations in different materials are a function of material properties and may be compared by normalizing the maximum energy by the volume of the structure, also known as the energy density. Single crystal Si resonators show orders of magnitude higher energy densities that most piezoelectric materials such as quartz [85], improving their linear range of operation.

Given the limitations faced by passive devices for scaling to multi-GHz frequencies (section 1.1.2), active FET-sensing using piezoelectric films in an Si-based resonator is explored as part of this work. Due to the (i) high transduction efficiency of piezoelectric films, especially for longitudinal transduction in the e_{33} direction, (ii) Q-boosting due to presence of Si in resonant body, (iii) enhanced power-handling capability, also due to Si in the resonant body; we explore the design of piezoelectric RBTs which employ sidewall-deposited piezoelectric films in place of the gate dielectric in an Si-based RBT configuration. The physics behind the operation of such a structure is different from a dielectric-based RBT and is considered below.

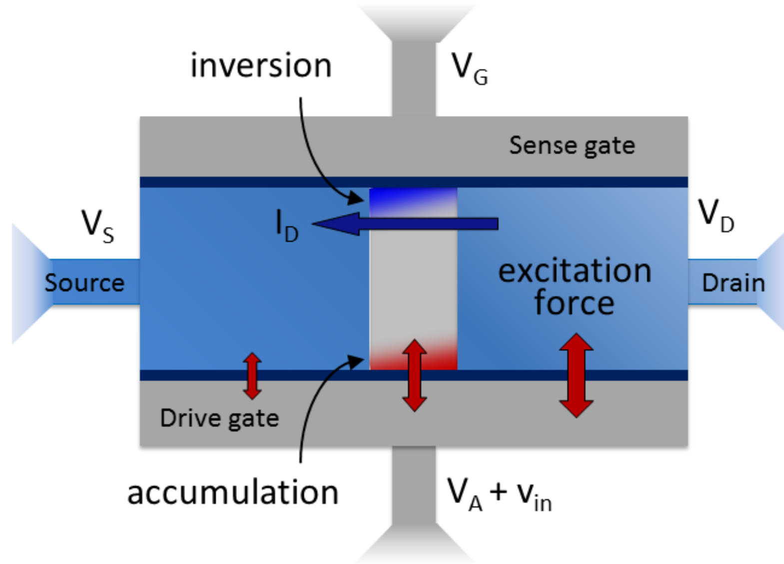


Figure 5-1: Top-view schematic of piezoelectrically transduced Resonant Body transistor. AlN piezoelectric films (dark blue) are used in place of the gate oxide for a double-gate transistor for sensing and actuation. Gates (gray) consist of metal such as molybdenum.

5.1 Physics of Piezoelectric RBTs

A piezoelectric RBT is envisioned as a two-gate transistor with piezoelectric films such as AlN in place of the gate oxide (Fig. 5-1).

On the driving side, acoustic vibrations are driven piezoelectrically, through the e_{33} coupling coefficient resulting in a higher driving stress and larger amplitude of vibrations. On the sensing side, the piezoelectric film experiences strain due to the longitudinal vibrations in the structure at resonance. This results in a change in the polarization and hence electric field across the film through the inverse piezoelectric coefficient. This is modeled as a modulation in net gate voltage and is usually the dominant term over piezoresistive and capacitive contributions.

A simple rectangular-shaped longitudinal mode device such as the one shown in Fig. 5-1) may be easily analyzed based on the theory presented in [86]. On the drive side, the back gate or driving gate of the piezoelectric RBT is biased into accumulation by applying a DC voltage V_A, and a small AC voltage $v_{ac}e^{j\omega_n t}$ to the drive gate to launch acoustic waves into the device. The source of the transistor is tied to ground

while the drain is biased at V_D. Thus, the average driving voltage applied across the back gate is $(V_A + v_{ac}e^{j\omega_n t} - V_D)/2$. and an average value for the electric field across the piezoelectric film of thickness g is given as $(V_A + v_{ac}e^{j\omega_n t} - V_D)/2g$. For certain device configurations in which the drive and sense are separated due to mechanical coupling, the average electric field simplifies to $(V_A + v_{ac}e^{j\omega_n t})/2g$.

Using the constituent equations of piezolectricity B.4 included in appendix B, the resultant in-plane stress in the piezoelectric film, σ_{pelec}, along the direction of the electric field, which is also along the direction of the c-axis is given by:

$$\sigma_{pelec} = e_{33}(\frac{V_A - V_D}{2g} + \frac{v_a c e^{j\omega_n t}}{2g}) \tag{5.1}$$

Hence the AC stress, σ_{pAC}, relevant for the amplitude of vibration calculation, is given by

$$\sigma_{pelecAC} = e_{33}\frac{v_a c e^{j\omega_n t}}{2g} \tag{5.2}$$

This may be used to calculate the amplitude of vibrations U_0 using the analysis for forced longitudinal vibrations in a damped bar [59] where the resonance frequency is given by:

$$f_n = \frac{n}{2L}\sqrt{\frac{c_{11}}{\rho}} \tag{5.3}$$

where f_n is the resonance frequency, L is the length along the resonant dimension, n is the harmonic, c_{11} and ρ are the effective stiffness coefficient along the direction of vibration and effective density respectively.

It may be shown that in addition to the piezoelectric effect, electrostriction also contributes to stress in the AlN. However, electrostrictive stress is more than two orders of magnitude smaller than the piezoelectric stress and is ignored for the subsequent analysis.

On the sensing side, assuming a DC bias point where source is tied to ground, gate is biased at V_{GS} with respect to source and drain is biased at V_{DS}, with a transistor threshold voltage V_T, the transistor drain current for long-channel devices is given by two simple relations:

In the linear regime, when $V_{DS} < V_{GS} - V_T$, for a sidewall transistor with sidewall depth h, we have the DC current I_{DCLin} given as

$$I_{DCLin} = \frac{h}{L_{gate}} \mu_n C_{piezo} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} \tag{5.4}$$

In the saturation regime we have $V_{DS} \geq V_{GS} - V_T$, and the current I_{DCsat} is given as

$$I_{DCsat} = \frac{h}{2L_{gate}} \mu_n C_{piezo} (V_{GS} - V_T)^2 \tag{5.5}$$

The small signal output current at the mechanical resonance frequency has three different components:

- Piezoelectric: Mechanical strain across the piezoelectric gate insulator induces a small signal gate voltage that modulates the drain current.
- Piezoresistive: Mechanical strain at the FET channel induces a small signal change in drain current due to the piezoresistive modulation of channel mobility.
- Capacitive: Mechanical strain across the FET piezoelectric layer results in a change in gate capacitance which modulates the drain current.

The physics and relative contributions of these are examined below.

Piezoelectric Contribution

At resonance, the stress field in the piezoelectric film results in an electric displacement vector, $[D]$ at its surface given by B.3:

$$[D] = [e].[S] \tag{5.6}$$

where $[S]$ is the strain vector. This induces a net voltage across the film which may be calculated by integrating the resultant electric field vector $[E]$ over the thickness of the film, given by:

$$V_{piezo} = \int_{thickness} [E_{piezo}] dx = \frac{1}{\epsilon_0 k_{piezo}} \int_{thickness} [e][S] dx \tag{5.7}$$

These matrices simplify to single values in case of a simple mode such as that of a longitudinal bar mode which is under consideration here but they have been retained in their original form to indicate that the same equation may be used for more complex 2D modes such as wineglass or Lamé modes.

This induced voltage may be considered as an additional voltage that appears at the gate of the transistor based on the analysis in [86] and thus modifies the transistor equations as:

$$I_{DCLin} = \frac{h}{L_{gate}} \mu_n C_{piezo} (V_{GS} + V_{piezo} - V_T - \frac{V_{DS}}{2}) V_{DS} \tag{5.8}$$

in the linear regime and in the saturation regime:

$$I_{DCsat} = \frac{h}{2L_{gate}} \mu_n C_{piezo} (V_{GS} + V_{piezo} - V_T)^2 \tag{5.9}$$

Piezoresistive Contribution

The standing acoustic wave in the resonator results in a time-dependent strain along the channel which modulates the mobility due to the piezoresistive effect similar to the case of the CMOS-RBTs. Based on 2.6 and appendix D we may express this as:

$$\frac{\Delta \mu}{\mu} = [\pi_{Si-(110)}][\sigma_{Si}] \tag{5.10}$$

where $\pi_{Si-(110)}$ is the piezoresistance matrix of Si for a typical (001) wafer and σ_{Si} is the stress vector in the same plane. Thus, the small signal output current due to this effect is given by:

$$i_{pres} = I_{DC} \frac{\Delta \mu_n}{\mu_n} \tag{5.11}$$

The value and sign of the piezoresistive coefficient along the direction of the current determines whether this contribution is in or out of phase with the piezoelectric contribution.

Capacitive Contribution

Apart from the piezoelectric contribution to the output AC current, we will also have an AC current resulting from the change in the gate capacitance provided by the

piezoelectric film. The insulating AlN film forms a gate capacitor which squeezes and expands due to the acoustic wave, and this results in small signal modulation of the DC drain current at resonance. Thus, this current is positive when the capacitance increases, i.e. when the piezoelectric film is compressed. Calculating the capacitance per unit area when not at resonance, C_{piezo}, and the change in this capacitance at resonance, ΔC_{piezo}, when the piezoelectric film expands to thickness $g + \Delta g$, we have,

$$\Delta C_{piezo} = \epsilon_0 k_{piezo} (\frac{1}{g} - \frac{1}{g + \Delta g}) \sim \epsilon_0 k_{piezo} \frac{\Delta g}{g^2} \tag{5.12}$$

where k_{piezo} is the relative permittivity of the piezoelectric film.

Δg may be calculated as the net increase in the thickness of the piezoelectric film by integrating the strain function over the thickness of the film.

Finally, the change in output current due to this change in capacitance is simply given by:

$$i_{cap} = I_{DC} \frac{\Delta C_{piezo}}{C_{piezo}} \tag{5.13}$$

The total modulation current in both, the linear and saturation regimes is thus given by summing these three contributions in that regime:

$$i_{out} = i_{pelec} + i_{pres} + i_{cap} \tag{5.14}$$

It may be shown that typically the capacitive contribution is 5 orders of magnitude smaller than the piezoelectric contribution and may be ignored. On the other hand, the relative magnitude of the piezoresistive contribution with respect to the piezoelectric contribution depends on the DC bias point of the device but is expected to be about 12× lower at the chosen operating voltages in the saturation regime.

A detailed analysis and modeling of such a device is presented in [49].

5.2 AlN as a candidate material for the piezoelectric RBT

While some piezoelectric materials such as quartz and PZT may not be integrated into a CMOS process due to the risk of contamination and manufacturing difficulties, materials such as AlN are CMOS-compatible and have already been demonstrated on top of the CMOS stack [12]. GLOBALFOUNDRIES has recently started offering an AlN on CMOS process as a post-CMOS MEMS or piezoelectric option in their fabrication facility. Thus AlN is considered as a candidate material for the piezoelectric RBT.

AlN is a wide bandgap semiconductor with a bandgap of $6.01 - 6.05\,\mathrm{eV}$ at room temperature. It crystallizes in wurtzite crystal structure which is a member of the hexagonal crystal system with lattice constants $a = 3.11\,\mathrm{\AA}$ (which gives the length of the sides of the diamond forming the base of the unit cell) and $c = 4.98\,\mathrm{\AA}$ (which is the height of the unit cell) [87]. In such a structure, 4 Miller-Bravais indices indicate the position along the three basal axes a_1, a_2 and a_3 in the hexagonal plane with the c axis perpendicular to it, which is also referred to as the [0001] direction along the crystal. The lack of inversion symmetry or centrosymmetry in AlN and other materials with wurtzite crystal structure such as ZnO and GaN results in such materials demonstrating properties such as piezoelectricity [88].

Several techniques such as pulsed laser deposition (PLD) [89], metal-organic chemical vapor deposition (MOCVD), sputtering [90] and molecular beam epitaxy (MBE) [91] are some possible techniques for the synthesis of AlN films on Si. MBE is the preferred technique of growth for high film purity and good c-axis orientation at the cost of a reduced growth rate. On the other hand, MOCVD and sputtering offer the advantages of high deposition rate, good uniformity and low temperature with good conformality in coating sidewalls of features. In recent years, it has been possible to reliably sputter AlN films with good c-axis orientation and piezoelectric properties on the sidewalls of a material such as Si or SiC [92]. This allows the design of sidewall transduction in piezoelectric resonators with lithographically defined frequencies

and high transduction efficiency due to the e_{33} coefficient, leading to extremely low motional impedance values for such sidewall transduced MEMS resonators [56].

TEM images show that with RF sputtered films, a thin semi-crystalline interface layer of AlN forms to a thickness of about 4 nm from the surface of the Si and columnar AlN originates from this interface layer extending through the remainder thickness of the material with c-axis oriented along the direction of growth [93]. It is noted here that for good piezoelectric properties and c-axis orientation perpendicular to the substrate faces, the surface and sidewalls need to as smooth as possible as the many planes of a rough surface will result in localized crystal growth in a variety of different directions [94] with poor crystallinity. Suitable nucleation layers such as Pt may be used to achieve good c-axis orientation as the lattice constants of hexagonal AlN match well with Pt resulting in quasi-epitaxial growth [95], [96]. For any roughness level of substrate, sputtered AlN will grow as a a highly granular microstructure in which the grains are long and needle shaped with the long axis coincident with the c-axis and oriented perpendicular to the substrate. X-ray diffraction topography is a measurement technique commonly used to study the irregularities in a non-ideal crystal lattice such as thin film AlN growth and the full width at half maximum (FWHM) of the resulting rocking curves indicate the mosaicity of the grains, with larger FWHM indicating a greater spread in angles of c-axis orientations. The overall piezoelectric coefficient is obtained by summing the piezoelectric contribution of each grain along the direction perpendicular to the surface and weighing it by the distribution of the grains' orientation. Thus poorly oriented films have compromised piezoelectric coefficients and k_{eff}^2 and any resonator made with such a film would suffer in Q and hence bandwidth.

Thus, sidewall transduction of AlN with sputtered films has been recently possible and is considered for this work for the higher transduction efficiency associated with the e_{33} piezoelectric coefficient. Furthermore, the relatively high dielectric strength (14 kV/mm) of AlN, along with its high resistivity ($1e13\,\Omega$cm) and thermal expansion coefficient similar to that of Si makes it an excellent candidate for microelectronics applications. Given these benefits of AlN films with the possibility of CMOS in-

Table 5.2: Some options of electrode metals for Piezoelectric RBT with AlN comparing their longitudinal acoustic impedance Z_a, and resistivity ρ.

Material	Z_a	Z_a/Z_{AlN}	ρ (nΩ m)
AlN	$3.44e7$	1.00	NA
Mo	$7.98e7$	0.43	53
Pt	$8.21e7$	0.42	105
Au	$7.03e7$	0.49	22
Al	$1.74e7$	1.98	28
Ni	$4.97e7$	0.69	69
Ti	$2.73e7$	1.26	420
W	$1.01e8$	0.34	52
Ag	$3.92e7$	0.88	16

tegration, we explore the design of piezoelectric RBTs which employ AlN films for piezoelectric transduction.

Metals such as Mo, Au and Pt etc. are usually used as the metal electrodes with AlN for their good acoustic impedance match and low electrical resistance [97]. In this process, Mo is chosen as the electrode material for its acoustic impedance (Z_a in the longitudinal direction) match with AlN, high conductivity (ρ) as compared to metals such as Pt, Ni or Ti and the low loss as compared to materials like Au, Ag and Al, which is necessary for design of high-Q devices [97]. Acoustic impedance and conductivity for some candidates for the metal electrode are given in Table 5.2.

The most important fabrication constraint for sidewall transduction based piezoelectric devices is the ability to conformally deposit high-k_{eff}^2 non-leaky piezoelectric films on vertical sidewalls with a controlled thickness. To experimentally verify the ability to deposit AlN films for sidewall transduction, test structures with fins, trenches and other geometric shapes of various dimensions were fabricated to observe the conformality of AlN sputtering on vertical, smooth sidewalls of Si. The film quality is strongly dependent on sidewall smoothness and cleanliness so wafers need to be thoroughly cleaned and possible thermally oxidized and stripped after processes such as DRIE which may leave residues on sidewalls. Cross-sectional images of test structures after deposition of 50 nm of AlN and 200 nm of Mo are included in Fig. 5-2.

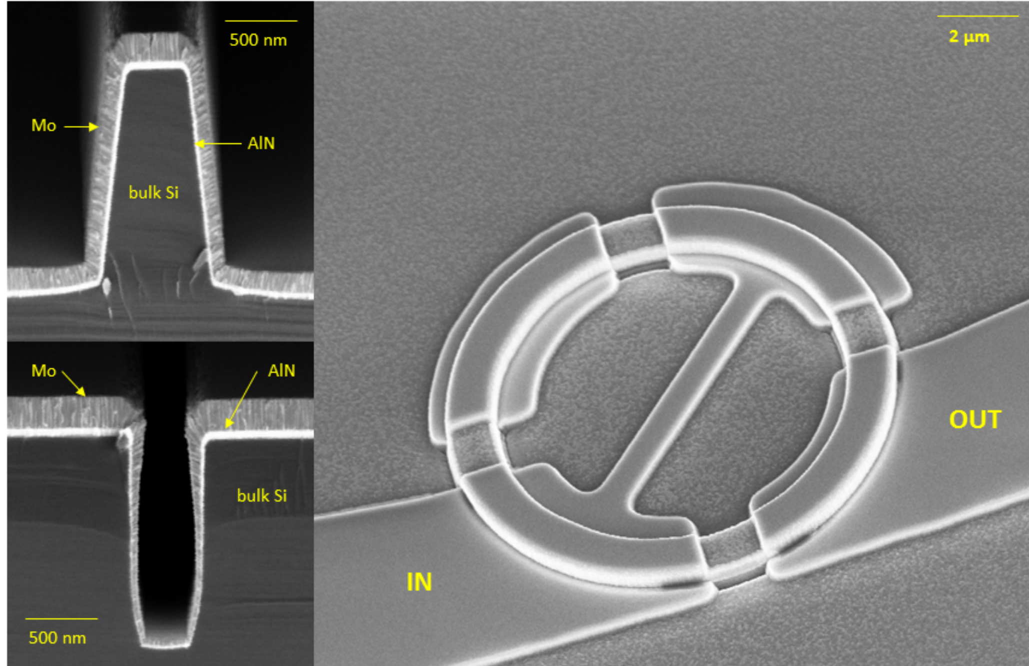


Figure 5-2: (left) Cross-sectional SEM of fin and trench structures in bulk Si showing conformal deposition of AlN and Mo films, sidewall film thicknesses are approximately 1/2 to 1/3 those at the top. (right) Sample test structure in the form of a ring, expected resonance is wineglass mode.

5.3 Design of the Piezoelectric RBT

The small signal model of such a device is similar to that of the CMOS-RBT with the only difference being the addition of a piezoelectric term on the driving side which modulates the effective gate voltage which may be expressed as $V_{GSeff} = V_{GS}+V_{piezo}$. The electromechanical signal at resonance in a piezoelectric RBT is much larger than a dielectric-based device due to the high driving forces across piezoelectric films and the presence of the additional sensing mechanism due to the piezoelectric effect across the gate insulator. This results in a significantly improved input-to-output transconductance as compared to a dielectric RBT. Additionally, due to the large voltages induced across the piezoelectric film in the sensing transistor gate, the piezoelectrically induced voltage at the gate may be significant compared to the DC bias voltage applied to it. Since the output signal is no longer restricted to small signal behavior, non-linearities and rectification behavior may be observed in the device as shown in Fig. 5-3 due to switching between transistor cut-off, linear and saturation

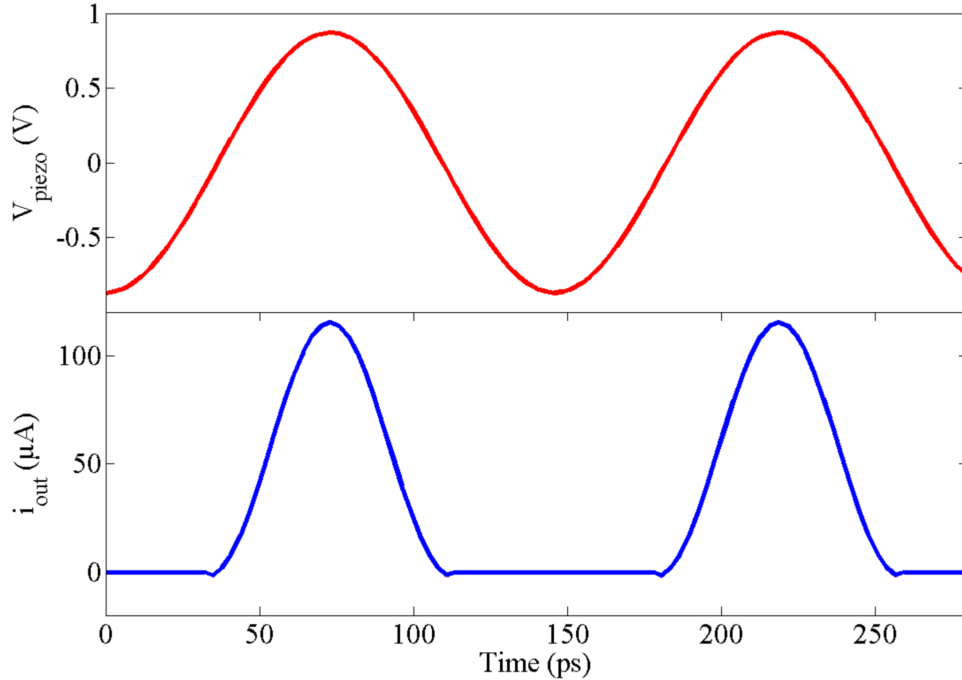


Figure 5-3: Plot showing non-linear output current for linear piezoelectrically induced voltage at the sensing gate. Half-wave rectification behavior is expected in the output current as the FET switches between subthreshold and linear regimes.

regimes.

The net RF output current in such a device is directly proportional to the DC output current and hence scales according to the transistor small-signal model. The effective motional impedance (R_X) in this case may be defined as the reciprocal of the input-to-output transconductance and may be optimized by changing the position and thickness of the piezoelectric films within the device, the thickness of the metal electrodes, the width of the device, which determines the frequency of operation etc. Finally, these trends in the motional impedance may be compared to equivalent trends in a piezoelectric resonator with identical mechanical structure but without active/FET sensing (so in this case $R_X = R_m$) to choose the optimal sensing mechanism based on application. These trends have been explored in detail in [49] and a sample figure showing the change in effective motional impedance (R_X) with thickness of the piezoelectric film is included in Fig. 5-4 as an example.

The three different mechanisms that result in the shape of this plot include:

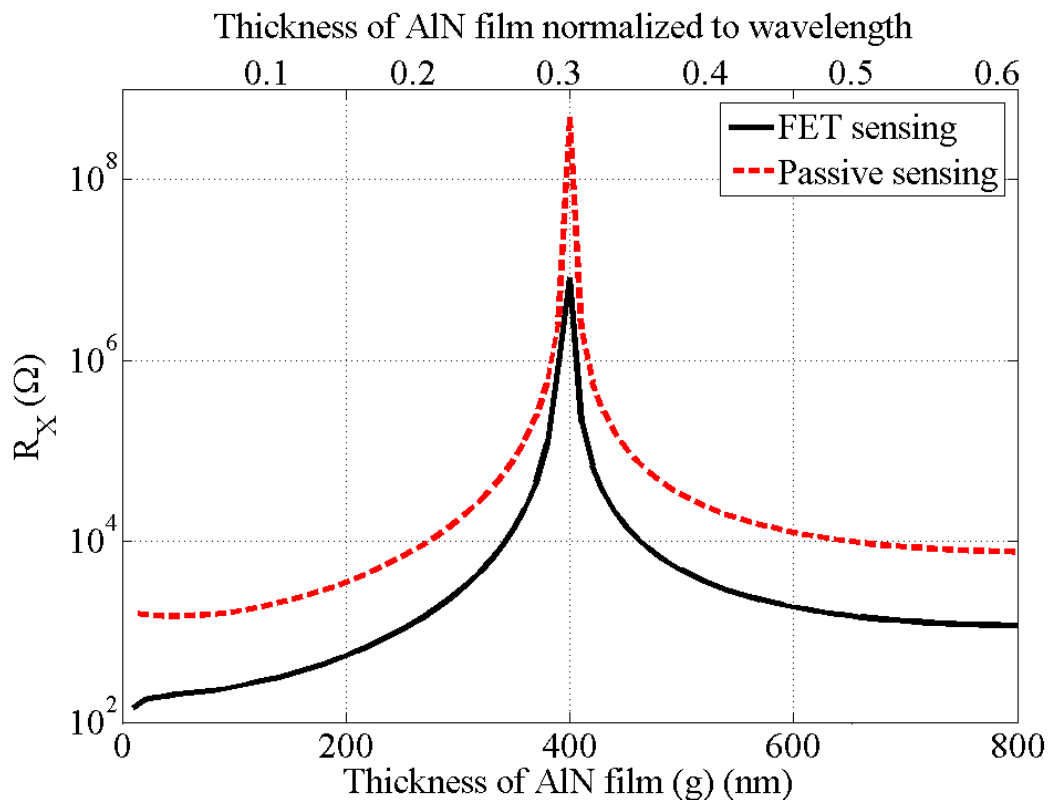


Figure 5-4: Plot comparing the motional impedance R_X for the Piezoelectric RBT with passive piezoelectric devices. Top axis shows thickness of film normalized to wavelength at frequency of 5 GHz for a longitudinal mode device operating in third harmonic.

- At low thicknesses, the gate capacitance is high, which increases the drain current at the same operating point, which increases the piezoresistive contribution to the output current and reduces R_X for thin films.

- A higher voltage is induced across a thicker piezoelectric film at the sensing gate at resonance, which reduces R_X for thick films.

- The simulation is carried out a a constant device resonant frequency, which means that the thickness of the metal electrodes is varied to maintain this frequency, which affects the relative placement of the AlN films with respect to the mode shape which again affects R_X.

In this case, a longitudinal bar resonator operating at 5 GHz is shown to have diminishing R_X at normalized thicknesses smaller than 0.3λ. This would imply that thinner piezoelectric films are desirable for minimized motional impedance at high frequencies of operation. The devices on this run were hence designed to use a 100 nm thick AlN film to minimize this R_X while avoiding leakage issues that occur at even lower thicknesses. Similar optimization was carried out to calculate the position of the piezoelectric films from the center of the device and the thickness of metal electrodes.

It may be noted that the optimized values are dependent on electro-mechanical properties of the film and metal, including experimentally measured breakdown voltage, relative permittivity, Q and k_{eff}^2 etc. These may be obtained by fabricating and characterizing test structures such as resistors, capacitors and FETs employing an identical film stack as used in the proposed design.

At this point it may be beneficial to compare the transduction efficiencies of a piezoelectric RBT versus the dielectric RBT. Overall, piezoelectric transduction efficiency is much greater than that of dielectric films and capacitive air gaps, which is offset by the much higher film thicknesses of piezoelectric films limited by fabrication processes to 100 s of nm as compared to dielectrics at < 10 nm, to avoid electrical leakage and to obtain good piezoelectric coefficients. For instance, for an applied AC voltage of 0.1 V, the stress generated across a 100 nm AlN film is 1.58 MPa while for the same voltage, the capacitively generated stress across a 10 nm SiO_2 film would be

35 kPa which is about 45× smaller. The stress generated across a high-κ dielectric like a 10 nm HfO_2 film would be 0.2 MPa which is 7× smaller. These differences would be exaggerated by higher efficiency piezoelectrics PZT and mitigated by using thinner dielectrics as the electrostatic force scales as $1/\text{thickness}^2$ but only linearly reduces breakdown voltage. However, comparing breakdown voltages in the above scenario, it is noted that a 100 nm thick film of AlN has roughly the same breakdown voltage as a 10 nm film of SiO_2 .

On the sensing side, the large induced voltages in piezoelectric materials as compared to dielectric materials allows higher efficiency sensing than piezoresistive. At resonance, the gate voltage induced on the gate of the FET due to the direct piezoelectric effect induces a small signal drain current which is upto 10× more than the the piezoresistive drain current. This results in low motional impedance (R_X) devices critical for design of oscillators and low loss filters at high frequencies. Since piezoelectric films are generally deposited at greater thicknesses, for a piezoelectric transistor this leads to smaller gate capacitance and reduced current or high power operation. For instance, using the example above, keeping all other dimensions constant, the gate capacitance of a 100 nm AlN film would be 5× smaller than that of a a 10 nm SiO_2 film.

5.4 Finite Element Analysis

The longitudinal mode devices with single ended drive and sense analyzed in section 5.1 were simulated using COMSOL multiphysics.

Single crystal Si was used for the bulk material, and AlN and Mo with rotated material properties are used to accurately simulate the material crystal orientation on the sidewalls of the device. Coupling beams to substrate were matched to $\lambda/4$ and PMLs were used to model losses beyond the beams. The devices were actuated with a small-signal drive voltage across the driving piezoelectric film and the resultant small-signal voltage across the sensing film was measured. A frequency response of a sample device is included in Fig. 5-5 and shows high-Q peaks for several different

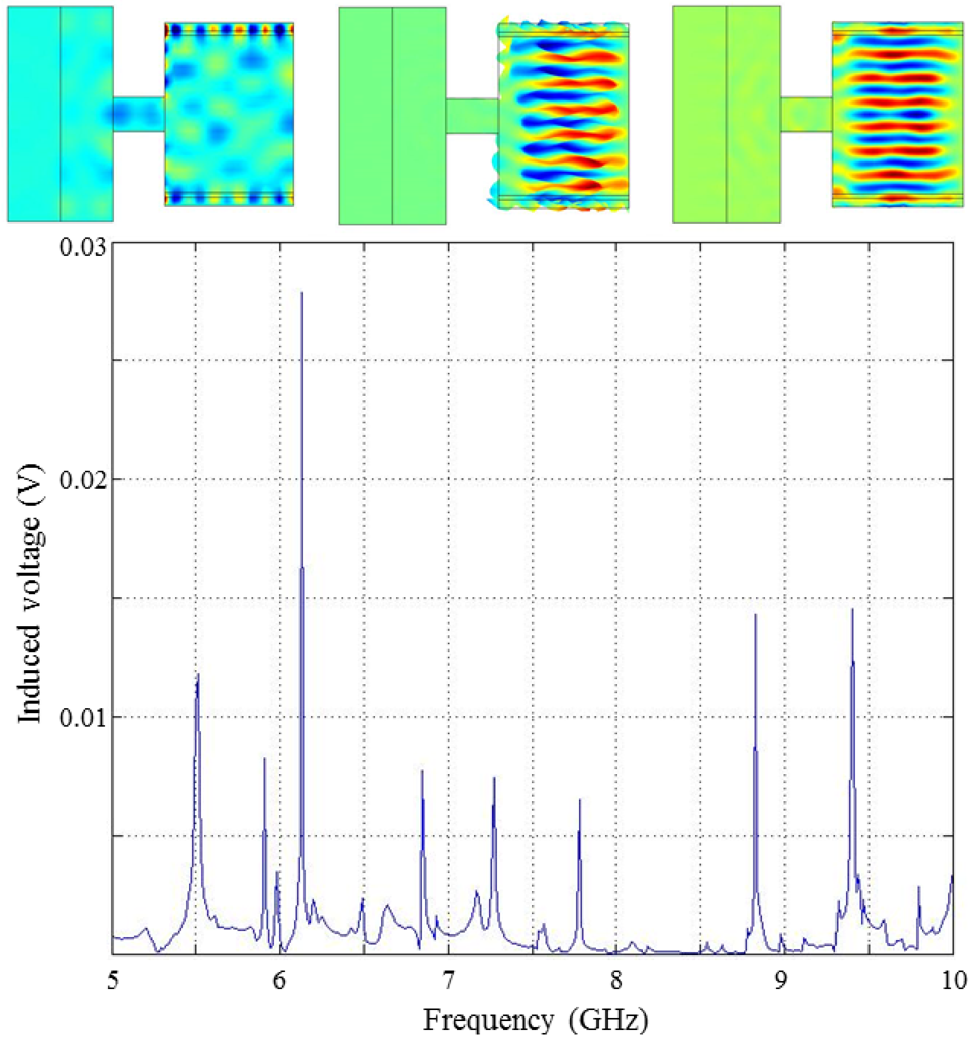


Figure 5-5: Frequency response of single-ended piezoelectric RBT showing several different resonance modes between 5 and 10 GHz. Three sample mode shapes of half of the symmetric resonant structure showing the x-displacement of various resonance modes are included above the frequency response.

resonant modes, some of which are higher order harmonics of the fundamental bulk acoustic mode. Half structures showing the stress distribution for various resonant modes are included above the frequency sweep.

While such a structure shows a high-Q resonance for the desired mode, the frequency response shows the presence of several spurious modes, some of which are higher amplitude than the resonance mode (around 5.5 GHz). Such a resonant device response requires the design of intermediate filtering stages to isolate the desired resonance resulting in increased power consumption. Spurious modes close to the desired frequency also reduce the Q of the peak due to coupling and exchange of energy between these frequencies. One method to improve the suppression of undesired or spurious modes in the frequency response of micromechanical resonators is through differential drive and sensing [98]. This has the added advantage of reducing capacitive feedthrough from input to output which contributes to significant parasitics as resonators scale to higher frequencies. Differential sensing also reduces ohmic losses in the coupling beams resulting in improved Q and lower motional resistance [99].

Along with differential drive and sensing, micromechanical resonators have also been demonstrated in mechanically coupled configurations to physically separate the input from output to reduce any feedthrough paths, for ease of routing, and to improve the motional impedance and linearity of devices [100]. The additional surface area for driving and sensing also improves power handling in mechanically coupled resonators. The disadvantages from using a differential scheme with mechanically coupled resonators include more complex routing and characterization and increased device footprint.

Differentially driven and sensed, mechanically coupled devices operating in wine-glass modes were designed with sidewall piezoelectric transduction, the frequency of operation which is given by [98]:

$$f = \frac{1}{\sqrt{2}L}\sqrt{\frac{G}{\rho}} \tag{5.15}$$

where G is the effective shear modulus of the device. In practice, in a differential

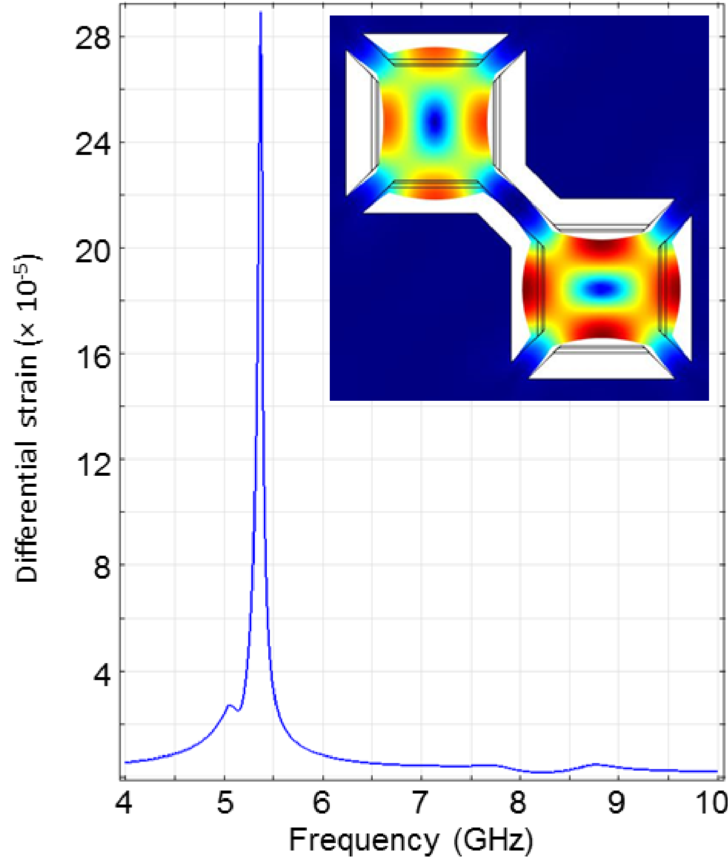


Figure 5-6: (left) Mode shape of differentially driven and sensed mechanically coupled device resonating in wineglass mode (right) Frequency response of device showing complete suppression of spurious modes.

drive configuration, regions of out-of-phase strains in the device based on the desired mode are driven with out-of-phase voltages for common mode suppression. Similarly, for differential sensing, regions of out-of-phase strains are sensed with two electrically isolated electrodes whose signals are summed 180 degrees out of phase. COMSOL simulations on these mechanically coupled, differential mode devices show a complete suppression of the square extensional common mode with the frequency response only showing the wineglass mode at the designed frequency Fig. 5-6.

The lengths of the suspension beams to substrate were designed to minimize acoustic losses at resonance. Fig. 5-7 shows an example of the peak differential strains, frequency and Q obtained on sweeping the length of the suspension beam to substrate in the COMSOL simulation. No material losses are included, however, PMLs are used to absorb any acoustic energy losses to substrate. The lengths of mechanical

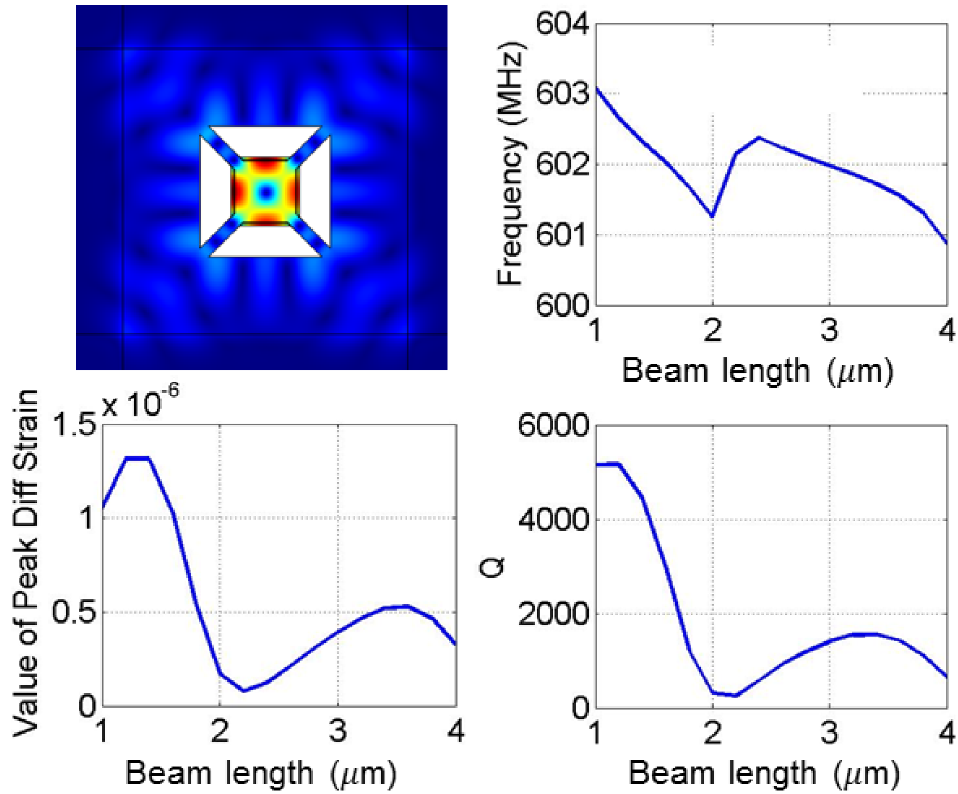


Figure 5-7: (top left) Mode shape of differentially driven and sensed resonator in wineglass mode (bottom left, top right and bottom right) Results from parametric sweep on suspension beam length showing highest differential strain and Q around $1.2\,\mu$m.

coupling beams were also similarly designed to maximize acoustic energy transfer between the two mechanically coupled islands at roughly 2× the substrate suspension beam lengths, while suppressing any spurious modes near the resonance frequency (resulting from mode shapes that extend into the coupling beam). The beam lengths were optimized for obtaining high Q at minimal dimensions to avoid adding inline electrical resistance to the devices. The widths of the beams were minimized and limited to photolithography resolution limits to avoid distortions to the mode shape.

The final parameters used in the design of the piezoelectric RBT are summarized in Table 5.3. Layout of devices was completed in Cadence and a snapshot of the die is included in Fig. 5-8. Fabrication of the piezoelectric RBT with AlN films is in development at MIT's Microsystems Technology Laboratories (MTL) as of the date

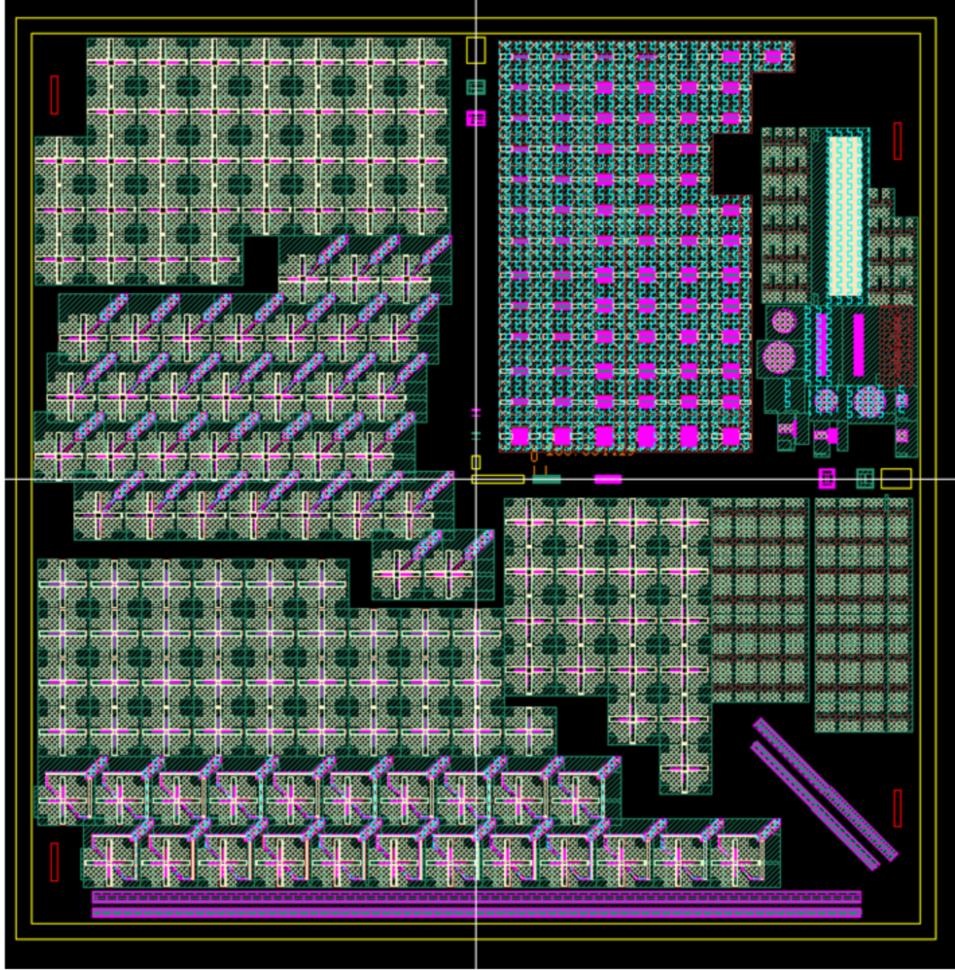


Figure 5-8: Final layout of piezoelectric RBT devices. Fabrication was carried out at MTL.

of writing this thesis.

Thus in summary, the analysis and performance optimization of such piezoelectric RBTs is discussed in this chapter. Simulations are carried out using AlN as the desired piezoelectric material which has been extensively studied for micromechanical resonators and which shows potential for CMOS integration. Sidewall sputtered AlN films are considered for integration into an RBT structure for improved transduction efficiency through the e_{33} coefficient. COMSOL simulations carried out with AlN as piezoelectric material and Mo as electrode material show high-Q modes with excellent spurious mode suppression through differential drive and sensing. Mechanically coupled devices were designed for ease of routing, reduced R_X reduced parasitic

Table 5.3: Material parameters used in final design of piezoelectric RBT.

Paramater	Value
resonance mode	square wineglass
Si square length	5μm
AlN sidewall thickness	100 nm
Mo sidewall thickness	200 nm
expected resonance frequency	600 MHz
substrate beam length	1.3μm
substrate beam width	1μm
# coupled resonators	2
coupling beam length	5.4μm
substrate doping	p-type
FET type	nFET
FET W/L	$\sim$1

feedthrough from input to output.

Chapter 6

Conclusion and Future Directions

This work presents implementations of active sensing in Si based resonators with two different transduction mechanisms: electrostatic and piezoelectric. Active sensing using a FET is a high-efficiency, low-noise transduction mechanism that is suitable for the resonator area limitations posed by high-frequency operation (section 1.1.3). FET-sensing is demonstrated in CMOS-integrated resonators for fully unreleased, monolithically integrated devices. FET-sensing is also explored as a technique for improved transduction efficiency and non-linear behavior in piezoelectric resonators.

ABR-confined CMOS-RBTs

First-generation CMOS-based unreleased RBTs are demonstrated in IBM's 32SOI process with resonance frequencies above 11 GHz, Qs of $24-30$ and footprint of less than $5\mu m \times 3\mu m$ (chapter 3). They are fabricated at the transistor level of the CMOS stack and are realized without the need for any post-processing or packaging. Acoustic Bragg reflectors used for acoustic isolation are designed in the front-end-of-line using shallow trench isolation structures. The resonators are driven capacitively and sensed piezoresistively using a FET.

Comparative behavior of devices with design variations is used to demonstrate the effects of ABRs on device performance (section 3.2). A shift in ABR design frequency from the resonance frequency shows reduced amplitude of the resonance mode and reduced suppression of spurious modes. Additionally, the frequency response of passively sensed electrostatic resonators shows no discernible peak, emphasizing the im-

portance of active sensing in CMOS. First-generation ABR-RBTs have demonstrated thermal stability or TCFs between 3 ppm/K (section 3.4). The complimentary nature of the TCEs of Si and SiO_2 in such CMOS-integrated RBTs shows potential for TCF manipulation for design of temperature sensors with high TCF or oscillators with sub-ppm/K sensitivity.

While the Q of these first-generation ABR-RBTs is comparable to on-chip LC tanks, it is still a couple of orders of magnitude lower than what may be realized with MEMS resonators. The presence of CMP-fill generated, randomly occurring, high-impedance metal layers above the resonant cavity resulted in spurious modes close to the resonance frequency. Additionally, several foundry DRC rules were violated in the design of these resonators, which resulted in compromised transistor performance. Finally, the non-uniformity in the resonance cavity arising from the fabrication of the driving MOSCAP and sensing FET on the same device layer "island" resulted in a small resultant stress at the sensing channel.

PnC-confined CMOS-RBTs

To address these problems, the second-generation CMOS-resonators were realized by designing acoustic isolation structures in the BEOL in the form of a PnC for enhanced confinement of mechanical vibrations. The first implementation of a PnC in standard CMOS is demonstrated using lithographically defined BEOL materials such as Cu surrounded by a low-k inter-metal dielectric for engineering of wide PnC bandgaps (chapter 4). These second-generation monolithically integrated CMOS-MEMS resonators are realized without any post-processing or packaging, with a footprint of $5\mu m \times 7\mu m$ and demonstrate Q of 252 at 2.8 GHz which is an $8\times$ improvement in Q over the previous generation and greatly extended spurious free range. The inclusion of long vias ensures uniformity of the resonant cavity design and shows improved Q and enhanced suppression of spurious modes. These second-generation CMOS-integrated resonators violated minimal DRC rules while achieving superior acoustic confinement using the BEOL PnC design, thus minimizing risk of performance and yield compromises arising from CMOS-MEMS co-design. Such a concept may be easily extended to any IC or III-V technology with multi-level metal stacks.

The design and implementation of PnC-RBTs in CMOS may also be used to characterize the unknown mechanical properties of the CMOS stack and may thus be developed as an analytical tool. The BEOL stack available in a particular technology is an important consideration for PnC design. Device performance can be enhanced further by using such extracted material properties of the CMOS stack and performing 3D geometric optimization based on those properties. With respect to implementation, the PnC-confined RBT still shows need for improvement in Q, input-to-output transconductance and reduction in direct feedthrough for integration with transceiver circuitry.

Differential design may be employed to reduce the direct input to output feedthrough signal. To improve Q and output signal, lateral confinement of the resonance mode may be improved by designing ABRs in the FEOL using bulk ties or vias with slowly increasing spacing between the metal interrupting the pre-metal dielectric. PnC performance may also be improved by using additional metal layers to form the PnC, exploring different unit cell configurations while satisfying DRC constraints and designing a gradual boundary between the PnC and surrounding dielectric regions to reduce reflections.

Towards piezoelectrically transduced RBTs

While electrostatically transduced RBTs were considered for CMOS-integration due to the availability of high quality dielectrics in a standard CMOS stack, piezoelectric transduction in MEMS resonators has demonstrated significantly better motional impedance and increased signal output. Recent years have seen a push towards integrating materials with piezoelectric properties into the CMOS stack for applications ranging from switching to memory and this leads to the consideration of piezoelectric-based RBTs for low insertion loss devices.

AlN was chosen as the piezoelectric material of choice due to its potential for CMOS-integration, in spite of its relatively modest piezoelectric coefficients with respect to materials such as PZT. Deposition of AlN on sidewalls of Si with good piezoelectric properties has been demonstrated in recent years and is utilized for the $\sim 3\times$ higher e_{33} piezoelectric coefficient as compared to lateral e_{31} coefficient for increased

transduction efficiency. On the sensing side, the additional sensing mechanism in the form of piezoelectrically induced gate voltage that modulates the transistor drain current further improves transduction efficiency and reduces the effective motional impedance, R_X. Piezoelectric devices are designed in mechanically coupled configurations with differential drive and sense for improved spurious mode suppression and reduced R_X (chapter 5). Ultimately, such devices can be monolithically integrated into the CMOS stack containing piezoelectric materials and may be acoustically isolated using structures such as ABRs and PnCs demonstrated in this thesis.

Seamless integration into a standard CMOS process obviates the need for complex and costly custom processes for MEMS fabrication. CMOS-integrated RBTs are the first step towards realizing on-chip acoustic frequency sources with reduced size, weight and power consumption. Temperature coefficients of frequency of these devices may be designed to be large for temperature sensors or small, for temperature-insensitive filters and oscillators by varying the relative proportions of Si and SiO_2 with complimentary TCEs in the resonator based on their relative contributions to the mode shape. The introduction of piezoelectric materials into the CMOS stack shows potential for further improvements in transduction efficiency and reduced constraints for filter and oscillator applications. Furthermore, such a demonstration of resonators fabricated side-by-side with CMOS circuitry greatly reduces parasitics of off-chip access, constraints of limited IO, and power consumption associated with impedance matching networks. Such benefits can provide increased system speed and dynamic range in wireless communication, navigation and sensing systems, particularly at RF and mm-wave frequencies of operation.

Appendix A

What determines the Q of a resonator?

One of the most important metrics of a micromechanical resonator is its quality factor (Q), defined as:

$$Q = 2\pi \frac{\text{Peak energy stored}}{\text{Energy lost per cycle}} \tag{A.1}$$

which is also directly related to the peak sharpness as $Q = f_0/\Delta f$, where f_0 is the peak frequency and Δf is the 3 dB bandwidth. A resonator with a high Q is desirable for several reasons:

- For filter applications, a high-Q resonator shows improved roll-off and insertion loss, thus allowing for narrower channel definition in given communication band, more secure and noise-free communications [101].

- High-Q resonators allow the design of MEMS-based oscillators with greater spectral purity, low jitter and low phase noise [102].

- Resonant MEMS sensors show enhanced sensitivity and higher resolution due to high Q [103] while resonant gyroscopes show higher sensitivity, reduced mechanical noise and bias stability [104].

Several intrinsic and extrinsic mechanisms limit the Q of a MEMS resonator. The overall Q of a device is related to the Q from these loss mechanisms as:

$$\frac{1}{Q_{total}} = \frac{1}{Q_{intrinsic}} + \frac{1}{Q_{extrinsic}} \tag{A.2}$$

Thus, reduced damping through intrinsic and extrinsic mechanisms leads to increased overall Q. Some types of intrinsic damping mechanisms include [105]:

1. Phonon-phonon interactions in which the acoustic wave traveling through the resonator interacts with the lattice vibrations (or thermal phonons) and loses energy as a result. This is minimized at low temperatures. At low frequencies, the acoustic wavelength is much larger than the mean free path of phonons, and is modeled to interact with an entire ensemble of phonons at once, allowing efficient energy dissipation (Akhieser regime). Physically, this may be also considered as a regime in which there is plenty of time for lattice phonons to dissipate energy due to low frequency of operation, which reduces the Q with frequency. On the other hand, at high frequencies, the time scale of these interactions is smaller than the mean time taken to dissipate mechanical energy, keeping the Q constant with frequency (Landau-Rumer regime). This is a dominant loss mechanism in insulators and semiconductors.

2. Phonon-electron interactions is a dominant loss mechanism in doped semiconductors, piezoelectric materials and metals in which acoustic waves couple with mobile charges. Typically, the standing waves in a resonator cause deformation potentials, resulting in a flow of charges leading to ohmic losses. This phenomenon increases with temperature as a result of thermal excitation of charges.

3. Thermoelastic damping (TED) which occurs due to regions of compressive and tensile strain in the mode of vibration. The resulting thermal gradients lead to irreversible heat loss from hot regions to cold regions.

4. Other intrinsic mechanisms include TED generated between grain boundaries

and mechanisms due to impurities, defects, dislocations and vacancies etc.

On the other hand, extrinsic damping mechanisms include [105]:

1. Anchor loss due to radiation of energy into the surrounding substrate. This may be avoided by designing anchors at regions of minimum strain or by design of reflective structures such as PnCs and ABRs.

2. Fluid damping occurs when the boundaries of the resonator exert a net force on the particles of the viscous medium such as air, that they come in contact with. The work done in displacing the fluid particles results in irreversible thermodynamic losses and may be avoided by operating in vacuum.

3. Surface and interface losses occur due to scattering off surface roughness such as the scallops produced by DRIE. Composite film stacks such as dielectric or piezoelectric films on Si also leads to losses at the imperfect interface.

4. Electrical losses occur as resistive losses through a lossy dielectric film, determined by the dielectric loss tangent and from electrical loading due to a mismatch between resonator impedance and interfacing circuitry.

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Appendix B

Constituent Equations of Piezoelectricity

Piezoelectricity was first discovered in quartz by the Jacques and Pierre Curie in 1880 as the phenomenon through which bound electric charge appears at the surface of a medium in response to acoustic strain [106]. Physically, this may be explained in terms of a simple atomic model. In materials demonstrating piezoelectricity, atoms of a solid get displaced under strain resulting in microscopic electric dipoles which combine to give a net electric polarization. The *direct piezoelectric effect*, appearance of bound charges in presence of strain, is always accompanied by a *converse piezoelectric effect*, which manifests as a strain in the solid on the application of an electric field. Piezoelectricity is a linear effect that only appears in certain materials and is distinct from the electrostrictive stress that appears in all materials as a quadratic function of electric field. The latter is a second-order phenomenon that may be ignored in small-signal modeling.

Both the direct and the converse piezoelectric effects may be included in the constituent equations of acoustics to obtain the constituent equations of piezoelectricity:

$$D = \epsilon^T . E + d . T \tag{B.1}$$

$$S = \underline{d} . E + s^E . T \tag{B.2}$$

where D is the electric displacement tensor, ϵ^T denotes the dielectric constant at constant stress, T. d and $\underline{d}$ are the direct and inverse piezoelectric strain constants respectively while s^E denotes the compliance matrix under conditions of constant electric field, E, to calculate the strain vector, S.

The above equations may also be defined in terms of piezoelectric stress constants given by e and $-\underline{e}$ as:

$$D = \epsilon^S.E + e.S \tag{B.3}$$

$$T = -\underline{e}.E + c^E.S \tag{B.4}$$

A material such as AlN has a hexagonal crystal structure and the piezoelectric matrix reduces to the following through symmetry, giving piezoelectric stress constants [107]:

$$e = \begin{bmatrix} 0 & 0 & 0 & 0 & -0.48 & 0 \\ 0 & 0 & 0 & -0.48 & 0 & 0 \\ -0.58 & -0.58 & 1.55 & 0 & 0 & 0 \end{bmatrix} C/m^2 \tag{B.5}$$

The d matrix which relates the induced strain to applied electric field may be obtained from the e matrix by multiplying the with the compliance matrix $d_{ij} = s_{ik}e_{kj}$

$$d = \begin{bmatrix} 0 & 0 & 0 & 0 & -4 & 0 \\ 0 & 0 & 0 & -4 & 0 & 0 \\ -1.98 & -1.98 & 4 & 0 & 0 & 0 \end{bmatrix} 10^{-12}C/N \tag{B.6}$$

It may be noted that the units C/N are dimensionally equal to m/V.

It may be observed from this matrix that in AlN, the e_{33} piezoelectric coefficient of $1.55\,\mathrm{C/m^2}$ is nearly $3\times$ that of the e_{31} coefficient of $-0.58\,\mathrm{C/m^2}$, making sidewall transduction more efficient than lateral transduction (in which the piezoelectric film is patterned on the top surface of the resonator and a voltage is applied across it, in the thickness direction to produce vibrations in the longitudinal direction).

B.1 Effective coupling coefficient

An important figure of merit for piezoelectric resonators is the effective coupling factor or k_{eff}^2 which describes the transduction efficiency of a device. Simply defined, this may be expressed as:

$$k_{eff}^2 = \frac{\text{Output mechanical energy}}{\text{Input electrical energy}} \tag{B.7}$$

In general, two different types of coupling factors may be considered when talking about a piezoelectric material:

- The quasi-static or material coupling factors are dependent only upon material properties and describe the transduction efficiency in a spatially uniform electric field due to the material's piezoelectric coefficients. For instance, strain in the "1" direction leading to an electric field in the "3" direction is described by k_{31}^2. The commonly used quasi-static coupling coefficient k_t^2 is applicable for FBARs vibrating in thickness mode.

- The effective coupling coefficient or k_{eff}^2 characterizes the performance of a device rather than the properties of its constituent piezoelectric films. It takes into account the non-idealities in design such as complex mode shapes, non-uniform electric fields etc. and for a passive piezoelectric resonator, may be expressed in terms of the parallel and series resonance frequencies, given by f_p and f_s respectively, as:

  $$k_{eff}^2 = \frac{f_p^2 - f_s^2}{f_p^2} \tag{B.8}$$

  The figure of merit that is used to characterize piezoelectric devices is expressed with respect to this k_{eff}^2 as:

  $$\text{Figure of Merit} = \frac{k_{eff}^2 Q}{1 - k_{eff}^2} \tag{B.9}$$

More details on these definitions may be found in the IEEE standards on piezoelectricity [108].

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Appendix C

Butterworth-Van Dyke model

One or two port passive resonators may be modeled using an equivalent RLC circuit where the L-C of the resonant branch determine the resonant frequency. The input and output capacitances and inline resistances may be included as additional circuit elements, and the direct input to output feedthrough is modeled using a feedthrough capacitance in parallel with the RLC branch. This is known as the Butterworth-Van Dyke (BVD) model [109] (Fig. C-1). We will first discuss the lumped element modeling of a mechanical resonator followed by the conversion into its equivalent BVD model.

A mechanical resonator may be represented by a lumped spring-mass-damper system which represents its internal physics as terminal relations. This means that instead of concerning ourselves with the displacement and velocity of each particle at every point of time, we think of the resonator as a discrete object with an effective mass m, connected to a spring with stiffness k and a dashpot with coefficient b which models the mechanical loss (Fig. C-2). We assume that signals do not take time to propagate within the resonator as the size of the resonator is smaller than the signal wavelength to change this continuous system described by partial differential equations into a system described by ordinary differential equations. Such an approach allows considerable simplification of a the physics of a complicated structure for static and dynamic analyses through conversion into equivalent system. One of the cons of such an approach is the loss of spatial information.

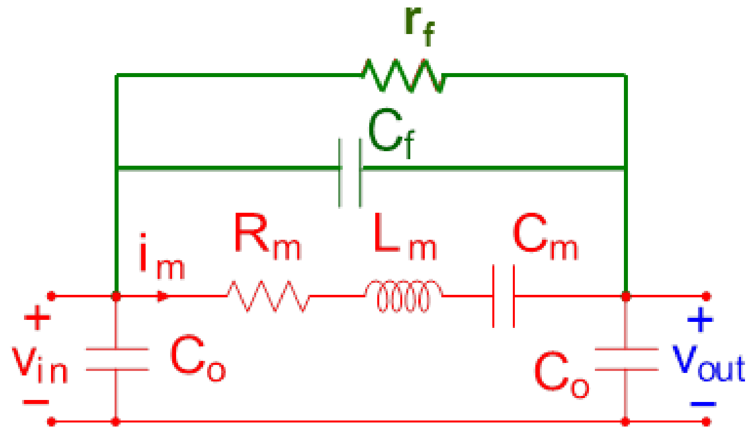

Figure C-1: The Butterworth Van-Dyke model is used for modeling passive resonators using their equivalent RLC circuit with shunt and feedthrough parasitics.

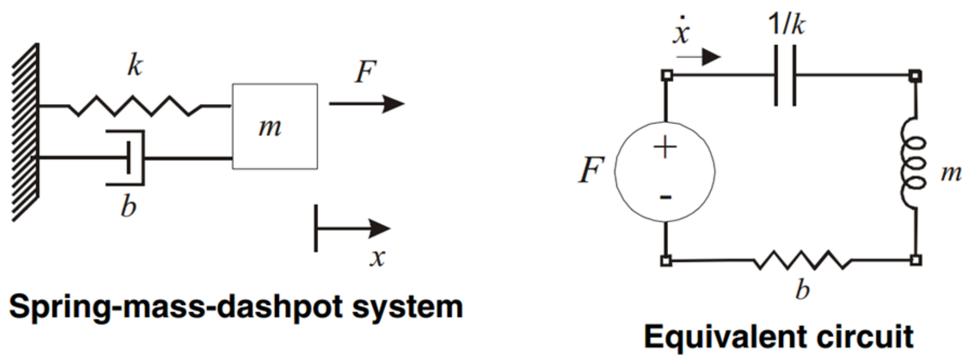

Figure C-2: Lumped model of a Spring-mass-dashpot system representing a mechanical resonator, and its equivalent electrical circuit. Source: MIT 6.777 lecture notes

The calculation of the equivalent mechanical parameters for a system is geometry, mode shape and force dependent. One example is provided in [49] where the equivalent m, k and b for an internal dielectric device is calculated. For a lumped model with a mass, spring damper, the ODE relating the driving force F to the system is given by:

$$F = m\ddot{x} + b\dot{x} + kx \tag{C.1}$$

$$F = m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx \tag{C.2}$$

Assuming a forcing function of the form $F = F(s)e^{st}$ and displacement function of the form $x = X(s)e^{st}$, we get

$$F(s) = X(s)(ms^2 + bs + k) \tag{C.3}$$

which gives the transfer function relating the input force and the output displacement as

$$\frac{X(s)}{F(s)} = \frac{1}{ms^2 + bs + k} \tag{C.4}$$

or in terms of the velocity as

$$\frac{\dot{X}(s)}{F(s)} = \frac{1}{ms + b + k/s} \tag{C.5}$$

The mechanical resonance frequency of this system is given by:

$$\omega_0 = \sqrt{\frac{k}{m}} \tag{C.6}$$

And representing the transfer function denominator in the conventional form:

$$s^2 + \frac{b}{m}s + \frac{k}{m} = s^2 + 2\alpha s + \omega_0^2 \tag{C.7}$$

we get the damping constant α and the quality factor Q as:

$$\alpha = \frac{b}{2m} \tag{C.8}$$

$$Q = \frac{\omega_0}{2\alpha} = \frac{m\omega_0}{b} \tag{C.9}$$

To convert this mechanical equation into its electrical equivalent circuit, we use voltage as the variable analogous to the force and velocity or $\dot{x}$ as analogous to the current. Comparing the mass-spring-damper system to the RLC branch of the BVD model, we have the electrical domain equations as:

$$V = L\frac{dI}{dt} + RI + \frac{1}{C}\int Qdt \tag{C.10}$$

where V is the voltage and I is the current. This may again be represented in the Laplace domain as:

$$\frac{I}{V} = \frac{1}{Ls + R + \frac{1}{Cs}} \tag{C.11}$$

Thus the equivalent circuit values for the mechanical system is given by:

$$L = m, R = b, C = 1/k \tag{C.12}$$

while the ω_0 and Q are given by:

$$\omega_0 = \sqrt{\frac{k}{m}} \tag{C.13}$$

$$Q = \frac{L\omega_0}{R} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{C.14}$$

However, we are still missing one part of the model. The calculated RLC values may not be used as such in the BVD model as our mechanical system assumed a mechanical forcing function while the electrical system has a driving voltage. We have so far ignored the the inefficient transduction mechanism that converts the electric driving voltage into the equivalent mechanical force, and vice-a-versa, the inefficient mechanism that will convert the velocity into a sensed current. If we assume the transduction efficiency of these mechanisms is $\eta < 1$ such that $F = \eta V$ and $I = \eta\dot{X}$

we get the equivalent parameters of the BVD model:

$$L_m = \frac{m}{\eta^2}, R_m = \frac{b}{\eta^2}, C_m = \frac{\eta^2}{k} \tag{C.15}$$

For instance, in the case of capacitive drive,

$$F = \frac{1}{2}\frac{\partial C_{drive}}{\partial x}(V_{DC} + v_{ac}e^{j\omega t})^2 \tag{C.16}$$

On ignoring the DC and 2ω components, this gives us the force at the resonance frequency and the transduction efficiency respectively as:

$$F = \frac{\partial C_{drive}}{\partial x} V_{DC} v_{ac} \tag{C.17}$$

$$\eta = \frac{\partial C_{drive}}{\partial x} V_{DC} \tag{C.18}$$

Thus, the R_m, L_m and C_m of the BVD model may be calculated using the transduction efficiency η and the mechanical equivalent model of the resonant system. Finally, the drive and sense capacitors are as designed electrically and the fringing feedthrough capacitance may be modeled using finite element methods.

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Appendix D

Piezoresistance in Si

Piezoresistance is the phenomenon through which certain conducting and semiconductor materials exhibit a change in resistance as a response to lattice strain. This effect is prominent in materials such as Si and Ge where the resistance change is typically several orders the contribution seen due to geometry changes [110].

The piezoresistive effect was first demonstrated by in 1856 by Lord Kelvin as the change in resistance of iron and copper wires when subject to elongation [111]. The piezoresistive effect in Si was first reported by C.S. Smith [112].

Theories of piezoresistivity are based on bandgap energy models, wave mechanics and quantum effects [113]. In unstrained n-type Si, the lowest conduction band energies are aligned along the $< 1 - 0 - 0 >$ direction which correspond to six equal low-energy states or "valleys" occupied by electrons. The mobility is minimum in the direction of the valley but maximum in the directions perpendicular to it. Thus an electron in an x valley will have maximum mobility along the y and z valleys. The total electron conductivity is the sum of the conductivity components along the three valley orientations independent of direction. Net mobility is the average mobility along the three valleys (two high and one low). Strain in the crystal (say along the x direction) increases the band energy of the valley parallel to the strain (x) direction and transfers electrons to perpendicular valleys (y and z), which also have high mobility along the direction of strain. Electrons preferentially move in directions of higher mobility (higher conductivity and lower resistance) which is the

direction of strain and average mobility is thus increased parallel to the direction of strain (longitudinal effect) and reduced perpendicular to that direction (transverse effect).

Silicon piezoresistance has been widely used for various sensors including pressure sensors [114], inertial sensors [115], cantilever force sensors [116], and strain gauges [117]. Recent years have seen a strong interest in piezoresistive theory for semiconductors, such as Si and Ge, for strain engineering in transistors as devices scale to smaller dimensions [118]. In single-crystal structures of Si and Ge, both of which have diamond lattice crystal structure, the fractional change in resistivity for a fixed voltage depends on the stress components σ_λ in the 6-component stress vector notation and the current orientation ω, and is given by [119]:

$$\frac{\Delta\rho_\omega}{\rho} = \sum_{\lambda=1}^{6} \pi_{\omega\lambda}\sigma_\lambda \tag{D.1}$$

where $\pi_{\omega\lambda}$ is a component of the piezoresistive coefficient tensor, which in crystals with cubic symmetry such as Si, is given by:

$$[\pi_{\omega\lambda}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{D.2}$$

There are primarily two types of piezoresistive coefficients that need to be considered.

1. The longitudinal coefficient when the current flow is in the same direction as the applied mechanical strain/stress represented by π_{11}, π_{22} and π_{33} which are equal in Si.

2. The shear coefficient when current flow is in a direction perpendicular to the

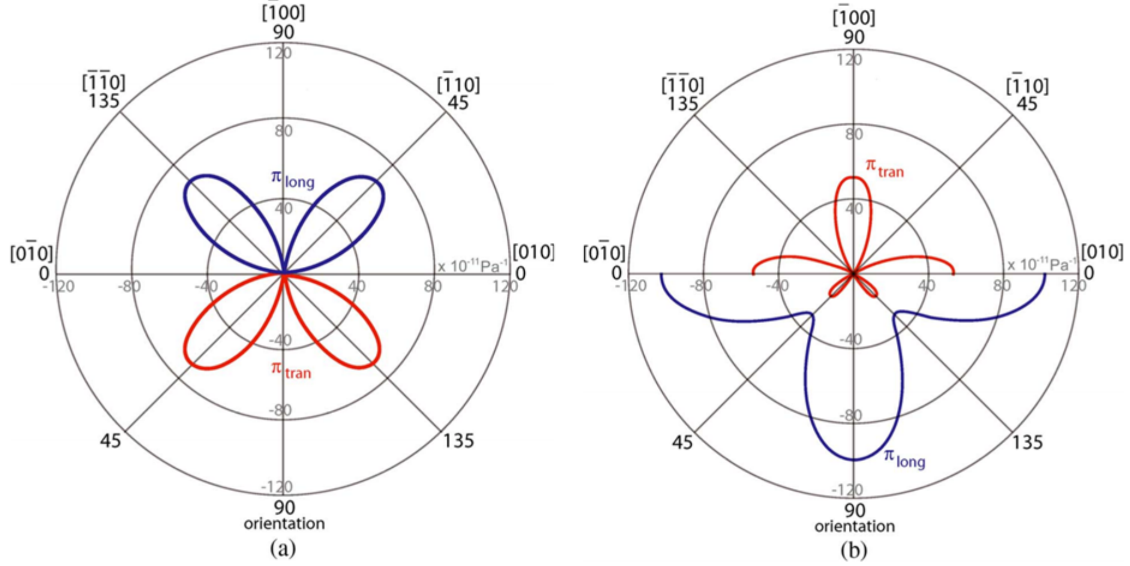

Figure D-1: Room temperature piezoresistive coefficients in the (100) plane of (a) p-type Si (b) n-type Si for low-moderate doping concentrations ($< 10^{18}/cc$).
Source: [119]

applied mechanical strain/stress represented by π_{12}.

Both longitudinal and shear coefficients in Si have been graphically represented in [119] along several directions of the (100), (110) and (211) plane (Fig. D-1). Based on this figure, piezoresistance coefficients in Si with the Cartesian coordinate system aligned with the $< 100 >$ axes at room temperature are given in Table D.1

In a typical scenario where (001) Si wafer is used with the two directions parallel and perpendicular to the flat being $< 110 >$, the new piezoresistance coefficients system may be obtained by rotation about the z axis through an angle $\pi/4$. For such

Table D.1: Piezoresistive coefficients of Si at room temperature [4]

Si material	ρ ($\Omega\,$cm)	π_{11} ($10^{-11}\,$Pa^{-1})	π_{12} ($10^{-11}\,$Pa^{-1})	π_{44} ($10^{-11}\,$Pa^{-1})	π_A ($10^{-11}\,$Pa^{-1})
SCS n-type	11.7	-102.2	53.4	-13.6	-142
SCS p-type	7.8	6.6	-1.1	138.1	-130.4

a wafer, the piezoresistance coefficient matrix may be derived as [4]:

$$[\pi'_{\omega\lambda}] = \begin{bmatrix} \pi_{11} - \pi_A/2 & \pi_{12} + \pi_A/2 & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} + \pi_A/2 & \pi_{11} - \pi_A/2 & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} + \pi_A \end{bmatrix} \tag{D.3}$$

where $\pi_A = \pi_{11} - \pi_{12} - \pi_{44}$. Based on Table D.1, for p-type Si this numerically corresponds to:

$$[\pi'_{Si-(110)}] = \begin{bmatrix} -58.6 & 66.3 & -1.1 & 0 & 0 & 0 \\ 66.3 & -58.6 & -1.1 & 0 & 0 & 0 \\ -1.1 & -1.1 & 6.6 & 0 & 0 & 0 \\ 0 & 0 & 0 & 138.1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 138.1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 72.9 \end{bmatrix} \times 10^{-11}\mathrm{Pa}^{-1} \tag{D.4}$$

For transistor calculations, we typically require the relationship between the piezoresistive coefficients and the change in channel mobility μ which is related to the change in resistivity ρ as:

$$\rho = \frac{1}{nq\mu} \tag{D.5}$$

$$\frac{d\rho}{d\mu} = \frac{-1}{nq\mu^2} \tag{D.6}$$

$$\frac{d\rho}{\rho} = -\frac{d\mu}{\mu} \tag{D.7}$$

Bibliography

[1] J. S. Orcutt, *Monolithic Electronic-Photonic Integration in State-of-the-Art CMOS Processes*. PhD thesis, Massachusetts Institute of Technology, February 2012.

[2] J. Reinke, G. Fedder, and T. Mukherjee, "CMOS-MEMS Variable Capacitors Using Electrothermal Actuation," *Microelectromechanical Systems, Journal of*, vol. 19, no. 5, pp. 1105–1115, 2010.

[3] V. Kaajakari, *Practical MEMS*. Small Gear Publishing, 2009.

[4] H.-J. Timme, *CMOS-based Pressure Sensors*, pp. 257–334. Wiley-VCH Verlag GmbH, 2008.

[5] W.-L. Huang, Z. Ren, and C.-C. Nguyen, "Nickel Vibrating Micromechanical Disk Resonator with Solid Dielectric Capacitive-Transducer Gap," in *International Frequency Control Symposium and Exposition, 2006 IEEE*, pp. 839–847, 2006.

[6] G. Ho, R. Abdolvand, A. Sivapurapu, S. Humad, and F. Ayazi, "Piezoelectric-on-silicon lateral bulk acoustic wave micromechanical resonators," *Microelectromechanical Systems, Journal of*, vol. 17, pp. 512–520, April 2008.

[7] A. Rahafrooz and S. Pourkamali, "High-Frequency Thermally Actuated Electromechanical Resonators With Piezoresistive Readout," *Electron Devices, IEEE Transactions on*, vol. 58, no. 4, pp. 1205–1214, 2011.

[8] K. Petersen, "Silicon as a mechanical material," in *Symposium C Science and Technology of Microfabrication*, vol. 76 of *MRS Proceedings*, 1986.

[9] R. Tabrizian, M. Rais-Zadeh, and F. Ayazi, "Effect of phonon interactions on limiting the f.Q product of micromechanical resonators," in *International Solid-State Sensors, Actuators and Microsystems Conference, 2009. (TRANSDUCERS)*, pp. 2131–2134, June 2009.

[10] S. Y. No and F. Ayazi, "The HARPSS process for fabrication of nano-precision silicon electromechanical resonators," in *Nanotechnology, 2001. IEEE-NANO 2001. Proceedings of the 2001 1st IEEE Conference on*, pp. 489–494, 2001.

[11] W.-C. Chen, C.-S. Chen, K.-A. Wen, L.-S. Fan, W. Fang, and S.-S. Li, "A generalized foundry CMOS platform for capacitively-transduced resonators monolithically integrated with amplifiers," in *Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on*, pp. 204–207, 2010.

[12] M. Aissi, E. Tournier, M.-A. Dubois, G. Parat, and R. Plana, "A 5.4GHz 0.35μm BiCMOS FBAR Resonator Oscillator in Above-IC Technology," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pp. 1228–1235, 2006.

[13] A. Rahafrooz and S. Pourkamali, "Active self-Q-enhancement in high frequency thermally actuated M/NEMS resonators," in *Micro Electro Mechanical Systems (MEMS), 2011 IEEE 24th International Conference on*, pp. 760–763, Jan 2011.

[14] J. T. M. Van Beek, G. Verheijden, G. E. J. Koops, K. Phan, C. van der Avoort, J. Van Wingerden, D. Badaroglu, and J. J. M. Bontemps, "Scalable 1.1 GHz fundamental mode piezo-resistive silicon MEMS resonator," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pp. 411–414, 2007.

[15] R. Marathe, B. Bahr, W. Wang, Z. Mahmood, L. Daniel, and D. Weinstein, "Resonant Body Transistors in IBM's 32 nm SOI CMOS Technology," *J. Microelectromech. Syst.*, no. 99, pp. 1–1, 2013.

[16] H. Nathanson, W. Newell, R. Wickstrom, and J. Davis, J.R., "The Resonant Gate Transistor," *Electron Devices, IEEE Transactions on*, vol. 14, no. 3, pp. 117–133, 1967.

[17] S. Bartsch, D. Grogg, A. Lovera, D. Tsamados, and A.-M. Ionescu, "Very high frequency double-ended tuning fork nano-mechanical Fin-FET resonator," in *International Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011*, pp. 938–941, 2011.

[18] S. Bartsch, C. Dupre, E. Ollier, and A. Ionescu, "Resonant-body silicon nanowire field effect transistor without junctions," in *Device Research Conference (DRC), 2012 70th Annual*, pp. 1–2, June 2012.

[19] D. Weinstein and S. A. Bhave, "The Resonant Body Transistor," *Nano Letters*, vol. 10, no. 4, pp. 1234–1237, 2010. PMID: 20180594.

[20] D. Weinstein and S. A. Bhave, "Acoustic resonance in an independent-gate FinFET," *Hilton Head*, pp. 459–462, 2010.

[21] M. Faucher, A. Ben Amar, B. Grimbert, V. Brandli, M. Werquin, L. Buchaillot, C. Gaquiere, D. Theron, Y. Cordier, and F. Semond, "GaN: A multifunctional material enabling MEMS resonators based on amplified piezoelectric detection," in *Frequency Control and the European Frequency and Time Forum (FCS), 2011 Joint Conference of the IEEE International*, pp. 1–5, 2011.

[22] L. Popa and D. Weinstein, "Switchable piezoelectric transduction in AlGaN/GaN MEMS resonators," in *Solid-State Sensors, Actuators and Microsystems, 2013 Transducers Eurosensors XXVII: The 17th International Conference on*, pp. 2461–2464, June 2013.

[23] A. Arun, M. Goffman, D. Grogg, A. Filoramo, S. Campidelli, V. Derycke, T. Idda, P. Salet, and A. Ionescu, "Tunable electromechanical resonator based on carbon nanotube array suspended gate field effect transistor (CNT-SGFET)," in *Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on*, pp. 112–115, Jan 2010.

[24] V. Leiman, M. Ryzhii, A. Satou, N. Ryabova, V. Ryzhii, T. Otsuji, and M. Shur, "Analysis of resonant detection of terahertz radiation in high-electron mobility transistor with a nanostring/carbon nanotube as the mechanically floating gate," *Journal of Applied Physics*, vol. 104, pp. 024514–024514–7, Jul 2008.

[25] K. Phan, J. van Beek, and G. Koops, "Piezoresistive ring-shaped MEMS resonator," in *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*, pp. 1413–1416, June 2009.

[26] A. Iqbal, J. Chapin, E. Mehdizadeh, A. Rahafrooz, B. Purse, and S. Pourkamali, "Real-time bio-sensing using micro-channel encapsulated thermal-piezoresistive rotational mode disk resonators," in *Sensors, 2012 IEEE*, pp. 1–4, Oct 2012.

[27] X. Wei and A. Seshia, "Differential piezoresistive sensing in a bulk-mode micromechanical resonator," *Micro Nano Letters, IET*, vol. 8, pp. 107–110, February 2013.

[28] S.-W. Lee, S. Truax, L. Yu, C. Roman, and C. Hierold, "Carbon nanotube resonators with capacitive and piezoresistive current modulation readout," *Applied Physics Letters*, vol. 103, pp. 033117–033117–5, Jul 2013.

[29] C. Li, M. Li, C. Chen, C. Chin, and S. Li, "A low-voltage CMOS-microelectromechanical systems thermal-piezoresistive resonator with Q ¿ 10,000," *Electron Device Letters, IEEE*, vol. 36, pp. 192–194, Feb 2015.

[30] X. Guo, Y. bo Yi, and S. Pourkamali, "Thermal-piezoresistive resonators and self-sustained oscillators for gas recognition and pressure sensing," *Sensors Journal, IEEE*, vol. 13, pp. 2863–2872, Aug 2013.

[31] G. Fedder, R. Howe, T.-J. K. Liu, and E. Quevy, "Technologies for Cofabricating MEMS and electronics," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 306–322, 2008.

[32] H. Xie, L. Erdmann, X. Zhu, K. Gabriel, and G. Fedder, "Post-CMOS processing for high-aspect-ratio integrated silicon microstructures," *Microelectromechanical Systems, Journal of*, vol. 11, no. 2, pp. 93–101, 2002.

[33] G. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, pp. 82–85, Jan 1998.

[34] J. Plummer, M. Deal, and P. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling*. Prentice Hall Electronics and Vlsi Series, Prentice Hall PTR, 2000.

[35] W. Frobenius, A. Sanderson, and H. Nathanson, "A microminiature solid-state capacitive blood pressure transducer with improved sensitivity," *Biomedical Engineering, IEEE Transactions on*, vol. BME-20, pp. 312–314, July 1973.

[36] K. Najafi, K. Wise, and T. Mochizuki, "A high-yield IC-compatible multichannel recording array," *Electron Devices, IEEE Transactions on*, vol. 32, pp. 1206–1211, Jul 1985.

[37] C. Sander, J. W. Knutti, and J. Meindl, "A monolithic capacitive pressure sensor with pulse-period output," *Electron Devices, IEEE Transactions on*, vol. 27, pp. 927–930, May 1980.

[38] R. Candler, W.-T. Park, H. Li, G. Yama, A. Partridge, M. Lutz, and T. Kenny, "Single wafer encapsulation of MEMS devices," *Advanced Packaging, IEEE Transactions on*, vol. 26, pp. 227–232, Aug 2003.

[39] T. Mukherjee and G. K. Fedder, *RF CMOS MEMS*, pp. 225–256. Wiley-VCH Verlag GmbH, 2008.

[40] E. Brown, "RF-MEMS switches for reconfigurable integrated circuits," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 1868–1880, Nov 1998.

[41] O. Brand, *CMOS-MEMS*. Weinheim Great Britain: Wiley-VCH, 2005.

[42] A. De Silva and H. Hughes, "The package integration of RF-MEMS switch and control IC for wireless applications," *Advanced Packaging, IEEE Transactions on*, vol. 26, pp. 255–260, Aug 2003.

[43] P. Blondy, D. Cros, P. Guillon, P. Rey, P. Charvet, B. Diem, C. Zanchi, and J. B. Quoirin, "Low voltage high isolation MEMS switches," in *Silicon Monolithic Integrated Circuits in RF Systems, 2001. Digest of Papers. 2001 Topical Meeting on*, pp. 47–49, Sept 2001.

[44] A. Oz and G. Fedder, "RF CMOS-MEMS capacitor having large tuning range," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003*, vol. 1, pp. 851–854 vol.1, June 2003.

[45] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. Carley, and G. Fedder, "Micromachined high-Q inductors in a 0.18 μm copper interconnect low-k dielectric CMOS process," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 394–403, Mar 2002.

[46] P. Blondy, A. Brown, D. Cros, and G. Rebeiz, "Low-loss micromachined filters for millimeter-wave communication systems," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 2283–2288, Dec 1998.

[47] C.-C. Nguyen and R. Howe, "An integrated CMOS micromechanical resonator high-Q oscillator," *Solid-State Circuits, IEEE Journal of*, vol. 34, pp. 440–455, Apr 1999.

[48] B. Otis and J. Rabaey, "A 300-μW 1.9-GHz CMOS oscillator utilizing micromachined resonators," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1271–1274, July 2003.

[49] R. Marathe, "Analysis and Modeling of Piezoelectric Resonant Body Transistors," Master's thesis, Massachusetts Institute of Technology, May 2011.

[50] Z. Jiang, M. Kuroda, Y. Tan, D. Newns, M. Povolotskyi, T. Boykin, T. C. Kubis, G. Klimeck, and G. Martyna, "Electron transport in nano-scaled piezoelectronic devices," *Applied Physics Letters*, vol. 102, 2013.

[51] D. Newns, B. Elmegreen, X.-H. Liu, and G. Martyna, "The piezoelectronic transistor: A nanoactuator-based post-CMOS digital switch with high speed and low power," *MRS Bulletin*, vol. 37, pp. 1071–1076, 11 2012.

[52] J. Crawford, "Piezoelectric response of a ferroelectric memory array," *Sonics and Ultrasonics, IEEE Transactions on*, vol. 19, pp. 139–146, April 1972.

[53] J. Rodriguez, K. Remack, J. Gertas, K. Boku, K. Udayakumar, S. Summerfelt, G. Shinn, S. Madan, H. McAdams, T. Moise, J. Eliason, R. Bailey, M. Depner, D. Kim, and P. Staubs, "Reliability demonstration of a ferroelectric random access memory embedded within a 130nm CMOS process," in *Non-Volatile Memory Technology Symposium, 2007. NVMTS '07*, pp. 64–66, Nov 2007.

[54] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive UHF RF Identification CMOS Tag IC Using Ferroelectric RAM in 0.35um technology," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 101–110, Jan 2007.

[55] A. Islam Khan, D. Bhowmik, P. Yu, S. Joo Kim, X. Pan, R. Ramesh, and S. Salahuddin, "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures," *Applied Physics Letters*, vol. 99, no. 11, pp. –, 2011.

[56] R. Tabrizian and F. Ayazi, "Laterally-excited silicon bulk acoustic resonators with sidewall AlN," in *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International*, pp. 1520–1523, June 2011.

[57] S. Marksteiner, R. Aigner, *et al.*, "Optimization of acoustic mirrors for solidly mounted BAW resonators," in *Ultrasonics Symposium, 2005 IEEE*, vol. 1, pp. 329–332, 2005.

[58] W. Wang and D. Weinstein, "Acoustic Bragg reflectors for Q-enhancement of unreleased MEMS resonators," in *Frequency Control and the European Frequency and Time Forum (FCS), 2011 Joint Conference of the IEEE International*, pp. 1–6, 2011.

[59] V. Kaajakari, A. Alastalo, and T. Mattila, "Electrostatic transducers for micromechanical resonators: free space and solid dielectric," *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 53, no. 12, pp. 2484–2489, 2006.

[60] A. Grill, S. Gates, C. Dimitrakopoulos, V. Patel, S. Cohen, Y. Ostrovski, E. Liniger, E. Simonyi, D. Restaino, S. Sankaran, S. Reiter, A. Demos, K. S. Yim, V. Nguyen, J. Rocha, and D. Ho, "Development and optimization of porous psicoh interconnect dielectrics for 45 nm and beyond," in *Interconnect Technology Conference, 2008. IITC 2008. International*, pp. 28–30, 2008.

[61] J. Choma and W. K. Chen, *Feedback Networks: Theory and Circuit Applications*. World Scientific Publishing Co., 2007.

[62] J. A. Judge, B. H. Houston, D. M. Photiadis, and P. C. Herdic, "Effects of disorder in one- and two-dimensional micromechanical resonator arrays for filtering," *Journal of Sound and Vibration*, vol. 290, no. 35, pp. 1119 – 1140, 2006.

[63] Y. Lin, W.-C. Li, B. Kim, Y.-W. Lin, Z. Ren, and C.-C. Nguyen, "Enhancement of micromechanical resonator manufacturing precision via mechanically-coupled arraying," in *Frequency Control Symposium, 2009 Joint with the 22nd European Frequency and Time forum. IEEE International*, pp. 58–63, 2009.

[64] R. Melamud, S. A. Chandorkar, B. Kim, H. K. Lee, J. Salvia, G. Bahl, M. Hopcroft, and T. Kenny, "Temperature-Insensitive Composite Micromechanical Resonators," *Microelectromechanical Systems, Journal of*, vol. 18, no. 6, pp. 1409–1419, 2009.

[65] S. Wang, W.-C. Chen, B. Bahr, W. Fang, S.-S. Li, and D. Weinstein, "Temperature coefficient of frequency modeling for CMOS-MEMS bulk mode composite resonators." 2015.

[66] W.-H. Chuang, T. Luger, R. K. Fettig, and R. Ghodssi, "Mechanical property characterization of LPCVD silicon nitride thin films at cryogenic temperatures," *Microelectromechanical Systems, Journal of*, vol. 13, no. 5, pp. 870–879, 2004.

[67] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *Power Delivery, IEEE Transactions on*, vol. 14, no. 3, pp. 1052–1061, 1999.

[68] Z. Mahmood, R. Suaya, and L. Daniel, "An efficient framework for passive compact dynamical modeling of multiport linear systems," in *Design, Automation Test in Europe Conference Exhibition (DATE), 2012*, pp. 1203–1208, 2012.

[69] S. Mohammadi, A. A. Eftekhar, W. D. Hunt, and A. Adibi, "High-Q micromechanical resonators in a two-dimensional phononic crystal slab," *Applied Physics Letters*, vol. 94, no. 5, 2009.

[70] M. Ziaei-Moayyed, M. Su, C. Reinke, I. El-Kady, and R. Olsson, "Silicon carbide phononic crystal cavities for micromechanical resonators," in *Micro Electro Mechanical Systems (MEMS), 2011 IEEE 24th International Conference on*, pp. 1377–1381, Jan 2011.

[71] Y. M. Soliman, M. F. Su, Z. C. Leseman, C. M. Reinke, I. El-Kady, and R. H. Olsson, "Phononic crystals operating in the gigahertz range with extremely wide band gaps," *Applied Physics Letters*, vol. 97, no. 19, 2010.

[72] R. Olsson, S. Griego, I. El-Kady, M. Su, Y. Soliman, D. Goettler, and Z. Leseman, "Ultra high frequency (UHF) phononic crystal devices operating in mobile communication bands," in *Ultrasonics Symposium (IUS), 2009 IEEE International*, pp. 1150–1153, Sept 2009.

[73] R. Olsson, M. Ziaei-Moayyed, B. Kim, C. Reinke, M. Su, P. Hopkins, Y. Soliman, D. Goettler, Z. Leseman, and I. El-Kady, "Micro and nano fabricated phononic crystals: technology and applications," in *Ultrasonics Symposium (IUS), 2011 IEEE International*, pp. 983–988, Oct 2011.

[74] B. Bahr, R. Marathe, and D. Weinstein, "Theory and design of phononic crystals for unreleased CMOS-MEMS resonant body transistors." 2015.

[75] M. S. Kushwaha *et al.*, "Acoustic band structure of periodic elastic composites," *Phys. Rev. Lett.*, vol. 71, pp. 2022–2025, 1993.

[76] B. Greene *et al.*, "High performance 32nm SOI CMOS with high-k/metal gate and $0.149\mu m^2$ SRAM and ultra low-k back end with eleven levels of copper," in *VLSI Technology, 2009 Symposium on*, pp. 140–141, 2009.

[77] J. Joannopoulos, S. Johnson, J. Winn, and R. Meade, *Photonic Crystals: Molding the Flow of Light (Second Edition)*. Princeton University Press, 2011.

[78] A. Grill, "Porous pSiCOH Ultralow-k Dielectrics for Chip Interconnects Prepared by PECVD," *Annual Review of Materials Research*, vol. 39, no. 1, pp. 49–69, 2009.

[79] G. Degrande, G. D. Roeck, P. v. d. Broeck, and D. Smeulders, "Wave propagation in layered dry, saturated and unsaturated poroelastic media," *International Journal of Solids and Structures*, vol. 35, no. 34, pp. 4753–4778, 1998.

[80] H. Jaffe and D. Berlincourt, "Piezoelectric transducer materials," *Proceedings of the IEEE*, vol. 53, pp. 1372–1386, Oct 1965.

[81] V. Bottom, *Introduction to Quartz Crystal Unit Design*. Electrical-Computer Science and Engineering Series, Van Nostrand Reinhold, 1982.

[82] R. Ruby, P. Bradley, I. Larson, J., Y. Oshmyansky, and D. Figueredo, "Ultra-miniature high-Q filters and duplexers using FBAR technology," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, pp. 120–121, Feb 2001.

[83] J. Molarius, A. Nurmela, T. Pensala, M. Ylilammi, and A. Dommann, "ZnO for thin film BAW devices," in *Ultrasonics Symposium, 2005 IEEE*, vol. 3, pp. 1816–1819, Sept 2005.

[84] R. Abdolvand and F. Ayazi, "7e-4 enhanced power handling and quality factor in thin-film piezoelectric-on-substrate resonators," in *Ultrasonics Symposium, 2007. IEEE*, pp. 608–611, Oct 2007.

[85] V. Kaajakari, T. Mattila, A. Oja, and H. Seppa, "Nonlinear limits for single-crystal silicon microresonators," *Microelectromechanical Systems, Journal of*, vol. 13, pp. 715–724, Oct 2004.

[86] E. W. Greeneich and R. S. Muller, "Theoretical transducer properties of piezoelectric insulator FET transducers," *Journal of Applied Physics*, vol. 46, no. 11, pp. 4631–4640, 1975.

[87] R. D. Vispute, J. Narayan, H. Wu, and K. Jagannadham, "Epitaxial growth of AlN thin films on silicon (111) substrates by pulsed laser deposition," *Journal of Applied Physics*, vol. 77, no. 9, pp. 4724–4728, 1995.

[88] G. Gautschi, *Piezoelectric Sensorics: Force, Strain, Pressure, Acceleration and Acoustic Emission Sensors, Materials and Amplifiers*. Engineering online library, Springer, 2002.

[89] Z. Wang, A. Morimoto, T. Kawae, H. Ito, and K. Masugata, "Growth of preferentially-oriented AlN films on amorphous substrate by pulsed laser deposition," *Physics Letters A*, vol. 375, no. 33, pp. 3007 – 3011, 2011.

[90] G. F. Iriarte, F. Engelmark, and I. V. Katardjiev, "Reactive sputter deposition of highly oriented AlN films at room temperature," *Journal of Materials Research*, vol. 17, pp. 1469–1475, 2002.

[91] T. Kehagias, L. Lahourcade, A. Lotsari, E. Monroy, G. Dimitrakopulos, and P. Komninou, "Interfacial structure of semipolar AlN grown on m-plane sapphire by MBE," *Physica Status Solidi (B) Basic Research*, vol. 247, no. 7, pp. 1637–1640, 2010.

[92] Q. Ma, L. Wang, and V. Rao, "Film bulk acoustic resonator structure and method of making," Nov. 23 2004. US Patent 6,822,535.

[93] S. Saravanan, E. Keim, G. Krijnen, and M. Elwenspoek, "Growth and surface characterization of piezoelectric AlN thin films on silicon (100) and (110) substrates," in *Microscopy of Semiconducting Materials* (A. Cullis and J. Hutchi-

son, eds.), vol. 107 of *Springer Proceedings in Physics*, pp. 75–78, Springer, July 2005.

[94] S. Mishin, D. Marx, B. Sylvia, V. Lughi, K. Turner, and D. Clarke, "Sputtered AlN thin films on Si and electrodes for MEMS resonators: relationship between surface quality microstructure and film properties," in *Ultrasonics, 2003 IEEE Symposium on*, vol. 2, pp. 2028–2032 Vol.2, Oct 2003.

[95] H.-P. Lobl, M. Klee, C. Metzmacher, W. Brand, R. Milsom, P. Lok, and R. Van Straten, "Piezoelectric materials for BAW resonators and filters," in *Ultrasonics Symposium, 2001 IEEE*, vol. 1, pp. 807–811 vol.1, 2001.

[96] H.-P. Lobl, M. Klee, O. Wunnicke, R. Kiewitt, R. Dekker, and E. Pelt, "Piezoelectric AlN and PZT films for micro-electronic applications," in *Ultrasonics Symposium, 1999. Proceedings. 1999 IEEE*, vol. 2, pp. 1031–1036 vol.2, 1999.

[97] R. Lanz and P. Muralt, "Solidly mounted BAW filters for 8 GHz based on AlN thin films," in *Ultrasonics, 2003 IEEE Symposium on*, vol. 1, pp. 178–181 Vol.1, Oct 2003.

[98] M. Ziaei-Moayyed, D. Elata, E. P. Quvy, and R. T. Howe, "Differential internal dielectric transduction of a Lamé-mode resonator," *Journal of Micromechanics and Microengineering*, vol. 20, no. 11, p. 115036, 2010.

[99] S. Bhave, D. Gao, R. Maboudian, and R. Howe, "Fully-differential poly-SiC Lamé mode resonator and checkerboard filter," in *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, pp. 223–226, Jan 2005.

[100] M. Demirci and C.-C. Nguyen, "Mechanically corner-coupled square microresonator array for reduced series motional resistance," *Microelectromechanical Systems, Journal of*, vol. 15, pp. 1419–1436, Dec 2006.

[101] C.-C. Nguyen, "MEMS technology for timing and frequency control," *Ultrasonics, Ferroelectrics, and Frequency Control, IEEE Transactions on*, vol. 54, pp. 251–270, February 2007.

[102] D. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, pp. 329–330, Feb 1966.

[103] K. L. Ekinci, Y. T. Yang, and M. L. Roukes, "Ultimate limits to inertial mass sensing based upon nanoelectromechanical systems," *Journal of Applied Physics*, vol. 95, no. 5, pp. 2682–2689, 2004.

[104] H. Johari and F. Ayazi, "Capacitive bulk acoustic wave silicon disk gyroscopes," in *Electron Devices Meeting, 2006. IEDM '06. International*, pp. 1–4, Dec 2006.

[105] F. Ayazi, L. Sorenson, and R. Tabrizian, "Energy dissipation in micromechanical resonators," vol. 8031, pp. 803119–803119–13, 2011.

[106] B. Auld, *Acoustic Fields and Waves in Solids.* No. v. 1 in Acoustic Fields and Waves in Solids, Krieger, 1990.

[107] I. P.-T. Institute, "New Semiconductor Materials. Characteristics and Properties," Mar. 2014.

[108] "IEEE Standard on Piezoelectricity," *ANSI/IEEE Std 176-1987*, 1988.

[109] I. Larson, J.D., R. Ruby, P. Bradley, and Y. Oshmyansky, "A BAW antenna duplexer for the 1900 MHz PCS band," in *Ultrasonics Symposium, 1999. Proceedings. 1999 IEEE*, vol. 2, pp. 887–890 vol.2, 1999.

[110] A. Barlian, W.-T. Park, J. Mallon, A. Rastegar, and B. Pruitt, "Review: Semiconductor Piezoresistance for Microsystems," *Proceedings of the IEEE*, vol. 97, pp. 513–552, March 2009.

[111] W. Thomson, "On the Electro-Dynamic Qualities of Metals:-Effects of Magnetization on the Electric Conductivity of Nickel and of Iron," *Proceedings of the Royal Society of London*, vol. 8, pp. 546–550, 1856.

[112] C. S. Smith, "Piezoresistance Effect in Germanium and Silicon," *Phys. Rev.*, vol. 94, pp. 42–49, Apr 1954.

[113] C. Herring, "Transport Properties of a Many-Valley Semiconductor," *Bell System Technical Journal*, vol. 34, no. 2, pp. 237–290, 1955.

[114] M. Esashi, S. Sugiyama, K. Ikeda, Y. Wang, and H. Miyashita, "Vacuum-sealed silicon micromachined pressure sensors," *Proceedings of the IEEE*, vol. 86, pp. 1627–1639, Aug 1998.

[115] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proceedings of the IEEE*, vol. 86, pp. 1640–1659, Aug 1998.

[116] M. Tortonese, "Advances in piezoresistive cantilevers for atomic force microscopy," in *Atomic Force Microscopy/Scanning Tunneling Microscopy 2* (S. Cohen and M. Lightbody, eds.), pp. 147–153, Springer US, 1997.

[117] G. R. Higson, "Recent advances in strain gauges," *Journal of Scientific Instruments*, vol. 41, no. 7, p. 405, 1964.

[118] Y. Sun, S. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 101, May 2007.

[119] Y. Kanda, "A graphical representation of the piezoresistance coefficients in silicon," *Electron Devices, IEEE Transactions on*, vol. 29, pp. 64–70, Jan 1982.