Virtual Ground Reference Buffer Technique in Switched-Capacitor Circuits

by

Hyun Ho Boo

B.S., Electrical Engineering
University of Illinois at Urbana-Champaign (2007)
S.M., Electrical Engineering and Computer Science
Massachusetts Institute of Technology (2009)

Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
June 2015

Author ..... Signature redacted .....
Department of Electrical Engineering and Computer Science
May 18, 2015

Certified by..... Signature redacted .....
Duane S. Boning
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by..... Signature redacted .....
Hae-Seung Lee
ATSP Professor of Electrical Engineering
Thesis Supervisor

Accepted by ..... Signature redacted .....
Leslie A. Kolodziejski
Chair, Department Committee on Graduate Students

Virtual Ground Reference Buffer Technique in Switched-Capacitor Circuits

by

Hyun Ho Boo

Submitted to the Department of Electrical Engineering and Computer Science
on May 18, 2015, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

The performance of switched-capacitor circuits depends highly on the op-amp specifications. In conventional designs, trade-offs in speed, noise, and settling accuracy make it difficult to implement power-efficient switched-capacitor circuits. The problem originates from the inverse relationship between the feedback factor and the signal gain. This thesis proposes the virtual ground reference buffer technique that enhances performance by improving the feedback factor of the op-amp without affecting signal gain. A key concept in the technique is the bootstrapping action of level-shifting buffers. It exploits op-amp-based circuits whose principles are very well understood and the design techniques are mature. The solution ultimately relaxes the required op-amp requirements including unity-gain bandwidth, noise, offset voltage and open-loop gain that would otherwise result in complex design and high power consumption. The concept is demonstrated in a 12-b 250MS/s pipelined ADC.

Thesis Supervisor: Duane S. Boning
Title: Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Hae-Seung Lee
Title: ATSP Professor of Electrical Engineering

Acknowledgments

I first arrived at MIT as a graduate student in the fall of 2007. After completing my S.M. degree with Professor Joel L. Dawson in February of 2009, I worked in Korea until August 2012 to fulfill my national service requirement. During that time, I envisioned myself returning to MIT to obtain my Ph.D. degree, and in 2012, I very happily returned to Cambridge. With that remarkable Ph.D. journey now coming to an end with the submission of this dissertation, I only hope I can reciprocate here at least a fraction of what I have kindly received from the countless number of people who have influenced me in many positive ways throughout these last few years.

I would like to thank Professor Duane S. Boning for welcoming me to his group in 2012. He was very generous in offering me a position, and with his remarkable support, I was able to return to MIT and pursue my Ph.D. I cannot express the depth of gratitude I owe him for giving me that opportunity and setting me on the journey that has led me to where I am today. Without him, my graduate student experience would have been much more difficult, less satisfying, and certainly less fruitful. He has given me his kind and consistent guidance and encouragement throughout my entire journey at MIT. He also encouraged me to look into the process variations of circuit design, which was a direction I appreciated immensely. I feel privileged to have learned so much from his wisdom, and I will always remember how vital he was to my Ph.D. study.

Professor Hae-Seung Lee has been an incredible mentor, and I have been more than fortunate to have had him as my advisor along with Professor Boning. His insights on integrated circuits have been awe-inspiring. He always showed much patience and expressed his constant faith in me throughout my research. He was available whenever I needed advice on resolving design challenges. Daily, he offered remarkable creative ideas and indeed always set the highest of bars for my work. I am sure that the learning I have acquired from him will have an immeasurable impact on my career long after I leave MIT.

I would like to thank my thesis committee member, Professor Anantha P. Chan-

drakasan. Although our interaction was limited due to his busy schedule, he took an interest in my work and gave me constructive feedback. I would also like to thank Professor Joel L. Dawson for advising me when I was an inexperienced student beginning the Master's program. He guided me through my first research project and inspired me to push forward and fulfill my educational goals.

I am very grateful to Albert Chang, John Haeseon Lee, Joy Johnson, and Li Yu in the Boning group. Not only have they given me technical and non-technical help from time to time, but more importantly, they have become incredible personal friends. Like so many other graduate students, I experienced both the thrilling and the difficult moments that are a part of student life. They were friends on whom I could rely and candidly talk about any issues that troubled me. They have steadily been with me throughout my journey, and I will always remember the wonderful times I was fortunate to have spent with them.

I also want to thank the members of the HSLee group: Sunghyuk Lee, Sungwon Chung, Daniel Kumar, Joohyun Seo, Sabino Pietrangelo, Xi Yang, Do Yeon Yoon, and Harneet Khurana. This team became a great company of learning. Sunghyuk taught me the basics of pipelined ADC in the beginning and gave me sound advice on measurements. I relied heavily on Sungwon for my Master's work, and he was always open and available whenever help was needed. Other members of this group have helped me as well, and it was always exciting and invigorating just to hang around them.

There are also many friends outside of the Boning and HSLee groups within and outside of MIT who have influenced me. These include members of the Dawson group during my Master's years, friends who I have met in classes or various activities, and my dear friends in Korea. I especially would like to express my deep appreciation and thanks to Geumok An for being an amazing friend for so many years. I cannot list all these people by name, so I happily acknowledge them all together here. Each impacted me in a unique way, and I would not have become the person I am today without their steadfastness and encouragement. I am constantly reminded of how everyone brought a difference into my life and changed it for the better.

I would like to thank the MIT/Masdar Institute Cooperative Program for their funding and the Taiwan Semiconductor Manufacturing Company (TSMC) for chip fabrication. Their contributions to my effort and the completion of my work at MIT were invaluable and fully supportive.

Lastly, I thank my family for their always unconditional love. My dissertation is dedicated to them. I am grateful to my parents, Sung Youn Boo and Young Nim Park, and my sister, Soo Jung Boo, for everything they have given me in life. I have been incredibly fortunate to have been brought up in a loving family, and indeed I would not be here completing this Ph.D. if it were not for them. My family will always be with me, supporting me in every future step that I take in life. I especially thank my parents for showing their unconditional love always and forever. They have done so much for me throughout my graduate student life–sending me delicious Korean food from Texas to make sure I stay healthy, being patient with my phone calls, encouraging me to endure each and every difficult time, and much more. They have sacrificed for me beyond measure. Thank you. I love you.

To My Loving Family

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Advances in electronic systems continue to demand improvement in speed, resolution, and power efficiency in Analog-to-Digital Converters (ADCs). The ADC is a key component in such systems since it bridges the real world analog signals to the digital signal domain in which the core signal computation and processing takes place. As more functionalities are being integrated in digital circuits, the need to implement high performance ADCs has become more critical than ever. The digital circuits continue rapid development with the help of technology node scaling, and ADCs with improved performance are required to avoid becoming the system bottleneck.

The choice of ADC topology depends on the target frequency and the resolution of the application. Figure 1-1 shows the signal-to-noise-and-distortion ratio (SNDR) as a function of the sampling frequency for each ADC topology published in the International Solid-State Circuits Conference (ISSCC) and Symposium on VLSI Circuits from 1997 to 2015 [1]. Sigma-Delta ($\Sigma\Delta$) ADCs dominate the high-resolution and low sampling speed applications. This topology spreads quantization noise across a wide frequency range via oversampling and implements a noise-shaping profile to further improve the signal-to-noise ratio (SNR). The quantization noise is then filtered and the data rate is decimated since sample rate only needs to be twice the input signal frequency for reconstruction.

Successive-Approximation-Register (SAR) ADCs are very popular in the medium to high-resolution and low to mid-speed segment. SAR ADCs are widely known to

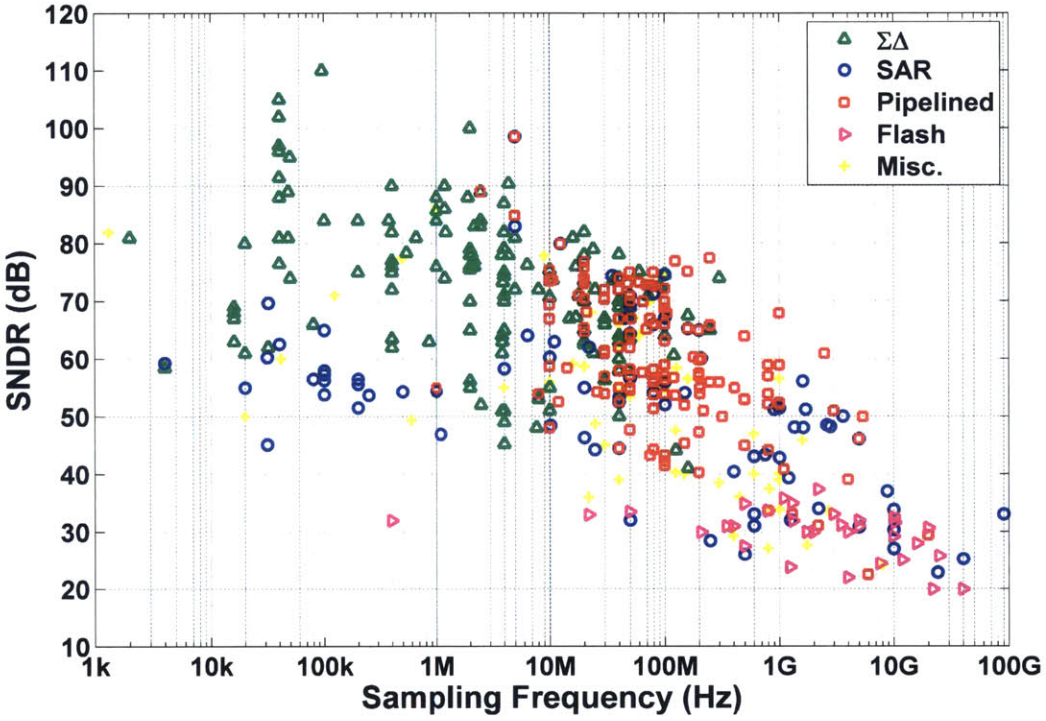


Figure 1-1: SNDR vs. sampling frequency based on the performance of published ADCs in ISSCC and VLSI from 1997 to 2015.

have the highest energy efficiency as power dissipation is mostly from the comparator and capacitor array switching activities. The SAR ADC sampling frequency is lower than its internal clock frequency since it performs a search algorithm on each sampled signal; the number of internal clock cycles needed for a single search depends on the resolution and the implemented search scheme. The settling time of the digital-to-analog converter (DAC) and the delay from the comparator decision and logic circuit must be minimized for fast operation. Finally, SAR ADC performance scales well with the technology since it does not rely on power-hungry analog circuit blocks.

Pipelined ADCs are popular in applications where the sampling rate reaches above 100MS/s and resolution as high as 16-bits is required. The pipelined ADC topology increases throughput at the cost of latency and power consumption. Although pipelined ADCs are typically designed to operate at higher sampling speed than SAR ADCs, its reliance on op-amps aggravates the design challenges. The op-amp becomes the performance bottleneck as it suffers from linearity, bandwidth, and noise issues and

consumes a large amount of power.

Flash ADCs dominate in high-speed and low to medium resolution design space. In its simplest form, a flash ADC is comprised of an array of comparators with reference voltages for the comparators' decision levels. Although this is the fastest architecture, the number and accuracy of comparators generally double for each additional resolution bit, making it difficult to achieve high resolution.

The Walden's figure of merit (FoM) is used most commonly for standard comparison among ADCs:

$$FoM_W = \frac{\text{Power}}{2\text{BW}2^{\text{ENOB}}}, \tag{1.1}$$

where the effective number of bits (ENOB) is

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}. \tag{1.2}$$

The Walden FoM is based on the assumption that power consumption is a linear function of the bandwidth, BW. However, this is not the case in actual circuits. For example, in an op-amp-based topology, the bandwidth is a linear function of the op-amp transconductance, and both the current in the op-amp as well as the transistor size must be scaled up to increase bandwidth linearly to the current consumption. However, increasing the transistor size adds internal parasitic poles in the op-amp and the bandwidth is affected. In addition, the parasitic capacitance increases at the input of the op-amp and impacts the bandwidth by degrading the feedback factor. The Walden FoM also does not adequately reflect power consumption in ADCs with high ENOB. For thermal noise limited ADC, the capacitor size is quadrupled to increase the SNR and ENOB by 6dB and 1-bit, respectively [2]. In this case, the power consumption is increased by a factor of four and the FoM_W eventually worsens by a factor of two. Figure 1-2 shows the energy consumption in the ADC as a function of the SNDR. As expected $\Sigma\Delta$ ADCs achieve high SNDR and generally do not have FoM_W of 100fJ/step, while SAR ADCs boast much better FoM_W. For this reason,

Schreier's FoM is used in higher resolution ADCs:

$$FoM_S = DR_{dB} + 10\log\left[\frac{BW}{\text{Power}}\right] \tag{1.3}$$

where DR is the dynamic range of the ADC. This places a more fair emphasis on the achieved SNDR.

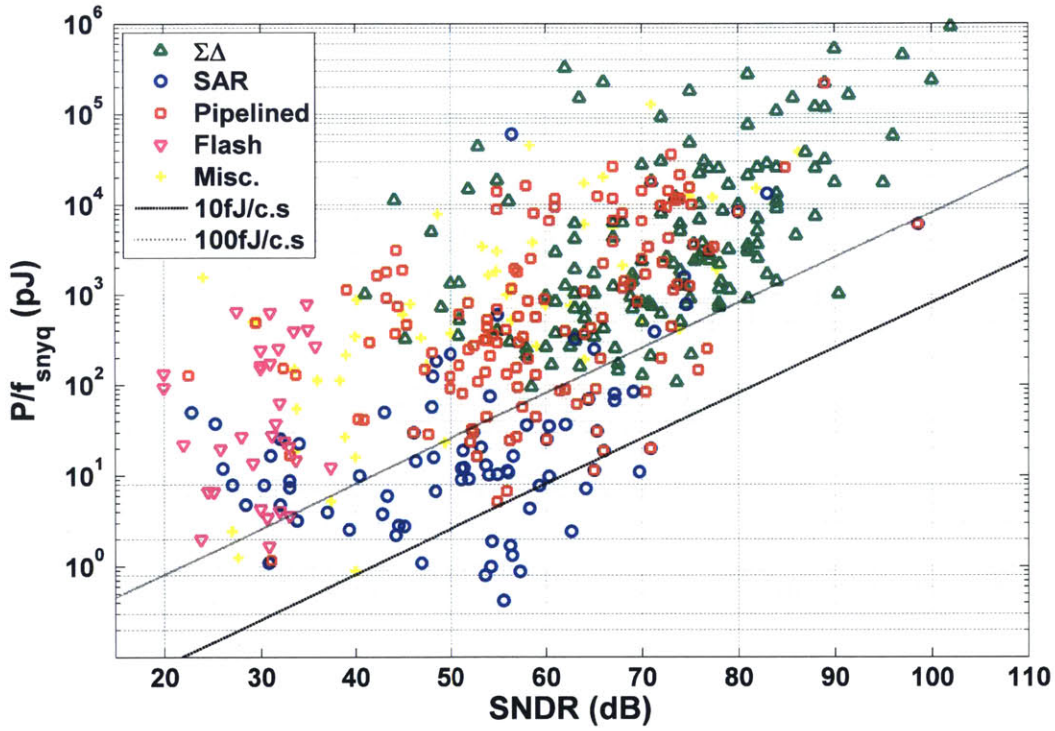
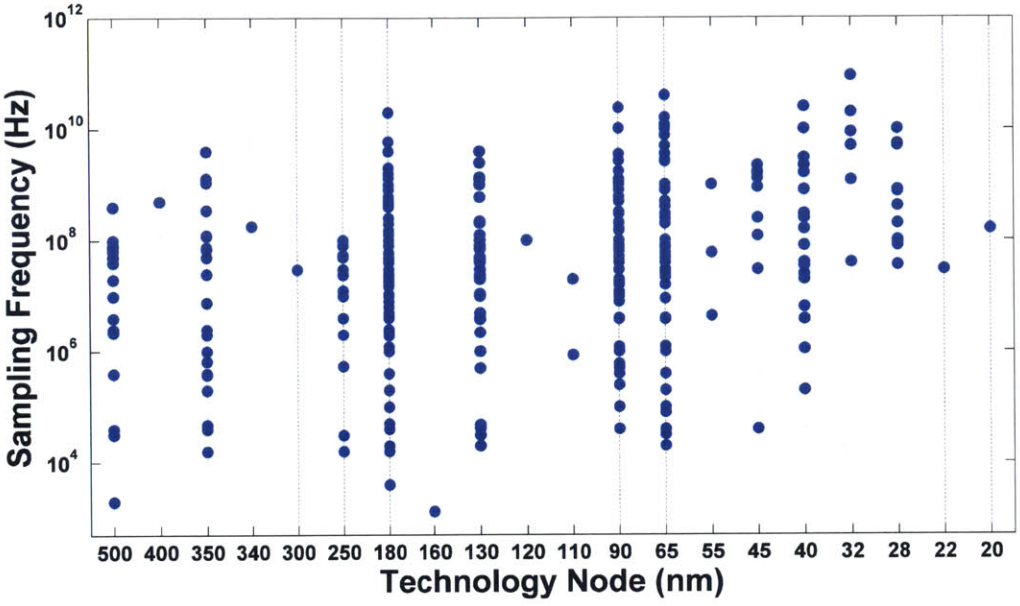


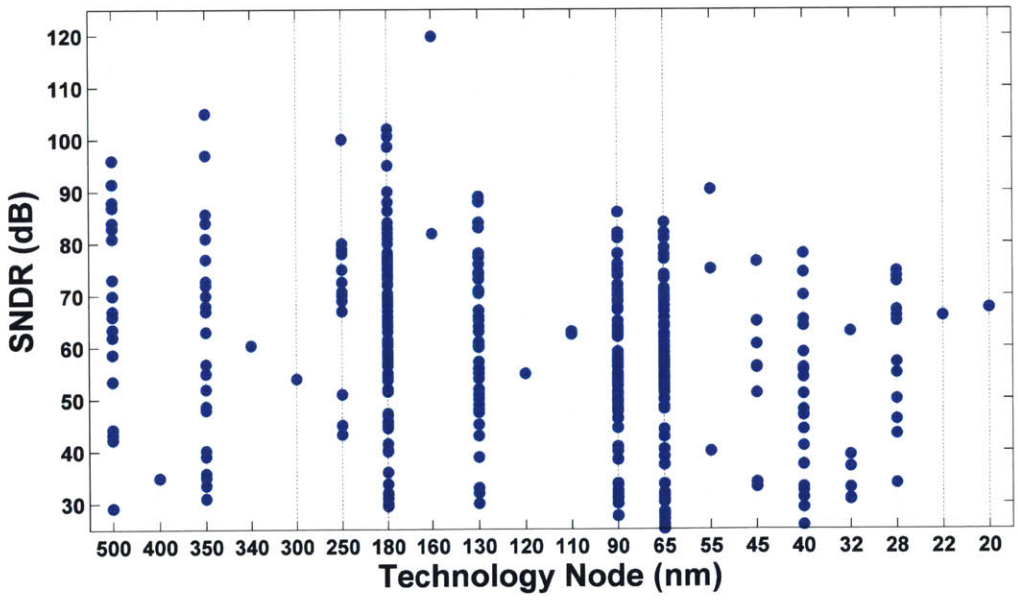
Figure 1-2: Energy vs. SNDR based on the performance of published ADCs in ISSCC and VLSI from 1997 to 2015.

The performance trend of sampling frequency and SNDR of published ADCs based on CMOS scaling is shown in Figure 1-3. Two observations are made. First, the sampling frequency has increased with scaling. This is a direct benefit from higher unity-gain current frequency, f_t, in scaled CMOS devices. The device parasitic capacitance is smaller and therefore circuit switching is faster, and the signal settling time is improved. The second observation is that SNDR tends to be lower in the advanced nodes. One explanation is the reduced supply voltage. To keep the devices in saturation mode, the signal swing range is now smaller and lower SNR is inevitable

unless considerable power is spent on lowering the noise floor. Another source of SNDR limitation is the reduced intrinsic transistor gain, aggravating the linearity. In short, although device scaling has improved the operating speed of the ADC, this is achieved at the cost of limited SNDR.



(a)



(b)

Figure 1-3: Performance of published ADCs for various CMOS process nodes: (a) Sampling Frequency, (b) SNDR.

1.1 Trends in Pipelined ADCs

The pipelined ADC architecture has gained popularity as it covers a wide range of applications, including imaging, Long Term Evolution (LTE), high-definition television (HDTV), and wireless local area network (WLAN). However, achieving an even higher sampling rate and resolution presents considerable number of challenges. Specifically, the switched-capacitor circuit that comprises the core of a pipelined ADC relies heavily on high performance op-amps, which have become increasingly difficult to implement. The scaling of CMOS results in low intrinsic gain and therefore low open-loop op-amp gain. Techniques such as gain enhancement and multi-stage configurations have been used at the cost of added power, noise and speed. To maintain the SNR at ever decreasing supply voltages, noise is reduced by increasing the sampling capacitance, which increases power consumption. Also, implementing high bandwidth op-amp circuits for high-speed operation increases power consumption and noise bandwidth. This has led to several directions in the development of pipelined ADCs.

A common approach is to employ low-gain and/or non-settling op-amps, and digitally calibrate the resulting nonlinearity [3, 4, 5, 6]. This takes advantage of the efficiency, flexibility, and scalability of digital CMOS. For example, in [3], a spline-based nonlinearity model is used to address the finite gain of the op-amp using digital background calibration. However, in order to track the power supply voltage and temperature, the calibration in general must run continuously in the background, which can consume significant power. In [4], the codes from each stage are used to construct an finite impulse response (FIR) with coefficients derived by an least mean squares (LMS) algorithm.

Analog techniques have also been employed to relax the open-loop gain requirements of the op-amp [7, 8, 9]. In one technique, the finite gain and in-band noise of the main op-amp is canceled by sampling a correction voltage onto the next-stage sampling capacitance through an auxiliary path [7]. An adaptive feedback algorithm is applied in the closed-loop calibration. While effective in removing errors due to

op-amp finite gain, the auxiliary path increases power consumption. The measurement results in [7] indicate maximum SNDR of 76.9dB at a sampling rate of 60MS/s. Correlated level shifting (CLS) is another technique that relaxes op-amp gain requirement and increases its output swing [8, 9]. The charge-transfer phase of the switched-capacitor circuit consists of the estimate phase in which a level-shifting capacitor samples a coarse output, and the level-shift phase in which the output settles to the final value. The drawback is the reduced speed due to the sampling and two settling periods required for its operation.

In other alternative approaches, the op-amp is replaced completely. Zero-crossing-based circuits (ZCBC) [10, 11, 12, 13, 14] are based on the insight that detecting the virtual ground node is more power-efficient than enforcing it with an op-amp in closed-loop. A current source applies a ramp across the capacitors and the zero-crossing detector detects the virtual ground crossing at which time the output sample is taken. While energy efficient, managing DC voltage drops across many switches requires considerable complexity [13]. In the pulsed bucket brigade (PBB) ADC [15, 16], the sampled input charge is re-used to charge the capacitors in the following stage and the voltage gain is achieved by capacitor scaling. Due to the nonlinearity of the circuit, continuous background calibration is necessary. Another alternative amplifier topology is a ring amplifier (RA) [17, 18, 19]. The speed of the RA-based switched-capacitor circuit is determined by the oscillating frequency, and the maximum sampling rate demonstrated thus far is 100MS/s at a modest 9-bit ENOB [19].

The principles of op-amp-based circuits are very well understood. This thesis takes further advantage of an op-amp-based circuit by introducing a technique that enables the design of power-efficient, high-speed, and high-resolution pipelined ADC. The proposed technique significantly relaxes key op-amp performance requirements including unity-gain bandwidth, noise, open-loop gain, and offset voltage. Complex digital background calibration is avoided. Since the op-amp is allowed to settle fully, calibration to remove charge-transfer error in PBB and in low gain or non-settling op-amp-based circuits is unnecessary. In addition, the transient current and corresponding voltage drop across switches and reference buffers in the ZCBCs and in

non-settling op-amp-based circuits are avoided. The circuit is also shown to achieve higher maximum operating speed than alternative methods.

1.2 Thesis Organization

The thesis is organized as follows. Chapter 2 gives an overview of the pipelined ADC topology and the problems that plague conventional designs. The performance requirements on the op-amp are detailed as these serve as a reference for comparison with the proposed work. Requirements in the sampling network, DAC linearity, and sub-ADC are also included. The input-referred noise contributions from the op-amp and the reference buffers are analyzed as well.

Chapter 3 introduces the virtual ground reference buffer (VGRB) technique. The key concept is capacitance bootstrapping action by a level-shifting buffer, and the feedback factor improvement this brings to the op-amp. First, the technique is explained in its simplest setting with the assumption of no parasitic capacitance. Then parasitic capacitance is considered for a more in-depth analysis. An equivalent block diagram of the system is used to derive the transfer function of the op-amp noise and the buffer noise. Lastly, the chapter discusses design issues such as how variations in the reference voltages from the multiple level-shifting buffers affect the differential reference voltage, and multiplying digital-to-analog converter (MDAC) residue.

In Chapter 4, the design of a 12-bit 250MS/s pipelined ADC using the VGRB technique is presented. Among the many circuit blocks that are detailed, such as the sampling network, op-amp, sub-ADC with offset calibration, the design of the level-shifting buffer is of critical importance. A circuit with good slewing is chosen to reduce transient settling time, and bulk biasing is applied as a coarse way to adjust the reference voltages. Since the reference voltage is internally generated in each stage by four level-shifting buffers, reference voltage tuning is necessary to compensate process variation and achieve high linearity. This is done by changing the current level via DAC control. The circuit implementation details are followed by discussion of the parasitic capacitance that limits the feedback factor. Finally, the input-referred

noise of the circuit is compared with that of the conventional circuit. Although the exact noise analysis depends on various implementation choices, it is shown that the proposed approach improves input-referred noise while simultaneously decreasing the required op-amp power compared with conventional approaches.

The testing of the fabricated chip is presented in Chapter 5. The measurement results are consistent across multiple-chips and compare well against other single-channel ADCs with similar performance specifications. The prototype chip was not fully power-optimized and future designs have potential for substantial further power savings.

Finally, Chapter 6 summarizes the contributions of this work and proposes future directions. It addresses both circuit and system level improvements that should be explored.

Chapter 2

Pipelined ADC Overview

This chapter begins with an overview of how a pipelined ADC operates. The details include the conversion process in each pipelined stage and how the digital bits are combined to construct the output code. Then, the chapter analyzes how performance specifications are allocated in the sampling network, MDAC, and sub-ADC. Especially, the requirements in the op-amp open-loop gain and bandwidth, and the input-referred thermal noise are the key challenges that the proposed technique in Chapter 3 addresses.

2.1 Pipelined ADC Architecture

A pipelined ADC is capable of resolving medium to high resolution with high sampling rates and consists of a cascade of several low resolution stages. In each pipelined stage, the input is first quantized to low resolution digital bits by a flash-based sub-ADC. The quantized bits are then converted back into an analog voltage through a DAC and subtracted from the original input signal to produce an error voltage. The error voltage is amplified by the residue amplifier to extend the error voltage range to the reference range. The last stage is implemented in a flash ADC. Finally, the bits from each stage are time-aligned and combined to give the final output code.

Figure 2-1 shows an example block diagram of a pipelined ADC with M stages and $B_j = B_{j+1} = B_{RA,j} = B_{RA,j+1} = 2$ in stages j and $j+1$. B_j and B_{j+1} are the

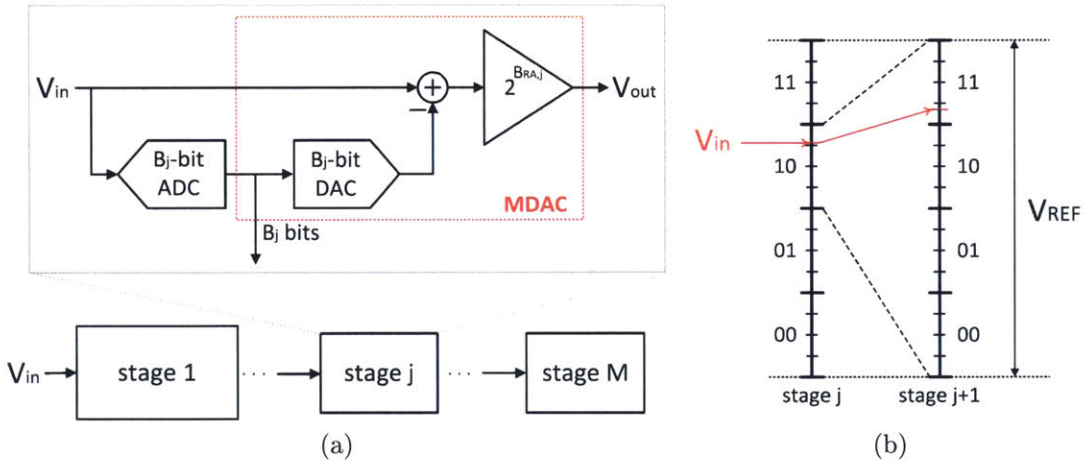


Figure 2-1: (a) General block diagram of a pipelined ADC and (b) the residue amplification for $B_j = B_{j+1} = B_{RA,j} = B_{RA,j+1} = 2$.

quantization resolution in the j_{th} and $(j+1)_{th}$ stage, respectively, and $2^{B_{RA,j}}$ and $2^{B_{RA,j+1}}$ are the signal gain in the j_{th} stage and $(j+1)_{th}$ stage, respectively. The B-bit DAC and residue amplifier are implemented in the MDAC circuit block. In the demonstrated example, two-bits are resolved and the residue is amplified by a factor of four in both the j_{th} and $(j+1)_{th}$ stage. In Figure 2-1b, for an input voltage in the range of $\frac{11}{16}V_{REF} < v_{IN} < \frac{12}{16}V_{REF}$, the j_{th} and $(j+1)_{th}$ stage outputs (10) and (11), respectively.

The digital bits from the pipelined stages are processed according to the signal gain of each stage and then combined to obtain the final digital output code. The digital bits B_{j+1} from the $(j+1)_{th}$ stage are multiplied by $2^{B_{RA,j+1}}$ and added to the back-end digital code constructed from the $(j+2)_{th}$ stage to the M_{th} stage. Likewise, the digital bits B_j from the j_{th} stage are multiplied by $2^{B_{RA,j}}$ and added to the digital code constructed from the $(j+1)_{th}$ stage to the M_{th} stage. This is repeated along the pipelined stages. The digital output code, D, is expressed as

$$D = (\cdots(((B_1 2^{B_{RA,1}}) + B_2)2^{B_{RA,2}} + B_3)2^{B_{RA,3}} + \cdots)2^{B_{RA,M+1}} + B_M. \tag{2.1}$$

The signal gain is typically set to a power of two. Simply shifting the digital bits can realize the multiplication. If $B_j > B_{RA,j}$, then the ADC has redundancy and can tolerate sub-ADC errors and any DC shifts in the residue. This over-range

is a function of the MDAC output linearity range as well as the input range of the following stage.

Each pipelined stage requires one clock cycle to resolve the digital bits and amplify the residue. Therefore, the latency of a pipelined ADC is equivalent to several clock cycles, or the number of stages. However, a new digital code output is obtained in every clock cycle for high throughput. The first stage has the most stringent requirements in terms of input-referred noise and accuracy. The accuracy requirements in the following stages are relaxed by the number of bits resolved in the preceding stages. Therefore, the power consumption, design complexity, and area are reduced along the pipelined stages [20, 21, 22, 23, 24].

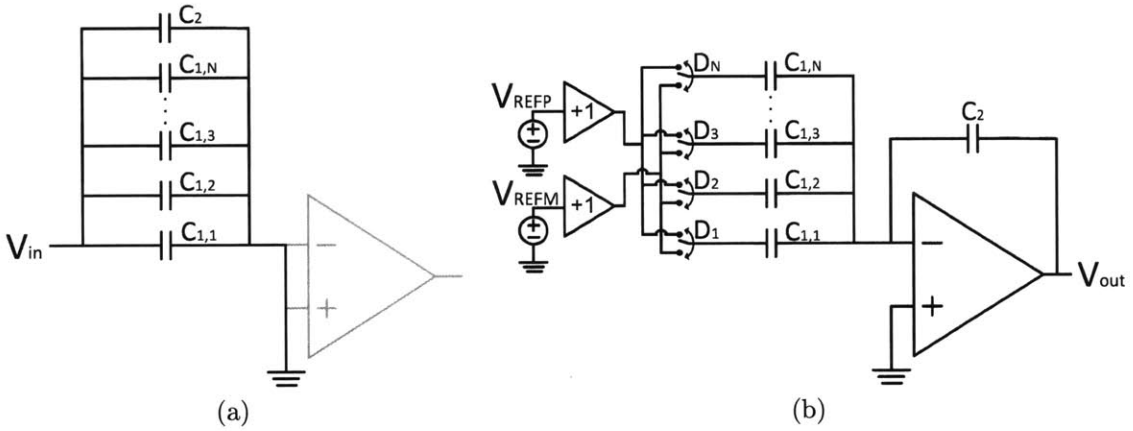


Figure 2-2: (a) Sample and (b) charge-transfer operation of the switched-capacitor circuit in a pipelined stage.

The MDAC is implemented in a switched-capacitor circuit. Figure 2-2 illustrates a simplified singled-ended sampling and charge-transfer operation of an MDAC in a conventional pipelined stage. In the sampling phase, input voltage is sampled on capacitors C_1 and C_2. C_1 consists of N unit capacitors, $C_{1,1}, C_{1,2} \cdots C_{1,N}$. In the charge transfer phase, C_2 flips around the op-amp and the $C_{1,i}$ unit capacitors are driven by either the positive reference voltage, V_{REFP}, or the negative reference voltage, V_{REFM}, depending on the sub-ADC bit-decisions. Since the op-amp is not required in the sampling phase, it can be shared with the adjacent stage to save power [25, 26]. In high-speed circuits, on-chip reference buffers are typically used; while off-chip bypass capacitors can be used in conventional circuits to ease the reference buffer re-

quirements [27, 28, 29], on-chip high-speed buffers are strongly desired in high-speed, high-SNR ADCs to avoid reference voltage ringing [30, 31, 32]. Assuming an ideal op-amp with infinite gain and no parasitic capacitance, the output voltage settles to

$$v_{OUT} = \frac{\sum_{i=1}^{N} C_{1,i} + C_2}{C_2} v_{IN} - \left[\frac{\sum_{i=1}^{k} C_{1,i}}{C_2} V_{REFP} + \frac{\sum_{i=k+1}^{N} C_{1,i}}{C_2} V_{REFM} \right] \tag{2.2}$$

where k is the sub-ADC output code. The term $\frac{\sum_{i=1}^{N} C_{1,i} + C_2}{C_2}$ is the signal gain G_s.

2.2 Accuracy Considerations

The performance specifications of the circuit blocks depend on the targeted speed and resolution of the pipelined ADC. The design requirements are derived and discussed in detail throughout this section.

2.2.1 Sampling Accuracy

The RC time constant of the sampling network must be short enough for the settling accuracy required. The sampling network results in an exponential settling behavior in the output voltage,

$$v_{OUT}(t) = v_{IN}\left(1 - e^{\frac{-t}{\tau}}\right), \tag{2.3}$$

where v_{IN} is the input voltage and the time constant is $\tau = RC$. The output voltage with $\frac{1}{4}$LSB settling accuracy in a B_T-bit resolution converter is

$$v_{OUT}\Big|_{\frac{1}{4}LSB} = v_{IN}\left(1 - \frac{1}{2^{B_T+2}}\right). \tag{2.4}$$

The required number of time constants for the targeted output accuracy is solved by equating Equation 2.3 to Equation 2.4 and solving for the time constant:

$$t_{\frac{1}{4}LSB} = -\tau \ln\left(\frac{1}{2^{B_T+2}}\right). \tag{2.5}$$

Table 2.1 shows the results for the charge time needed for 8, 10, 12, and 14-bit conversion with $\frac{1}{4}$LSB accuracy.

Resolution	Charge time
8-b	6.93τ
10-b	8.32τ
12-b	9.70τ
14-b	11.09τ

Table 2.1: Charge time required for $\frac{1}{4}$LSB accuracy.

2.2.2 Aperture Jitter

The short interval time required to disconnect the capacitance from the input signal source is called the aperture time. Aperture time leads to a final sampled value that is a delayed version of the input signal. Although the fixed delay itself is not a problem, the sample-to-sample variation in the aperture time results in sampling voltage error. This is exacerbated by the frequency of the input signal as demonstrated in Figure 2-3.

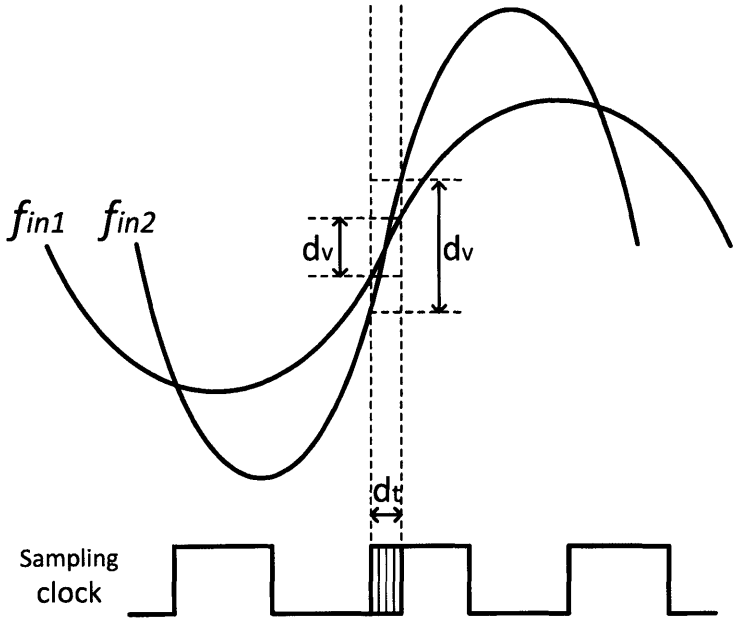


Figure 2-3: Effect of aperture jitter on the error of sampled voltage for two different input signal frequencies.

Consider a sine wave input signal with amplitude V_a and input frequency f_{in}

$$v_{IN}(t) = V_a \sin(2\pi f_{in} t). \tag{2.6}$$

The magnitude of the sampled voltage error is proportional to the time derivative of the function

$$\left| \frac{\mathrm{d}v_{IN}}{\mathrm{d}t} \right| = 2\pi f_{in} V_a \cos(2\pi f_{in} t). \tag{2.7}$$

The maximum error occurs at $t = 0$ when $\cos(2\pi ft) = 1$. This corresponds to the zero-crossing instant of the input signal. At the instant of maximum error, Equation 2.7 is simplified to

$$\frac{\Delta v_{rms}}{t_{jitter}} = \frac{2\pi f_{in} V_a}{\sqrt{2}}, \tag{2.8}$$

where Δv_{rms} is the error voltage in rms, and t_{jitter} is the aperture jitter. The rms signal to rms noise ratio is given by

$$SNR = 20\log_{10}\left(\frac{\frac{V_a}{\sqrt{2}}}{\Delta v_{rms}}\right) = 20\log_{10}\left(\frac{1}{2\pi f_{in} t_{jitter}}\right). \tag{2.9}$$

This assumes that the sampling circuit does not suffer from any thermal noise and that the aperture jitter is the only factor affecting SNR. Equation 2.9 is plotted in Figure 2-4. Aperture jitter leads to SNR degradation at high input frequencies. For instance, in order to achieve 70dB SNR when sampling a 100MHz signal, the required aperture jitter is less than 500fs.

2.2.3 Op-Amp Open-Loop Gain

Figure 2-5 illustrates the AC equivalent incremental circuit model of the pipelined stage in Figure 2-2b. The reference buffers are assumed to have infinite BW for simplicity. C_1 is defined as

$$C_1 = \sum_{i=1}^{N} C_{1,i}. \tag{2.10}$$

Parasitic capacitance, C_p, is added to model the loading at the virtual ground node caused by parasitic routing capacitance and the op-amp input capacitance. The load

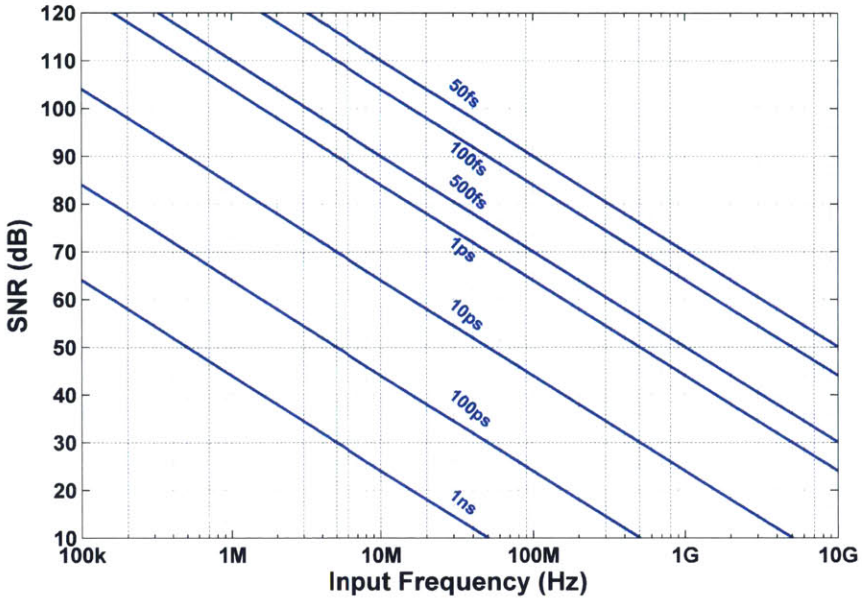


Figure 2-4: SNR degradation due to aperture jitter as a function of input frequency.

capacitance, C_L, is the sampling capacitance of the next stage.

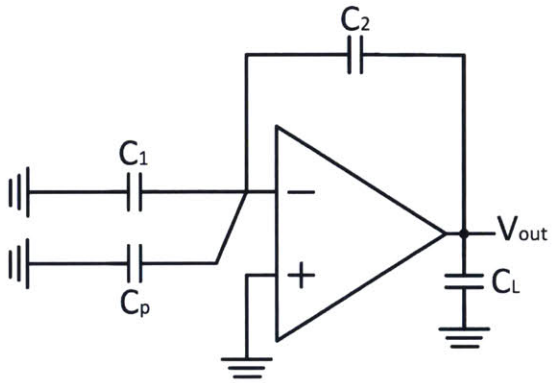


Figure 2-5: Equivalent incremental circuit of an MDAC with parasitic capacitance, C_p, loading the virtual ground node.

For a finite op-amp open-loop gain A, the circuit with signal gain G_s outputs

$$v_{OUT} = v_{IN} \frac{G_s}{1 + \frac{1}{A\beta}} \tag{2.11}$$

for a feedback factor β of the closed-loop system

$$\beta = \frac{C_2}{C_1 + C_2 + C_p}. \tag{2.12}$$

If the op-amp has infinite open-loop gain, then the ideal output is

$$v_{OUT}|_{ideal} = G_s v_{IN}. \tag{2.13}$$

Comparing Equation 2.11 to Equation 2.13, the error term is

$$\epsilon = \frac{1}{A\beta}. \tag{2.14}$$

The error is input-referred to obtain the required minimum open-loop gain. For a B_T-bit pipelined ADC resolving B_1 bits in the first stage, the following requirement must be met for $\frac{1}{4}$LSB accuracy:

$$\frac{1}{2^{B_T+2}} = \frac{1}{A\beta 2^{B_1}}. \tag{2.15}$$

For example, in a 12-bit pipelined ADC with $B_1 = 3$ and $\beta = \frac{1}{10}$, a minimum open-loop gain of 86.2dB is required. The effect of insufficient op-amp open-loop gain is illustrated in Figure 2-6. Missing codes are generated around the sub-ADC code transition boundaries. In reality, the op-amp is designed to have higher open-loop gain for margin since various other nonlinearities throughout the ADC degrade the overall performance.

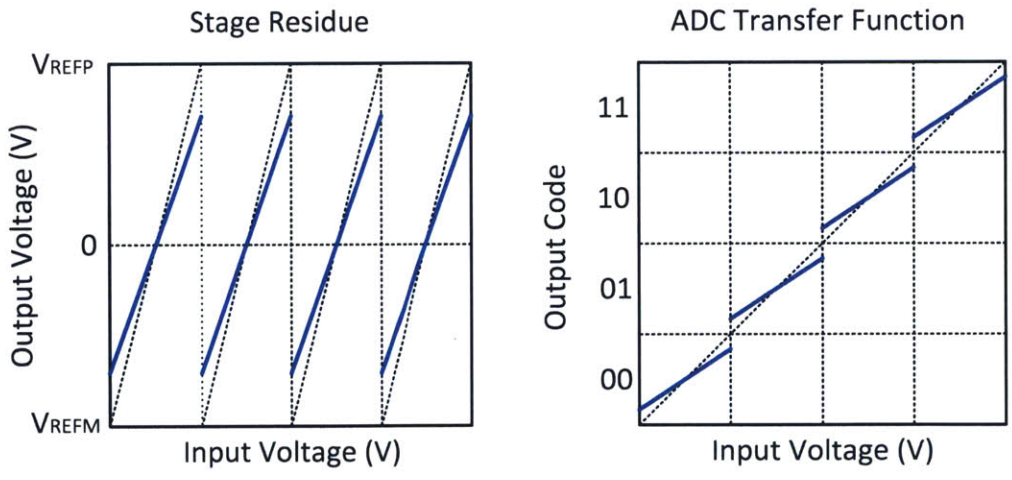


Figure 2-6: Effect of insufficient op-amp open-loop gain on the stage residue and the ADC transfer function.

For high op-amp open-loop gain, a multi-stage op-amp with nested Miller compensation may become necessary due to the low transistor intrinsic gain in advanced CMOS processes. A gain-boosted op-amp can also be employed. Unfortunately, these topologies require extra current to push the parasitic poles to higher frequencies for phase margin and are therefore not power efficient. Little can be done to improve β since it is largely fixed by the capacitive ratio set by C_1, C_2, and C_p. In the most optimistic ideal case with $C_p = 0$, the previous example with $B_1 = 3$ leads to $\beta = \frac{1}{8}$, while typical β would be $\frac{1}{10}$.

2.2.4 Op-Amp Bandwidth

In the previous example on the B_T-bit pipelined ADC resolving B_1 bits in the first stage, a single-pole closed-loop system with a $\frac{1}{4}$LSB settling accuracy has a required time constant

$$\tau < \frac{1}{2(B_T - B_1 + 2) f_s \ln 2}, \tag{2.16}$$

where f_s is the sampling frequency of the circuit. In Equation 2.16, the charge-transfer phase takes half of the clock period. This leads to the closed-loop bandwidth requirement of

$$f_{3dB} > \frac{(B_T - B_1 + 2) f_s \ln 2}{\pi}, \tag{2.17}$$

and the unity-gain frequency of the op-amp

$$f_u = \frac{f_{3dB}}{\beta}. \tag{2.18}$$

The required f_u is inversely proportional to the feedback factor. For a single-stage op-amp with transconductance g_m,

$$f_u = \frac{g_m}{2\pi \left(C_L + \dfrac{(C_1 + C_p) C_2}{C_1 + C_2 + C_p} \right)}. \tag{2.19}$$

For transconductance in square-law region, g_m is proportional to the square-root of the transistor width and current. Increasing the width and current of the op-amp input transistor improves f_u. Unfortunately, bigger transistor size adds more C_p and degrades β.

2.2.5 Input-Referred Thermal Noise

The thermal noise contribution from the sampling circuit, op-amp, and the reference buffers are detailed. Although the noise analysis for the sampling circuit and the op-amp is straightforward, the noise analysis for the reference buffer is particularly interesting since it is code-dependent. In the conventional design, the reference buffer noise is partially canceled depending on the sub-ADC code and the noise bandwidth is set by the op-amp bandwidth.

Sampled Thermal Noise

Capacitors are ideally and approximately noiseless, but resistors from the sampling switches add noise to the sampled values. As shown in Figure 2-7, the resistor adds white thermal noise, and the spectral noise density is expressed as

$$S_{n,R}(f) = 4kTR, \tag{2.20}$$

where k is the Boltzmann constant ($1.38 \times 10^{-23} J/K$) and T is the temperature expressed in Kelvin. The thermal noise is low-pass filtered by the RC circuit, and the transfer function from the noise source, $v_{n,R}$, to v_{out} is

$$H(s) = \frac{V_{out}}{V_{n,R}}(s) = \frac{1}{RCs+1}. \tag{2.21}$$

The output spectral noise density is given by

$$S_{n,out}(f) = S_{n,R}(f) \left| \frac{V_{out}}{V_{n,R}}(j2\pi f) \right|^2. \tag{2.22}$$

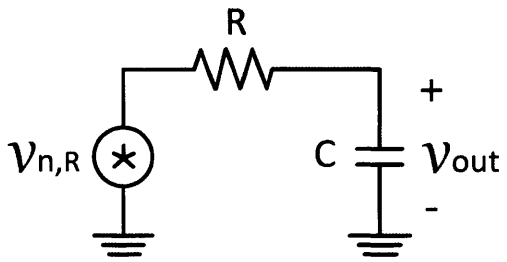


Figure 2-7: Sampled noise in the sampling circuit.

Integrating $S_{n,out}(f)$ over infinite bandwidth gives the total noise power at the output

$$P_{n,out} = \int_0^\infty S_{n,out}(f)\,\mathrm{d}f. \tag{2.23}$$

This can be simplified by integrating the spectral noise density $S_{n,out}(f)$ over the equivalent noise bandwidth $\frac{\pi}{2}f_0$, where

$$f_0 = \frac{1}{2\pi RC}. \tag{2.24}$$

Solving 2.23,

$$P_{n,out} = S_{n,out}(f)\frac{\pi}{2}f_0 = \frac{KT}{C}. \tag{2.25}$$

The total output noise power is determined by the size of the sampling capacitance regardless of the resistance value. This is because the spectral noise density is proportional to the resistance whereas the noise bandwidth is inversely proportional to the resistance. The inverse relationship between the spectral noise density and noise bandwidth cancel out when the noise is integrated, and the total noise power is eventually determined only by the capacitance value.

Op-Amp Noise

The power spectral density of the input-referred op-amp noise is

$$S_{n,oa}(f) = \frac{4kT\gamma n_f(2g_{mp,oa} + 2g_{mn,oa})}{g_{mn,oa}^2} \tag{2.26}$$

as derived in [33] where $g_{mp,oa}$ and $g_{mn,oa}$ are the transconductance of the PMOS and NMOS device, respectively, and γ, typically $\frac{2}{3}$ in strong inversion, is a coefficient dependent on the region of operation. An NMOS transistor input pair with PMOS current source load is assumed. To achieve high open-loop gain, more complicated configurations, such as two-stage or folded cascode are often implemented. The noise from the added circuitry is considered by the noise multiplication factor, n_f. If the op-amp is simplified to a single-pole model without internal parasitics, the transfer function of the closed-loop response is

$$H(s) = \frac{1}{\beta\left(1 + \frac{s}{BW}\right)} \tag{2.27}$$

with closed-loop bandwidth

$$BW = \frac{g_m}{C_T}\beta, \tag{2.28}$$

where the total loading capacitance, C_T, of the op-amp is

$$C_T = \frac{(C_1 + C_p)C_2}{C_1 + C_2 + C_p} + C_L. \tag{2.29}$$

Given $S_{n,oa}(s)$ and $H(s)$, the total integrated noise power at the output is obtained by integration:

$$\overline{v_{n,oa,out}^2} = \int_0^\infty S_{n,oa}(f)|H(j2\pi f)|^2 \,\mathrm{d}f \tag{2.30}$$

$$= S_{n,oa}(f)\frac{BW}{4}\frac{1}{\beta^2}. \tag{2.31}$$

The output-referred op-amp noise power is then referred back to the system input:

$$\overline{v_{n,oa,in}^2} = \frac{\overline{v_{n,oa,out}^2}}{G_s^2} \tag{2.32}$$

$$= \frac{4kT\gamma n_f(2g_{mp,oa} + 2g_{mn,oa})}{g_{mn,oa}^2}\frac{BW}{4}\frac{1}{\beta^2}\frac{1}{G_s^2}. \tag{2.33}$$

Reference Buffer Noise

Next, the noise contribution from both the PMOS and NMOS reference buffers must be considered as well. A simple source follower in Figure 2-8 is considered as an example. For each source follower, the noise is dominated by a pair of transistors with noise current

$$\overline{i_{p,1}^2}=\overline{i_{p,2}^2} = 4kT\gamma g_{mp,b} \tag{2.34}$$

$$\overline{i_{n,1}^2}=\overline{i_{n,2}^2} = 4kT\gamma g_{mn,b} \tag{2.35}$$

where $g_{mp,b}$ and $g_{mn,b}$ are the transconductance of the PMOS and NMOS device, respectively. The noise is referred back to the PMOS input transistor in the PMOS reference buffer and the NMOS input transistor in the NMOS reference buffer:

$$S_{n,bp}(f)=\frac{8kT\gamma}{g_{mp,b}} \tag{2.36}$$

$$S_{n,bn}(f)=\frac{8kT\gamma}{g_{mn,b}}. \tag{2.37}$$

The input-referred spectral noise density of the PMOS and NMOS reference buffers are $S_{n,bp}(f)$ and $S_{n,bn}(f)$, respectively.

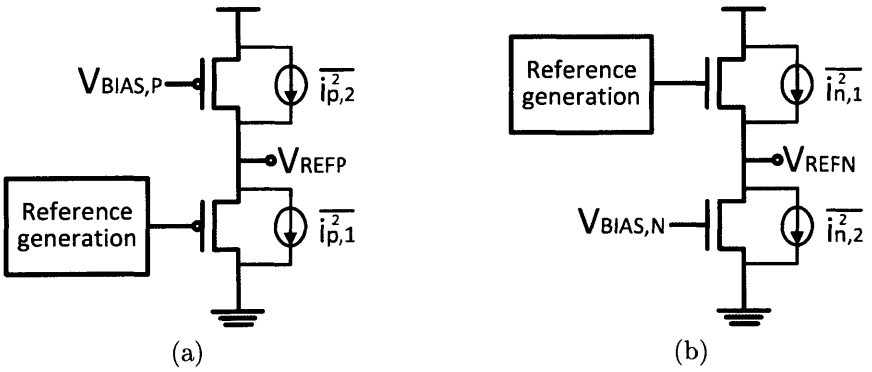


Figure 2-8: (a) PMOS and (b) NMOS source follower buffer for reference driving.

In the conventional fully differential configuration, the noise from the reference buffer is partially canceled depending on the sub-ADC code. For example, if the

input signal corresponds to a maximum sub-ADC code, $k = N$, then the PMOS reference buffer drives all the $C_{1,i+}$ unit capacitors and the NMOS reference buffer drives all the $C_{1,i-}$ unit capacitors. The reference buffer connection configuration is shown in Figure 2-9a. The noise voltage referred to the MDAC output, $v_{n,b,out}$, for this case is

$$\begin{aligned} v_{n,b,out}(N) &= v_{n,b,out+}(N) - v_{n,b,out-}(N) \\ &= -\frac{\sum_{i=1}^{N} C_{1,i+}}{C_2} v_{n,bp} + \frac{\sum_{i=1}^{N} C_{1,i-}}{C_2} v_{n,bn}, \end{aligned} \tag{2.38}$$

where $v_{n,bp}$ and $v_{n,bn}$ are the input-referred noise voltages of the PMOS and NMOS reference buffers, respectively. Similarly, if the input signal corresponds to a minimum code, $k = 0$, then the NMOS reference buffer drives all the $C_{1,i+}$ unit capacitors and the PMOS reference buffer drives all the $C_{1,i-}$ unit capacitors, resulting in an output-referred noise voltage

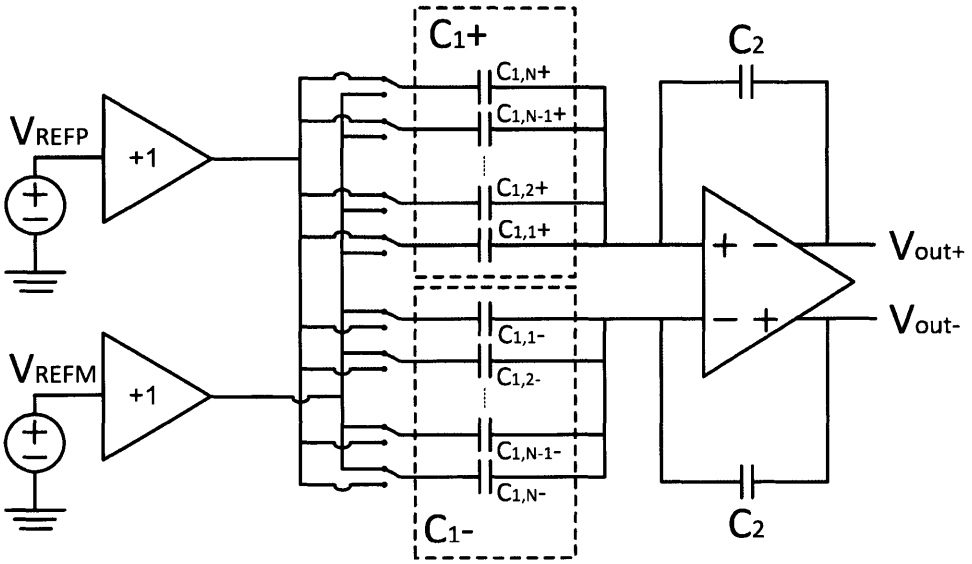
$$v_{n,b,out}(0) = -\frac{\sum_{i=1}^{N} C_{1,i+}}{C_2} v_{n,bn} + \frac{\sum_{i=1}^{N} C_{1,i-}}{C_2} v_{n,bp}. \tag{2.39}$$

On the other hand, if the input signal corresponds to a sub-ADC code of $N - 1$, then the PMOS reference buffer drives $N - 1$ $C_{1,i+}$ unit capacitors and a single $C_{1,i-}$ unit capacitor. The remaining single $C_{1,i+}$ unit capacitor and $N - 1$ $C_{1,i-}$ unit capacitors are driven by the NMOS reference buffer. Then the output-referred noise voltage is reduced to

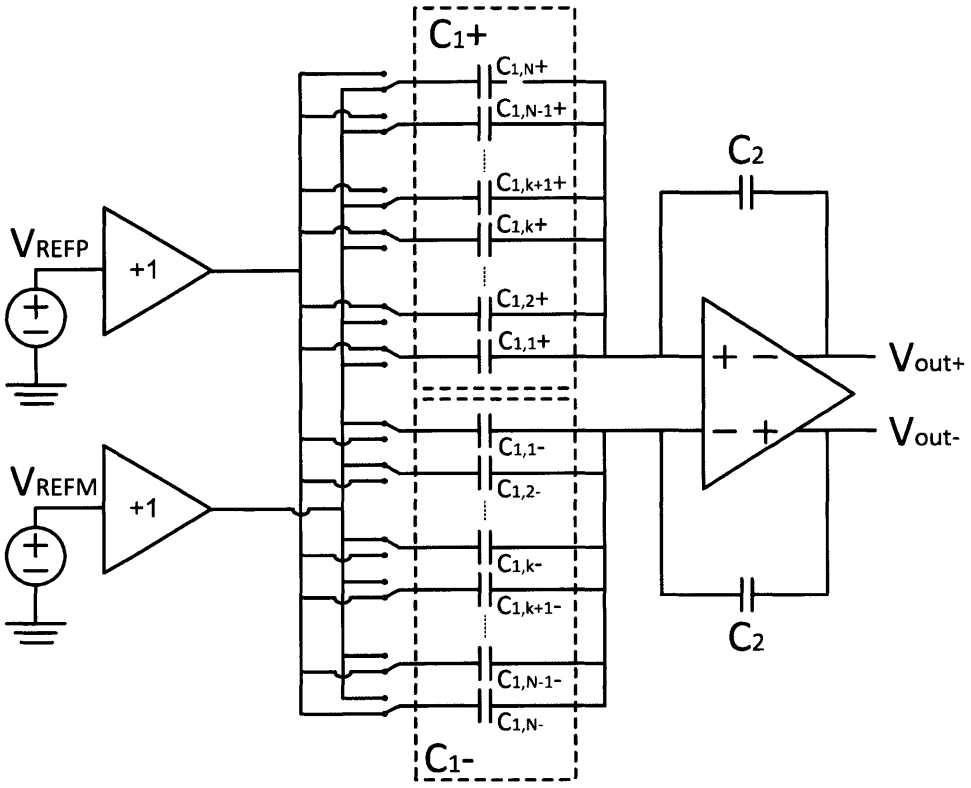
$$\begin{aligned} v_{n,b,out}(N-1) = &-\frac{\sum_{i=1}^{N-1} C_{1,i+}}{C_2} v_{n,bp} - \frac{\sum_{i=1}^{1} C_{1,i+}}{C_2} v_{n,bn} \\ &- \left(-\frac{\sum_{i=1}^{N-1} C_{1,i-}}{C_2} v_{n,bn} - \frac{\sum_{i=1}^{1} C_{1,i-}}{C_2} v_{n,bp} \right). \end{aligned} \tag{2.40}$$

For equivalent $C_{1,i+}$ and $C_{1,i-}$ unit capacitors

$$v_{n,b,out}(N-1) = -\frac{\sum_{i=1}^{N-2} C_{1,i}}{C_2} v_{n,bp} + \frac{\sum_{i=1}^{N-2} C_{1,i}}{C_2} v_{n,bn}. \tag{2.41}$$



(a)



(b)

Figure 2-9: Reference buffer connection configuration for (a) maximum sub-ADC code $k = N$ and (b) mid-code $k = \frac{N}{2}$.

Intuitively, if the input signal corresponds to the mid-code, $k = \frac{N}{2}$, as shown in Figure 2-9b, the PMOS and NMOS reference buffers each drive half of the C_1 unit capacitors on the positive and negative virtual ground node, and the reference buffer noise is differentially canceled at the output:

$$\begin{aligned} v_{n,b,out}\left(\frac{N}{2}\right) = & -\frac{\sum_{i=1}^{\frac{N}{2}} C_{1,i+}}{C_2} v_{n,bp} - \frac{\sum_{i=1}^{\frac{N}{2}} C_{1,i+}}{C_2} v_{n,bn} \\ & - \left(-\frac{\sum_{i=1}^{\frac{N}{2}} C_{1,i-}}{C_2} v_{n,bn} - \frac{\sum_{i=1}^{\frac{N}{2}} C_{1,i-}}{C_2} v_{n,bp} \right) \\ = & 0. \end{aligned} \tag{2.42}$$

The code-dependent output-referred reference buffer noise voltage is illustrated in Figure 2-10.

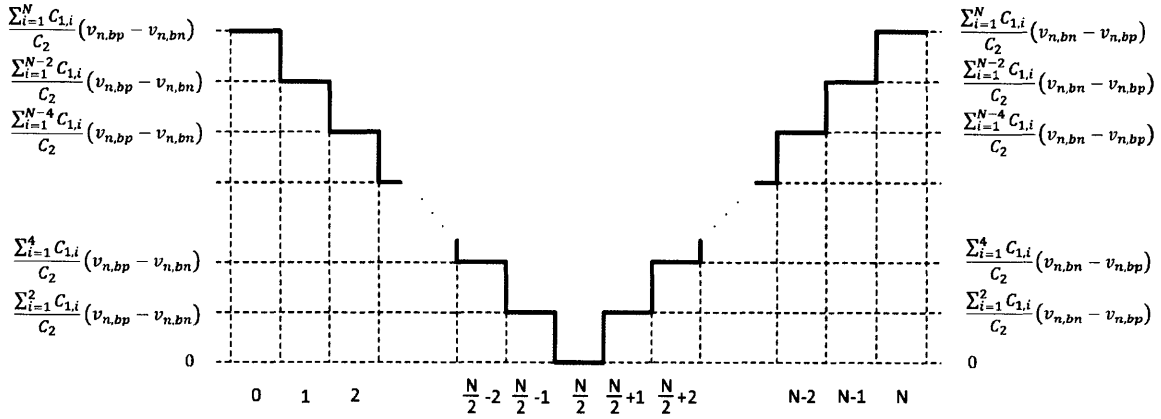


Figure 2-10: Reference buffer noise voltage referred to the MDAC output.

The noise sources from each of the reference buffers are uncorrelated and therefore the noise power adds. Since the low feedback factor of the op-amp limits the closed-loop bandwidth, the bandwidth for the noise power integration is set by Equation 2.28 and

$$\overline{v_{n,b,out}^2}(k) = \left(S_{n,bp}(f) + S_{n,bn}(f)\right) \left(\frac{\sum_{i=1}^{|N-2k|} C_{1,i}}{C_2}\right)^2 \frac{BW}{4}. \tag{2.43}$$

The code-dependent output-referred reference buffer noise power is shown in Figure 2-11. The noise power is highest near the maximum and minimum sub-ADC codes and

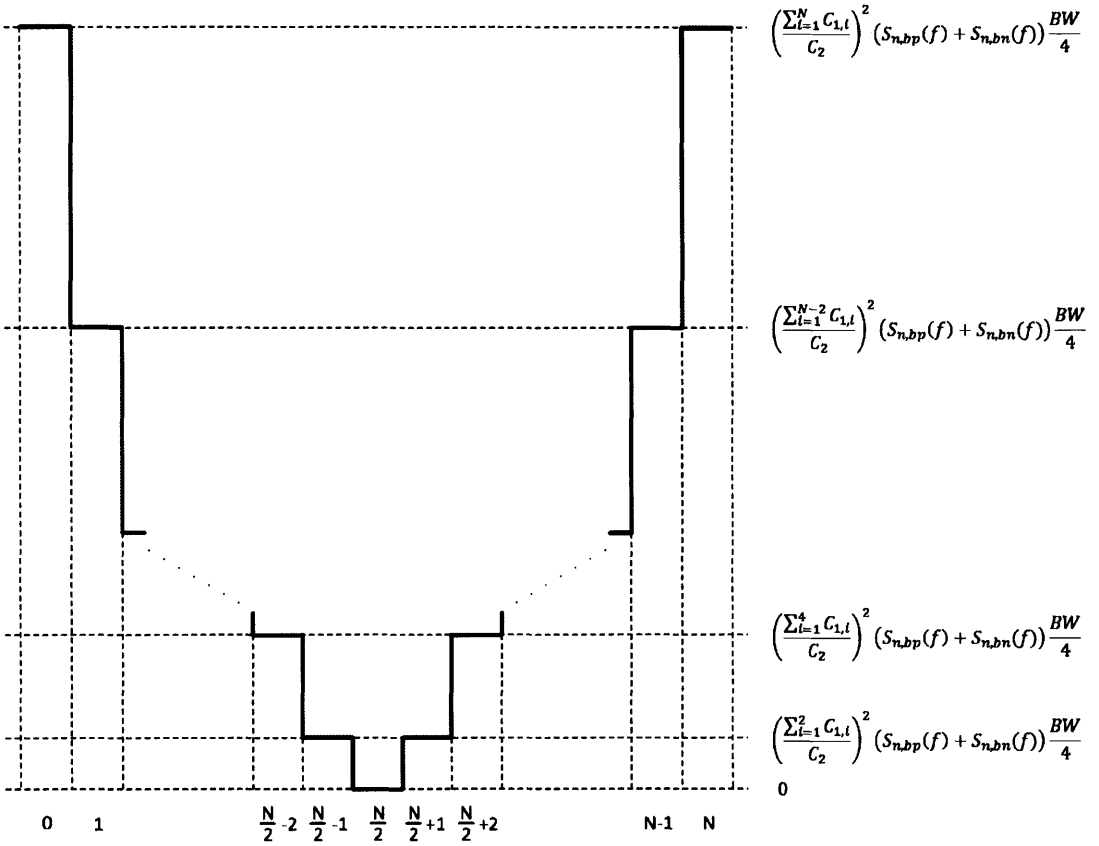


Figure 2-11: Reference buffer spectral noise power referred to the MDAC output.

is canceled differentially as the input signal approaches the mid-code.

For a random input signal, it can be assumed that the probability for each sub-ADC code is uniformly distributed and the mean square output noise power is

$$\overline{v_{n,b,out}^2} = \Big(S_{n,bp}(f) + S_{n,bn}(f)\Big)\frac{\sum_{k=0}^{N}\left(\frac{\sum_{i=1}^{|N-2k|} C_{1,i}}{C_2}\right)^2}{N+1}\frac{BW}{4}. \tag{2.44}$$

If the sub-ADC has more than a few bits of resolution and if C_2 is twice the capacitance of $C_{1,i}$ unit capacitor as in the implemented ADC in Chapter 4, then the output noise power can be approximated:

$$\begin{aligned}\overline{v_{n,b,out}^2} &= \left(\frac{1}{N}\int_{-\frac{N}{2}}^{\frac{N}{2}}\Big(S_{n,bp}(f) + S_{n,bn}(f)\Big)x^2\mathrm{d}x\right)\frac{BW}{4} \\ &= \Big(S_{n,bp}(f) + S_{n,bn}(f)\Big)\frac{N^2}{12}\frac{BW}{4}\end{aligned} \tag{2.45}$$

The output-referred reference buffer noise is referred back to the MDAC input as

$$\overline{v_{n,b,in}^2} = \frac{\overline{v_{n,b,out}^2}}{G_s^2} \tag{2.46}$$

$$= \left(\frac{8kT\gamma}{g_{mp,b}} + \frac{8kT\gamma}{g_{mn,b}} \right) \frac{N^2}{12} \frac{BW}{4} \frac{1}{G_s^2}. \tag{2.47}$$

2.2.6 MDAC Capacitor Mismatch

Process variation results in mismatch in capacitor values. In Equation 2.2, the effective signal gain, $G_{s,eff}$, deviates from its ideal value if

$$G_{s,eff} = \frac{\sum_{i=1}^{N} C_{1,i} + C_2}{C_2} \neq G_s. \tag{2.48}$$

Missing codes are present with negative differential nonlinearity (DNL) if $G_{s,eff} < G_s$ and wide codes are present with positive DNL if $G_{s,eff} > G_s$.

Capacitor mismatch between $C_{1,i}$ also results in DAC nonlinearity which introduces inconsistent residue transition magnitude in sub-ADC code boundaries. Ideally, the same reference voltage must be subtracted or added whenever the sub-ADC code changes. This leads to constant voltage jump in the MDAC residue at each sub-ADC bit-decision transition. DAC nonlinearity causes a varying residue voltage jump for

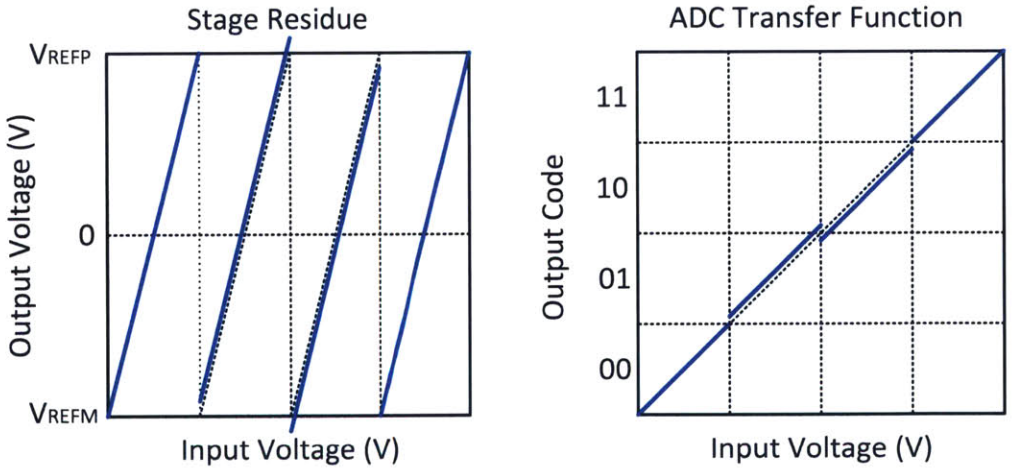


Figure 2-12: Effect of capacitor mismatch in inconsistent residue transition magnitude in sub-ADC code boundary and the ADC transfer function.

each output code of the sub-ADC in Figure 2-12.

The capacitance matching can be improved with increased area. Therefore, the capacitance size is determined by not only the thermal noise requirement, but the linearity as well. Symmetric layout using unit size capacitors and dummy capacitors is standard practice to improve the matching. Digital calibration can also improve the linearity without adding significant overhead [34, 35].

2.2.7 Sub-ADC

In Figure 2-13, a generic B-bit flash ADC is shown for the sub-ADC. The resistor ladder generates the reference voltages for the comparator array. The number of comparators determine the resolution of the flash ADC. In its simplest form, $2^B - 1$ comparators are needed for a B-bit resolution. The output of the comparators form a thermometer code representation of the input.

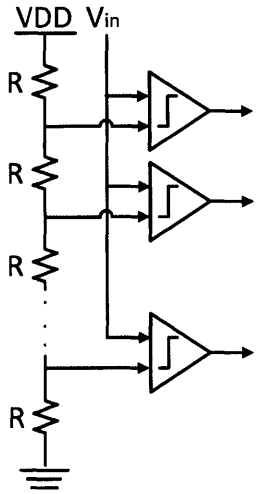


Figure 2-13: Flash ADC example.

In a pipelined ADC, the over-range scheme ensures that a certain magnitude of comparator offsets can be tolerated. However, attention is needed in stages that have high signal gain and resolve a high number of bits. For example, consider an over-range that extends the MDAC ideal output range by an additional $\pm$100mV. For an MDAC with a signal gain of 8, the over-range can handle a maximum comparator offset of 12.5mV. The standard deviation of the comparator offset must be less than

4.2mV such that a 3σ deviation is less than the maximum correctable offset; if the offset is too large, it results in clipping in the residue. Higher signal gain in the MDAC leads to an even more stringent maximum tolerable comparator offset requirement. Unfortunately, large over-range is costly in advanced CMOS due to the low supply voltages. The MDAC ideal residue range can be reduced to accomodate bigger comparator offset, but the SNR is then lower due to the smaller signal swing unless the noise voltage is decreased accordingly. Pre-amplifiers can be placed before the comparators but at a cost of additional power. Pre-amplifiers also have the benefit of mitigating kickback noise from the latch.

If a dedicated sample-and-hold (S/H) circuit is not used at the ADC front-end, dynamic offsets must be considered as well. The S/H circuit is used to hold the sampled signal for the first pipelined stage, but consumes a significant amount of power. It also adds substantial noise and distortion, while the noise generated from the following stages are input-referred without any attenuation. For a fixed SNR, the capacitor size is doubled if a S/H circuit is employed with the assumption that the noise and power consumption budget is equivalent in the S/H circuit and the rest of the ADC. The total power dissipation is increased by a factor of four because of the added S/H circuit and the more stringent noise requirement from the pipelined stages. Therefore, a dedicated front-end circuit is typically avoided by integrating the S/H operation into the first stage MDAC [36, 37]. In this approach, however, the sampled voltages in the MDAC and the sub-ADC may be different due to the mismatch in the sampling network bandwidth and the clock skew caused by unbalanced routing and process variations in the sampling switches. The maximum error in the sampled voltage can be approximated as

$$v_{ERR,max} \approx \omega_{max} V_a \Delta t, \tag{2.49}$$

with effective timing mismatch

$$\Delta t = \Delta t_{clk} + \Delta \tau. \tag{2.50}$$

Here, ω_{max} is the highest input signal frequency, V_a is the signal amplitude, Δt_{clk} is the clock skew, and $\Delta\tau$ is the sampling network time-constant mismatch between the MDAC and the sub-ADC. The effects are illustrated in Figure 2-14, where τ_{MDAC} and $\tau_{sub-ADC}$ are the time constants of the two sampling networks. At high input frequencies and large input signals, the two sampling networks might sample the signal with large difference. Again, this is aggravated in stages with high MDAC signal gain since the dynamic offset takes up a portion of the over-range. For example, for f_{in} = 100MHz, V_a = 1V, and Δt = 10ps, the difference in the sampled voltage is v_{ERR} = 6.28mV. If the signal gain in the MDAC is 8, then a minimum of additional 50mV in over-range is required.

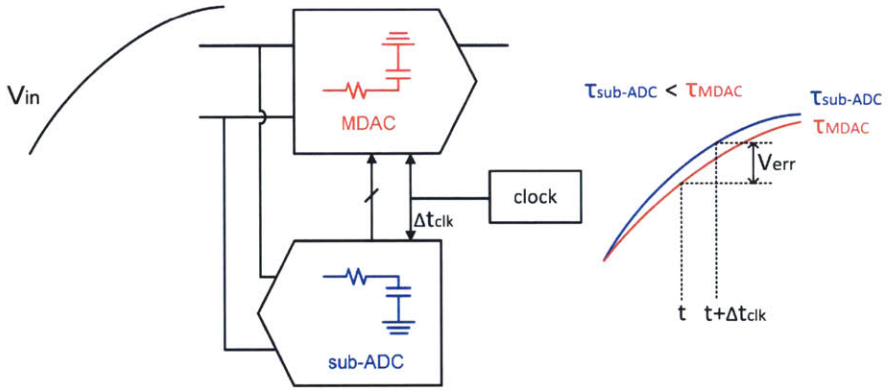


Figure 2-14: Sampling mismatch between the MDAC and the sub-ADC.

Chapter 3

Virtual Ground Reference Buffer Technique

This chapter presents the proposed VGRB technique [38]. The technique improves the feedback factor of the op-amp without affecting the signal gain. First, the concept is explained assuming no parasitic capacitance, and the performance is compared with that of the conventional circuit. Then, an AC equivalent incremental circuit model and its corresponding block diagram is used to analyze the feedback factor and the noise transfer function of the op-amp and the buffer. The analysis includes the effect of the buffer gain and the parasitic capacitance on the ADC performance. The chapter also details the effect of reference voltage variations considering the multiple positive and negative reference voltages that are generated in this technique.

3.1 Bootstrapping Action by the Virtual Ground Reference Buffer

The proposed VGRB technique in its charge-transfer phase is shown in Figure 3-1. The sampling phase is identical to that of the conventional scheme in Figure 2-2a. In the charge-transfer phase, similarly to the conventional circuit, C_2 flips around the op-amp and C_1 is driven by either the positive or negative reference voltage. Here,

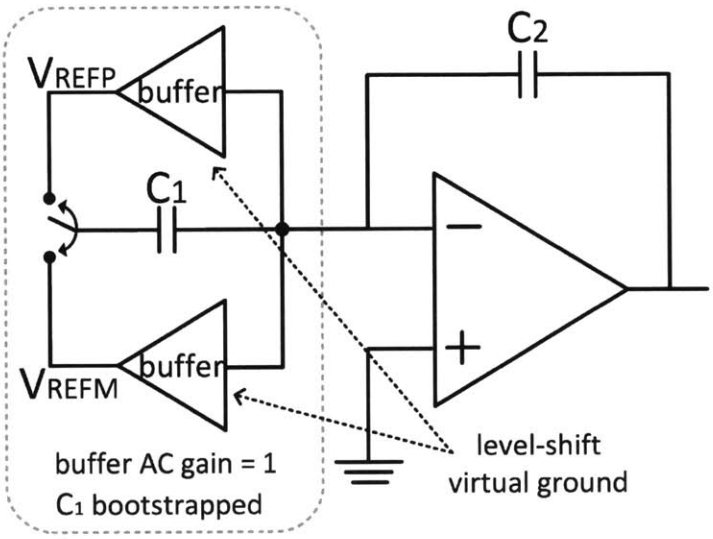


Figure 3-1: Proposed VGRB technique applied to a switched-capacitor circuit in the charge-transfer phase.

however, the reference voltages are referenced to the virtual ground node instead of the system ground, and they are generated by level-shifting the virtual ground potential.

A variety of circuits, such as a simple source follower, can be used as the level-shifting buffer. For example, a PMOS source follower generates V_{REFP} by level-shifting the virtual ground potential up, and an NMOS source follower generates V_{REFM} by level-shifting the virtual ground potential down. The output voltage of the circuit is identical to that of the conventional circuit once the signals settle.

The benefit of this technique is revealed in the AC equivalent incremental circuit model in Figure 3-2. Assuming an ideal buffer for simplicity, any change in the virtual ground node voltage is reflected at the output of the buffer, effectively bootstrapping C_1 away. Therefore, C_1 is removed from the feedback network of the op-amp, resulting in a unity feedback factor independent of the signal gain. This is in contrast to the conventional circuit, where the feedback factor β is the inverse of the signal gain G_s. In the proposed technique, that constraint no longer applies and both high signal gain and unity feedback factor can be achieved.

The bootstrapping action can also be explained in terms of Miller capacitance.

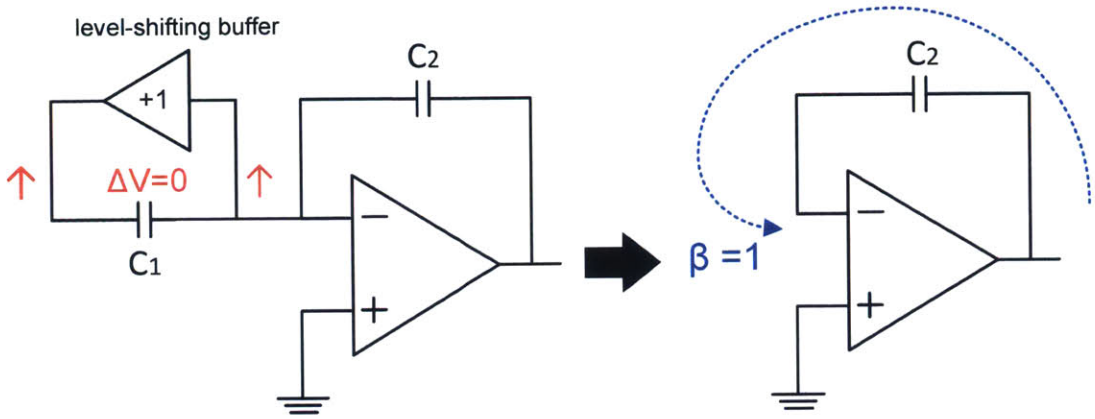


Figure 3-2: The AC equivalent incremental circuit model of the VGRB technique circuit in the charge-transfer phase.

For a buffer gain of G_b, the impedance looking into bootstrapped C_1 is

$$Z = \frac{1}{sC_1(1 - G_b)}. \tag{3.1}$$

For a unit-gain and positive polarity, $G_b = 1$, the C_1 capacitance vanishes and input impedance is $Z = \infty$, resulting in an ideal unity feedback factor regardless of the signal gain.

The performance of the VGRB technique is compared with that of the conventional circuit, both without parasitic capacitance, in Table 3.1. In the conventional circuit, the signal gain G_s is determined by the ratio between C_1 and C_2. For example, in a typical 4-bit/stage ADC, C_1 is 7 times C_2, and G_s is 8. High signal gain corresponds to resolving a large number of bits in the corresponding stage. The feedback factor, β, of the circuit is the inverse of the signal gain in the conventional circuit. Therefore, for G_s of 8, β is $\frac{1}{8}$. The closed-loop bandwidth is given by βf_u where f_u is the unity-gain bandwidth. Since the signal gain is typically much larger than unity, the unity-gain bandwidth of the op-amp must be much higher than the closed-loop bandwidth required for settling. For given sampling capacitance of the subsequent stage, correspondingly high transconductance is required in the op-amp, thus resulting in high power consumption. In addition, the signal gain is equal to the op-amp noise gain, thus the integrated input-referred noise of the switched-capacitor circuit is equivalent to the input-referred noise of the op-amp integrated over the closed-loop

bandwidth. High op-amp open-loop gain is required for small charge-transfer error.

	Conventional	Proposed
Gs signal gain	$1+\frac{C_1}{C_2}$	$1+\frac{C_1}{C_2}$
β feedback factor	$\frac{C_2}{C_1+C_2}$	1
Closed-loop bandwidth	$\frac{f_u}{G_s}$	f_u
Input-referred noise density	$S_{n,oa}(f)^{**}$	$\frac{S_{n,oa}(f)^{***}}{G_s{}^2}$
Charge-transfer error	$\frac{G_s}{A^*}$	$\frac{1}{A}$

* op-amp open-loop gain
** op-amp input-referred spectral noise density, noise BW = f_u/G_s
*** op-amp input-referred spectral noise density, noise BW = f_u

Table 3.1: Performance comparison of a switched-capacitor circuit based on the conventional approach and the VGRB technique assuming no parasitic capacitance.

In the proposed circuit, the signal gain G_s is identical to that of the conventional circuit. However, the feedback factor β is unity independent of the signal gain. In Equation 2.18, substituting $\beta = 1$ gives $f_{3dB} = f_u$. Thus, the closed-loop bandwidth is higher by a factor of the signal gain compared with that of the conventional circuit. This translates to either lower op-amp power or faster circuit operation. In Figure 3-3, for an op-amp input-referred spectral noise density $S_{n,oa}(f)$, the spectral noise density at the output is

$$S_{n,oa,out}(f) = \frac{S_{n,oa}(f)}{\beta^2}. \tag{3.2}$$

Then, the spectral noise density is referred back to the ADC input,

$$S_{n,oa,in}(f) = \frac{S_{n,oa,out}(f)}{G_s^2} = \frac{S_{n,oa}(f)}{\beta^2 G_s^2}. \tag{3.3}$$

Since $\beta = 1$,

$$S_{n,oa,in}(f) = \frac{S_{n,oa}(f)}{G_s^2}. \tag{3.4}$$

The op-amp noise gain is unity and the noise power is reduced by a factor of the signal gain compared with that of the conventional circuit when referred to the input. This is a major advantage since reducing input-referred noise requires significant power consumption. In addition, the op-amp open-loop gain and offset requirements are reduced by a factor of the signal gain. This is due to the unity feedback factor in Equation 2.14. Therefore, all key performance parameters are improved by a factor of the signal gain.

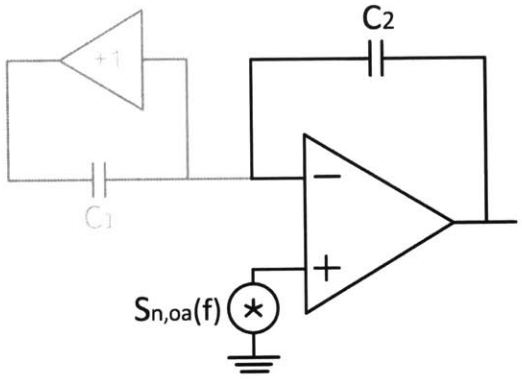


Figure 3-3: VGRB technique with op-amp input-referred spectral noise density $S_{n,oa}(f)$.

For a fair comparison, however, bandwidth, noise, and power consumption of the buffers must be considered. In the presented ADC, the buffers replace existing reference buffers, thus incurring insignificant penalty; conventional circuits require on-chip reference buffers in high-speed and high-resolution ADCs as mentioned in Section 2.1. More detailed analysis of the buffer bandwidth and noise is presented in Section 3.2.

It is important to note that the benefits are obtained without affecting the signal gain. More importantly, the higher the ADC resolution, the bigger is the performance improvement that can be obtained since high resolution ADCs typically have large signal gain and low feedback factor. The performance is improved by breaking away from the conventional inverse relationship between the signal gain and the feedback factor.

3.1.1 Effect of Parasitic Capacitance

To be more realistic, the effect of parasitic capacitance must also be considered as shown in Figure 3-4. The actual improvement in the feedback factor depends on the value of the parasitic capacitance, C_p, at the virtual ground node. There are four sources of C_p: the finite gain of the buffer, the buffer input capacitance $C_{i,b}$, the op-amp input capacitance $C_{i,oa}$, and routing capacitance C_w. In practice, the incremental gain of the source follower buffer is typically less than unity and C_1 is not completely bootstrapped away; a portion of C_1 loads the virtual ground node. If the buffer gain is 0.9 instead of unity, the buffer bootstraps away only 90% of C_1 capacitance, and the remaining 10% of C_1 effectively shows up at the virtual ground node. The source follower input capacitance is dominated by the gate-to-drain capacitance C_{gd} because the gate-to-source capacitance C_{gs} is bootstrapped away and is not a major source of parasitic capacitance. The op-amp input capacitance is another source of parasitic capacitance, and it affects both conventional and proposed designs. In the proposed scheme, for the same op-amp noise and bandwidth requirements, the op-amp requires much smaller input transistors, and thus has much smaller $C_{i,oa}$. The routing of the virtual ground node contributes parasitic capacitance in the conventional circuit. In the proposed scheme, it can be mostly bootstrapped away by the buffers as shown later in the implementation in Chapter 4.

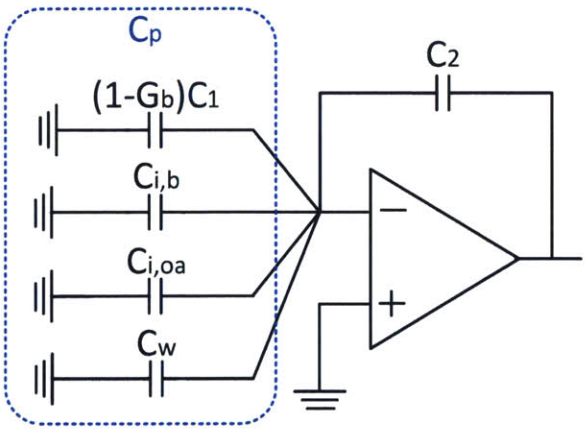


Figure 3-4: Sources of the parasitic capacitance that loads the virtual ground node and degrades op-amp feedback factor.

3.1.2 Performance Advantage in Scaled CMOS

A notable performance advantage of the VGRB technique in scaled CMOS is the reduced noise power. The significance of the advantage in noise power reduction is evident in advanced processing nodes. For a fixed device transconductance, CMOS scaling does not significantly impact absolute thermal or shot noise floor, which is inversely proportional to the device transconductance [39]. However, the supply voltage reduces signal swing and therefore the SNR as well. The SNR degradation is a prominent issue that analog circuits must address. In [40], it is shown that the relative noise floor, defined as

$$n_r = -(\text{SNR} + 10\log_{10}\text{BW}) \tag{3.5}$$

for Nyquist bandwidth BW, increases with CMOS scaling. While new CMOS technologies enable higher bandwidth, this is offset by the degradation in SNR, leading to higher n_r. Therefore, high-resolution ADC implementations are becoming less prevalent in scaled CMOS, as noted previously in Figure 1-3b.

The VGRB technique reduces the noise power contribution from the op-amp referred to the switched-capacitor circuit input by a factor of the feedback factor improvement. In the implemented ADC in Chapter 4, the feedback factor is improved by a factor of three compared with the conventional circuit, and therefore the noise power from the op-amp is reduced by a factor of three even with the increased bandwidth. The VGRB technique has the advantage of regaining SNR in low supply voltages that continue to decrease with CMOS scaling. In addition, the benefit is obtained without penalty in power, whereas conventional circuits trade power-efficiency in high-resolution ADCs to reduce the noise floor.

3.1.3 Multi-bit MDAC Implementation

In a multi-bit differential implementation as shown in Figure 3-5, C_1 consists of an array of N unit capacitors and the switches configure the connection between the level-shifting buffers and the C_1 capacitor array. The switched-capacitor circuit has four

level-shifting buffers. The positive and negative reference voltages generated by level-shifting the positive virtual ground potential are V_{REFP1} and V_{REFM1}, respectively. Likewise, the positive and negative reference voltages generated by level-shifting the negative virtual ground potential are V_{REFP2} and V_{REFM2}, respectively.

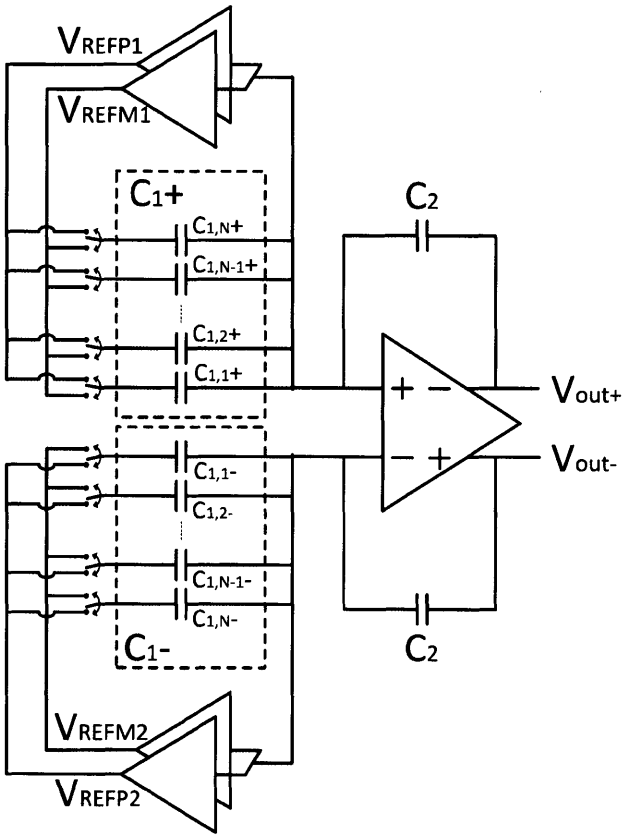


Figure 3-5: A multi-bit differential switched-capacitor circuit with VGRBs in the charge-transfer phase.

3.1.4 Noise Contribution from the Level-Shifting Buffers

In the VGRB technique, each level-shifting buffer contributes noise to the output. In the connection configuration of the level-shifting buffers and the capacitor array in Figure 3-6, k is the number of comparators that output a high decision-bit in the sub-ADC among the N total comparators; $k = N$ at maximum input voltage and $k = 0$ at minimum input voltage. The code-dependent output-referred noise power contribution from the PMOS level-shifting buffer on the positive virtual ground node

with input-referred spectral noise density $S_{n,bp1}(f)$ can be shown to be

$$\overline{v^2_{n,bp1,out}}(k) = \left(\frac{\sum_{i=1}^{k} C_{1,i+}}{C_2}\right)^2 S_{n,bp1}(f)\frac{BW}{4}, \tag{3.6}$$

and similarly, the code-dependent output-referred noise power contribution from the NMOS level-shifting buffer on the positive virtual ground node with input-referred spectral noise density $S_{n,bn1}(f)$ is

$$\overline{v^2_{n,bn1,out}}(k) = \left(\frac{\sum_{i=1}^{|N-k|} C_{1,i+}}{C_2}\right)^2 S_{n,bn1}(f)\frac{BW}{4}, \tag{3.7}$$

The code-dependent output-referred noise power contribution from the level-shifting buffers on the negative virtual ground node is also derived to be

$$\overline{v^2_{n,bp2,out}}(k) = \left(\frac{\sum_{i=1}^{|N-k|} C_{1,i-}}{C_2}\right)^2 S_{n,bp2}(f)\frac{BW}{4} \tag{3.8}$$

$$\overline{v^2_{n,bn2,out}}(k) = \left(\frac{\sum_{i=1}^{k} C_{1,i-}}{C_2}\right)^2 S_{n,bn2}(f)\frac{BW}{4}. \tag{3.9}$$

Here, $\overline{v^2_{n,bp2,out}}(k)$ and $\overline{v^2_{n,bn2,out}}(k)$ are the code-dependent output-referred noise power from the PMOS level-shifting buffer with input-referred spectral noise density $S_{n,bp2}(f)$ and NMOS level-shifting buffer with input-referred spectral noise density $S_{n,bn2}(f)$, respectively, on the negative virtual ground node.

The total output-referred noise power is the sum of the noise contribution from all four level-shifting buffers.

$$\overline{v^2_{n,b,out}}(k) = \overline{v^2_{n,bp1,out}}(k) + \overline{v^2_{n,bn1,out}}(k) + \overline{v^2_{n,bp2,out}}(k) + \overline{v^2_{n,bn2,out}}(k) \tag{3.10}$$

For a random input signal, it can be assumed that the probability for each sub-ADC code is uniformly distributed and the mean square output noise power is

$$\overline{v^2_{n,b,out}} = \frac{\sum_{k=0}^{N} \overline{v^2_{n,b,out}}(k)}{N+1}. \tag{3.11}$$

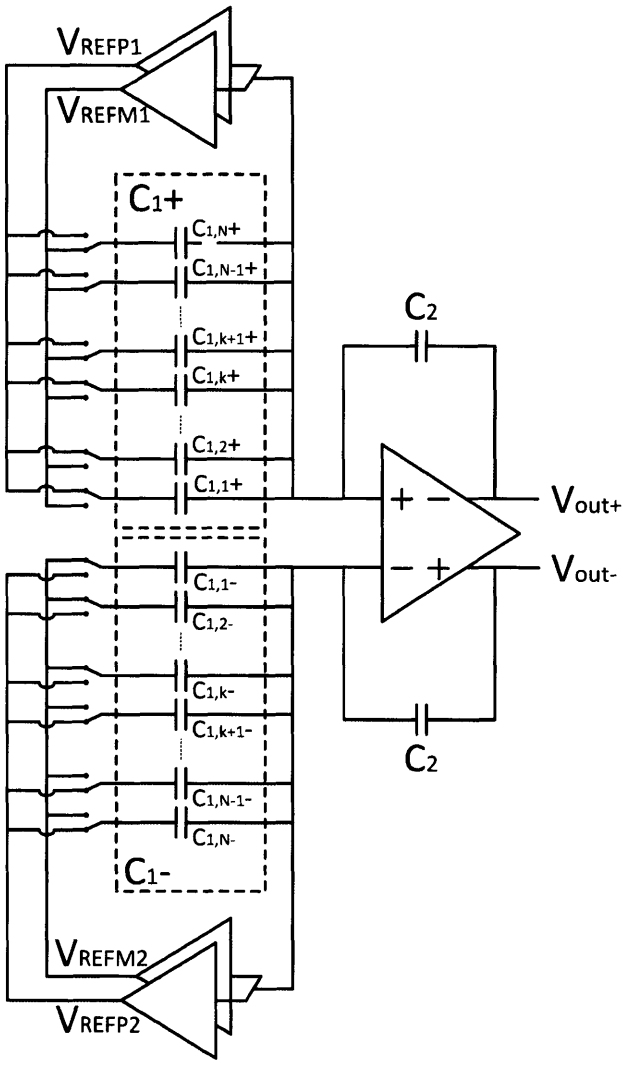


Figure 3-6: Configuration of the level-shifting buffers and capacitor array with k high decision-bits from the sub-ADC.

If the sub-ADC has reasonably high resolution and if C_2 is twice the capacitance of the $C_{1,i}$ unit capacitor, it can be approximated

$$\begin{aligned}\overline{v_{n,b,out}^2} &= S_{n,b}(f)\left(\frac{2}{N}\int_{-\frac{N}{4}}^{\frac{N}{4}}\left(x+\frac{N}{4}\right)^2 \mathrm{d}x\right)\frac{BW}{4} \\ &= S_{n,b}(f)\frac{N^2}{12}\frac{BW}{4},\end{aligned} \tag{3.12}$$

where

$$S_{n,b}(f) = S_{n,bp1}(f) + S_{n,bn1}(f) + S_{n,bp2}(f) + S_{n,bn2}(f). \tag{3.13}$$

The two PMOS level-shifting buffers have the same transconductance and

$$S_{n,bp}(f) = S_{n,bp1}(f) = S_{n,bp2}(f) \tag{3.14}$$

from Equation 2.36. Likewise, the two NMOS-level shifting buffers have the same transconductance and

$$S_{n,bn}(f) = S_{n,bn1}(f) = S_{n,bn2}(f) \tag{3.15}$$

from Equation 2.37. Then the output-referred noise power is

$$\overline{v_{n,b,out}^2} = \left(\frac{16kT\gamma}{g_{mp,b}} + \frac{16kT\gamma}{g_{mn,b}}\right)\frac{N^2}{12}\frac{BW}{4}. \tag{3.16}$$

Finally, the noise is referred to the ADC input:

$$\overline{v_{n,b,in}^2} = \left(\frac{16kT\gamma}{g_{mp,b}} + \frac{16kT\gamma}{g_{mn,b}}\right)\frac{N^2}{12}\frac{BW}{4}\frac{1}{G_s^2}. \tag{3.17}$$

Compared to reference buffer noise in the conventional circuit in Equation 2.47, the buffer noise contribution increases by a factor of two due to the lack of the partial noise cancellation.

3.2 Analysis of the AC Equivalent Incremental Circuit Model

The equivalent incremental circuit model in Figure 3-7 is used for a more detailed analysis of the VGRB technique in a switched-capacitor circuit. The op-amp is modeled as a voltage-controlled voltage source with a finite gain of A and finite output impedance r_o. The level-shifting buffer is modeled as a voltage-controlled voltage source with gain of G_b and finite output impedance r_b. A single-pole model is chosen for both the op-amp and the level-shifting buffer. In reality, both circuit blocks have high frequency internal poles which can be modeled by adding frequency de-

pendency on A and G_b. These effects are not considered in the following analysis for simplicity. The parasitic capacitance at the level-shifting buffer output is $C_{p,1}$. The parasitic capacitance at the virtual ground node is $C_{p,2}$ and includes input capacitance of the level-shifting buffers and the op-amp as well as the routing capacitance. The load capacitance, C_L, is equivalent to the sampling capacitance of the following stage. The voltages at the dependent voltage source of the level-shifting buffer and the op-amp are v_1 and v_2, respectively. The input-referred noise voltages of the level-shifting buffer and the op-amp are $v_{n,b}$ and $v_{n,oa}$, respectively. Without loss of generality, the following parameter values are assumed throughout the analysis: $r_b = 100\Omega, r_o = 200\text{k}\Omega, C_{p,1} = 50\text{fF}, C_{p,2} = 200\text{fF}, C_L = 450\text{fF}$, and $A = 4000$. These parameter values approximate the design values in Chapter 4.

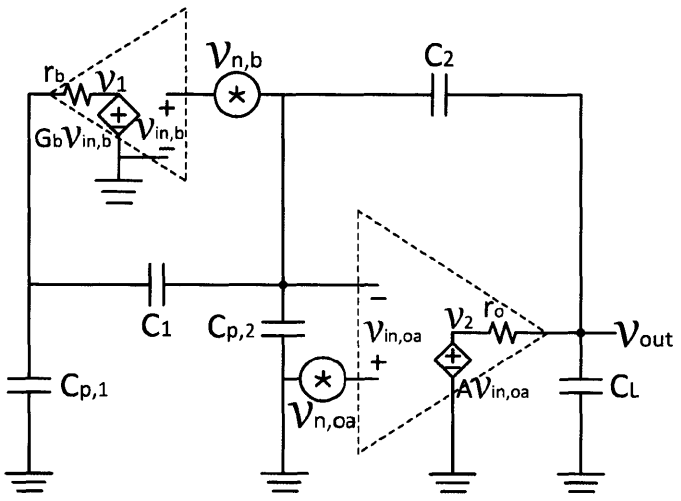


Figure 3-7: The equivalent incremental circuit model of a switched-capacitor circuit with VGRB.

3.2.1 Op-Amp Feedback Factor and Noise Gain

The op-amp feedback factor is analyzed first. For this purpose, the equivalent incremental circuit model in Figure 3-7 is simplified to the equivalent incremental circuit model in Figure 3-8. Here, Z_1 is the impedance looking into the level-shifting buffer

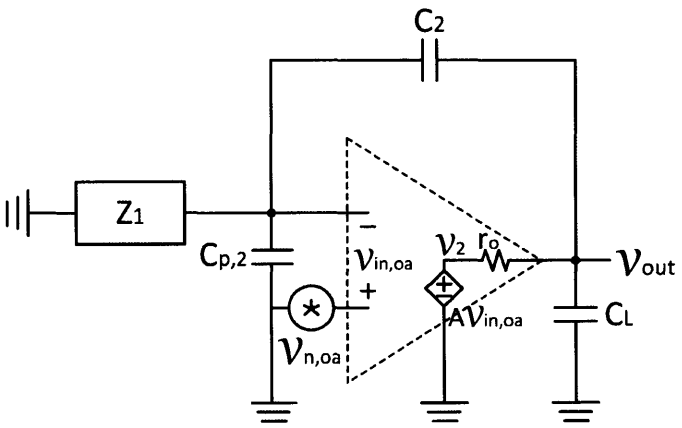


Figure 3-8: The AC equivalent incremental circuit model used for op-amp feedback analysis.

bootstrapping C_1 as shown in Figure 3-9. Solving for Z_1 using nodal analysis gives

$$Z_1 = \frac{1 + sr_b(C_1 + C_{p,1})}{s^2 C_1 C_{p,1} r_b + sC_1(1 - G_b)}. \tag{3.18}$$

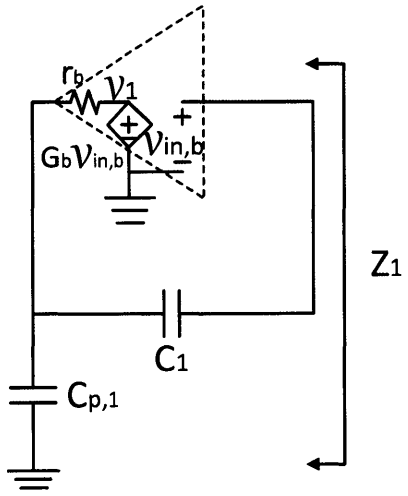


Figure 3-9: Impedance looking into the level-shifting buffer bootstrapping C_1.

The closed-loop transfer function is obtained using the block diagram of the circuit model in Figure 3-10. Based on the widely known loop-gain analysis formula,

$$H_{oa}(s) = \frac{V_{out}}{V_{n,oa}} = \frac{Ab}{1 + Ab\beta}, \tag{3.19}$$

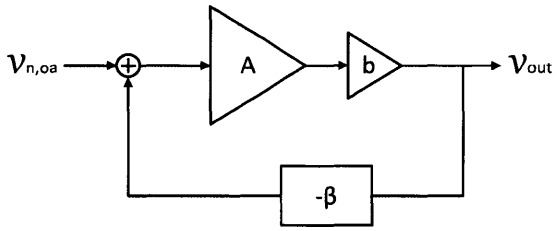


Figure 3-10: Block diagram of the VGRB circuit.

where b is

$$b = \frac{V_{out}}{V_2}\Big|_{V_{n,b=0}} = \frac{\left(Z_1 \| \frac{1}{sC_{p,2}} + \frac{1}{sC_2}\right) \| \frac{1}{sC_L}}{\left(Z_1 \| \frac{1}{sC_{p,2}} + \frac{1}{sC_2}\right) \| \frac{1}{sC_L} + r_o} \tag{3.20}$$

and the feedback factor is

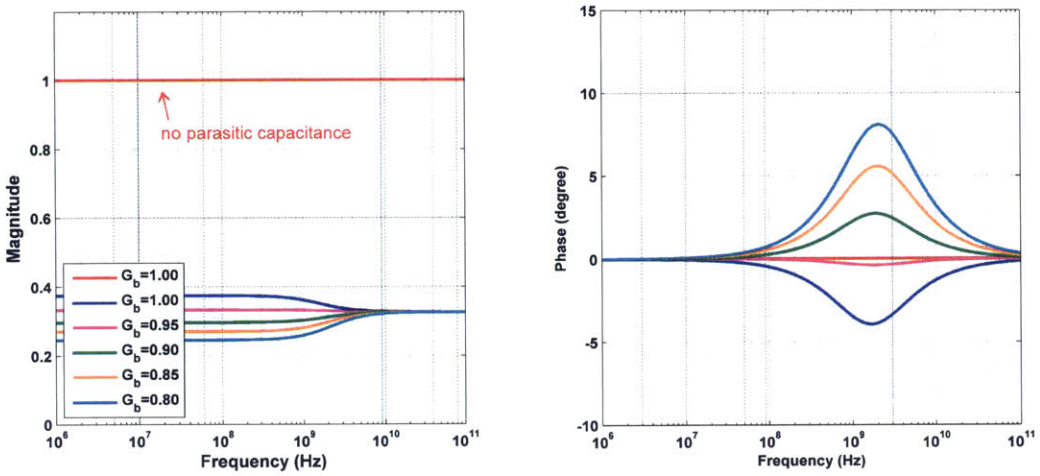
$$\beta = \frac{Z_1 \| \frac{1}{sC_{p,2}}}{Z_1 \| \frac{1}{sC_{p,2}} + \frac{1}{sC_2}}. \tag{3.21}$$

The frequency response of β in Equation 3.21 with varying G_b is shown in Figure 3-11. In the simplest case when $G_b = 1$ and $C_{p,1} = C_{p,2} = 0$, the feedback factor is unity as expected. In reality, the presence of the parasitic capacitances $C_{p,1}$ and $C_{p,2}$ degrades the feedback factor and β becomes frequency-dependent since the level-shifting buffer has a finite bandwidth. The frequency dependency of β also contributes phase shift in the feedback path. At low frequencies, the closer G_b is to unity, the larger the proportion of C_1 that is bootstrapped away, resulting in an improved feedback factor

$$\beta_{lf} = \frac{C_2}{(1 - G_b)C_1 + C_{p,2} + C_2}. \tag{3.22}$$

To achieve a favorable β, G_b close to unity and low parasitic capacitance is desired. At high frequencies, the level-shifting buffer is no longer able to bootstrap away C_1, and β converges to

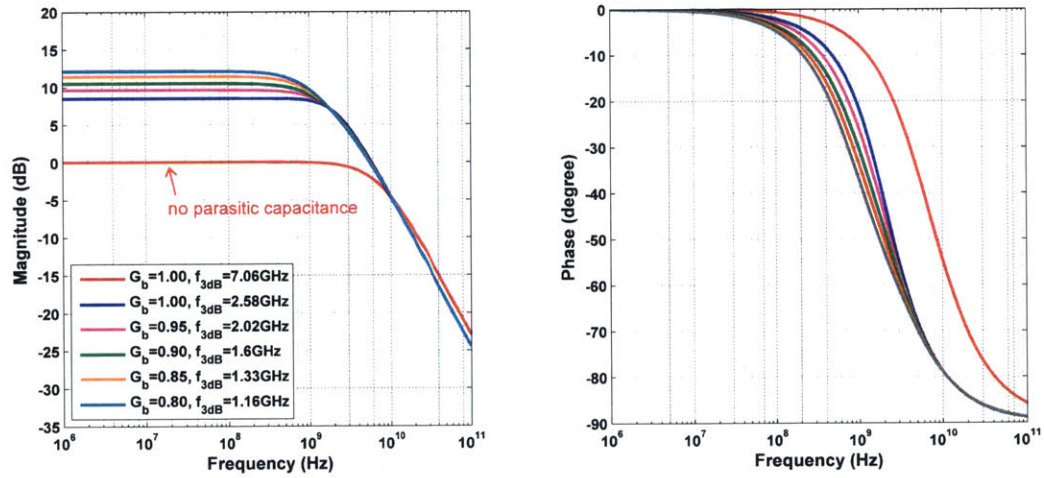
$$\beta_{hf} = \frac{C_2}{\frac{C_1 C_{p,1}}{C_1 + C_{p,1}} + C_{p,2} + C_2}. \tag{3.23}$$



(a) (b)

Figure 3-11: (a) Magnitude and (b) phase of the frequency response of of the feedback factor β as a function of the level-shifting buffer gain G_b.

Next, the frequency response of the transfer function $H_{oa}(s)$ in Equation 3.19 is explored. The transfer function is plotted in Figure 3-12 for different buffer gain settings. For a unity buffer gain that completely bootstraps away C_1 with no parasitic capacitance, the op-amp noise gain to the output is unity and the transfer function has maximum bandwidth. As expected, the transfer function gain increases with reduced buffer gain, resulting in greater amplification of the op-amp input-referred



(a) (b)

Figure 3-12: (a) Magnitude and (b) phase of the op-amp noise transfer function H_{oa}(s) as a function of the level-shifting buffer gain G_b.

noise to the output. The bandwidth decreases due to degraded feedback factor as previously mentioned in the discussion for Figure 3-11. Also, even with the ideal unity buffer gain, the magnitude and bandwidth of the transfer function is affected by the presence of the added parasitic capacitance.

3.2.2 Level-Shifting Buffer Noise Gain

The block diagram of the circuit in Figure 3-7 is shown in Figure 3-13. The feedforward transmission in [41, 42] is not included in the block diagram for simplification. Here, b_1 is the transfer function from v_1 to the virtual ground node, v_x, with the output node grounded, while b_2 is the transfer function from v_2 to v_{out} with $v_{n,b}$ shorted. The feedback factor from v_{out} to v_x while v_1 is grounded is β_o. Although β_o is equivalent to the feedback factor of the op-amp in the conventional circuits, it is not the effective feedback factor in the VGRB technique.

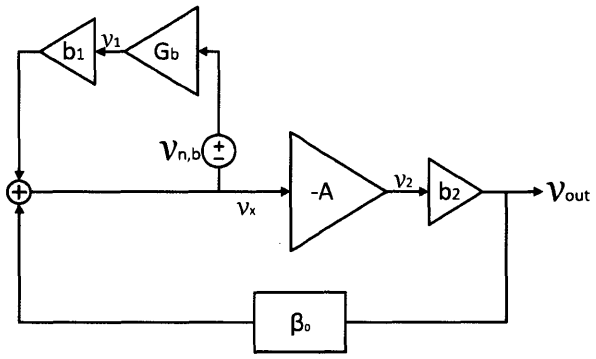


Figure 3-13: The block diagram of a switched-capacitor circuit based on the VGRB technique.

The system in Figure 3-13 is solved to obtain the closed-loop response:

$$H(s) = \frac{V_{out}}{V_{n,b}} = \frac{-G_b A b_1 b_2}{1 - G_b b_1 + \beta_o A b_2}. \tag{3.24}$$

where expressions for b_1, b_2, and β are as follows:

$$b_1 = \frac{V_x}{V_1}\Big|_{V_{out}=0}$$

$$= \frac{1}{sr_b\Big(\frac{C_1(C_2+C_{p,2})}{C_1+C_2+C_{p,2}} + C_{p,1}\Big) + 1} \frac{C_1}{C_1+C_2+C_{p,2}} \tag{3.25}$$

$$b_2 = \frac{V_{out}}{V_2}\Big|_{V_{n,b}=0} = b \tag{3.26}$$

$$\beta_o = \frac{V_x}{V_{out}}\Big|_{V_1=0}$$

$$= \frac{\left(r_b \Big\| \frac{1}{sC_{p,1}} + \frac{1}{sC_1}\right) \Big\| \frac{1}{sC_{p,2}}}{\left(r_b \Big\| \frac{1}{sC_{p,1}} + \frac{1}{sC_1}\right) \Big\| \frac{1}{sC_{p,2}} + \frac{1}{sC_2}}. \tag{3.27}$$

Equation 3.24 can also be expressed as

$$H(s) = H_1(s)H_2(s), \tag{3.28}$$

where

$$H_1(s) = \frac{V_x}{V_{n,b}}\Big|_{V_{out}=0} = \frac{G_b b_1}{1 - G_b b_1}, \tag{3.29}$$

$$H_2(s) = \frac{V_{out}}{V_x}\Big|_{V_{n,b}=0} = \frac{-Ab_2}{1 + Ab_2\beta_{VGRB}}, \tag{3.30}$$

and

$$\beta_{VGRB} = \frac{\beta_o}{1 - G_b b_1}. \tag{3.31}$$

$H_1(s)$ is the transfer function from $V_{n,b}$ to the virtual ground node and $H_2(s)$ is the transfer function from the virtual ground node to the output voltage in a closed-loop system with effective feedback factor, β_{VGRB}. In the VGRB technique, the local

feedback formed by the level-shifting buffer and C_1 improves the feedback factor of the op-amp from β_o to β_{VGRB}.

Interestingly, if Equations 3.21 and 3.31 are fully expanded, it can be proven that

$$\beta = \beta_{VGRB} \tag{3.32}$$

and ultimately, comparing Equation 3.19 to 3.30

$$H_2(s) = -H_{oa}(s). \tag{3.33}$$

This shows that the transfer function of the noise gain from the input-referred noise of the level-shifting buffer to the output of the switched-capacitor circuit is equivalent to the cascade of $H_1(s)$ and $-H_{oa}(s)$. It is shown in the frequency response analysis later in this section that $H_{oa}(s)$ has smaller bandwidth than $H_1(s)$ in practical designs and therefore, the op-amp closed-loop bandwidth sets the noise bandwidth of the level-shifting buffer.

Noise Gain in Ideal Case

To analyze the closed-loop response in its simplest form, the equivalent incremental circuit in Figure 3-7 is reduced by assuming $r_b = r_o = 0$, and $C_{p,1} = C_{p,2} = 0$. The level-shifting buffer and op-amp have infinite bandwidth and the parasitic capacitances are removed. Then, Equations 3.25, 3.20, 3.27, and 3.18 become

$$b_1 \approx \frac{C_1}{C_1 + C_2}, \tag{3.34}$$

$$b_2 \approx 1, \tag{3.35}$$

$$\beta_o \approx \frac{C_2}{C_1 + C_2}, \tag{3.36}$$

$$Z_1 \approx \infty. \tag{3.37}$$

Also, substituting Equations 3.34 and 3.36 into 3.31,

$$\beta_{VGRB} \approx \frac{C_2}{C_1 + C_2 - G_b C_1}. \tag{3.38}$$

If the level-shifting buffer has an ideal unity gain, the effective feedback factor of the op-amp is improved to unity from the β_o in Equation 3.36 as previously discussed. Again, this is intuitively explained by the fact that $Z_{in} = \infty$ in Equation 3.37 and C_1 is completely removed from the feedback network. As G_b decreases, a bigger proportion of C_1 loads the virtual ground node and β_{VGRB} worsens.

Substituting Equations 3.34-3.36 with $G_b = 1$ and $A = \infty$ into Equations 3.29 and 3.30,

$$H_1 \approx \frac{b_1}{1 - b_1} \approx \frac{C_1}{C_2}, \tag{3.39}$$

$$H_2 \approx -\frac{1}{\beta_{VGRB}} \approx -1, \tag{3.40}$$

and

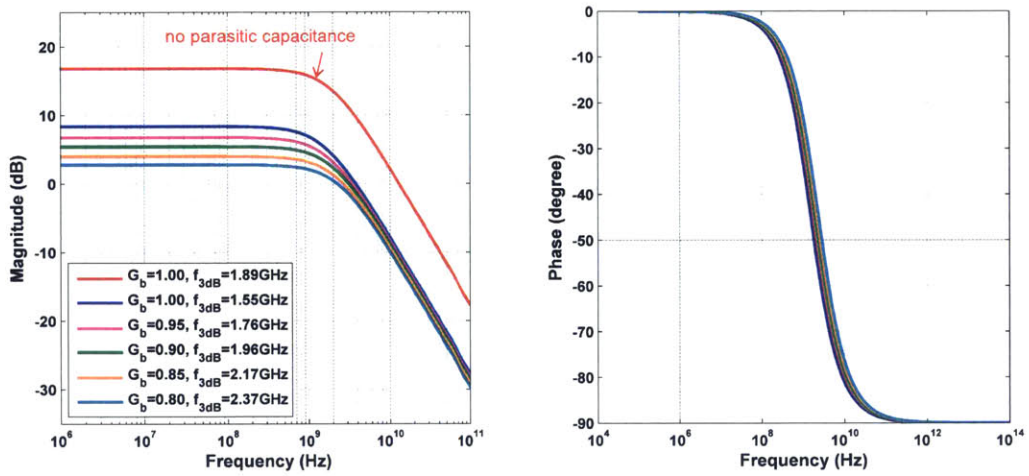
$$H \approx -\frac{C_1}{C_2}. \tag{3.41}$$

This is equivalent to the signal gain of an ideal inverting amplifier configuration.

Frequency Response Analysis

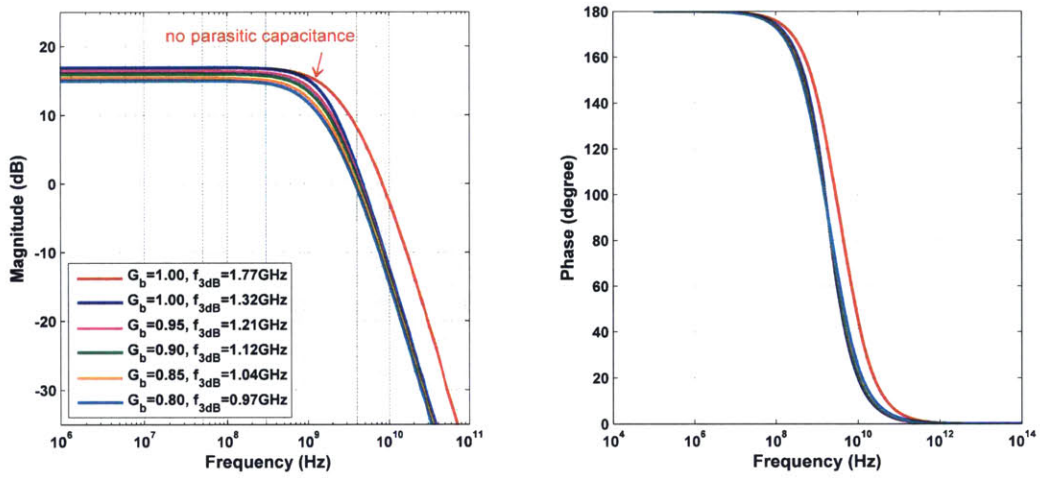
The frequency response of $H(s)$ consists of the transfer function $H_1(s)$ and $H_2(s)$ in Equation 3.28. The frequency response of $H_1(s)$ is shown in Figure 3-14. At $G_b = 1$, $H_1(s)$ has high gain at the cost of lower f_{3dB} bandwidth. As G_b decreases, the gain drops and the bandwidth increases. The parasitic capacitance reduces the gain as well as the bandwidth. $H_2(s)$ is equivalent to $-H_{oa}(s)$ in Equation 3.33 and the frequency response of $H_{oa}(s)$ was presented in Figure 3-12.

Combining the frequency response of $H_1(s)$ and $H_2(s)$, the frequency response of $H(s)$ is shown in Figure 3-15. Considering the frequency response of $H_1(s)$ in Figure 3-14 and $H_{oa}(s)$ in Figure 3-12, the bandwidth of $H(s)$ is dominantly set by



(a) (b)

Figure 3-14: Frequency response of $H_1(s)$ as a function of the level-shifting buffer gain G_b.



(a) (b)

Figure 3-15: Frequency response of $H(s)$ as a function of the level-shifting buffer gain G_b.

the bandwidth of $H_1(s)$ when $G_b = 1$ since the op-amp has high bandwidth attributed to high β_{VGRB}. The bandwidth of $H_2(s)$ becomes the more dominant factor as G_b decreases and degrades β_{VGRB}. Specifically in the demonstrated example, the op-amp bandwidth becomes more critical as G_b falls below 0.9. In fact, this is the likely scenario in actual implementation since it is difficult to design a level-shifting buffer with unity gain.

3.3 Variations in Reference Voltages

Due to process variation, V_{REFP1} differs from V_{REFP2}, and V_{REFM1} differs from V_{REFM2}. The differential reference voltage is a function of all four reference voltages. Figure 3-6 is used for the analysis. Charge conservation gives the following set of equations for the charge-transfer phase:

$$C_2(v_{OUT+} - V_{CM}) = -\left((V_{REFP1} - V_{CM})\sum_{i=1}^{k} C_{1,i+} + (V_{REFM1} - V_{CM})\sum_{i=k+1}^{N} C_{1,i+}\right)$$
$$+(v_{IN+} - V_{CM})\sum_{i=1}^{N}(C_{1,i+} + C_2), \tag{3.42}$$

$$C_2(v_{OUT-} - V_{CM}) = -\left((V_{REFM2} - V_{CM})\sum_{i=1}^{k} C_{1,i-} + (V_{REFP2} - V_{CM})\sum_{i=k+1}^{N} C_{1,i-}\right)$$
$$+(v_{IN-} - V_{CM})\sum_{i=1}^{N}(C_{1,i-} + C_2). \tag{3.43}$$

Solving for the differential output with equivalent unit capacitor $C_{1,i} = C_{1,i+} = C_{1,i-}$,

$$\begin{aligned} v_{OUT} &= v_{OUT+} - v_{OUT-} \\ &= \frac{(-V_{REFP1} + V_{REFM2})\sum_{i=1}^{k} C_{1,i} + (V_{REFP2} - V_{REFM1})\sum_{i=k+1}^{N} C_{1,i}}{C_2} \\ &\quad + \frac{(v_{IN+} - v_{IN-})\sum_{i=1}^{N}(C_{1,i} + C_2)}{C_2} \end{aligned} \tag{3.44}$$

The differential reference voltage can then be derived based on Equation 3.44. If a single comparator that outputs a low decision-bit flips its decision and outputs a high decision-bit for the same sampled input signal, the MDAC residue voltage drops by

$$\Delta v_{OUT,k\to k+1} = \frac{(-V_{REFP1} + V_{REFM2})\sum_{i=1}^{k} C_{1,i} + (V_{REFP2} - V_{REFM1})\sum_{i=k+1}^{N} C_{1,i}}{C_2}$$
$$- \frac{(-V_{REFP1} + V_{REFM2})\sum_{i=1}^{k+1} C_{1,i} + (V_{REFP2} - V_{REFM1})\sum_{i=k+2}^{N} C_{1,i}}{C_2},$$

which reduces to

$$\Delta v_{OUT,k\rightarrow k+1} = \frac{(V_{REFP1} - V_{REFM2})C_{1,i} + (V_{REFP2} - V_{REFM1})C_{1,i}}{C_2}. \quad (3.45)$$

In the implementation of the pipelined ADC in Chapter 4, $C_2 = 2C_{1,i}$, and

$$V_{REF} = \frac{(V_{REFP1} - V_{REFM2}) + (V_{REFP2} - V_{REFM1})}{2}. \quad (3.46)$$

The effective differential reference voltage is thus the average of two sets of reference voltages.

Examples of the residue plot with various reference voltage variation values are shown in Figure 3-16 for a 14 decision-level MDAC. The four reference voltages are set to the nominal values in Figure 3-16a and variations are added in Figures 3-16b to 3-16f. V_{REF} is set to 800mV for all examples according to Equation 3.46. The output swing is limited to $\pm$0.5V including the over-range. Regardless of the variation in the reference voltages, each comparator bit transition results in 800mV of residue voltage drop because V_{REF} is set to 800mV. The absolute values of the reference voltages, however, may add offset that amounts to

$$V_{OFFSET} = \frac{-(V_{REFP1} - V_{REFM2})\sum_{i=1}^{\frac{N}{2}} C_{1,i} + (V_{REFP2} - V_{REFM1})\sum_{i=1}^{\frac{N}{2}} C_{1,i}}{C_2}, \quad (3.47)$$

and corresponds to a voltage shift in the residue by -70mV, -70mV, and 140mV in Figures 3-16b, 3-16c, and 3-16f, respectively. The offset in the residue does not impact the linearity of the MDAC as long as the residue is within the op-amp output range. In Figure 3-16f, however, the offset is large enough that the residue extends beyond the over-range and linearity degradation is inevitable. This is an extreme example for illustration, however, since $V_{REFP1} - V_{REFP2} = -35$mV in this case; in implementation, the level-shifting buffers are sized to have much smaller process variations and the offset is significantly reduced. In addition, they are designed to be programmable. Nevertheless, the offset in Equation 3.47 increases with higher signal gain.

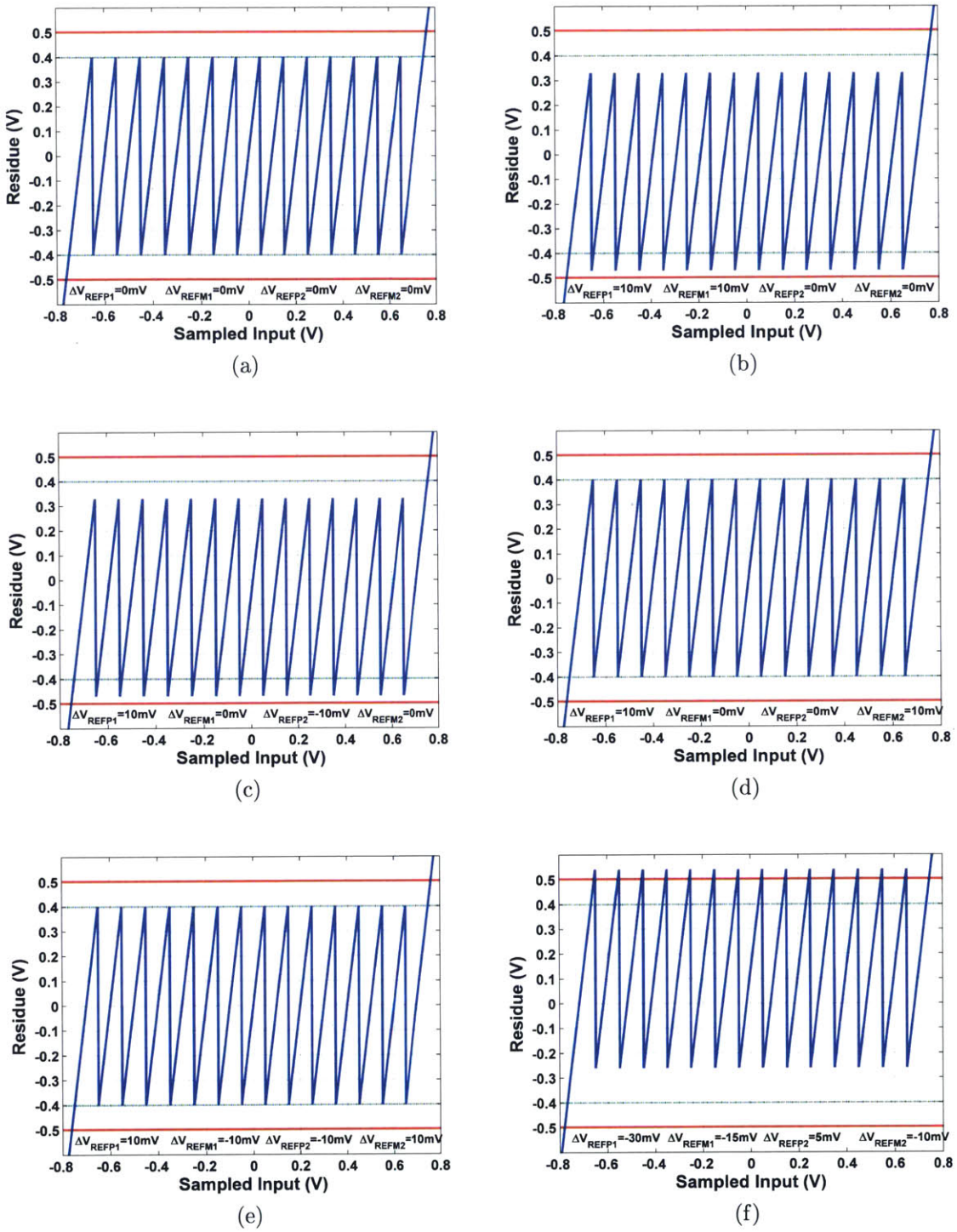


Figure 3-16: Residue plot of a pipelined stage using VGRBs with varying reference voltages.

3.4 Reference Voltage for the Resistor Ladders

In conventional pipelined ADCs, the positive and negative reference voltages can be used as the power rails of the resistor ladder. In the pipelined ADC with VGRBs, the power rails of the resistor ladders come from a different source. The mismatch between the reference voltage, V_{REF}, generated by the level-shifting buffers and the reference voltage that is set for the resistor ladder manifest as skewed residue as shown in Figure 3-17. For example, if the reference voltage set for the resistor ladder is higher than the reference voltage generated in the MDAC, then the residue plot has an upward slope as shown. On the other hand, if the reference voltage set for the reference ladder is lower than the reference voltage generated in the MDAC, then the residue plot has a downward slope. The issue aggravates with high signal gain.

The linearity is not affected as long as the residue remains within the over-range. It is the vertical residue voltage drop at each comparator bit transition that must be maintained for linearity and this is fixed by the level-shifting buffer. The slope in the residue plot can be understood as comparator offsets, which is corrected by the over-range scheme. However, due to the high signal gain in the front-end stage and the reduced over-range with low supply voltage in advanced CMOS, the effect should not be ignored. The signal gain in the second stage and beyond is usually lower and the linearity requirement is significantly relaxed, reducing the impact of this issue.

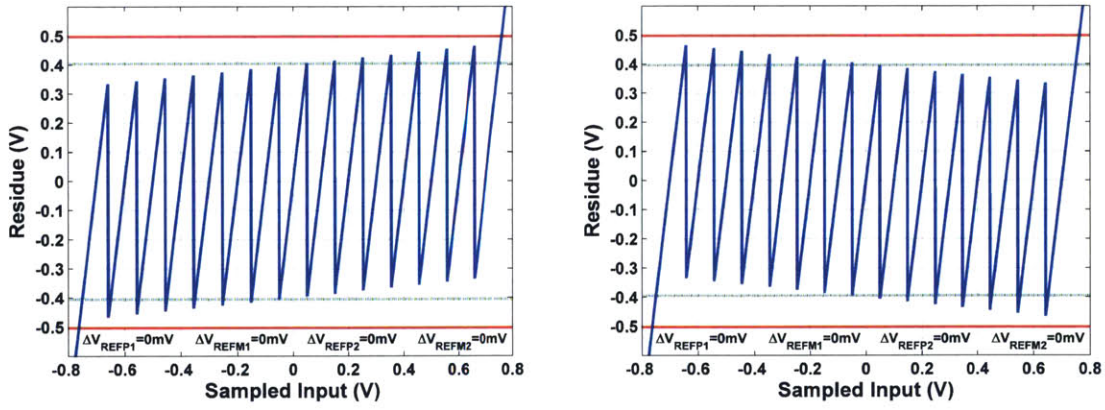


Figure 3-17: Residue plot of a pipelined stage with reference voltage for the reference ladder set (a) 10mV higher and (b) 10mV lower than the MDAC reference voltage.

3.5 Other Applications of Virtual Ground Reference Buffer Technique

In this thesis, the VGRB technique is applied in the MDAC of a pipelined ADC, but the technique can be applied on various other switched-capacitor circuits. Discrete-time filters are one possible application. The parasitic insensitive switched-capacitor integrators shown in Figure 3-18 are key building blocks of discrete-time filters. In the lossless noninverting integrator in Figure 3-18a, the C_1 capacitor is charged in clock phase Φ_1. During Φ_1, the charge transfers to the C_2 capacitor. The lossy noninverting integrator in Figure 3-18b is formed by a switched-capacitor resistor across the C_2 capacitor. In these two integrator configurations, the closed-loop response in terms of speed, noise, and settling accuracy is governed by the principles explained in Chapter 2. By bootstrapping away C_1 using the VGRB technique, better feedback factor can be achieved for the integration phase. Unlike in the MDAC application, the addition or subtraction of reference voltage is not needed. Therefore, a non-level shifting virtual ground buffer is preferred for this application.

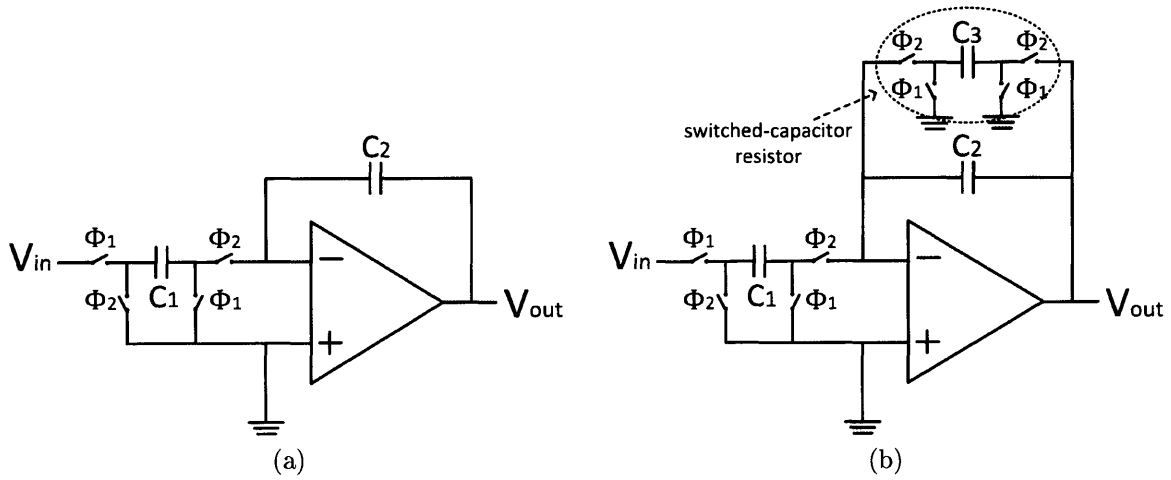


Figure 3-18: Parasitic-insensitive noninverting integrators: (a) lossless noninverting and (b) lossy integrator.

$\Sigma\Delta$ modulators are also often implemented in switched-capacitor circuits. A first-order $\Sigma\Delta$ modulator is shown in Figure 3-19. The switched-capacitor circuit integrates the input signal in each clock period. The reference voltage is subtracted when

the comparator output, D, flips high. In the $\Sigma\Delta$ modulator, the quantization noise is pushed to higher frequencies. Oversampling reduces in-band noise further and the shaped noise is removed using a decimation filter. The foregoing switched-capacitor integrators form the building block of $\Sigma\Delta$ modulators, and higher-order $\Sigma\Delta$ modulators use additional integrators to increase the noise-shaping characteristics. Reference voltage addition and subtractions can be implemented with the level-shifting buffers. Since the speed of the $\Sigma\Delta$ modulator largely depends on the settling of the switched-capacitor circuit, which in turn sets the required op-amp performance, applying the VGRB technique provides the same set of advantages detailed throughout this chapter. Also, another interesting application is proposed in [43]. The sampling capacitance is bootstrapped using non-level shifting buffers for jitter and load-insensitive charge-transfer in continuous-time $\Sigma\Delta$ ADCs. Although the proposed solution is not meant for op-amp feedback factor improvement, it addresses distortion of the input signal and inaccurate charge-transfer.

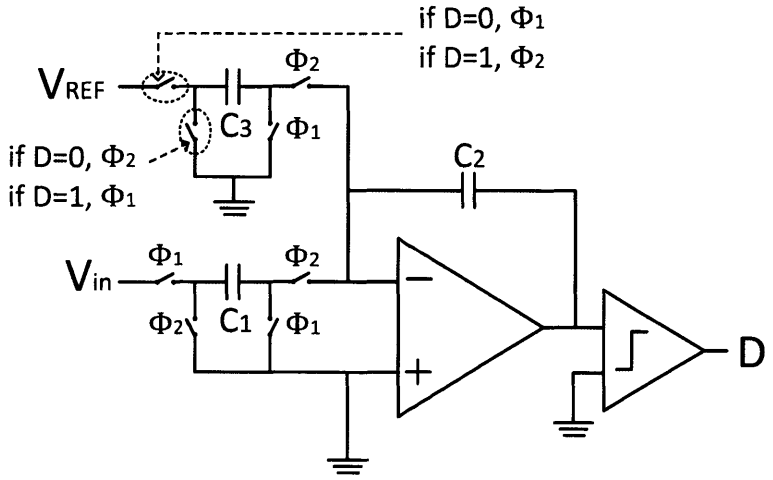


Figure 3-19: Switched-capacitor first-order $\Sigma\Delta$ modulator.

Chapter 4

Design and Implementation of a Pipelined ADC with Virtual Ground Reference Buffers

In this chapter, the design and the implementation details of the 12-bit 250MS/s ADC are presented. The VGRB technique is applied in every stage except in the last stage which is a flash ADC. Each circuit block and the timing of its operation are detailed. The implementation of the level-shifting buffers with good slewing is particularly important. Bulk-biasing is applied in the input transistor of the level-shifting buffers as a coarse tuning method to achieve the targeted reference voltage. The matching in the reference voltages generated in each stage affects the ADC linearity and this problem is addressed by applying current-controlled fine tuning. Due to the limited over-range, comparator offsets are calibrated in the first stage sub-ADC. In layout, bootstrapping of the routing capacitance at the virtual ground node provides better feedback factor. The obtained feedback factor is examined based on the decomposition of the parasitic capacitance loading the virtual ground node. Lastly, the input-referred noise of the circuit is discussed.

4.1 Circuit Implementation

The top-level block diagram of the pipelined ADC implemented based on the VGRB technique is shown in Figure 4-1. The ADC consists of five stages. The first stage resolves 3.9-bits with 14 comparators and a signal gain of 8. The second stage to the fourth stages are identical, each stage resolving 2.6-bits with six comparators and a signal gain of 4. These stages resolve 2-bits excluding the over-range correction bits. The final stage is a 4.5-bit flash. The digital bits in each stage are time-aligned, then added to convert to a binary code from a thermometer code, and the low-voltage differential signal (LVDS) buffers drive the digital codes off-chip where they are truncated to 12-bits. The chip also includes circuits for clock buffering and biasing.

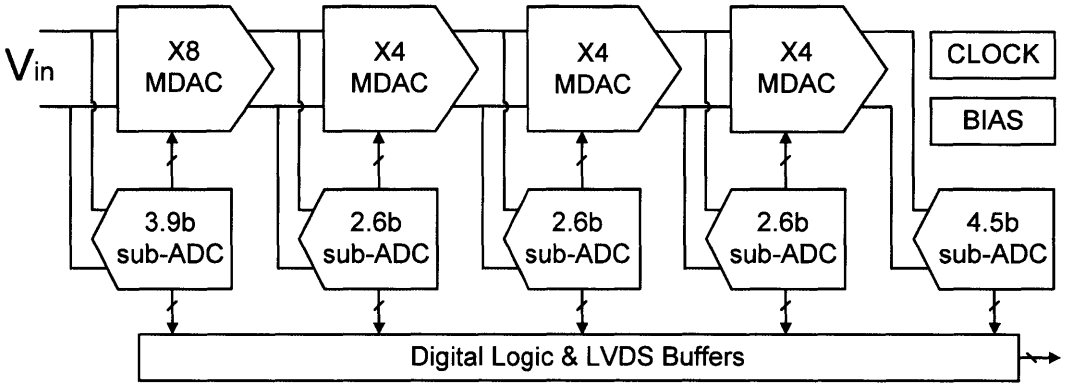
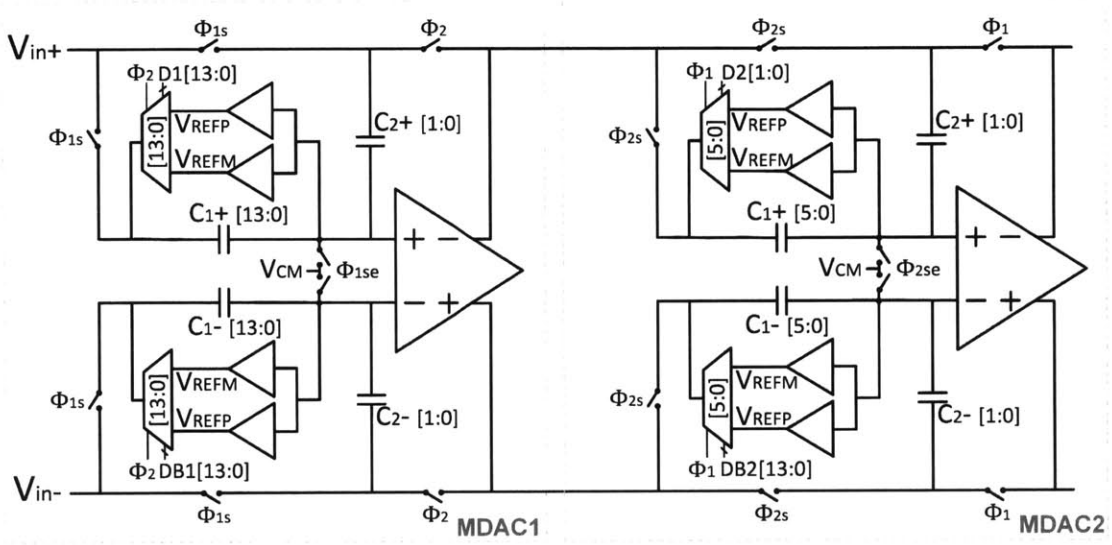


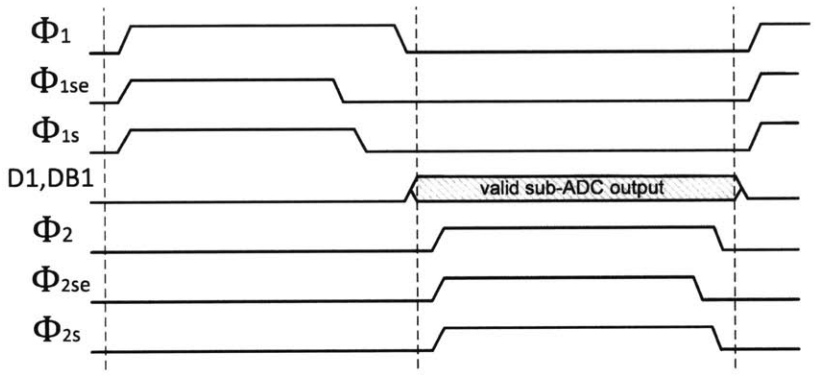
Figure 4-1: Block diagram of the 12-bit 250MS/s pipelined ADC.

4.1.1 Multiplying Digital-to-Analog Converter

The MDAC is the core of the pipelined stages. It samples the input signal and either subtracts or adds a low resolution quantized input signal based on the sub-ADC bit-decision output. The resulting residue is amplified and sampled by the MDAC in the following stage. The proposed VGRB technique makes key contributions in improving the performance of this process. The simplified schematic of the MDAC of the first two pipelined stages and the corresponding timing of the operation are shown in Figure 4-2.



(a)



(b)

Figure 4-2: (a) Schematic of first and second MDAC stages and the (b) corresponding timing of the operation.

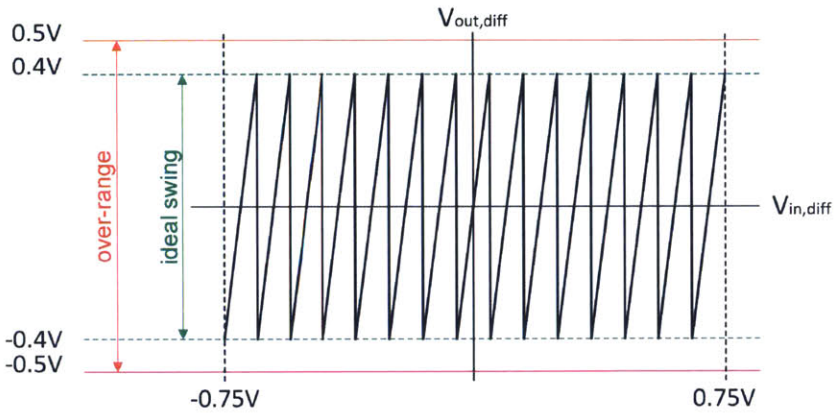
The sampling clock, Φ_{1se}, and the two non-overlapping clock Φ_1 and Φ_2 are generated from the clock generation circuit described in Section 4.1.7. All other clock signals are generated internally in each pipelined stage. In the sampling phase, Φ_{1se} and Φ_{1s} are high and both C_1 and C_2 track the input signal. The bottom-plate sampling occurs at the falling edge of Φ_{1se}. In the charge-transfer phase, Φ_2, the bit decisions D1 and DB1 from the sub-ADC configure the connections between the level-shifting buffers and the C_1 capacitor arrays. Then, C_2 flips around the op-amp and the MDAC amplifies the residue. Throughout the charge-transfer phase, the level-shifting buffers drive C_1 and engage in the bootstrapping action. The second

stage operates similarly, but it is in charge-transfer phase when the first stage is in sampling phase and vice versa.

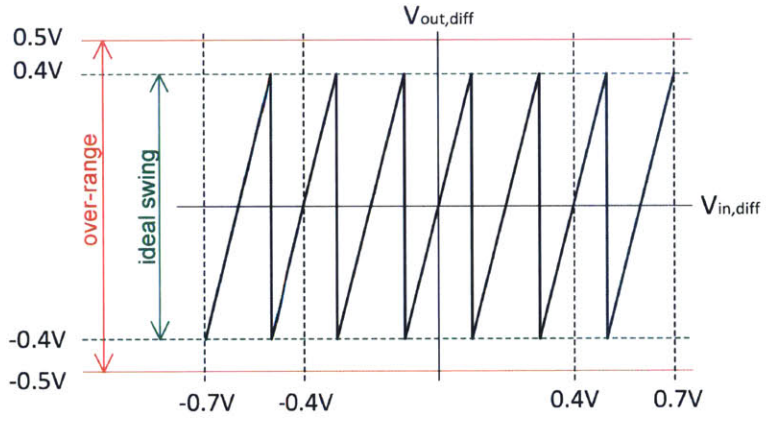
The positive reference voltage, V_{REFP}, and the negative reference voltage, V_{REFM}, are generated by the level-shifting reference buffers. The PMOS level-shifting buffer and C_1 form a feedback path when V_{REFP} drives C_1. Likewise, the NMOS level-shifting buffer and C_1 form a feedback path when V_{REFM} drives C_1. A total of four level-shifting buffers are employed in each stage of the fully-differential prototype since each virtual ground node requires two level-shifting buffers to generate the positive and negative reference voltages. Therefore, the implementation in this prototype chip consumes twice as much power in the buffers compared with conventional circuits that have two reference buffers. Although not implemented in the prototype, since each stage has a separate set of reference buffers that are engaged only in the charge-transfer phase, the reference buffers can be duty-cycled to save approximately 50% of power. Therefore, the total buffer power would be comparable to those in conventional circuits. Moreover, by breaking up the buffers into multiple parallel segments and selectively enabling them based on the number of capacitors connected to them, buffer power can be reduced by an additional 50%.

4.1.2 Stage Residue and Over-Range Correction

The residue plots of the first stage and the following stages are shown in Figure 4-3. The first stage has a peak-to-peak differential input signal range of 1.5V and resolves 3.9-bits. The comparator bit-decision threshold levels in the first stage sub-ADC are 100mV apart, resulting in a peak-to-peak differential output swing of 800mV in the MDAC for a signal gain of 8. The over-range correction extends the peak-to-peak differential output swing to 1V. In the second to the fourth stages, comparator bit-decision threshold levels in the sub-ADC are 200mV apart and the over-range correction can be applied to a differential input swing range as large as 1.4V. However, the residue of the preceding stage is limited to a differential swing of 1V since the op-amps suffer from nonlinearity beyond that range.



(a)



(b)

Figure 4-3: Residue plot of the (a) first stage and (b) second to fourth stage.

4.1.3 Sampling Network

The sampling network with bootstrapping circuit is shown in Figure 4-4. To reduce power consumption, the implemented ADC does not have a dedicated sample and hold circuit. Instead, the input signal is directly sampled on the C_1 and C_2 unit capacitors of the first pipelined stage. Bottom-plate sampling is used to reduce signal-dependency of charge injection. The switches at the common-mode voltage, V_{CM}, open slightly earlier than the bootstrapped switches and inject a constant charge that is canceled in the differential circuit. There is no charge injection from the bootstrapped switches when they open since the top plates of C_1 and C_2 are floating. The top plate switches are bootstrapped for higher linearity over a wider range of

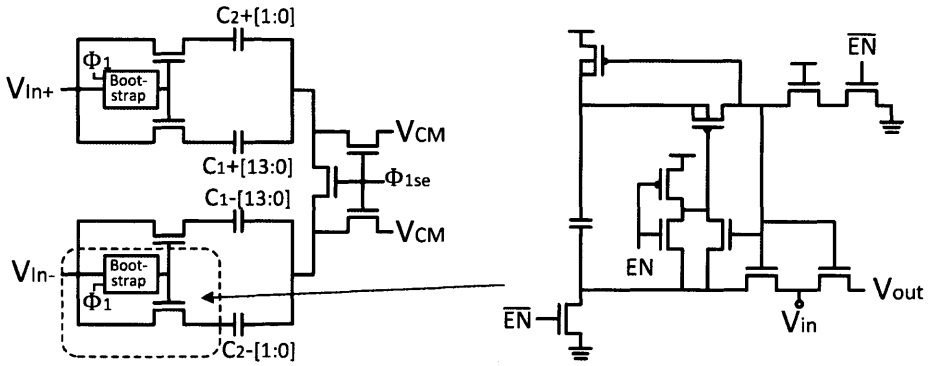


Figure 4-4: Schematic of the sampling network with bootstrapped switches.

input signals compared with transmission gates. The bootstrapped switches maintain nearly constant gate-source overdrive voltage to minimize the on-resistance variation dependent on the input signal amplitude, resulting in much less distortion in the sampling network [44]. The unit capacitor size in the first stage MDAC is 60fF and the total sampling capacitance in the MDAC is 960fF single-ended and 480fF differentially. This sampling capacitance corresponds to $92.5\mu V_{rms}$ of $\sqrt{\frac{KT}{C}}$ thermal noise voltage, corresponding to SNR of 75.16dB if limited by $\sqrt{\frac{kT}{C}}$ noise of the first stage. The unit capacitors in the second to the fourth stage MDAC are scaled down to 35fF.

4.1.4 Multiplex (MUX) Switches

The MUX switch is shown in Figure 4-5. The enable signal, EN, is set high during the charge-transfer phase and the bit decision, D, from the sub-ADC output configures the switches. V_{REFP} drives the output when D is high, and V_{REFM} drives the output when D is low. A MUX switch cell is required for each C_1 unit capacitor.

4.1.5 Gain-Boosted Operational Amplifier

Due to the reduced open-loop gain requirement, the proposed technique allows a single-stage gain-boosted telescopic op-amp in Figure 4-6 to be used in the pipelined stages for 12-bit accuracy. A current-efficient telescopic topology is chosen for the main amplifier instead of the folded cascode or two-stage op-amp at the cost of reduced

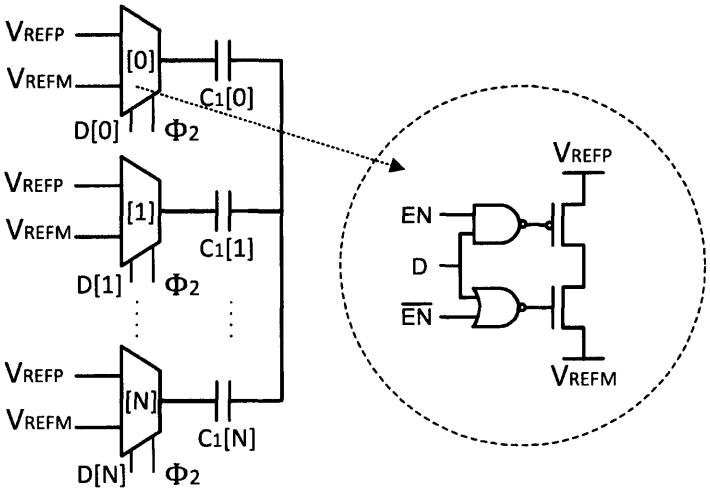


Figure 4-5: Schematic of the MUX switch.

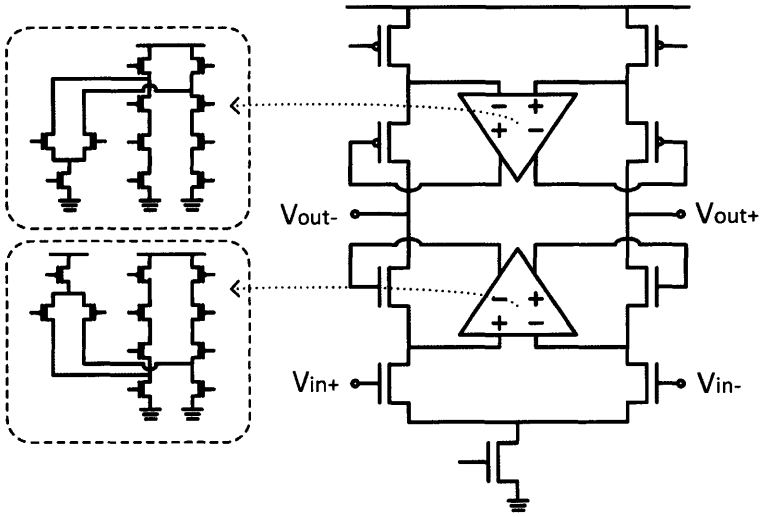


Figure 4-6: Gain boosted telescopic op-amp.

output swing range. Due to the five stacked transistors inherent in the telescopic op-amp topology, the peak-to-peak differential output swing including the over-range is limited to 1V in a 1.2V supply. The NMOS and PMOS cascode transistors are gain-boosted by a folded cascode boosting amplifier with a PMOS and NMOS differential input pair, respectively. The gain-boosting amplifier uses a single transistor for common-mode feedback for simplicity [45]. A conventional switched-capacitor common-mode feedback circuit is applied to the op-amp [46].

Since the parasitic capacitance of the input pair degrades the feedback factor of the switched-capacitor circuit as described in Section 3.1.1, the input transistors are

kept at minimum length to minimize parasitic contributions. For simplicity, identical op-amps are used throughout the pipelined stages without scaling, leaving room for a large amount of power savings in future designs.

4.1.6 Level-Shifting Buffers

The level-shifting buffers drive the $C_{1,i}$ unit capacitors fast enough that the closed-loop dynamics are limited by the op-amp performance. However, the settling of the reference voltages can be limited by the slewing rate of the level-shifting buffers and must be considered. If the sampled input signal is at the extreme ends, a single level-shifting buffer from each virtual ground node drives the maximum capacitive load corresponding to the full C_1. For example, if the sampled input signal is near its maximum, the PMOS level-shifting buffer on the positive virtual ground node drives all $C_{1,i}+$ unit capacitors, and the NMOS level-shifting buffer on the negative virtual ground node drives all $C_{1,i}-$ unit capacitors. This is illustrated in Figure 4-7. Likewise, if the input signal is at its minimum, the NMOS level-shifting buffer on the positive virtual ground node drives all $C_{1,i}+$ unit capacitors, and the PMOS level-shifting buffer on the negative virtual ground node drives all $C_{1,i}-$ unit capacitors. These two cases present the maximum settling time constant. However, the level-shifting buffers drive a relatively small voltage difference and thus the required slewing is not significant.

The mid-level sampled input signal can cause a longer settling if the slewing is considered. If the sampled input signal is at mid-level, the PMOS and NMOS level-shifting buffers on the positive virtual ground node each drive half of C_{1+} and the PMOS and NMOS level-shifting buffers on the negative virtual ground node each drive half of C_{1-}. This is illustrated in Figure 4-8. In this case, the loading from the $C_{1,i+}$ and $C_{1,i-}$ unit capacitors are equally distributed to the level-shifting buffers and the settling time constant of the reference voltage is reduced. However, the PMOS level-shifting buffers must pull up the voltage from the mid-scale input voltage to V_{REFP} and the NMOS level-shifting buffers must pull down the voltage to V_{REFM}. Due to the large voltage change magnitude, the slewing time can take up a significant

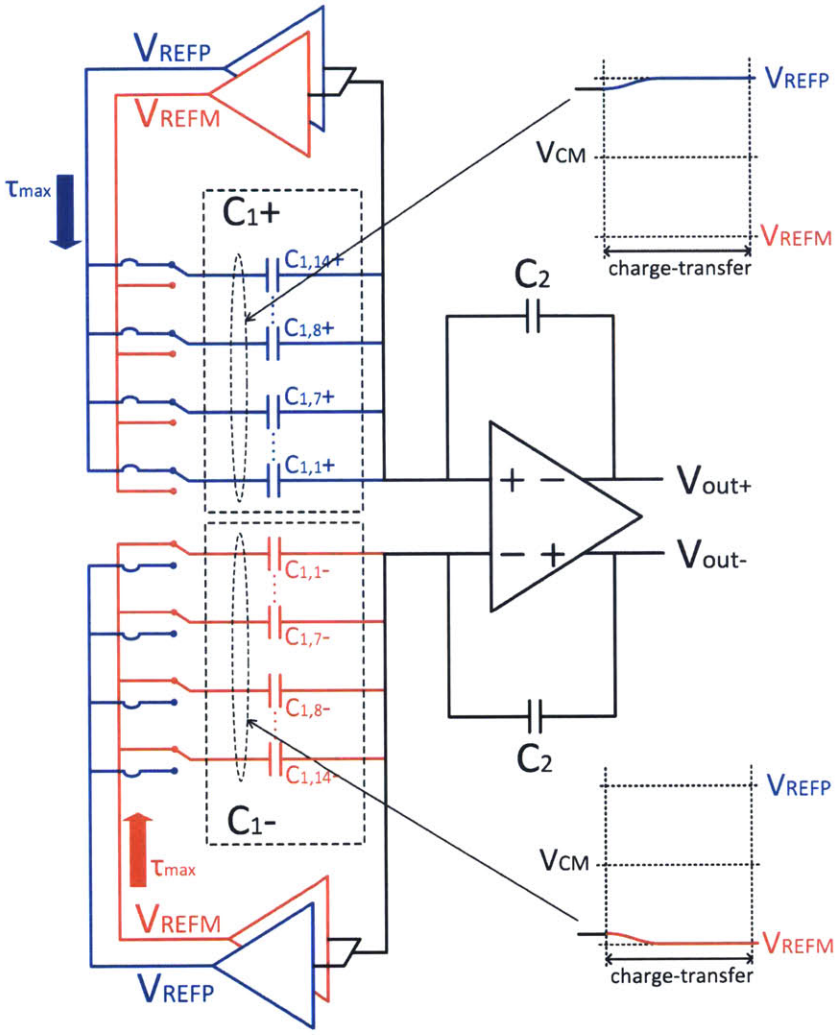


Figure 4-7: The connection configuration between the level-shifting buffers and the C_1 unit capacitors when the sampled input signal is near maximum value.

proportion of the charge-transfer phase compared with the previous example.

The flipped voltage follower (FVF) [47, 48] in Figure 4-9 is used as the level-shifting buffer to alleviate this issue. Compared with the conventional source follower, the PMOS and NMOS FVFs have better current sourcing and sinking ability, respectively. With the mid-scale input, the PMOS buffers only need to source current to C_1, and the NMOS buffers only need to sink current to C_1. Therefore, the current sourcing from the PMOS FVFs and the current sinking from the NMOS FVFs give much improved slewing. In the second to the fourth stages, the PMOS FVFs sink current and the NMOS FVFs source current if the output of the previous stage is in the

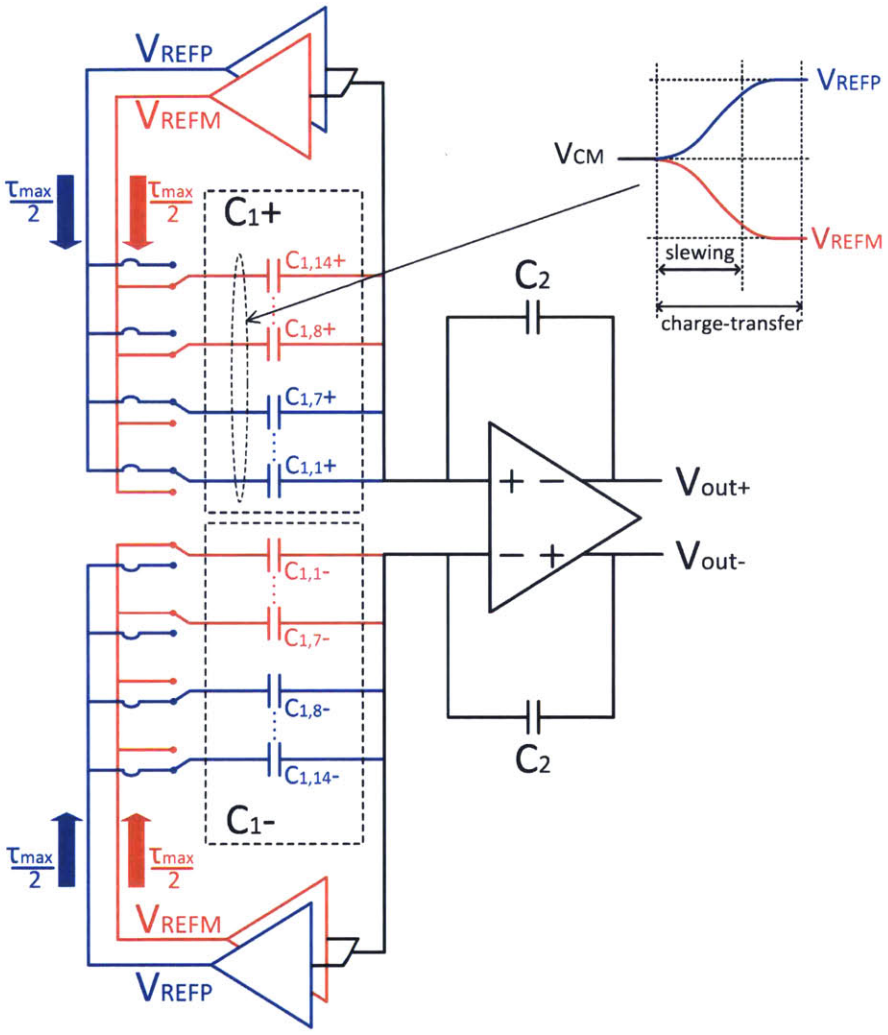
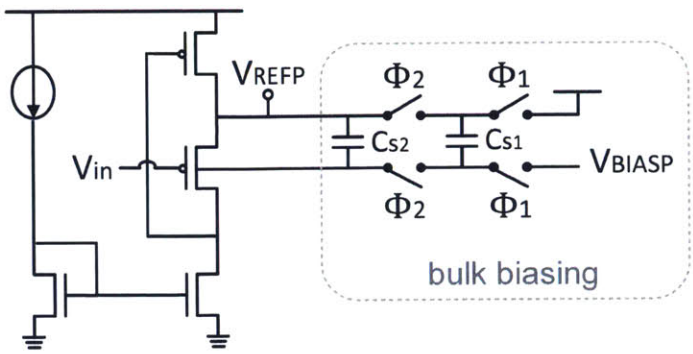


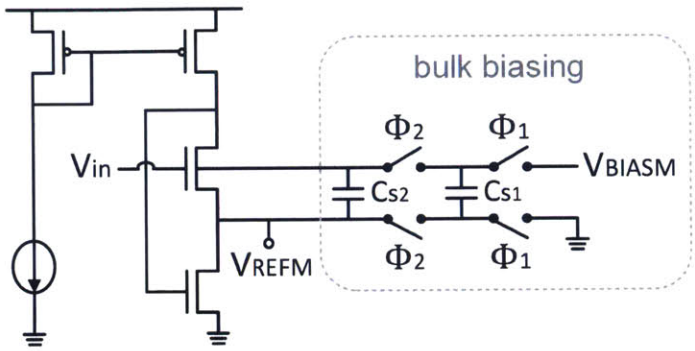
Figure 4-8: The connection configuration between the level-shifting buffers and the C_1 unit capacitors if the sampled input signal is near mid-level value.

over-range. However, the need for fast slewing is less crucial since the performance of the ADC is dominated by the first stage.

In addition to using low-V_T input transistors, a switched-capacitor circuit sets the body-to-source voltage, V_{BS}, of the input transistor to further reduce its V_T. The bulk biasing voltages V_{BIASP} and V_{BIASM} reduce the $|V_{GS}|$ in the PMOS and NMOS FVF, respectively, to achieve the targeted reference voltage $V_{REFP} - V_{REFM} \approx 800\text{mV}$. In the sampling phase, Φ_1, the bulk biasing voltage is sampled on C_{s1}. In the charge-transfer phase, Φ_2, the charge on C_{s1} is shared with C_{s2} and a voltage difference is applied across the source and bulk terminals of the input transistor. The change in

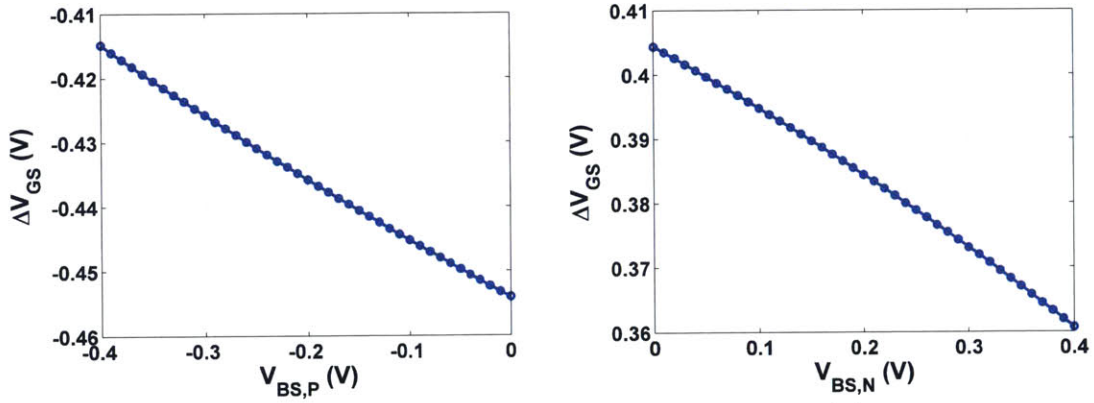


(a)



(b)

Figure 4-9: (a) PMOS and (b) NMOS flipped voltage follower for generation of V_{REFP} and V_{REFM}, respectively.



(a) (b)

Figure 4-10: Change in gate-to-source voltage in the input transistor as bulk voltage is applied in the (a) PMOS and (b) NMOS FVF.

V_{REFP} and V_{REFM} with varying V_{BS} in the input transistor is shown in Figure 4-10. For every Δ10mV in $|V_{BS}|$, the $|V_{GS}|$ varies by 1mV. Therefore, any $\sqrt{\frac{KT}{C}}$ noise voltage added by the bulk biasing capacitance is reduced by a factor of 10 and the

capacitance for the bulk biasing can be scaled down by a large factor compared to the MDAC sampling capacitance, making the area penalty negligible. Throughout the ADC, all PMOS and NMOS level-shifting buffers share the same V_{BIASP} and V_{BIASM}, respectively.

Process variation leads to reference voltage mismatch since each pipelined stage generates its own independent reference voltage in the VGRB technique. If the reference voltage tuning is not addressed, the reference voltage mismatch can introduce nonlinearity in the ADC. Simply increasing the transistor sizes of the level-shifting buffer to minimize process variation results in high parasitic capacitance and degrades the closed-loop bandwidth of the MDAC. Instead, the current through the NMOS level-shifting buffer is controlled to vary its V_{GS}, which in turn adjusts the reference voltage. To achieve fine tuning in the reference voltages and compensate process variation, current is controlled with a 6-bit DAC in the first stage NMOS FVFs, a 5-bit DAC in the second stage NMOS FVFs, and a 4-bit DAC in the third and fourth stage NMOS FVFs. Figure 4-11 shows the tuning of V_{REF} in the front two stages as a function of the DAC current control code. An automatic V_{REF} tuning loop was not implemented for this proof of concept chip, but the output of the reference buffer can be compared to the desired reference, and a feedback loop can increase or decrease the current to keep the V_{GS} constant.

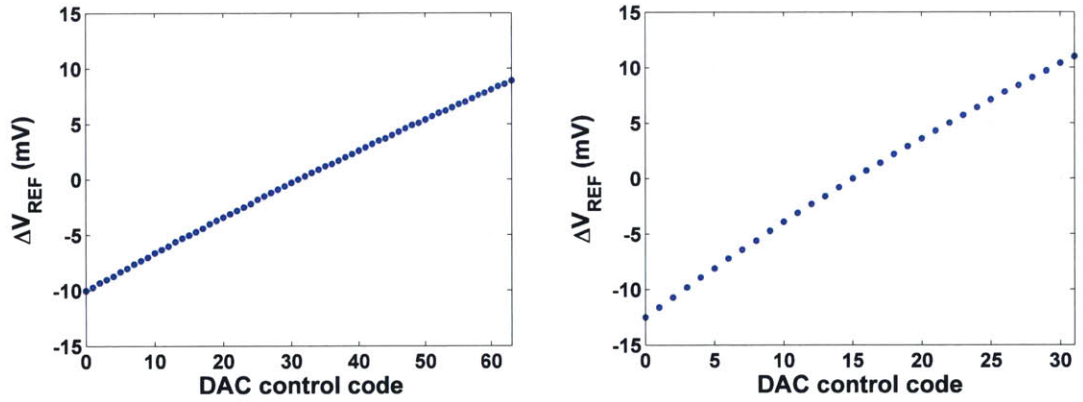


Figure 4-11: Reference voltage tuning as a function of the DAC current control code in the (a) first stage and (b) second stage.

4.1.7 Clock Generation

The clock generation circuit is shown in Figure 4-12. The differential to single-ended (D2S) amplifier converts the differential clock signal to a single-ended signal, Φ_{clk}. After a fixed delay of t_d, the non-overlapping clock generates Φ_1 and Φ_2. The sampling clock Φ_{1se} is generated in a separate path. The rising edge of Φ_1 and the falling edge of Φ_{clk} sets the rising and falling edge of Φ_{1se}, respectively. The falling edge of Φ_{1se} corresponds to the sampling moment in the first pipelined stage and low jitter is required to minimize SNR degradation. Therefore, a few logic gate delays are used from the falling edge of Φ_{clk} to the falling edge of Φ_{1se}. A delay cell separates the falling edges of Φ_{1se} and Φ_1. Φ_1 and Φ_2 signals are distributed to all pipelined stages.

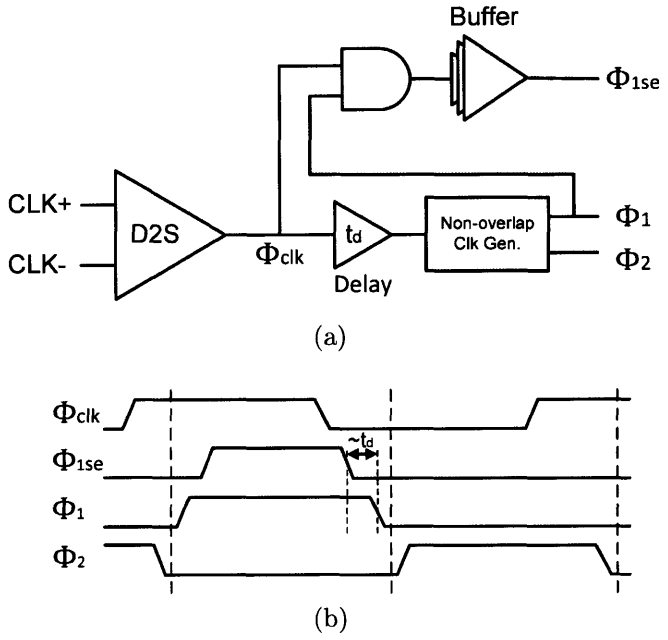


Figure 4-12: (a) Clock generation circuit and its (b) timing operation.

4.1.8 Sub-ADC

A flash ADC is used as the sub-ADC in the pipelined stage. The 3.9-bit flash ADC in the first stage with 14 decision levels is shown in Figure 4-13. The sampling process is identical to that of the MDAC. To minimize the dynamic offsets produced by the timing mismatch in the sampling network between the MDAC and the sub-ADC, the

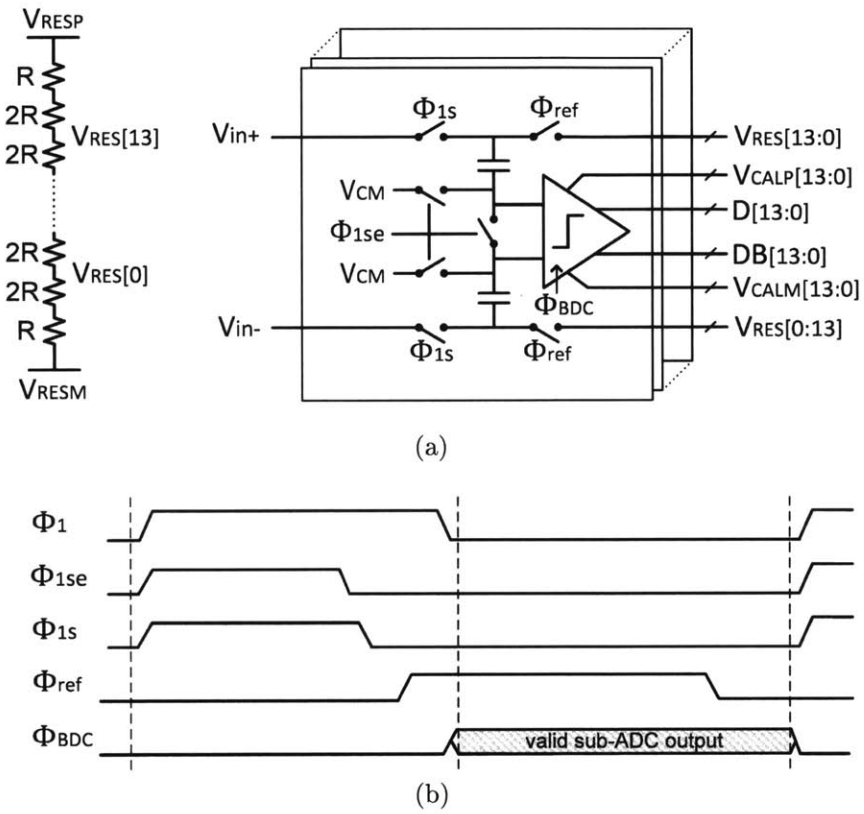


Figure 4-13: (a) Sub-ADC of the first pipelined stage and (b) corresponding operation timing.

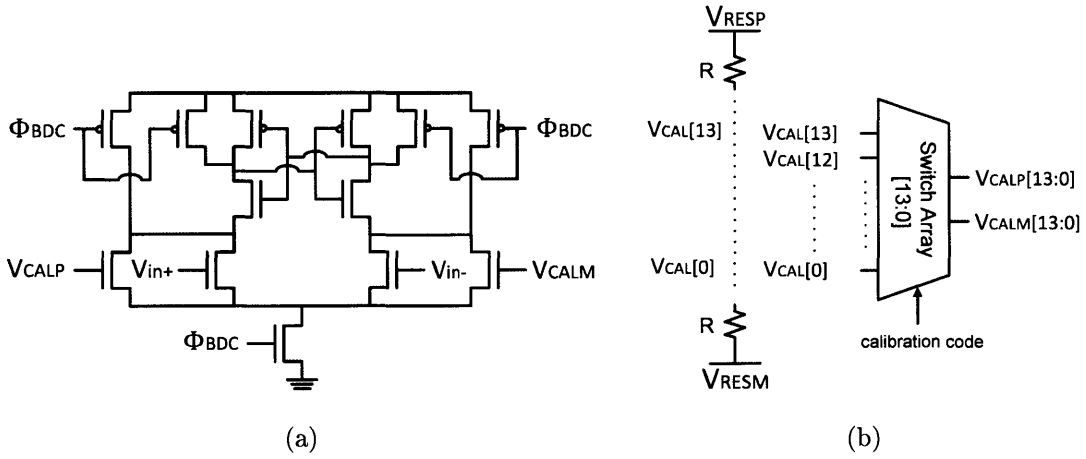
sub-ADC in the first stage uses unit capacitance and switch sizes identical to those used in the MDAC. The dynamic offset in the second stage and beyond is relatively less serious since both the MDAC and sub-ADC sample a DC signal from the previous stage. Therefore, the sub-ADC unit capacitor is scaled down to 25fF to reduce the capacitive loading to the op-amp in the previous stage.

Bottom-plate sampling occurs at the falling edge of Φ_{1se}. Shortly after sampling, at Φ_{ref} the reference ladder provides the bit-decision threshold levels to the sub-ADC. Enough time is given for the voltages at the input of the comparators to settle before the comparators are enabled at the rising edge of Φ_{BDC}. The comparator delivers the bit decisions to the multiplexer in the MDAC before the charge-transfer phase.

The high voltage gain in the MDAC also amplifies the comparator offset in the sub-ADC. The over-range allows extension in the output swing by $\pm$100mV. The signal gain in the first stage is 8, and therefore a maximum comparator offset of

$3\sigma = \pm 12.5$mV can be tolerated. Comparator offsets are calibrated using calibration voltages V_{CALP} and V_{CALM} to ensure that the amplified residue in the MDAC stays within limits of the over-range correction.

The StrongArm comparator [49] with an extra input pair for calibration in the first stage sub-ADC is shown in Figure 4-14. The calibration input pair is scaled down in size by a factor of five compared with the main input pair. A dedicated resistor ladder generates an array of calibration voltages that are multiplexed into the calibration input pair. These differential calibration voltages control the comparator offsets by a step size of $\pm$8mV up to $\pm$40mV.



(a) (b)

Figure 4-14: (a) First stage sub-ADC StrongArm comparator with offset calibration input pair and (b) resistor ladder and multiplexer for offset calibration.

The sub-ADCs in the second to the fourth stage are identical and have the same structure as the first stage sub-ADC. Each sub-ADC resolves 2-bits and the input transistors in the StrongArm comparators are scaled up for smaller offsets to avoid offset calibration.

4.2 Layout and Floorplan

The routing capacitance of the virtual ground node is bootstrapped to achieve better feedback factor. The bootstrapping is achieved in layout. The floorplan of the a ADC consists of the pipelined stages, clock generator, biasing cell, and four resistor

ladders. The layout and floorplan of the pipelined stages requires the most attention. The capacitor arrays are shielded to to minimize any noise injection and includes dummy metal layers to meet the density rule.

4.2.1 Bootstrapping the Virtual Ground Parasitic Capacitance

In conventional circuits, the routing capacitance between the virtual ground and the substrate degrades the feedback factor. The input-referred noise and charge-transfer error increases, and the bandwidth decreases as a result. In the VGRB technique, the routing capacitance can be bootstrapped away by the level-shifting buffers as shown in Figure 4-15. The level-shifting buffer must drive a slightly larger capacitive load since it now sees the additional parasitic capacitance $C_{p,rout}$ and $C_{p,sub}$. However, $C_{p,rout}$ and $C_{p,sub}$ are typically small compared with the C_1 the level-shifting buffers are designed to drive, thus the additional capacitance is not significant. For the prototype ADC, the NMOS level-shifting buffer is used to bootstrap the routing capacitance since it has a higher transconductance.

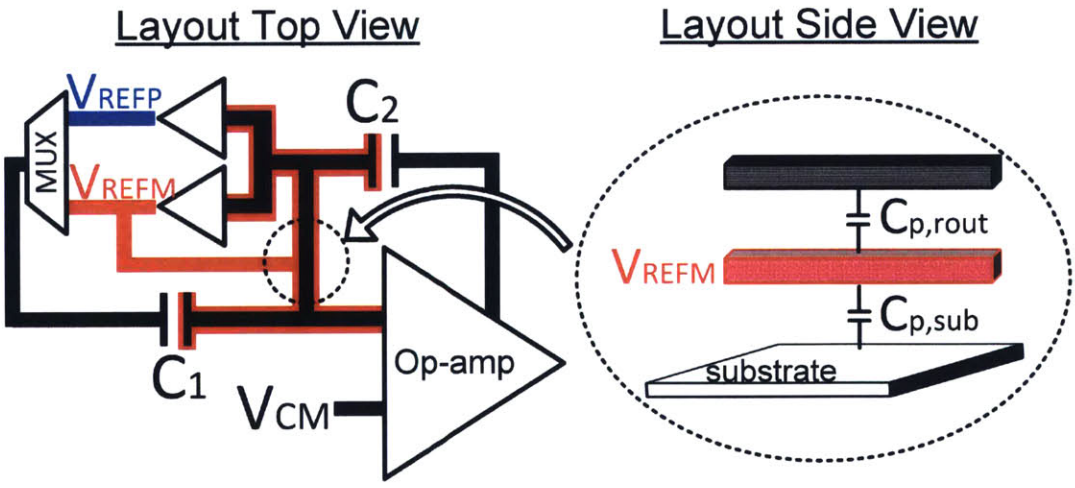


Figure 4-15: The routing of the NMOS level-shifting buffer output underneath the virtual ground node.

4.2.2 Floorplan

The floorplan of the first stage is shown in Figure 4-16. The front-end consists of the bootstrapped input switches, stage clock generator, and the sub-ADC. The sub-ADC output bits are routed to the mux array and the bottom-plate sampling switches. The capacitor array consists of C_1, C_2 and dummy capacitors. The capacitor array is followed by the level-shifting buffers, op-amp, and the bootstrapped switches that flip C_2 around the op-amp for the charge-transfer phase. The second to the fourth stages have identical floor plan and the last stage only consists of the sub-ADC block. To avoid injecting noise into the substrate, P+ substrate guard rings for digital circuits were connected to a clean ground signal not shared with any circuit blocks. Likewise, N-well guard rings were connected to a dedicated clean VDD from off-chip.

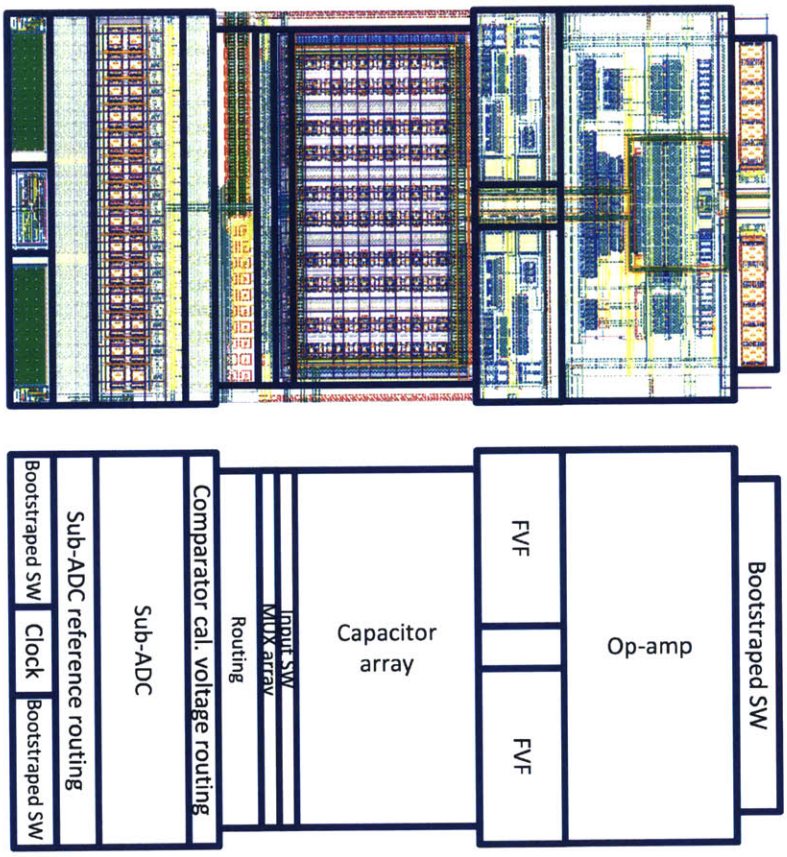


Figure 4-16: Floorplan of the first stage.

The metal-insulator-metal (MiM) capacitor array is shown in detail in Figure 4-17. Metal layer1 to layer9 were stacked with via connections along the perimeter to

shield the capacitor array. Within the capacitor array, dummy capacitors surround the core capacitors. To meet the density requirements, poly layer and dummy metals from layer1 to layer3 were placed underneath each capacitor array. Also, dummy metal layer9 was necessary and was placed above the routing wires. The perimeter metal layers, dummy metals, and dummy capacitors are all connected to the ground node.

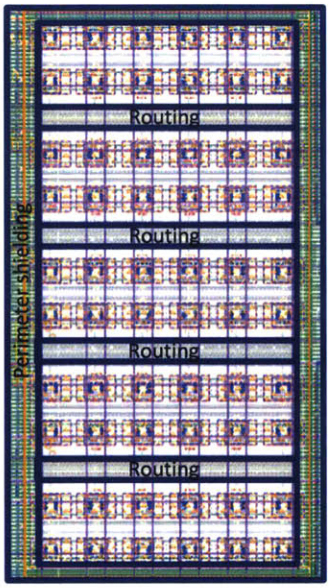


Figure 4-17: Floorplan of first stage capacitor array.

There are four resistor ladders in the ADC core shown in Figure 4-18. Reference 1 and 2 are used in the first stage sub-ADC and the comparator offset calibration, respectively. The sub-ADCs in the second to the fourth stage share reference 3. The fifth stage uses reference 4. Reference 1 and 3 are designed to have low time constant using minimum decoupling capacitance for fast settling. On the other hand, in reference 2 and 4, each node has a decoupling capacitance and the time constant is larger. Although it takes longer time for the reference voltages to settle once an instant current injection is applied, the decoupling capacitance limits the initial voltage spike and sufficient settling is obtained while reducing current in the reference ladders. The biasing cell is located on the left side of the ADC core.

The op-amps, level-shifting buffers, and digital logic and sub-ADC have separate power supplies in Figure 4-19. The supply for the op-amps and the level-shifting

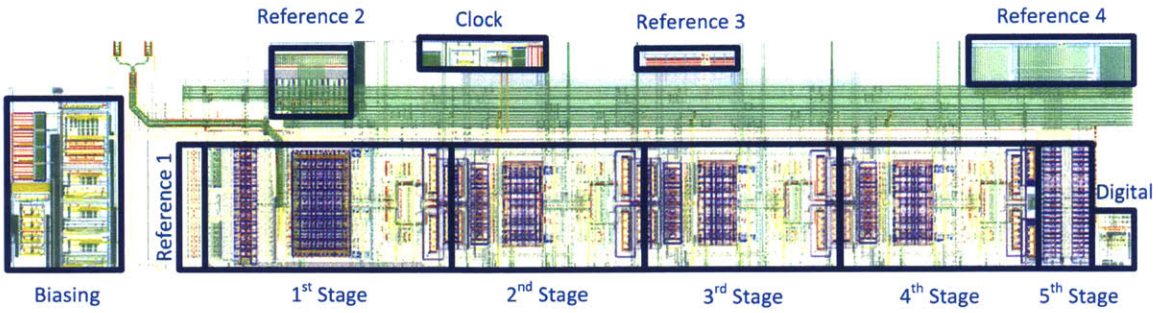


Figure 4-18: Floorplan of the ADC core.

buffers are VDDA and VDDAB, respectively. Both share the same analog ground, GND. The digital logic and sub-ADC share VDDD and GNDD. The supply rails are routed in the top metal layer along the pipelined stages. The VDDA is routed closest to the core, then followed by the VDDAB and VDDD.

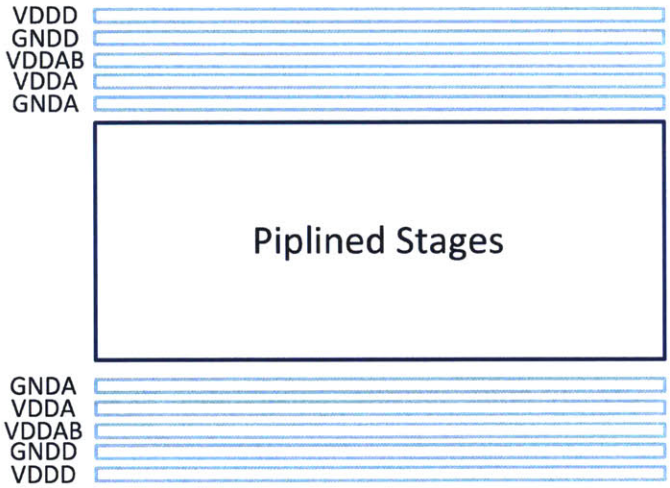


Figure 4-19: Routing of the supply rails.

4.3 Feedback Factor with Parasitics

The parasitic capacitances in Figure 3-4 are listed in Table 4.1. The effect of the level-shifting buffer gain, G_b, on the feedback factor was detailed in Chapter 3. An ideal unity gain is desired to completely bootstrap away C_1. In simulation, both level-shifting buffer was found to have a gain of 0.91. Therefore, 840fF$\times$0.09 = 75.6fF of C_1 effectively appears at the virtual ground node.

Source		Capacitance (fF)	Contribution	Total (fF)
Residual C_1	C_1	840	$(1-G_b)C_1$	75.6
PMOS FVF $C_{i,b}$	C_{gs}	140.8	$(1-G_b)C_{gs}$	64.9
	C_{gb}	6.6	$(1-G_b)C_{gb}$	
	C_{gd}	51.6	C_{gd}	
NMOS FVF $C_{i,b}$	C_{gs}	50.5	$(1-G_b)C_{gs}$	22.8
	C_{gb}	4.5	$(1-G_b)C_{gb}$	
	C_{gd}	17.9	C_{gd}	
Op-amp $C_{i,oa}$	C_{gs}	54.4	C_{gs}	78.0
	C_{gb}	3.4	C_{gb}	
	C_{gd}	20.2	C_{gd}	
Routing C_w	$C_{p,rout}$	70.5	$(1-G_b)C_{p,rout}$	56.9
	$C_{p,sub}$	21.3	$C_{p,sub}$	
	C_{cc1}	21.5	C_{cc1}	
	C_{cc2}	3.9	$2C_{cc2}$	

Table 4.1: List of the parasitic capacitances that degrade the feedback factor in the first stage.

The input capacitance of the FVF, $C_{i,b}$, consists of the gate-to-drain capacitance, C_{gd}, the gate-to-bulk capacitance, C_{gb}, and the gate-to-source capacitance, C_{gs}. The effective parasitic capacitance, C_{FVF}, from each level-shifting buffer is calculated as

$$C_{FVF} = (1 - G_b)(C_{gs} + C_{gb}) + C_{gd}. \tag{4.1}$$

The C_{gd} component directly adds parasitic capacitance to the virtual ground node, but C_{gs} and C_{gb} only contribute $0.09 \times (C_{gs} + C_{gb})$. Therefore, C_{gd} causes bigger feedback factor degradation even though C_{gs} is much larger. In the PMOS FVF, C_{gs} and C_{gb} contribute 13.3fF out of the 64.9fF, and C_{gd} contributes the remaining 51.6fF. In the NMOS FVF, C_{gs} and C_{gb} contribute only 4.9fF out of the 22.8fF, and C_{gd} contributes the remaining 17.9fF. The PMOS FVF has a larger transistor size than the NMOS FVF and contributes larger parasitic capacitance. The PMOS and NMOS level-shifting buffers combined contribute 87.7fF.

The op-amp input capacitance $C_{i,oa}$ is 78.0fF. The op-amp C_{gs} contributes the most with 54.4fF. There is little miller effect amplification in the input transistor C_{gd} since the impedance looking into the cascode device of the input transistor is low due to the gain-boosting op-amp.

The routing capacitance, C_w, largely consists of the capacitance to the reference voltage, $C_{p,rout}$, substrate capacitance, $C_{p,sub}$, and coupling capacitance C_{cc1} and C_{cc2}. $C_{p,rout}$ is largely boostrapped away as explained in the previous section. However, $C_{p,sub}$, is not completely eliminated despite routing the negative reference voltage underneath the virtual ground node. This is largely due to the fringing capacitance which can be further reduced by widening the routing trace of the reference voltage. C_{cc1} is the coupling capacitance between the virtual ground node and other signal traces such as the clock, and common-mode voltage, and ground signal. Most of C_{cc1} comes from the multiplexer array. C_{cc2} is the coupling capacitance formed between the two virtual ground nodes.

Adding all these capacitances together, the total parasitic capacitance at the virtual ground node is C_p =298.2fF and the feedback factor is $\beta = 0.3$. Further optimization can improve the feedback factor drastically. For an improved level-shifting buffer gain of $G_b = 0.95$ via cascoding the current sources, the portion of C_1 that is not bootstrapped is reduced to 42fF and the $C_{gs} + C_{gb}$ in the PMOS and NMOS level-shifting buffers contribute a negligible 7.4fF and 2.8fF, respectively. Also, bootstrapping the drain of the input transistor is critical in reducing the impact of C_{gd} on the feedback. The routing capacitance can be significantly reduced as well. The effective contribution of $C_{p,rout}$ is also very little for near unity G_b. $C_{p,sub}$ and C_{cc1} can be reduced by shielding the virtual ground node with the reference voltage more aggressively, and C_{cc2} can be minimized by increasing the separation distance between the two virtual ground nodes. For the same op-amp input capacitance, if G_b is improved to 0.95 and the C_{gd} in the level-shifting buffers is bootstrapped away, feedback can be improved to $\beta \approx 0.5$

4.4 Noise Comparison with Conventional Circuit

The precise noise analysis depends on the implementation. In this section, the noise contribution from the op-amp and the level-shifting buffers in the first stage is compared with the case in the conventional circuit that has the same bandwidth. The

additional loading capacitance from the sub-ADC sampling network is not considered and the comparison is made with reasonable simplifying assumptions.

4.4.1 Conventional Circuit

In the conventional circuit, the sampling capacitance in the second stage, C_L, is assumed to be scaled by a factor of four compared to the sampling capacitance, $C_1 + C_2$, in the first stage. Although 3.9-bits are resolved in the first stage and more aggressive capacitor scaling is possible for better power optimization, often the capacitance sizing is dictated by the capacitor matching requirement to ensure DAC linearity [50]. For a signal gain of $G_s = 8$, the feedback factor is $\beta = \frac{1}{10}$ considering the parasitic capacitance at the virtual ground node. Given $C_1 = 7C_2$, $C_p = 2C_2$ and the total load capacitance is

$$C_T = \frac{C_2(C_1 + C_p)}{C_1 + C_2 + C_p} + C_L = 2.9C_2. \tag{4.2}$$

Assuming $g_m = g_{mp,oa} = g_{m,noa}$ in Equation 2.33, the op-amp noise power referred to the ADC input is

$$\overline{v_{n,oa,in}^2} = \frac{16kT\gamma n_f}{g_m} \frac{BW}{4} \frac{1}{\beta^2} \frac{1}{G_s^2} \tag{4.3}$$

$$= 0.216 \frac{kT\gamma n_f}{C_2}. \tag{4.4}$$

with BW$=\frac{g_m}{29C_2}$ from Equation 2.28. It can also be assumed that $g_m = g_{mp,b} = g_{mn,b}$ for the transconductance of the buffer. In this case, the time constant at which the reference buffer charges C_1 is $\frac{7C_2}{g_m}$, which is faster than the time constant at which the op-amp output settles in closed-loop $\frac{29C_2}{gm}$, and the closed-loop bandwidth is largely limited by the op-amp bandwidth. Based on Equation 2.47, the reference buffer noise power is referred to the ADC input,

$$\overline{v_{n,b,in}^2} = \frac{16kT\gamma}{g_m} \frac{N^2}{12} \frac{BW}{4} \frac{1}{G_s^2}. \tag{4.5}$$

Since $N = 14$ in the prototype,

$$\overline{v_{n,b,in}^2} = 0.035\frac{kT\gamma}{C_2} \tag{4.6}$$

The total input-referred noise power in the charge-transfer phase is therefore

$$\overline{v_{n,in}^2} = \overline{v_{n,oa,in}^2} + \overline{v_{n,b,in}^2} = \frac{kT\gamma}{C_2}\left(0.216n_f + .035\right). \tag{4.7}$$

The noise contribution of the reference buffers is insignificant because their noise is partially canceled by the differential architecture and further filtered by the op-amp closed-loop bandwidth, and because their noise gain is much lower than signal gain.

4.4.2 Virtual Ground Reference Buffer Circuit

In the VGRB implementation, the feedback factor is assumed to be approximately 0.3 as in the prototype, although it can be further improved in future designs. The transconductances $g_{mp,b}$ and $g_{mn,b}$ are assumed to be identical to those in the reference buffer in the conventional circuit for straightforward comparison. The load capacitance C_L is assumed to be identical as well. However, the effective capacitance loading the virtual ground node is $C_p = \frac{7}{3}C_2$ for a $\beta = 0.3$. Now the total load capacitance is

$$C_T = \frac{C_pC_2}{C_p + C_2} + C_L = 2.7C_2. \tag{4.8}$$

Due to the larger feedback factor and reduced load capacitance, the input transconductance of the op-amp can be reduced for the same closed-loop bandwidth as that of the conventional circuit. It can be shown that the op-amp transconductance can be reduced to $g'_m = 0.31g_m$ and the op-amp power consumption can be reduced by the same factor. The op-amp noise power referred to the ADC input is

$$\overline{v_{n,oa,in}^2} = \frac{16kT\gamma n_f}{g'_m}\frac{BW}{4}\frac{1}{\beta^2}\frac{1}{G_s^2} \tag{4.9}$$

$$= 0.077\frac{kT\gamma n_f}{C_2}. \tag{4.10}$$

Note that the noise referred to the ADC input is much lower than that of the conventional circuit in Equation 4.4 due to the increased feedback factor, even at much lower power consumption.

Unlike the conventional circuit, noise from the level-shifting buffers does not partially cancel. From Equation 3.17, the noise from the level-shifting buffers is

$$\overline{v_{n,b,in}^2} = \frac{32KT\gamma}{g_m}\frac{N^2}{12}\frac{BW}{4}\frac{1}{G_s^2} \tag{4.11}$$

$$= .07\frac{kT\gamma}{C_2} \tag{4.12}$$

for $g_m = g_{mp,b} = g_{mn,b}$. The noise bandwidth is still limited by the op-amp bandwidth. The total input referred noise power is

$$\overline{v_{n,in}^2} = \frac{KT\gamma}{C_2}\left(0.077n_f + .07\right). \tag{4.13}$$

Compared to the conventional circuit the op-amp power is reduced by a factor of 3.2 due to the reduced op-amp transconductance requirement, and the noise contribution from the op-amp is reduced by a factor of 2.8. The reference buffer noise contribution increases due to the lack of the partial noise cancellation, but the overall noise is still much lower in the proposed circuit. Even in the conservative case of $n_f = 1$, the total input-referred noise power is reduced by a factor of 1.7. It is interesting to note that with $\gamma = \frac{2}{3}$ in strong inversion, the total noise power during the charge-transfer phase is $\frac{kT}{10C_2}$, which is lower than the sampling noise $\frac{kT}{8C_2}$. In reality, the op-amp in the conventional circuit will likely have higher n_f since more devices are needed to achieve the required higher op-amp open-loop gain, and the input-referred noise power as well as op-amp power consumption in the VGRB technique become even more favorable. Moreover, the feedback factor in the proposed circuit can be improved further, which will increase the improvement factors in both the power consumption and noise.

Chapter 5

Measurement Results

This chapter opens with the measurement setup for the implemented 12-bit 250MS/s pipelined ADC. This includes details on the testing equipments and PCB components used, as well as the chip bonding. The measurement includes the comparator offet calibration and the tuning in the reference voltages. An ENOB of 10.84-bits and 10.62-bits are achieved for low input signal frequency and near Nyquist input signal frequency, respectively. The calibration of the reference voltages generated by the level-shifting buffers is critical in improving the SNDR to this level. Lastly, the chapter compares the performance between the prototype chip and other published single-channel ADCs that have similar performance specifications.

5.1 Measurement Setup

The prototype chip was fabricated in a TMSC 65nm LP technology. The die, whose core occupies $0.59mm^2$, is shown in Figure 5-1. Decoupling capacitance is placed throughout the remaining area. The bonding diagram of the chip is shown in Figure 5-2. Multiple bondwire connections are made for the supply pins and the common-mode voltage pin to reduce bondwire inductance. The chip is placed directly on the PCB using Chip-on-Board (COB) technology to further minimize the bondwire inductance. All ground pads are downbonded.

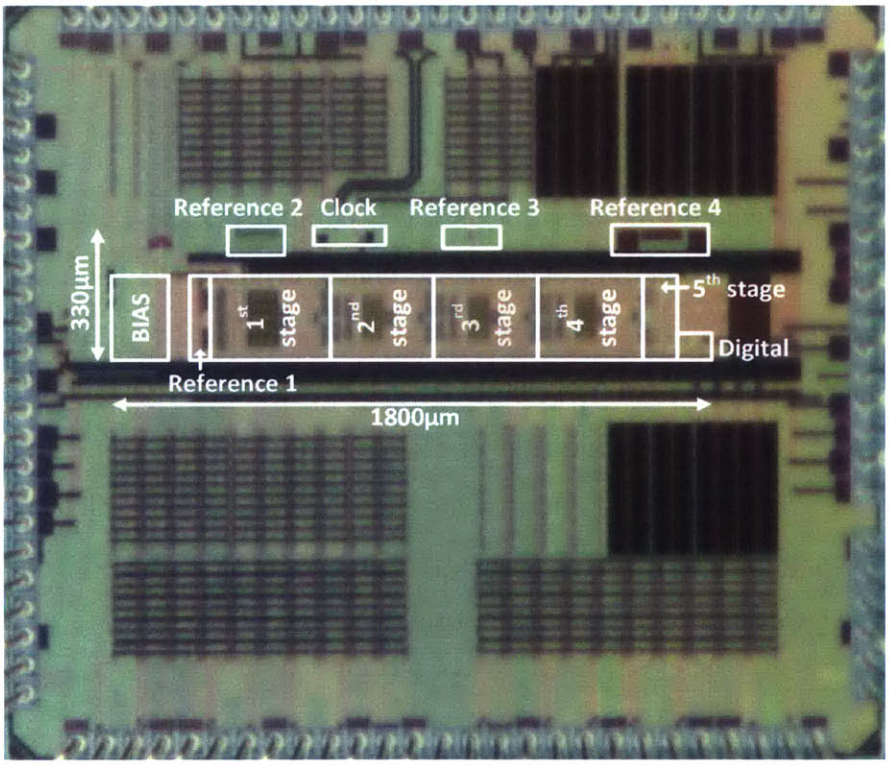


Figure 5-1: Die photograph of the 12-bit 250MS/s pipelined ADC.

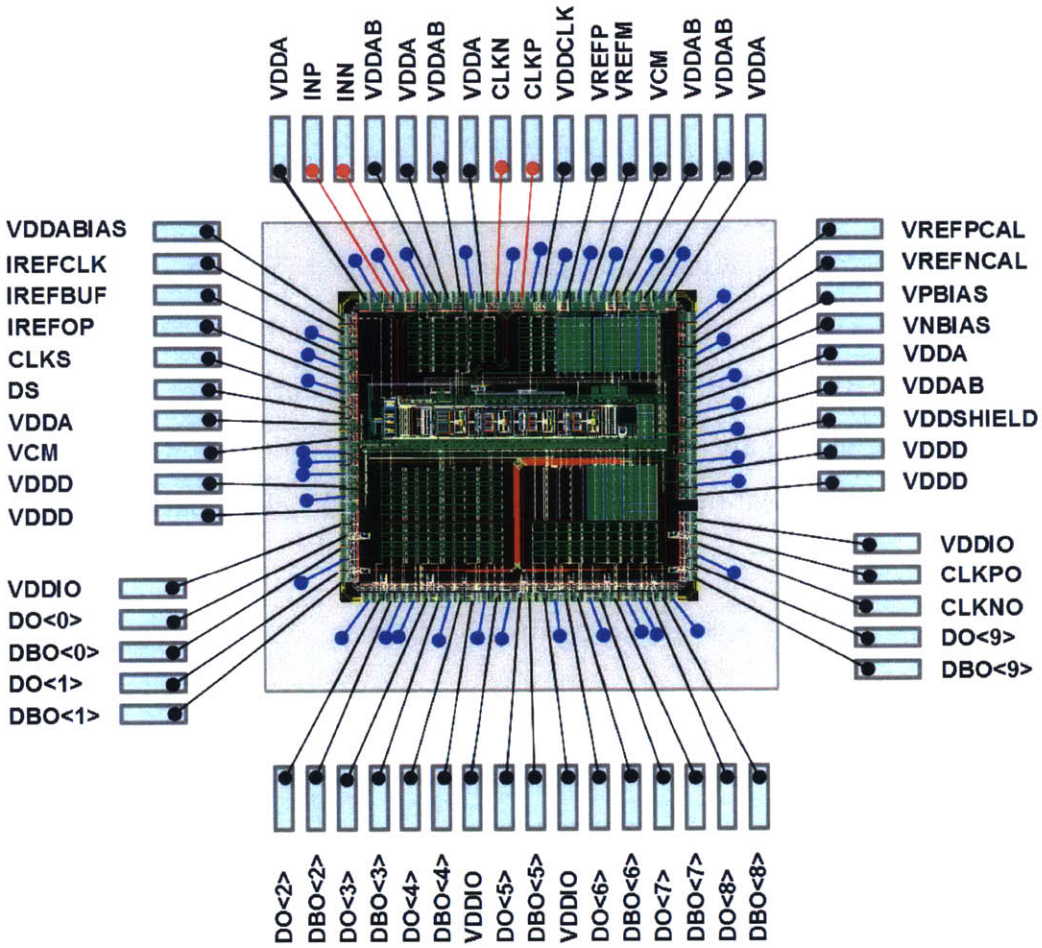


Figure 5-2: Die bonding diagram for COB.

The test setup is shown in Figure 5-3. The input signal from a signal generator (Agilent 8644B) is bandpass filtered to eliminate the harmonics and reduce the signal noise. The single-ended input signal is converted to a differential signal on the PCB using two cascaded transformers (TC1-1-13+, Mini-Circuits). The double transformer configuration has a much improved phase imbalance and reduces the second-order distortion. The clock signal from the signal generator (HP 83732B) is also bandpass filtered to eliminate wide-band noise. In addition, the clock signal is driven at high amplitude and is clamped by back-to-back connected diodes (HSMS2812) to make the clock edges as sharp as possible, reducing the sampling jitter. The singled-ended clock signal is converted to a differential signal on the PCB using a transformer (TC1-

1-13+, Mini-Circuits). The LVDS data outputs are captured on the logic analyzer (TLA 715) and processed in MATLAB. The registers for the on-chip control bits are loaded from an arbitrary function generator (Tektronix AFG3102), that is controlled by a PC. The DC power supply (Agilent E3646) provides the supply voltage to the PCB board, and separate low dropout voltage linear regulators (LT3021) are used for different on-chip power supplies and references. A total of 11 regulators are used to give maximum flexibility: VDDA, VDDAB, VDDCLK, VDDD, VDDIO, VCM, VRESP, VRESM, VBIASP, VBIASM, and VCMCLK. The current for the op-amp and the level-shifting buffers are sourced by BJT (MMBT3904) devices while the current source for the differential-to-single-ended amplifier in the clock path is sourced by LM334M.

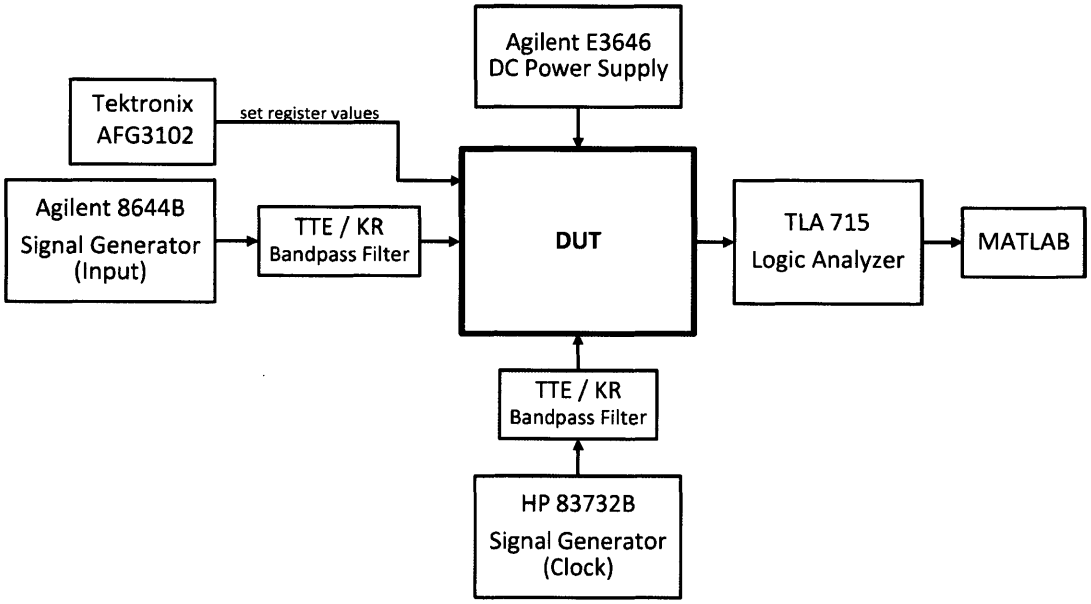


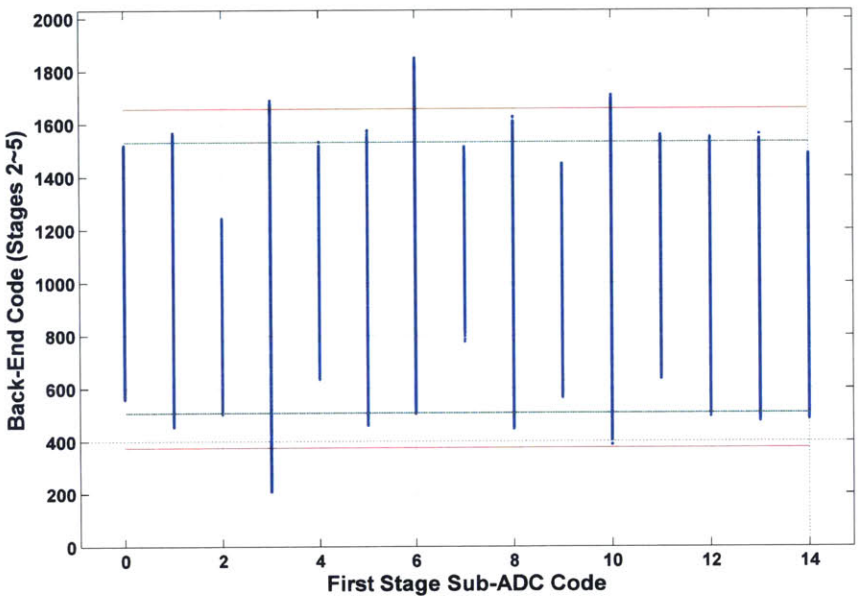
Figure 5-3: Test setup for chip measurement.

5.2 Chip Performance

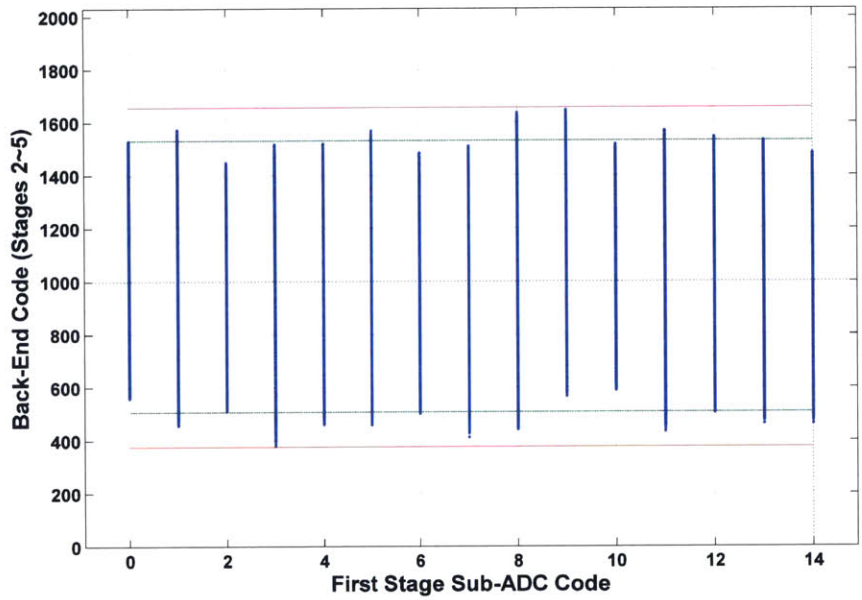
The full-scale input signal range is approximately 1.5 Vpp differentially. Foreground capacitor mismatch calibration is applied off-chip and the calibration coefficients are frozen throughout the measurements. During the normal conversion, the capacitor mismatch calibration requires coefficient additions only, and is estimated to consume 100μW if implemented on-chip.

For each sub-ADC code in the first stage, the sub-ADC codes from the second stage to the last stage are combined to construct the back-end codes. The results are plotted in Figure 5-4. The back-end code corresponds to the digital representation of the first stage residue. The ideal back-end code ranges from 507 to 1531, which is a 10-bit resolution code range; the pipelined ADC resolves 13.9-bits before any truncation. Over-range correction is applied for back-end codes that extend to 379 and 1659. If the comparators in the first stage sub-ADC are not calibrated, then the back-end code has a wider range as shown in Figure 5-4a. This causes linearity degradation since the telescopic op-amp is not able to handle such residue output without adding distortions. Calibrating the comparator offsets limits the first stage residue and keeps the back-end codes to within the over-range as shown in Figure 5-4b.

In Figure 5-5, the ADC back-end code constructed by combining the sub-ADC codes from the third stage to the last stage is plotted for each sub-ADC code in the second stage after comparator offset calibration in the first stage. The ideal back-end code ranges from 123 to 379, an 8-bit resolution code range, and over-range is applied for any back-end code that extends to 91 and 411. The back-end codes are within the over-range without applying comparator offset calibration in the second stage. This is because the transistor input pair in the comparator is scaled up to reduce process variation, and also the over-range is larger than in the first stage. Notice that the second stage sub-ADC codes do not span the full range from 0 to 6 by design. The second stage sub-ADC code of either 0 or 6 corresponds to first stage residue that extends beyond the over-range. Since the first stage residue is within the over-range, the second stage sub-ADC codes are limited to between 1 and 5.



(a)



(b)

Figure 5-4: The back-end code (stages 2-5) range for each sub-ADC code in the first stage (a) before comparator offset calibration and (b) after comparator offset calibration.

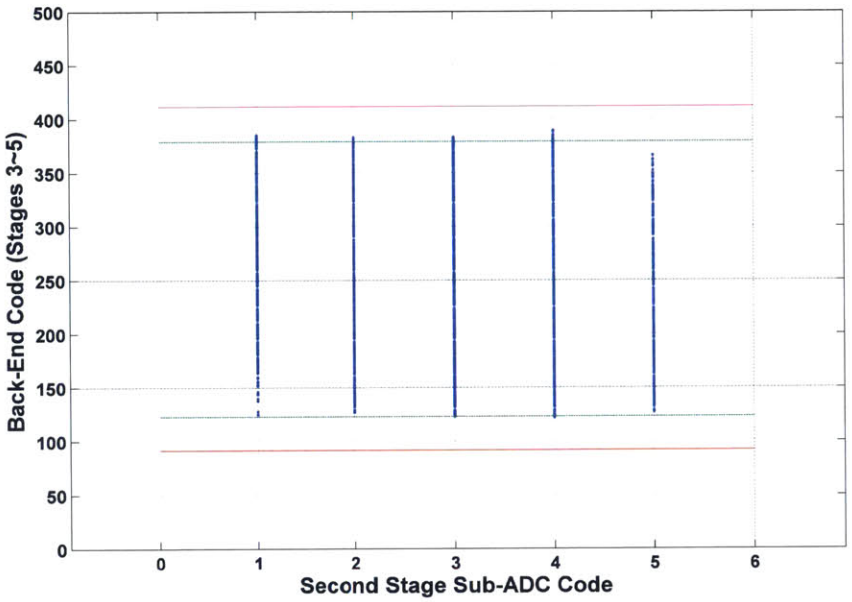
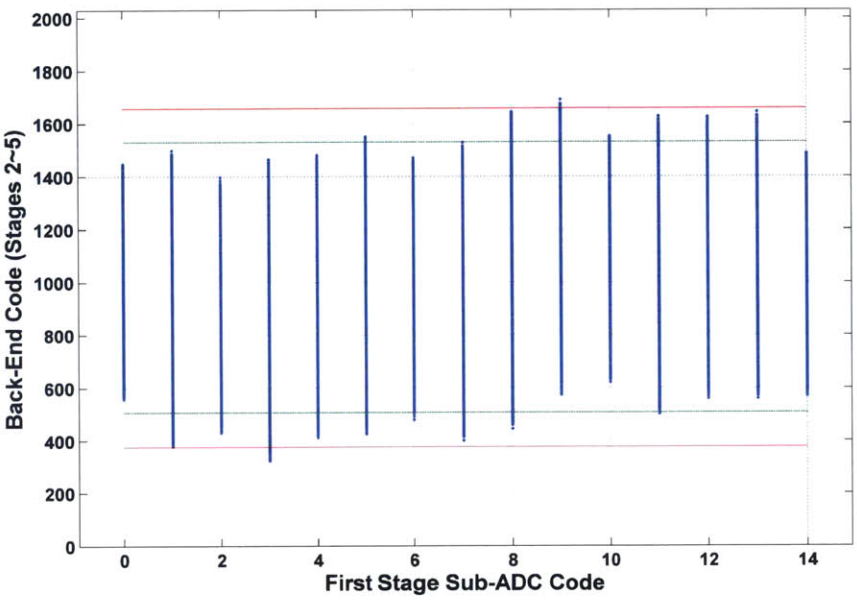
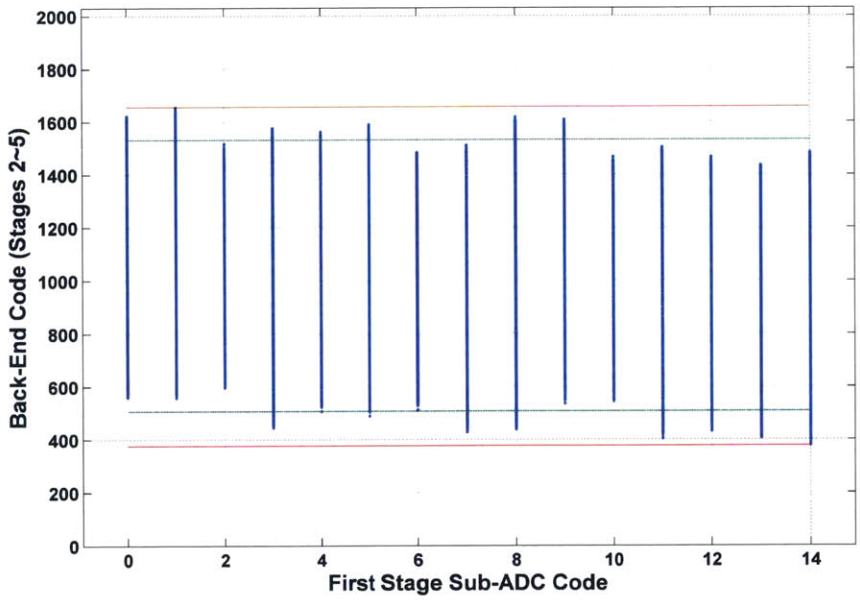


Figure 5-5: The back-end code (stages 3-5) range for each sub-ADC code in the second stage after comparator offset calibration in the first stage sub-ADC.

Although not as critical as the inter-stage reference voltage matching, the reference voltage for the resistor ladders in the sub-ADC also needs to match to the reference voltages generated by the level-shifting buffers. In Figure 5-6a, the reference voltage for the resistor ladders is set 10mV larger than the reference voltage set by the level-shifting buffers. This translates to an upward skew in the back-end code plot. On the other hand, in Figure 5-6b, the reference voltage for the resistor ladders is set 10mV smaller than the reference voltage set by the level-shifting buffers and results in a downward skew in the back-end code plot. As long as the back-end code with skewing is within the over-range, the mismatch does not degrade the linearity of the ADC. However, over-range is limited in applications with low supply voltage and therefore it is important not to dismiss the issue entirely.



(a)



(b)

Figure 5-6: The back-end code (stage 2-5) range for each first stage sub-ADC code with the reference voltage for the resistor ladders set (a) 10mV larger and (b) 10mV smaller than the reference voltage set by the level-shifting buffers.

Figure 5-7 shows the measured linearity of the ADC before calibrating the reference voltages. The DNL and INL are -0.85/+0.59 LSB and -5.40/+7.31 LSB, respectively. The 14 vertical drops in the INL indicate mismatch in the reference voltage between the first and the second stage. In the prototype, the reference voltage is systematically lower in the first stage than in the second stage. To resolve the difference, the differential reference voltage in the first stage is increased by increasing the current in the first stage NMOS level-shifting buffers. Also, the differential reference voltage in the second stage is decreased by decreasing the current in the second stage NMOS level-shifting buffers. Within each 14 segments in the INL plot, additional vertical drops exist that arise from the differential reference voltage mismatch between the second and third stage, as well as the third and the fourth stage.

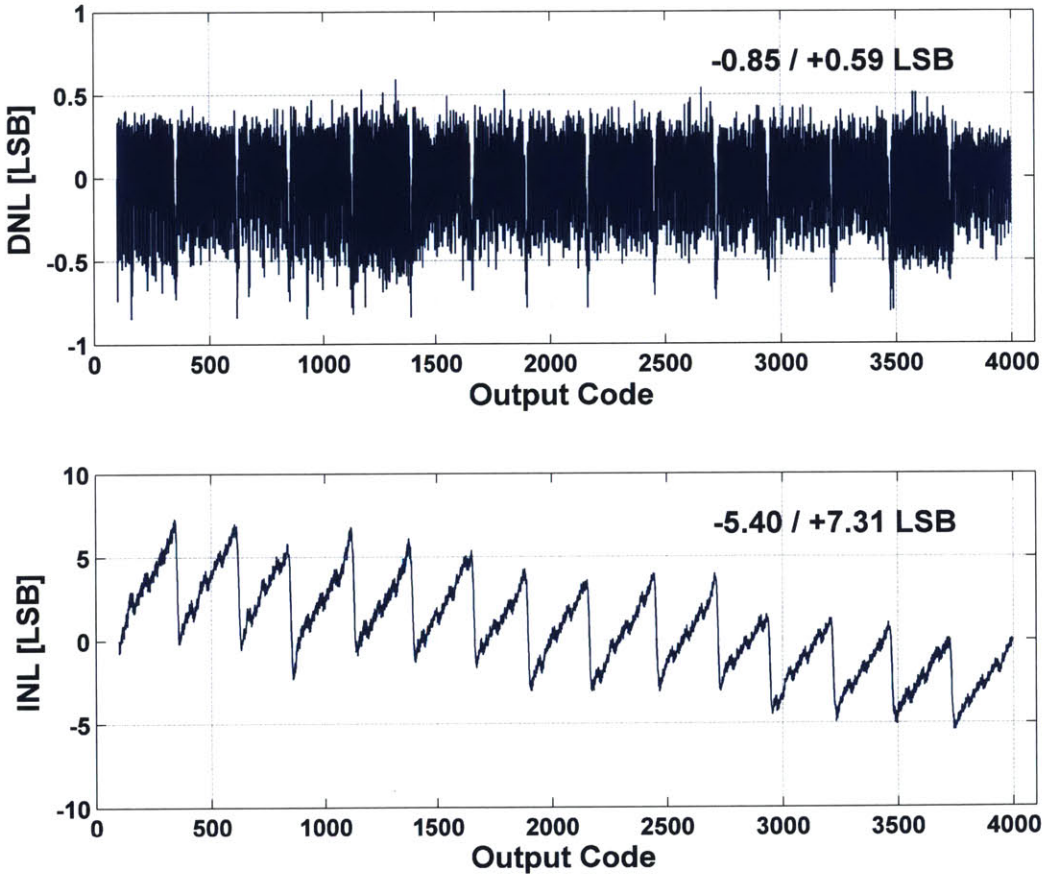


Figure 5-7: Measured DNL/INL of the ADC without calibration.

The mismatch is calibrated by adjusting the current level in the NMOS level-shifting buffers in the corresponding stages. Significant performance improvement is obtained after calibration. The DNL and INL are within -0.85/+0.52 LSB and -1.50/+1.33 LSB, respectively, as shown in Figure 5-8. Although automatic foreground or background calibration of references is relatively straightforward, it is not implemented in the prototype for simplicity. In addition to the reference voltage mismatch, capacitor mismatch in the MDAC also causes vertical INL drops. The difference is that reference voltage mismatch contributes constant 14 vertical INL drops while the capacitor mismatch causes varying 14 vertical drops. After applying standard capacitor mismatch calibration, the DNL and INL are within -0.86/+0.52 LSB and -0.90/+1.08 LSB, respectively, as shown in Figure 5-9.

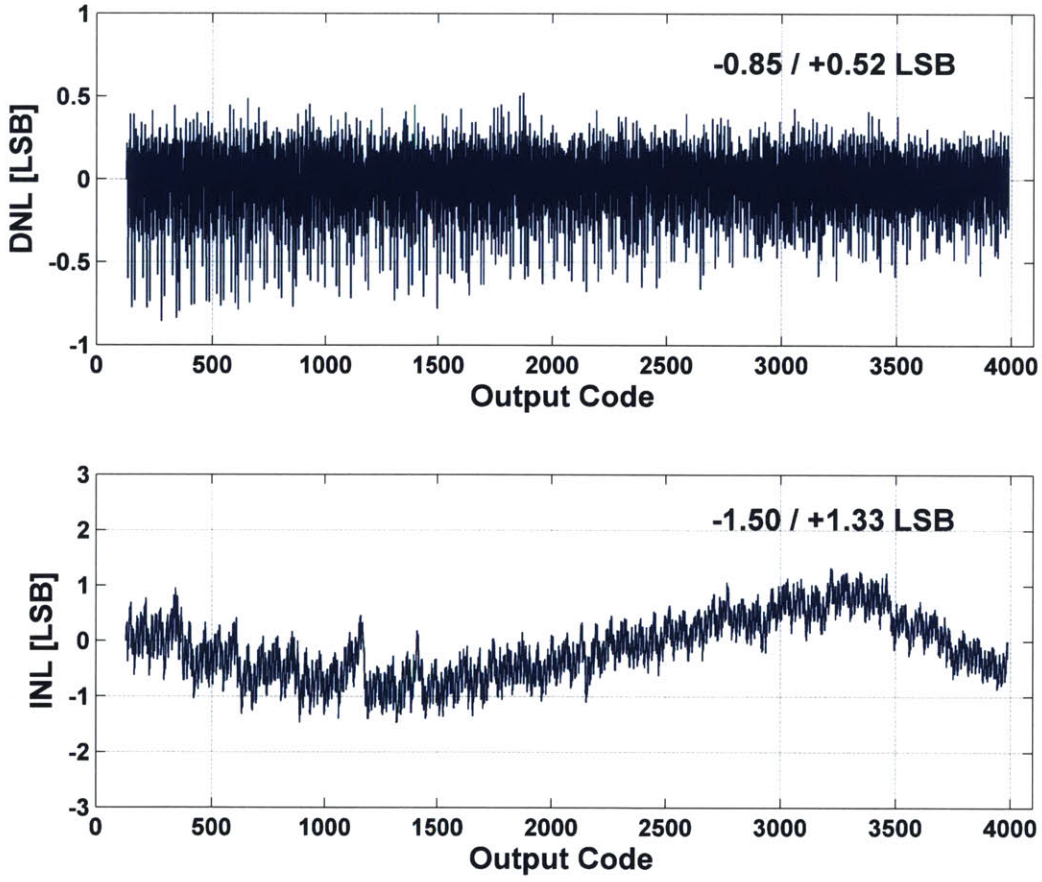


Figure 5-8: Measured DNL/INL of the ADC after reference voltage mismatch calibration only.

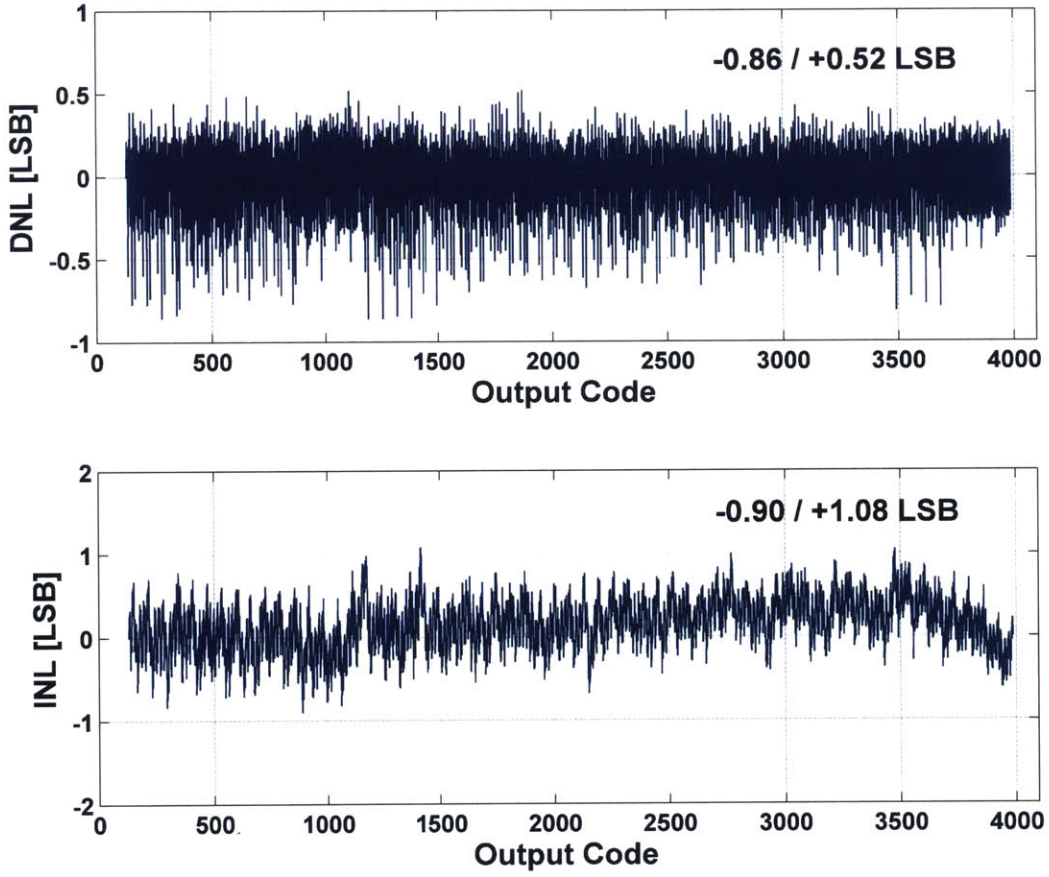


Figure 5-9: Measured DNL/INL of the ADC after reference voltage mismatch and capacitor mismatch calibration.

Figure 5-10 shows the output spectra with 12.1MHz input frequency and grounded input signal at the sampling rate of 250MS/s before capacitor mismatch calibration. The SFDR is limited to 72.9dB. Figure 5-11 shows the output spectra with input frequencies of 12.1MHz and 121.8 MHz at the sampling rate of 250MS/s after capacitor mismatch calibration. At 12.1MHz, SNDR of 67.0dB (10.84-b ENOB) and SFDR of 84.6dB are achieved. At 121.8MHz, the SNDR degrades by 1.3dB to 65.7dB, which is believed to be due to the sampling clock jitter.

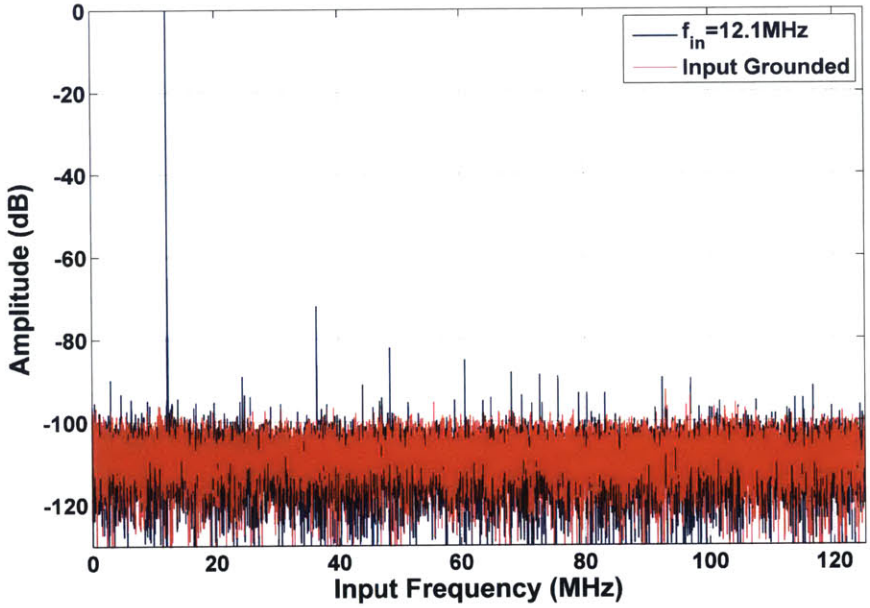
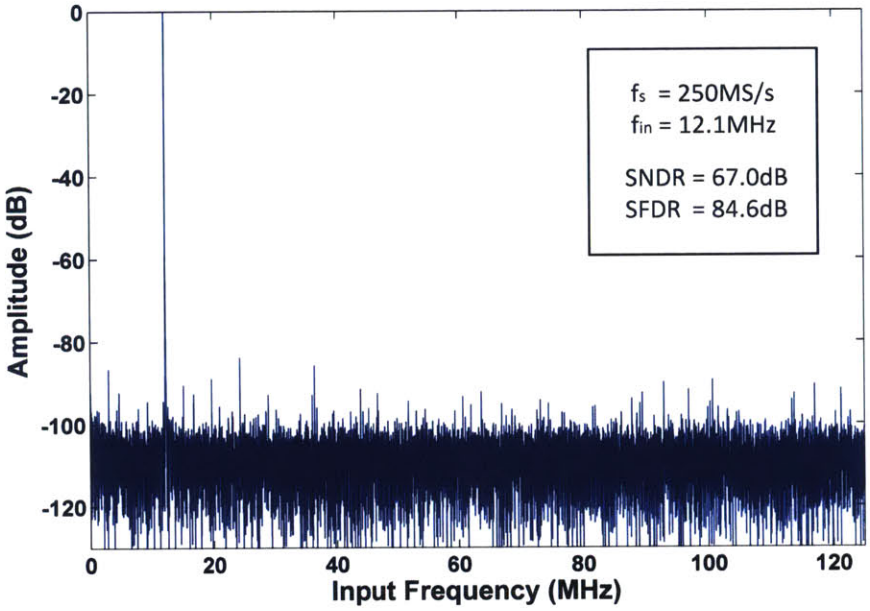
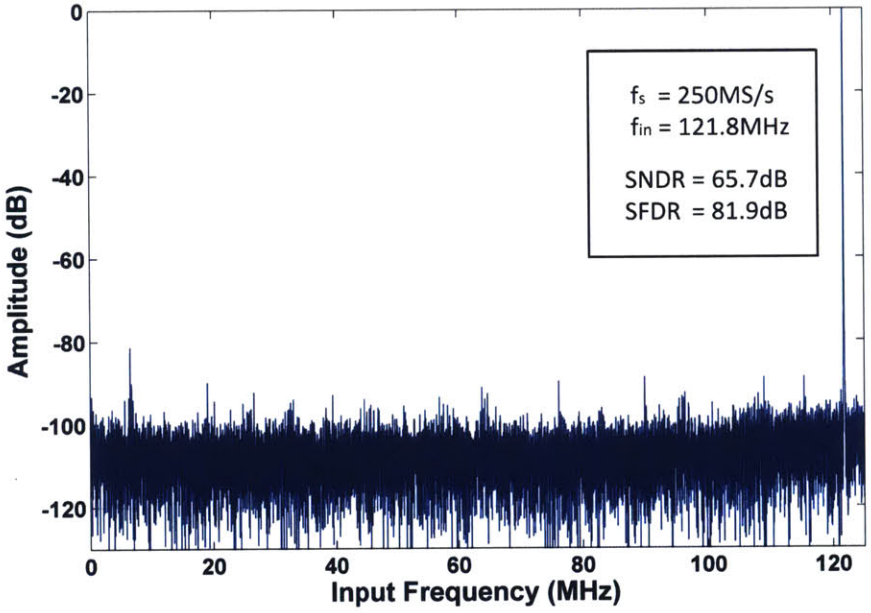


Figure 5-10: Measured spectrum at a sampling rate of 250MS/s for f_{in}=12.1MHz and a grounded input signal before capacitor mismatch calibration.

Figure 5-12 shows the SNDR and SFDR performance of three randomly selected dies at a sampling rate of 250MS/s as the input frequency is swept. The SNDR is consistent across the three chips. Sampling frequency is swept in Figure 5-13 while the input signal is set at a low frequency. The ENOB remains at 10.3-bits even at a sampling rate of 280MS/s.



(a)



(b)

Figure 5-11: Measured spectrum at a sampling rate of 250MS/s for (a) f_{in}=12.1MHz and (b) f_{in}=121.8MHz.

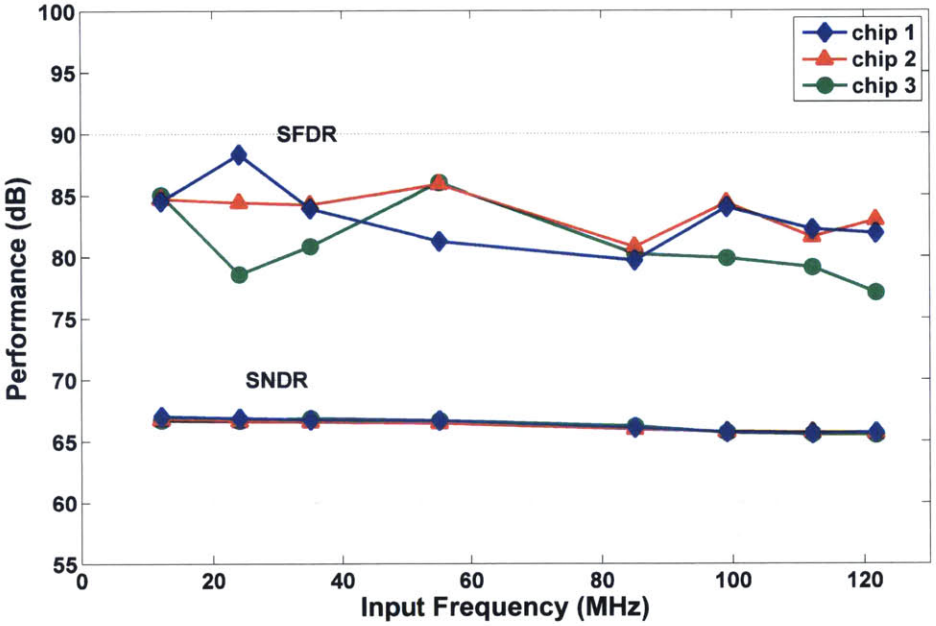


Figure 5-12: Measured dynamic performance vs. input signal frequency for three randomly selected chips.

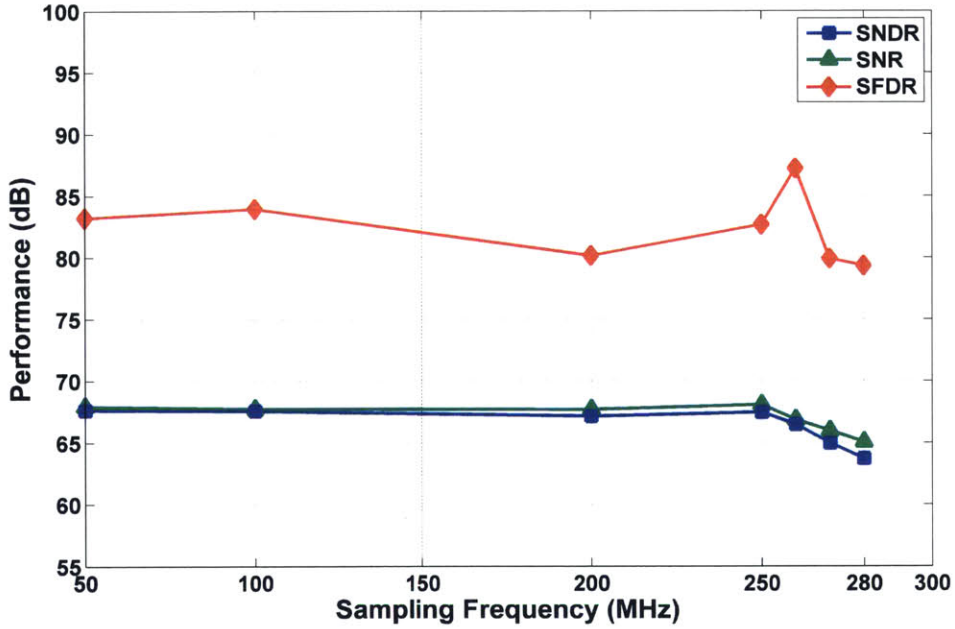


Figure 5-13: Measured dynamic performance vs. sampling frequency.

The chip operates from 1.2V power supply, and consumes 49.7mW at 250MS/s. The current consumption for each circuit block is shown in Figure 5-14: 23.3mA in the op-amps, 6.9mA in the level-shifting buffers, 6.0mA in the clock, digital and flash ADC, 3.3mA in the flash reference ladders, and 2.0mA in the biasing cell. Even though the level-shifting buffers in the current implementation consume twice as much power as the reference buffers in the conventional circuits, they are far from being the dominant power consumption block, and can be further reduced by duty-cycling and multiple unit buffers. The op-amp takes more than half of the total power consumption. In this proof of concept chip, standard power saving measures such as op-amp scaling and duty cycling were not implemented for simplicity. Therefore, there is substantial room for further optimization and large power savings in future designs.

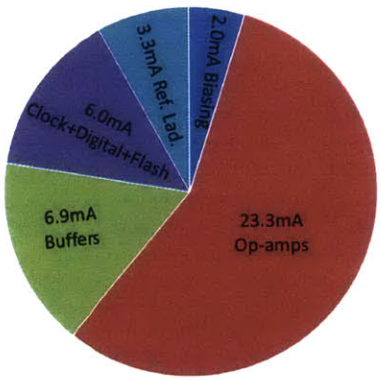


Figure 5-14: Measured current consumption for each circuit block.

The performance of this work compared to other single-channel ADCs 12-bit resolution and sampling rate of 200MS/s in Table 5.1. In [14] and [16], the op-amps are replaced, and in [4], an op-amp-based digital calibration scheme is presented. The proposed ADC demonstrates the highest sampling rate, SNDR and SFDR.

	This Work	Shin [14] JSSC 2014	Dolev [16] VLSI 2013	Sahoo [4] JSSC 2009
Technology	65nm	55nm	65nm	90nm
Type	Op-amp-based virtual ground reference buffer	Zero-crossing based	Pulsed bucket brigade digital calibration	Op-amp-based digital calibration
Sampling Rate	250MS/s	200MS/s	200MS/s	200MS/s
Resolution	12b	12b	12b	12b
Power Supply	1.2V	1.1V	1V	1.2V
Input Signal Range	1.5Vp-p	2Vp-p	-	1.2Vp-p
SNDR	67.0dB @ 12.1MHz 65.7dB @ 121.8MHz	64.6dB @ 10.1MHz 63.2dB @ 100MHz	65dB @ 1MHz 57.6dB @ 99MHz	64dB @ 3.5MHz 61.6dB @ 91MHz
SFDR	84.6dB @12.1MHz	82.9dB @ 10.1MHz	82dB @ 1MHz	70dB
Power	49.7mW	30.7mW	11.5mW*	348mW
FoM	108.5fJ/step	111.0fJ/step	39.6fJ/step*	1.34pJ/step

* Excludes power consumption in reference buffers and digital calibration circuits

Table 5.1: Performance summary and comparison with other single-channel ADCs with similar performance specifications.

Chapter 6

Conclusion and Future Work

This thesis contributes a VGRB technique that relaxes the key op-amp performance specifications by improving its feedback factor in switched-capacitor circuits.

6.1 Contribution

The op-amp has become the performance bottleneck in many traditional op-amp-based designs as technology continues to scale. In conventional designs, the signal gain of a switched-capacitor circuit is largely set by the inverse of the feedback factor, and this determines the op-amp specifications. Previously published work has proposed various complex digital calibration schemes or even replaced the op-amp entirely at the cost of raised concerns in robustness and reliability. In this work, by improving the feedback factor without altering the signal gain, a low power, high resolution, and high speed op-amp-based pipelined ADC is implemented. Unlike alternative approaches, the VGRB approach retains the conventional design style as much as possible, all the while improving the performance by virtue of a simple yet power-efficient way of operating an op-amp-based switched-capacitor circuit. Complex digital calibration to mitigate the performance degradation from finite gain or insufficient settling of the op-amp is avoided, since the signal chain is accurate without the need to calibrate op-amp nonlinearity. The circuit operation is also more straightforward and simple than the published work in ZCBC, PBB, and ring amplifier based pipelined ADCs.

The prototype pipelined ADC was fabricated in TSMC 65nm LP technology. It achieves 67.0dB SNDR, 84.6 SFDR, -0.86/+0.52 DNL and -0.90/+1.08 INL at a sampling rate of 250MS/s and input signal frequency of 12.1MHz. The power consumption is 49.7mW, corresponding to 108.5fJ/step FoM. Large power savings can be achieved by applying standard power saving measures such as op-amp duty-cycling, sharing, and scaling in future designs.

6.2 Future Work

There are significant opportunities to improve the current implementation. The additional effort can push the ADC performance well beyond what is achieved in the prototype. Also, the application of the VGRB technique is not limited to pipelined ADCs. The concept can be applied to any switched-capacitor circuit in general. This opens room for creativity in other analog circuit designs.

The pipelined ADC with the proposed VGRB technique demonstrates excellent performance results, but little effort was made for optimization and the op-amps are responsible for the majority of the power consumption. For a better power-optimized design, the op-amps can be scaled throughout the stages. Also, gain-boosting op-amps are not necessary in every stage and can be dropped towards the back-end stages. Power consumption in the op-amps can be further decreased by duty-cycling or sharing between stages.

In addition to these standard measures mentioned above, outstanding issues must be addressed. On the circuit side, the level-shifting buffer is of significant importance since by and large other circuit blocks follow conventional designs. Among the several design parameters, the gain of the level-shifting buffer determines how much residual capacitance loads the virtual ground node and therefore deserves high attention. It is critical to make the gain close to the ideal unity to bring forward the maximum benefit of the VGRB technique. Minimization of the parasitic capacitance, particularly C_{gd}, becomes more important in ADCs with higher sampling rate. As op-amps are scaled up for faster operation, the buffers also need to scale up accordingly. As discussed

in Chapter 4, C_{gd} is responsible for approximately one third of the total parasitic capacitance loading the virtual ground node in the current implementation. This can become the dominant limiting factor in the feedback factor in high performance ADCs. Circuit techniques to bootstrap the C_{gd} capacitance will bring a major performance improvement. For better noise rejection, the level-shifting buffers can be implemented differentially. In this case, the current can be shared between the PMOS and NMOS buffers, reducing power consumption. Another interesting design approach is to have a unit level-shifting buffer cell for each unit capacitor in the MDAC array. Although this may increase the design complexity, the unit level-shifting buffers can be turned off to eliminate static current when they are not being used, achieving 2x power saving. In the current prototype, this is not possible since a pair of PMOS and NMOS level-shifting buffers drive all the unit capacitors.

The stabilization of the reference voltages against process and temperature variations is another concern that requires further research. Specifically, the transistor V_T ultimately sets the reference voltages, but varies substantially across corners. If V_T is significantly reduced, than the full-scale range is reduced as well, leading to lower SNR. On the other hand, higher V_T demands more head-room in the op-amp for linear amplification across a wider output range. Reference voltage mismatch due to process variation can also limit the linearity as shown in measurement results in Chapter 5. An automatic tuning loop was not included in the prototype chip, but a feedback loop can be implemented to control the current of the level-shifting buffers to keep the V_{GS} constant. Also, the level-shifting buffers can be shared across stages since reference voltages are required in the charge-transfer phase only. This way, two consecutive stages can have the identical set of reference voltages, eliminating mismatch. This also comes with the additional benefit of power savings. In addition, both reference voltage and capacitor mismatch calibration can be applied using decision boundary gap estimation in [51]. Capacitor mismatch is independent of process, voltage, and temperature (PVT) variation. The reference voltage, however, suffers from PVT variation and it is necessary to recalibrate if conditions change.

On the system side, a better optimization scheme can be explored. Although

generally greater performance improvement can be obtained in stages with large signal gain since the improvement in the feedback factor becomes more dramatic, this is not true in every implementation. For example, for fixed sampling capacitance, resolving a larger number of bits in the stage results in lower op-amp feedback capacitance, C_2. Assuming the parasitic capacitance from the op-amp and the level-shifting buffers is largely unchanged, the feedback factor can potentially degrade relative to that of a switched-capacitor circuit that resolves lower number of bits but has higher C_2 capacitance. It will be interesting to investigate the optimum number of bits per stage throughout the pipelined stages in the context of either power-optimized or noise-optimized solutions.

Bibliography

[1] (2015) ADC Performance Survey (ISSCC & VLSI Symposium). [Online]. Available: http://www.stanford.edu/ murmann/adcsurvey.html

[2] N. Maghari and U.-K. Moon, "Emerging analog-to-digital converters," in *IEEE European Solid State Circuits Conference*, Sep. 2014, pp. 43–50.

[3] J.-R. Kim and B. Murmann, "A 12-b, 30-MS/s, 2.95-mW Pipelined ADC Using Single-Stage Class-AB Amplifiers and Deterministic Background Calibration," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2141–2151, Sep. 2012.

[4] B. Sahoo and B. Razavi, "A 12-Bit 200-MHz CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2366–2380, Sep. 2009.

[5] A. Panigada and I. Galton, "A 130 mW 100 MS/s Pipelined ADC With 69 dB SNDR Enabled by Digital Harmonic Distortion Correction," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.

[6] A. Verma and B. Razavi, "A 10-Bit 500-MS/s 55-mW CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.

[7] Y. Miyahara, M. Sano, K. Koyama, T. Suzuki, K. Hamashita, and B.-S. Song, "Adaptive cancellation of gain and nonlinearity errors in pipelined ADCs," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2013, pp. 282–283.

[8] B. Gregoire and U.-K. Moon, "An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2008, pp. 540–634.

[9] B. Hershberg, S. Weaver, and U.-K. Moon, "Design of a Split-CLS Pipelined ADC With Full Signal Swing Using an Accurate But Fractional Signal Swing Opamp," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2623–2633, Dec. 2010.

[10] L. Brooks and H.-S. Lee, "A 12b 50MS/s fully differential zero-crossing-based ADC without CMFB," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2009, pp. 166–167.

[11] J. Chu, L. Brooks, and H.-S. Lee, "A zero-crossing based 12b 100MS/s pipelined ADC with decision boundary gap estimation calibration," in *IEEE Symposium on VLSI Circuits*, Jun. 2010, pp. 237–238.

[12] S. Lee, A. Chandrakasan, and H.-S. Lee, "A 12 b 5-to-50 MS/s 0.5-to-1 V Voltage Scalable Zero-Crossing Based Pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1603–1614, Jul. 2012.

[13] D.-Y. Chang, C. Munoz, D. Daly, S.-K. Shin, K. Guay, T. Thurston, H.-S. Lee, K. Gulati, and M. Straayer, "A 21mW 15b 48MS/s zero-crossing pipeline ADC in 0.13μm CMOS with 74dB SNDR," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2014, pp. 204–205.

[14] S.-K. Shin, J. Rudell, D. Daly, C. Munoz, D.-Y. Chang, K. Gulati, H.-S. Lee, and M. Straayer, "A 12 bit 200 MS/s Zero-Crossing-Based Pipelined ADC With Early Sub-ADC Decision and Output Residue Background Calibration," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 6, pp. 1366–1382, Jun. 2014.

[15] M. Anthony, E. Kohler, J. Kurtze, L. Kushner, and G. Sollner, "A process-scalable low-power charge-domain 13-bit pipeline ADC," in *IEEE Symposium on VLSI Circuits*, Jun. 2008, pp. 222–223.

[16] N. Dolev, M. Kramer, and B. Murmann, "A 12-bit, 200-MS/s, 11.5-mW pipeline ADC using a pulsed bucket brigade front-end," in *IEEE Symposium on VLSI Circuits*, Jun. 2013, pp. C98–C99.

[17] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring Amplifiers for Switched Capacitor Circuits," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.

[18] B. Hershberg and U.-K. Moon, "A 75.9dB-SNDR 2.96mW 29fJ/conv-step ringamp-only pipelined ADC," in *IEEE Symposium on VLSI Circuits*, Jun. 2013, pp. C94–C95.

[19] Y. Lim and M. P. Flynn, "A 100MS/s 10.5b 2.46mW comparator-less pipeline ADC using self-biased ring amplifiers," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2014, pp. 202–203.

[20] S. Lewis, "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 39, no. 8, pp. 516–523, Aug. 1992.

[21] C. Conroy, D. Cline, and P. Gray, "An 8-b 85-MS/s parallel pipeline A/D converter in 1-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 447–454, Apr. 1993.

[22] D. Cline and P. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, Mar. 1996.

[23] T. Cho and P. Gray, "A 10-bit, 20-MS/s, 35-mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[24] J. Goes, J. Vital, and J. Franca, "Systematic design for optimization of high-speed self-calibrated pipelined A/D converters," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 12, pp. 1513–1526, Dec. 1998.

[25] P. Yu and H.-S. Lee, "A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1854–1861, Dec. 1996.

[26] N. Sasidhar, Y.-J. Kook, S. Takeuchi, K. Hamashita, K. Takasuka, P. Hanumolu, and U.-K. Moon, "A Low Power Pipelined ADC Using Capacitor and Opamp Sharing Technique With a Scheme to Cancel the Effect of Signal Dependent Kickback," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2392–2401, Sep. 2009.

[27] L. Singer, S. Ho, M. Timko, and D. Kelly, "A 12 b 65 MSample/s CMOS ADC with 82 dB SFDR at 120 MHz," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2000, pp. 38–39.

[28] Y.-J. Cho and S.-H. Lee, "An 11b 70-MHz 1.2-mm^2 49-mW 0.18-μm CMOS ADC with On-Chip Current/Voltage References," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 10, pp. 1989–1995, Oct. 2005.

[29] K. Gulati, M. Peng, A. Pulincherry, C. Munoz, M. Lugin, A. Bugeja, J. Li, and A. Chandrakasan, "A Highly Integrated CMOS Analog Baseband Transceiver With 180 MSPS 13-bit Pipelined CMOS ADC and Dual 12-bit DACs," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1856–1866, Aug. 2006.

[30] L. Sumanen, M. Waltari, and K. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1048–1055, Jul. 2001.

[31] Z. Cao, S. Yan, and Y. Li, "A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 862–873, Mar. 2009.

[32] Y.-D. Jeon, Y.-K. Cho, J.-W. Nam, K.-D. Kim, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15mW 0.22mm^2 10b 204MS/s pipelined SAR ADC in 65nm CMOS," in *IEEE Custom Integrated Circuits Conference*, Sep. 2010, pp. 1–4.

[33] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York, NY, USA: McGraw-Hill, Inc., 2001.

[34] H.-S. Lee and D. Hodges, "Self-calibration technique for A/D converters," *IEEE Transactions on Circuits and Systems*, vol. 30, no. 3, pp. 188–190, Mar. 1983.

[35] A. Karanicolas, H.-S. Lee, and K. Barcrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.

[36] D.-Y. Chang, "Design techniques for a pipelined ADC without using a front-end sample-and-hold amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 11, pp. 2123–2132, Nov. 2004.

[37] P. Huang, S. Hsien, V. Lu, P. Wan, S.-C. Lee, W. Liu, B.-W. Chen, Y.-P. Lee, W.-T. Chen, T.-Y. Yang, G.-K. Ma, and Y. Chiu, "SHA-Less Pipelined ADC With In Situ Background Clock-Skew Calibration," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1893–1903, Aug. 2011.

[38] H. H. Boo, D. S. Boning, and H.-S. Lee, "12b 250MS/s pipelined ADC with virtual ground reference buffers," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2015, pp. 282–283.

[39] W. Sansen, "Analog design challenges in nanometer CMOS technologies," in *IEEE Asian Solid-State Circuits Conference*, Nov. 2007, pp. 5–9.

[40] B. Jonsson, "On CMOS scaling and A/D-converter performance," in *NORCHIP*, Nov. 2010, pp. 1–4.

[41] P. Hurst, "A comparison of two approaches to feedback circuit analysis," *IEEE Transactions on Education*, vol. 35, no. 3, pp. 253–261, Aug. 1992.

[42] B. Nikolic and M. Slavoljub, "A general method of feedback amplifier analysis," in *IEEE International Symposium on Circuits and Systems*, vol. 3, May 1998, pp. 415–418.

[43] G. A. Miller and M. C. W. Coln, "Jitter and load insensitive charge transfer," U.S. Patent US6 452 531 B1, Sep., 2002.

[44] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[45] J. Lloyd and H.-S. Lee, "A CMOS op amp with fully-differential gain-enhancement," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 41, no. 3, pp. 241–243, Mar. 1994.

[46] D. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, 1997.

[47] R. Carvajal, J. Ramirez-Angulo, A. Lopez-Martin, A. Torralba, J. Galan, A. Carlosena, and F. Chavero, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.

[48] T. Man, K. N. Leung, C. Y. Leung, P. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 5, pp. 1392–1401, Jun. 2008.

[49] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.

[50] I. Ahmed and D. Johns, "An 11-bit 45 MS/s pipelined ADC with rapid calibration of DAC errors in a multi-bit pipeline stage," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 7, pp. 1626–1637, Jul. 2008.

[51] L. Brooks and H.-S. Lee, "Background Calibration of Pipelined ADCs Via Decision Boundary Gap Estimation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2969–2979, Nov. 2008.