Merged Multi-Stage Power Conversion: A Hybrid Switched-Capacitor/Magnetics Approach

by

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Submitted to the Department of Electrical Engineering and Computer Science,
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Doctor of Philosophy

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Abstract

Emerging applications of power electronics introduce challenging design requirements. Increasing the system complexity in appropriate ways can bring many advantages, yielding reduced system volume and/or improved system performance. This thesis explores new circuit design techniques that can leverage the advantages of merged multi-stage power conversion through a hybrid switched-capacitor/magnetics approach. Multiple circuits and system aspects of this approach are investigated in this thesis.

A 70 W grid-interfaced solar micro-inverter with a *multilevel energy buffer and voltage modulator* (*MEB*) is developed to demonstrate the advantages of a merged multi-stage system in dc-ac applications. By synthesizing a multilevel voltage in pace with the ac grid voltage using the energy buffer, the wide operation range of the inverter stage is compressed, leading to a significantly improved overall system performance.

A high-power-density wide-input-voltage-range isolated dc-dc converter with a *MultiTrack* power conversion architecture is also investigated. The MultiTrack architecture delivers power in multiple voltage domains and current tracks. It incorporates multiple distributed circuit cells, and benefits from the way they are merged together. By changing the use of multiple cells according to the system operating condition, the overall device utilization of the system is enhanced, leading to significantly improved power density as compared to conventional designs while maintaining high efficiency. The prototype 18 V–80 V input, 5 V output, 75 W isolated dc-dc converter achieves 453.7 W/inch^3 power density, which is 3x higher than the best commercial product presently available. It maintains high efficiency across a wide (>4:1) input voltage range, and has a peak efficiency of 91.3%.

Advanced magnetics structures are an enabling technique on the path to improved power conversion. This thesis developed a systematic approach to modeling impedances and current distribution in planar magnetics. It captures electromagnetic coupling relationships using an analytical lumped circuit model, and enables rapid evaluation of planar magnetics designs. The effectiveness of the model is verified by numerical methods and experimental measurements. A software package – *M2Spice* – that can rapidly convert design information into SPICE netlists has been developed and is being utilized in many real designs.

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Finally, the finishing of this thesis is not an end. It is a start!

"Good, better, best,

never let it rest.

Until your good is better,

and your better is your best."

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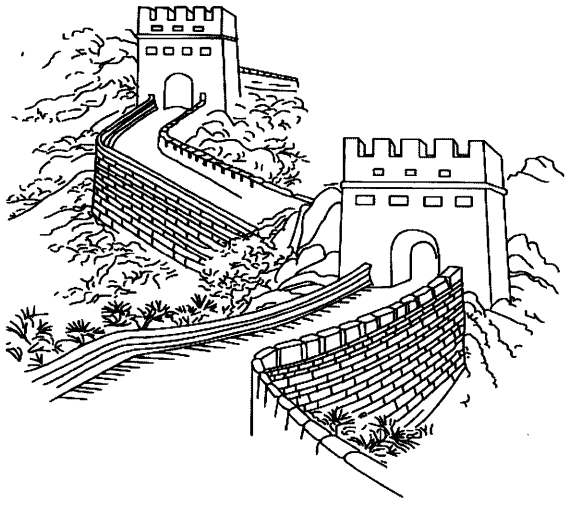

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Chapter 1

Thesis Overview

1.1 Merged Multi-Stage Power Conversion

The advances in power electronics have been driven by the increasing capability of semiconductor devices, together with advances in circuit topologies, packaging techniques and system architectures. As new devices and new applications emerge, there are new challenges and opportunities in all aspects of power electronics design [1, 2]. Emerging and growing applications of power electronics, such as the renewable energy integration, electric vehicles and energy harvesting devices, brings multi-dimensional design requirements. Take the solar micro-inverter as an example. A commonly used solar micro-inverter system needs to

1. operate efficiently over wide voltage conversion ranges and power ranges;
2. interface with the grid with high power factor and THD;
3. perform maximum power point tracking function;
4. be highly reliable in a wide range of ambient conditions;
5. has small size and light weight to minimize the hardware and installation cost;
6. be low-cost and have long-life-time to reduce the solar electricity price.

Likewise, there is a need for advances in power electronic converters owing to the continual competitive drive towards higher performance and smaller size in all kinds of electronic systems. For example, the requirements on efficiency and power density of isolated dc-dc converters in telecommunications applications (e.g., for powering devices on server computer boards, for communications systems and data centers, etc.) continue to go up. There are

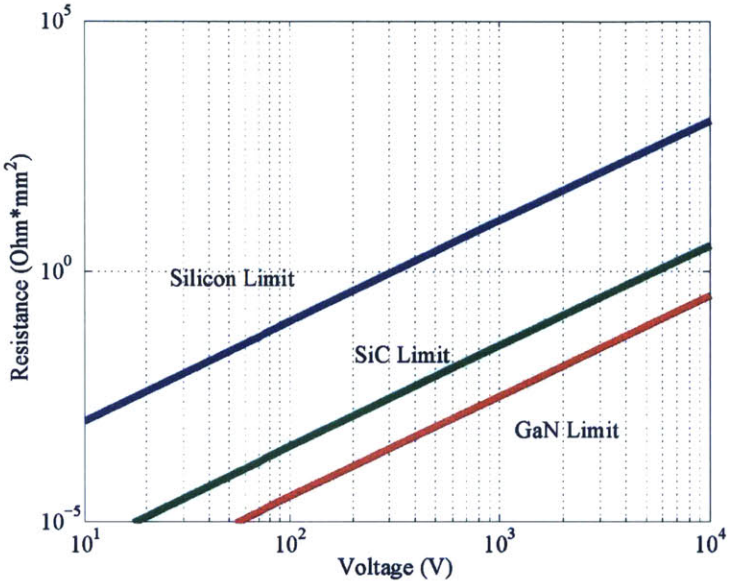


Figure 1-1: Theoretical on-resistance v.s. blocking voltage capability for silicon, silicon-carbide (SiC), and gallium nitride (GaN) [3].

continuously increasing performance demands placed on these multi-dimensional requirements, motivating innovations from device level to system level. Improved power electronics architectures that can satisfy these increased design requirements, are in need.

The next generation of power electronics will be able to take advantage of the continued progress in wide band-gap semiconductor devices, especially silicon-carbide (SiC) and gallium nitride (GaN) devices. As shown in Fig. 1-1, SiC and GaN both have a superior relationship between on-resistance and breakdown voltage due to their higher critical electric field strength. For a given breakdown voltage requirement, this allows smaller devices and shorter channel lengths. Their greater thermal conductivity provide access to higher power densities that are difficult for Si-based devices. For the same blocking voltage and on-resistance, footprints of the state-of-art GaN devices can be more than 3 times smaller than that of equivalent silicon MOSFETs [4]. In addition, the advantages of moving the operating frequencies of power converters upward, are significantly enhanced by the extremely fast switching speeds (low parasitics and short turn-on/-off time) of wide band-gap power semiconductor devices.

In contrast, developments in passive components are lagging behind. The energy density and power density of capacitors and inductors are highly constrained by the material physics

and manufacturing capabilities. Evolution of passive components naturally has a much longer innovation cycle. Power conversion architectures and topologies which heavily utilize active semiconductor devices to reduce the overall requirements on the passive components are thus a promising approach towards improved power electronics. The author envisions that this is a key opportunity, and will become a the major trend in the near future. As will be seen, the developments in this thesis are directly targeted at this opportunity.

Increasing the switching frequency of power converters is one fundamental approach to take advantages of better semiconductors, and to reduce energy storage requirements of passive components (though not their peak power handling capability). Much research has been done to explore the advantages of high frequency (HF), and very-high-frequency (VHF) power electronics, e.g. [5–8]. Increasing the sophistication of system architecture is another approach. By increasing the circuit complexity (e.g., higher component count), the stress and energy storage requirements on the passive components can be reduced.

Power electronics designs have always been heavily driven by cost. Simple circuit topologies with low complexity, low component counts, and simple controls used to be preferable in practical designs. However, with the increasing electronics content of industrial and consumer applications, and the wide deployment of renewable energy, power electronics are playing more important and sophisticated roles in systems. At the same time, the relative cost of power devices and control circuitry has fallen (following the trend of the semiconductor industry overall). Enhancing the system performance through more sophisticated circuit architecture is attractive with many emerging design opportunities.

Power conversion architectures can be grouped into single-stage architectures and multi-stage architectures. In a single-stage architecture, multiple tasks (e.g., voltage modulation, power modulation) are realized in a single power stage. They have low circuit complexity and simple control, but cannot achieve high performance while meeting requirements such as wide operating ranges, high power density and/or low cost. Multi-stage architectures have multiple power conversion stages with each stage performing one or more functions. Each stage can be optimally designed to only address a portion of the system requirements. As a result, the overall system performance is often better, while the total component counts and control complexities are usually higher. Sometimes, some multi-stage architectures may fully process the system energy multiple times, imposing a penalty on efficiency.

As the function of power electronics systems get increasingly sophisticated, and semiconductor devices are continuously miniaturized, there is an urgent desire (and an exciting opportunity) to develop new circuit topologies with multiple stages functionally or topologically merged together to achieve higher performance. These power conversion architectures and design-concepts are generally referred to as the *merged multi-stage* power conversion architecture in this thesis. In particular, we further focus on architectures that combine the best aspects of switched-capacitor and magnetic power conversion methods.

A systematic investigation into merged multi-stage power conversion architectures utilizing hybrid switched-capacitor and magnetics techniques will be presented as the main body of this thesis. The advantages and design considerations of merged multi-stage architectures are discussed through the design of two practical power conversion systems, and the development of one theoretical modeling method.

Here we briefly discuss some advantages of merged multi-stage power conversion architectures. Firstly, there usually exist many devices and circuit blocks in multi-stage power electronics. Some of them are repeated in many stages, and some of them are not well utilized across the full operation range. In many multi-stage systems, electric power is "reprocessed" by the multiple stages, inducing undesired loss along the sequence. Some components play single/simple functions but occupy substantial system volume. Some components are rated for the worst-case, while most of the time the system doesn't operate close to the worst-case. Merging some stages, reusing some components, and appropriately increasing system complexity, can improve the device utilization, create mutual advantages and improve system performance.

By replacing a centralized power conversion system with a merged multi-stage system, several advantages of *distributed power conversion* [9–12] can be achieved, including:

1. **High-Frequency Operation:** By dividing a concentrated system into multiple stages and merging them, active and passive devices with lower power ratings and smaller packages can be used. Smaller devices generally favor high-frequency operation due to the significantly reduced parasitics effects, such as lower gating inductances [11] and smaller current loops. High frequency operation can reduce the physical size of passive components. [5–8].

2. **Better Device Utilization/Performance:** It is known that the on-resistance per die area of an ideal Schottky junction device is proportional to the square of its blocking voltage (V^2) [3, 13]. If n devices with $1/n$ voltage rating are cascaded in series to replace a single device that has the full voltage rating, the total conduction loss (i^2R) of the device is expected to drop by a factor of $\frac{1}{n}$. Similarly, the drain-to-source capacitance of a switch is proportional to its current rating. If a high-voltage rating, hard-switched devices are replaced with n series-connected lower-voltage-rating hard-switched devices, the total switching loss is expected to drop by a factor of $\frac{1}{n}$.

3. **Simplified Thermal Management:** In the distributed configuration, each converter stage/cell handles only a portion of the total power. Heat dissipation is better distributed on the printed circuit board (PCB), reducing the peak temperature and simplifying the thermal design.

4. **Enhanced Reliability:** Distribution reduces electrical and thermal stresses on semiconductor devices. Distribution also offers additional ways of creating system redundancy. Although the number of components in a distributed architecture is increased, the overall system reliability can be improved [11].

5. **Reduced Filter Size:** Filter size and EMI considerations play important role and take significant volume in power electronics systems. Distributed design can reduce the filter size because (1) the subsystem can operate at higher frequencies; (2) Interleaving of distributed circuit cells can increase the ripple frequency.

All of these advantages may or may not be fully achieved in real designs, due to the natural complexity of design tradeoffs. Nevertheless, these engineering insights are in favor of moving towards more sophisticated and distributed power conversion architecture with multiple merged-stages.

1.2 Switched-Capacitor Circuits and Planar Magnetics

Capacitors and inductors are two major groups of passive components utilized in power electronics systems. Capacitors store energy in the format of voltage (or, more precisely, in electric fields), and inductors store energy in the format of current loops (or, more precisely, in magnetic fields). It is known that the energy densities of capacitors at typical

scales for power conversion systems are at least an order of magnitude higher than those of inductors [14, 15]. Thus, switched-capacitor circuits are promising to achieve higher power density/efficiency tradeoffs than conventional magnetics-based topologies for functions where they are effective, including for realizing fixed voltage/current transformations and for synthesizing multiple ratiometrically-related voltages.

One major branch of switched-capacitor circuits is switched-capacitor voltage converters. Systematic investigations about switched-capacitor dc-dc converters are provided in [16–18] and references therein. Besides voltage conversion, switched-capacitor circuit can also be utilized as active energy buffering devices. A stacked switched capacitor energy buffer architecture is proposed in [19, 20] to enhance the utilization of capacitors, to reduce the overall energy buffer size and to eliminate the usage of electrolytic capacitors in applications if long lifetime is required. Lastly, switched-capacitor converters are often effective for synthesizing multiple related voltage levels, either one at a time or simultaneously creating multiple voltage rails (e.g. [21, 22]).

One natural drawback of switched-capacitor voltage converters is their weakness in voltage regulation (that is, the inability of a switched-capacitor to efficiently process energy except at one or more fixed voltage conversion ratios, or – more precisely – current conversion ratios). In applications where voltage regulation is required, inclusion of magnetic devices is useful. There has been significant recent work in hybridizing switched-capacitor and magnetic conversion, with consequent performance advantages. Resonant switched-capacitor circuit is one approach. By adding one or more inductive components into the circuit structure, enhanced performance with reasonable regulation capability can be achieved [23–25]. Merging multi-stage systems incorporating switched-capacitor circuits, switched-inductor circuits and/or magnetically-coupled circuits (e.g., "dc transformers") is another branch. A switched-capacitor voltage divider and a multi-phase buck converter were combined to implement a high performance laptop power supply in [26]. The merged-two-stage dc-dc converter presented in [27] and the wide-input-range converter presented in [28] each incorporated switched-capacitor circuit with switched-inductor circuit. An on-chip switched-capacitor converter was combined with capacitive isolation circuits and magnetics as the dc-dc portion of a LED driver in [22]. A few versions of high-frequency grid-interfaces LED drivers using merged circuit architectures were presented in [29–31].

Although switched-capacitor circuit topologies can replace magnetics-based circuit topolo-

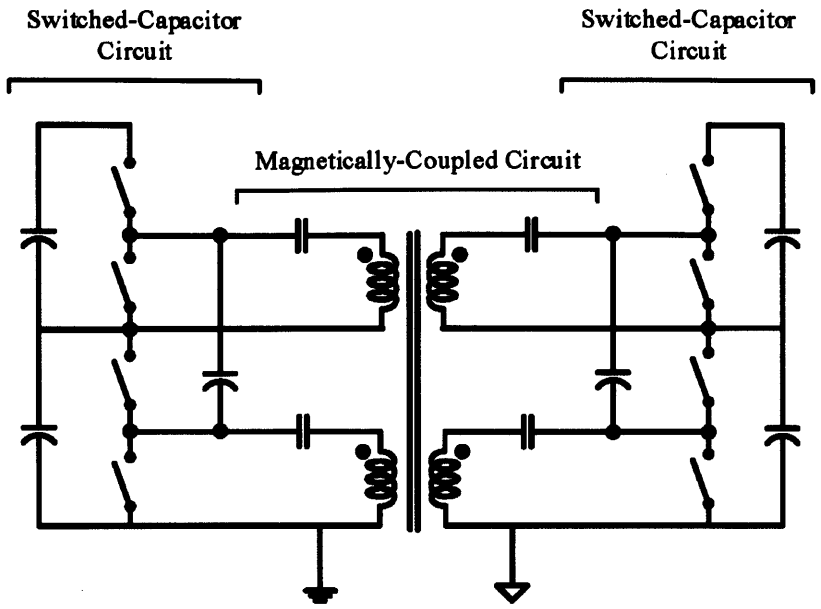


Figure 1-2: An example hybrid switched-capacitor/magnetics circuit structure. Multiple switching nodes of switched-capacitor circuit are utilized to drive/load multiple magnetic windings. This structure can be utilized as a core for many merged-multi-stage topologies.

gies in many applications, magnetics-based circuits still play key roles in power electronics systems. Power electronics engineers need their capabilities (arbitrary conversion ratios, galvanic isolation, large conversion ratios, soft switching, filtering, etc.) in realizing many required functions. Decades of research have been done on power magnetics [32–36]. However, the electrical characteristics of inductors, coupled inductors, and transformers can still be difficult to adequately predict and control, especially at high switching frequencies with sophisticated winding structures. This is partially because of the complicated nature in magnetic materials, and partially because of the difficulties of predicting fields and current distributions with complex windings in the presence of magnetic cores (e.g. skin- and proximity-effects [37], fringing effects [38, 39]).

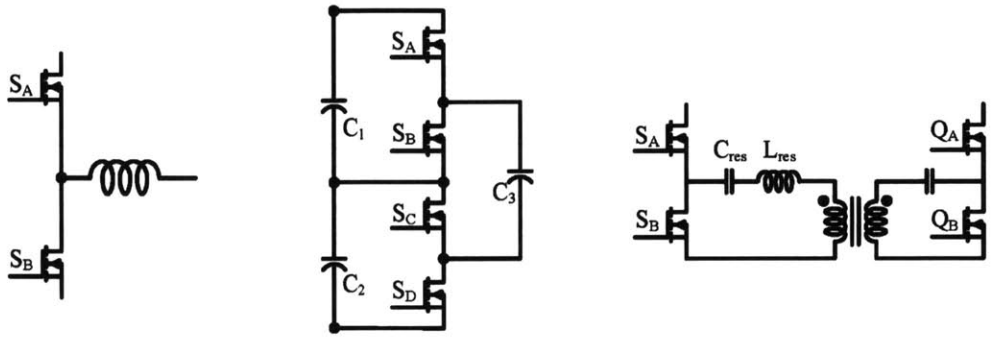
Planar magnetics have core geometries that can often be modeled adequately with analytical equations, are capable of utilizing complex printed circuit winding patterns to realize designs that are attractive for high-frequency merged multi-stage power electronics design [33, 35]. Chapter 4 of this thesis is dedicated to the development of a systematic approach to modeling the impedances and current distribution in planar magnetics.

Many characteristics of switched-capacitor circuits and magnetic converter circuits are compatible: switched-capacitor circuits naturally incorporate many ac voltage sources (e.g., as realized with switching networks such as half-bridge inverters), which can be utilized to drive/load the multiple windings of magnetic devices. Switched capacitor circuits usually are hard-switched and/or hard-charged, suffering hard-switching loss and/or charge-sharing loss. Loading/driving switched-capacitor circuit with magnetic devices can enable soft-switching and soft-charging operation of switched-capacitor circuit [27, 28]. Magnetics also enable voltage regulation capability of switched-capacitor circuits. As will be shown, using switched-capacitor circuits to subdivide or create voltage domains can compress or expand the voltage conversion range of magnetics-based circuits. An example hybrid switched-capacitor/magnetics circuit structure is shown in Fig. 1-2. The multiple switching nodes of the switched-capacitor circuit are loaded/driven by a few windings that are coupled together through the single magnetic path of a transformer. As will be investigated in Chapter 2 and Chapter 3, appropriately combining switched-capacitor circuit with magnetics can create many system-level advantages.

1.3 Three Basic Circuit Blocks in Power Electronics

Switched-inductor, switched-capacitor, and magnetically-coupled (magnetically-isolated) circuits are sometimes considered as three building block circuits in power electronics systems [15]. Fig. 1-3 shows three example embodiments of these three types of basic circuits. A switched-inductor circuit naturally creates multiple current paths; a switched-capacitor circuit naturally creates multiple voltage domains; and a magnetically-coupled circuits utilizes magnetic fields to transfer energy from one voltage domain to another and provide voltage and current scaling. These characteristics allow magnetic isolation circuits to split/merge electrical power smoothly across different voltage domains and current paths created/generated by switched-inductor/switched-capacitor circuits.

The investigation into merged multi-stage power conversion is centered around the utilization of these three basic circuit cells. The major goals of this thesis are (1) to develop advantageous ways of combining these three basic circuit blocks; (2) to merge the functions in multi-stage conversion systems in ways that benefit converter performance; and (3) to demonstrate and quantify these approaches and their advantages in practical designs.



Switched-Inductor Circuit **Switched-Capacitor Circuit** **Magnetically-Coupled Circuits**

Figure 1-3: Example embodiments of a switched-inductor circuit (canonical cell), a switched-capacitor circuit (2:1 ladder switched-capacitor), and a magnetically-coupled circuit (an isolated series-resonant converter).

In the solar micro-inverter presented in Chapter 2, a switched-capacitor circuit is utilized to synthesize a grid-synchronized multilevel voltage that can enhances the performance of the high-frequency-link magnetic-isolated converter. To maintain the appropriate operation of this switched-capacitor circuit, a switched-inductor circuit is utilized as a current source which interfaces with the switched-capacitor circuit. In the wide-input-voltage-range isolated dc-dc converter presented in Chapter 3, the multiple switch nodes of a switched capacitor circuit are utilized to drive a transformer with multiple windings. The multiple dc-voltages synthesized by the switched-capacitor circuit are connected to a switched-inductor circuit to enable voltage regulation. In addition to these two experimental efforts, the major purpose of developing the planar magnetics modeling approach presented in Chapter 4, is to enable more sophisticated magnetically-coupled merged multi-stage systems that combine switched-inductor circuits and switched-capacitor circuits in appropriate ways.

1.4 Thesis Organization

Three branches of efforts have been made in this thesis to investigate and demonstrate the advantages of merged multi-stage power conversion through a hybrid switched-capacitor/ magnetics approach. A 70 W grid-tied solar microinverter with a multilevel energy buffer and voltage modulator is developed and presented in Chapter 2 to demonstrate the advan-

tages of a hybrid switched-capacitor/magnetics system in dc-ac applications. By actively synthesizing a multilevel voltage that is in pace with the ac grid voltage, the switched-capacitor circuit compresses the wide operation range of the magnetics-based circuit, leading to significantly improved overall system performance across a wide dc-ac operation range.

A high-power-density wide-input-voltage-range isolated dc-dc converter with a *Multi-Track* power conversion architecture is then proposed and developed in Chapter 3. It demonstrates the effectiveness of a hybrid switched-capacitor/magnetics system in wide-operating-range dc-dc applications (e.g. Telecom power supplies). The MultiTrack architecture delivers power in multiple voltage domains and current tracks. It incorporates multiple distributed circuit cells, and benefits from the way they are merged together. By reconfiguring the multiple building blocks according to the system operation state, the overall component utilization of the system can be improved, leading to significantly improved power density while maintaining state-of-art efficiency. The prototyped 18 – 80 V input, 75 W isolated dc-dc converter achieves 453.7 W/inch^3 power density. It maintains high efficiency across a wide input voltage range, and has a peak efficiency of 91.3%.

Magnetics structures with sophisticated coupling relationships are envisioned to be an enabling technique on the path to merged multi-stage power conversion architecture. Based on Maxwell's equations and Kirchhoff's Laws, a systematic approach to modeling impedances and current distribution in planar magnetics is developed in Chapter 4. It captures sophisticated electromagnetic coupling relationships in planar magnetics with a modular lumped circuit model, and enables rapid comparison and evaluation of planar magnetics designs through SPICE simulations. Its effectiveness and applicability are verified by finite-element-modeling methods and experimental measurements. A software package – *M2Spice* – that can rapidly convert magnetic geometry information into SPICE netlists has been developed and utilized in real designs.

Chapter 5 summaries these three branches of efforts and puts forward a vision for future work in this area. One promising research direction is to bring the merged multi-stage implementations to high-voltage, high-power applications, where passive components dominate the system volume and performance, and the incremental costs of more complicated gate drive and auxiliary circuitries tend to be negligible. Secondly, given that the device-level advantages of the MultiTrack architecture have been theoretically demonstrated in Chapter 3, it would be interesting to realize/investigate/justify these advantages in a customized

integrated-circuit (IC) design with appropriate device-level tradeoffs, i.e., on-resistances ($R_{\text{ds-on}}$), gate-to-source charge (Q_{gs}) and drain-to-source capacitance (C_{oss}). Finally, the development of *M2Spice* offers a lot of exciting opportunities to develop many novel merged multi-stage circuits that centered-around planar magnetics.

Extended details including theoretical derivations, circuit schematics, Printed-Circuit-Board (PCB) layouts, alternative embodiments, software codes, and practical design considerations are included in the four Appendices attached at the end of this thesis.

Chapter 2

Merged Multi-Stage Power Conversion in a Dc-Ac Converter

Abstract

This chapter investigates the merged multi-stage power conversion approach in dc-ac applications through the design and implementation of a grid-interface solar microinverter. Micro-inverters operating into the single-phase grid from solar photovoltaic (PV) panels or other low-voltage sources must buffer the twice-line-frequency variations between the energy sourced by the PV panel and that required for the grid. Moreover, in addition to operating over wide average power ranges (due to the variations in the strength of the solar power), they inherently operate over a wide range of voltage conversion ratios as the line voltage traverses a cycle. These factors make the design of micro-inverters challenging.

A Multilevel Energy Buffer and Voltage Modulator (MEB) is presented in this chapter. It consists a switched-capacitor circuit and a switched-inductor circuit. It significantly reduces the range of voltage conversion ratios that the dc-ac converter portion of the micro-inverter must operate over by stepping its effective input voltage in pace with the line voltage. The MEB partially replaces the original bulk input capacitor, and functions as an active energy buffer to reduce the total size of the twice-line-frequency energy buffering capacitance. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter stage, leading to a higher overall system efficiency. The MEB architecture can be implemented in a variety of manners, allowing different design tradeoffs to be made. A prototype micro-inverter incorporating an MEB, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for a line cycle average power of 70 W, has been built and tested in grid-connected mode. It is shown that the MEB can successfully enhance the performance of a single-phase grid-interface micro-inverter by increasing its efficiency and reducing the total size of the twice-line-frequency energy buffering capacitance.

This chapter demonstrates that by replacing a single-function, volume-consuming component in a multi-stage system with a more sophisticated circuit block that has multiple functions, the overall system performance can be significantly improved without reducing the system power density.

2.1 Design of Grid-Interfaced Dc-Ac Micro-inverters

In large-scale solar photovoltaic (PV) installations, multiple PV modules (panels) are connected to the electric grid through a single high-power inverter. However, for smaller residential and commercial applications, PV micro-inverters are attractive and are a focus of extensive research in both academia and industry. Each micro-inverter directly connects one PV module to the grid, hence enabling higher overall maximum power point tracking (MPPT) efficiency and improved system reliability by eliminating the potential single point of failure [40–47]. Two important considerations in the design of micro-inverters are converter efficiency and size. The size of the micro-inverter can be reduced by increasing its switching frequency. However, to maintain or enhance efficiency at the higher switching frequencies, advanced topologies and control strategies are necessary.

Recently proposed single-phase micro-inverter architectures have been reviewed in [40–43]. One attractive multi-stage architecture for micro-inverters is shown in Fig. 2-1 [43–45]. It comprises a high frequency resonant inverter, a transformer, and a cycloconverter. The resonant inverter is controlled in such a manner that it produces a high-frequency-sinusoidal current with its amplitude modulated at the line frequency (60 Hz in the US). The high frequency transformer steps up the voltage, and the cycloconverter converts the high frequency current into a sinusoidal line-frequency current, which is injected into the grid. Output power can be controlled by a combination of frequency control and phase-shift control. The twice-line-frequency energy buffering in the circuit of Fig. 2-1 - and in many other micro-inverter architectures - is provided by the input capacitor, C_{IN}, though other methods are possible (e.g., [42,45–48]). Related micro-inverter architectures likewise incorporate a high-frequency inverter and step-up transformation, with subsequent transformation of energy to the line voltage. However, all such architectures must buffer the twice-line-frequency energy and must vary the amplitude of the high frequency output current across a very wide range (e.g., in proportion to the line voltage and the average power delivered by the inverter), posing design and control challenges. For example, if frequency control alone is used to control the amplitude of the output current, the required frequency range can be very wide. Hence, there is an evident need for micro-inverter circuit designs and associated controls that can provide improved performance for operating over wide output voltages and power ranges while providing buffering for the twice-line-frequency power variations.

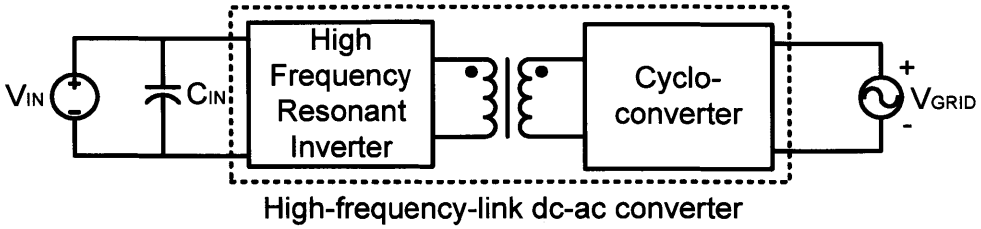


Figure 2-1: Architecture of a micro-inverter incorporating a the twice-line-frequency energy buffer capacitance, C_{IN}, a high-frequency resonant inverter, a transformer and cycloconverter.

The challenges faced by micro-inverters - wide operating voltage and power ranges and the need to buffer the twice-line-frequency energy - also exist in other single-phase grid-interface dc-ac converters. Many approaches have been employed to handle the twice-line-frequency energy concerns, including energy buffers interfaced within the high-frequency portion of the inverter system [45–47], "dc" interface energy buffers that have wider operating range than simple capacitors placed across the panel or elsewhere [19,20,29,48–51], and active power filters placed on the ac side of the system [52], among other approaches. To reduce the required operating ranges of the high-frequency parts of the system, cascaded power stages (such as variable switched-capacitor stages) have sometimes been employed (e.g., [53, 54]). Another approach that has been used is stacking multiple PV modules as part of a multilevel converter to synthesize the ac line voltage [55]. However, this approach is not applicable to single-module micro-inverter systems.

This chapter introduces a new technique to address the above-mentioned challenges. The new technique is one embodiment of the generalized Merged Multi-Stage architecture in dc-ac applications. The new technique shares some of the benefits of both variable-topology cascade converter structures [54] and switched-capacitor energy buffers [19, 20], while enabling very high efficiency to be maintained. The new power converter architecture incorporates a Multilevel Energy Buffer and Voltage Modulator (MEB) to achieve compression of the high-frequency inverter operating range, thereby improving the efficiency of the high-frequency-link dc-ac converter stage. The MEB also partially replaces the original bulk input capacitor and provides the twice-line-frequency energy buffering between dc and ac. By adding this MEB stage, the performance of the high-frequency-link magnetic isolation circuit can be significantly improved.

The remainder of this chapter is organized as follows: Section 2.2 describes the overall architecture of the proposed MEB micro-inverter. A specific implementation of the MEB micro-inverter and its design methodology is described in Section 2.3. Section 2.3 also explains the expected efficiency benefits of this implementation. Section 2.4 describes alternative implementations of the MEB micro-inverter. The design details of a prototype MEB micro-inverter are given in Section 2.5. Section 2.6 presents the experimental results of the MEB micro-inverter tested while connected to the grid, together with estimates of the loss breakdown based on experimental results. Section 2.7 compares the proposed MEB micro-inverter with other recently-proposed micro-inverters to highlight the key contributions of this chapter. Finally, the summary of this chapter are presented in Section 2.8.

2.2 Architecture of the Proposed MEB Micro-inverter

The architecture of the proposed MEB micro-inverter is shown in Fig. 2-2. The MEB is connected in cascade between the input capacitor and a dc-ac converter block. The MEB comprises a Switched-Capacitor Energy Buffer (SCEB) and an optional Charge Control Circuit (CCC). The SCEB is used to modulate the dc-ac converter block's input voltage, v_X, as the line voltage traverses a cycle to reduce the required amount and variations in voltage conversion ratio of the high-frequency dc-ac converter block over the line cycle. Consequently, the operating range of the high-frequency, high-step-up portion of the micro-inverter is reduced. The SCEB also functions as an active energy buffer and helps to reduce the total energy storage requirement for the twice-line-frequency energy buffering by separating the energy buffer voltage from the input (panel) voltage. Since the capacitor(s) in the SCEB can be charged over a wider range than is permissible for a buffer capacitor across the panel output, the required total energy storage (and capacitor size) can be reduced. This represents a form of third-port energy buffering [41, 42, 45–47], providing active control of the energy storage stage, independent of the input and output voltages. The switches in the SCEB switch at low multiples of the line frequency, allowing the SCEB to be highly efficient. The SCEB also steps up the voltage on the primary side of the transformer. Hence, it reduces the transformer primary-side current and the primary-side conduction losses.

The optional CCC provides an additional means to balance the total charge entering and leaving the SCEB over a line cycle, thereby providing greater flexibility in the operation

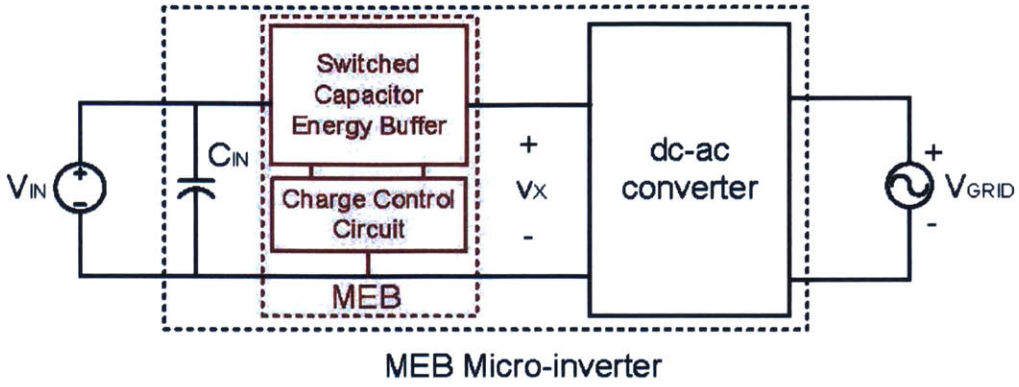


Figure 2-2: Architecture of the proposed MEB micro-inverter. It incorporates a MEB and a dc-ac converter. Although here the MEB is shown on the dc side of the micro-inverter, an alternative is to incorporate the MEB function on the ac side of the micro-inverter, as discussed in section 2.4.

of the SCEB. The power rating of the CCC is a fraction of the power rating of the MEB micro-inverter, and it only operates over part of the line cycle. Hence, it can be small and its losses do not substantially impact the overall efficiency of the micro-inverter. The small additional loss of the MEB can be compensated by the improved efficiency of the dc-ac converter block, leading to a higher overall system efficiency.

Although in this chapter we present the use of the MEB in the context of a micro-inverter, this MEB based architecture can be applied more broadly to converters interfacing between low-voltage dc and the single-phase ac grid.

2.3 Design of An Example MEB Micro-inverter

There are many possible implementations of the proposed MEB micro-inverter and the MEB itself, allowing trade-offs to be made between complexity and performance. In this section we describe an example MEB micro-inverter implementation and its design methodology. The full system architecture and some operating waveforms are shown in Fig. 2-3. The main power path of this architecture consists of two stages: a MEB stage and a dc-ac converter stage. The MEB stage synthesizes a multilevel voltage v_X that is the input voltage of the dc-ac converter. The multilevel voltage v_X steps in pace the line voltage, thus reducing the required voltage conversion range of the dc-ac converter. The dc-ac converter is a high-frequency-link resonant converter, incorporating a series resonant inverter, a high-

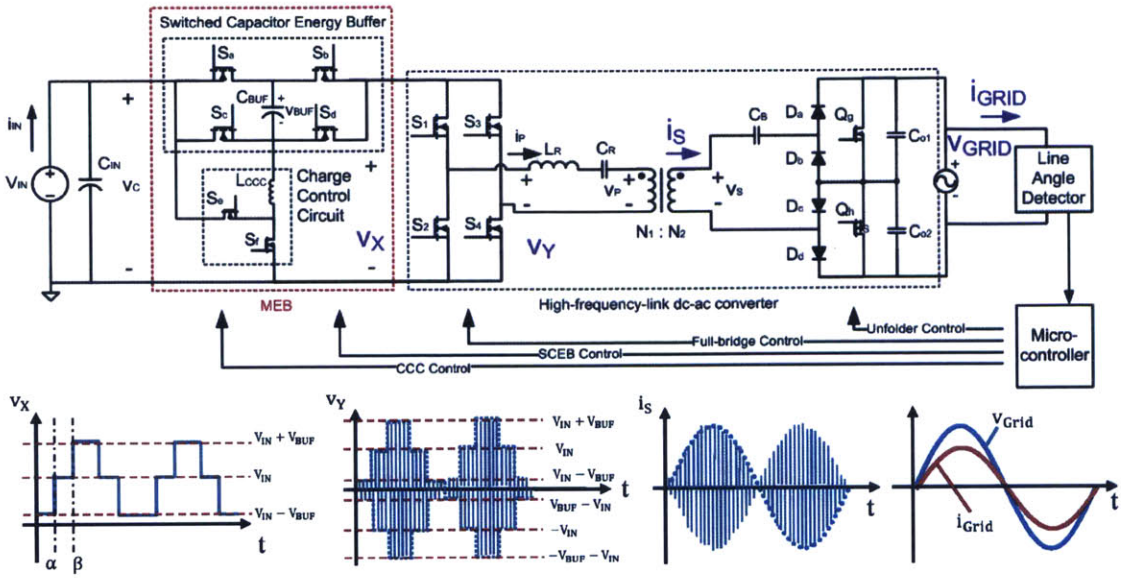


Figure 2-3: One implementation of the MEB micro-inverter and its conceptual operating waveforms: v_X is the multilevel voltage synthesized by the MEB stage; v_Y is a high frequency voltage created by the H-bridge; i_S is the current of the resonant tank with a sinusoidal envelope; v_{GRID} and i_{GRID} are the line voltage and the line current.

frequency transformer and a cycloconverter. The series resonant inverter creates a high frequency current i_S with the line-frequency sinusoidal voltage envelope. The high frequency current i_S is then processed by the cycloconverter to generate a line-frequency current that is injected into the grid. Since the dc-ac converter is switching at a high frequency, the high frequency components remaining after the cycloconverter can be filtered by two small output capacitors C_{o1} and C_{o2}. The full system also includes a line angle detector circuit and a micro-controller unit (MCU). We first describe the design of the MEB, and then the design of the high-frequency dc-ac converter stage.

2.3.1 Design of the MEB

One implementation of the MEB is shown in Fig. 2-4a. The MEB has two subsystems: a Switched-Capacitor Energy Buffer (SCEB) and an associated Charge-Control Circuit (CCC). The SCEB comprises four switches, connected as a full bridge, and one buffer capacitor C_{BUF}. The switches of the SCEB change state at line angles α, β, $(180° - \beta)$ and $(180° - \alpha)$ to generate the dc-ac converter input voltage v_X shown in Fig. 2-4b. When the

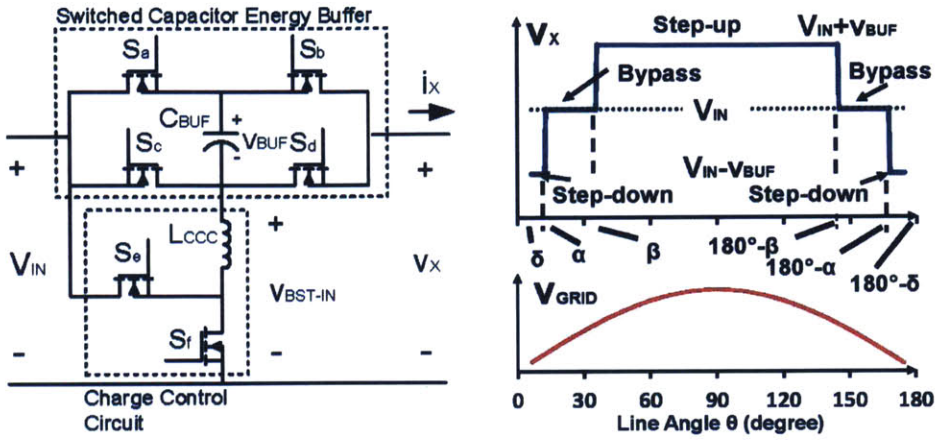
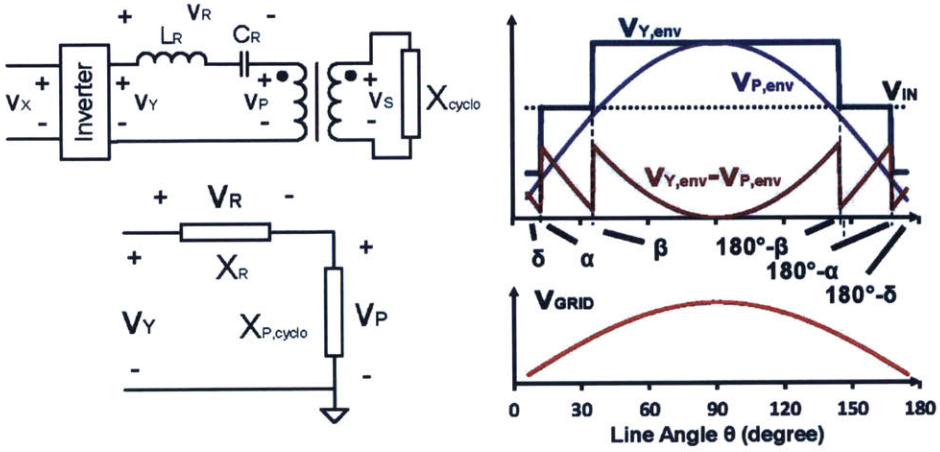


Figure 2-4: One embodiment of the proposed MEB: (a) MEB circuit implementation, and (b) waveform of v_X relative to v_{GRID} during a half line-cycle.

magnitude of the line voltage, $|v_{GRID}|$, is low (corresponding to $\theta \in [0°, \alpha] \cup [180° - \alpha, 180°]$, i.e., line angles in the range 0° to α and $180° - \alpha$ to 180°), the SCEB operates in the Step-down Mode with S_a and S_d on (S_b and S_c off) and $v_X = V_{IN} - v_{BUF}$; when $|v_{GRID}|$ is in the mid-range ($\theta \in [\alpha, \beta] \cup [180° - \beta, 180° - \alpha]$), the SCEB operates in the Bypass Mode (S_a, S_b on) and $v_X = V_{IN}$; and when $|v_{GRID}|$ is high ($\theta \in [\beta, 180° - \beta]$), the SCEB operates in the Step-up Mode (S_b, S_c on) and $v_X = V_{IN} + v_{BUF}$. In Fig. 2-4b and the following analysis, C_{BUF} is assumed to be large enough that v_{BUF} does not vary significantly over a line cycle. With the SCEB operated in this manner, v_X is modulated in pace with the line voltage, yielding a significantly compressed range of voltage conversion ratios for the high-frequency converter. The three SCEB modes repeat periodically every half-line cycle. Each switch changes state twice in each half-line cycle, leading to low switching loss of the SCEB.

In Fig. 2-4b, v_X is not specified for line angles close to the zero crossings of the line. At the zero crossings (i.e., when $\theta = 0°$ and $\theta = 180°$), the output current needs to approach zero in a continuous manner to achieve a perfect power factor. This is practically unachievable under continuous modulation of the converter. To limit the operating frequency range of the dc-ac converter block, a dead-angle, δ, of several degrees is introduced before and after the zero-crossings of the line voltage, during which time the micro-inverter is shut-off and no current is injected into the grid (though other strategies could be used). In this chapter, a δ of 6° is selected.



(a) (b)

Figure 2-5: (a) Model of the dc-ac converter stage. Here X_R is the impedance of the resonant tank, X_{cyclo} is the impedance of the cycloconverter (rectifier/unfolder), and $X_{P,cyclo}$ is the impedance of the cycloconverter reflected to the primary side of the transformer. (b) Waveforms of the envelope of v_Y, v_P ,$v_Y - v_P$ and v_{GRID} relative to the line voltage during a half line-cycle.

The design of the MEB involves selecting optimal values for the three design parameters: v_{BUF}, α and β, so as to achieve the maximum reduction in dc-ac converter block's operating range. To minimize this operating range we must minimize the maximum voltage drop across the resonant tank, v_R, over the line cycle. This is equivalent to minimizing the difference between the envelope of the high frequency output voltage of the full bridge, $v_{Y,env}$, and the envelope of the voltage across the primary side of the transformer, $v_{P,env}$ (see Fig. 2-5). Note $v_{P,env}$ is sinusoidal and in phase with v_{GRID}. In this work, with δ chosen as 6°, to minimize the operating range of the dc-ac converter, the optimal value of v_{BUF} is $0.6V_{IN}$, α is 12.8°, and β is 40.9°. These control parameters yield a multilevel voltage that optimally approximates a line-synchronized sinusoidal voltage. Detailed derivations of these control parameters are provided in Appendix A.1.

With these design parameters, a CCC which maintains the charge balance of C_{BUF} (hence maintaining v_{BUF}) is needed. An example implementation of the CCC is shown in Fig. 2-4a, where a modified boost converter connects the negative terminal of C_{BUF} to the MEB input. The output voltage of this boost converter is fixed (V_{IN}), while its input voltage is regulated (v_{BST-IN}). When S_a is on, regulating v_{BST-IN} effectively regulates v_{BUF}. The CCC switches at a higher frequency than the operating frequency of the SCEB, acting as a

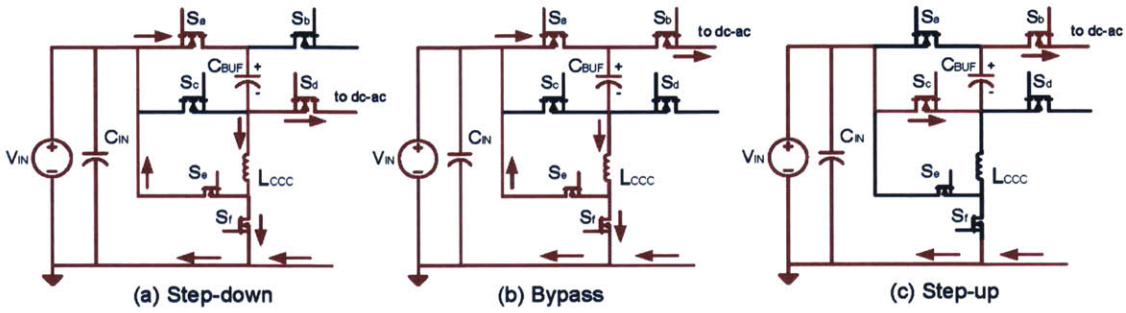


Figure 2-6: Current flow directions in the MEB during the three operating modes: (a) Step-down mode, (b) Bypass mode and (c) Step-up mode.

controlled current source. In the Step-down mode, the CCC and the dc-ac converter charge C_{BUF} adiabatically; in the Bypass mode, the CCC continues to charge C_{BUF} adiabatically; and in the Step-up mode, the CCC is turned off, and C_{BUF} is discharged adiabatically by the dc-ac converter. Figure 2-6 shows the current flow directions in the MEB during the three operating modes. In this design, the CCC operates in continuous conduction mode (CCM) with the duty-ratio of switch S_e fixed at 0.4. This keeps v_{BST-IN} stable at $0.4V_{IN}$, maintaining v_{BUF} at $0.6V_{IN}$ as required. With this control, v_X equals $1.6V_{IN}$ during the Step-up mode, V_{IN} during the Bypass mode, and $0.4V_{IN}$ during the Step-down mode (as shown in Fig. 2-4b).

In the steady state, the buffer capacitor C_{BUF}, is charged when the line voltage is low, and is discharged when the line voltage is high. However, before the system enters periodic steady state operation, v_{BUF} needs to be precharged to $0.6V_{IN}$. The CCC implementation described above has a built-in feedback mechanism which automatically precharges C_{BUF} to this level without the need for additional control. For example, if v_{BUF} is less than $0.6V_{IN}$ either during the startup or because of disturbances, then during the Step-down mode, since v_X will be larger than $0.4V_{IN}$, the fixed duty ratio control of the CCC will charge up C_{BUF}. Furthermore, during the Step-up mode, since v_X will be smaller than the desired value of $1.6V_{IN}$, the dc-ac converter block will have a lower input voltage and thus draw less charge from C_{BUF}. As a result, C_{BUF} has a positive net charge during one line cycle and v_{BUF} increases. This process is repeated over a few line cycles until v_{BUF} reaches its steady state value of $0.6V_{IN}$. Because the input voltage of the CCC boost converter is regulated, it behaves similar to a buck converter, which remains stable in the face of disturbances.

The line-synchronized multilevel voltage v_x significantly reduces the required voltage conversion range of the dc-ac converter, resulting in higher dc-ac converter efficiency. To achieve high overall system efficiency, the MEB stage itself also needs to be very efficient. The switches of the SCEB are switched at multiplies of line frequency and its loss is dominated by conduction loss, which can be kept low by using semiconductor devices with low on-resistance. The CCC is very efficient because of its relatively low voltage rating and fixed voltage conversion ratio. In addition, the average power processed by the CCC circuit is only a fraction of the average output power of the micro-inverter. With the previously-indicated control parameters, only 44.43% of the average output power is processed by the CCC (as shown in Appendix A.2). As a result, the loss caused by the CCC circuit only penalizes a portion of the total power of the micro-inverter, resulting in high overall system efficiency.

Many micro-inverter topologies require all the twice-line-frequency energy buffering to be done by a capacitor placed across the PV panel (e.g., C_{IN} in Fig. 2-1) [43, 44]. This makes the size of the energy buffering capacitor large, since there is a limit (of typically 10% peak-to-peak) on the maximum voltage ripple allowed across the PV panel (to ensure it is operating near it maximum power point) resulting in a low utilization of the energy in C_{IN}. In the MEB micro-inverter, the buffer capacitor, C_{BUF}, absorbs energy when the SCEB is in the Step-down or Bypass mode (i.e., when the power delivered to the grid is low), and delivers energy to the grid when the SCEB is in the Step-up mode (i.e., when the power delivered to the grid is high). In this way, C_{BUF} functions as the storage element of an active energy buffer and can be used to replace the C_{IN} with smaller size. Since C_{BUF} is not across the PV panel, a larger voltage ripple is allowed across it than would otherwise be permissible. This increases the utilization of energy in C_{BUF} and allows a smaller capacitor to be used, creating spaces for the added semiconductor devices in the MEB. As a result, the overall size of the MEB stage (plus a much smaller input capacitor) is demonstrated to be equivalent to the size of the original bulk input capacitor. The size of the MEB stage can potentially be further reduced by using a Stacked Switched Capacitor (SSC) energy buffer instead of a single capacitor [19, 20].

2.3.2 Design of the dc-ac converter stage

A series-resonant high-frequency-link dc-ac converter is chosen as the dc-ac converter stage. The MEB provides two benefits to the dc-ac converter stage: a reduced transformer turns ratio, and a compressed operation range.

The transformer turns ratio of the dc-ac converter stage needs to satisfy $\frac{N_2}{N_1} > \frac{v_{S,1}(\theta)}{v_{P,1}(\theta)}$, where $v_{P,1}$ and $v_{S,1}$ are the fundamental components of v_P and v_S (Fig. 2-3). Without the MEB, assuming square-wave switching of a full-bridge, $v_{P,1} = \frac{4}{\pi} V_{IN} \sin(\theta)$, and $v_{S,1} = \frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)$; thus:

$$\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)}{\frac{4}{\pi} V_{IN} \sin(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{2V_{IN}}. \tag{2.1}$$

This is a lower bound on the required transformer turns ratio if there is no MEB. With the MEB, as described in Appendix A.1, $v_{P,1} = \frac{4}{\pi}(V_{IN}+V_{BUF}) \sin(\theta)$, and $v_{S,1} = \frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)$; thus:

$$\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\frac{2\sqrt{2}}{\pi} V_{GRID,rms} \sin(\theta)}{\frac{4}{\pi}(V_{IN} + V_{BUF}) \sin(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{2(V_{IN} + V_{BUF})}. \tag{2.2}$$

If $v_{BUF} = 0.6V_{IN}$, then $\frac{v_{S,1}(\theta)}{v_{P,1}(\theta)} = \frac{\sqrt{2} V_{GRID,rms}}{3.2V_{IN}}$. In this case, ideally the MEB reduces the transformer turns ratio of the dc-ac converter stage by a factor of 1.6.

The MEB also provides unique opportunities in the control of the dc-ac converter stage. To keep the explanation of this benefit simple, we assume in the following analysis that the dc-ac converter stage is under pure frequency control. In practice, both frequency control and phase-shift control are used. When the micro-inverter has no MEB, and if the resonant inverter is designed to operate at its resonant frequency when the line voltage is at its peak, then its required switching frequency, f_{noMEB}, as function of line angle θ ($0° < \theta < 180°$), is given by:

$$f_{noMEB}(\theta) = \frac{\frac{X_{cyclo} C_R}{N^2} |\cot(\theta)| + \sqrt{(\frac{X_{cyclo} C_R}{N^2} \cot(\theta))^2 + 4L_R C_R}}{4\pi L_R C_R}. \tag{2.3}$$

Here, L_R and C_R are the inductance and the capacitance of the resonant tank, respectively, N ($= \frac{N_2}{N_1}$) is the transformer turns ratio, and X_{cyclo} is the impedance of the cycloconverter (or rectifier/unfolder). Under fundamental frequency approximation, for a unity power factor micro-inverter, X_{cyclo} is resistive and given by $\frac{4V_{IN}^2}{\pi^2 P_{OUT(avg)}}$. When the micro-inverter

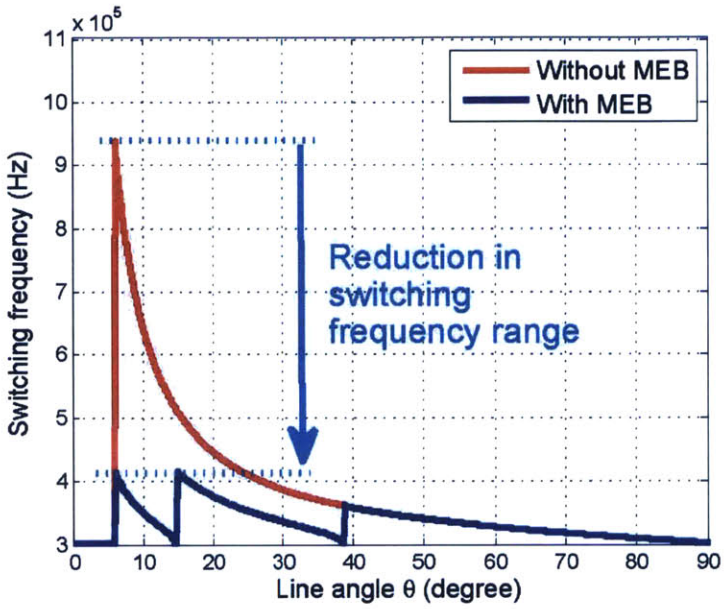


Figure 2-7: Calculated switching frequencies of the micro-inverter over a quarter line cycle with and without the MEB with only frequency control, plotted for $P_{\mathrm{OUT(avg)}}$ equals 70 W, $C_{\mathrm{R}} = 62$ nF, $L_{\mathrm{R}} = 4.5$ μH, $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{BUF}} = 16.2$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$. The transformer turns ratio for the micro-inverter with the MEB is 5:28, and the transformer turns ratio for the micro-inverter without the MEB is 4:28. The value of $X_{\mathrm{P,cyclo}}$ is 10.7 Ω for the micro-inverter with the MEB, and is 4.22 Ω without the MEB.

is designed with the MEB, the required switching frequency, f_{MEB}, as a function of line angle is given by:

$$f_{\mathrm{MEB}}(\theta) = \frac{C_{\mathrm{R}}|X_{\mathrm{R}}(\theta)| + \sqrt{C_{\mathrm{R}}^2 X_{\mathrm{R}}(\theta)^2 - 4L_{\mathrm{R}}C_{\mathrm{R}}}}{4\pi L_{\mathrm{R}}C_{\mathrm{R}}}. \tag{2.4}$$

Here, $|X_{\mathrm{R}}(\theta)|$ is the magnitude of the impedance of the resonant tank and is given by:

$$|X_{\mathrm{R}}(\theta)| = \sqrt{(\frac{X_{\mathrm{cyclo}}v_{\mathrm{X}}(\theta)}{N^2(V_{\mathrm{IN}}+V_{\mathrm{BUF}})\sin(\theta)})^2 - (\frac{X_{\mathrm{cyclo}}}{N^2})^2}, \tag{2.5}$$

where $v_{\mathrm{X}}(\theta)$ is the inverter input voltage as shown in Fig. 2-4b, and X_{cyclo} equals $\frac{4(V_{\mathrm{IN}}+V_{\mathrm{BUF}})^2}{\pi^2 P_{\mathrm{OUT(avg)}}}$. Figure 2-7 illustrates the difference in switching frequency operating range across a half-line cycle for the micro-inverter without and with the MEB (computed using (2.3), (2.4), respectively). When the resonant frequency of the inverter is chosen to be 300 kHz, the MEB compresses the switching frequency range from 300-950 kHz to 300-410 kHz.

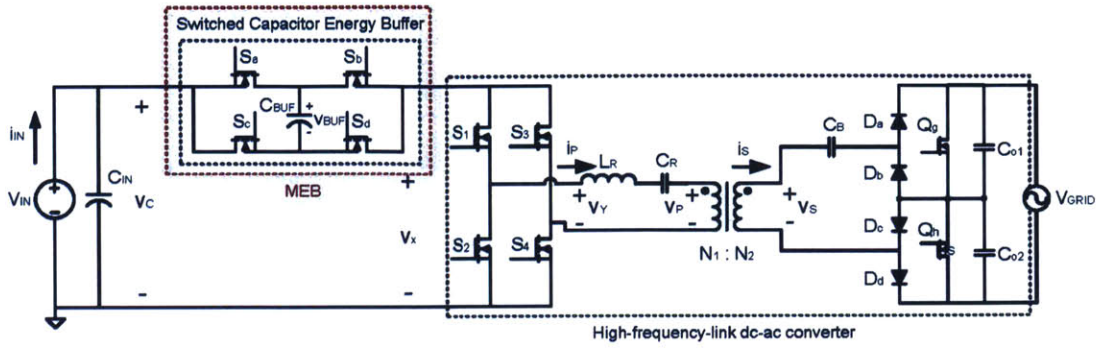


Figure 2-8: Schematic of a simplified MEB micro-inverter without the CCC. The charge balance of C_{BUF} is achieved by keeping $cos(\alpha) + cos(\beta) = cos(\delta)$. The SCEB can also be operated in a PWM manner.

2.4 Alternative Implementations

The MEB micro-inverter architecture proposed here has many alternative implementations, providing additional design flexibility and tradeoff possibilities. The alternatives are at the level of each sub-block of the architecture, as well as at the overall system level.

Figure 2-8 shows an alternative MEB micro-inverter architecture with a simplified MEB stage without the CCC. By controlling the switching angles of the SCEB (for example, making the switching angles α, β, and δ satisfy $cos(\alpha) + cos(\beta) = cos(\delta)$ as shown in Appendix A.3), the charge balance of the C_{BUF} is automatically achieved, thus the CCC can be eliminated, reducing the circuit complexity (while the benefits of the MEB stage to the dc-ac converter are also reduced). Another way is to operate the switches of the SCEB at a higher switching frequency, e.g. in a PWM manner, to synthesize the required voltage difference between a dc voltage and a sinusoidal voltage. The charge balance of C_{BUF} can be obtained by phase-shifting the switches. When the switching frequency of the SCEB is comparable to the switching frequency of the dc-ac converter, the MEB stage can be merged with the inverter switches of the dc-ac converter and becomes a high frequency switched capacitor energy buffer (more closely resembling the system of [45], which has higher switching loss and control complexity). This chapter focuses on exploring the concept of combining a low-frequency switched-capacitor stage with a high-frequency dc-ac stage to inherit their strengths in handling different tasks. As a result, a low frequency SCEB with the CCC is selected to minimized the operation range of the dc-ac converter.

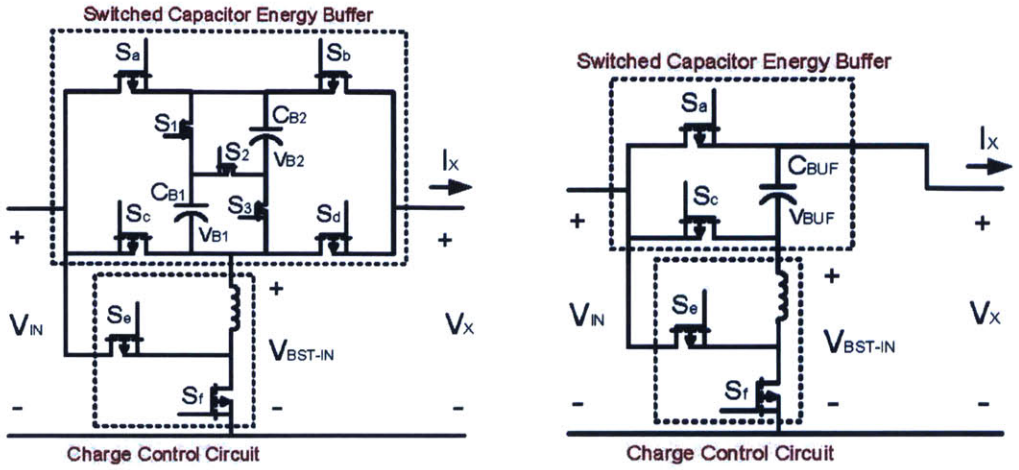
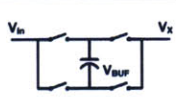
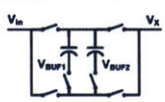
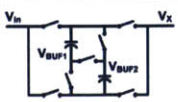
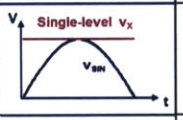
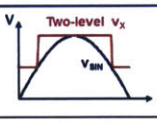
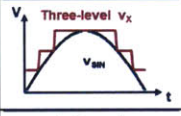
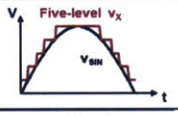
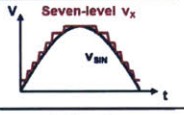


Figure 2-9: Topological extensions of the MEB enabling tradeoffs between circuit complexity and performance: (a) A modified MEB stage with seven v_x levels: (1) v_x equals $V_{IN} - v_{B1} - v_{B2}$ when S_a, S_2, S_d are on (and other switches in the SCEB are off) ; (2) v_x equals $V_{IN} - v_{B1}$ when S_a, S_1, S_d are on; (3) v_x equals $V_{IN} - v_{B2}$ when S_a, S_3, S_d are on; (4) v_x equals V_{IN} when S_a, S_b are on; (5) v_x equals $V_{IN} + v_{B2}$ when S_b, S_3, S_c are on; (6) v_x equals $V_{IN} + v_{B1}$ when S_b, S_1, S_c are on; (7) v_x equals $V_{IN} + v_{B1} + v_{B2}$ when S_b, S_2, S_c are on. (b) A modified MEB stage with two v_x levels: (1) v_x equals V_{IN} when S_a is on; (2) v_x equals $V_{IN} + v_{BUF}$ when S_c is on.

In the SCEB, by adding one capacitor and three switches, a modified MEB implementation shown in Fig. 2-9a can be created. This MEB implementation can produce seven levels of v_x and hence synthesizes a voltage that more closely approximates the ac line voltage envelope, leading to further reduction in the operating range of the dc-ac converter. On the other hand, by removing S_b and S_d from the original MEB implementation, the modified implementation shown in Fig. 2-9b can be created. While this implementation has fewer switches, it only generates a v_x having two levels, limiting the compression of the voltage conversion range. To investigate the tradeoff between circuit complexity and performance for the variants of the SCEB, Table 2.1 shows and compares the schematics, waveforms, number of switches and frequency modulation ranges of the dc-ac converter if a single capacitor, a two-level SCEB, a three-level SCEB, a five-level SCEB or a seven-level SCEB is used. Increasing v_x levels compresses the required frequency modulation range (or, more generally, the operating range) of the dc-ac converter, at the cost of higher circuit complexity.

On the overall system level, an alternative implementation of the MEB micro-inverter

Table 2.1: Schematics, waveforms, number of switches and frequency modulation ranges of a single capacitor, a two-level SCEB, a three-level SCEB, a five-level SCEB and a seven-level SCEB. The frequency modulation range is calculated for the same setup as that used in Fig. 2-7.

	Single Capacitor	Two-Level SCEB	Three-Level SCEB	Five-Level SCEB	Seven-Level SCEB
Schematic					
Modulated Multilevel V_X	V_{in}	V_{in} $V_{in} - V_{BUF}$	$V_{in} + V_{BUF}$ V_{in} $V_{in} - V_{BUF}$	$V_{in} + V_{BUF2}$ $V_{in} + V_{BUF1}$ V_{in} $V_{in} - V_{BUF1}$ $V_{in} - V_{BUF2}$	$V_{in} + V_{BUF1} + V_{BUF2}$ $V_{in} + V_{BUF2}$ $V_{in} + V_{BUF1}$ V_{in} $V_{in} - V_{BUF1}$ $V_{in} - V_{BUF2}$ $V_{in} - V_{BUF1} - V_{BUF2}$
Voltage Waveforms					
Complexity	1 Capacitor 0 Switch	1 Capacitor 2 Switches	1 Capacitor 4 Switches	2 Capacitors 6 Switches	2 Capacitors 7 Switches
Frequency Modulation Range	300kHz~950kHz	300kHz~600kHz	300kHz~410kHz	300kHz~350kHz	300kHz~320kHz

is to have the MEB stage on the ac side instead of on the dc side. Instead of synthesizing an approximated replica of the ac line voltage amplitude from the dc input, the MEB stage synthesizes an approximately constant voltage amplitude from the ac line. Hence, it also reduces the voltage conversion range of the high-frequency portion of the system. More details about the operation of the ac side MEB are provided in Appendix A.4. Compared to the dc side MEB, the higher operating voltage of the ac side MEB reduces the conduction loss and the total capacitor size (since higher voltage rating capacitors tend to have higher energy density). However, due to the higher operating voltage, the CCC has significantly higher switching loss. Furthermore, since the MEB stage is connected directly to the ac line, this implementation is more complex to drive and control.

Different alternatives have different advantages and drawbacks in different applications. Since the wide voltage conversion range is a key bottleneck of the micro-inverter incorporating a high-frequency-link resonant dc-ac converter, a MEB that optimally compresses the voltage conversion range of the dc-ac converter is demonstrated in this chapter.

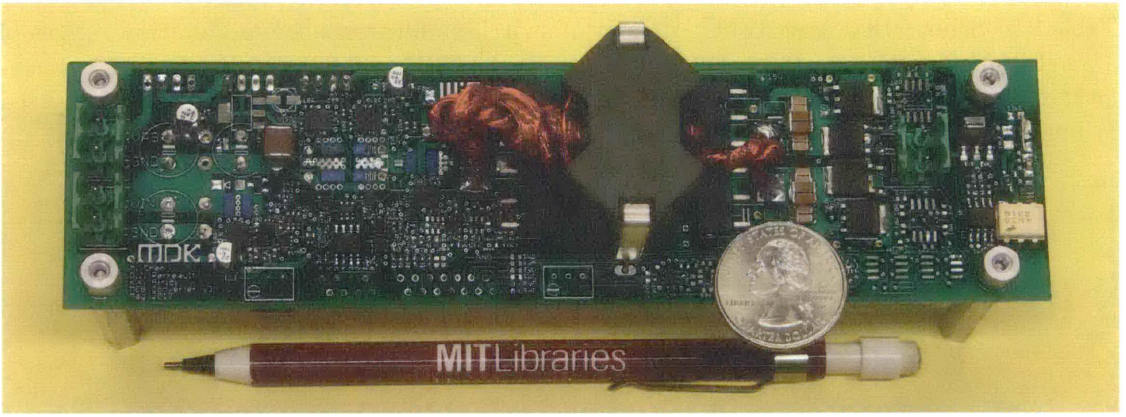


Figure 2-10: Picture of the prototype MEB micro-inverter. Also shown are a pencil and a US quarter to indicate relative size.

2.5 Prototype Micro-Inverter

To validate the proposed architecture, a prototype MEB micro-inverter, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for 70 W (line cycle average power), has been built, tied to the grid and tested. The peak power rating of the dc-ac converter stage is 140 W, and the peak power rating of the CCC is 68 W. A photograph of the prototype is shown in Fig. 2-10. Also shown are a pencil and a US quarter to indicate relative size. For comparison purposes, a high-frequency-link micro-inverter without the MEB (and with a different transformer turns ratio) has also been built and tested (on the same PCB board with a blank MEB stage). The schematic of these two prototypes are shown in Fig. 2-11. The components used in these two prototypes are listed in Table 2.2. The board area used by the various functional blocks in the case of the micro-inverter with the MEB is shown in Fig. 2-12. The MEB stage collectively uses 14.3% of the total board area. The micro-inverter without the MEB is implemented on the same board with the space of the MEB replaced by additional input capacitors. Figure 2-13a shows the back side of the board where some major passive components - C_{IN}, C_{BUF}, L_{CCC}, and L_R - are placed. The transformer is on the front side of the board and is shown in Fig. 2-10.

The switch and gate drive implementations of the MEB are shown in Fig. 2-14. The required voltage and current ratings of the six switches in the MEB stage are listed in Table 2.3. S_a has the highest current rating because it needs to handle the sum of the

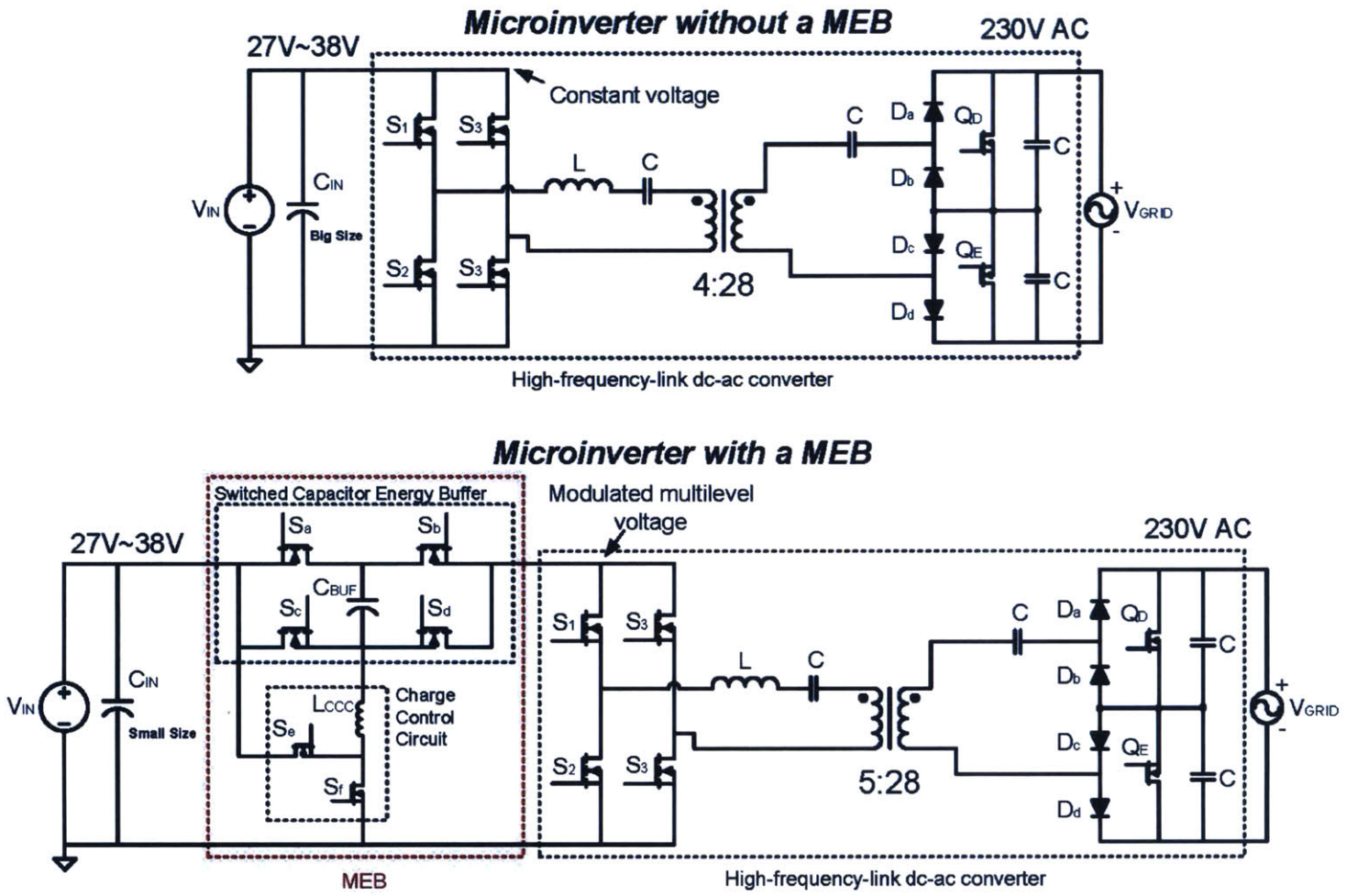


Figure 2-11: Schematics of the prototyped micro-inverter without and with the MEB. The MEB stage replaces the original bulk input capacitor. A small C_{IN} is still needed to hold the voltage across the solar panel constant.

Table 2.2: Micro-inverter Component Lists for the schematic shown in Fig. 2-11.

Name	With MEB	Without MEB
C_{IN}	3 × 1 mF, 50 V, Panasonic ECA-1HM102 (3.4 cm^3 each)	5 × 1 mF, 50 V, ECA-1HM102 (3.4 cm^3 each)
C_{BUF}	5.6 mF, 25 V, Panasonic EEU-HD1E562 (5.4 cm^3)	Not required
C_{o1} & C_{o2}	Two EPCOS film capacitors, 0.2 uF, 630 V, 2 cm^3	
Total Cap Size	15.6 cm^3	17 cm^3
$S_{b,d}$	EPC2016 100 V 11 A GaN FETs	
$S_{a,c,e,f,1,2,3,4}$	EPC2001 100 V 25 A GaN FETs	
$Q_{g,h}$	Infineon IPD65R380C6 CoolMOS MOSFETs	
$D_{a,b,c,d}$	CREE CSD01060 SiC Schottky diodes	
L_R	4.3 uH, R_{dc} smaller than 4mΩ, size: 15.75 cm^3; Core area: 3 cm^2	
L_{CCC}	10 uH, R_{dc} smaller than 10 mΩ, size: 1 cm^3	Not needed
C_R	60 nF (10nF × 6) 100 V 1206 C0G Ceramic	
Transformer	RM12-3F3, Primary: 5 turns, Secondary: 28 turns	RM12-3F3, Primary: 4 turns, Secondary: 28 turns
CCC control	fixed duty ratio control with LTC6992 VCO	Not Needed
Full bridge timing	LTC6990 VCO with LTC6994 time delay block	
Gate drive ICs for Ss	TI LM5113; Five half-bridge pairs: (S_a-S_c), (S_b-S_d), (S_e-S_f), (S_1-S_2), (S_3-S_4)	
Gate Drive ICs for Qs	Silicon labs Si8420 digital isolator	
Optocoupler	Fairchild 4N35 optocoupler	

current of the CCC and the dc-ac converter block. S_b and S_c have higher current ratings than S_d because they are conducting in the step-up mode when the line current is high. Gallium Nitride (GaN) switches manufactured by EPC (Efficient Power Conversion, Inc., a semiconductor company) are selected and intentionally oversized. This improves the transient and fault capability, with negligible increase in overall area. Further optimizations can be made if more advanced GaN switches become available. Three half-bridge gate drives (LM5113) drive these six switches. The gate drive IC for S_e and S_f is referenced to ground. The gate drive ICs for S_a, S_b, S_c, and S_d are referenced to the negative terminal of C_{BUF}, and can be powered by v_{BUF} through a 5V linear regulator when v_{BUF} is larger than 5 V. In the precharge period, S_a conducts in reverse to charge C_{BUF} when v_{BUF} is smaller than 5 V. As

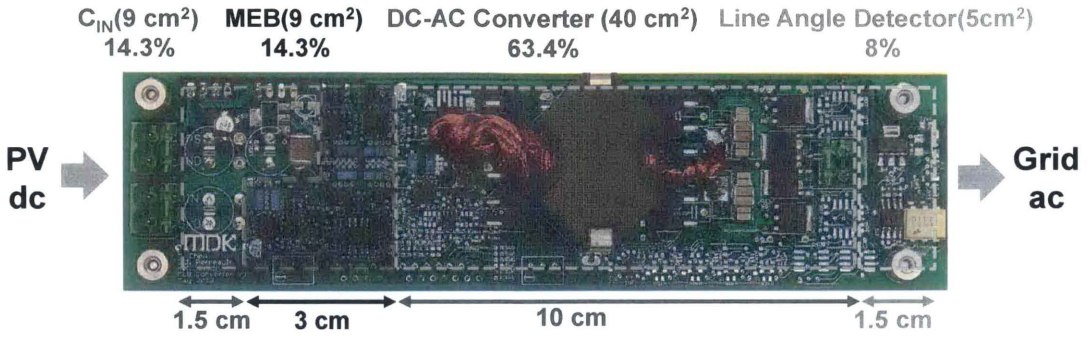


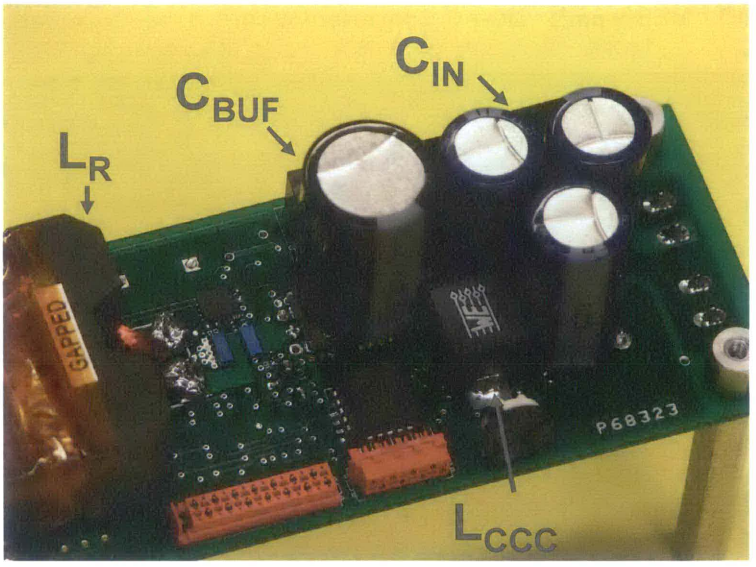
Figure 2-12: Board area used by the various functional blocks of the MEB micro-inverter. The micro-inverter without the MEB is implemented on the same board with the space labeled as "MEB" replaced by additional input capacitors. The ac power density is about 1W/cm^3.

Table 2.3: Required voltage ratings (maximum blocking voltage) and current ratings (maximum rms current) of the power switches in the MEB stage. $V_{\text{IN(max)}}$ is the maximum input voltage (38 V). $V_{\text{IN(min)}}$ is the minimum input voltage (27 V). $P_{\text{OUT(avg,max)}}$ is the maximum line cycle average output power (70 W). $\alpha = 12.8°$ and $\beta = 40.9°$. D is the duty ratio of S_e (0.4). γ_{CCC} is the fraction of line cycle average output power processed by the CCC (44.43%). The peak power rating of the prototype micro-inverter is 140 W.

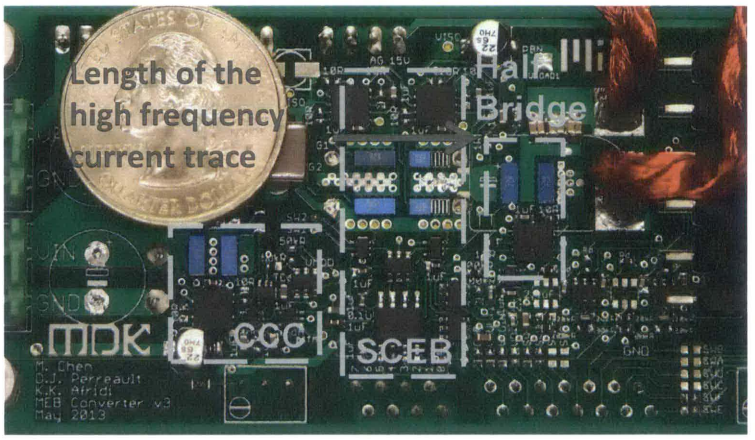
Switch	Required voltage rating	Required current rating
S_a	23 V [$=(1-D)\,V_{\text{IN(max)}}$]	7.40 A [$=\frac{90°\gamma_{\text{CCC}}P_{\text{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\text{IN(min)}}} + \frac{2P_{\text{OUT(avg,max)}}}{(1+D)V_{\text{IN(min)}}}\sin(\beta)$]
S_b	23 V [$=(1-D)\,V_{\text{IN(max)}}$]	3.24 A [$=\frac{2P_{\text{OUT(avg,max)}}}{(1+D)V_{\text{IN(min)}}}$]
S_c	23 V [$=(1-D)\,V_{\text{IN(max)}}$]	3.24 A [$=\frac{2P_{\text{OUT(avg,max)}}}{(1+D)V_{\text{IN(min)}}}$]
S_d	23 V [$=(1-D)\,V_{\text{IN(max)}}$]	0.72 A [$=\frac{2P_{\text{OUT(avg,max)}}}{(1+D)V_{\text{IN(min)}}}\sin(\alpha)$]
S_e	38 V [$=V_{\text{IN(max)}}$]	2.11 A [$=(1-D)\frac{90°\gamma_{\text{CCC}}P_{\text{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\text{IN(min)}}}$]
S_f	38 V [$=V_{\text{IN(max)}}$]	3.16 A [$=D\frac{90°\gamma_{\text{CCC}}P_{\text{OUT(avg,max)}}}{(90°-\beta)(1-D)V_{\text{IN(min)}}}$]

a result, no isolated power supply for the gate drive is needed. The high-frequency-current ripple created by the full bridge passes through the SCEB and is buffered by C_{IN}. The size of the MEB stage is compared to a US quarter in Fig. 2-13b. Figure 2-13b also shows the length of the high frequency current path through the SCEB switches. The extremely small size of the GaN switches and careful PCB layout enables low parasitic inductances and mitigates possible parasitic effects. The CCC is designed to switch at 500 kHz.

The four switches in the full-bridge inverter (S_1-S_4) are also GaN switches. Their low output capacitance enables high-frequency switching, and helps to reduce any loss caused



(a)



(b)

Figure 2-13: (a) Photograph of the back side of the board showing: C_{IN}, C_{BUF}, L_{CCC}, and L_R. (b) PCB layout of the MEB comparing the size of the MEB and a US quarter. The area of the high-frequency current loop is minimized.

by the stepped waveform of v_X. A 4.5 μH inductor and a 60 nF (6 $\times$ 10nF) C0G ceramic capacitor (with low equivalent series resistance) form the series resonant tank of the inverter, with a resonant frequency of 300 kHz. The dc-ac converter stage is operated above the resonant frequency to achieve ZVS soft switching. The MEB increases the input voltage of the dc-ac converter stage during a portion of the line cycle. As a result, the peak voltage stress of the switches in the full-bridge is higher than in the micro-inverter without a MEB. However, the current stress of the full-bridge switches is reduced with the MEB present.

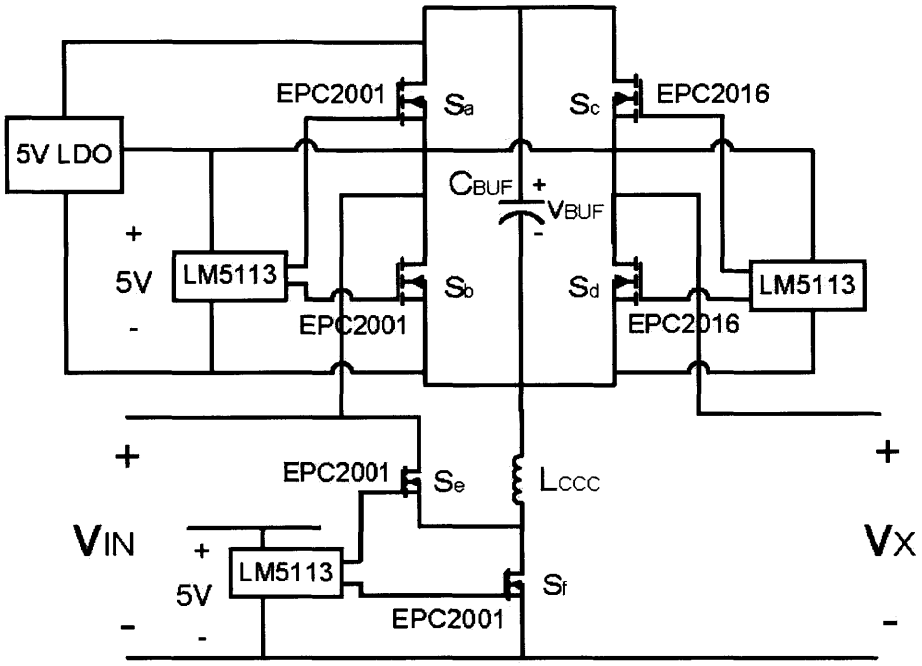


Figure 2-14: Switch and gate drive implementation of the MEB.

The MEB reduces the transformer turns ratio. However, since the transformer volt-seconds and the number of turns on the secondary are the same with or without the MEB, the MEB converter has more primary side turns. The transformer turns ratio is 4:28 in the converter without the MEB, and 5:28 in the MEB converter.

Four Cree CSD01060 Silicon Carbide (SiC) diodes and two Infineon IPD65R380C6 power transistors are used for the combined rectifier and unfolder stage (cycloconverter). While using diodes increases the losses in the cycloconverter stage, it avoids the control complexity of synchronous conversion. To further improve efficiency, synchronous cycloconverter designs similar to those in [44, 45] can be used. If a synchronous cycloconverter is implemented, power can be controlled by phase shifting the full-bridge inverter relative to the cycloconverter in addition to frequency control, full-bridge phase-shift control, and burst-mode control of the inverter (e.g., [6–8, 44, 45, 57]).

An opto-isolated line angle detector is implemented to synchronize the micro-inverter with the grid. It senses the zero crossing and the polarity of the line voltage, and computes the line angle. A state machine triggered by the line angle detector is implemented in a micro-controller (MCU). The state machine uses the line angle and a look-up table to control

Table 2.4: Look-up table for the Micro-controller of the Micro-inverter without and with the MEB when $V_{IN} = 30$ V and $P_{OUT(avg)} = 70$ W.

	Without MEB		**With MEB**				
Line angle θ	f_{FM}(kHz)	$\delta_{PM}(°)$	**SCEB Mode**	**CCC**	f_{FM}(kHz)	$\delta_{PM}(°)$	**Cycloconverter**
0° → 6°	dead-angle (Micro-inverter off)						
6° → 15°	500	20	Step-down	On	368	20	Q_h on, Q_g off
15° → 20°	470	20	Bypass	On	325	16	Q_h on, Q_g off
20° → 25°	454	20	Bypass	On	312	8	Q_h on, Q_g off
25° → 30°	425	20	Bypass	On	368	20	Q_h on, Q_g off
30° → 35°	400	20	Bypass	On	335	20	Q_h on, Q_g off
35° → 40°	386	20	Bypass	On	325	16	Q_h on, Q_g off
40° → 45°	378	20	Step-up	Off	312	8	Q_h on, Q_g off
45° → 50°	360	20	Step-up	Off	368	20	Q_h on, Q_g off
50° → 55°	348	20	Step-up	Off	340	20	Q_h on, Q_g off
55° → 60°	330	20	Step-up	Off	330	16	Q_h on, Q_g off
60° → 65°	320	20	Step-up	Off	320	16	Q_h on, Q_g off
65° → 70°	318	10	Step-up	Off	318	12	Q_h on, Q_g off
70° → 75°	316	10	Step-up	Off	316	12	Q_h on, Q_g off
75° → 80°	314	10	Step-up	Off	314	8	Q_h on, Q_g off
80° → 85°	312	5	Step-up	Off	312	8	Q_h on, Q_g off
85° → 90°	311	5	Step-up	Off	311	5	Q_h on, Q_g off
90° → 180°	Same as 90° → 0°						Q_h on, Q_g off
180° → 270°	Same as 0° → 90°						Q_h off, Q_g on
270° → 360°	Same as 90° → 0°						Q_h off, Q_g on

all switches in the system. It controls the output power, and modulates the output current to be sinusoidal in phase with the line voltage. The look-up table for the state machine over a quarter line cycle at full power operation is shown in Table 2.4. This pattern is repeated in the remaining portions of the line cycle. Considering an inverter phase-shift range of up to 20 degrees (each half-bridge goes positive or negative 10 degrees from center), it is experimentally verified that the MEB helps to compress the frequency control range of the dc-ac converter block from 310-500 kHz to 310-368 kHz when $V_{IN} = 30$ V and $P_{OUT(avg)} = 70$ W (see Fig. 2-15).

Extended details about the implementation of the MEB micro-inverter, including the schematics, the PCB layouts, and the bill-of-materials are provided in Appendix A.

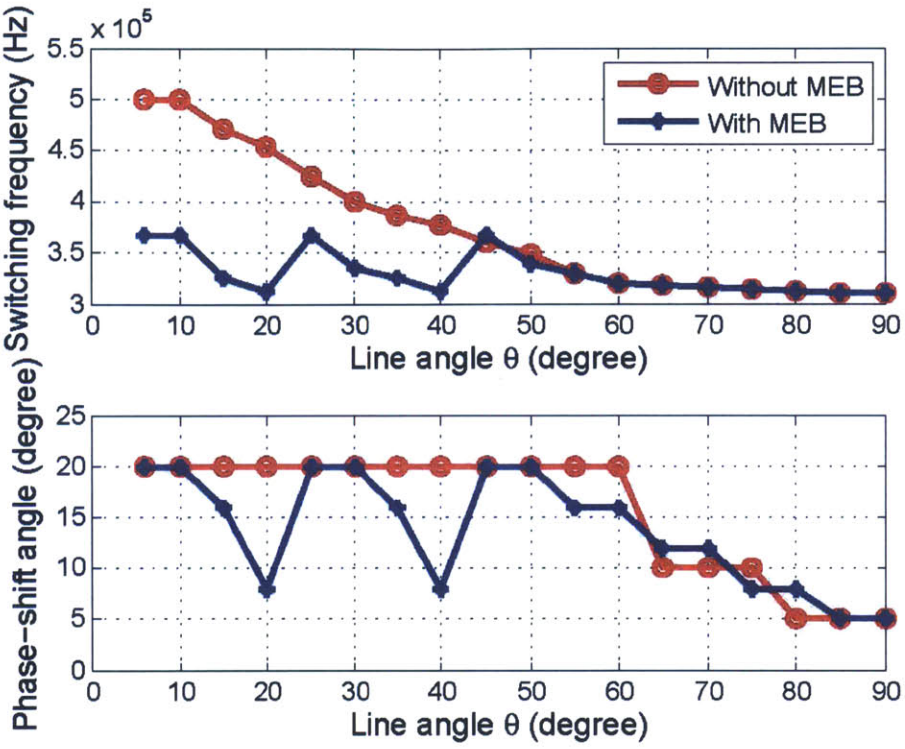


Figure 2-15: Frequency and phase modulation range of the micro-inverter without and with the MEB. Range plotted for $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W.

2.6 Experimental Results

The prototype MEB micro-inverter described in the previous section has been tested in both islanded and grid-connected mode. Figure 2-16 shows the waveforms of the MEB micro-inverter when it is delivering full power (line cycle average output power, $P_{\mathrm{OUT(avg)}}$, of 70 W) from a 27 V dc input into a 230 V_{rms} (60 Hz) ac mains. The output current, i_{GRID}, has a sinusoidal shape and is in phase with the line voltage. EMI filter is not included. A small EMI filter can further null the switching noise. The input voltage of the dc-ac converter stage, v_{X}, is also shown in Fig. 2-16. As expected it follows a staircase pattern, synchronized with the line voltage, similar to the idealized waveform of Fig. 2-4b. However, unlike in the idealized waveform there is an expected droop of about 4 V in v_{X} during the Step-up mode as the finite sized buffer capacitor, C_{BUF}, is being discharged. To maintain high efficiency, all the switches in the full-bridge inverter of the dc-ac converter stage are soft-switched by operating the inverter at switching frequencies above resonance.

Table 2.5: Prototype Specifications

Input voltage range	27 V to 38 V dc
Output voltage	230 V rms ac
Line cycle average power	70 W (peak power: 140 W)

Figure 3.5.3 illustrates the soft-switching of switch S_1, when the MEB micro-inverter has an input voltage of 27 V and an average output power of 48 W while switching at 312 kHz. In Fig. 3.5.3 the inverter output current, i_P, is negative when S_1 turns on, ensuring that the current is flowing through its anti-parallel diode and holding its voltage near zero volts during switch turn-on.

The expected advantages of the MEB micro-inverter compared to the one without the MEB are in terms of efficiency and the total size of the twice-line-frequency buffering capacitors. To confirm these advantages, the performance of the prototype MEB micro-inverter is compared with the performance of the prototype micro-inverter without the MEB. Both micro-inverters have been designed for the same specifications as shown in Table 2.5. The maximum line cycle average power delivery capability of the two prototypes has been confirmed by running them into the ac mains, and their instantaneous peak power capability has been confirmed by operating them in islanded mode into a resistive load. Figure 2-18 shows the measured waveforms for the two prototype micro-inverters while delivering power into the 230 V_{rms} (60 Hz) mains. Note the difference in the waveform of the input voltage of the dc-ac converter stage, v_X, for the two prototypes. This voltage (v_X) is modulated into staircase pattern in the micro-inverter with the MEB (Fig. 2-18a), but is constant in the micro-inverter without the MEB (Fig. 2-18b).

Since the MEB stage is isolated from the line by the dc-ac converter stage, the MEB stage has no impacts on the power factor and THD. The prototype maintains the power factor between 98% and 99.5%, and THD between 15% and 23% in repeating measurements.

System startup waveforms of the MEB micro-inverter are shown in Fig. 2-19a. It takes about 400 ms to charge up C_{IN} and C_{BUF}. Figure 2-19b shows the converter waveforms as the load steps from 25 W to 35 W. The ripple in v_X is slightly larger after the load step because C_{BUF} is being discharged by a larger output current. Both the startup and the load-step-up were commanded near a zero-crossing of the line voltage to minimize the transient impacts.

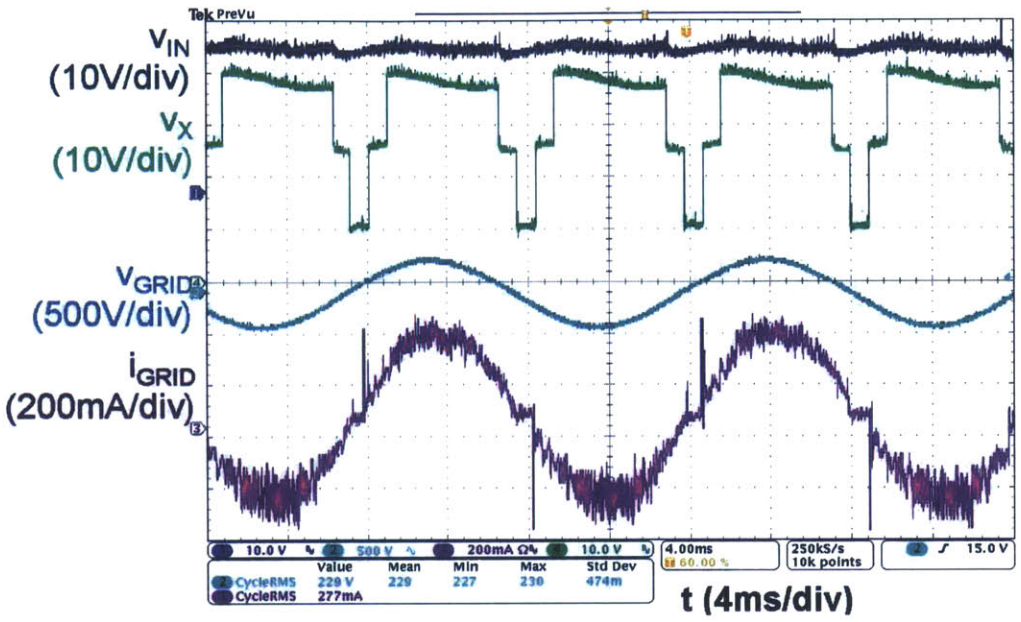


Figure 2-16: Waveforms of the MEB micro-inverter, when $V_{\text{IN}} = 27$ V, $V_{\text{GRID}} = 230\text{V}_{\text{rms}}$ and $P_{\text{OUT(avg)}} = 70$ W. The power factor in this measurement is 98.2% and the THD is 23% (without the EMI filter).

2.6.1 Efficiency Comparison

The line cycle average efficiency of the two prototypes is measured across a range of line cycle average power levels with the micro-inverters tied to the grid. The measured efficiency for the micro-inverter with and without the MEB is plotted in Fig. 2-20 for two different input voltages levels: 30 V and 33 V. At both input voltages, the micro-inverter with the MEB has a higher efficiency across the measured power range of 15 W to 70 W. Although the MEB introduces small additional losses, it significantly reduces the losses in the dc-ac converter stage by compressing its operating range. Thus, in turn, results in an overall higher system efficiency. The MEB is more effective at improving converter efficiency in the low power range, when the switching frequency without the MEB is very high. It is less effective in improving efficiency at the high power range since both micro-inverters are already operating close to the resonant frequency. For both micro-inverters, a higher input voltage results in lower efficiency. This is because a higher input voltage requires a larger voltage to be dropped across the resonant tank of the inverter, meaning that the inverter must be operated at a higher switching frequency and leading to higher losses.

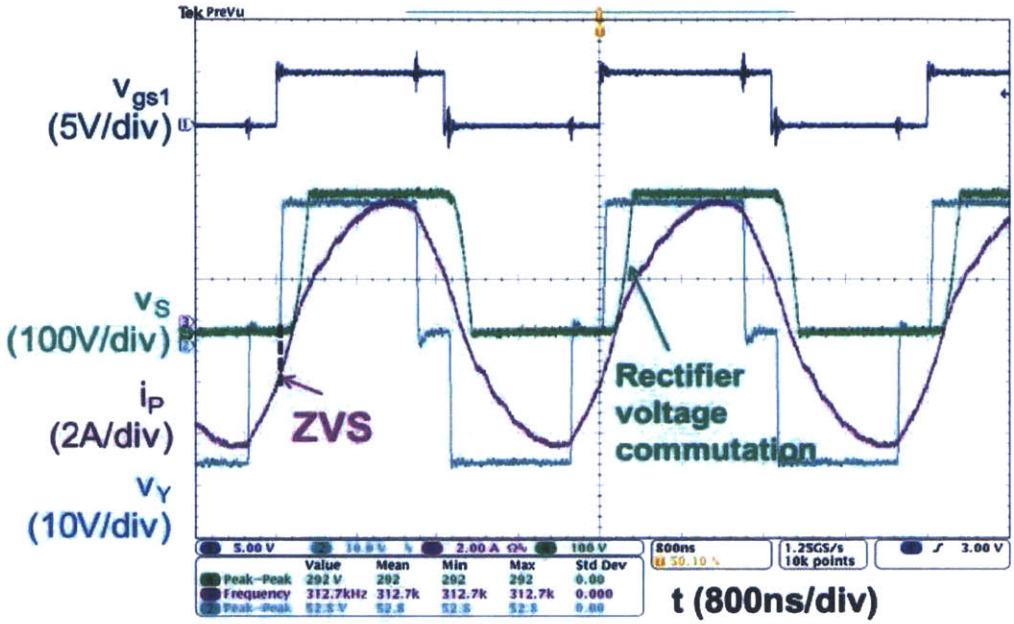
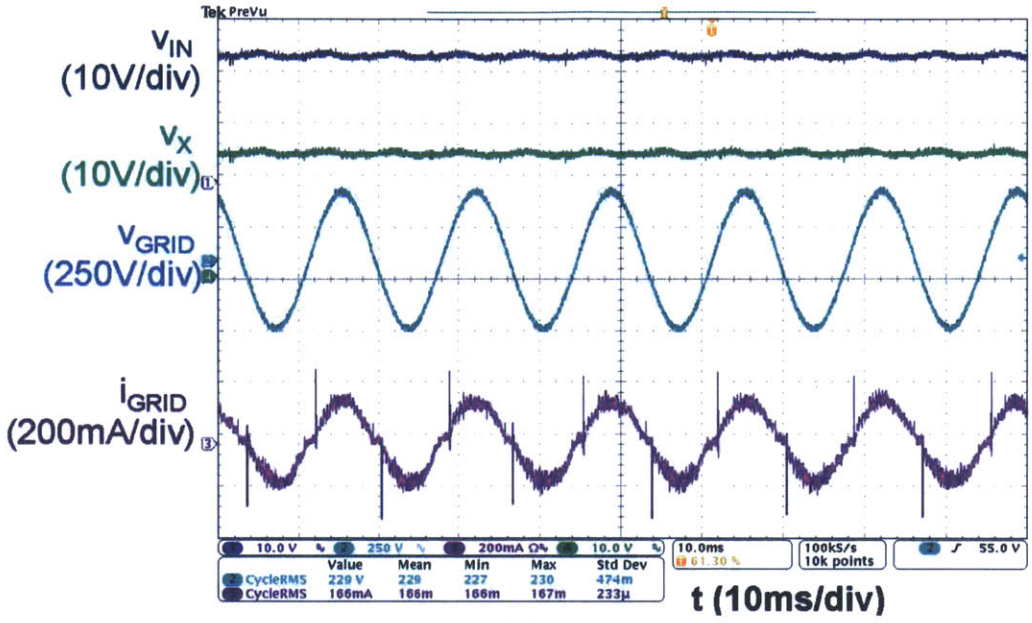


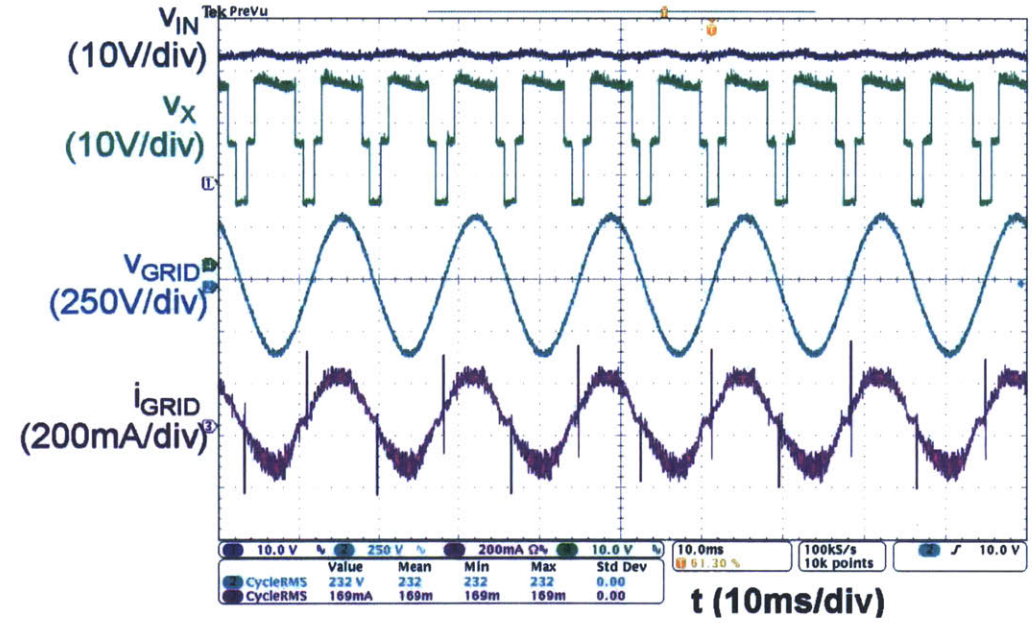
Figure 2-17: Waveforms of the MEB micro-inverter showing soft-switching of the full bridge when the switching frequency is 312 kHz, $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$ and $P_{\mathrm{OUT(avg)}} = 48$ W. v_{gs1} is the gate signal of $\mathrm{S_1}$; v_{S} is the voltage at the switching node of the rectifier; i_{P} is the inverter resonant current; and v_{Y} is the voltage generated by the full bridge.

The efficiency of a micro-inverter system can be evaluated either by the California Energy Commission (CEC) efficiency weighting (Table 2.6), or by the European Efficiency weighting (Table 2.7). The CEC efficiency places more weight on high power operation, and the European Efficiency places more weight on low power operation. The measured CEC efficiency of the micro-inverter increased from 91.1% to 92.4% by adding the MEB stage, and the measured European Efficiency increased from 85.7% to 89.4% by adding the MEB stage. Table 2.8 summarizes the measured efficiency of the two prototype micro-inverters, together with the average power factors and THDs when doing these measurements (power factor $> 98\%$ and $15\% <$ THD $< 23\%$). The efficiency of the two micro-inverters can be further enhanced by using a synchronous cycloconverter (e.g. [44, 45]) instead of the diode-based rectifier/unfolder utilized here.

To better understand the tradeoffs of adding a MEB stage to the micro-inverter, a loss breakdown analysis of the micro-inverter with and without the MEB is necessary. To investigate the loss breakdown percentage, the efficiencies of each function block (MEB, dc-ac converter) are separately measured. To measure the efficiency of the MEB, switch

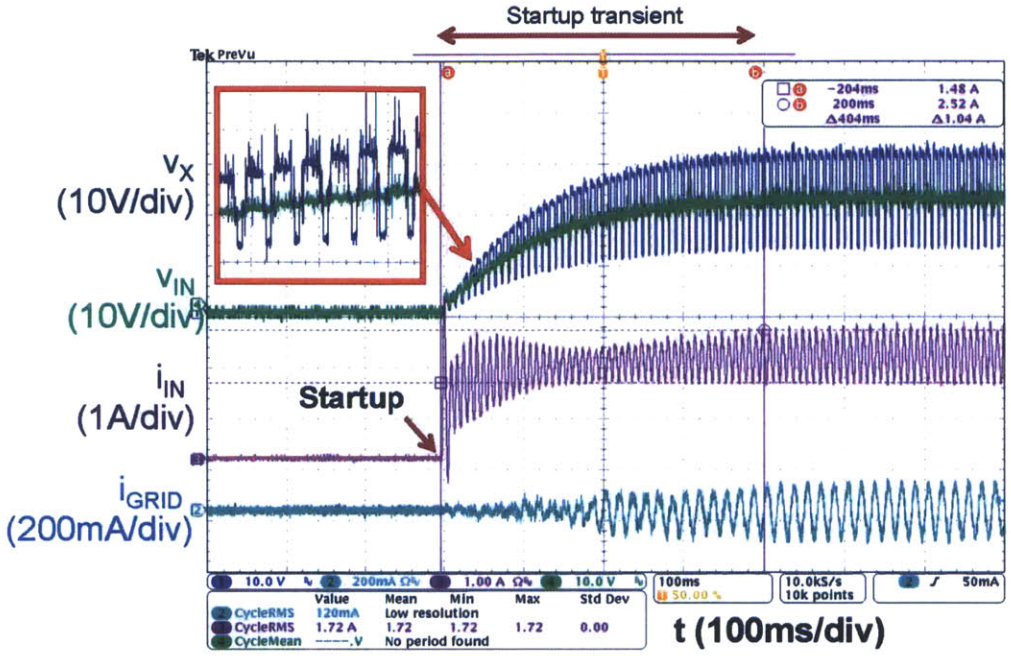


(a)

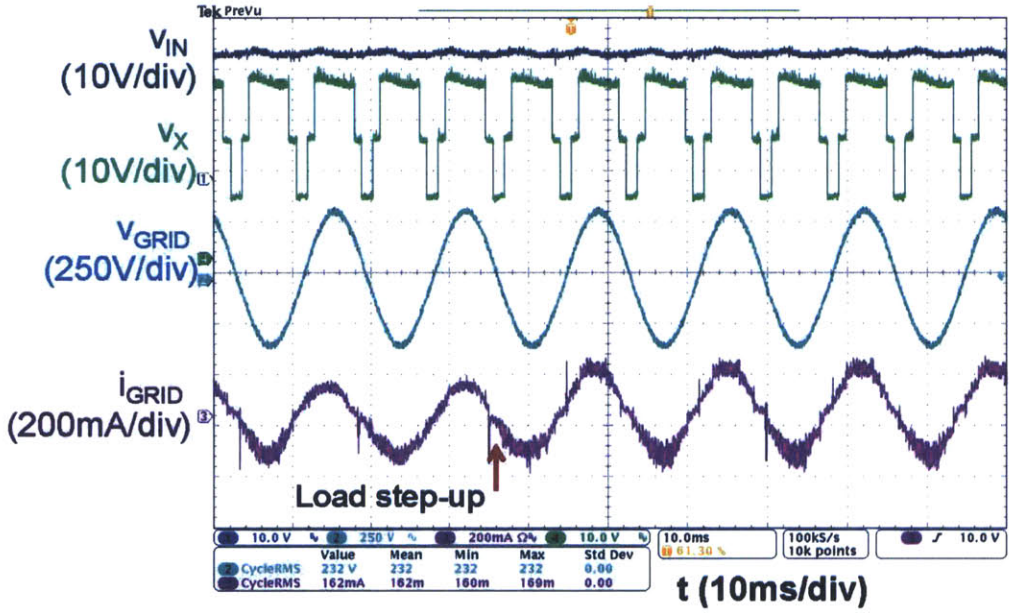


(b)

Figure 2-18: Waveforms of the micro-inverter (a) without the MEB (power factor of 99.1% and THD of 19%), and (b) with the MEB (power factor of 98.4% and THD of 23%) without EMI filters. Both figures are measured under the same set-up: $V_{\mathrm{IN}} = 27$ V, $V_{\mathrm{GRID}} = 230$ $\mathrm{V_{rms}}$, $P_{\mathrm{OUT(avg)}} = 38.4$ W. Note: the power factors and THDs provided here are calculated from the example measurements shown in the figure. The power factors of two prototype are both maintained between 98% and 99.5%, and the THDs are both maintained between 15% and 23% in all measurements.



(a)



(b)

Figure 2-19: (a) System start-up waveforms of the MEB micro-inverter when $V_{\text{IN}} = 27$ V, $V_{\text{GRID}} = 230$ V_{rms}, and $P_{\text{OUT(avg)}} = 38.4$ W; (b) Load step-up waveforms of the MEB micro-inverter when $V_{\text{IN}} = 27$ V, $V_{\text{GRID}} = 230$ V_{rms}, and $P_{\text{OUT(avg)}}$ steps from 25 W to 35 W.

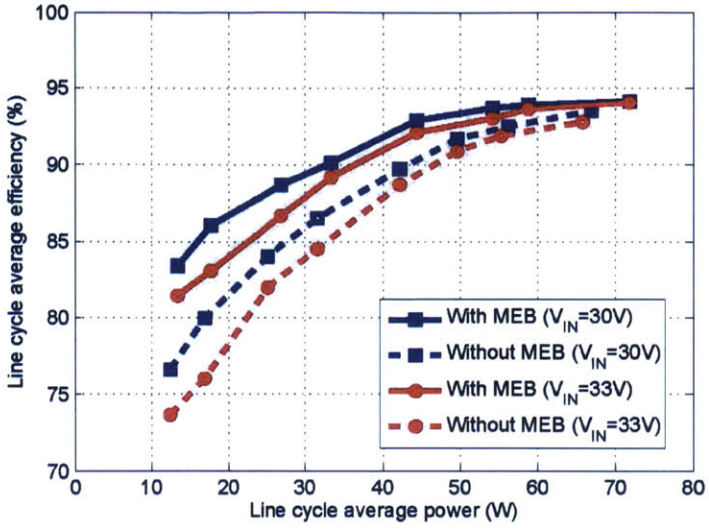


Figure 2-20: Line cycle average efficiency of the micro-inverter with and without the MEB, with $V_{\text{GRID}} = 230$ V_{rms}, and $V_{\text{IN}} = 30$ V or 33 V. The efficiency when $V_{\text{IN}} = 33V$ is lower because more voltage is dropped on the resonant tank, yield higher circuilating current loss.

Table 2.6: CEC Efficiency weighting [58].

Output Power	**100%**	**75%**	**50%**	**30%**	**20%**	**10%**
Weight	0.05	0.53	0.21	0.12	0.05	0.04

Table 2.7: European Efficiency weighting [59].

Output Power	**100%**	**50%**	**30%**	**20%**	**10%**	**5%**
Weight	0.20	0.48	0.10	0.13	0.06	0.03

S_a is kept on, while switches S_b, S_c and S_d are kept off. A variable resistive load is placed across the buffer capacitor, C_{BUF}, to vary the power drawn by the CCC from close to 0 W to 60 W. The efficiency of the dc-ac converter block is measured under conditions mimicking its operation without and with the MEB. First its efficiency is measured with a fixed input voltage, V_{IN}, of 30 V and with frequency control similar to that used in the micro-inverter without the MEB, as given by (2.3). Next its efficiency is measured with a multilevel input voltage (mimicking the output of the MEB) created by externally adjusting the voltage of a dc voltage source. When doing these measurements, the input current flows through S_a and S_c to imitate the conduction loss of the SCEB. The output power is controlled using

Table 2.8: Efficiencies, power factors and THDs of the micro-converter with and without the MEB for different output powers (Average of five measurements). Note: V_{in} = 30 V. The micro-inverter has no line-frequency EMI filter.

	Efficiency		**Power Factor**		**THD**	
	Without MEB	**With MEB**	**Without MEB**	**With MEB**	**Without MEB**	**With MEB**
20% output power (14W)	79.2%	85.3%	98.1%	98.2%	21%	19%
40% output power (28W)	84.9%	88.2%	98.6%	98.4%	17%	15%
60% output power (42W)	89.3%	92.1%	98.4%	99.1%	19%	23%
80% output power (56W)	93.1%	94.1%	98.8%	98.9%	18%	20%
100% output power (70W)	93.9%	94.2%	99.1%	99.2%	17%	15%
CEC efficiency	91.1%	92.4%	-	-	-	-
European efficiency	85.7%	89.4%	-	-	-	-

frequency control similar to that used in the micro-inverter with the MEB, as given by (2.4). In both cases the efficiency of the dc-ac converter block is measured across its full instantaneous power range (0 V to 140 W). The results of these efficiency measurements are shown in Fig. 2-21. These results are used to identify the power losses in each of the micro-inverter function blocks.

The results of a loss breakdown analysis for the micro-inverter with and without the MEB are shown in Fig. 2-22. This loss breakdown analysis is done for an input voltage of 30 V and average output power in the range of 10 W to 70 W. The MEB stage introduces additional loss, but significantly improves the efficiency of the dc-ac converter block. The increased input voltage reduces the inverter current, thus reduces the conduction loss in the switches, the resonant tank and the primary side winding of the transformer. The compressed frequency range not only reduces the magnetic core losses, but also limits the ac resistance of the winding and reduces its conduction losses. For example, when $P_{OUT(avg)}$ = 70 W, the conduction loss in the dc-ac converter is reduced by 0.4 W, the inductor core loss is reduced by 0.6 W, and the transformer core loss is reduced by 0.4 W. Hence, even with the additional 1 W loss in the MEB stage, the system with the MEB has about 0.4 W less loss than the system without the MEB.

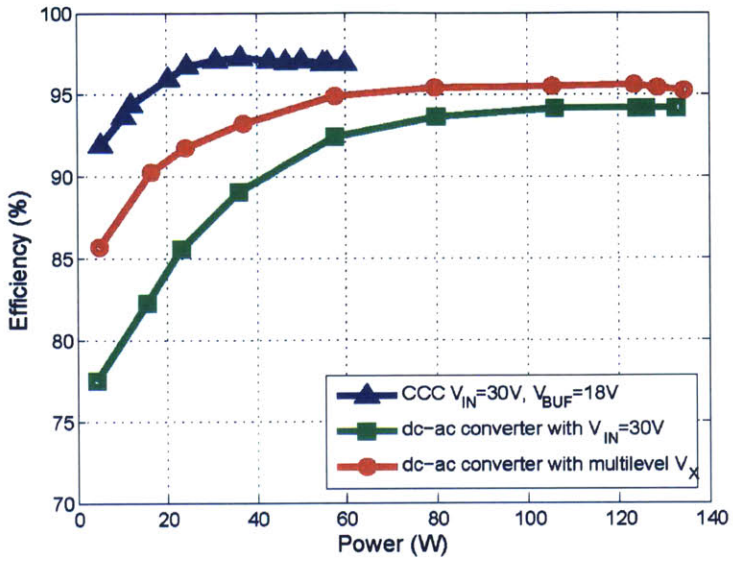


Figure 2-21: Measured efficiency of the CCC, the dc-ac converter block with a fixed input voltage, and the dc-ac converter block with a multilevel input voltage when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}} = 70$ W. The peak power rating of the dc-ac converter block is 140 W, and the peak power rating of the CCC is 68 W.

2.6.2 Capacitor Size Comparison

In the MEB micro-inverter the twice-line-frequency energy buffering is provided by both $\mathrm{C_{IN}}$ and $\mathrm{C_{BUF}}$. Since there is no strict voltage ripple constraint for $\mathrm{C_{BUF}}$, moving some buffering capacitance from $\mathrm{C_{IN}}$ to $\mathrm{C_{BUF}}$ reduces the total size of the capacitors. Selecting the relative sizes of $\mathrm{C_{IN}}$ and $\mathrm{C_{BUF}}$ requires a trade-off. Buffering more energy in $\mathrm{C_{BUF}}$ reduces the total capacitor size, but introduces more ripple in the dc-ac converter block's input voltage, v_{X}. A larger variation in v_{X} complicates the control of the dc-ac converter block and increases the peak voltage stress on the full-bridge switches. The potential for capacitor size reduction also depends on the allowed voltage ripple across the PV panel. As the voltage ripple allowance at the output of the solar panel becomes smaller, the amount of total capacitor size reduction possible with the MEB becomes larger.

In the prototype MEB micro-inverter, three 1 mF, 50 V capacitors (Panasonic ECA-1HM102) serve as $\mathrm{C_{IN}}$, while one 5.6 mF, 25 V capacitor (Panasonic EEU-HD1E562) serves as the $\mathrm{C_{BUF}}$. The total volume of these capacitors is 15.6 $\mathrm{cm^3}$. It is experimentally verified that with an input voltage of 27 V and an average output power of 70 W (worst case), the MEB micro-inverter has a 7% peak-to-peak voltage ripple across $\mathrm{C_{IN}}$ (and a 4 V peak-to-

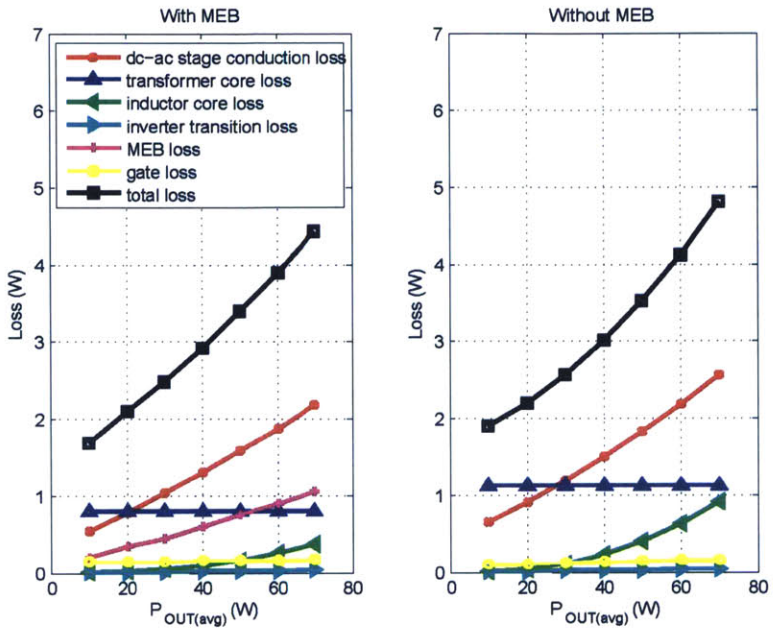


Figure 2-22: Loss break-down comparison between the micro-inverter with and without the MEB, when $V_{\mathrm{IN}} = 30$ V and $P_{\mathrm{OUT(avg)}}$ sweep between 10 W and 70 W.

peak voltage ripple across C_{BUF}). To achieve the same voltage ripple across C_{IN} without the MEB, five 1 mF, 50 V capacitors (Panasonic ECA-1HM102) must serve as C_{IN}. The total volume of these capacitors is 17 cm^3, which is 9% larger than the total capacitor volume in the MEB micro-inverter. This volume reduction creates spaces for the additional semiconductor devices in the MEB stage. The volume of the MEB stage can be further reduced if a narrower ripple is allowed at the micro-inverter input and/or a larger ripple on C_{BUF} can be managed.

2.7 Comparisons and Discussions

Table IX compares the figure-of-merit (FOM) of some recently proposed multiple-stage micro-inverter topologies with the micro-inverters (with and without the MEB, Fig. 2-11) prototyped in this work. Compared to [51, 59, 60], the prototyped MEB micro-inverter achieves higher efficiency and eliminates the need for a bulky line frequency filter. Compared to the topology proposed in [44], the prototyped micro-inverters have similar high-frequency-link dc-ac stage. As a benefit of the MEB stage, the high-frequency-link dc-ac stage in the MEB micro-inverter achieves higher efficiency at a higher switching frequency. The overall

system efficiencies are comparable, but the MEB micro-inverter is switching at a higher frequency, resulting in higher power density. It also reduces the twice-line-frequency energy buffering capacitance. Compared to [61], the prototyped MEB micro-inverter achieves comparable CEC efficiency at a lower power rating, and eliminates the need for a bulky line frequency filter. Compared to the prototyped micro-inverter without the MEB, the MEB micro-inverter achieves higher CEC and European efficiencies without increasing the system size. The additional switches in the MEB have low power ratings, small foot prints, and are easy to drive and control. These advantages will be further enhanced by the continued evolution of semiconductor technologies.

The MEB architecture represents a new concept which integrates low frequency switched capacitor circuits with high-frequency-link dc-ac converters. It inherits the advantages of switched capacitor circuits in handling wide voltage conversion range, and the advantages of high-frequency-link dc-ac converters in achieving high power density and high efficiency for grid interfacing (without line frequency filtering).

2.8 Summary of Chapter 2

This chapter explores a merged multi-stage architecture in dc-ac applications. A multilevel energy buffer and voltage modulator, consisting a switched-capacitor circuit and a switched-inductor circuit, is proposed as an additional stage for grid-interface micro-inverters. The MEB significantly reduces the voltage conversion range that the high-frequency dc-ac converter portion of the micro-inverter must operate over by stepping its input voltage in pace with the line voltage. This enables the dc-ac converter stage to operate in a narrower operating range and achieve higher efficiency. The MEB also functions as an active energy buffer, which helps to reduce the total size of the twice-line-frequency energy buffering capacitance, creating space for the additional components in the MEB stage. A prototype 70 W MEB micro-inverter, designed for 27 V to 38 V dc input and 230 V rms ac output, has been built, and used to validate the principles and performance advantages of the MEB micro-inverter. The MEB stage improves the efficiency of the micro-inverter by 3.7% (EU efficiency), while maintaining same volume, power factor and THD performances. The proposed micro-inverter architecture with a MEB stage can be applied more broadly to converters interfacing between dc voltage and the single-phase ac grid.

Table 2.9: FOM of many recently published micro-inverters and the MEB micro-inverter architecture.

	[51]	[60]	[59]	[44]	[61]	**Prototype without MEB**	**Prototype with MEB**
Topology	dc-dc-ac	dc-dc-ac	dc-ac-dc-ac	dc-ac-ac	dc-dc-ac-dc-ac	dc-ac-ac	dc-multilevel dc-ac-ac
Year	2006	2007	2008	2010	2013	2013	2013
Peak Power	100W	500W	150W	100W	250W	70W	70W
Grid Voltage rms ac	120V	100V	250V	240V	110V/220V	230V	230V
Input Voltage	35V	30V	36V	25V-40V	22V-40V	27V-38V	27V-38V
Switching Frequency	50kHz	20kHz	200kHz	45kHz-350kHz	-	310kHz-500kHz	310kHz-368kHz
PK: peak efficiency, EU: European efficiency, CEC: CEC effciency	70%PK	85%CEC	87%PK 85%EU	96%PK	93%CEC 94%PK	91%CEC 94%PK 85.7%EU	92%CEC 94%PK 89.4%EU
Power Factor	-	99%	-	-	-	99%	99%
THD	5% with line frequency filter	4.2% with line frequency filter	1.50% with line frequency filter	-	-	15%-25% without line frequency filter	15%-25% without line frequency filter
Num. of switches and diodes (FR: fully rated, PR: partially rated)	4 FR switches, 3 FR diodes	4 FR switches, 4 FR diodes	9 FR switches, 9 FR diodes	8 FR switches	7 FR switches, 3 FR diodes	6 FR switches, 4 FR diodes	6 FR switches, 4 FR diodes, 6 PR switches
Reduced twice-line-frequency energy buffer	Yes	Yes	Yes	No	Yes	No	Yes
Grid Interfacing	Line frequency unfolder and filter	Line frequency unfolder and filter	Line frequency unfolder and filter	High frequency cycloconverter	Line frequency unfolder and filter	High frequency cycloconverter	High frequency cycloconverter

Chapter 3

Merged Multi-Stage Power Conversion in a Dc-Dc Converter

Abstract

This chapter studies the hybrid switched-capacitor/magnetics merged multi-stage power conversion through the design and implementation of a high-power-density wide-input-voltage-range isolated dc-dc converter. A *MultiTrack* power conversion architecture that splits charge into multiple voltage domains and delivers power through multiple tracks is proposed. The MultiTrack architecture reduces the voltage ratings on devices, reduces the voltage regulation stress of the system, improves the component utilization, and reduces the sizes of passive components. The architecture also leverages the complementary strengths of switched-inductor, switched capacitor, and magnetic isolation circuits, and gains mutual benefits from the way they are merged together. This architecture is suitable to applications which require both isolation and wide-voltage-conversion range. Compared to a conventional two-stage design, its regulation stage and isolation stage are merged, leading to a *hybrid-switched-capacitor/magnetics* structure that reduces the energy that is "reprocessed" by the two-stages.

An 18 V – 80 V input, 5 V output, 15 A, 800 kHz, 0.93 inch^2 (1/16 brick equivalent) isolated dc-dc converter has been built and tested to verify the effectiveness of this architecture. It has a power density of 453 W/inch^3 (at 75 W peak power, 200 LFM air flow, 25 °C ambient temperature, peak device temperature 115 °C) and a peak efficiency of 91.3%. This yields a power density that is approximately a factor of three higher than the best commercial designs having equivalent performance specifications.

This chapter demonstrates that by splitting a centralized power conversion block into multiple distributed (but coupled) power conversion block, the overall system power density can be significantly improved while maintaining state-of-art system performance.

3.1 Design of Wide-Input-Voltage-Range Isolated Dc-Dc Converters

In this chapter, we presents a *MultiTrack* power conversion architecture that has a *hybrid switched-capacitor-magnetic* structure that splits the wide voltage conversion range into multiple regions, delivers power in multiple tracks, and functionally merges the regulation stage and the isolation stage. The system operates in multiple operation modes across the wide input voltage range, with its performance optimized for each sub-section of the input voltage range. Compared to conventional two-stage designs, it provides advantages in terms of reduced switch voltage ratings, reduced magnetics size (especially inductor size), improved component utilization, and reduced drive of parasitic transformer capacitances. To demonstrate the effectiveness of the MultiTrack architecture, a 18 V – 80 V input, 5 V output, 75 W, 800 kHz, 0.93 inch^2 (1/16 brick equivalent) dc-dc converter has been built, optimized, and tested to verify the effectiveness of this architecture.

The challenges of wide-input-voltage-range design come from the imbalanced utilization of the voltage and current ratings of devices. Both the voltage rating and the current rating of the devices have to be able to meet the worst case, i.e. the peak operation current and the peak operation voltage. If the input voltage can change across a wide range, the current ratings of many devices are determined by the current that they carry when the input voltage is the lowest, and the voltage ratings of many devices are determined by the voltages that they block when the input voltage is the highest. The switch stress factor ($V_{\mathrm{sw,pk}} I_{\mathrm{sw,pk}} / P_{\mathrm{out}}$) is sometimes used as a dimensionless performance factor that reflects the switch ratings [62]; requiring both high voltage/low-current ranges and low-voltage/high-current ranges increases switch stress factor. Similarly, reduced range of conversion ratios reduces the required energy storage of the passive components for a given worst-case ripple [62–64]. More design considerations regarding peak device stress are listed in Table 3.1.

Fig. 3-1 illustrates this relationship. In conventional wide-input-voltage-range designs (Fig. 3-1a), there exists a big gap between the voltage-current region that the converter actually operates in, and the voltage and current combinations that the devices are rated for. This gap indicates opportunities in improving the device utilization in conventional designs. Exploring merged multi-stage power conversion architectures that can better utilize the device ratings and reduce the gap (Fig. 3-1b), is a major target of this chapter.

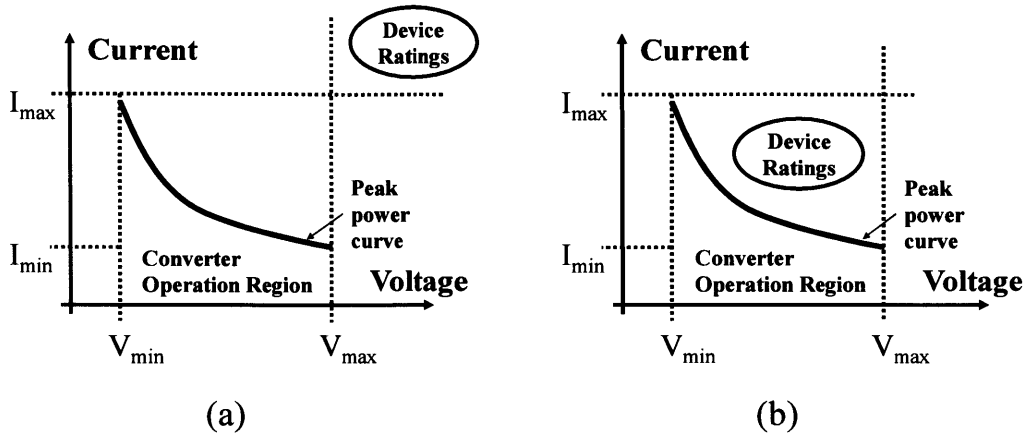


Figure 3-1: The converter operation region and device rating region in (a) conventional wide-input-voltage-range power conversion architecture, (b) merged multi-stage power conversion architecture.

Table 3.1: Challenges on device ratings in wide-input-voltage-range designs.

Operating Condition	Inductors	Capacitors	Switches
High Voltage, Low Current	High Inductance	High Voltage Rating	High Voltage Rating
Low Voltage, High Current	High Current Rating	High Capacitance	High Current Rating

The remainder of this chapter is organized as follows: Section 3.2 provides an overview of the MultiTrack power conversion architecture. A basic 2-Track implementation and its operation is introduced in Section 3.3. The 2-Track architecture is extended to a generalized MultiTrack architecture in Section 3.4. Theoretical analysis about the advantages of the MultiTrack architecture are provided in Section 3.5. Section 3.6 presents several practical design considerations. Experimental and benchmark results are provided in Section 3.7, and Section 3.8 concludes this chapter. Extended theoretical discussions and experimental details are provided in Appendix B.

3.2 Architecture Overview

Fig. 3-2 shows the block diagram of the proposed MultiTrack power conversion architecture. It comprises a switched-inductor circuit, a switched-capacitor circuit, and a magnetic isolation circuit. The switched-inductor circuit is principally responsible for voltage regulation; the magnetic isolation circuit offers isolation and voltage scaling (and - in some cases - a sec-

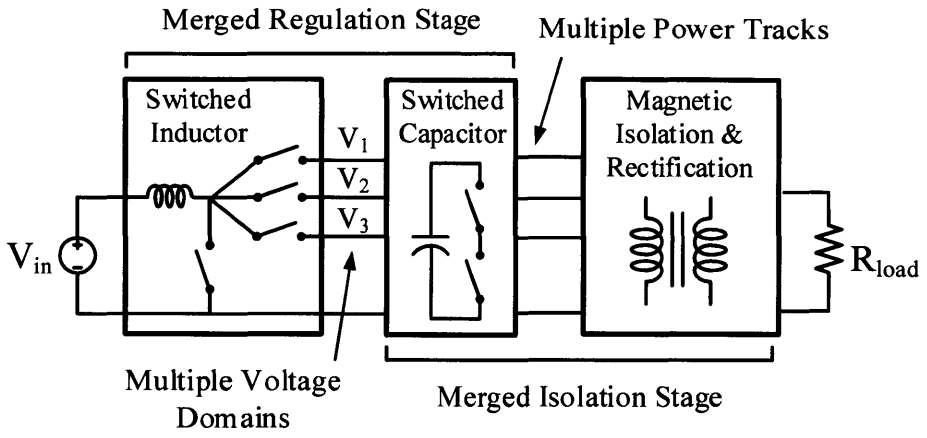


Figure 3-2: The proposed MultiTrack power conversion architecture comprising multiple voltage domains and multiple power tracks. Its regulation and isolation stage are merged with reduced amount of power that is "re-porcessed" by the two-stages.

ondary means of voltage regulation); the switched-capacitor circuit creates multiple related voltage levels (V_1, V_2, V_3, etc.) and ac power tracks that bridge the other two sub-circuits. Components of these sub-circuits are reused, and their functions are partially merged. The switched-inductor circuit couples into the multiple levels of the switched-capacitor circuit as a *merged regulation stage* that provides voltage regulation; likewise, as will be shown, by reusing the switches of the switched-capacitor circuits as inverters that drive the isolation transformer, the switched-capacitor circuit is also merged into the magnetic isolation circuit formulating a *merged isolation stage.*

In conventional wide-input-voltage range designs, there is often a regulation stage (typically a buck, or boost, or buck-boost) that compresses the variable input voltage to a fixed intermediate bus voltage. This intermediate bus voltage is then processed by a separate isolation stage. Since the regulation stage has to be designed for the worst case (blocking peak voltage and carrying peak current), high-stress semiconductor devices and passive components are typically required. These components are not well utilized because high voltage stress and current stress are each imposed on this stage by different portions of the wide operating range. This represents a critical factor in the design of converters for wide voltage range operation.

In the MultiTrack architecture, there exists multiple voltage domains with ratiometrically-related intermediate bus voltages (V_1, V_2, V_3, etc.). Depending on the input voltage level,

the switched inductor circuit redistributes the energy drawn from the input into the closest intermediate bus voltages, thus effectively reducing the voltage conversion range of the regulation stage, and the imposed energy storage requirements of the passive components. The power is then delivered through multiple power tracks located in different voltage domains. As will be shown in detail below, the power delivered by these multiple tracks are naturally balanced by the switched capacitor circuit, allowing balanced stress on them. By having multiple power tracks, the heat generated during power conversion is more distributed and can be better removed, yielding lower temperature rise and/or cooling requirements. By splitting into multiple voltage domains (and using intermediate voltages well), switches can have lower voltage ratings and lower on-resistance. Moreover, by splitting up the drive among several levels, the transformer used in the merged isolation stage can produce lower common-mode drive of current across the isolation barrier due to inter-winding capacitance.

3.3 A Basic 2-Track Embodiment

A 2-to-1 input voltage range 2-track converter as shown in Fig. 3-3 is a simple implementation of the MultiTrack architecture. This 2-track converter has two related intermediate bus voltages (V_X and $2V_X$) and has a 2-to-1 input voltage range between V_X and $2V_X$. The relative values of bus voltages V_X and $2V_X$ are synthesized by a 2:1 ladder switched capacitor circuit. The voltages between $2V_X$ and V_X and between V_X and the reference potential are the inputs to the isolation stage.

We first introduce the isolation stage. The isolation stage includes a pair of half bridges (S_A/S_B and S_C/S_D) that operate synchronously to drive a pair of identical resonant tanks ($C_{res1}|L_{res1}$ and $C_{res2}|L_{res2}$). These are coupled to a *multiple-input-single-output* (MISO) transformer (whose leakage inductances form L_{res1}, L_{res2}), with the output tied to a synchronous full-bridge rectifier (Q_1-Q_4). The isolation stage has relatively fixed voltage conversion ratio. The system operates in a manner very similar to a conventional series-resonant converter, except that the magnetic core is driven in parallel by two identical primary windings. The transformer turns ratio is determined by the required voltage conversion ratio.

S_A-S_D are reused to create a 2:1 ladder switched-capacitor structure that can balance the two stacked intermediate bus voltages (V_X and $2V_X$) formed by the two capacitors (C_1 and C_2). Charge is transferred through an additional capacitor, C_3, which ties the two

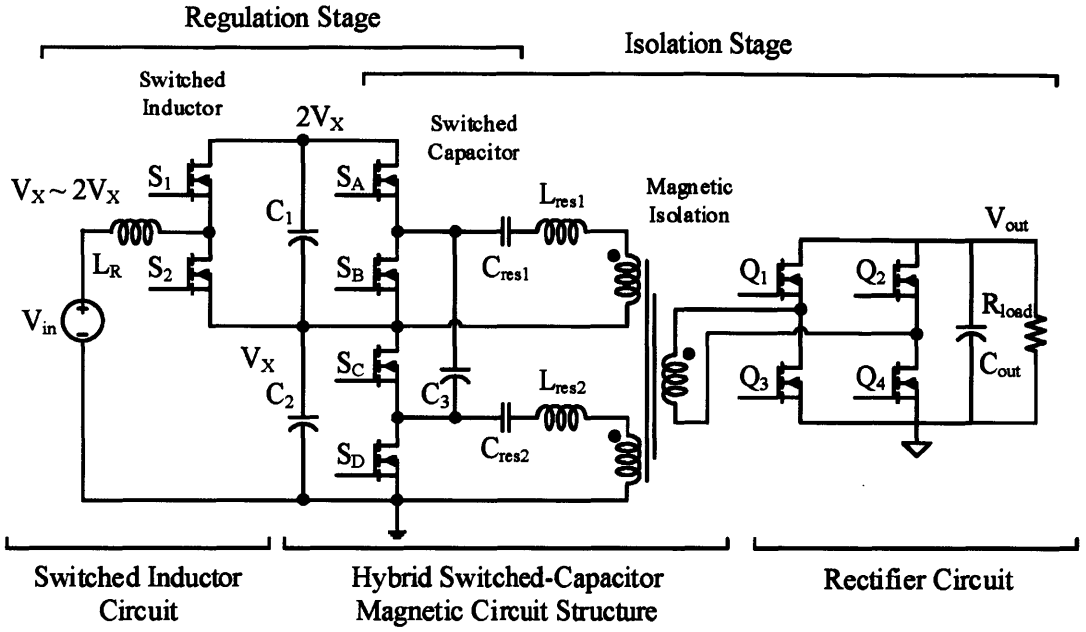


Figure 3-3: Schematic of an example 2-to-1 input voltage range 2-Track converter comprising a switched-inductor circuit, a switched-capacitor circuit and a magnetic isolation circuit. The regulation stage and the isolation stage are merged by a *hybrid switched-capacitor-magnetic* circuit structure.

switch nodes together. The switched-capacitor charge-redistribution mechanism ensures $V_{C1} \approx V_{C2}$. The combination of a switched-capacitor circuit and a multiple-winding transformer may be described as a *hybrid switched-capacitor/magnetics* circuit structure. This hybrid switched-capacitor/magnetics structure serves as a core sub-section of the Multi-Track architecture. The switched capacitor circuit naturally drives the MISO transformer, and smoothly rebalances the power processed by different tracks with low loss.

The regulation stage in this two-track converter comprises inductor L_R and switches S_1 and S_2. By controlling the duty ratio of S_1 and S_2, the voltage of C_1 is regulated, and the voltage of C_2 is effectively regulated through the ladder switched-capacitor mechanism. In this embodiment, voltage regulation and dynamic control are dominated by the modulation of S_1 and S_2. For an input voltage v_{in} between V_X and $2V_X$, S_1 and S_2 are controlled such that the voltages across C_1 and C_2 are always V_X. If the input voltage is closer to V_X, S_2 has a higher duty ratio and more charge is delivered to V_X; if the input voltage is closer to $2V_X$, S_1 has a higher duty ratio and more charge is delivered to $2V_X$. If S_1 and S_2 are switched in complimentary pulse-width-modulation (PWM) mode, the required duty ratio

of S_1 that can regulate the voltage across C_1 and C_2 to be V_X, d_1, is

$$d_1 = \frac{v_{\text{in}} - V_X}{V_X}. \tag{3.1}$$

and the duty ratio of S_2, d_2, is

$$d_2 = 1 - d_1 = 2 - \frac{v_{\text{in}}}{V_X}. \tag{3.2}$$

This is somewhat similar to regulating a boost converter, but with V_X instead of ground as the second potential. This changes the control law (in particular, V_X as a function of d_1 and v_{in}) and reduces the stresses on the devices and passive components.

The isolation stage of the MultiTrack architecture reuses the switches in the switched-capacitor circuits, and employs magnetic coupling to provide galvanic isolation and to combine the power carried by the multiple intermediate buses. In the 2-Track converter shown in Fig. 3-3, the isolation stage can be interpreted as two ac power tracks distributed in two stacked voltage domains ([0, V_X], [V_X, $2V_X$]), each processing a half of the output power. The cross-sectional area of the magnetic core is determined by the volt-seconds of the secondary winding. The window area of the magnetic core is determined by the output current. Thus, the power conversion stress of this two-track isolation stage is the same as a conventional series-resonant converter with a full power rating, indicating equivalent magnetics volume and efficiency. It is in some respects similar to a series-primary parallel-secondary configuration [65], whereas only a single magnetic core and a single rectifier is needed. This MultiTrack configuration distributes the concentrated device voltage-ratings on the high-voltage side into multiple devices, which can be beneficial. Moreover, as will be shown shortly, the current driven through the common-mode capacitances of the transformer is much smaller than that in a single-primary-winding design. This effect can be beneficial in high frequency designs. Similar to other two-stage or multi-stage designs with intermediate bus voltages, the intermediate bus voltages V_X and $2V_X$ are independent from the input voltage variation. Thus, the isolation stage can always has a fixed voltage conversion ratio, and can be optimized to achieve high efficiency and high power density.

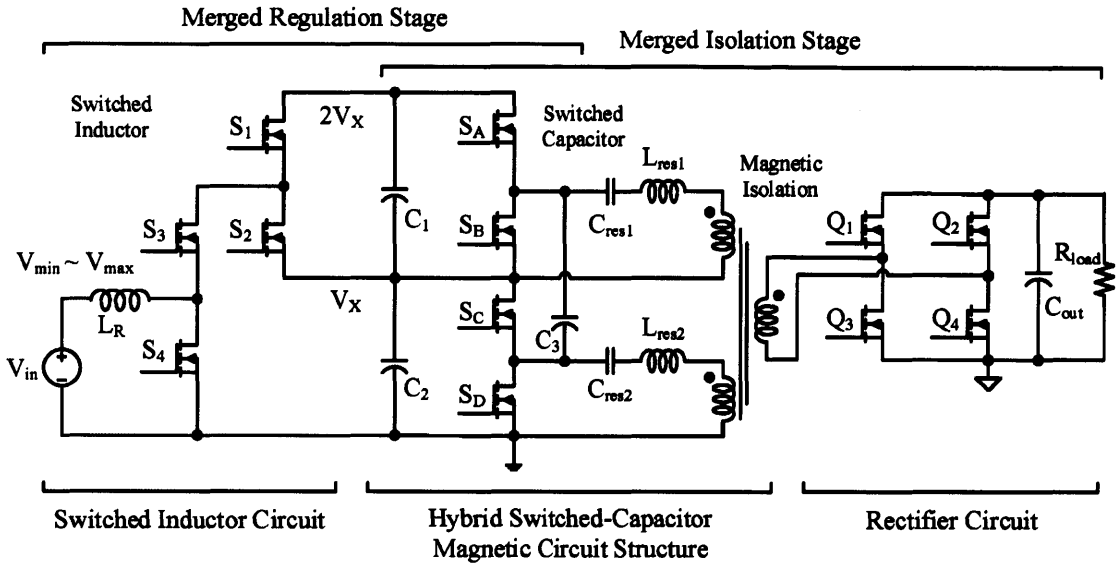


Figure 3-4: An example 2-Track power converter that can handle wide input voltage range. For this converter, the maximum input voltage, $V_{\max}$, must be smaller than $2V_X$.

3.4 MultiTrack Architecture with Wide Input Voltage Range

The basic 2-Track converter shown in Fig. 3-3 is suitable to applications with restricted 2-to-1 input voltage range ($v_{\text{in}} \in [V_X, 2V_X]$). By adding two additional switches (S_3 and S_4) in the regulation stage as shown in Fig. 3-4, the converter can handle any desired input voltage range between 0V to $2V_X$ (albeit requiring appropriate component current ratings). The voltage ratings of C_1 and C_2 are both V_X. The operation of this enhanced design can be split into two regions determined by the input voltage v_{in}. When $v_{\text{in}} \in [0, V_X]$, S_3 and S_4 are switching, S_1 is kept off, and S_2 is kept on. In this manner, the L_R, S_3 and S_4 formulates a ground referenced boost converter that feeds current into the V_X node. The switched capacitor circuit balances the voltages of C_1 and C_2. When $v_{\text{in}} \in [V_X, 2V_X]$, S_3 is kept on, S_4 is kept off, and S_1 and S_2 are switching. The L_R, S_1 and S_2 formulates boost-based converter structure that feeds power from the input into both the V_X and the $2V_X$ node. Fig. 3-5 illustrates the operation of the switches in these two operation modes.

Figure 3-5 shows the two different operating modes of the regulating (switched-inductor) portion of the circuit. Depending upon the operating mode, the switched capacitor circuit is used differently to maintain voltage balance between the two stacked cells in the 2:1

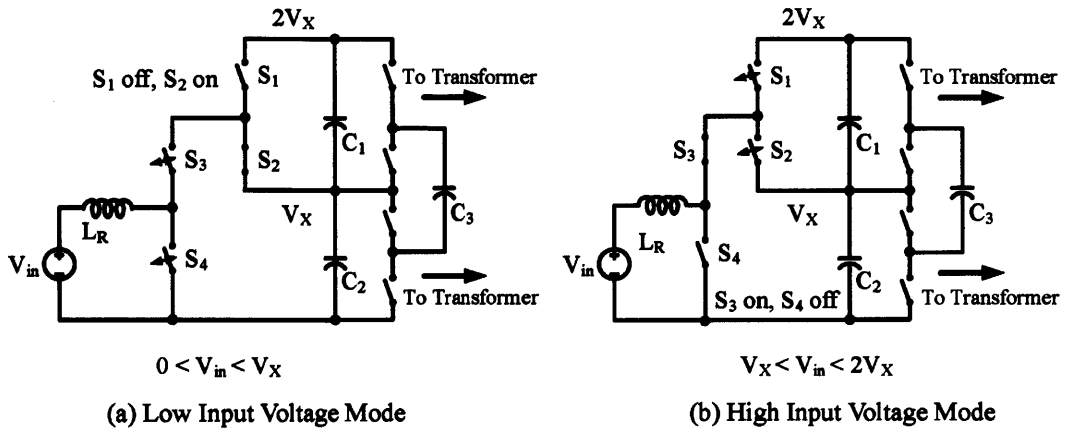


Figure 3-5: Two operation modes of the two pairs of half-bridges in the regulation stage of a 2-Track converter. When $0 < v_{\text{in}} < V_X$, S_3 and S_4 are switching, S_1 is kept off, and S_2 is kept on. When $V_X < v_{\text{in}} < 2V_X$, S_3 is kept on, S_4 is kept off, and S_1 and S_2 are switching.

ladder switched capacitor circuit. When the input voltage is high, power (from the input and inductor) is injected into both the V_X and $2V_X$ nodes, and the total voltage of the two stacked cells (voltage $2V_X$) serve to counter the input voltage (in providing volt-seconds balance on the inductor). When the input voltage is low, the input power is injected into the V_X node only. The ladder switched capacitor circuit operates to redistribute charge such that the different windings of the isolation stage magnetics can be utilized equally. Each of the transformer sections processes half of the full rated power. The PWM operation of the half-bridges (S_1-S_4) in conjunction with the switched-capacitor conversion enables voltages V_X, $2V_X$ to be regulated with low stress on the inductor and with balanced utilization of the isolation stage magnetics across the full input voltage range.

In this wide-input-voltage-range 2-Track converter, the magnitude of the voltage applied across the inductor L_R never exceeds V_X, and the charge coming from the input source is always delivered to the closest dc voltages to the input. For example, if $v_{\text{in}} \in [0, V_X]$, power coming from v_{in} is always delivered to the V_X node; if $v_{\text{in}} \in [V_X, 2V_X]$, power coming from v_{in} is always delivered to the V_X node and the $2V_X$ node. As will be analyzed, the smaller resulting voltage drop on the inductor, and compressed voltage conversion ratio can significantly reduce the inductor size and the regulation loss.

One can even use a higher-order capacitor stack to create more intermediate voltages

and power delivery tracks if a wider input voltage range is desired. The schematic of a 3-Track converter is shown in Fig. 3-6. Implementations with more tracks can be created following a similar pattern. By creating n intermediate voltages and power tracks, the power conversion stress is further distributed, the voltage across the inductor is further reduced, and the effective voltage conversion ratio is further compressed. As will be analyzed, these advantages don't scale up linearly with the number of tracks, but will gradually saturate in a manner that may be likened to the gradually saturated advantages of multi-phase interleaving techniques [10, 11, 66, 67].

Note the voltage ratings of S_4 and S_6 in the schematic shown in Fig. 3-6 are $2V_X$ and $3V_X$, respectively. If S_4 and S_6 are implemented as multiple cascaded devices as shown in Fig. 3-7, all switches on the primary side has a voltage rating of V_X. This can be further benefited by using the intermediate bus voltage(s) to provide voltage clamping for the devices (e.g. One can add a few small protection diodes (e.g. D_1-D_3) to ensure voltage sharing of the stacked low voltage rating devices.) This modification is beneficial in discrete designs as considered here, and would also be valuable in an integrated circuit (IC) implementation if the peak device voltage rating is constrained by the fabrication process.

The MISO transformer in the isolation stage has multiple primary windings and a single secondary winding. One can synthesize different resonant tanks (or non-resonant networks) and/or switch networks to implement different isolation circuits for different purposes, e.g., LLC converters [68], series-resonant converters [69], dual-active-bridge converters [70,71]. If planar transformers are utilized, a systematic magnetics modeling technique ([72,73], which will be presented as the Chapter 4 of this thesis) that can rapidly estimate the impedances and current distribution can be utilized to design these resonant tanks and transformers.

Many known rectifier structures (e.g. center-tapped rectifier, current-doubler rectifier, full bridge rectifier, switched-capacitor step-down rectifier [77], etc.) are compatible with the MultiTrack architecture.

3.5 Advantages

We quantify the advantages of the MultiTrack architecture by comparing the MultiTrack architecture with a conventional boost-type two-stage (BTS) architecture - as shown Fig. 3-8. In the BTS architecture, the input voltage is firstly boosted to an relatively fixed interme-

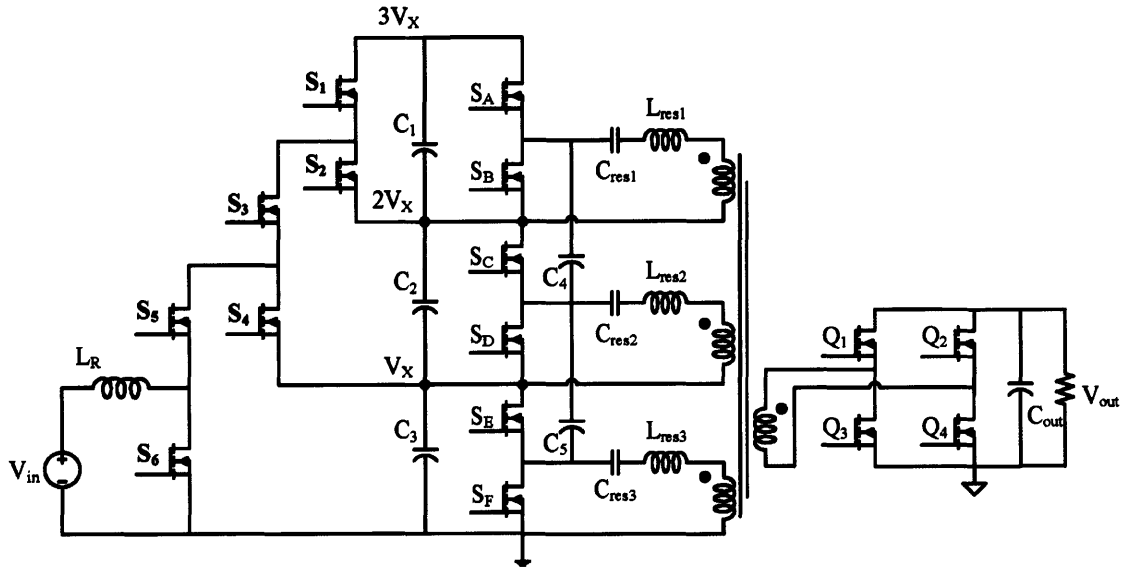


Figure 3-6: An example 3-track converter that can handle wide input voltage range. It is recognized that one needn't use all possible switches, depending on the desired input range. For example, one might remove S_6 and replace S_5 with a short in order to have a 3-to-1 input voltage range.

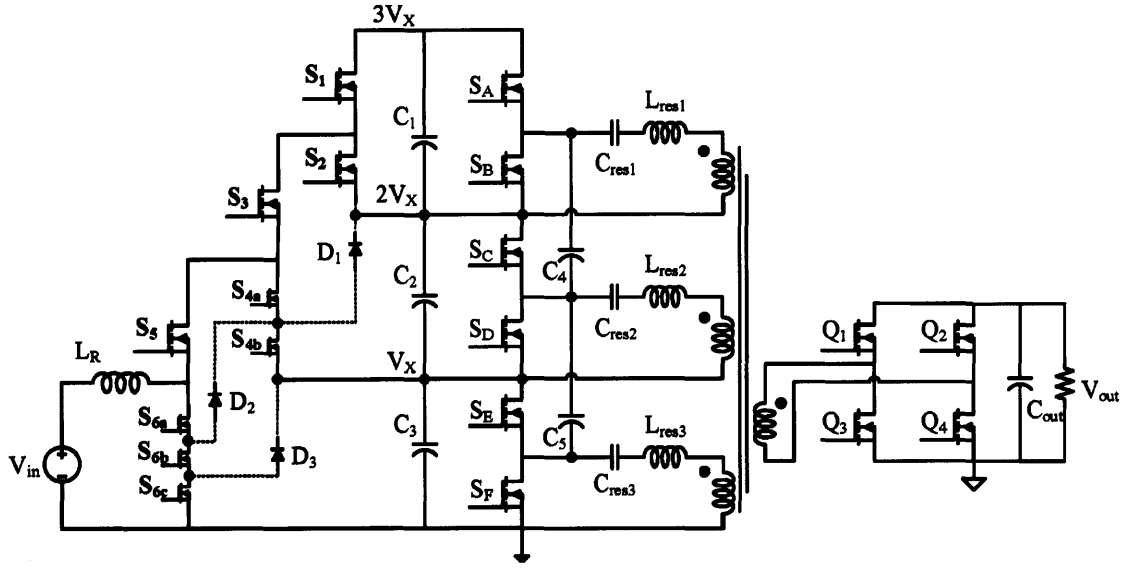


Figure 3-7: A modified 3-track converter with uniform switch voltage ratings. By replacing S_4 and S_6 with low voltage rating cascaded switches (S_{4a}, S_{4b}, S_{6a}, S_{6b}, S_{6c}), all primary side devices in this schematic have a voltage rating of V_X. One can add a few protection diodes (e.g. D_1-D_3) to help ensure voltage sharing of the cascaded switches.

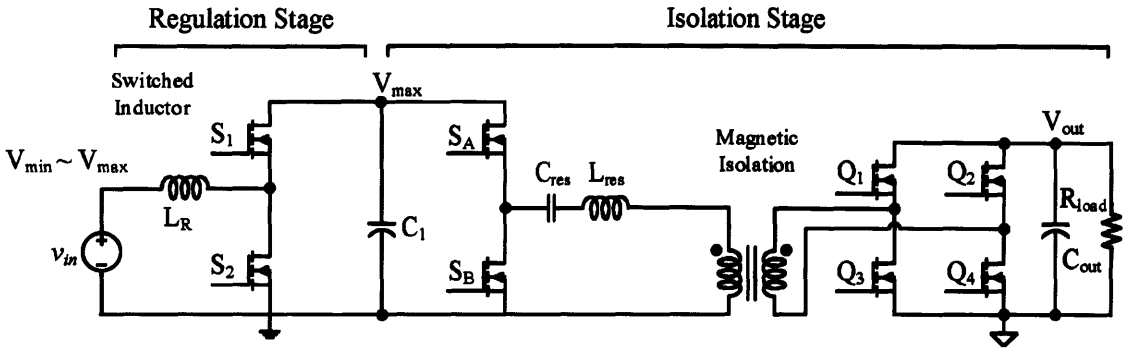


Figure 3-8: Schematic of a boost-type two-stage (BTS) converter having a boost converter as the regulation stage, and a series-resonant converter as the isolation stage.

diate bus voltage that is equal to or higher than the maximum input voltage. This voltage is then converted into the desired output voltage by an isolation stage with a fixed voltage conversion ratio. It is suitable to wide input-voltage range applications (e.g. in grid-tied power factor correction (PFC) systems [74–76]).[1]

The n-Track circuit can be interpreted as being somewhat similar to a n BTS circuit with an n-level boost converter structure, with n equal-voltage levels stacked on top of each other. Each of them processes $\frac{1}{n}$ of the full rated power. A key advantage of the MultiTrack architecture over the BTS architecture is the creation of the split voltage domains and the multiple balanced power delivery tracks. We compare the BTS converter with a n-Track converter for an input voltage range of $[V_{\text{min}}, V_{\text{max}}]$. The intermediate bus voltage of the conventional BTS converter is assumed to be V_{max}. The n intermediate bus voltages of the n-Track converter are $\frac{1}{n}V_{\text{max}}$, $\frac{2}{n}V_{\text{max}}$, $\frac{3}{n}V_{\text{max}}$, ..., V_{max}, respectively.

3.5.1 Reduced Regulation Inductor Size.

Both the BTS converter and the MultiTrack converter have a voltage regulation inductor (L_R) in the regulation stage. The size of L_R is related to the maximum amount of energy that it needs to buffer in each switching cycle, which is itself related to the voltage conversion

[1] A buck-type two-stage architecture with a buck converter as the regulation stage is also widely used. In a buck-type implementation, the wide input voltage range is first regulated to a voltage that is lower than or equal to the minimum input voltage. Since the Buck converter is a topological dual of the Boost converter, many of their theoretical characteristics are similar or even identical. The MultiTrack design we have implemented is more related to the boost-type two-stage architecture because its regulation stage is more similar to a boost converter. As a result, we use the boost-type two-stage architecture as a benchmark in this chapter.

ratio of the regulation stage [62]. We define Γ_E as the ratio between the energy buffered in the inductor in each switching cycle, and the total energy that the converter delivers in each switching cycle. For a fixed output power, a higher Γ_E ratio indicates a higher inductive energy buffering requirement, yielding a larger inductor size. As derived in Appendix B.1, the Γ_E of the BTS converter when $V_{\min} < v_{\text{in}} < V_{\max}$ is

$$\Gamma_{\text{E,BTS}}|_{(V_{\min}<v_{\text{in}}<V_{\max})} = 1 - \frac{v_{\text{in}}}{V_{\max}}. \tag{3.3}$$

It increases monotonically as the input voltage reduces. This is due to the fact that the boost converter in the BTS architecture has a higher voltage conversion ratio if the input voltage is lower (closer to $V_{\min}$). The inductor needs to be sized for the worst case - when the input voltage equals to $V_{\min}$.

The Γ_E of a n track converter when $V_{\min} < v_{\text{in}} < V_{\max}$ is a piecewise function of v_{in}. The percentage of energy that is buffered in the inductor when v_{in} belongs to the k_{th} sub-section of the input voltage range, i.e. $[\frac{k-1}{n}V_{\max}, \frac{k}{n}V_{\max}]$, is

$$\begin{aligned}&\Gamma_{\text{E,n-track}}|_{\frac{k-1}{n}V_{\max}<v_{\text{in}}<\frac{k}{n}V_{\max}} \\ &= \frac{\left(\frac{k}{n}V_{\max} - v_{\text{in}}\right)\left(v_{\text{in}} - \frac{k-1}{n}V_{\max}\right)}{\frac{1}{n}V_{\max}v_{\text{in}}}.\end{aligned} \tag{3.4}$$

Eq. 3.3 and Eq. 3.6 are plotted and compared in Fig. 3-9. The Γ_E of an 1-Track converter is identical to the Γ_E of a boost converter. And the Γ_E gradually reduces as the number of tracks increases. Fig. 3-10 compared the maximum Γ_E for a BTS converter[2] and multiple n-track converters as a function of the input voltage range ($V_{\max}/V_{\min}$ ratio). If $V_{\max}/V_{\min} = 2:1$, the maximum Γ_E of the BTS converter is 0.5, the maximum Γ_E of a 2-Track converter is 0.172, and the maximum Γ_E of a 4-Track converter is 0.101. If $V_{\max}/V_{\min} = 4:1$, the maximum Γ_E of the BTS converter is 0.75, the maximum Γ_E of a 2-Track converter is 0.5, and the maximum Γ_E of a 4-Track converter is 0.172. In general, for a specified input voltage range ($V_{\max}/V_{\min}$ ratio), increasing the number of tracks can reduce the maximum Γ_E, yielding smaller regulation inductor size at the expense of greater complexity and component count. As the number of tracks increases, the marginal advantages of adding more tracks gradually saturates.

[2]As the regulation stages are topological duals of each other, a buck-type two-stage converter has identical $\max(\Gamma_E)$ as the BTS converter for the same $V_{\max}/V_{\min}$ ratio. Both of them can be interpreted as a 1-Track system.

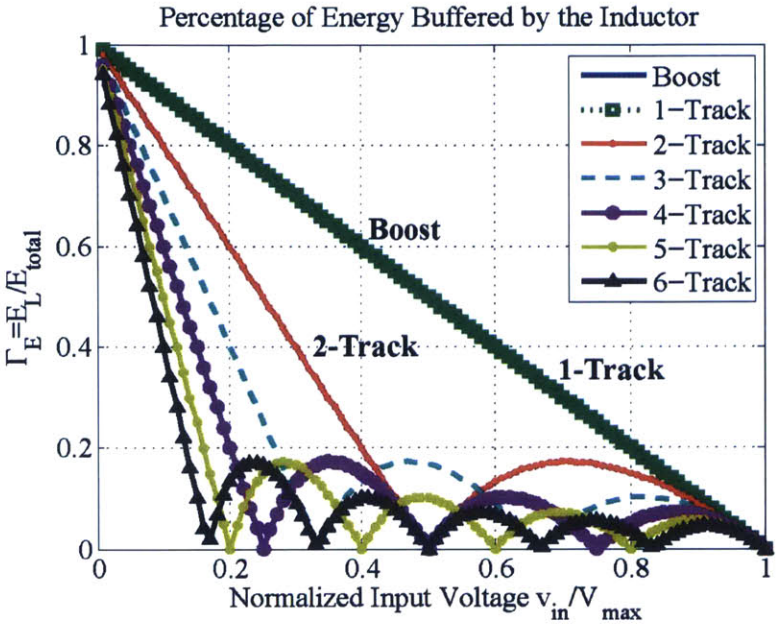


Figure 3-9: Fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_{\mathrm{L}}/E_{\mathrm{total}}$). E_{L} is the energy buffered by the inductor. E_{total} is the energy processed by the full system.

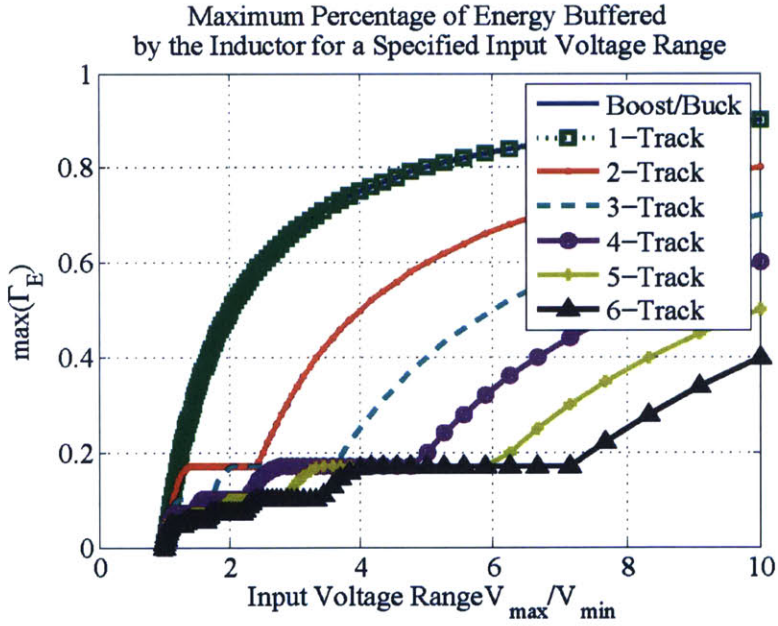


Figure 3-10: Fraction of energy buffered by the regulation inductor in each switching cycle ($\Gamma_E = E_{\mathrm{L}}/E_{\mathrm{total}}$). For a fixed overall power, Γ_E is proportional to the inductor size.

A special value $\max(\Gamma_E) = 0.172$ ($= \frac{\sqrt{2}-1}{\sqrt{2}+1}$) can be utilized as a threshold to indicate the saturation of the marginal advantages. According to Fig. 3-9, the minimum $v_{\text{in}}/V_{\max}$ that can have $\max(\Gamma_E)$ equals 0.172 is $\frac{2}{\sqrt{2}+1}\frac{1}{n}$. This relationship can be presented as a *MultiTrack Design Guideline*:

MultiTrack Design Guideline #1:

For a voltage conversion range of $\frac{V_{\max}}{V_{\min}}$, there is a threshold number of tracks ($n_{\text{th}} = \frac{2}{\sqrt{2}+1}\frac{V_{\max}}{V_{\min}} \approx 0.83\frac{V_{\max}}{V_{\min}}$) that would allow the regulation inductor to only buffer 17.2% of the total processed energy. The marginal advantages of adding more tracks beyond n_{th} would gradually saturate.

In other words, for a n-track converter, the maximum input voltage range that it can take to maintain a miniaturized inductor size (having an energy storage rating less than 17.2% than that required in a single-track design) is ($\frac{V_{\max}}{V_{\min}} = \frac{\sqrt{2}+1}{2}n \approx 1.2n$). Beyond this input voltage range, the required inductor energy storage rating would significantly increase.

By taking the derivative of Eq. 3.6 relative to v_{in}, the local maximum of Γ_E when v_{in} locates between $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$ are reached when the input voltage equals the geometric mean of the two voltages

$$v_{\text{in}} = \sqrt{\frac{kV_{\max}}{n} \times \frac{(k-1)V_{\max}}{n}} = \sqrt{k(k-1)}\frac{V_{\max}}{n}. \tag{3.5}$$

The local maximum is

$$\begin{aligned} &\max(\Gamma_{\text{E,n-track}}(v_{\text{in}})|_{\frac{k-1}{n}V_{\max}<v_{\text{in}}<\frac{k}{n}V_{\max}}) \\ &= \frac{\sqrt{\frac{k}{n}V_{\max}} - \sqrt{\frac{k-1}{n}V_{\max}}}{\sqrt{\frac{k}{n}V_{\max}} + \sqrt{\frac{k-1}{n}V_{\max}}} = \frac{\sqrt{k}-\sqrt{k-1}}{\sqrt{k}+\sqrt{k-1}}, \end{aligned} \tag{3.6}$$

3.5.2 Reduced Switch Conduction Loss and Switch Stress.

The switches in the regulation stage of the BTS converter (S_1 and S_2) have to block the peak input voltage ($V_{\max}$). In the wide-input-voltage-range 2-Track converter (Fig. 3-4),

S_1, S_2 and S_3 only need to block $\frac{1}{2}V_{\max}$. S_4 still needs to block $V_{\max}$, but it only conducts for portion of the input voltage range[3]. This mechanism reduces the conduction loss on switches. It is derived in [13] that for an ideal Schottky junction device, the on-resistance (per die area) of the drift region is a quadratic function of its rated voltage V_B,

$$R_{\text{dson}-1} = \frac{4V_B^2}{\epsilon_S \mu_n E_C^3}, \tag{3.7}$$

where $\epsilon_S \mu_n E_C^3$ is a constant that is related to the material characteristics ("Baliga Figure-of-Merit"). In a BTS converter, S_A and S_B both needs to block $V_{\max}$. Assume all of them have the same drain-to-source resistance R_{BTS}, and the regulation inductor has small current ripple, the total conduction loss in the two switches can be calculated as a function of the input voltage (v_{in}) and input power (P_{in}):

$$Loss_{\text{BTS}} = (\frac{P_{\text{in}}}{v_{\text{in}}})^2 R_{\text{BTS}}. \tag{3.8}$$

In a n track converter, all high-side switches in the modular half-bridge pairs (S_1, S_3, S_5, ..., S_{2n-1}) need to block $\frac{V_{\max}}{n}$. According to Eq. (3.7), since the device resistance is a quadratic function of the rated voltage, their resistance can be approximated as $\frac{R_{\text{BTS}}}{n^2}$. The low side switches in the modular half-bridge pairs (S_2, S_4, S_6, ..., S_{2n}) need to block ($\frac{1}{n}V_{\max}$, $\frac{2}{n}V_{\max}$, $\frac{3}{n}V_{\max}$, ..., $\frac{n}{n}V_{\max}$), respectively. And their resistances would ideally scale as ($\frac{R_{\text{BTS}}}{n^2}$, $\frac{2^2 R_{\text{BTS}}}{n^2}$, $\frac{3^2 R_{\text{BTS}}}{n^2}$, ..., $\frac{n^2 R_{\text{BTS}}}{n^2}$), respectively.

The total conduction loss is a piecewise function of the input voltage v_{in}. Using our idealized scaling rules, we can approximate the impact of the MultiTrack system on device loss. When v_{in} is between $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$, a total of $(k-1)$ switches (S_{2n-1}, S_{2n-3}, ..., $S_{2n-2k+3}$) with their resistances equal to $\frac{R_{\text{BTS}}}{n^2}$ are kept on and are conducting. One $\frac{R_{\text{BTS}}}{n^2}$ switch ($S_{2n-2k+1}$) and one $\frac{(n-k)^2}{n^2}R_{\text{BTS}}$ switch (S_{2n-2k}) are conducting with a duty ratio of ($\frac{v_{\text{in}}n}{V_{\max}} - k + 1$); and one $\frac{(n-k+1)^2}{n^2}R_{\text{BTS}}$ switch ($S_{2n-2k+2}$) is conducting with a duty ratio of ($k - \frac{v_{\text{in}}n}{V_{\max}}$). The input current, i_{in}, is also a function of v_{in}, $i_{\text{in}} = P_{\text{in}}/v_{\text{in}}$. Assume the inductor current equals the input current and has no ripple. The total conduction loss in

[3] S_4 can also been implemented as a switch string with voltage sharing imposed using the different levels

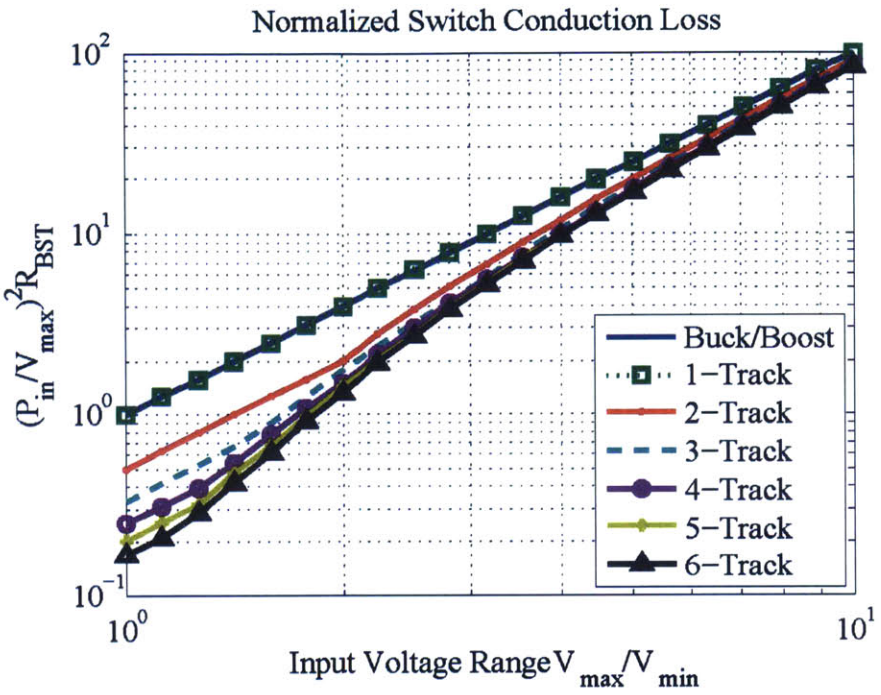


Figure 3-11: Normalized switch conduction loss as a function of the input voltage range. The Buck/Boost converter and 1-Track converter have identical switch conduction loss, which scales quadratically with the input voltage range. An n-track converter always has lower conduction loss than single track converters.

the devices of the switched-inductor circuit can be estimated as

$$\begin{aligned} Loss_{\text{ntrack}} &= (k-1)\frac{P_{\text{in}}^2}{v_{\text{in}}^2}\frac{1}{n^2}R_{\text{BTS}} \\ &+ \frac{P_{\text{in}}^2}{v_{\text{in}}^2}\left(\frac{1}{n^2}R_{\text{BTS}} + \frac{(n-k)^2}{n^2}R_{\text{BTS}}\right)\left(\frac{v_{\text{in}}n}{V_{\text{max}}} - k + 1\right) \\ &+ \frac{P_{\text{in}}^2}{v_{\text{in}}^2}\left(\frac{(n-k+1)^2}{n^2}R_{\text{BTS}}\right)\left(k - \frac{v_{\text{in}}n}{V_{\text{max}}}\right) \end{aligned} \tag{3.9}$$

Fig. 3-11 plots the worst-case conduction loss of a buck/boost converter and multiple n-Track converters as a function of the input voltage range ($V_{\text{max}}/V_{\text{min}}$), and assuming the device voltage scaling rule described previously (Eq. 3.7). For Buck/Boost/1-Track converters, the conduction loss scales quadratically with the input voltage range (because the conduction loss is a quadratic function of the input current). For an n-Track converter, when $1 < \frac{V_{\text{max}}}{V_{\text{min}}} < \frac{n}{n-1}$, the conduction loss is linearly reduced by a factor of $1/n$. For wider input voltage range, e.g. if $\frac{V_{\text{max}}}{V_{\text{min}}} > \frac{n}{n-1}$, the conduction loss gradually approach

the conduction loss of the Buck/Boost/1-Track converters. This is because as the input-voltage-range expands, more current is carried by switches with high voltage ratings. This gradually saturated relationship can be presented as another *MultiTrack Design Guideline*:

MultiTrack Design Guideline #2:

For a fixed input voltage conversion range ratio $\frac{V_{\max}}{V_{\min}}$, there is an threshold number of tracks ($n_{\text{th}} = \frac{V_{\max}}{V_{\max}-V_{\min}}$) that can provide a significant reduction in conduction loss ($\frac{1}{n_{th}}$ of the conduction loss of a 1-Track converter). The marginal advantages of adding more tracks beyond n_{th} gradually saturate.

In other words, for a n-Track converter, the widest input voltage range it can take to achieve $1/n$ reduction in conduction loss is ($\frac{V_{\max}}{V_{\min}} = \frac{n}{n-1}$). Beyond this input voltage range, the conduction loss on switches would approach the conduction loss of the single-track converter.

In this comparison, the difference between the die-area of the Boost/Buck converter and the die area of the n-track converter is not considered/controlled. Generally speaking, the n-track converter requires more devices with lower voltage ratings and current ratings. It may or may not require larger die-area for the same power rating. For a specific die area and a specific n-track converter, the optimal die-area allocation on each device also depends on the input voltage range. All these factors may impact the tradeoff analysis in a specific design. With additional device-level and circuit-level assumptions, a rigorous theoretical comparison considering these effects can be done, though it is not pursued here.

3.5.3 Soft-Switching and Reduced Switching Loss

The high-side switch of a boost converter (S_1 in Fig. 3-8) can operate as a diode, with zero-voltage turn on. Under PWM operation with small inductor current ripple, the low side switch (S_2) is usually hard-switched at both turn on and turn off. S_2 needs to block $V_{\max}$. In an n-Track converter, the low-side switches (S_2, S_4, ..., S_{2n}) have a similar situation and are typically hard-switched in the worst case. The voltage ratings of these switches are ($\frac{1}{n}V_{\max}$, $\frac{2}{n}V_{\max}$, $\frac{3}{n}V_{\max}$, ..., $\frac{n}{n}V_{\max}$), respectively. Although they have different voltage ratings, when they are switching, their off-state drain-to-source voltages are always $\frac{1}{n}V_{\max}$.

In other words, the Boost/Buck/1-Track converter has a "heavily-rated" device switching between zero and $V_{\max}$, and the n-Track converter has a "lightly-rated" device switching between $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$. Thus, the switching loss on the regulation switches of the n-Track converter can be much smaller (this is of course achieved at the expense of a higher switch and driver count in the MultiTrack system).

Quantitatively, assume all of these low-side switches are hard-switched, and assume the drain-to-source capacitance of all switches are linearly related to their current ratings (die area) and are not related to their voltage rating, the switching loss per cycle on the low-side switch of a boost converter with $V_{\max}$ as the intermediate bus voltage is

$$E_{\text{sw-BST}} = \frac{1}{2}C_{\text{oss-I}_{\text{pk}}}V_{\max}^2. \tag{3.10}$$

Here $C_{\text{oss-I}_{\text{pk}}}$ is the output capacitance of a switch that has to carry the maximum inductor current $I_{\text{pk}} = \frac{P}{V_{\min}}$. In comparison, when v_{in} is between $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$, in a n-Track converter, k switches are always on and have no switching loss (including S_{2n-1}, S_{2n-3}, ..., $S_{2n-2k+1}$), S_{2k-1} and S_{2k} are functioning as a half-bridge switch pair with $\frac{1}{n}V_{\max}$ as the drain-to-source voltage. The S_{2k-1} is zero-voltage turn on and can be soft-switched. The current rating of S_{2k} is $I_{S_k} = \frac{P}{\frac{k-1}{n}V_{\max}}$. The switching loss per cycle on S_{2k} is

$$E_{\text{sw-MultiTrack}} = \frac{1}{2}C_{\text{oss-I}_{S_k}}\left(\frac{V_{\max}}{n}\right)^2 \tag{3.11}$$

Since $I_{S_k} < I_{\text{pk}}$, thus $C_{\text{oss-I}_{S_k}} < C_{\text{oss-I}_{\text{pk}}}$. Comparing Eq. 3.10 and Eq. 3.11, we can conclude that the switching loss in the regulation stage of a hard-switched n-Track converter is bounded to be less than $\frac{1}{n^2}$ of that of a hard-switched buck/boost/1-Track converter.

Similar to the previous analysis about the device conduction loss, the difference between the die-area of the Boost/Buck converter and the die area of the n-track converter is not considered. With additional device-level and circuit-level assumptions, a rigorous theoretical comparison capturing these effects can be done, though it is not pursued here.

The n-level ladder switched capacitor circuits also have switching loss. Switches in a switched-capacitor circuits are usually hard switched. In the MultiTrack architecture, the combination of the switched capacitor circuits and the MISO transformer (the *hybrid switched-capacitor/magnetics* circuit structure) creates both soft-switching and soft-charging [23–25, 27, 28] opportunities for the switched-capacitor switches. In the 2-track

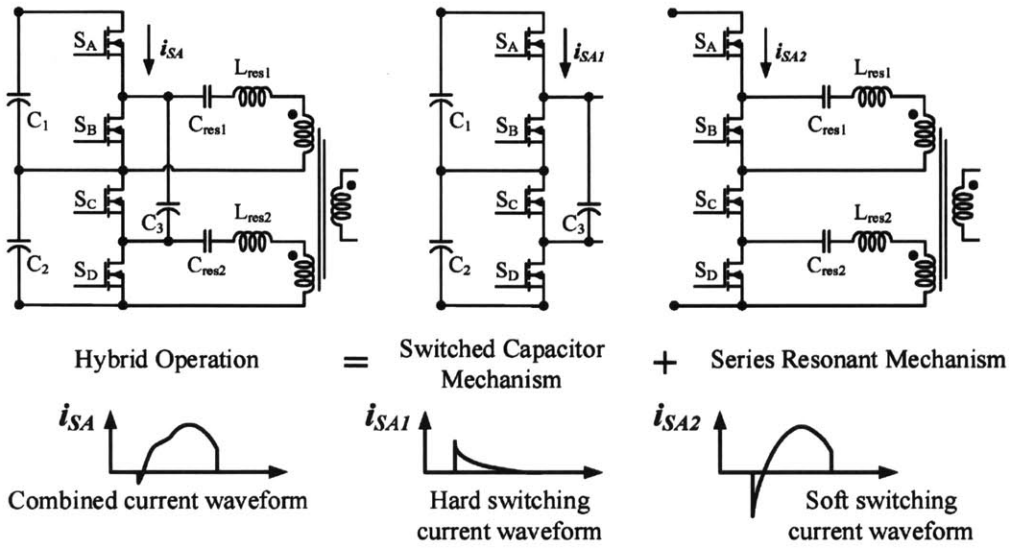
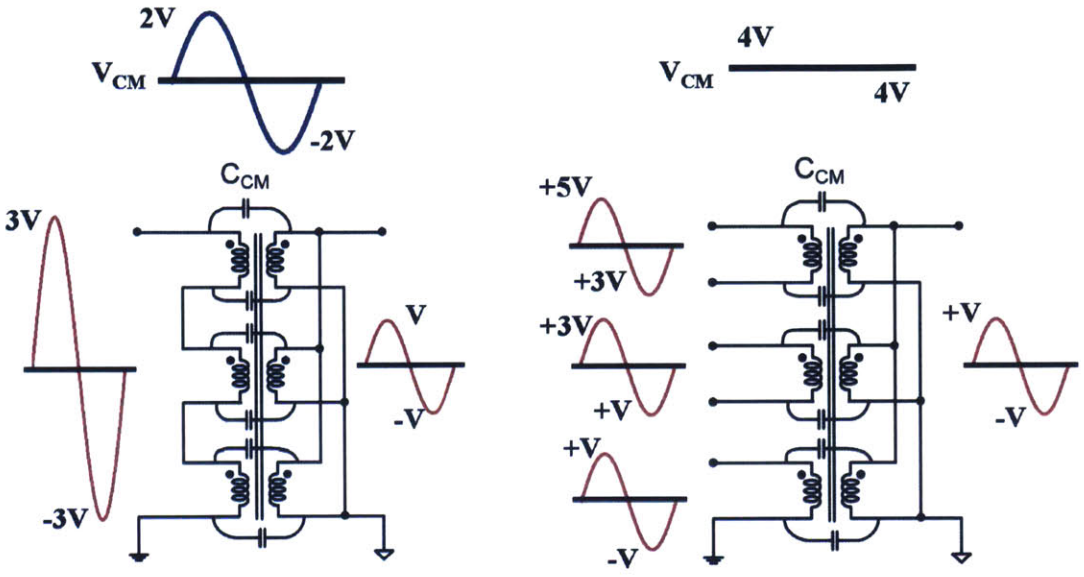


Figure 3-12: The *hybrid switched-capacitor/magnetics* circuit structure is the superposition of a hard-switched hard-charged ladder switched capacitor circuit, and multiple stacked soft-switched resonant circuits.

converter shown in Fig. 3-4, the operation of S_A-S_D can be interpreted as the superposition of a switched-capacitor circuit and two series-resonant circuits (Fig. 3-12). When the input voltage is close to V_{max} or when the load impedance is high, the switched-capacitor mechanism dominates - the switches see capacitive load and are hard-switched. When the input voltage is close to V_{max} or when the load impedance is low, the series-resonant mechanism dominates - the switches see inductive load and can be zero-voltage-switching (ZVS) soft-switched. Note the four switches (S_A-S_D) see different impedances when they are switching.

3.5.4 Reduced Voltage Drive on Common-Mode Capacitances

Small common-mode current flow (i.e.,from primary to secondary) is desired in most isolated power conversion applications. This requirement becomes increasingly critical as the converter operates at increasingly high frequencies. The MISO transformer structure helps to reduce the ac voltage drive across these common-mode capacitances as compared to a single series primary winding of the same number of turns, and thus reduce the induced common-mode reactive energy flow. In a fully interleaved planar transformer having n series-connected single-turn primary layers and n parallel-connected single-turn secondary



(a) Series-Primary Parallel-Secondary Transformer

(b) Multiple Input Single Output Transformer

Figure 3-13: The ac-voltage-drive across the common-mode capacitance of the Multiple-Input-Single-Output transformer is much lower than the ac voltage-drop across the common-mode capacitance of a conventional high-turns-ratio transformer (e.g. having primary layers connected in series, and secondary layers connected in parallel).

layers, as shown in Fig. 3-13a, the voltage drop across the common-mode capacitance between the top primary layer and the top secondary layer changes between $-\frac{n-1}{n}V_{\max}$ and $\frac{n-1}{n}V_{\max}$, inducing a significant common-mode reactive energy flow of $\frac{1}{2}C_{CM}\frac{(n-1)^2}{n^2}V_{\max}^2$ (in this example, n=3 and $V_{\max}$=3V). Similar results can be found in other primary-to-secondary capacitances. If the primary and secondary windings are configured as a MISO transformer having n separated single-turn primary layers as shown in Fig. 3-13b, the common-mode capacitances only block dc voltage, and there is ideally no common-mode capacitance current flow between the primary side and the secondary side.

3.6 Prototype Design

To demonstrate and evaluate the advantages of the MultiTrack power conversion architecture, a 18 Vin-80 Vin, 5 Vout, 15 Aout, 75 W, 800 kHz, 2-Track converter has been built and tested. The prototype is designed based on the schematic shown in Fig. 3-4. Full

Table 3.2: Bill of Materials (BOM) of the prototype converter.

Schematic Symbol	**Component Name**
S_1-S_4, S_A-S_D	EPC2016c, 100 V
L_R	Coilcraft EPL6024-522ME: 5.2 uH, 44 mohm, height (measured): 2 mm
C_{in}	X5R Ceramic, 100 V, 2 uF, 1206
C_1, C_2	X7R Ceramic, 50 V, 10 uF, 1206
C_3	X7R Ceramic, 50 V, 15 uF, 1206
C_{out}	X5R Ceramic, 10 V, 188 uF, 0805
C_{res1}, C_{res2}	C0G Ceramic, 50 V, 0.1 uF, 1206; X7R Ceramic, 50 V, 0.2 uF, 1206;
MISO Transformer	Ferroxcube EQ13, Core Material 3F45, turns ratio 4:4:1, 8-layer PCB layers and 2 external 2 oz foil layers. An extracted lumped model of the transformer is provided in Fig. 3-20.
Q_1-Q_4	EPC2023c
All gate drives	TI LM5113
Primary side linear regulator	Linear Tech LT1060 40 V-5 V
Level-shifter diode	Bourns CD0603 80 V 100 mA
Level-shifter capacitors	X7R Ceramic, 50 V, 1 uF, 0603
Opto-coupler	Silicon Labs SI8420
Signal buffer	Texas Instruments SN74LVC
Secondary side gate driver supply	NXP BAT54XY Diode Array, Micrel MIC5235 LDO, a 4-turn auxiliary transformer winding printed on PCB Layers 3-6.

schematics, the bill of materials and the printed circuit board layout are provided in Appendix B. The two intermediate voltage levels are regulated at 40 V and 80 V, respectively. The simplified bill of materials of the prototype is listed in Table 3.2.

Fig. 3-14 shows the gate drive implementation of the eight primary-side switches (S_1-S_4 and S_A-S_D). Two identical gate drive modules are utilized. S_1, S_2, S_A and S_B are driven by one gate drive module referring to the V_X node. S_3, S_4, S_C and S_D are driven by another gate drive module referred to the input-side reference potential (ground). Each gate drive module contains one linear regulator, four level-shifters and two half-bridge gate drivers. The ground referenced gate drive module is powered by the input voltage. The

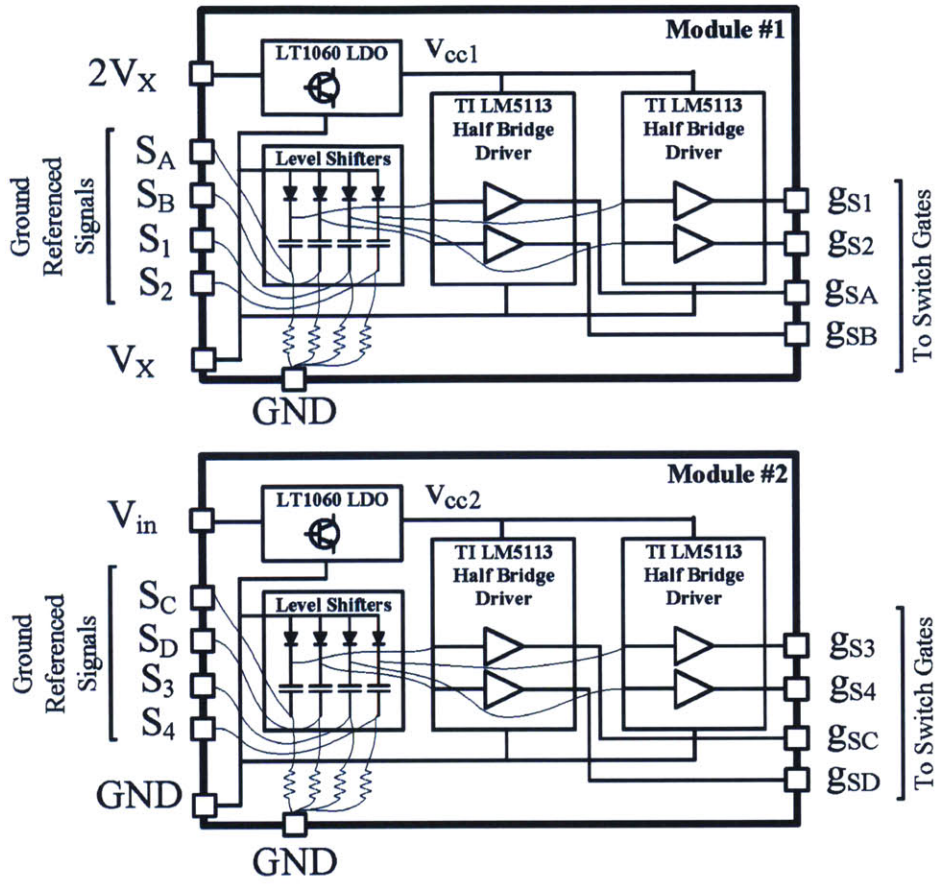


Figure 3-14: Gate drive implementation of the primary side switches. Two identical gate drive module are stacked in two voltage domains. This gate drive implementation can be easily extended and utilized in an n-track converter. The ground reference gate drive is powered from V_{in} to enable the startup of the circuit.

V_X referenced gate drive module is powered from C_1. This gate drive configuration can be easily integrated and extended to drive the switches in an n-track implementation. An auxiliary transformer winding (4-turns) with full-bridge diode arrays and linear regulators is utilized to power the two secondary-side half-bridge gate drivers.

An off-board Texas Instruments TMS320F28069 micro-controller with 4 PWM channels is utilized to control the prototype. As explained in Fig. 3-5, there are two operating modes for the regulation switches (S_1-S_4): (1) when the input voltage is between 18 V and 40 V, S_2 is kept on, S_1 is kept off, and S_3 and S_4 switch; (2) when the input voltage is between 40V and 80V, S_3 is kept on, S_4 is kept off, and S_1 and S_2 switch. In actual operation, however, neither of S_2 and S_3 can be kept on continuously; an interval is needed to enable

the boot-strap and level shifter capacitors to be refilled within a limited period of time. Also, when the input voltage is very close to 40 V, it is a challenge to modulate the duty ratio of S_2 and S_3 because their duty ratios are either very close to unity or zero. To address these practical issues, we had added a "Dual Modulation Mode" operation in which both the two half-bridge pairs are modulated:

1. *Low Input Voltage Mode:* when the input voltage is below 40 V, S_1 is mostly kept off, and S_2 is mostly kept on. S_2 may be switched off for a short period of time (minimum transistor on-time) every few switching cycles (10-20 cycles) to reset the level-shifter capacitor of S_2. S_3 and S_4 are switched at the PWM frequency.

2. *Dual Modulation Mode:* when the input voltage is close to 40 V, S_1 and S_4 are kept off, and S_2 and S_3 are kept on. S_2 and S_3 may be switched off for a short time every long period to reset their level-shifter/boot-strap capacitors. Modulating the difference between the on-time of S_2 and S_3 would provides the desired voltage regulation capability when the input voltage fluctuates around 40 V.

3. *High Input Voltage Mode:* when the input voltage is above 40 V, S_3 is mostly kept on, and S_4 is mostly kept off. S_4 may be switched on for a short period of time every few switching cycles to reset the boost-strap capacitor of S_3. And S_1 and S_2 are switched at the PWM frequency.

Fig. 3-15 illustrates the switching sequence of the four switches in the three regulation modes, as well as the corresponding voltage and current waveforms. The operating condition of the converter is jointly determined by the input voltage and the output power (i.e. load regulation behavior). Fig. 3-16 shows the measured input-voltage/output-current curves under a few relatively fixed control signal combinations. As the power changes, the input voltage is adjusted to regulate the output voltage. A clear load regulation behavior is observed. When the converter operates above Curve #1 ("High Input-Voltage Mode"), S_1 and S_2 are PWM modulated. When the converter operates below Curve #3 ("Low Input-Voltage Mode"), S_3 and S_4 are PWM modulated. When the converter operates between Curve #1 and Curve #3 ("Dual Modulation Mode"), both the two half-bridge pairs are modulated. It was experimentally verified that the switches in the regulation stage (S_1-S_4) can be turn-on/-off appropriately across the full power range with an on-/off-time of 150ns.

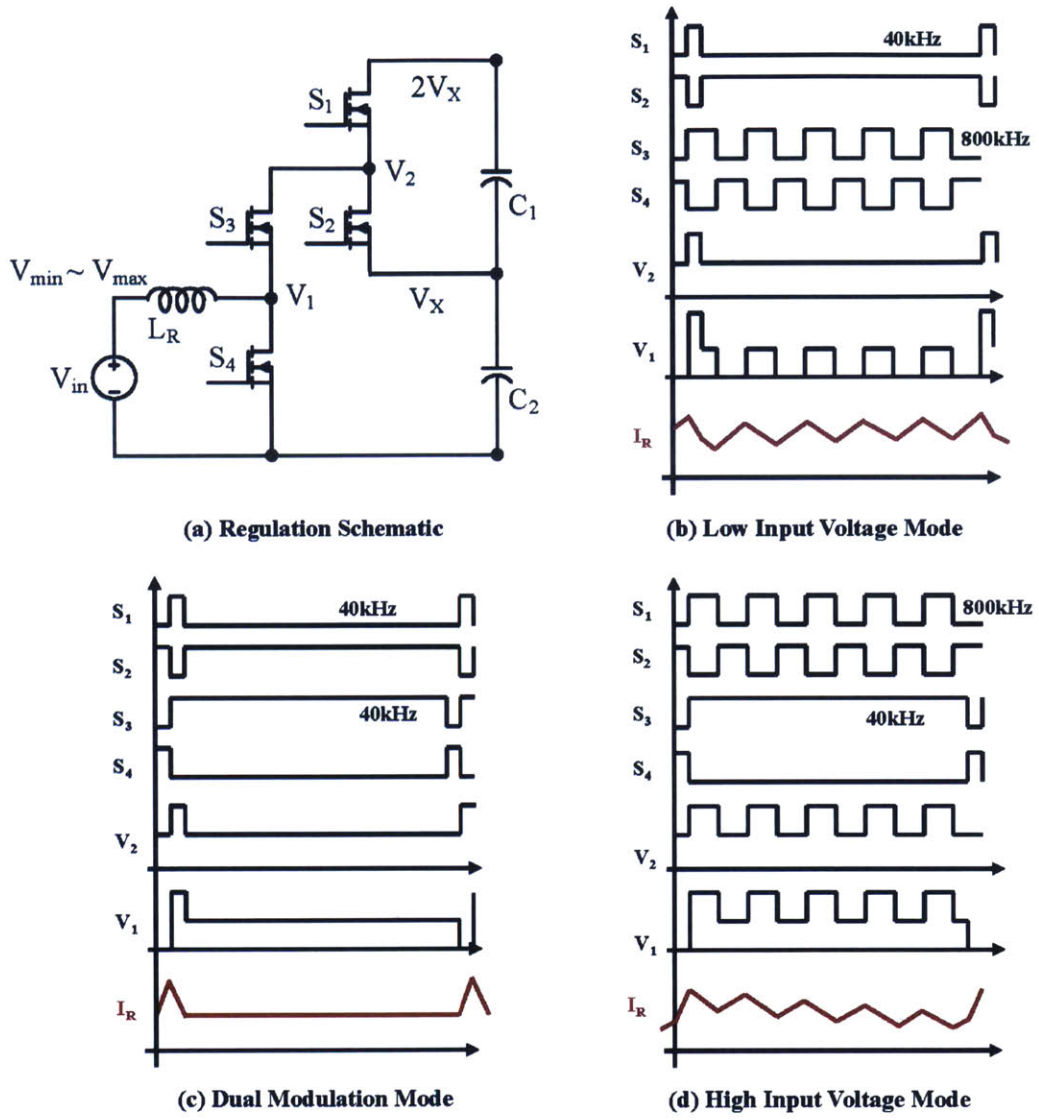


Figure 3-15: Three operation modes of the regulation stage. The distribution of the operation modes depend on the input voltage and output current. (a) Regulation circuit schematic. (b)-(d) Operation waveforms of the converter in the three operation modes.

Many strategies can be implemented to modulate the duty ratios of the two half-bridges. In this specific prototype, when the converter is operating on Curve #2, S_2 and S_3 are turned off for 150ns every 25μs to refill the boost-strap/level-shifter capacitors. Tuning the length of this "150ns" period according to the circuit operating may further improve the converter performance, although this option is not explored in this thesis.

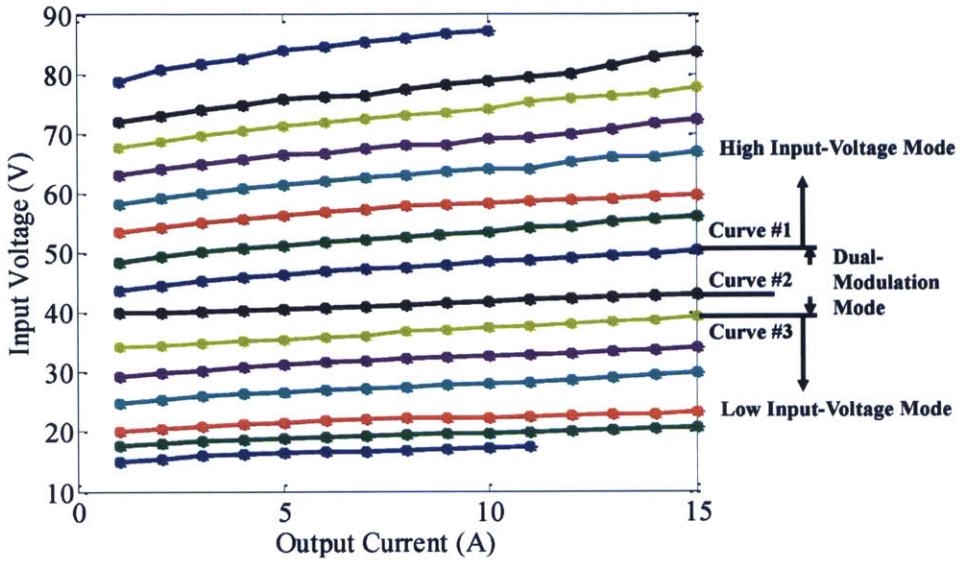


Figure 3-16: Curves of measured operating points when the converter operate in open-loop with fixed output voltage and variable input voltage.

Starting from Curve #2, as the operating point moves towards Curve #1, the clock frequency of S_1 and S_2 are gradually increased, reducing the effective duty ratio of S_2 (when S_2 is on). Similarly, as the operating point moves towards Curve #2, the clock frequency of S_3 and S_4 are gradually increased, reducing the effective duty ratio of S_3 (when S_3 is on). The duty ratio and clock frequency of S_1-S_4 when the converter is operating between Curve #1 and Curve #3 are listed in Table 3.3.

Assume the duty ratio of S_1 is d_1, and the duty ratio of S_3 is d_3, the relationship between the input voltage v_{in} and the voltage span of each voltage domain V_X, is:

$$\frac{v_{\text{in}}}{V_X} = d_3(1 + d_1). \tag{3.12}$$

Fig. 3-17 plots this relationship. Depending on the input voltage v_{in}, the modulation of d_1 and d_3 can be designed. To make efficient utilization of the switches, it is generally preferable to operate the converter close to the "SouthEast" boundary of this region (with d_1 close to zero, or d_3 close to unity).

Fig. 3-18a illustrates the implemented open-loop voltage regulation strategy (v_{in} as a function of d_1 and d_3). When the input voltage is below 40 V, d_1 is kept as low as possible and d_3 is modulated. When the input voltage is above 40 V, d_3 is kept as high as possible

Table 3.3: Duty ratio and clock frequency of S_1-S_4 when the converter is operating between the Curve #1 and Curve #3 labeled in Fig. 3-16.

Switches	**Curve #1**	**#1 ↔ #2**	**Curve #2**	**#2 ↔ #3**	**Curve #3**
S_1	0.12, 800 kHz	800 kHz↔40 kHz	0.006, 40 kHz	-	0.006, 40 kHz
S_2	0.88, 800 kHz	800 kHz↔40 kHz	0.994, 40 kHz	-	0.994, 40 kHz
S_3	0.994, 40 kHz	-	0.994, 40 kHz	40 kHz↔800 kHz	0.88, 800 kHz
S_4	0.006, 40 kHz	-	0.006, 40 kHz	40 kHz↔800 kHz	0.12, 800 kHz

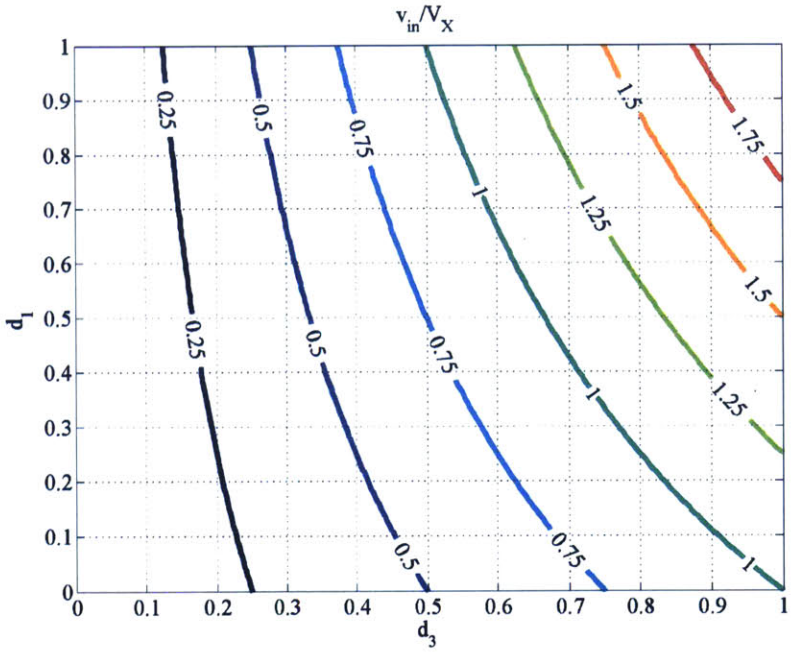


Figure 3-17: v_{in} to V_X ratio as a function of the duty ratio of S_1 and S_3 (d_1 and d_3). This plot can be utilized to develop the voltage regulation strategies of the MultiTrack converter.

and d_1 is modulated. To stabilize the system when the input voltage is crossing through 40 V, a hysteresis duty ratio locus is recommended (as illustrated in Fig. 3-18b). Again, this option is not explored in this thesis.

The regulation inductor should be designed such that it can work efficiently across the wide input voltage range and power range. Low profile is also a critical requirement in this prototype as the inductor tends to be the tallest component on the board. We choose to size the inductor such that it has 50% current ripple when the input voltage is at 30 V, the output power is 75 W, with 800 kHz switching frequency. The average inductor current is 2.5 A, and the calculated inductance value is 3.75 μH. A low profile Coilcraft inductor

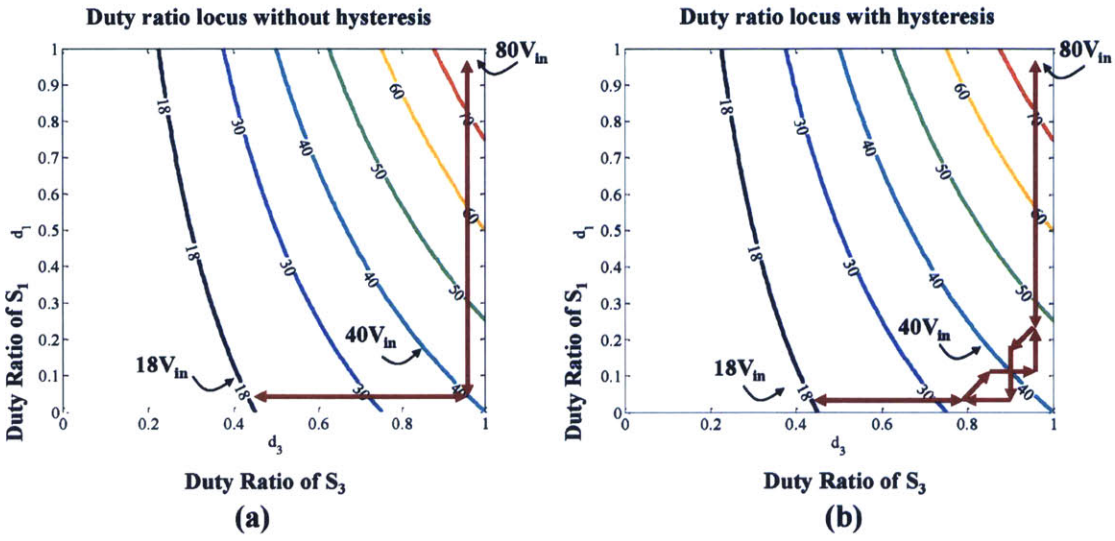


Figure 3-18: Duty ratio locus as a function of the input voltage (a) without hysteresis, (b) with hysteresis. Hysteresis helps to stabilize the system when the operating point crosses the boundaries of the two control modes. In this example design, the input voltage range is 18 – 80 V, and V_X equals 40 V .

(EPL6024-522) with 2 mm measured thickness is utilized to implement this inductor. Its loss across the overall input voltage range is within our budget. It is the tallest component on the board. It also limits the efficiency performance when the input voltage is close to the minimum of the full voltage range (e.g. 18 V). A custom designed inductor with wider area and lower thickness could further improve the power density and efficiency of the prototype (reducing the inductor height from 2 mm to 1.5 mm could raise the overall converter box power density from 453.7 W/in^3 to higher than 500 W/in^3.).

The multiple ac-tracks in the isolation stage are implemented as low Q series resonant converters. The resonant inductance of each low Q tank is created using the leakage inductance of the transformer, together with the PCB trace inductances. Since the resonant tank has low Q (when loaded with the equivalent rectifier resistance of 0.33 ohm at full power), close matching between the two primary windings is not necessary. The secondary winding of the multiple input single output (MISO) transformer needs to carry the high output current. As a result, its ac resistance should be minimized.

A Ferroxcube EQ13 core with 3F45 material was selected based on core loss and winding loss analysis. It was selected also because it has suitable window-area/core-area/height

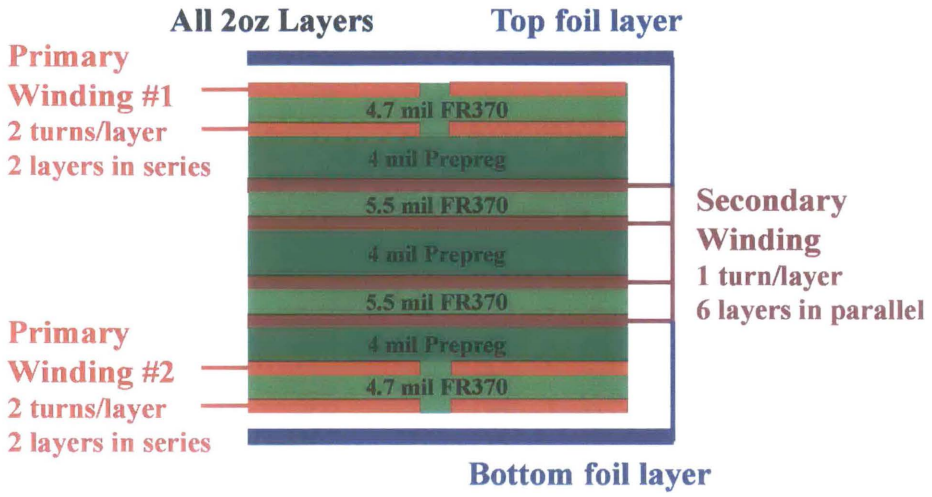


Figure 3-19: Cross-section view of the layer stack of the PCB Transformer.

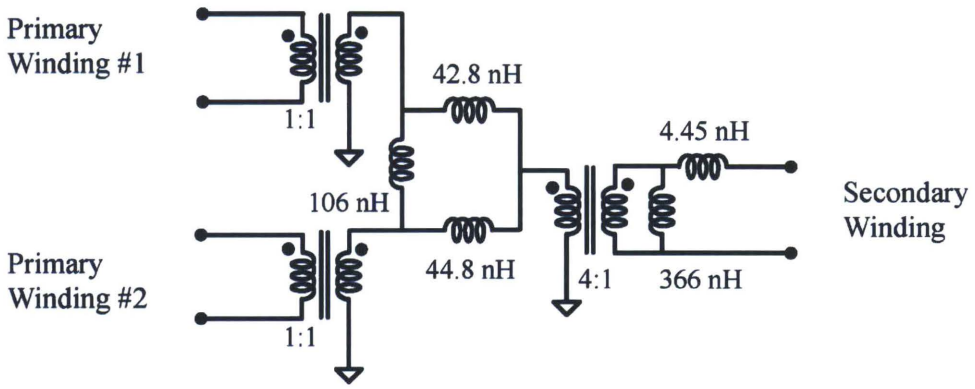


Figure 3-20: Experimentally extracted cantilever model of the prototype MISO transformer.

combinations. The windings were fabricated on a 8-layer printed circuit boards (PCB) with 2 oz copper on each layer. The finished pcb board thickness is 52 mil (1.32 mm). Fig. 3-19 shows the layer stack information. Layers 1,2,7,8 each have two series-connected turns. Layers 1–2 are connected in series through blind vias to implement a 4-turn primary winding. Layers 7–8 are also connected in series through blind vias to implement another 4-turn primary winding. Layers 3 through 6 are utilized to implement the single-turn secondary winding with the four layers connected in parallel. Two additional 2 oz foil layers were attached on top and bottom of the PCB board. They are connected as added parallel secondary windings to enable a "symmetric-interleaving" configuration to reduce the ac resistance and provide the flexibility to adjust the leakage inductance.

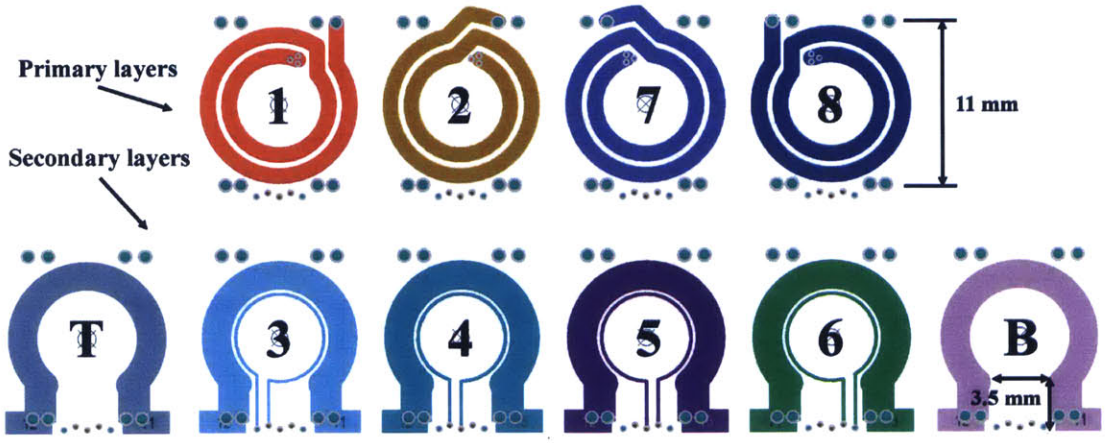


Figure 3-21: Layout of the PCB windings. Layers 1–2 are connected in series to formulate one primary winding. Layers 7–8 are connected in series to fomulate another primary winding. Layers 3–6, together with two foil layers on top and bottom of the PCB board (T and B), are connected in parallel to formulate the single-turn secondary winding.

The loop inductance between the two legs of the secondary winding also contributes to the series-resonant tank. Utilizing the method provided in [78], the loop inductance is estimated to be about 3 nH. The trace inductances added by the switches are estimated to be about 0.5 nH. The leakage inductance of the 10 layer PCB windings is estimated utilizing the planar magnetics modeling approach presented in Chapter 4. Fig. 3-20 shows the cantilever circuit model of the transformer extracted by doing open- and short-circuit measurements. Details about the transformer modeling (using the approach presented in Chapter 4) and parameter extraction are provided in Appendix B.2. The modeling results and measured results show a good match.

We seek to simplify the cantilever model to facilitate convenient design of the series-resonant tank of the MultiTrack converter. Fig. 3-22 illustrates a suggested four-step approach that is applicable to the resonant tank design if the multiple primary windings are driven by multiple identical voltage sources (e.g. as with the switched-capacitor circuit as the drive stage):

1. Step 1: the mutual inductance between the two primary windings (the 106 nH inductance in Fig. 3-20) can be neglected because the two primary windings are driven by two identical voltage sources synthesized by the ladder switched-capacitor circuit.

2. Step 2: the two 4-turn primary windings can be connected in series to formulate a single primary winding having 8 turns (assuming good current sharing between the two primary windings).
3. Step 3: the secondary side leakage inductance is reflected to the primary side and combined with the primary side leakage inductances.
4. Step 4: the 8-turn primary winding is split into two 4-turn primary windings with divided primary side leakage inductance.

Based on the estimated primary-side-lumped leakage inductance, the resonant capacitance is tuned experimentally to set the resonant frequency to be around 700 kHz – 750 kHz. The prototype utilized one 200 nF X7R ceramic capacitor, and one 100 nF C0G ceramic capacitor in parallel for each resonant capacitor. The switching frequency is 800 kHz.

3.7 Experimental Results

Fig. 3-23 shows pictures of the prototyped 18 V – 80 V input, 5 V/75 W isolated dc-dc converter and a US quarter. Fig. 3-24 shows component placement on the top abd bottom side of the PCB board. There are four modular switch and gate drive circuitry on the primary side. Each modular switch and gate drive circuitry consists two switches (EPC2016c) formulating a half-bridge, one LM5113 half-bridge gate drive, and the corresponding signal paths. They are placed on the top side of the PCB board. The full bridge rectifier consists four switches: two of them are on the top side of the board, two of them are on the bottom side of the board. The opto-coupler, linear regulator, capacitors and other auxiliary circuits and chips are placed on the bottom side of the board. The regulation inductor (L_R) is placed on the left-bottom corner of the PCB board. The off-board microcontroller, Texas Instruments TMS320F28069, interfaces with the prototype through a 10-pin interface. If the microcontroller needs to be placed on the board, the 10-pin interface can be removed to create enough board area. The minimum package area of the TMS320F28069 microcontroller is 12 mm×12 mm.

Fig. 3-26 shows the operation waveforms of the primary side of the converter. In this operation point, soft-switching of many primary side switches, including the switches in the switched-capacitor circuit are achieved (V_{sw}). Fig. 3-27 shows the operation waveforms

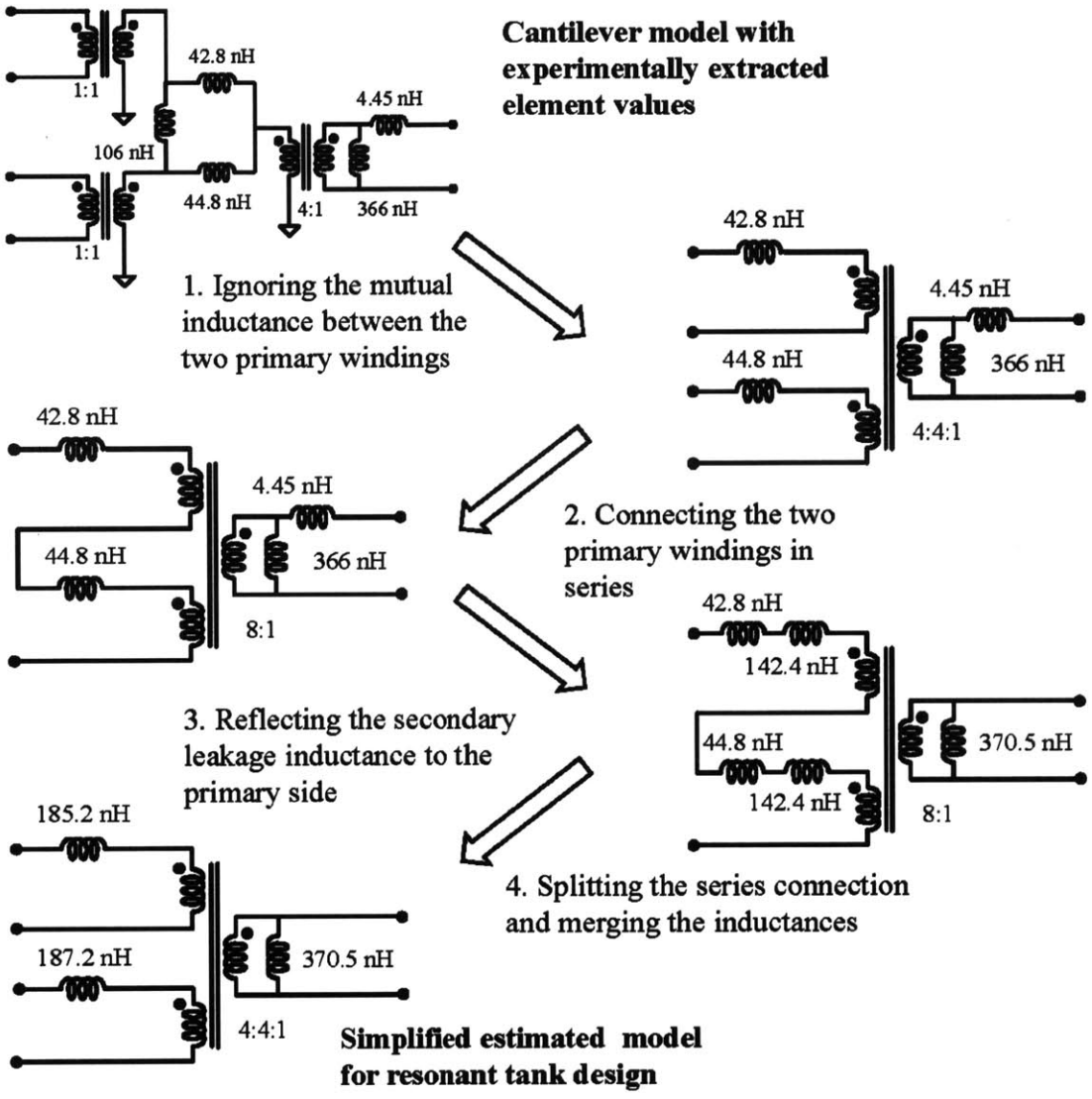


Figure 3-22: Converting the cantilever model into a simplified lumped circuit model which is suitable to the resonant tank design.

of the prototype under three operation modes with different input voltages. Fig. 3-28 and Fig. 3-29 shows the measured efficiency of the prototype with ambient temperature at 200 LFM, 25°C air flow (measured using a Pyle PMA90 digital anemometer with a 2.4 W fan placed in open space). The converter achieves a peak efficiency of 91.3% when the input voltage is 58 V and when the output current is 8 A. Fig. 3-30 compares the thermal images of the converter working with three different input voltages when they are all delivering

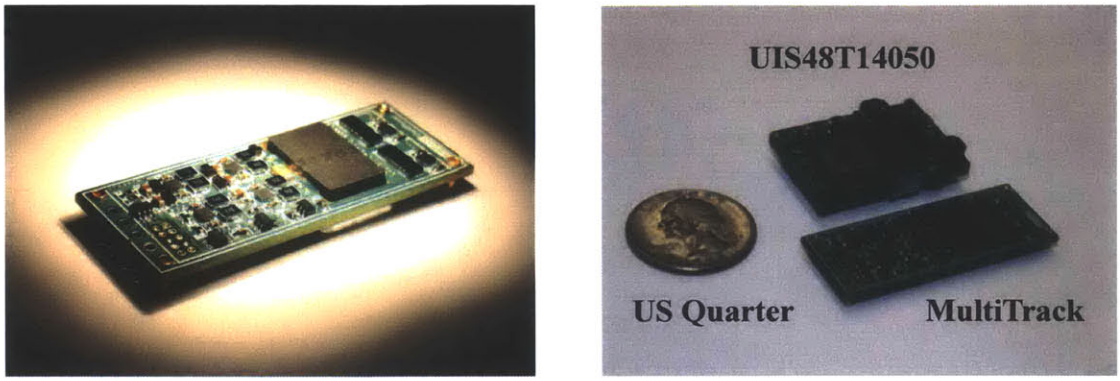


Figure 3-23: Pictures of the MultiTrack prototype, a US quarter, and a commercial product (UIS48T14050).

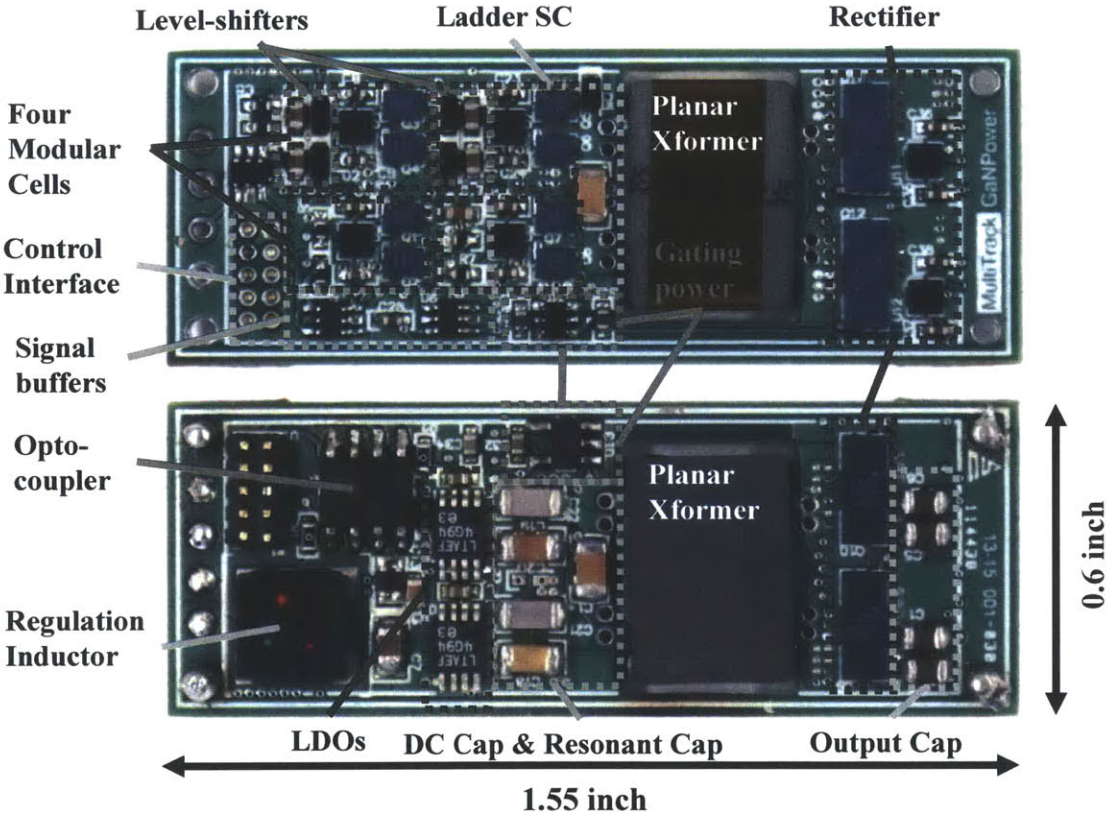


Figure 3-24: Component placement on the top and bottom side of the PCB board. The four modular half-bridge cells contain level shifters, LDOs, gate drivers and switches.

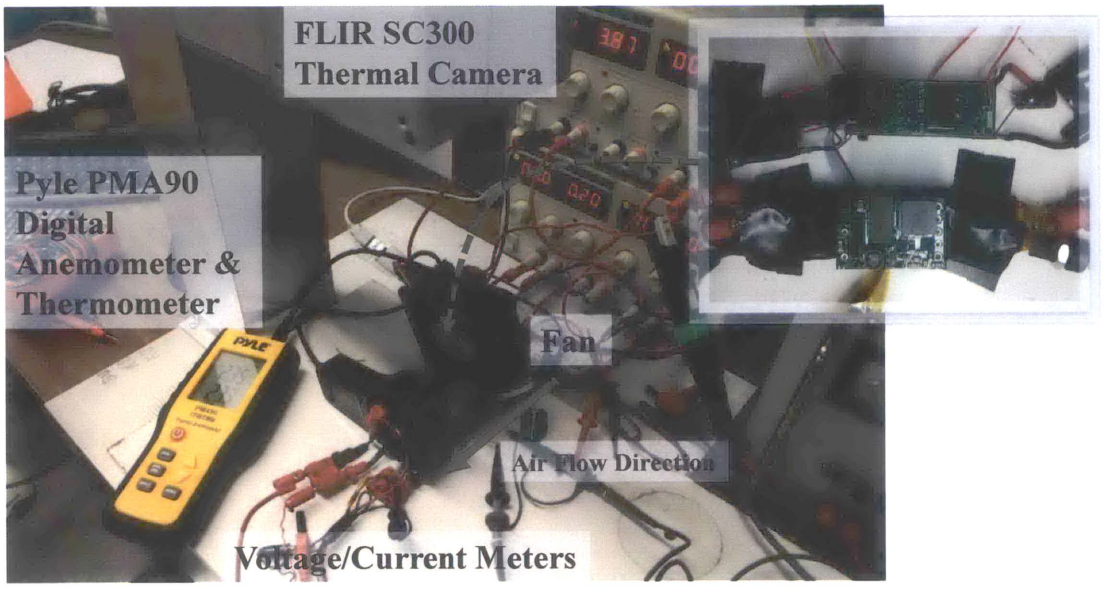


Figure 3-25: Experimental setup of the thermal related measurements.

7 A output current (using a FLIR E6 thermal camera). When the input voltage is high, the secondary side conduction loss dominates. When the input voltage is close to 40 V, the ladder switched capacitor mechanism causes high loss on S_A and S_B. When the input voltage is low, high current is processed through the input side switches, resulting in them having the highest temperature rise.

A thermal derating test has been done in the lab using a 2.4 W fan, a thermal camera (FLIR E6), and a digital anemameter (Pyle PMA90 digital anemometer). With 200 LFM 25 °C air flow (a typical Telecom power supply application working environment) and 20 V input voltage, the prototype delivers 15 A output current with a peak board temperature of 115 °C. This represents a power density of 453.7 W/inch^3. When there is no air flow, the peak board temperature reaches 125 °C when the output current is 12 A (339 W/inch^3), and reaches 150 °C when the output current is 13.5 A (381.3 W/inch^3).

A state-of-art commercial 1/16 brick 18 Vin-75 Vin 5 V/70 W isolated dc-dc converter (Power-One UIS48T14050) was utilized to benchmark this MultiTrack prototype (This converter has the highest power density among commercial converters with similar input voltage range that the authors were able to find). Fig. 3-31 compares the form factor of the two converters. Both converters have two magnetic devices - one transformer and one inductor

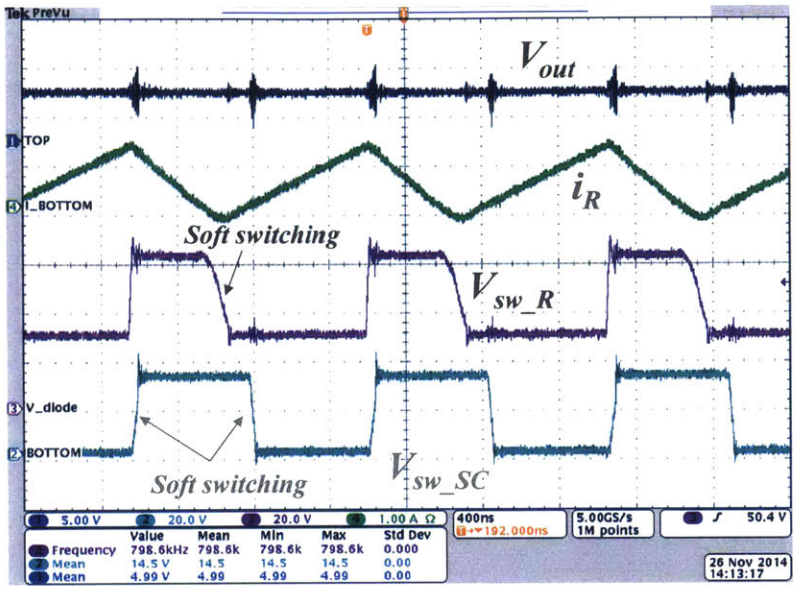
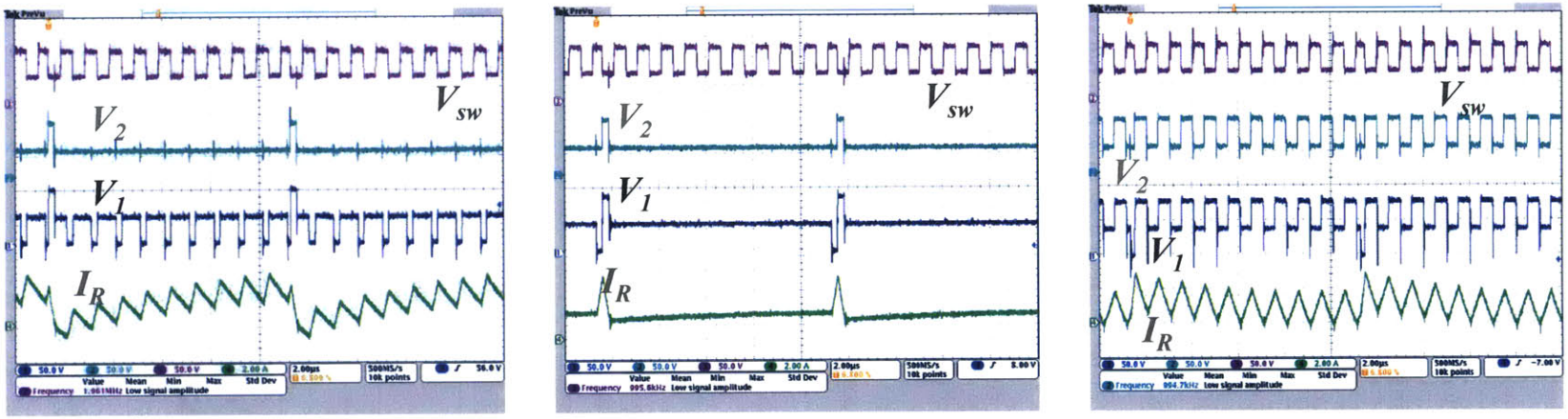


Figure 3-26: Operation waveforms of the prototype converter when the input voltage is 52 V and the output power is 6 A. V_{out}: output voltage; i_{R}: current of L_{R}; v_{swR}: voltage at the switch node of the switched-inductor circuit; v_{swSC}: voltage at the switch node of the ladder switched-capacitor circuit. Soft-switching voltage waveforms are observed in both two nodes.

(this commercial product is speculated to be a forward converter). The inductor utilized in the MultiTrack converter is much smaller (thinner) than the inductor utilized in the commercial converter. The box power density of the MultiTrack prototype is 457.3 W/inch^3, which is more than three times higher than the 143.5 W/inch^3 of the commercial product (under 200 LFM 25 °C air flow and 125 °C peak device temperature). The prototype weights 6.53 g, which is less than a half of the 15.3 g of the commercial product.

The measured efficiency data of the commercial product under the same setup as the MultiTrack converter is provided in Fig. 3-34 and Fig. 3-35. The overall efficiency of the commercial product is comparable to the efficiency of the MultiTrack prototype. When the input voltage is high, the MultiTrack converter is more efficient. When the input voltage is low, the commercial converter is more efficient. The efficiency of the commercial product drops monotonically as the input voltage increases. In comparison, the efficiency of the MultiTrack prototype is relatively independent of the input voltage.

The surface area available for heat extraction remains relatively unchanged in both of the two converters. In the MultiTrack converter, heat is generated by multiple distributed



(a) Low Input Voltage Mode **(b) Dual Modulation Mode** **(c) High Input Voltage Mode**

Figure 3-27: Example operation waveforms of the prototype converter working in three different operation modes: (a) Low Input Voltage Mode: v_{in}=20 V, I_{out}=7 A, with S_1 and S_2 switched at 80 kHz, and S_3 and S_4 switched at 800 kHz; (b) Dual Modulation Mode: v_{in}=40 V, I_{out}=9.5 A, with two half-bridges both switched at 80 kHz; (c) High Input Voltage Mode: v_{in}=60 V, I_{out}=10 A, with S_1 and S_2 switched at 800 kHz, and S_3 and S_4 switched at 80 kHz. The dual-modulation frequency was selected as 80 kHz in this demonstration to show the low frequency fluctuation of the inductor current. The real circuit operation used 20kHz as the lower frequency.

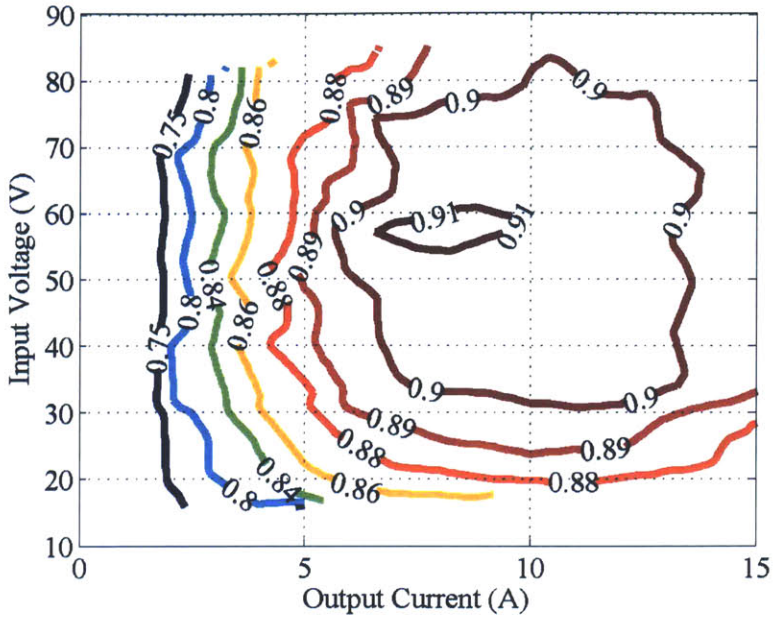


Figure 3-28: Efficiency of the MultiTrack converter over the 0 A – 15 A, 18 V – 80 V range. This efficiency is measured with 200 LFM, 25°C air flow. The air flow direction is indicated in Fig. 3-30.

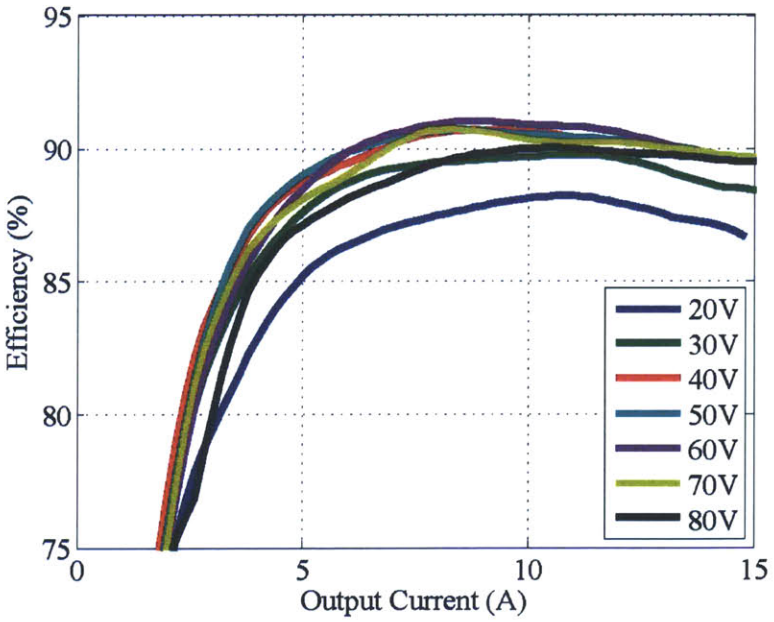
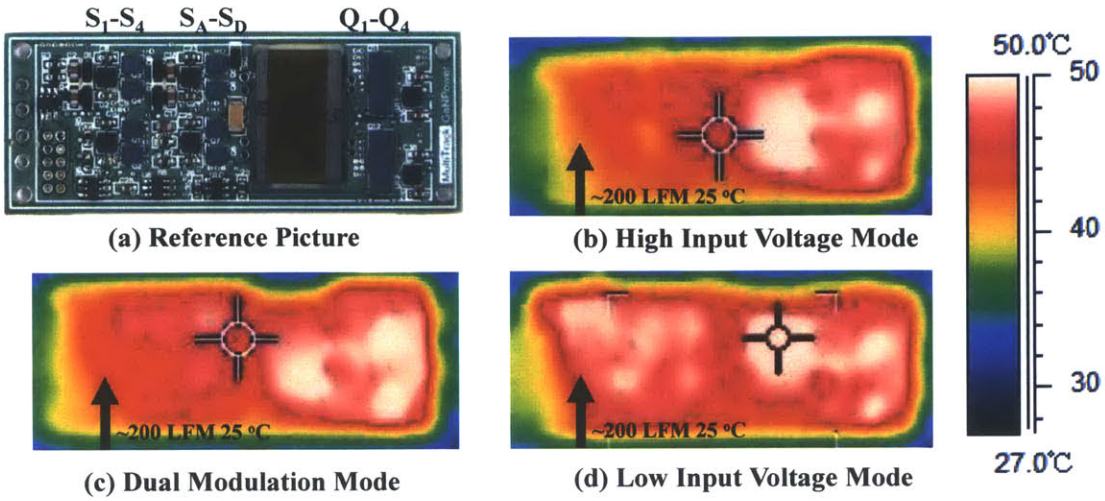


Figure 3-29: Efficiency of the prototype converter over the 0 A – 15 A, 18 V – 80 V range. This efficiency is measured with 200 LFM, 25°C air flow. The air flow direction is indicated in Fig. 3-30.



(a) Reference Picture (b) High Input Voltage Mode

(c) Dual Modulation Mode (d) Low Input Voltage Mode

Figure 3-30: Hot spots of the converter working in the three operation modes. The thermal images were taken with 25 °C 200 LFM air flow blowing from bottom to top. (a) Reference picture; (b) High input voltage mode: V_{in}=60 V, I_{out}=7 A, 90.7% efficiency; (c) Dual modulation mode: V_{in}=40 V, I_{out}=7 A, 90.2% efficiency; (d) Low input voltage mode: V_{in}=20 V, I_{out}=7 A, 88% efficiency.

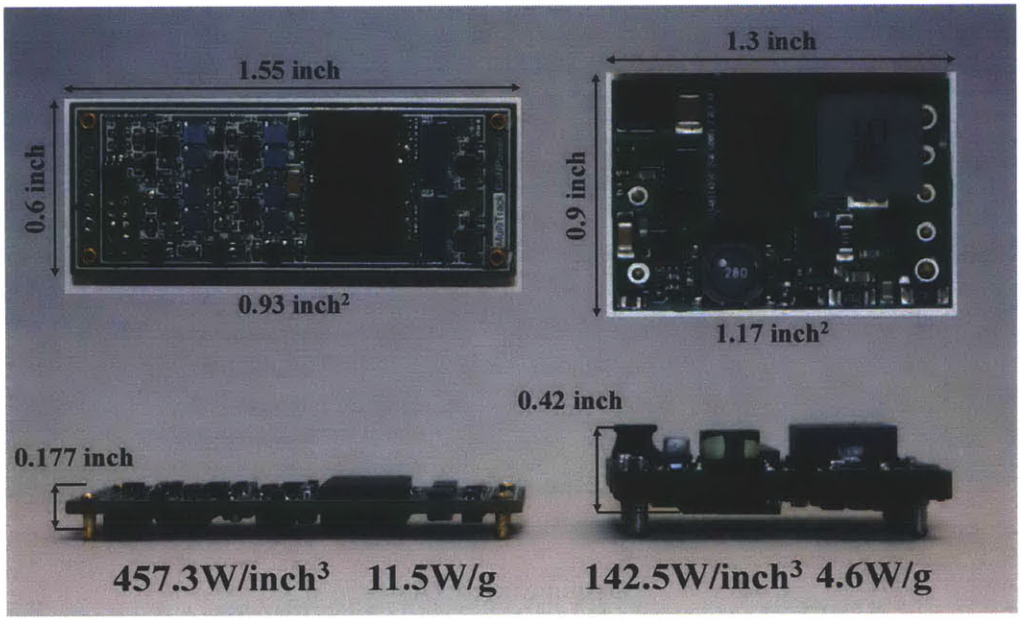
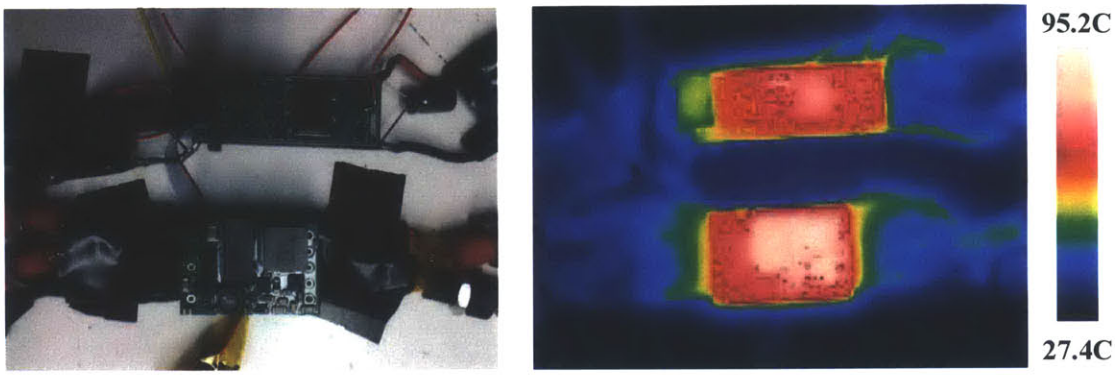


Figure 3-31: Form factors of the prototype MultiTrack converter (left) and a comparable commercial converter (PowerOne UIS48T14050, right).



(a) Experimental Setup (a) Thermal Image

Figure 3-32: Thermal image of the MultiTrack converter and the comparable commercial converter when they are working with 42 V input voltage and 7 A output current (measured with no air flow, 0 LFM, 25°C).

devices, allowing heat to be more easily removed and providing lower temperature rise. Fig. 3-32 shows the thermal images of the MultiTrack converter and the commercial converter when they are operating in the same steady-state condition (41 Vin, 5 Vout, 7 Aout, 0 LFM 25 °C air flow, measured using a FLIR SC300 thermal camera). Fig. 3-33 shows the recorded temperature curves of the two converters working with and without 300 LFM air flow. In the first 13 minutes, the two converters are turned on and operate without the air flow. Due to the thinner board and the reduced weight, the temperature of the MultiTrack prototype changed faster than the commercial product, but its final peak temperature was 4°C lower than that of the commercial product. A 2.4 W fan was turned on between minute 13 to minute 28, generating 300 LFM 25 °C air flow on the two converters. The air flow had significantly reduced the peak and average board temperature: the difference between the average temperatures of the two converters was not significantly changed, while the difference between the peak temperatures of the two converters was changed from 4 °C to 8 °C. This experiment demonstrates that the MultiTrack converter can better take advantage of active cooling if peak board temperature is a design requirement.

Table. 3.4 and Fig. 3-36 compares the figure-of-merits (FOM) of the MultiTrack prototype and many state-of-art commercial products under 200 LFM 25 °C air flow with 125 °C allowable device temperature[4]. The commercial products represent the best-performing

[4]This operating condition is selected as the benchmark condition because most of the commercial products

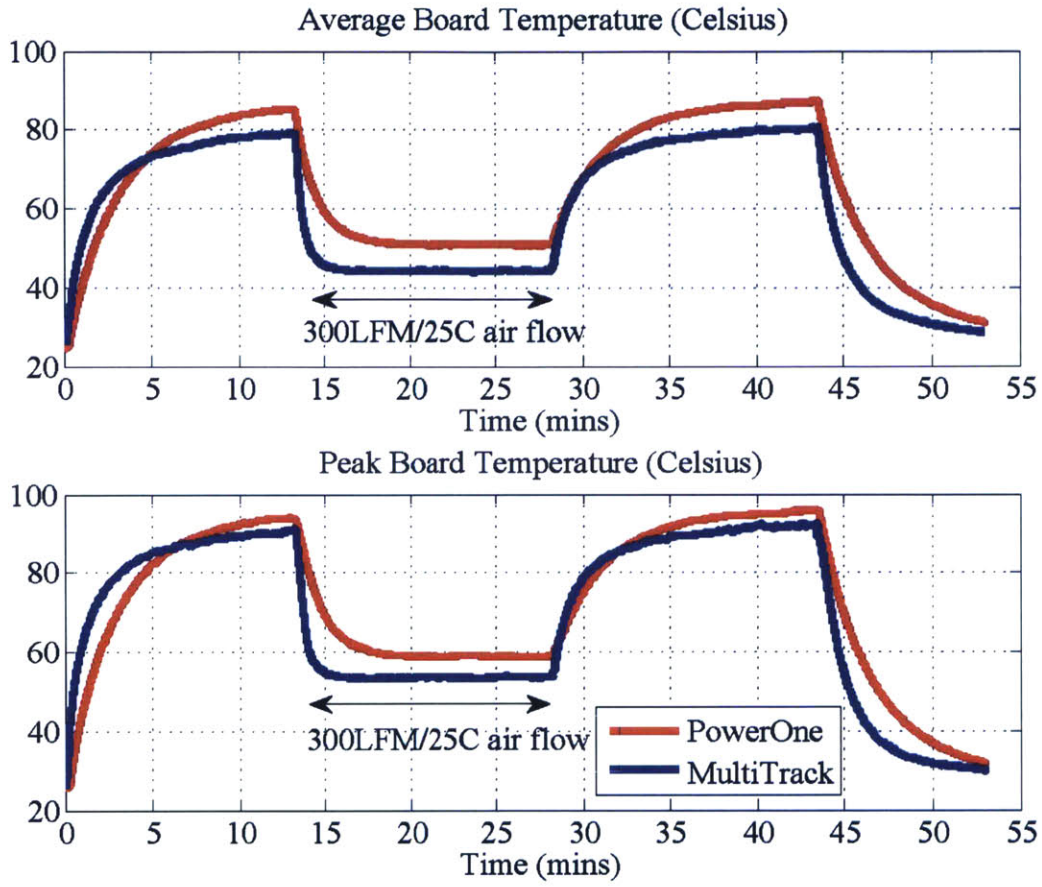


Figure 3-33: Measured (a) average board temperature and (b) peak board temperature of the MultiTrack converter and the commercial converter. Both converters are delivering 7 A from a 42 V input voltage.

ones that the authors could find having similar wide-input-range capability. All these commercial products are in 1/16 brick form factor, have Silicon devices and switch at around 200 kHz-300 kHz. As demonstrated, for wide input-voltage-range applications, by utilizing a merged multi-stage power conversion architecture, switching at higher frequency, and taking advantages of the miniaturized GaN switches, the MultiTrack converter requires reduced inductor size, component thickness and PCB thickness, and achieves 3x higher power density while maintaining comparable efficiency performance.

can meet their peak power density under this operating condition according to their datasheets.

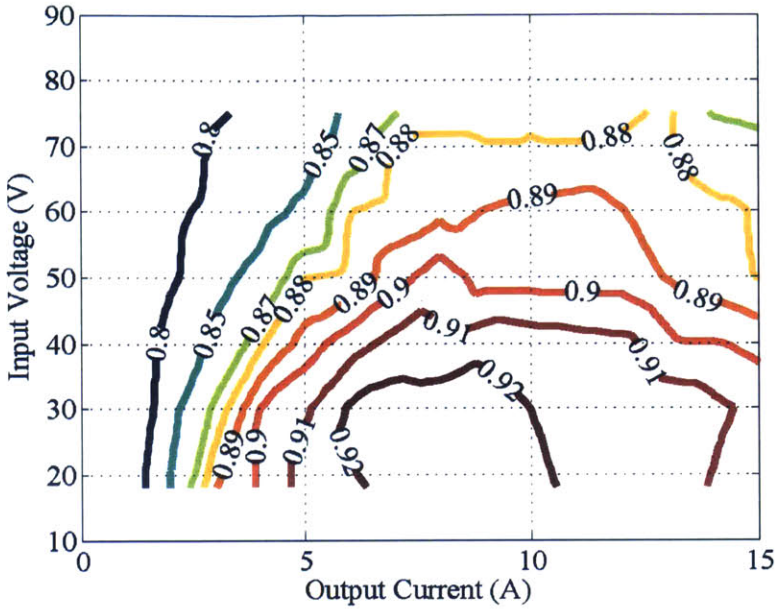


Figure 3-34: Measured efficiency of the commercial product. This efficiency is measured with 200 LFM, 25°C air flow.

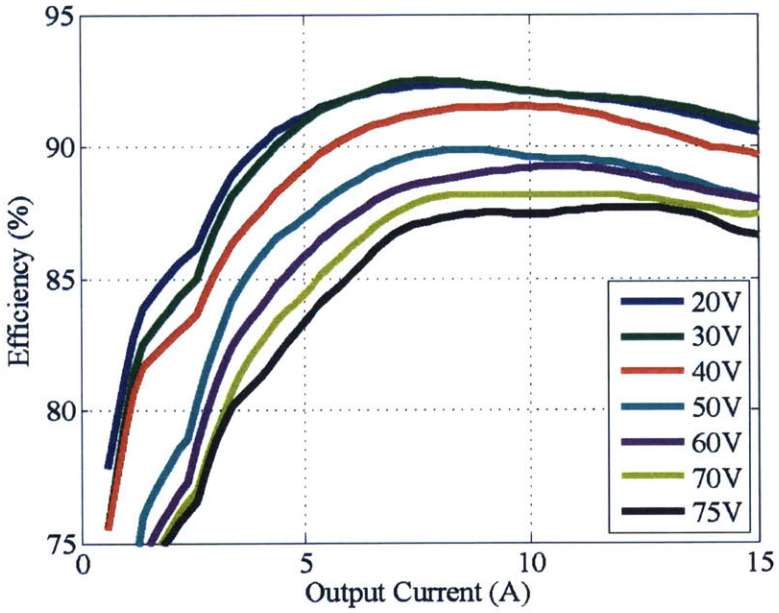


Figure 3-35: Measured efficiency of the commercial product. This efficiency is measured with 200 LFM, 25 °C air flow.

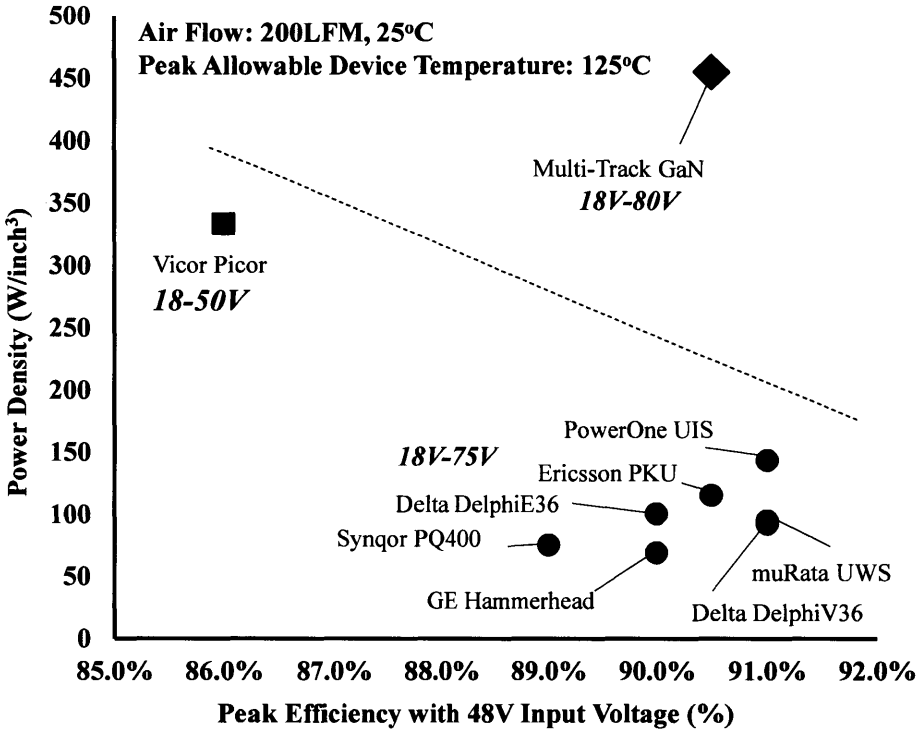


Figure 3-36: Comparing the MultiTrack converter with many state-of-art commercial products. The MultiTrack converter achieves 3x higher power density while maintaining comparable efficiency performance. The 18 V – 50 V Vicor Picor converter was also included in this comparison to demonstrate a typical power density/efficiency/voltage-conversion-range tradeoff curve.

3.8 Summary of Chapter 3

This chapter investigates the effectiveness of the merged multi-stage power conversion approach in isolated dc-dc applications with wide input-voltage range. A MultiTrack power conversion architecture which has many advantages compared to conventional power conversion architectures for applications that require isolation and wide-input-voltage range is proposed. This power conversion architecture leverages the complementary strengths of switched-inductor, switched-capacitor, and magnetic isolation circuits, and gains mutual benefits from the way they are merged together by processing power in multiple voltage domains and current channels. A prototype 18 V – 80 V input, 5 V output, 15 A, 800 kHz, 0.93 inch^2 (1/16 brick equivalent) isolated dc-dc converter was designed and tested, validating the effectiveness of the proposed widely-applicable MultiTrack design concept.

Table 3.4: Isolated Wide-Input-Voltage Range Dc-Dc Converter Performance Comparison.

Converter	V_{in}	I_{out}	Area	Height	Volume	Weight	Peak Efficiency (48 Vin)	Power Density (200 LFM)[4]	Power Density (0 LFM)[4]
PowerOne UIS	18 V–75 V	14 A	1.17 inch^2	0.42 inch	0.488 inch^3	15.3 g	90%	143.5 W/inch^3	143.5 W/inch^3@30 LFM
Ericsson PKU	18 V–75 V	10 A	1.17 inch^2	0.37 inch	0.433 inch^3	9.9 g	90.5%	115.5 W/inch^3	115.5 W/inch^3
Delta DelphiE	18 V–75V	15 A	2.07 inch^2	0.36 inch	0.752 inch^3	25 g	90%	100.6 W/inch^3	86.7 W/inch^3
Delta DelphiV	18 V–75 V	8 A	1.17 inch^2	0.37 inch	0.433 inch^3	12.1 g	91%	92.4 W/inch^3	92.4 W/inch^3
GE Hammerhead	18 V–75 V	6 A	1.17 inch^2	0.37 inch	0.433 inch^3	13 g	90%	69.3 W/inch^3	69.3 W/inch^3
Synqor PQ40050	18 V–75 V	20 A	3.34 inch^2	0.40 inch	1.324 inch^3	37.5 g	89%	75.5 W/inch^3	71.7 W/inch^3@50 LFM
muRata UWS	18 V–75 V	8 A	1.17 inch^2	0.36 inch	0.421 inch^3	13.6 g	91%	95.0 W/inch^3	95.0 W/inch^3@65 LFM
Vicor PI3109	18 V–50 V	10 A	0.56 inch^2	0.27 inch	0.150 inch^3	7.8 g	86%	333.7 W/inch^3	300.1 W/inch^3
MultiTrack[1–3]	18 V–80 V	15 A	0.93 inch^2	0.16 inch	0.149 inch^3	6.4 g	90.5%	457.3 W/inch^3	339 W/inch^3

[1] The MultiTrack prototype utilizes GaN devices. Other converters use Silicon devices.

[2] The MultiTrack prototype switches at 800 kHz. Other converters switch at 200 kHz-300 kHz.

[3] The MultiTrack prototype utilizes an off-board TI TMS320F28069 micro-controller. Other converters have their controllers on board.

[4] Power density values are listed assuming 25 °C ambient air temperature and 125 °C maximum allowable device temperature.

Chapter 4

A Systematic Approach to Modeling Planar Magnetics

Abstract

This chapter develops a systematic planar magnetics modeling approach. Magnetic components play key roles in power electronics systems, including merged switched-capacitor/magnetic converters. Merging multiple power electronics circuits through magnetic coupling is envisioned to be a promising way to realizing innovative circuitry with sophisticated coupling relationships. Among the many types of magnetic devices, planar magnetic components using printed-circuit-board (pcb) windings are attractive due to their high repeatability, good thermal performance and usefulness for realizing intricate winding patterns. To enable higher system integration at high switching frequency, more sophisticated methods that can rapidly and accurately model planar magnetics are needed.

A systematic approach to modeling impedances and current distribution in planar magnetics based on a lumped circuit model, named the *Modular Layer Model* (MLM), is developed in this chapter. Stacked pcb layers are modeled as repeating modular impedance networks, with additional modular impedances representing the magnetic core, air gaps and vias. The model captures skin and proximity effects, and enables accurate predictions of impedances, losses, stored reactive energy and current sharing among windings. The MLM can be used to simulate circuits incorporating planar magnetics, to visualize the magnetic fields, and to extract parameters for magnetic models by simulations, among many other applications. The modeling results are checked with results of previous theories and finite-element-modeling approaches, with good matching demonstrated. A group of planar magnetic devices, including transformers and inductors with various winding patterns, are prototyped and measured to validate the proposed approach and clarify the boundaries of its applicability.

This chapter demonstrates that the impedance and current distribution of a planar magnetic devices (which satisfy the MQS and 1-D assumption) can be well predicted and controlled. It can be very helpful in designing novel magnetic devices with sophisticated coupling relationships, opening up many opportunities in developing future *merged-multi-stage* power conversion circuits and systems.

4.1 Introduction to Planar Magnetics Modeling

For inductors and transformers in high-frequency power conversion applications, windings fabricated in a printed-circuit-board (pcb) process with ferrite cores assembled through holes in the board have become a popular strategy. We use the term *planar magnetics* for this approach, which offers high repeatability, good thermal performance, and ease of realizing intricate winding patterns [32–35]. These advantages makes planar magnetics attractive as switching frequencies increase [5, 31, 36]. However, the increasing skin and proximity effects and the resulting self and mutual impedances make modeling challenging, especially when parallel windings are included. Previous modeling efforts have estimated ac resistance [37, 38, 79–83], predicted parasitics [39, 84, 85], estimated core losses [86–92], extracted parameters by experimental measurements [93,94], and investigated current sharing among multiple windings [95–99]. This has been achieved through means including models using optical system analogies [100–104] and discretization-oriented methods [105–110], among other approaches. These approaches have different focuses, rely on various assumptions, and sometimes are not easy to use. Numerical methods (e.g., finite-element-modeling (FEM)) [111–114] and experimental measurements are widely applicable, but are not analytical and are time-consuming for design optimization. A systematic approach to modeling planar magnetics, which is fully analytical with low computational requirements, provides intuitive insights, and is capable of capturing many parameters under a minimized assumption setup, is needed and is the main focus of this chapter.

Models for planar magnetics commonly share two assumptions, in addition to other case-by-case assumptions. The first common assumption is the "1-D" assumption, under which the electromagnetic field and current distribution within and around the conductor change only along the thickness of the conductor (or insulator). This assumption is satisfied in many designs using high-permeability cores as discussed in detail in Section 4.7. The second assumption is the "MQS" assumption: the electromagnetic field in the planar structure satisfies the Magneto-Quasi-Static (MQS) requirements [115–119], in which the time derivative of the electric field (i.e. capacitive effect) can be decoupled from the other terms in Maxwell's equations and either neglected, or modeled separately with other specific approaches. In a majority of power electronics applications, the MQS assumption is satisfied.

The presented approach requires, and only requires, these two assumptions. The electromagnetic interactions within and among the windings of a planar structure are expressed using the MQS version of Maxwell's equations. These equations are converted into a lumped circuit model with element values explicitly determined by solutions to the magnetic diffusion equation. The lumped circuit model bridges the circuit domain and the electromagnetic domain: it allows the electromagnetic field and current distributions to be easily calculated, provides insights into the magnetic structure design, and is useful for analyzing circuits incorporating planar magnetic devices. The modeling approach is applicable to a wide variety of devices, from inductors and coupled inductors to multiple-winding transformers incorporating interleaving among windings, paralleled windings and energy storage (e.g., for flyback transformers). The single frequency (fundamental harmonic) behaviors of this lumped circuit model can be rapidly solved by circuit simulators (e.g., SPICE). With some modifications, the lumped circuit is also capable of accurately capturing wide-band operation, such as for use in time-domain simulations with many harmonic components. The proposed approach can be applied to various electromagnetic systems, from windings in planar transformers to windings in electric machines.

This chapter is organized as follows. Section 4.2 outlines the terminology used in the model, and presents an overview of the proposed approach. A step-by-step derivation of the lumped circuit model is provided in Section 4.3. Section 4.4 explains how the lumped circuit model can be applied to circuit simulations, field visualizations and parameter/impedance extractions. The proposed approach is verified through FEM simulations and experimental measurements in Section 4.6. Section 4.7 presents the boundaries of applicability of the model, investigates a few practical design constraints, and quantitatively shows the performance of this approach under these constraints. Finally, Section 4.8 summarizes this chapter. Extended derivation of the lumped circuit model and theoretical verifications are provided in Appendix C.

4.2 Overview of the Approach

The terminology used in this chapter is illustrated in Fig. 4-1. A planar magnetic structure comprises a *winding stack*, a *magnetic core*, and a set of possible *air gaps*. A winding stack has one or more *windings*. Each winding comprises one or more turns on one or

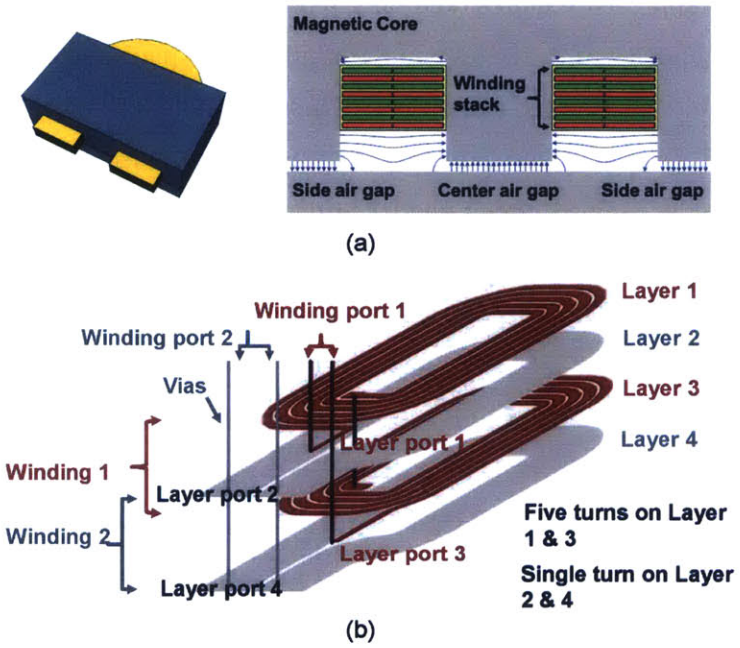


Figure 4-1: (a) Cross-sectional view of a planar magnetic structure. It comprises a magnetic core, a winding stack and a set of possible air gaps. (b) Winding stack of an example two-winding, four-layer transformer with 10:1 turns ratio.

more *layers*. Each layer can have multiple *turns*. Usually, turns on the same layer are connected in series. Each layer has a *layer port*. Layer ports are connected by *electrical vias* to form windings. Turns on different layers can be connected in series or parallel, and can be interleaved in various ways. An example winding stack with two windings and a 10:1 primary-to-secondary turns ratio is shown in Fig. 4-1b. It has four layers: layer 1 and layer 3 have five turns each and are connected in series; layer 2 and layer 4 have a single turn each and are connected in parallel.

The proposed approach is developed based on a lumped circuit model - named the *Modular Layer Model (*MLM) - which utilizes repeating modular impedance networks to represent stacked pcb layers (or other layer stacks). The concept of using modular networks to model magnetic iterations among multiple layers of windings is not new. Here we highlight two branches of related work to provide the background and clarify the commonalities and differences between the MLM introduced here and other existing circuit models.

Keradec and colleagues modeled multilayer windings in a magnetic component by adapting models for electromagnetic waves propagating in multi-layered media, as is sometimes

found in optical systems [100–104]. Analogies are made between the circuit domain and the optical domain. This model is simple, analytical and intuitive. However, it requires unwieldy assumptions for the cross-discipline analogies to be fully satisfied. Additional analogies are needed to make the model compatible to other existing models, and/or applicable to more sophisticated cases. Additional analogies, variable matchings and unit-conversions are required to compare, verify and extend this approach. Nevertheless, this set of papers introduces a very valuable analytical framework for mapping electromagnetic relationships among layers into connections of three-port circuit blocks, an approach we also adopt.

Lopera and colleagues also developed computational models to capture the behavior of magnetic components comprising electromagnetic fields diffusing through multilayer magnetic windings [105–110]. Each layer is discretized into multiple small units. Each unit is represented by a lossy transmission line model. Multiple transmission-line structures are interconnected to model the whole magnetic component. The behavior of the resulting system is found using numerical methods (e.g., with a circuit simulator), essentially placing the burden of solving for the propagation of the magnetic fields onto the circuit simulator. This branch of approaches also uses repeating impedance networks to analytically represent layers, but is more similar to finite-element-modeling because each conductor layer is further discretized. The accuracy of the model depends on the discretization resolution. Empirical design rules are required to choose the appropriate discretization resolution that balances the model complexity and accuracy [109]. The other disadvantage of discretization is that the dependence of the device impedance on the geometry parameters cannot be explicitly expressed using equations. Because the burden of computing the magnetic response (e.g., diffusion of magnetic fields into conductors and the resulting behavior in the electrical domain) is placed on the circuit simulator, extensive computational resources may be required. An analytical solution would also be especially desirable for situations where large numbers of cases must be run (e.g., as when optimizing winding structures). Nevertheless, discretization enables these group of techniques to be used to capture 2-D cases [107], which is an unique advantage compared to 1-D analytical methods. Another unique, and very useful characteristic of this approach is that its impedance values in the model are not frequency dependent [105].

The proposed approach takes on the advantages of each of the above-described models: 1) It is developed directly from basic electromagnetic theory, which allows it to be easily

interpreted and rapidly implemented; 2) It relies on very few assumptions, thus allows us to study the applicability and limitations of this "1-D" and "MQS" analysis framework with minimum constraints, and to further expand the model; 3) It provides analytical solutions for the magnetic fields and resulting electrical characteristics, provides clear design guidelines and minimizes computational requirements and time; 4) It reexamines many aspects of modeling planar magnetics under a unified set of assumptions, and reveals the underlying connections among many existing approaches. Moreover, we provide clear, validated guidelines for where the underlying modeling assumptions hold, including estimates of the degree of error incurred by adopting them, making the approach highly useful in practice. The approach is presented with a focus on emphasizing the physical nature of its analysis framework, while retaining its theoretical integrity, implementation simplicity, modification flexibility and application generality.

4.3 Generating the Lumped Circuit Model

The development of the lumped circuit model begins by deriving a modular impedance network for a single turn on a layer (referred to here as a *one-turn layer*) having analytically-derived parameters. This modular network is repeated and extended to model multiple layers with multiple turns. The magnetic core, the air gaps and the cross-layer connections (electrical vias) place additional boundary conditions on the impedance networks, and are modeled by additional components in the lumped circuit model. To make the model compatible with circuit analysis, linear conversions (ideal transformers) and electrical interconnects are used to link the electromagnetic domain to the circuit domain.

4.3.1 Modeling a one-turn layer.

Fig. 4-2a shows the geometry of a one-turn layer (e.g. one layer in an E core), with length $\boldsymbol{d}$, width $\boldsymbol{w}$, and thickness $\boldsymbol{h}$. This single turn carries a current $\boldsymbol{I}$ (having current density $\boldsymbol{J}$ with units "A/m^2" pointing towards the *y-axis*, and integrated surface current density, current per width $\boldsymbol{K}$ with units "A/m" distributed along the *x-axis*). This current induces a voltage $\boldsymbol{V}$ across its two terminals. $H_T|H_B$ is the magnetic field ($\boldsymbol{H}$ field) strength on the top|bottom surface of the layer (along the width). $E_T|E_B$ is the electric field ($\boldsymbol{E}$ field) strength on the top|bottom surface of the layer (along the length). As derived in

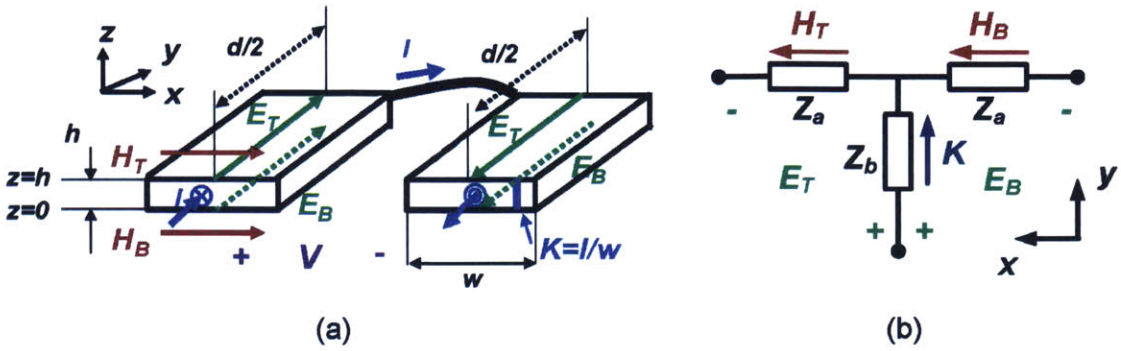


Figure 4-2: (a) A one-turn layer and (b) its three-terminal impedance network. The positive directions of all variables (H, E, I, V, K, etc) used in this chapter are referred to the x-y-z axes shown in this figure. A positive $E|H$ field in the physical structure is represented by a positive $E|H$ value in the impedance network. The two conductors form a single turn and are connected by a interconnect wire whose impedance is neglected. This one-turn layer is modeled as a three terminal impedance network.

Appendix C.1.1, solving the 1-D diffusion equation in the conductor under MQS conditions, with the specified boundary conditions [116], and applying *Ohm's Law* (J=σE; where σ is the conductivity of this conductor) gives the relationship between the magnetic fields and electric fields on the top and bottom surfaces, and the integrated surface current density K carried by this layer:

$$\begin{aligned} E_T &= Z_a\ H_T + Z_b\ K \\ \underbrace{E_B}_{\text{V/m}} &= \underbrace{Z_b}_{\Omega}\ \underbrace{K}_{\text{A/m}} - \underbrace{Z_a}_{\Omega}\ \underbrace{H_B}_{A/m}. \end{aligned} \tag{4.1}$$

Here Z_a and Z_b are two complex impedances (with units of Ω) explicitly determined by the geometry of the structure and the operating angular frequency (ω), and are given by

$$\begin{aligned} Z_a &= \frac{\Psi(1-e^{-\Psi h})}{\sigma(1+e^{-\Psi h})} \\ Z_b &= \frac{2\Psi e^{-\Psi h}}{\sigma(1-e^{-2\Psi h})}. \end{aligned} \tag{4.2}$$

Here $\Psi = \frac{1+j}{\delta}$, where $\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$ is the skin depth of the conductor and μ is its permeability. Also, H_T, H_B, I and K are related through *Ampere's Law*:

$$(H_T - H_B)w = I = Kw. \tag{4.3}$$

All variables (E, H, V, I, Z, etc.) are complex variables. Since H_T, H_B, and K are related to current (units: A/m), E_T and E_B are related to voltage (unit: V/m), and Z_a and Z_b are impedances (unit: Ω), Eq. (4.1) and (4.3) can be considered as the *Kirchhoff's Voltage Law* (KVL) and *Kirchhoff's Current Law* (KCL) determining a three-terminal impedance network, as shown in Fig. 4-2b, with impedance values calculated with (4.2). A related circuit configuration can be found in [100]. Compared to Keradec's derivation, our derivation is self-consistent without making cross-discipline analogies. Variables and relationships have circuit domain definitions, representing different field-to-circuit mapping relationships. For example, the E field in our derivation is the actual physical electric field commonly used in magnetic modeling (i.e. $E = V/d$). While in Keradec's derivation, optical wave propagation concepts such as "electrostatic field" and "induced electric field" were borrowed.

4.3.2 Modeling two adjacent layers.

Figure 4-3a shows the geometry of two adjacent one-turn layers separated by a spacing (created with an insulator) between them. Based on the previous derivation, the electromagnetic fields around and within each layer can be described by the following two sets of equations

$$\begin{array}{ll} \text{Layer 1:} & \text{Layer 2:} \\ \begin{cases} E_{T1} = Z_{a1}H_{T1} + Z_{b1}K_1 \\ E_{B1} = Z_{b1}K_1 - Z_{a1}H_{B1} \\ H_{T1} - H_{B1} = K_1 \\ wK_1 = I_1. \end{cases} & \begin{cases} E_{T2} = Z_{a2}H_{T2} + Z_{b2}K_2 \\ E_{B2} = Z_{b2}K_2 - Z_{a2}H_{B2} \\ H_{T2} - H_{B2} = K_2 \\ wK_2 = I_2. \end{cases} \end{array} \tag{4.4}$$

Here $H_{Ti}|H_{Bi}$ is the magnetic field strength on the top|bottom surface of the layer i; $E_{Ti}|E_{Bi}$ is the electric field strength on the top|bottom surface of layer i; Z_{ai} and Z_{bi} are complex impedances of layer i defined by the geometry and frequency; I_i is the current that is carried by layer i. Based on (4.4), layer 1 and layer 2 can be represented by two modular impedance networks labeled as "Layer 1" and "Layer 2" in Fig. 4-3b. Also labeled are the associated electromagnetic field variables on the top and bottom surfaces of each layer.

The electromagnetic fields surrounding the two layers are related by the magnetic flux flowing in the spacing between them (Φ_{S12}). The spacing has a thickness a_1, width w and length d. From flux continuity, the magnetic field strength in the spacing, H_{S12}, equals

H_{B1} and H_{T2}. Considering the voltage loops on the bottom surface of layer 1, and on the top surface of layer 2 (including layer surfaces, external wires and sources surrounding the center post), and using *Faraday's Law* and flux continuity (as shown in Appendix C.1.2), the magnetic flux flowing through the center post across the two surfaces, Φ_{B1} and Φ_{T2}, can be written as functions of the electric fields on the two layer surfaces (E_{B1}, E_{T2}), as well as the external voltages applied to the two layer ports (V_1 and V_2), such that

$$\begin{cases} j\omega\Phi_{B1} = V_1 - dE_{B1} \\ j\omega\Phi_{T2} = V_2 - dE_{T2} \\ \Phi_{B1} + \Phi_{S12} = \Phi_{T2} \\ H_{S12} = \frac{\Phi_{S12}}{\mu_0 a_1 d}. \end{cases} \tag{4.5}$$

Here the permeability of the space (insulator) between the two layers is assumed to be μ_0. Thus, the magnetic field in the spacing, H_{S12}, can be expressed as

$$H_{S12} = \frac{1}{j\omega\mu_0 a_1}\left(\frac{V_2}{d} - E_{T2} - \frac{V_1}{d} + E_{B1}\right). \tag{4.6}$$

Defining $Z_{S1} = j\omega\mu_0 a_1$ gives

$$\underbrace{H_{S12}}_{\text{A/m}}\underbrace{Z_{S1}}_{\Omega} = \underbrace{\frac{V_2}{d} - E_{T2} - \frac{V_1}{d} + E_{B1}}_{\text{V/m}}. \tag{4.7}$$

Eq. (4.7) is an important KVL relation that links the two impedance networks. The resulting lumped circuit model for two adjacent layers is shown in Fig. 4-3b. Note that the integrated surface current densities, K_1 and K_2, need to be linearly converted into external layer currents $I_1 = wK_1$ and $I_2 = wK_2$. These linear conversions are modeled with current-dependent-current-sources (CDCS) with gains of w (layer width). According to Eq. (4.7), linear conversions are also required to convert the induced layer port voltages V_1 and V_2 to electric fields $\frac{V_1}{d}$ and $\frac{V_2}{d}$. These linear conversions are modeled with voltage-dependent-voltage-sources (VDVS) with gains of $\frac{1}{d}$. These VDVSs and CDCSs are paired up for each layer and labeled as "layer ports" in Fig. 4-3b.

The modeling of the layer port becomes simpler and more straight-forward if we consider a general case when there are multiple series-connected (concentric) turns on one or many layers. Figure 4-4a shows an example setup with layer 1 having two series-connected turns, and layer 2 having a single turn. In a general case, assume layer i has m_i turns, and all

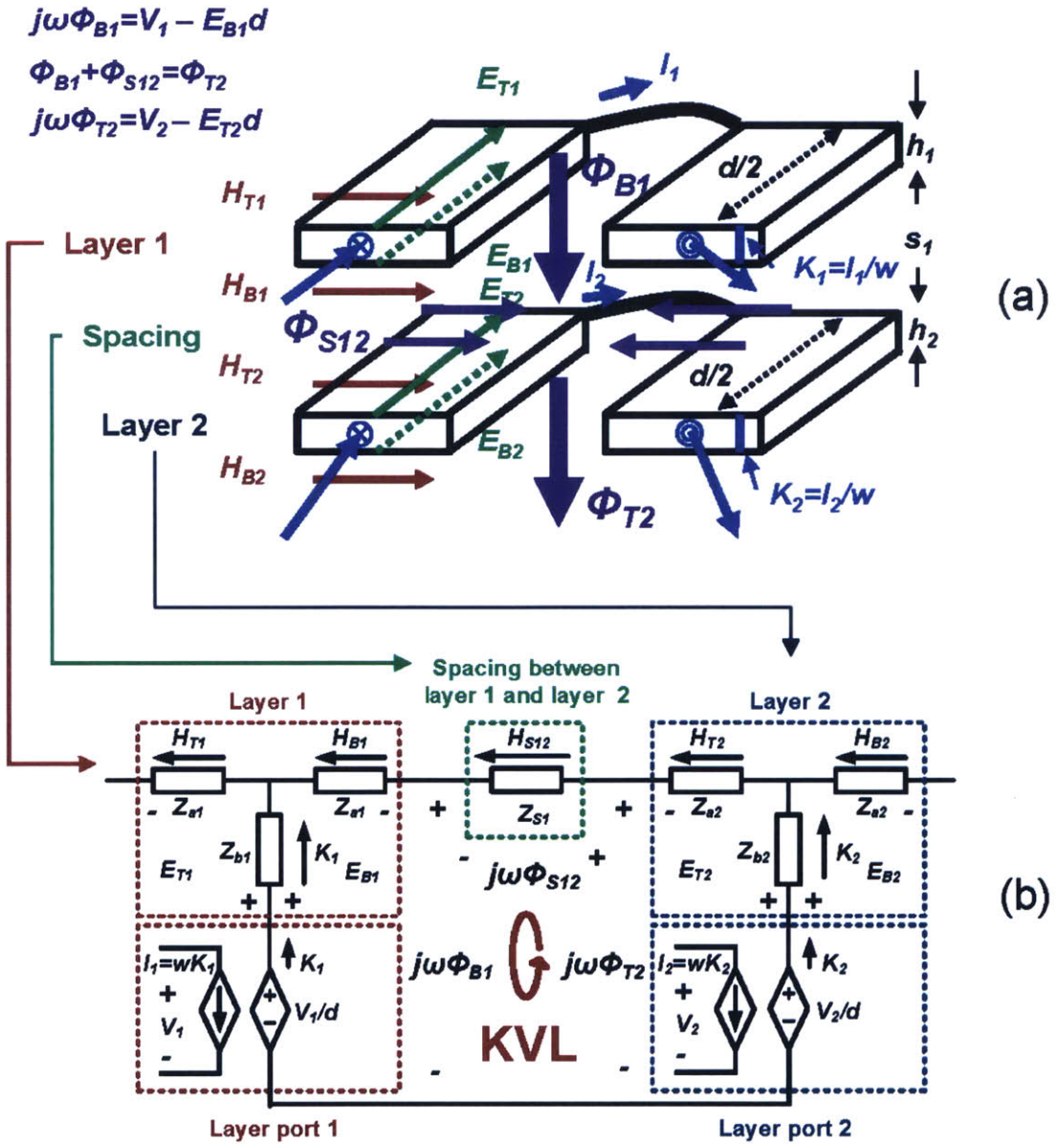


Figure 4-3: Two one-turn adjacent layers: (a) planar geometry and (b) impedance network model with "V/m", "A/m" and "Ω" as the internal units. The variables on one side of the dependent sources are H, E and K. They are in the electromagnetic domain. The variables on the other side of the dependent sources are voltages and currents. They are in the circuit domain.

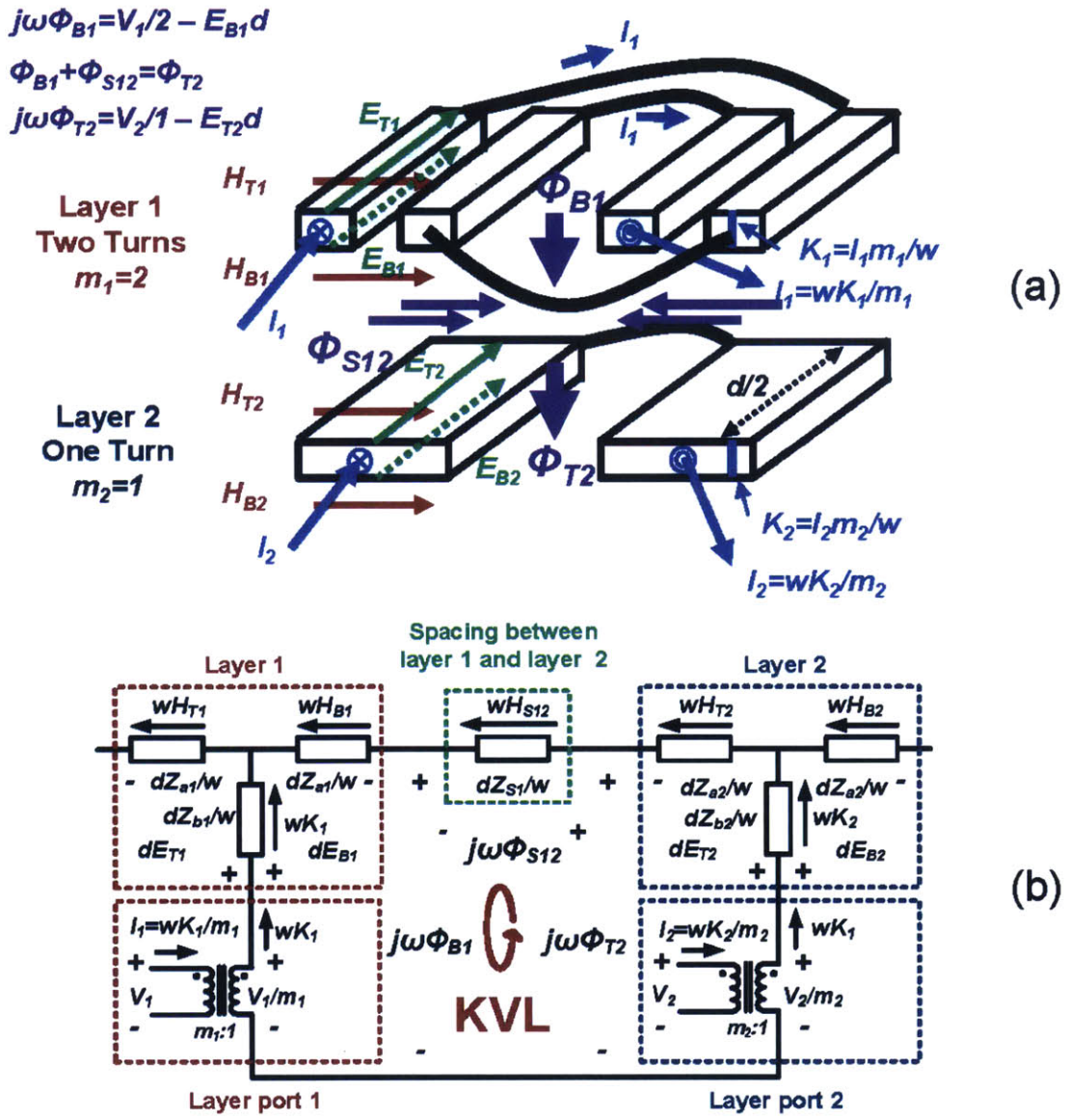


Figure 4-4: Two adjacent layers - layer 1 has two series-connected turns ($m_1 = 2$), and layer 2 has a single turn ($m_2 = 1$): (a) planar geometry and (b) impedance network model with "V", "A", and "Ω" as the internal units. This system is entirely in the circuit domain. The circuit architecture is determined by using Maxwell's equations as KVL and KCL rules. The complex impedances are determined by solutions to 1-D diffusion equation under MQS conditions.

turns have the same width - $\frac{w}{m_i}$, thickness - h_i and length - d. H_{Ti}, H_{Bi} and K_i are linearly related to I_i: $I_i = \frac{wK_i}{m_i} = \frac{w(H_{Ti}-H_{Bi})}{m_i}$. Also the Φ_i on the top|bottom surfaces of layer i is linearly related to E_i and V_i on the top|bottom surfaces: $j\omega\Phi_i = \frac{V_i}{m_i} - dE_i$. Eq. (4.4) and (4.7), which were developed for single-turn layers and were represented with the circuit of Fig. 4-3b, generalize to the following set of equations including m_1 and m_2 as parameters:

$$
\begin{aligned}
&\text{Layer 1}: \begin{cases} \underbrace{dE_{T1}}_{\text{V}} = \underbrace{wH_{T1}}_{\text{A}}\underbrace{\frac{d}{w}Z_{a1}}_{\Omega} + \underbrace{wK_1}_{\text{A}}\underbrace{\frac{d}{w}Z_{b1}}_{\Omega} \\ dE_{B1} = wK_1\frac{d}{w}Z_{b1} - wH_{B1}\frac{d}{w}Z_{a1} \\ H_{T1} - H_{B1} = K_1 \\ wK_1 = I_1 m_1. \end{cases} \\
&\text{Layer 2}: \begin{cases} dE_{T2} = wH_{T2}\frac{d}{w}Z_{a2} + wK_2\frac{d}{w}Z_{b2} \\ dE_{B2} = wK_2\frac{d}{w}Z_{b2} - wH_{B2}\frac{d}{w}Z_{a2} \\ H_{T2} - H_{B2} = K_2 \\ wK_2 = I_2 m_2. \end{cases} \\
&\text{Spacing}: \underbrace{\frac{V_2}{m_2} - dE_{T2} - \frac{V_1}{m_1} + dE_{B1}}_{\text{V}} = \underbrace{wH_{S12}}_{\text{A}}\underbrace{\frac{d}{w}Z_{S1}}_{\Omega}.
\end{aligned}
\tag{4.8}
$$

This reorganized equations has individual terms having circuit domain units ("V", "A", "Ω"). It can be represented by a lumped circuit model as shown in Fig. 4-4b. By linearly scaling all impedances with a geometry factor $\frac{d}{w}$, all dependent sources (VDVSs and CDCSs) can be replaced by ideal transformers[1] with turns ratios of m_1 and m_2, directly representing the numbers of physical turns on each layer. With these linear conversions[2], all variables in Fig. 4-4b are entirely in the circuit domain.

[1]This "ideal-transformer" configuration is also utilized in [100] and [105]. However, we rigorously derived it using Maxwell's equations (to provide a proof and to avoid using vague analogy/assumptions), and took this opportunity to convert all variables back to the circuit domain. Presenting all variables in the circuit domain allows the magnetic device integrally analyzed and interpreted with external circuits under a unified system setup (e.g. the current distribution can be directly measured in SPICE simulations). Linear conversions after simulations/computations are avoided. This modeling approach also results in a physical, rational ideal transformer turns ratio that intuitively represents the number of physical turns.

[2]A more intuitive way to interpret these linear relationships is to consider the m_i turns as a single turn having equivalent total width, with its current multiplied by m_i, and its voltage divided by m_i. An ideal transformer with turns ratio of m_i:1 naturally reflects these linear relationships. This interpretation is an additional analogy, but it doesn't require additional assumption because small spacings between adjacent turns are implicitly assumed when utilizing the "1-D" assumption. The presented derivation of Eq. (4.8) is a strict theoretical proof for this analogy. As will be experimentally investigated in Section 4.7, small spacings between adjacent turns on the same layer are required. The relative size of these spacings are usually constrained by pcb manufacturing capability and insulation requirements.

4.3.3 Modeling the magnetic core and the air gaps

Consider a planar structure with n layers, one magnetic core and two air gaps as shown in Fig. 4-5. The number of series-connected turns on layer 1 to layer n are m_1 to m_n, respectively. The core has a gap of length g_1 in the outer legs, and a gap of length g_2 in the center post (the total gap length is $g_1 + g_2$). The cross sectional area of the air gap in the center post is A_c and that of the outer surfaces are $\frac{A_c}{2}$. The thicknesses of layers 1 to n are h_1 to h_n, respectively. The spacing thickness between layer i and layer $(i+1)$ is a_i. The spacing thickness between the top surface of layer 1 and the magnetic core is b_t. The spacing thickness between the bottom surface of layer n and the magnetic core is b_b. The thickness of the top side of the core is c_t; the thickness of the bottom side of the core is c_b. The magnetic field strength on the top|bottom surface of the layer i is $H_{Ti}|H_{Bi}$. The electric field strength on the top|bottom surface of layer i is $E_{Ti}|E_{Bi}$. The magnetic flux flowing through the center post across the top|bottom surfaces of layer i is Φ_{Ti} and Φ_{Bi}. The currents that flow through layers 1 to n are I_1 to I_n. The induced voltages of layers 1 to n are V_1 to V_n. The reluctance of the top side of the core is $\mathcal{R}_T$, carrying magnetic flux Φ_T. The reluctance of the bottom side of the core and the air gap is $\mathcal{R}_B$, carrying magnetic flux Φ_B. Note that $\mathcal{R}_T$ and $\mathcal{R}_B$ include the reluctances of the spacings (between the winding stack and the core) and the magnetic core itself. As shown in Fig. 4-5, Φ_{T1} and Φ_{B1} are the summations of the flux carried by the spacings and the magnetic core ($\Phi_{T1} = \Phi_{ts} + \Phi_T$, $\Phi_{Bn} = \Phi_B - \Phi_{bs}$).

We investigate how to rigorously represent these variables and their relationships in the lumped circuit model. The lumped model for the n conductor layers, and the n-1 spacings among them can be generated by simply repeating the modular network of each layer and spacings between two conductor layers (simply extending Fig. 4-4b). The magnetic core and the air gaps impose additional boundary conditions, and hence add additional circuit elements. Derived from the magnetic reluctance circuit model as shown in Appendix C.1.3, variables on the top and bottom of the layer stack (E, V, and H) are related by the reluctances of the top and bottom side of the core ($\mathcal{R}_T$ and $\mathcal{R}_B$):

$$\begin{aligned} dE_{T1} - \frac{V_1}{m_1} &= -\frac{j\omega}{\mathcal{R}_T} w H_{T1} \\ dE_{Bn} - \frac{V_n}{m_n} &= \frac{j\omega}{\mathcal{R}_B} w H_{Bn}. \end{aligned} \tag{4.9}$$

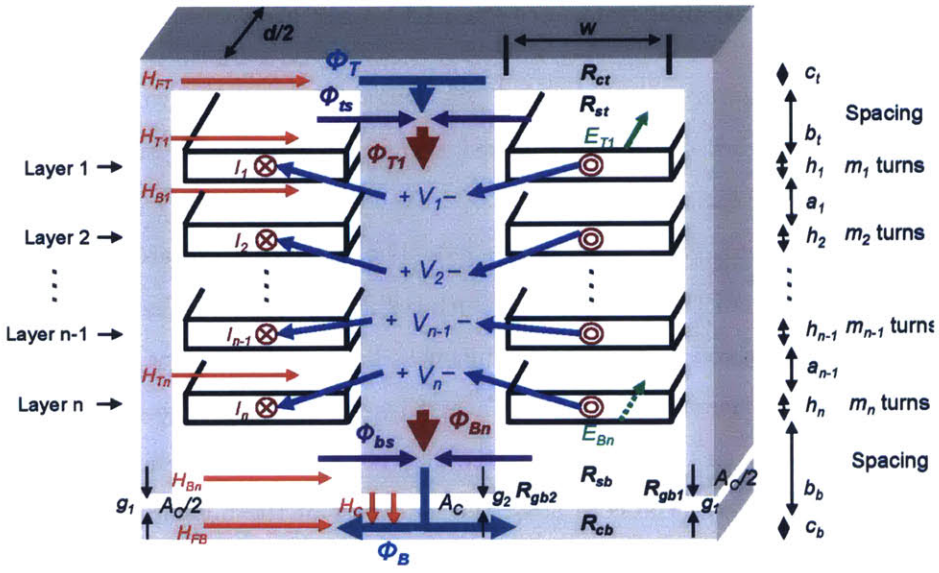


Figure 4-5: Planar structure with n layers, a magnetic core and multiple air gaps, with $g_1 + g_2$ as the total gap length. All layers are drawn as one-turn layers for simplicity. In a general case, layer 1 to layer n have m_1 to m_n series-connected turns. All layers usually have the same length d (determined by the core length) and width w (determined by the window width).

We define two impedances:

$$\begin{aligned} Z_T &= j\omega/\mathcal{R}_T \\ Z_B &= j\omega/\mathcal{R}_B. \end{aligned} \tag{4.10}$$

Eq. (4.9) can be rewritten as

$$\begin{aligned} dE_{T1} - \frac{V_1}{m_1} &= -wH_{T1}Z_T \\ dE_{Bn} - \frac{V_n}{m_n} &= wH_{Bn}Z_B. \end{aligned} \tag{4.11}$$

As KVL rules, Eq. (4.11) places Z_T and Z_B on the left and right side of the lumped circuit model as shown in Fig. 4-6. $\mathcal{R}_T$ and $\mathcal{R}_B$ can be calculated as the series/parallel combination of any gap reluctances $\mathcal{R}_{gt}$ and $\mathcal{R}_{gb}$, the core reluctances $\mathcal{R}_{ct}$ and $\mathcal{R}_{cb}$, and the shunt reluctances of the spacings between the winding and the core, $\mathcal{R}_{st}$ and $\mathcal{R}_{sb}$:

$$\begin{aligned} \mathcal{R}_T &= (\mathcal{R}_{ct} + \mathcal{R}_{gt}) \parallel \mathcal{R}_{st} \\ \mathcal{R}_B &= (\underbrace{\mathcal{R}_{cb}}_{core} + \underbrace{\mathcal{R}_{gb}}_{gap}) \parallel \underbrace{\mathcal{R}_{sb}}_{spacing}. \end{aligned} \tag{4.12}$$

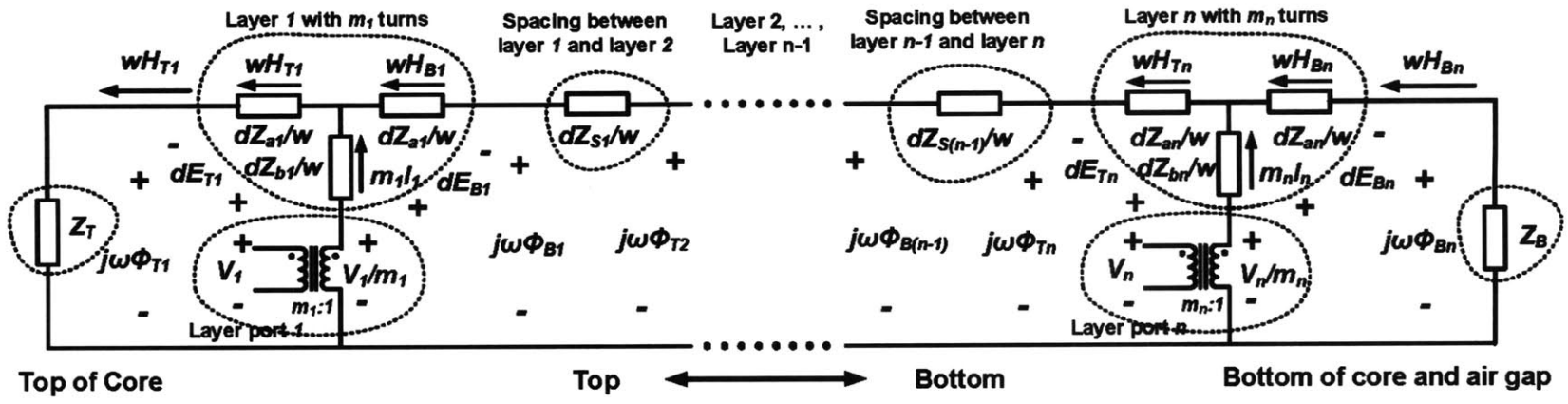


Figure 4-6: Lumped circuit model for a planar magnetic structure with n windings, a magnetic core and multiple air gaps as shown in Fig. 4-5. The n layers from top to bottom in the physical geometry are mapped one-to-one to the n modular impedance networks from left to right in the lumped circuit model. The additional constraints brought by the top and bottom magnetic core and air gaps place additional impedances (Z_T and Z_B) on the left and right sides of the n modular impedance networks.

Note that reluctances of the vertical core legs are neglected, based on the assumption of a high permeability core and/or short lengths of these legs in a planar core shape. For un-gapped structures, gap reluctances, $\mathcal{R}_{gt}$ and $\mathcal{R}_{gb}$, are zero, leaving only core reluctances. The reluctance of a short gap, that is, a gap with of length g much smaller than the lateral dimensions of the gap, can be approximated by $\mathcal{R}_g \approx \frac{g}{\mu_0 A_c}$. For longer gaps and arbitrary gap distribution, 2-D or 3-D reluctance calculations considering fringing effects, such as those in [120–124] should be used. If there are multiple gaps at the top or bottom, $\mathcal{R}_{gt}$ and $\mathcal{R}_{gb}$ are the sums of the reluctances at top and bottom, respectively. For example, in Fig. 4-5, there is no core gap on the top side, so $\mathcal{R}_{gt}$ equals zero. $\mathcal{R}_{gb}$ is the sum of the reluctances of the two gaps at the bottom center and bottom sides ($\mathcal{R}_{gb}$=$\mathcal{R}_{gb2}$+$\mathcal{R}_{gb1}$/2).

Note the underlying connections between the modular layer model (focus on the windings), and conventional magnetic reluctance circuit models (focus on cores). As derived in Appendix C.1.3, if we ignore Z_as, Z_bs and Z_Ss, and only consider Z_T and Z_B and the layer ports, the lumped circuit model shown in Fig. 4-6 is equivalent to a topological dual of a conventional magnetic reluctance circuit model [117–119]. The inclusion of Z_as, Z_bs and Z_Ss automatically capture the self-impedance, the mutual impedance, and the skin- and proximity-effects. The modeling of the winding and the core are rigorously integrated in a unified setup.

The KVL and KCL rules of the circuit shown in Fig. 4-6 is interchangeable with the electromagnetic constraints imposed by the MQS version of Maxwell's equations. All impedances are calculated explicitly with formulas using the geometry of the planar structure and the operating frequency. All parameters (m_i, d, w, h_i, etc.) have clear physical meanings. All physical variables (V_i, I_i, wH_{Bi}, wH_{Ti}, Φ_{Ti}, Φ_{Bi}, etc.) are mapped one-to-one with across and through variables (voltages and currents) in the circuit model and can be found by circuit analysis. All units are compatible with electrical circuit analysis methods (measured in "V", "A" and "Ω"). Since the model is rigorously derived based on the 1-D and MQS assumption without using additional analogies/assumptions, the modeling of each element of the system are strictly compatible with other existing techniques specified for each individual element. For example, resistances in shunt with Z_Ts and Z_Bs, calculated using conventional core loss estimation approach, can be included to capture the core loss and its impacts on winding loss.

4.3.4 Modeling cross-layer connections

In a pcb magnetics with many turns, multiple layers are usually connected by cross-layer connections (electrical vias) in series or parallel to form complete windings. Layers of different windings can be interleaved in multiple ways. These electrical vias brings additional constraints, and can be realized by connecting the corresponding layer ports in the same pattern as they are connected in the physical circuit. For example, consider the case where layer i and layer j are connected in series to form winding a, driven by voltage V_a and carrying current I_a, and layer k and layer l are connected in parallel to form winding b, driven by voltage V_b and carrying net current I_b. The following four KCL or KVL constraints

$$\begin{cases} V_i + V_j = V_a \\ V_k = V_l = V_b \\ I_i = I_j = I_a \\ I_k + I_l = I_b. \end{cases} \tag{4.13}$$

are added to the existing Maxwell's equations (i.e. (4.8) and (4.11)). These constraints can be naturally included in the lumped circuit model by connecting the layer ports of layer i and layer j in series, and connecting the layer ports of layer k and layer l in parallel, as shown in Fig. 4-7.

Note that this treatment does not include the impedances of the cross-layer interconnects and inter-winding capacitances. Without making additional assumptions/approximations (that may violate the "1-D" or "MQS" assumption), these effects can not be rigorously included under this analysis framework, and thus are beyond the capability of this lumped circuit model. In many designs, the cross-layer interconnects and capacitances can be approximated by isolating the electro-quasi-static (EQS) and magneto-quasi-static (MQS) characteristics [116], and thus be modeled as additional impedances that are not mutually correlated with those already modeled impedances. A few example place holders for impedances of the interconnects (Z_{cnt1}, Z_{cnt2}), vias (Z_{via}), and cross-layer capacitances (C_{ij}, C_{jk}, etc.) are shown in Fig. 4-7. Classic impedance calculation methods in radio-frequency (RF) engineering [78] and power electronics [125] can be utilized to find approximate values of these impedances. This treatment is generally applicable in power electronics applications, while specific accuracy/limitations require case-by-case evaluation.

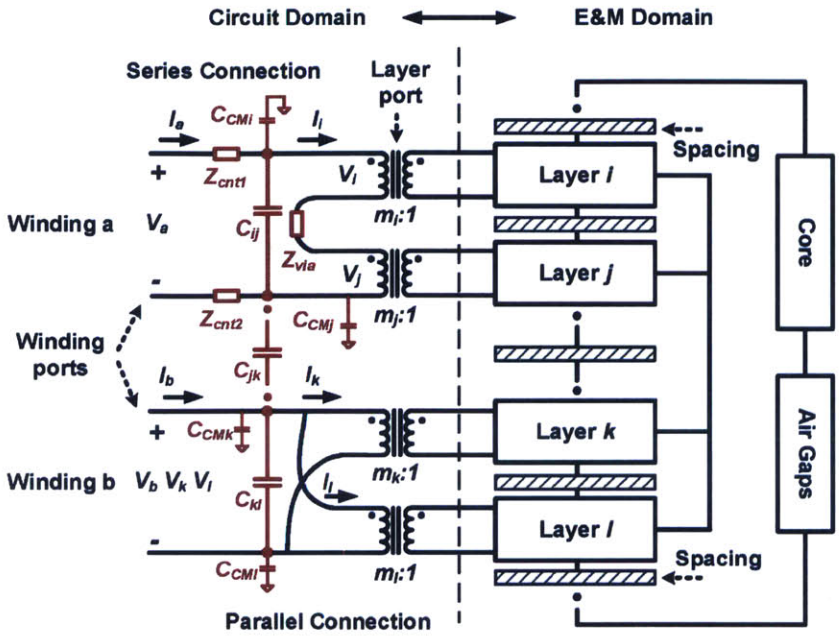


Figure 4-7: Model showing cross-layer connections (electrical vias) of the layer ports to formulate windings. Layers i and j are connected in series, and layers k and l are connected in parallel. Modular impedance networks are drawn as blocks. A few example places holders for modeling the impedances of the interconnects (z_{ts1}, z_{ts2}), vias (z_{via}), and parasitic capacitances (common-mode, differential-mode) are also shown. The interconnect impedances and parasitic capacitance values can be estimated using techniques such as those developed in [78, 125].

4.3.5 Summary of the lumped circuit model

The generation of the lumped circuit model can be summarized as a step-by-step procedure. All variables are the same as previously defined.

Conductor layers

Each conductor layer i is modeled as a three-terminal impedance network comprising two "horizontal" impedances $\frac{d}{w}Z_{ai}$ and one "vertical" impedance $\frac{d}{w}Z_{bi}$. The values of Z_{ai} and Z_{bi} are determined by the thickness (h_i) of this layer, parameters of the conductive material (μ_i, σ_i), the angular operating frequency (ω), $\Psi_i = \frac{1+j}{\delta_i}$, and $\delta_i = \sqrt{\frac{2}{\omega\mu_i\sigma_i}}$, according to

$$\begin{aligned} Z_{ai} &= \frac{\Psi_i(1-e^{-\Psi_i h_i})}{\sigma_i(1+e^{-\Psi_i h_i})} \\ Z_{bi} &= \frac{2\Psi_i e^{-\Psi_i h_i}}{\sigma_i(1-e^{-2\Psi_i h_i})}. \end{aligned} \tag{4.14}$$

The geometry factor of $\frac{d}{w}$ is applied to Z_{ai} and Z_{bi} to bring the results into the circuit domain. Under the 1-D assumption, all layers can be approximated to have the same effective length d and total width w, although they may have different numbers of series-connected turns (m_i). The clearances between two adjacent turns on the same layer, and between the conductor and the ferrite core should be minimized. The impacts of these clearances are investigated in Section 4.7.2.

Layer ports

Each conductor layer has a layer port. It performs linear conversions, and allows connections to other layers through electrical vias. The interconnection into the electromagnetic model at the layer port is realized with an ideal transformer, whose turns ratio equals the number of series-connected turns on that layer (m_i:1).

Spacings

The spacings between adjacent layers are modeled by impedances. The interconnect impedance between layer i and layer $(i+1)$ is $\frac{d}{w}Z_{Si}$, where

$$Z_{Si} = j\omega\mu_i a_i. \tag{4.15}$$

The spacing between layer i and layer $(i+1)$ has thickness of a_i and permeability of μ_i.

Magnetic core and air gaps

The effect of the magnetic core and air gaps are modeled by additional impedances on both sides of the circuit. The impedances representing the top and bottom of the magnetic core are Z_T and Z_B, where

$$\begin{aligned} Z_T &= j\omega/\mathcal{R}_T \\ Z_B &= j\omega/\mathcal{R}_B. \end{aligned} \tag{4.16}$$

Here $\mathcal{R}_T$ and $\mathcal{R}_B$ are the reluctances of the top and bottom of the core, respectively, including the reluctance of any gaps in the core in each of those positions. Core loss and its impacts can be captured by adding appropriate shunt resistances.

Cross-layer connections

The final step is to connect the layer ports of all modular impedance network in the same pattern as they are connected in the physical circuits. Cross layer capacitances and interconnect impedances can be modeled as independent elements as shown in Fig. 4-7.

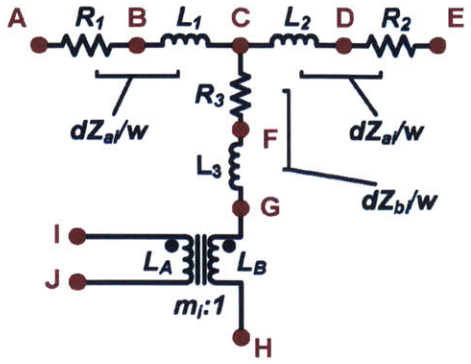
The lumped circuit model is completed up to this step. This model has frequency-dependent impedances, and thus can only rigorously capture single-frequency behaviors in the context of a circuit simulator that does not allow arbitrary impedance formulations. The model can be applied in fundamental harmonic analysis even when significant harmonics are present. The modeling accuracy is usually sufficient for making preliminary engineering design choices. Further expansions can be made to model systems with wide frequency range by various known techniques. One way is to simply repeat the modeling approach at each independent frequency of interest (utilized in this chapter). The other way is to generate more complicated impedance networks to capture behavior over a wide frequency range. Methods in this type include simple first- or second-order approximate networks [100], and discretized numerically-fitted networks [106]. Designers can make tradeoffs between model simplicity and accuracy by choosing and mixing these techniques.

4.4 Applications

4.4.1 Generating netlists for circuit simulation

The lumped circuit model shown in Fig. 4-6 (and shown in Fig. 4-7 with cross-layer connections included) can be solved analytically. More conveniently, it can be described by a netlist, and directly solved with a circuit simulator, such as SPICE. For example, a layer with m_i series-connected turns can be represented by a lumped circuit model as shown in Fig. 4-8a, and described by a netlist as shown in Fig. 4-8b. Since the generation of the lumped circuit model follows a step-by-step procedure, the full netlist of the pcb magnetics can be rapidly synthesized by a computer program[3] which calculates the impedance values based on geometry information and exports a netlist. Circuit simulations can be used to determine the current flowing through each winding and each layer, to calculate the mag-

[3] A software package that can generate SPICE netlists based on geometry information has been developed by the author and colleagues and is accessible by emailing the author (or by searching online for keyword "M2Spice").



*----------Netlists of a single layer----------
*----------1. Describing the Impedances----------

*--Name---	Node 1------	Node 2----------	Value------
R1	A	B	$\Re(dZ_{al}/w)$
L1	B	C	$\Im(dZ_{al}/w)/\omega$
L2	C	D	$\Re(dZ_{al}/w)/\omega$
R2	D	E	$\Re(dZ_{al}/w)$
R3	C	F	$\Re(dZ_{bl}/w)$
L3	F	G	$\Im(dZ_{bl}/w)/\omega$

*----------2. Describing the ideal transformer-----

LA	I	J	m_i^2
LB	G	H	1
K	LA	LB	1

(b)

Figure 4-8: Modular impedance network and its netlist for a layer with m_i turns. Here $\Re$ represents the real part of a complex value, and $\Im$ represents the imaginary part of a complex value.

netic field strengths at the surface of each conductor, to predict the loss on each layer, and to perform small signal analysis between two ports. Since the impedance values are calculated analytically and explicitly using the solutions to 1-D diffusion equations, this circuit simulation captures the skin and proximity effects, allowing impedances, losses, reactive energy, current sharing, etc., to be determined with the magnetics netlists simulated with the circuits.

A Python-based software tool - *M2Spice* has been developed to rapidly convert magnetics geometry information into SPICE netlists. A screenshot of the software user interface is shown in Fig. 4-9. A brief introduction to this software tool is provided in Appendix D.

4.4.2 Field visualization

This lumped circuit model also provides insight into the design of the magnetic structure. Fields at the surfaces of conductors solved using the lumped circuit model (i.e. H_T, H_B and K) can be used in calculating the fields and current densities inside the conductors using known formulations. For example, based on knowing the fields at the conductor surfaces (H_T and H_B) and the solutions to the 1-D diffusion equation (Appendix C.1.1), the H field strength inside the conductor as a function of the distance from the surfaces can be found

$$H_x(z) = \frac{H_T \sinh(\Psi z) + H_B \sinh(\Psi(h-z))}{\sinh(\Psi h)}. \tag{4.17}$$

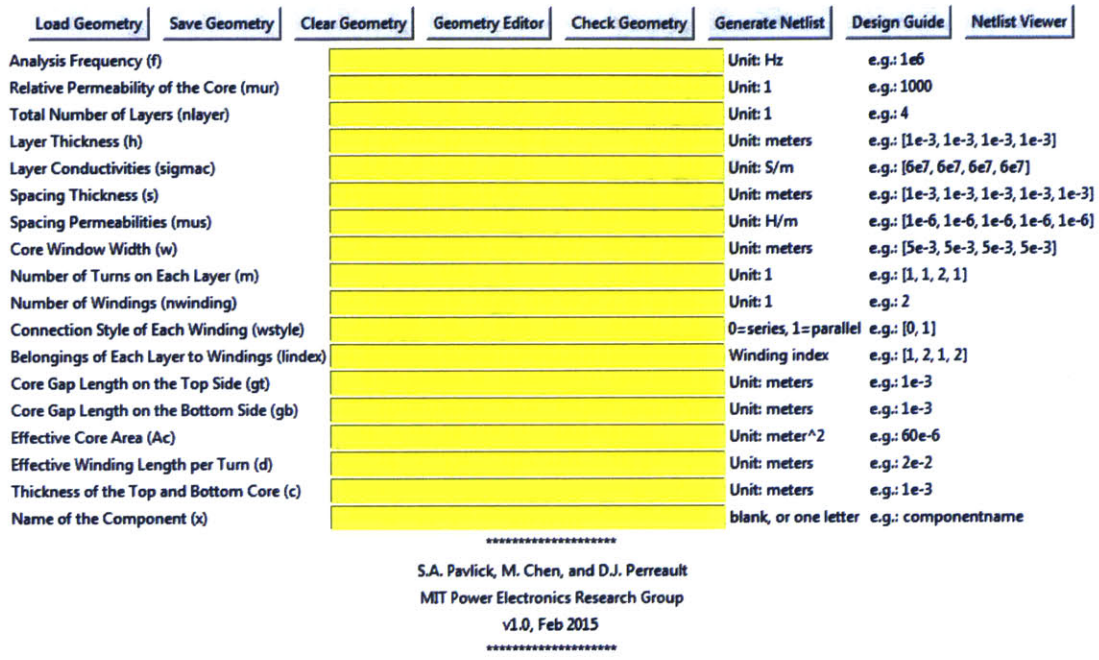


Figure 4-9: A screenshot of the user interface of the Magnetics to SPICE Netlists Conversion Tool - *M2Spice*.

Note $H_x(z)$ points towards the *x-axis*, and varies along the *z-axis* (the axes directions are defined in Fig. 4-2). Using *Ampere's Law*, $J_y(z) = \nabla \times H_x(z)$, the current density distribution in the conductor, $J_y(z)$, is

$$J_y(z) = \Psi \left[\frac{H_T e^{\Psi h} - H_B}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi(h-z)} - \frac{H_B e^{\Psi h} - H_T}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi z} \right]. \tag{4.18}$$

The loss in each layer can be calculated by $\frac{wd}{2\sigma} \int_0^h |J_y(z)|^2 dz$. Finally, using *Ohm's Law*, $J_y = \sigma E_y$, the electric field distribution inside the conductor, $E_y(z)$, is

$$E_y(z) = \frac{\Psi}{\sigma} \left[\frac{H_T e^{\Psi h} - H_B}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi(h-z)} - \frac{H_B e^{\Psi h} - H_T}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi z} \right]. \tag{4.19}$$

Hence, the field distribution and the current densities in the magnetic structure, within and outside the conductors along the thickness (z) direction, can be rapidly and explicitly solved and visualized (as demonstrated in Fig. 4-23).

4.4.3 Parameter/impedance extraction by simulation

Numerous ways of modeling magnetic devices with simpler circuit models have been developed [115–119]. To determine the parameters of many of these models, experimental measurements are required. For example, open- and short-circuit measurements are often used to extract the parameters of the inductance matrix [115, 117] and inductance-based cantilever model [94]. Well conducted experimental measurements undoubtedly capture the most information. However, the accuracy of experimental measurements are limited by many practical constraints (e.g., instrument capability, non-ideal open- and short-connections, etc.). The layer port configuration of the MLM model is similar to a physical multi-port planar magnetic structure, it can be analyzed and simulated similar to many experimental measurements (e.g. open- and short-circuit tests), while many practical constraints are avoided. It well captures major electromagnetic interactions and requires few approximations. As a result, by simulating the netlist (i.e. open- and short-circuit tests), one can use the MLM to rapidly extract parameters and generate simpler circuit models, e.g. synthesizing an impedance matrix description as demonstrated in Table 4.2 and Fig. 4-24, or determining self- and mutual-resistances among different windings [79]. An example of this in real power converter is presented in Chapter 4 and Appendix C for the transformer in the prototype dc-dc converter presented there..

4.5 Theoretical Verification

The proposed modeling approach can be theoretically verified by checking its results against some known results.

4.5.1 Poynting's theorem and energy conservation rule

The energy processed in any structure must satisfy the Poynting's theorem: the power dissipated and stored within it must equal the integral of the Poynting vector over a closed surface boundary cutting into this surface. In Fig. 4-4a, assuming that there is no spacing between two series-connected turns on the same layer, and that all turns have the same

width $\frac{w}{m_1}$, the complex power dissipated and stored in layer 1 is

$$P_{poynting} = \underbrace{dw}_{\text{Surface Area}} \underbrace{(E_{T1}H_{T1}^* - E_{B1}H_{B1}^*)}_{\text{Poynting vectors}}. \tag{4.20}$$

Now consider the three-terminal impedance network of "Layer 1" in Fig. 4-4b. The electrical power going into layer 1 is

$$\begin{aligned} P_{model} &= \underbrace{\frac{V_1}{m_1}m_1 I_1^* + (\frac{V_1}{m_1} - E_{B1}d)wH_{B1}^* - (\frac{V_1}{m_1} - E_{T1}d)wH_{T1}^*}_{\text{Electrical power of the three terminals}} \\ &= dw(E_{T1}H_{T1}^* - E_{B1}H_{B1}^*). \end{aligned} \tag{4.21}$$

Hence, the match between (4.20) and (4.21) shows that the MLM model predicts the same loss and energy storage in a layer as the Poynting's theorem. The energy conservation rule holds.

4.5.2 Current distribution at dc

The proposed modeling approach can be checked to ensure that it predicts correct results in the extreme case when the conductor carries dc current ($\omega \to 0$). For the one-turn layer shown in Fig. 4-2, if $\omega \to 0$, then $\delta \to \infty$, and $\Psi \to 0$. Using (4.18), the current distribution at dc is

$$\lim_{\Psi \to 0} J_y(z) = \lim_{\Psi \to 0} \frac{2(H_T - H_B)\Psi}{e^{\Psi h} - e^{-\Psi h}} = \frac{K}{h}. \tag{4.22}$$

This indicates that the current distribution is a constant along the conductor thickness when $\omega \to 0$, which is as expected.

4.5.3 Dowell's formulation

For planar structures with multiple adjacent layers connected in series, the proposed approach can be used to derive the well-known Dowell's formulation [37]. Considering the planar structure shown in Fig. 4-5 and Fig. 4-6, if all n layers are one-turn layers with identical thicknesses h and width w, and all n layers are connected in series, the ac impedance of this n layer structure is

$$Z_{ac} = \left(nZ_b + 2Z_a \sum_{k=1}^{n-1} k^2 + n^2 Z_a \right). \tag{4.23}$$

Substituting (4.14) into (4.23), the ac resistance (R_{ac}) can be found as the real part of Z_{ac}:

$$\begin{aligned} R_{ac} =&\Re(Z_{ac}) = R_{dc}\Delta \times \Re\left[\coth(\Delta(1+i))(1+i)\right] + \\ & R_{dc}\frac{2(n^2-1)}{3}\Delta \times \Re\left[\tanh(\frac{\Delta}{2}(1+i))(1+i)\right]. \end{aligned} \tag{4.24}$$

Here $R_{dc} = \frac{nd}{\sigma wh}$ and is the dc resistance of the n series layers. Δ is the "thickness-to-skin-depth" ratio ($\frac{h}{\delta}$). Since

$$\begin{aligned} \Re\left[\coth(\Delta(1+i))(1+i)\right] &= \frac{\sinh(2\Delta)+\sin(2\Delta)}{\cosh(2\Delta)-\cos(2\Delta)} \\ \Re\left[\tanh(\frac{\Delta}{2}(1+i))(1+i)\right] &= \frac{\sinh(\Delta)-\sin(\Delta)}{\cosh(\Delta)+\cos(\Delta)}, \end{aligned} \tag{4.25}$$

the ac resistance to dc resistance ratio, $F_R = \frac{R_{ac}}{R_{dc}}$, is

$$F_R = \Delta\left(\frac{\sinh(2\Delta)+\sin(2\Delta)}{\cosh(2\Delta)-\cos(2\Delta)} + \frac{2(n^2-1)}{3}\frac{\sinh(\Delta)-\sin(\Delta)}{\cosh(\Delta)+\cos(\Delta)}\right). \tag{4.26}$$

This is the well-known Dowell's formulation.

4.6 Experimental Verification and Application Examples

To further verify the model, we compare the modeling results against FEM simulations and experimental measurements. These verifications also serve as application examples to demonstrate how to use the model in practical designs. Figure 4-10 shows the geometry of a selected example structure. It has four one-turn 17 μm thickness (half oz) copper layers, fabricated using two 0.787 mm (31 mil) thickness double-sided copper boards with FR4 material as the core. A 0.14 mm thickness polyimide (Kapton) film is used as the spacing insulator between the two copper boards. Seven ELP22 cores of MnZn ferrite (Epcos N49) are lined up to make a long structure with impedances that were high enough to be accurately measured. Under this setup, structures are sufficiently long and since the permeability of the core is very high, the 1-D assumption is satisfied. In all following modeling calculations, μ_0, μ_r, and σ are selected to be $4\pi \times 10^{-7}$ H $\cdot$ m^{-1}, 1500, and 5.8×10^7 S $\cdot$ m^{-1}, respectively. Cases with fewer cores and shorter length were also checked to study when the feasible range of the 1-D assumption. The frequency range for testing was 10 kHz to 100 MHz. Two impedance analyzers - Agilent 4192A (5Hz-13MHz) and Agilent 4395A (100kHz-500MHz) - are calibrated and utilized to cover this frequency range. The operating temperature was selected to be 20°C. Fig. 4-11 shows a few pictures of these

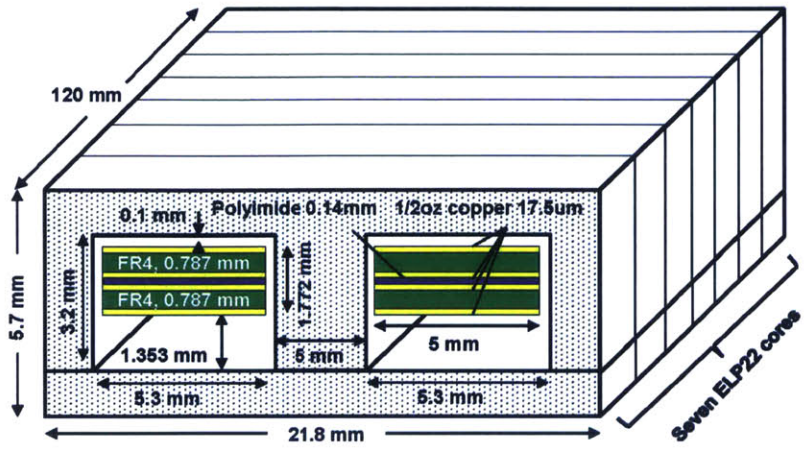


Figure 4-10: Geometry of the seven-core four-layer structure. It is used to fabricate the 1:1 and 2:1 transformers. The calculated dc resistance of a single layer at 20°C is 44.8mΩ, which is high enough to be measured with the impedance analyzers.

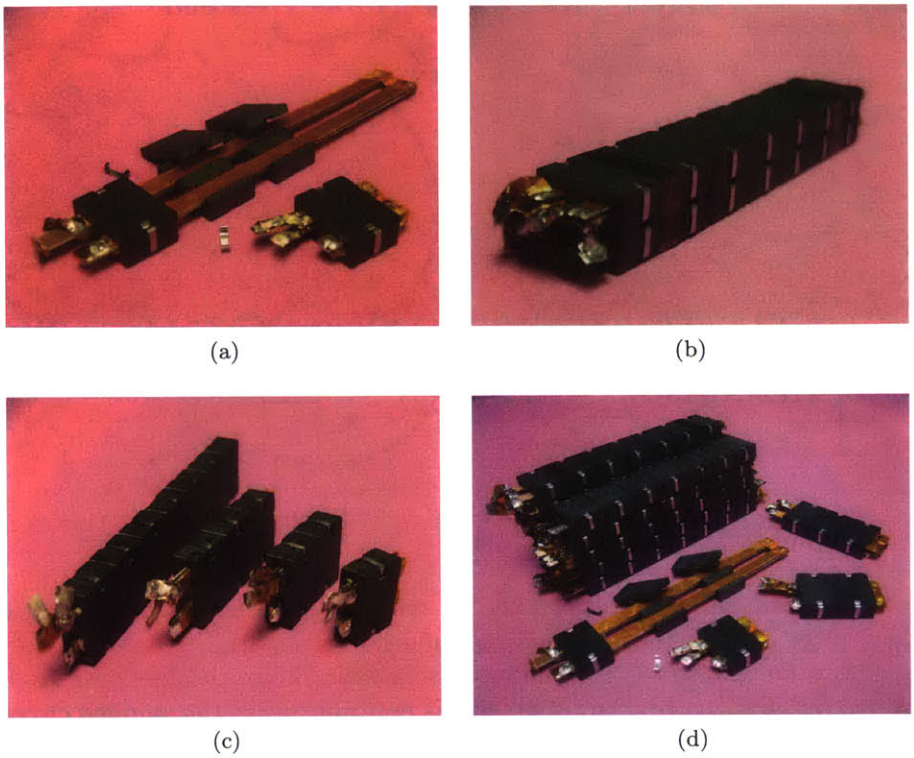
prototypes. For each group of devices, interleaving patterns can have significant impact on the impedances and current distributions, as does the spacing of the pcb layer stacks. Three types of configurations, which represent a majority of possible interleaving patterns, are prototyped by connecting the four copper layers in three ways:

1. *1:1 transformers with parallel-connected layers*: two layers are connected in parallel as a one-turn winding; two layers are connected in parallel as another one-turn winding.

2. *2:1 transformers with hybrid series-parallel-connected layers*: two layers are connected in series as a two-turn winding; two layers are connected in parallel as a one-turn winding.

3. *One-turn inductors with parallel-connected layers*: two layers are selected and connected in parallel as a one-turn winding; the other two layers are not presented (this prototype is manufactured using two single-sided copper boards).

The goal is to compare the predicted and measured ac resistance (R_{ac}) and ac inductance (L_{ac}) in these structures under the setup as shown in Fig. 4-12 when they are operating in the 10 kHz to 100 MHz frequency range.



(a) (b)

(c) (d)

Figure 4-11: Photographs of the constructed prototype: (a) copper layers and magnetic cores of a prototype. (b) Two 2:1 transformers connected and measured in the setup shown in Fig. 4-12b, (c) Four 1:1 transformers with different lengths (i.e. one core, two cores, three cores and seven cores), and (d) all constructed prototypes.

4.6.1 1:1 transformers with parallel-connected layers

Figure 4-13 shows three different ways of connecting the four layers in a 1:1 transformer having two paralleled layers in each winding, including one "non-interleaved" option, one "alternating" interleaved option, and one "symmetric" interleaved option. The measurement setup is shown in Fig. 4-12a. This setup avoids exciting the magnetizing flux path in the core, and thus isolates the impact of core losses on the verification results. Cases when the core is excited are separately presented in Section 4.6.3. Figure 4-14 shows the lumped circuit models for the four layer structures. Note that in this setup, the impedances associated with the top and bottom magnetic cores (Z_T and Z_B in Fig. 4-6) carry no flux. Considering cross-layer connections (electrical vias), three simplified circuits shown in Fig. 4-15 are generated. One can easily analyze these circuits, and compare the R_{ac} and L_{ac} in each case.

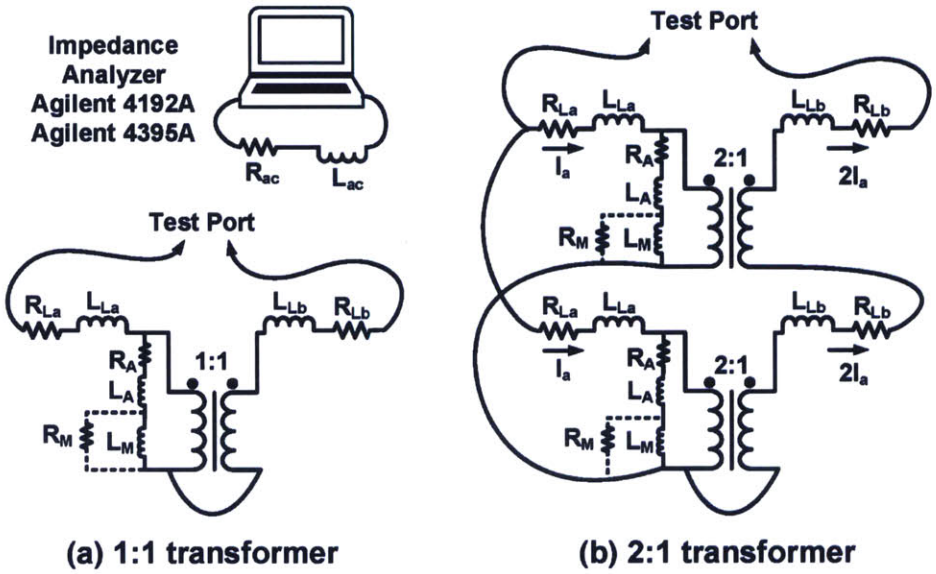


Figure 4-12: Experimental configurations for measuring (a) 1:1 transformers with two-parallel-layer pairs; (b) 2:1 transformers with hybrid-series-parallel windings pairs. These configurations avoid exciting the core and thus isolate the impact of core losses on the results (bypassing the R_A, L_A, L_M branch). Core loss is not captured in this lumped circuit model. If one would like to include the modeling of core loss, it could be represented as a resistance R_M in parallel with L_M.

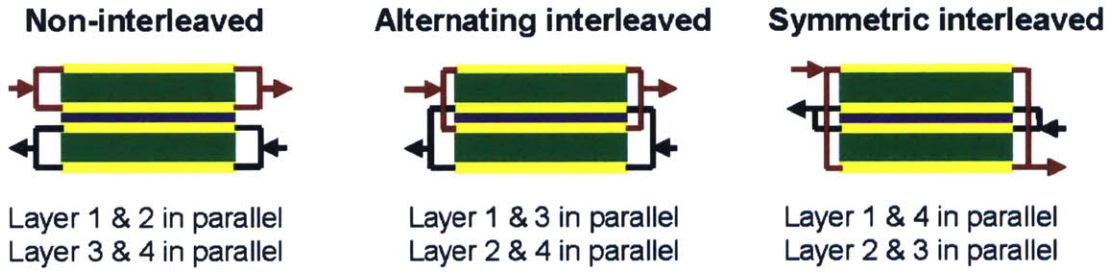


Figure 4-13: Three different ways of interleaving the four conductor layers in a 1:1 transformer having two paralleled layers for each winding, including a "non-interleaved" option, an "alternating" interleaved option, and a "symmetric" interleaved option. The four conductive layers are referred as "Layer 1" to "Layer 4" from top to bottom.

In addition, FEM models for these structures are analyzed using the ANSYS Maxwell 2-D FEM simulation package (version 16.0, 64-bit). Figure 4-16 shows the magnetic field strength in the three structures when they are operating at 10 MHz. The dissipated power (P_{ac}) and stored reactive energy (E_{ac}) in these structures as a function of frequency are found by the software, leading to the simulated R_{ac} and L_{ac} determined by FEM methods.

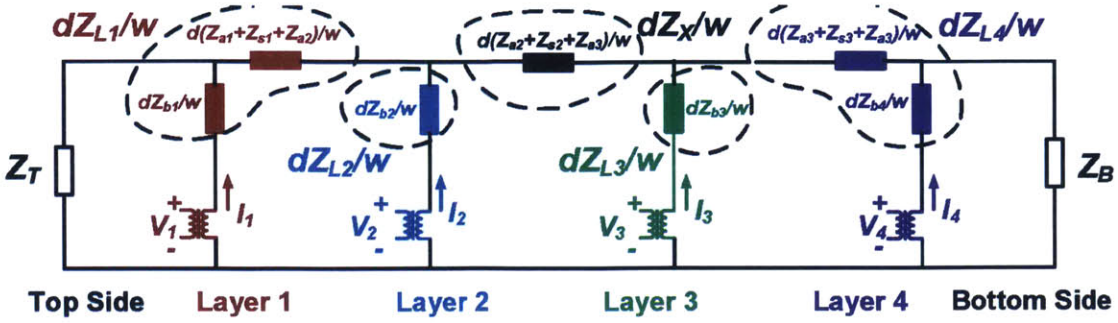


Figure 4-14: Modular layer model for the structure shown in Fig. 4-10 without modeling the electrical vias. The colors of impedances in this figure are labeled in the same way as in Fig. 4-15.

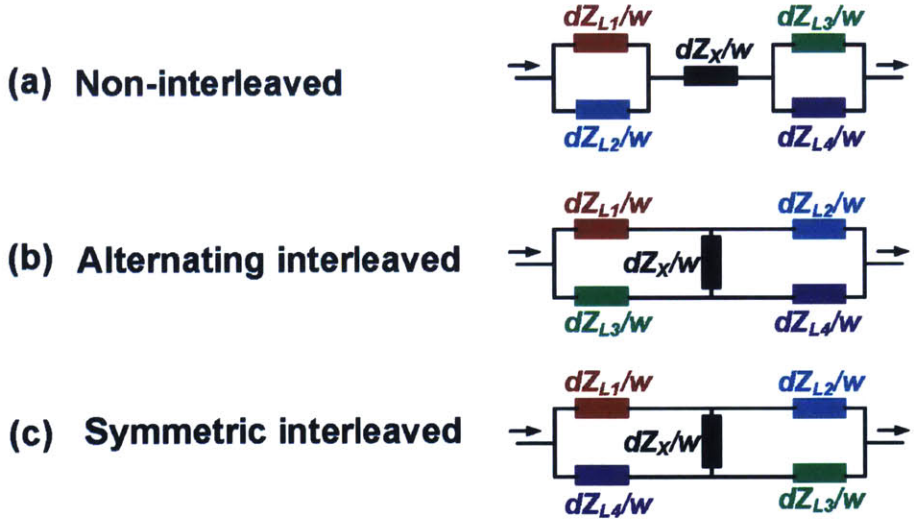


Figure 4-15: Simplified modular layer model for the three interleaving patterns of the 1:1 transformer, including the vias. The colors of impedances in this figure are labeled in the same way as in Fig. 4-14. Since the core is not excited, the impedances representing the core (Z_T and Z_B) in Fig. 4-14 have been removed.

Finally, the ac resistance (R_{ac}) and ac inductance (L_{ac}) of these transformers are measured with the impedance analyzers using the setup shown in Fig. 4-12. As shown in Fig. 4-17, the results from analyzing the lumped circuit model match extremely well with FEM simulations over the entire frequency range[4], and match very well with experimental measurements. A few practical constraints that may cause the mismatches are investigated in Section 4.7.

[4]This may be because ANSYS Maxwell 2-D also makes the MQS assumption. And the 1-D assumption is well satisfied in the prototyped geometry. In other words, the FEM is effectively numerically solving the same Maxwell's equation sets as the proposed analytical model, yielding the well-matched results.

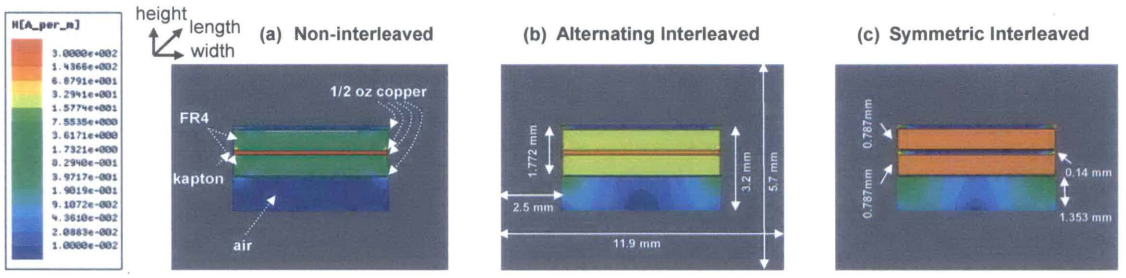


Figure 4-16: Magnetic field distribution in three 1:1 transformers having two paralleled layers for each winding, each with different interleaving patterns, driven by a 10 MHz 1 A (peak) current (using the setup in Fig. 4-12a). Layer indices from top to bottom are: layer 1, layer 2, layer 3, layer 4. The simulation was done in ANSYS Maxwell 2-D FEM simulation environment.

It is known that as the operating frequency increases, skin and proximity effects change the current distribution, changing the real and reactive impedances of a magnetic device. These effects are often extremely difficult to analytically and quantitatively determine when there are parallel layers, multiple windings and/or multiple interleaving options. The proposed approach is a powerful tool to systematically study and control these complicated frequency dependent effects. Many qualitative and quantitative findings can be observed from Fig. 4-17; among those are:

1. Starting from 100 kHz, interleaved designs ("alternating" and "symmetric") have lower loss than the non-interleaved design ("non-interleaved"). The loss reduction can be as high as 50% at 10 MHz.

2. Between the two interleaved structures, the loss of the "symmetric" design can be up to 37.5% lower than that of the "alternating" design at 10 MHz. This is because the current directions in layers 2 and 3 are opposite to each other in the "alternating" design, with narrow spacing in between. A big portion of the current concentrates in layers 2 and 3, causing high loss. This may alternatively be viewed as the "alternating" design having more circulating current in the parallel layers and hence higher loss. As the proposed model well predicts this effect, the model is well suited to selecting interleaving configurations (especially when there are parallel layers) to minimize loss.

3. Which interleaving pattern has higher ac resistance actually depends on the pcb layer stack spacings. Figure 4-18 shows two selected layer stacks for comparison purposes. One layer stack has thin polyimide film (0.14 mm) as the middle spacing layer (Thin-

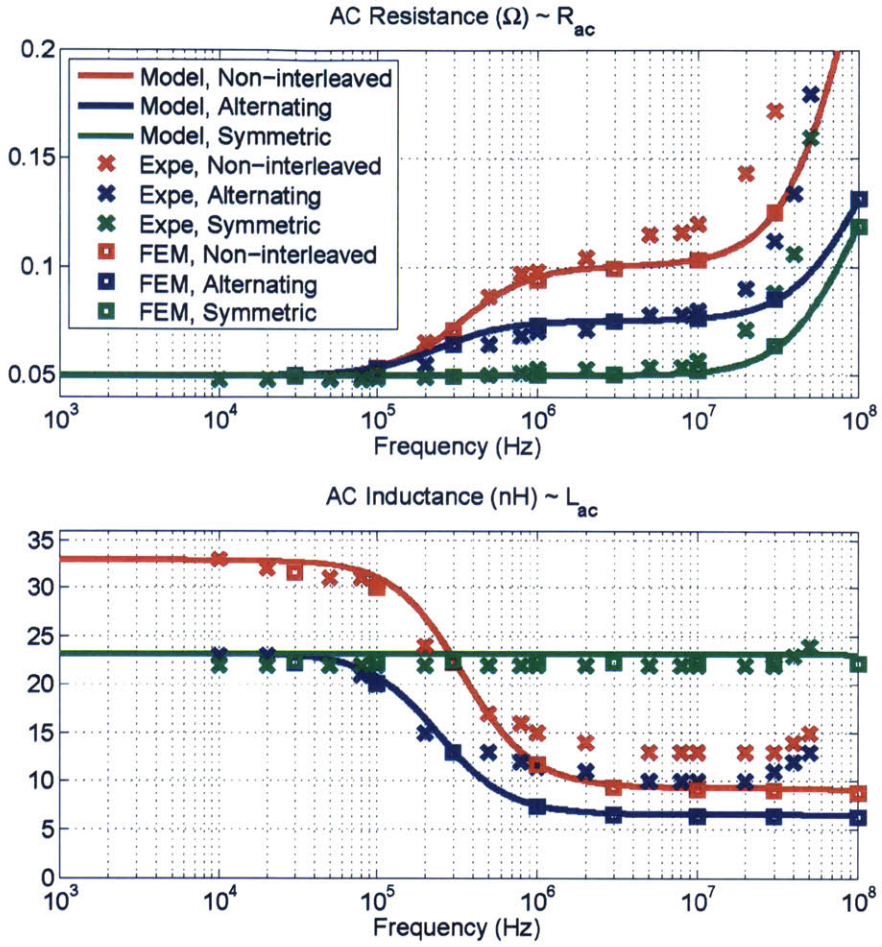


Figure 4-17: R_{ac} and L_{ac} of the 1:1 transformer structure with the three interleaving patterns as shown in Fig. 4-14, predicted by the proposed approach (Model), simulated by ANSYS (FEM), and measured from the prototype (Expe) under the setup as shown in Fig. 4-12a.

Mid-Layer). This layer stack is also the default layer stack used in this chapter. The other layer stack, in comparison, employs a thick FR4 board (1.574 mm) as the middle spacing layer (Thick-Mid-Layer). The winding width, length, height, core shape and other experimental aspects are kept the same as described in Fig. 4-10. The R_{ac} and L_{ac} in the two pcb layer stacks with different interleaving patterns are shown in Fig. 4-19. With the "Thin-Mid-Layer" layer stack, the "symmetric" design has significantly lower R_{ac} than the "alternating" design. With the "Thick-Mid-Layer" layer stack, however, the "symmetric" design has slightly higher R_{ac} than the "alternating" design. This example illustrates the importance of considering layer spacing in selecting an interleaving scheme,

Figure 4-18: Two pcb stacks having different spacings among the four conductive layers: (a) Thin-Mid-Layer: with thin polyimide film as the middle spacing layer; (b) Thick-Mid-Layer: with thick FR4 board as the middle spacing layer.

and demonstrates that the MLM can be used to select the optimal interleaving structure that has the minimum R_{ac} for a chosen pcb stack spacing, and to optimally select pcb stack spacings/materials.

4. The change of the ac resistance is caused by the redistribution of current and magnetic field, which also changes the reactive impedance of the planar structure (e.g., leakage inductances of transformers). The proposed approach can be used to select an interleaving structure that has the most appropriate reactive impedance. As shown in Fig. 4-19, for the "Thin-Mid-Layer" layer stack, the "non-interleaved" design has high L_{ac} at low frequencies because it excites high magnetic fields in both the side spacings and the middle spacing. The L_{ac} of the "non-interleaved" design and "alternating" design drop as the frequency increases, because as current concentrates in the middle layers, energy stored in the spacings and within conductors decreases. Considering various interleaving patterns and pcb layer stacks, the proposed approach can be used to model the reactive impedance in a magnetic device, enabling multiple design tradeoffs to be made together (e.g. when designing a pcb integrated transformer for a resonant converter).

5. Fig. 4-21 shows the experimentally-measured magnitudes ($|Z|$) and phases ($\angle Z$) of the impedances of the "alternating" interleaved design across the 10 MHz-200 MHz range for the configuration shown in Fig. 11a. The device is inductive when the frequency is lower than 128.31 MHz, and becomes capacitive when the frequency exceeds 128.31 MHz. This threshold frequency is usually referred to as the "resonant frequency", which is determined by the inductive and capacitive characteristics of the winding layers. As shown in Fig. 4-17, the modeling/experimental mismatch starts to increase significantly

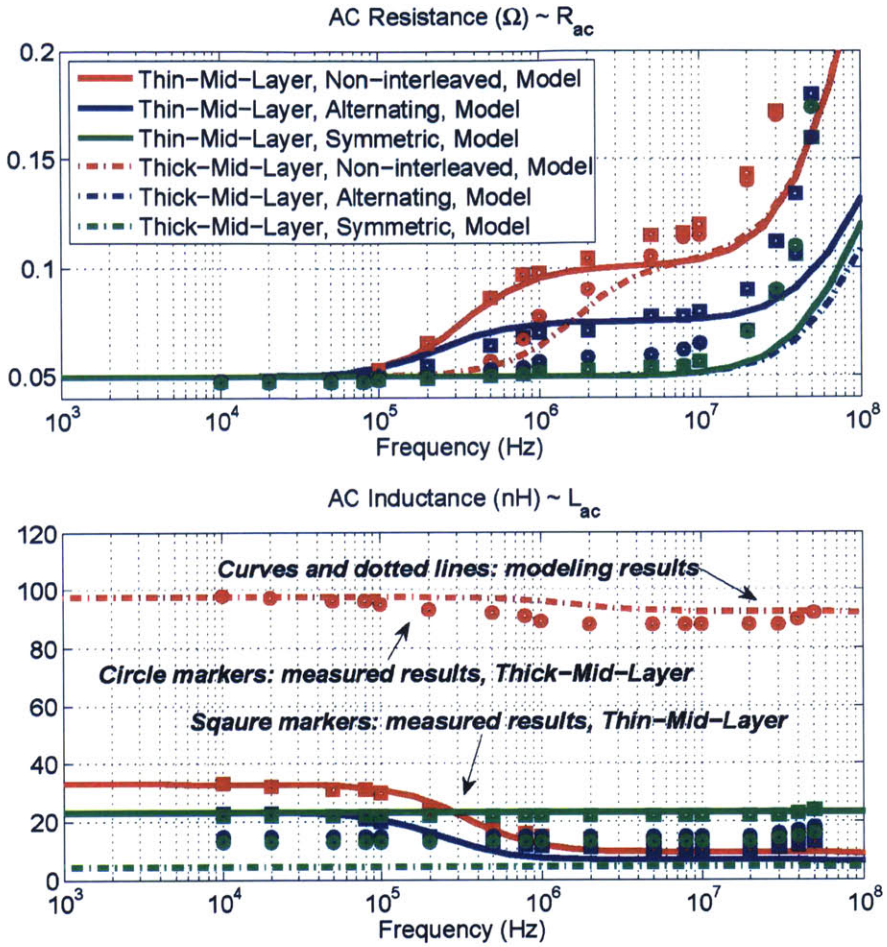


Figure 4-19: R_{ac} and L_{ac} of the 1:1 transformer for two different pcb layer stacks and three different interleaving patterns. One layer stack has thin polyimide film as the middle spacing (Thin-Mid-Layer). The other layer stack has thick FR4 board as the middle spacing (Thick-Mid-Layer). Curves and dotted lines are modeling results. Measured results of prototypes with Thin-Mid-Layer pcb stack spacing are labeled with *square* markers. Measured results of prototypes with Thick-Mid-Layer pcb stack spacing are labeled with *circle* markers.

as the frequency approaches the resonant frequency (i.e. frequencies approaching 100 MHz). Under the EQS assumption, the estimated capacitance of the "alternating" interleaved design is 120.04 pF. Following the configuration of Fig. 4-7, this capacitance is connected in parallel with the estimated ac inductance, resulting in an estimated resonant frequency of 162.41 MHz. This is roughly in the right frequency regime, as compared the experimental value of approximately 128.3 MHz (Fig. 4-21). Many other effects (e.g. interconnects, 2-D/3-D effects, distributed LC (transmission-line) effects, manufacturing

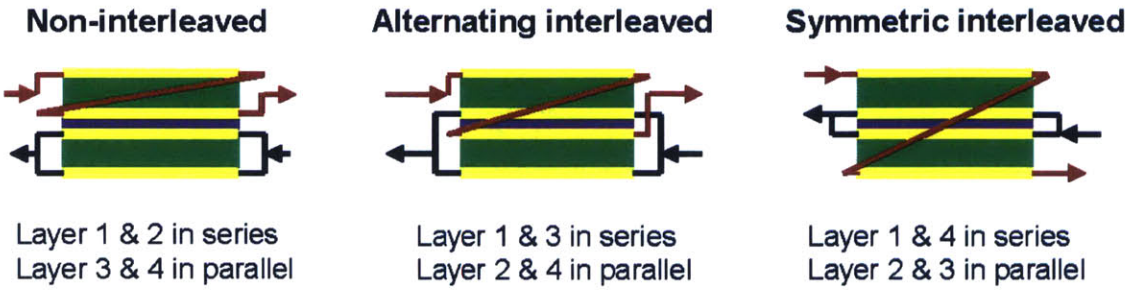


Figure 4-20: Three different interleaving patterns of the hybrid-series-parallel 2:1 transformer having one winding comprising two series-connected layers and the other winding comprising two parallel-connected layers.

Table 4.1: Calculated loss in the four layers of the "alternating" and "symmetric" interleaved transformers under the setup of Fig. 4-12b, when they are operating at 10 MHz and 100 MHz and driven by a 1 A rms sinusoidal current in the two series-connected layers, and a reverse 2 A rms sinusoidal current in the two parallel-connected layers.

Loss in Each Layer # (mW)	#1	#2	#3	#4	Total
Alternating, 10 MHz	24.7	79.6	24.1	0.7	129.1
Symmetric, 10 MHz	24.7	24.7	24.7	24.7	98.8
Alternating, 100 MHz	62.7	100.3	44.4	1.7	209.1
Symmetric, 100 MHz	62.7	62.7	62.7	62.7	250.8

White: series-connected layers; Grey: parallel-connected layers.

mismatches) which are not considered in this estimation, cause the modeling mismatch. Nevertheless, it can be seen that a first-order approximation of the resonant frequency (which defines the applicable range of the 1-D MQS model) can be obtained simply by combining the 1-D MQS model with simple EQS models.

4.6.2 2:1 transformers with hybrid-series-parallel layers

The purpose of this experiment is to verify the effectiveness of the proposed approach for modeling planar magnetics with hybrid series- and parallel-connected layers, and to demonstrate more application examples. Figure 4-20 shows three different ways one may connect the four layers to construct a 2:1 transformer with both series- and parallel-connected layers. Two layers are series-connected as a two-turn primary winding, and two layers are parallel-connected as a one-turn secondary winding. Because the primary current is twice

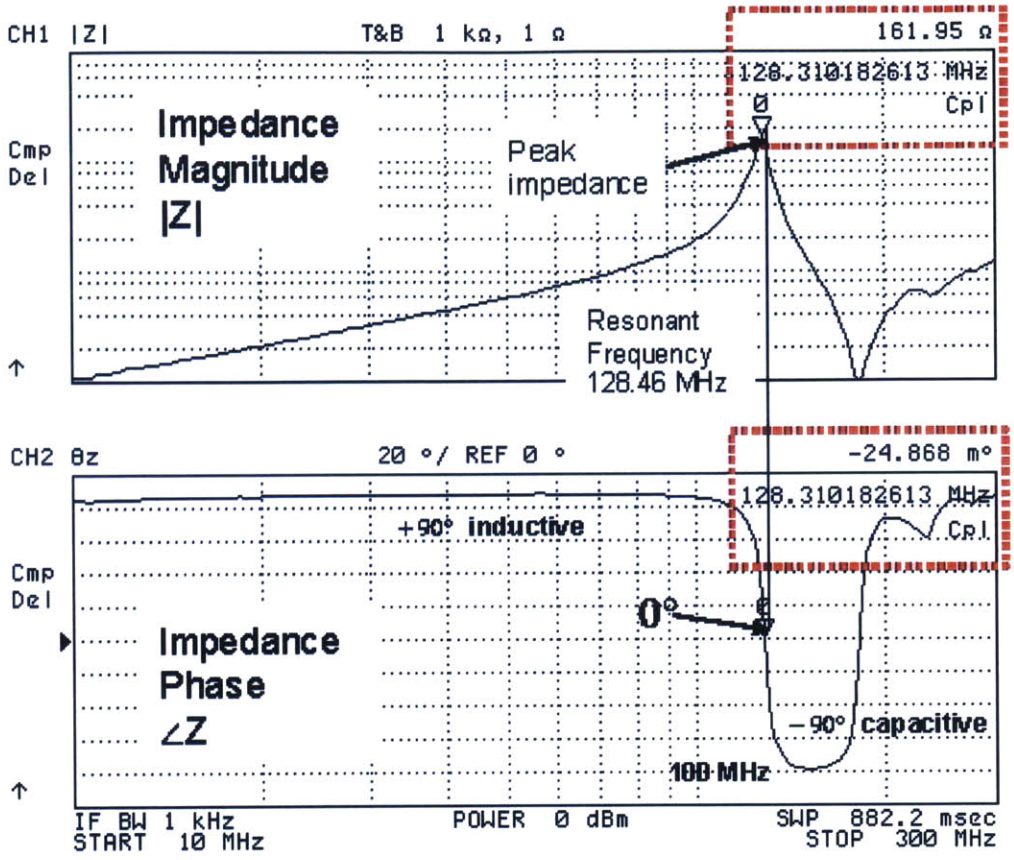


Figure 4-21: Measured impedance of the "alternating" interleaved 1:1 transformer (connected as shown in Fig. 11a, measured using an Agilent 4395A impedance analyzer). The measured resonant frequency is 128.31 MHz. In comparison, the estimated cross-layer capacitance is 120.04 pF, resulting in an estimated resonant frequency of 162.41 MHz. Many other effects (e.g. interconnects, 2-D effects, 3-D effects, manufacturing mismatches) are not considered in this estimation.

as large as the secondary current, a "parallel-primary series-secondary" setup as shown in Fig. 4-12b is utilized to measure winding impedances while avoiding exciting the magnetizing inductance. This setup needs two identical 2:1 transformers. Figure 4-22 compares the results from the model, the FEM simulations and experimental measurements. The modeling results match very well with FEM simulations over the entire frequency range, and match experimental results within 20% up to 10 MHz. This setup has higher mismatch than the 1:1 transformer setup because the two transformers connected to make the measurement are not entirely identical (thus exciting the core to some extent), and the interconnects between the two transformers are not captured in the model. Nevertheless,

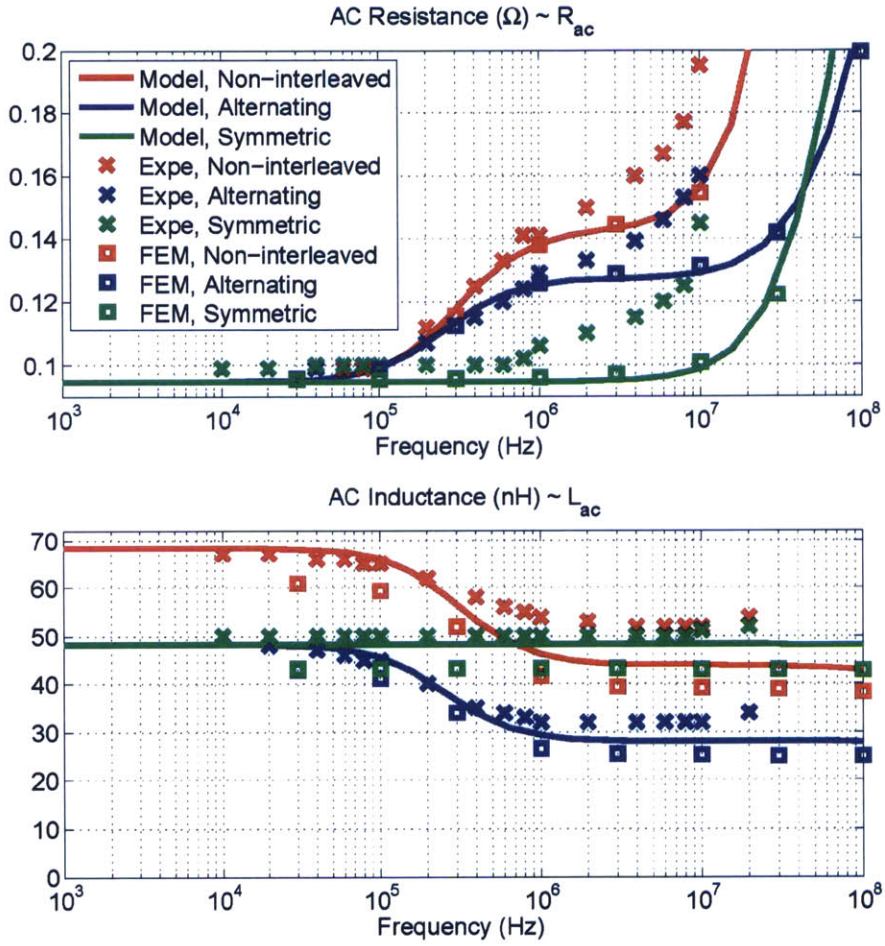


Figure 4-22: R_{ac} and L_{ac} of the planar transformer with 2:1 hybrid series-parallel layers and three interleaving patterns, predicted by the lumped model (labeled as "Model"), simulated by ANSYS (labeled as "FEM"), and measured from the prototype (labeled as "Expe") under the setup as shown in Fig. 4-12b.

the results demonstrate the efficacy of the proposed approach for capturing the behavior of sophisticated winding structures.

As a field visualization example, Fig. 4-23 shows the calculated current distribution (density) within the four layers when the "alternating" and "symmetric" interleaved transformers are operating at 10 MHz and 100 MHz (using Eq. (4.18) after solving the circuit). Based on this current distribution, the loss of the four layers under the two interleaving connections were calculated and are listed in Table 4.1. Fig. 4-23 and Table 4.1 match with and explain Fig. 4-22. At 10 MHz, the "symmetric" design has lower R_{ac} than the "alternating" design because its current distributes symmetrically and is equally shared in

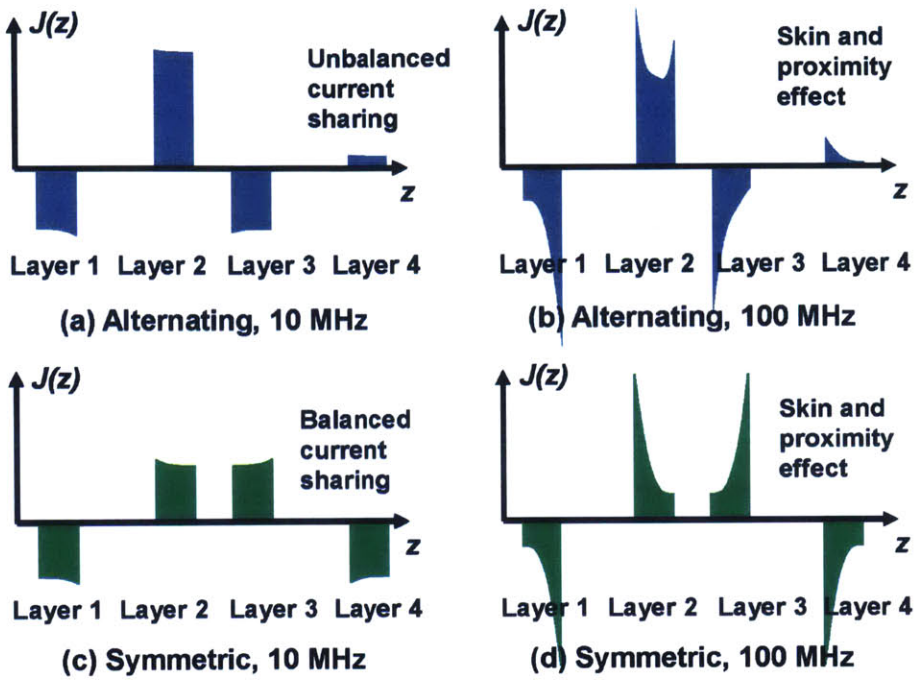


Figure 4-23: Calculated current distribution in the four conductive layers in the "alternating" and "symmetric" interleaved transformers under the setup of Fig. 4-12b when they are operating at 10 MHz and 100 MHz, using simplified lumped circuits shown in Fig. 4-20. The two series-connected layers are shown with negative current densities while the two parallel-connected layers are shown with positive current densities.

Table 4.2: Extracted impedance matrices of the "alternating" and "symmetric" interleaved transformers when they are operating at 10 MHz and 100 MHz. The polarities of the voltages and currents are defined in Fig. 4-24.

$\mathbf{Z}$, unit : Ω	defined as: $\begin{pmatrix} V_a \\ V_b \end{pmatrix} = \mathbf{Z} \times \begin{pmatrix} I_a \\ I_b \end{pmatrix}$
Alternating, 10 MHz	$\begin{pmatrix} 24.253 + 28\,417j & 12.052 + 14\,208j \\ 12.052 + 14\,208j & 6.0487 + 7\,104.9j \end{pmatrix}$
Symmetric, 10 MHz	$\begin{pmatrix} 24.153 + 28\,416j & 12.036 + 14\,208j \\ 12.036 + 14\,208j & 6.0408 + 7\,105.6j \end{pmatrix}$
Alternating, 100 MHz	$\begin{pmatrix} 2\,406.3 + 284\,150j & 1\,203.1 + 142\,070j \\ 1\,203.1 + 142\,070j & 601.63 + 71\,043j \end{pmatrix}$
Symmetric, 100 MHz	$\begin{pmatrix} 2\,406.3 + 284\,144j & 1\,203.1 + 142\,071j \\ 1\,203.1 + 142\,071j & 601.70 + 71\,051j \end{pmatrix}$

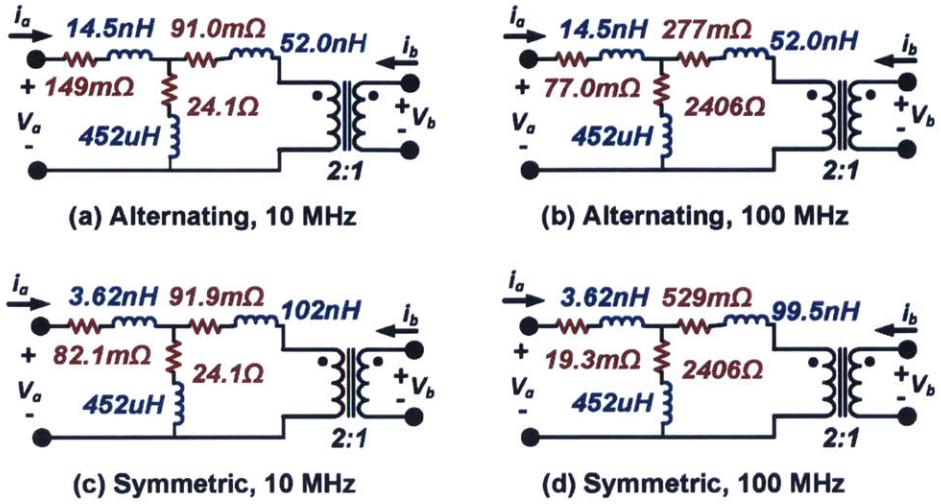


Figure 4-24: Simplified circuit models (T models with magnetizing and leakage inductances) of the "alternating" and "symmetric" interleaved transformers when they are operating at 10 MHz and 100 MHz. All component values are extracted from the lumped circuit model by open- and short-circuit simulations.

parallel layers (layers 2 and 4). However, at 100 MHz, with stronger skin and proximity effects, the "alternating" design has lower R_{ac}. This is because although current is not equally shared between the two parallel layers in the "alternating" design, its layer 2 is still effectively utilized on both sides, whereas all the layers in the "symmetric" design only carry significant current on one side. At 100 MHz, layer 3 in the "symmetric" design also benefits mildly from having the current better distributed throughout the conductor, compared to the conductors in the "symmetric" design. It can be concluded that balanced current sharing between parallel-connected layers doesn't necessarily guarantee lower loss when the frequency is high enough so that the conductor thickness is significant relative to the skin depth. In this frequency range, it is not only the current distribution between layers that matters, but also the current distribution between surfaces of the conductors.

As a parameter extraction example, Table 4.2 shows the impedance matrices of the "alternating" and "symmetric" interleaved transformers operating at 10 MHz and 100 MHz. Elements of these impedance matrices are extracted by doing open- and short-circuit simulations using the lumped circuit model in LTspice IV. These impedance matrices are interchangeable with four example simplified circuit models (T models with magnetizing and leakage inductances) as shown in Fig. 4-24. These simplified circuit models carry the same

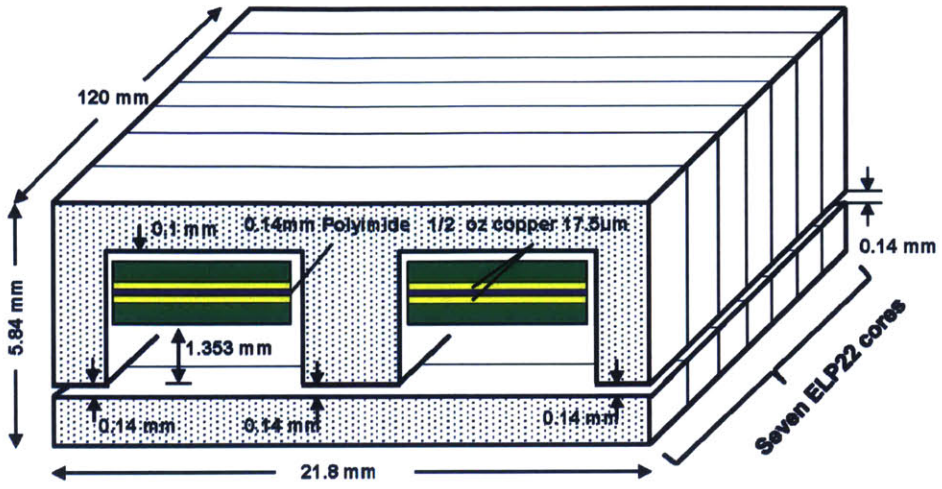


Figure 4-25: Geometry of the prototyped two-parallel-layer inductor with a narrow spacing between the two conductive layers. Carefully controlled gaps are created in the center and side legs.

information as the original MLM model, but have fewer components, can be easily utilized in conventional circuit analysis, and can be easily integrated into circuit simulations. They are related to the models derived in [93], based on short-circuit analysis, but are more complete because they are based on the full impedance matrix (i.e. both the energy storage and loss are captured).

Figures 4-22-4-24 and Tables 4.1-4.2 show the same results, and demonstrate a variety of different ways to utilize the model and interpret the results.

4.6.3 One-turn inductors with parallel-connected layers

The purpose of this experiment is to verify the effectiveness of the proposed approach for modeling planar magnetics with excited cores (e.g., inductors) and parallel-connected layers. (The modeling results for inductors with series-connected layers are theoretically verified by comparing them with Dowell's formulation [37] in Section 4.5). Figures 4-25-4-26 show the geometry and layer connections of an inductor with two parallel-connected layers. The winding stack is placed far from the air gap to reduce the fringing effect [38, 39]. In one inductor, layers 2 and 3 are selected and paralleled. This inductor has narrow spacing between two layers (polyimide film). In the other inductor, layers 2 and 4 are selected and paralleled. This inductor has wide spacing between two layers (FR4 broad and polyimide

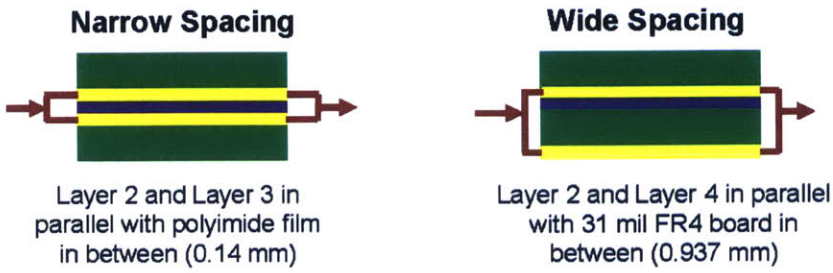


Figure 4-26: Two layers out of the four layers are selected and connected in parallel. One implementation has a narrow spacing between the two parallel-connected layers ("Narrow Spacing"). The other implementation has a wide spacing between the two parallel-connected layers ("Wide Spacing").

film). The ac resistance and ac inductance of this inductor are measured with an impedance analyzer (100 kHz-1 MHz). The core loss can be estimated by using the datasheet, and subtracted to yield the winding loss. At the same time, the R_{ac} and L_{ac} are predicted using the proposed model and FEM simulations. As shown in Fig. 4-27, the modeling results match very well with FEM results, and match well with experimental results up to 1 MHz (This is the highest recommended operating frequency for the EPCOS N49 MnZn material with known core loss). No effort has been made to measure its core loss above 1 MHz.

4.7 Model Applicability and Practical Considerations

4.7.1 Model applicability

The proposed modeling approach provides accurate results as long as the MQS and 1-D assumptions are both satisfied. In most power electronics applications, the MQS assumption typically holds because the operating frequency is low enough such that the winding length is much shorter than the corresponding wavelength. The 1-D assumption results in important constraints on applicability. We first provide a general explanation of the situations in which the 1-D assumption applies, followed by empirical examination to better define the boundaries of applicability in practical cases.

High-permeability cores with rectangular winding windows are the most common types of geometries in which the 1-D assumption can, under certain conditions, apply. In a transformer with an un-gapped high-permeability core, and thus, negligible magnetizing admittance (high magnetizing inductance), the MMF produced by the primary winding

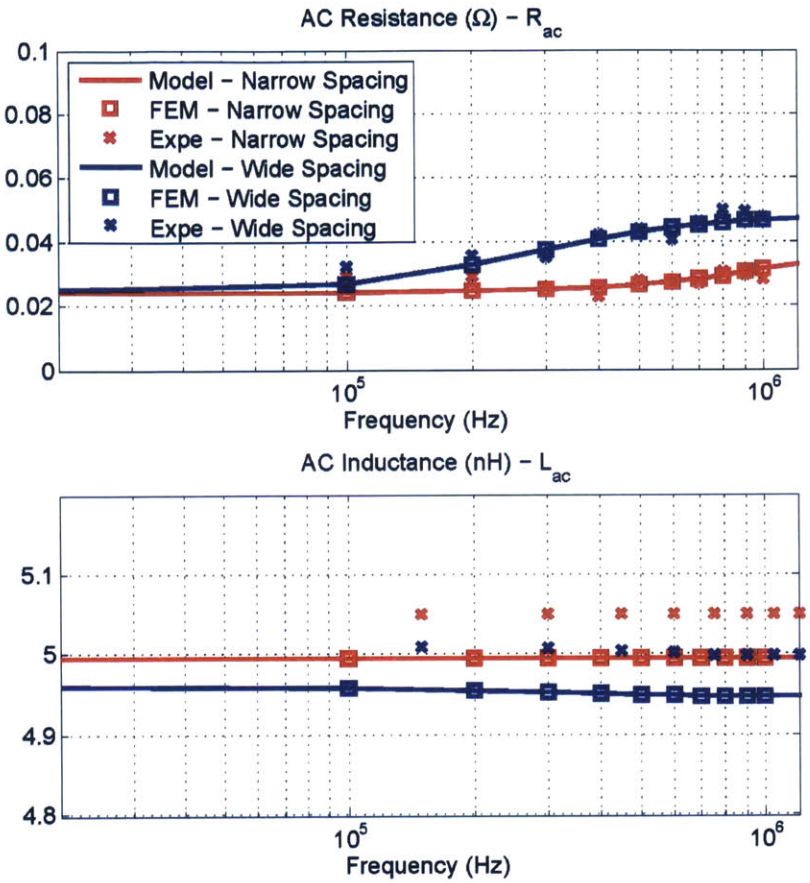


Figure 4-27: Comparing the R_{ac} and L_{ac} of the two single-turn inductors shown in Fig. 4-26 ("Narrow Spacing" and "Wide Spacing") based on the modeling results (Model), FEM simulations (FEM) and experimental measurements (Expe).

is all dropped by the secondary winding(s). If the windings are stacked vertically in a rectangular window, and they all occupy the full breadth of the winding window, the field will be uniform across the breadth of the window, and will only vary with the vertical dimension. In practice, the windings do not truly span the full breadth of the window. There is some spacing for electrical insulation, mechanical support, and/or manufacturing tolerance. Section 4.7.2(3-4) examines the effect of non-zero spacings in more detail. One example structure that doesn't perfectly satisfy the 1-D assumption but may require special attention is shown in Fig. 4-28a. The primary and secondary windings on the middle layer are positioned next to each other horizontally rather than being stacked vertically, resulting in a vertical field component, in addition to the horizontal field component produced by the windings on the bottom and top layers. Thus, the 1-D assumption fails.

Inductors may not satisfy the 1-D assumption as naturally. An air gap in the core will have curved "fringing" flux lines, and if conductors are in this region, the 1-D assumption does not hold (as shown in Fig. 4-28b). Furthermore, the orientation of the field depends on the position of the gap, even for regions of the window far from the gap. A low-permeability core (as shown in Fig. 4-28c) can be used for an inductor without needing a gap. This might seems to solve the problem and allow the 1-D assumption. However, the result includes concentric field lines near the center of the winding and additional field lines parallel to these further out and closer to the core. These vertical field lines are not captured by the 1-D model.

One way to achieve a good 1-D field in an inductor is to use a composite core with a low-permeability plate on one or two sides of the winding window, and with high-permeability material everywhere else as shown in Fig. 4-28d [126]. This situation can be approximated with multiple distributed gaps in place of the high permeability material, if the spacing from the winding to the gapped core (s_w) is adequate in comparison to the spacing between the gaps (s_g), as shown in Fig. 4-28e, discussed in Section 4.7.2(2) and [38]. With adequate spacing, although the flux distribution in the core region is not 1-D, it is possible to achieve an approximately 1-D field in the winding region with even just one or two gaps.

A common misconception is that a short gap length helps make the 1-D assumption accurate in an inductor with a gapped core, by minimizing fringing effects. In fact, discrepancies relative to the 1-D approximation are slightly reduced by a longer gap in a sufficiently high permeability core, as demonstrated in Fig. 7 in [38]. Although a short gap length does mean that the fringing flux is a smaller percentage of the total flux, the strength of the fringing flux for a giving winding current stays approximately constant, independent of gap length, in the region of the winding, if it is spaced well away from the gap. Very close to the gap, the field become more concentrated and causes more severe problems with a shorter gap than with a longer gap.

For transformers with significant magnetizing admittance (i.e., low magnetizing inductance), deliberately introduced with a gap or the use of a low-permeability core material, the 1-D assumption holds if the winding and gap configurations are both set up according to the considerations above, and are configured to produce field lines in the same axis, such that the one dimension to be analyzed is the same for both.

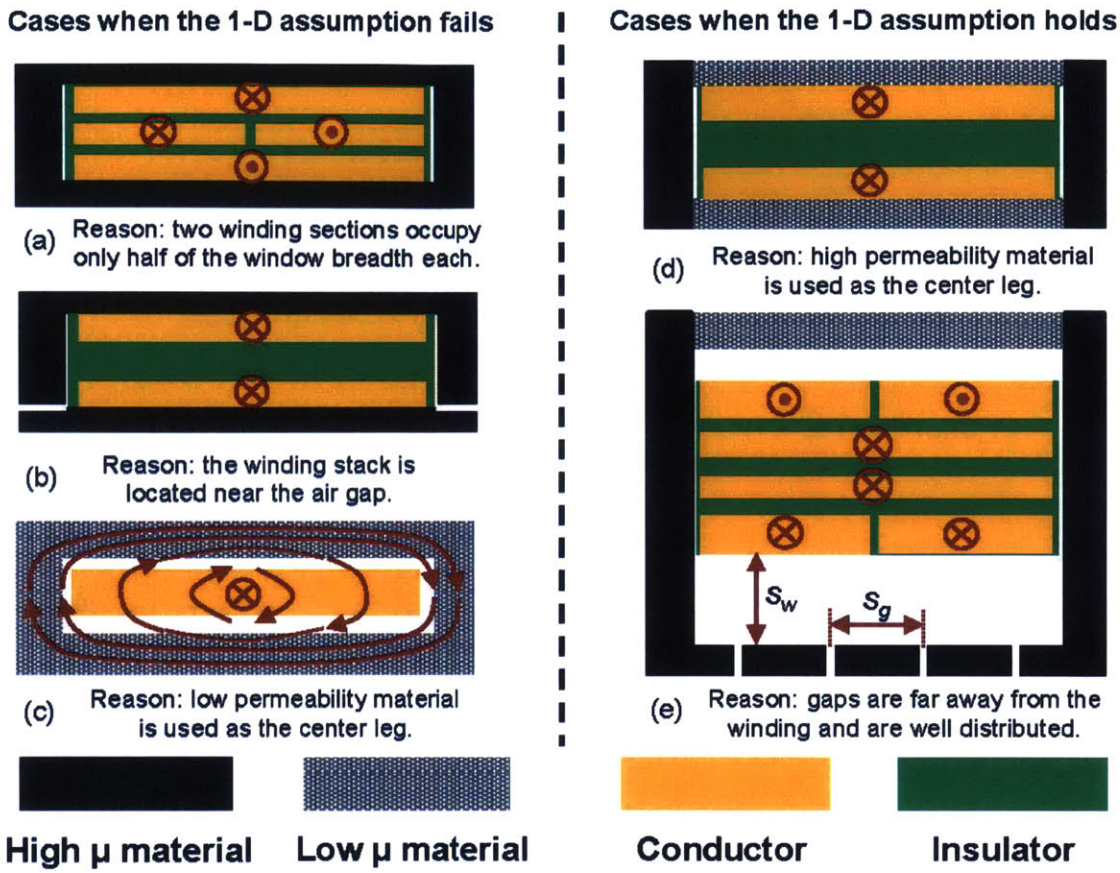


Figure 4-28: Example planar structures in which the 1-D assumption (a)-(c) fails, and (d)-(e) holds for different reasons.

4.7.2 Practical Considerations and Design Rules

Many practical designs may not fully satisfy the 1-D assumption. In some of these cases, the model is still highly accurate, while in others, the error would be unacceptable. Here we discuss some of these cases along with ways to address them, and present a few rules that can be used to empirically judge the satisfaction of the 1-D assumption. For cases that can be analyzed with 2-D methods, we present the mismatch between the modeling results and FEM simulations[5]. For cases that require 3-D analysis, we present the mismatch between the modeling results and experimental measurements.

1. *End effects*: As shown in Fig. 4-29a, in some core shapes, e.g., ELP cores, a portion of the conductor is not covered by the magnetic core. They no longer satisfy the 1-D

[5]The contributions of Mohammad Araghchini to the 2D modeling is gratefully acknowledged by the author.

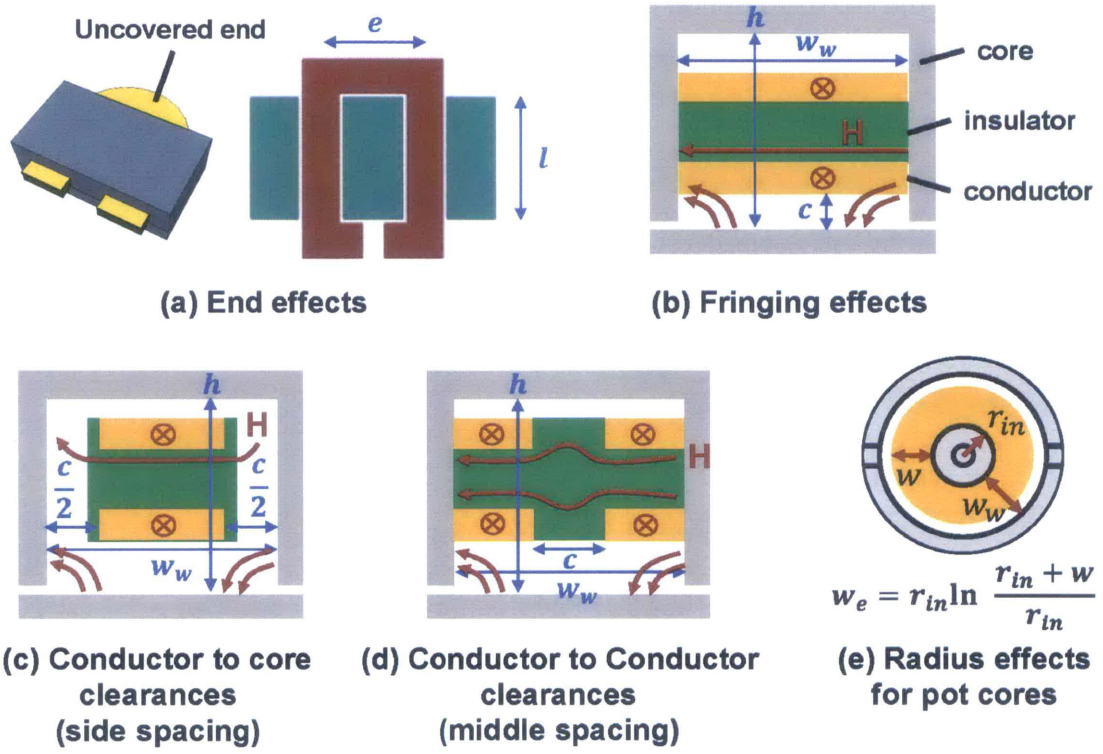
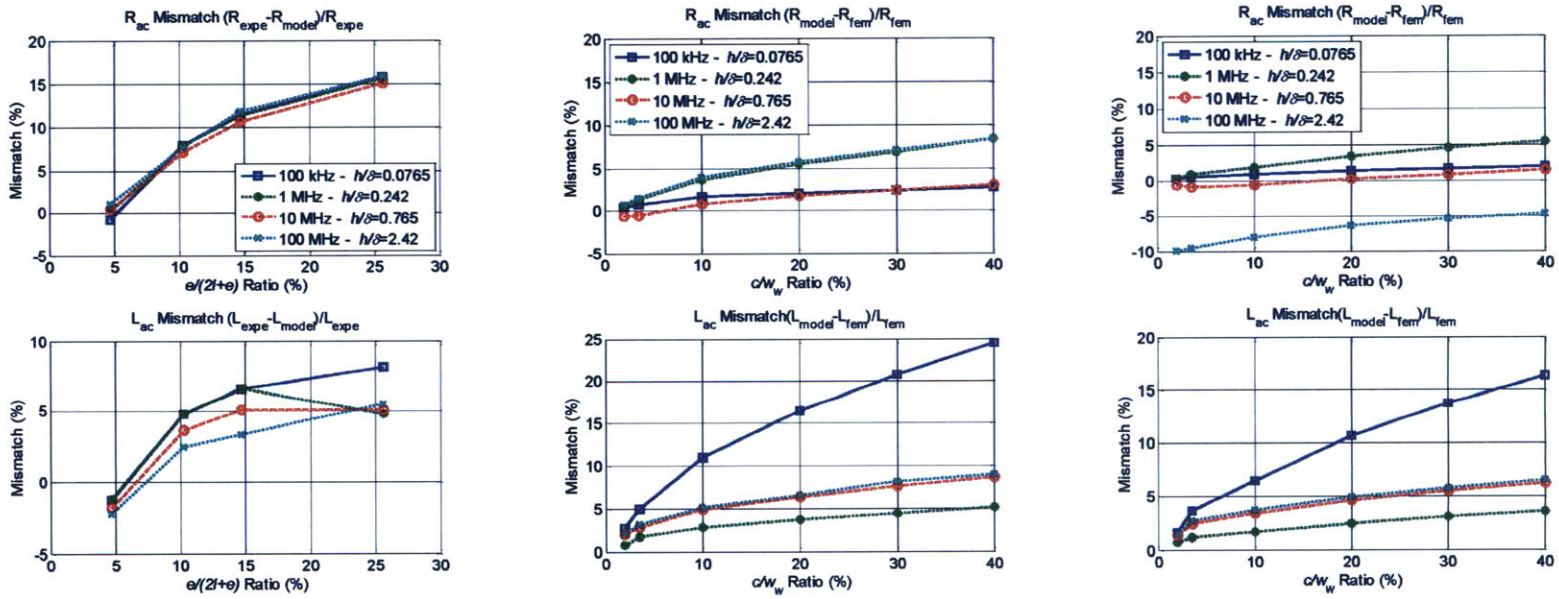


Figure 4-29: Five practical constraints that may cause prediction mismatch.

assumption but require 3-D analysis for full accuracy. We experimentally measured R_{ac} and L_{ac} in four 1:1 transformers with different numbers of cores (as shown in Fig. 4-11c) and compared them with results predicted by the model for different operating conditions. The mismatch as a function of the "uncovered-length to total-length" ratio $(e/(2l + e))$ and the "conductor-thickness to skin-depth" ratio (h/δ) are presented in Fig. 4-30a. The mismatch due to end effects does not have a strong dependence on frequency (i.e. h/δ ratio) but is a strong function of the $e/(2l+e)$ ratio. However, in this specific setup, as long as $e/(2l + e)$ is smaller than 25%, the mismatch in R_{ac} is under 15%, and the mismatch in L_{ac} is under 10%. The mismatch can be further reduced by separately calibrating the impedances of the uncovered ends in a way similar to modeling vias and interconnects.

2. *Fringing effects*: As shown in Fig. 4-29b, if conductor layers are placed near the air gap, fringing fields can penetrate the windings and change the current distribution, causing modeling mismatches (usually leading to underestimated conduction losses). This effect



(a) Mismatch between the modeling results and the experimental results as a function of the "*e/(2l+e)*" ratio for end effects.

(b) Mismatch between the modeling results and the FEM simulation results as a function of the "c/w_w" ratio for side spacing.

(c) Mismatch between the modeling results and the FEM simulation results as a function of the "c/w_w" ratio for middle spacing.

Figure 4-30: Mismatch between the modeling results and FEM (or experimental) results when considering (a) end effects (modeling v.s. experimental), (b) conductor-core clearances (modeling v.s. FEM), and (c) conductor-conductor clearances (modeling v.s. FEM). Mismatch is defined as the ratio of the difference between modeling and FEM (or experimental) results. Here h is the thickness of the copper layer (h is default to be half oz, 17.5 μm, in this chapter), and δ is the skin depth of the conductor depending on the operating frequency. In (b) and (c), since a portion of the conductor width is occupied by spacings, the w used in the model calculation is the modified effective conductor width $w = w_w - c$.

has been numerically analyzed in [38, 39], and it was recommended in [38] that the clearance (c) be at least 25% of the total window width w_w (i.e. gap to gap spacing) to limit the fringing effects.

3. *Conductor-core clearances (side spacing)*: As shown in Fig. 4-29c, clearances are required between conductors and pcb edges, and between pcb edges and the core. These clearances change the dissipated loss and stored reactive energy from a 2-D perspective. Figure 4-30b shows the mismatch between the model prediction and FEM results as a function of the "clearance to window-width" ratio (c/w_w), and the "conductor-thickness to skin-depth" ratio (h/δ) for the 1:1 transformers described in Section 4.6.1. Up to frequencies where h/δ equals 2.42 (this frequency is 100 MHz for half-oz copper), the mismatch of R_{ac} is less than 10% if c/w_w is smaller than 40%. For accurate estimation of L_{ac}, it is preferable if h/δ is below 1. Note, for half-oz copper (17.5 μm), the frequency when h/δ equals 1 is approximately 14 MHz, similar results are found in [129].

4. *Conductor-conductor clearances (middle spacing)*: As shown in Fig. 4-29d, clearances between two adjacent turns can also cause mismatches. Figure 4-30c shows the increase in mismatch as the c/w_w ratio increases. Up to frequencies when h/δ equals 2.42, the mismatch in R_{ac} is less than 10% if c/w_w is smaller than 40%. To achieve accurate estimation for L_{ac}, it is preferable if h/δ is below 1.

5. *Radius effects for pot cores*: Figure 4-29e shows a pot core whose window width (w_w) is comparable to its window inner radius (r_{in}). In this situation, the magnetic field and current distributions along the radius follows a "logarithmic" distribution similar to that described in [80, 110]. Assuming that the conductive layer fills the window width (i.e. $w = w_w$), this effect can be easily included in the lumped circuit model by replacing the layer width (w) in all impedance calculations with an effective width $w_e = r_{\text{in}} \ln(1 + \frac{w}{r_{\text{in}}})$ (Note: $\lim_{r_{\text{in}} \to +\infty} w_e = w$).

4.8 Summary of Chapter 4

This chapter presents a systematic approach to modeling impedances and current distribution in planar magnetics. The electromagnetic interactions in planar magnetics are clarified, organized and converted into a lumped circuit model under the 1-D and MQS assumptions. The lumped circuit model can be used to estimate the ac impedances, to determine cur-

rent sharing in parallel windings, and to extract parameters for impedance matrices and simplified circuit models, among many other uses. The proposed approach is tied with and verified by many existing theories, reexamining them from new perspectives and revealing their relationships. The modeling performance under a few practical constraints is investigated experimentally to clarify the boundaries of applicability. It is demonstrated that the approach performs very well in modeling commonly-used planar magnetics.

Chapter 5

Conclusion and Future Work

5.1 Thesis Roadmap

The rapid development of emerging power electronics applications places many requirements and challenges on power conversion circuit design. For example, solar micro-inverters have to achieve high power density, high efficiency across a wide operating range, good waveform quality, and long lifetime. Telecom power supplies have to be able to handle a wide input voltage range and be as small as possible with low profile. At the same time, recent developments in semiconductor devices offer many exciting design opportunities. With smaller footprints and lower parasitics and (potentially) lower cooling requirements, SiC and GaN power devices can provide superior power conversion performance than conventional silicon-based devices. Circuit topologies and architectures that can better utilize semiconductors and passive components, and can better meet the design requirements of modern system are needed. Novel magnetic devices and related design methods, that can facilitate sophisticated power conversion architectures and take advantage of the semiconductor device performance, are also important.

This thesis is developed in consideration of these emerging challenges and opportunities. Fig. 5-1 summaries the roadmap and contributions of this thesis. First, the thesis seeks to demonstrate that substantial advances can be made by appropriately splitting and combining functional blocks in conventional power conversion architectures, and by constructing new power conversion architecture using multiple basic circuit blocks. In particular, the thesis explores *merged-multi-stage* power conversion architectures using hybrid switched-capacitor/magnetics designs, to take advantages of new semiconductor devices, to better

utilize passive components, and to achieve improved system performance. The author also envisions that novel planar magnetics devices, whose impedances and current distribution can be analytically predicted and designed, may play key roles in future *merged-multi-stage* power conversion systems with complicated magnetic coupling relationships. The major contributions of this thesis are (1) two practical design implementations incorporating *merged-multi-stage* power conversion architectures; and (2) a systematic approach to modeling the impedances and current distribution in planar magnetics.

The development of this thesis is centered around a *hybrid switched-capacitor/magnetics* design approach. Switched-capacitor circuits naturally utilize semiconductor devices well, and take advantage of the higher energy density of capacitors as compared to magnetic devices. As is shown in the thesis, the multiple ac switching nodes in switched-capacitor circuits are suitable to be used as the ac voltage sources driving magnetically-coupled circuits. The parasitics/inductive-impedances of magnetically-coupled circuits can be utilized to create soft-switching opportunities. By appropriately combining switched-capacitor circuits with magnetically-coupled circuits, the advantages of each sub-circuit are well leveraged, while mutual-advantages can be created.

Through the design and implementation of a *multilevel energy buffer and voltage modulator (MEB)* – based dc-ac micro-inverter presented in Chapter 2, it is shown that by replacing a "single-function" component in a system with a "merged-multi-stage" circuit block that has multiple functions, the overall system performance can be improved without sacrificing the power density. As a specific example, the twice-line-frequency energy buffer capacitor in a dc-ac solar micro-inverter is replaced with a hybrid switched-capacitor and switched-inductor circuit block – the proposed MEB stage. The MEB significantly compresses the operation range of the high-frequency-link converter (a magnetically-coupled isolation stage), allowing higher efficiency to be achieved across a wide range (3.7% EU efficiency improvement). The MEB stage also functions as an active energy buffer that helps to reduce the requirement of the twice-line-frequency energy buffer capacitor size. Although it is more complicated, the overall volume of the MEB stage is comparable to the volume of the original energy buffer that it replaces.

Through the development of a wide input-voltage-range isolated MultiTrack dc-dc converter presented in Chapter 3, it is demonstrated that by splitting a centralized power conversion block into multiple distributed (but coupled) power conversion blocks, the over-

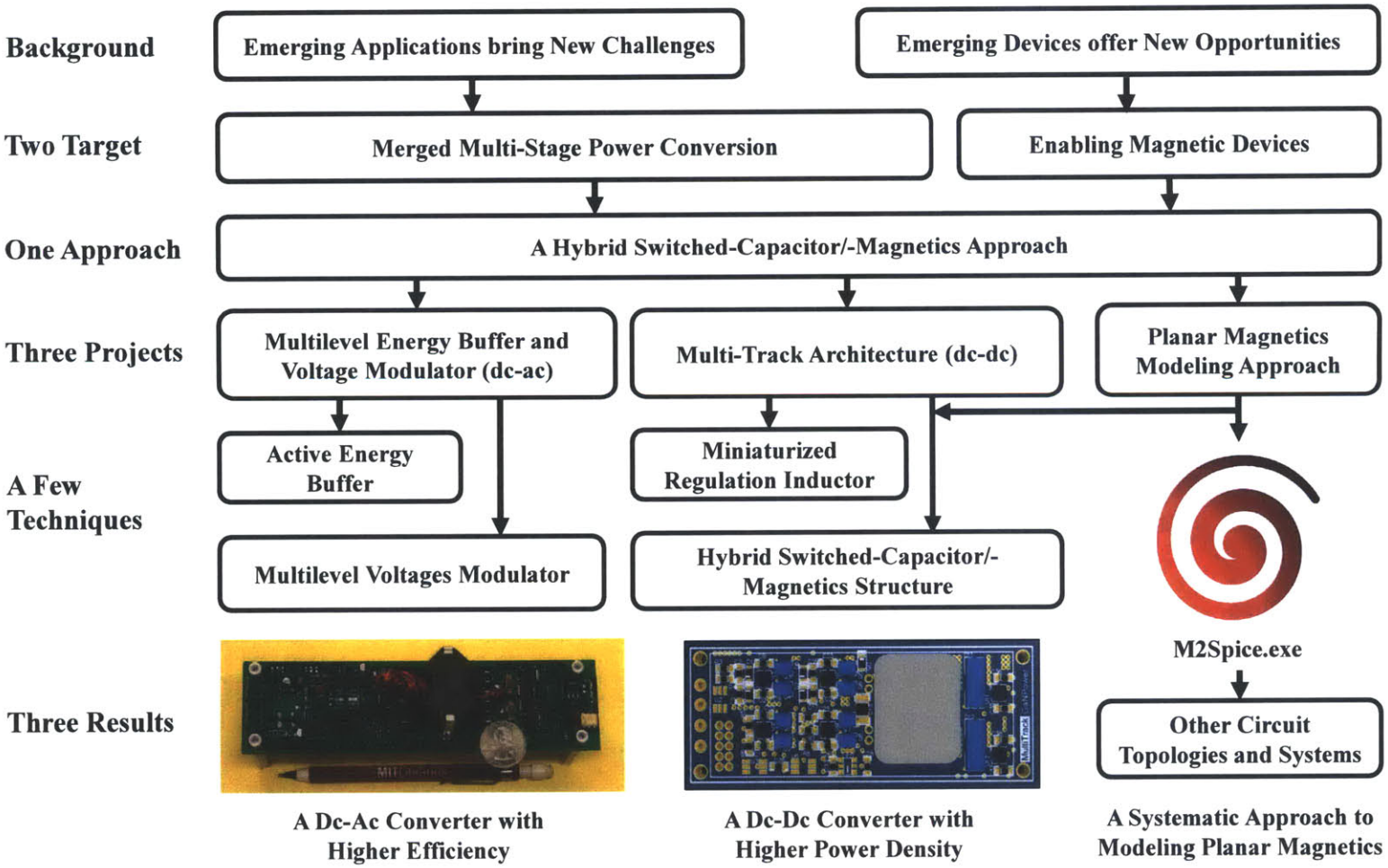


Figure 5-1: Thesis contributions and roadmap.

all system power density can be significantly improved without sacrificing efficiency. By splitting and merging the multiple stages in a multi-stage system, and operating them in different manners for different input voltage and output power, the advantages of *distributed power conversion architecture* can be leveraged, with additional advantages coming from the *hybrid switched-capacitor/magnetics* circuit structure. The prototyped 18 – 80 V input, 75 W, isolated dc-dc converter achieves over three times higher power density than state-of-the-art commercial products, benefits from better cooling, and maintains comparable best-in-class efficiency across the wide operation range.

Through the theoretical derivation and experimental verification of a systematic planar magnetic modeling approach, it is demonstrated that the impedance and current distribution of planar magnetic devices (which satisfy the MQS and 1-D assumption) can be well predicted and controlled. Compared to conventional previous analytical and/or numerical based approaches, the developed planar magnetics modeling approach is simpler, more effective and widely applicable to many magnetics designs. It can be very helpful in designing novel magnetic devices with sophisticated coupling relationships, opening up many opportunities in developing future "merged-multi-stage" power conversion architectures. A Python-based magnetics-to-SPICE-netlist conversion tool – *M2Spice* – has been developed and is being utilized in many practical designs.

5.2 Future Work

There are many potential future research topics that can be explored following the development of this thesis.

1. As mentioned in Chapter 2 and Appendix A, an ac side MEB stage could compress the output voltage range and power range of the high-frequency-link isolated converter in the schematic shown in Fig. 2-11. The high-frequency-link converter behaves much like a constant power dc-dc converter across the line cycle, promising significant performance improvement. The gate-drive and control circuitry in an ac side MEB stage would, however, be more sophisticated than those in a dc side MEB stage.

2. Besides voltage modulation and energy buffering, it is possible to integrate more micro-inverter system functions, such as reactive power compensation, and solar panel

maximum-power-point-tracking (MPPT), into the MEB stage presented in Chapter 2 to further enhance the system performance and/or reduce the system volume.

3. One promising research direction is to bring the merged multi-stage implementation presented in Chapter 3 (for 10s of volts and 10s of watts) to higher-voltage, higher-power applications, where passive components dominate the system volume and performance, and the marginal cost of more complicated gate drive and auxiliary circuitry is less important.

4. Given that the device-level advantages of the MultiTrack architecture have been theoretically demonstrated in Chapter 3, it would be interesting to realize/investigate/justify these advantages in a customized integrated-circuit (IC) design with appropriate device-level tradeoffs, i.e. on-resistances ($R_{\text{ds-on}}$), gate-to-source charge (Q_{gs}) and drain-to-source capacitance (C_{oss}).

5. It is discussed in Chapter 3 that the MultiTrack architecture can significantly reduce the common-mode current injection in the transformer. This effect is not critical in the 800 kHz prototype demonstrated in this thesis. It would be interesting to develop an appropriate implementation that functions at a higher switching frequency (e.g. 3 MHz – 10 MHz) to take advantage of this characteristic.

6. Finally, the development of the magnetic modeling approach in Chapter 4 and associated software package – *M2Spice* – offers a lot of exciting opportunities to investigate novel magnetic components for improved power electronics circuits.

Appendix A

Multilevel Energy Buffer and Voltage Modulator

A.1 Optimally Select the Switching Angles of the SCEB

The switching angles of the SCEB can be optimized for different design considerations. If a minimized voltage conversion range of the dc-ac converter is the goal, the v_x needs to step in pace with the line voltage as shown in Fig. 2-4b. Since we are using a series resonant converter, the amplitude $v_{P,env}$, is limited to $V_{IN} + v_{BUF}$. Therefore, if $v_{P,env}$ is modulated to be $v_{P,env}(\theta) = (V_{IN} + v_{BUF}) \sin(\theta)$, the difference between $v_{Y,env}(\theta)$ and $v_{P,env}(\theta)$ will be minimized, as shown in Fig. 2-5b. Furthermore, we can minimize this difference by making $v_{Y,env}(\theta)$ and $v_{P,env}(\theta)$ equal at $\theta = \alpha$ and at $\theta = \beta$. Hence, v_{BUF}, α and β satisfy the following two constraints:

$$\begin{cases} (V_{IN} + v_{BUF}) \sin(\alpha) = V_{IN} - v_{BUF} \\ (V_{IN} + v_{BUF}) \sin(\beta) = V_{IN} \end{cases} \tag{A.1}$$

The normalized difference between $v_{Y,env}(\theta)$ and $v_{P,env}(\theta)$, which must be minimized, can be quantified as $\frac{v_{Y,env}(\theta) - v_{P,env}(\theta)}{v_{P,env}(\theta)}$. From Fig. 2-5b it is easy to see that the maximum of this normalized difference can only occur at one of the following line angles: δ, α or β.

Hence, the optimization target, C, to be minimized is given by:

$$C = \max[\frac{V_{IN} - v_{BUF} - (V_{IN} + v_{BUF})\sin(\delta)}{(V_{IN} + v_{BUF})\sin(\delta)}, \frac{v_{BUF}}{(V_{IN} + v_{BUF})\sin(\alpha)}, \frac{v_{BUF}}{(V_{IN} + v_{BUF})\sin(\beta)}]. \tag{A.2}$$

Since $\alpha < \beta < \pi/2$, the second argument of (A.2) is greater than its third argument, i.e., $\frac{v_{BUF}}{(v_{IN}+v_{BUF})\sin(\alpha)} > \frac{v_{BUF}}{(v_{IN}+v_{BUF})\sin(\beta)}$. Hence, the normalized difference will be minimized when the first argument of (A.2) is equal to its second argument, i.e., when $\frac{V_{IN}-v_{BUF}-(V_{IN}+v_{BUF})\sin(\delta)}{(V_{IN}+v_{BUF})\sin(\delta)} = \frac{v_{BUF}}{(V_{IN}+v_{BUF})\sin(\alpha)}$. Using (A.1) to eliminate α from this equation yields:

$$v_{BUF}^2 - [2 + \sin(\delta)]V_{IN}v_{BUF} + [1 - \sin(\delta)]V_{IN}^2 = 0, \tag{A.3}$$

which can be solved for the optimal value of v_{BUF}:

$$v_{BUF} = \frac{V_{IN}[2 + \sin(\delta)] + V_{IN}\sqrt{[2 + \sin(\delta)]^2 - 4[1 - \sin(\delta)]}}{2}. \tag{A.4}$$

The optimal values of α and β can now be determined using (A.1), rewritten explicitly below:

$$\begin{cases} \alpha = \sin^{-1}(\frac{V_{IN}-v_{BUF}}{V_{IN}+v_{BUF}}) \\ \beta = \sin^{-1}(\frac{V_{IN}}{V_{IN}+v_{BUF}}). \end{cases} \tag{A.5}$$

With δ chosen as 6°, the optimal value of v_{BUF} is $0.6V_{IN}$, α is 12.8°, and β is 40.9°.

A.2 Calculate the Percentages of the Power Processed by the CCC

The average power over a line cycle processed by the CCC (P_{CCC}) can be calculated from the extra energy that must be delivered to C_{BUF} to maintain its charge balance:

$$\begin{aligned} P_{CCC} &= \frac{\int_{\beta}^{\pi-\beta} V_{BUF}I_{IN}\sin(\theta)d\theta - 2\int_{\delta}^{\alpha} V_{BUF}I_{IN}\sin(\theta)d\theta}{\pi} \\ &= \frac{2V_{BUF}I_{IN}[\cos(\alpha) + \cos(\beta) - \cos(\delta)]}{\pi}. \end{aligned} \tag{A.6}$$

Here I_{IN} is the amplitude of the envelope of the input current of the dc-ac converter block. The fraction of line cycle average output power ($P_{OUT(avg)} = \frac{2V_{IN}I_{IN}\cos(\delta)}{\pi}$) processed by the

CCC is given by:

$$\gamma_{CCC} = \frac{P_{CCC}}{P_{OUT(avg)}} = \frac{V_{BUF}[\cos(\alpha) + \cos(\beta) - \cos(\delta)]}{V_{IN}\cos(\delta)}. \tag{A.7}$$

With $v_{BUF} = 0.6V_{IN}$, $\delta = 6°$, $\alpha = 12.8°$, and $\beta = 40.9°$, γ_{CCC} equals 44.43%. Hence, only 44.43% of the average output power is processed by the CCC. Since the SCEB is switched at a low frequency (240 Hz for a 60Hz line frequency), its switching loss is negligible compared to that of the CCC. Therefore, assuming the efficiency of the CCC circuit is η_{CCC}, and neglecting the losses in the SCEB, the efficiency of the MEB architecture is:

$$\eta_{MEB} = \frac{P_{OUT(avg)}}{P_{OUT(avg)} + P_{Loss,CCC}} = \frac{1}{1 + \gamma_{CCC}(1 - \eta_{CCC})}. \tag{A.8}$$

This shows that the loss caused by the CCC circuit only penalizes the energy passing through the CCC in the MEB architecture. This allows the MEB based micro-inverter architecture to have a higher efficiency than conventional two-stage architectures.

With the SCEB controlled as described above, the peak power rating of the CCC, $P_{CCC,peak}$, is 97.7% of the line cycle average output power of the micro-inverter, $P_{OUT(avg)}$. Hence, the peak power rating of the CCC is only 48.8% of the peak power rating of the micro-inverter (itself equal to $2P_{OUT(avg)}$). The CCC can be made extremely small and highly efficient since it has a fixed and reasonably small input to output voltage conversion ratio (0.4 : 1), processes only a portion of the total energy and can be switched at a relatively high switching frequency.

A.3 Operation of the MEB Stage without the CCC

To eliminate the requirement of the CCC, the average current of C_{BUF} needs to be zero over the line cycle. C_{BUF} is charged when the line voltage is low ($\theta \in [0°, \alpha] \cup [180° - \alpha, 180°]$), and is discharged when the line voltage in high ($\theta \in [\beta, 180° - \beta]$). Assume the dc-ac converter draws sinusoidal input current, the charge balance relationship of C_{BUF} is:

$$\int_{\delta}^{\alpha} I_{GRID} sin(\theta)\, d(\theta) = \int_{\beta}^{\frac{\pi}{2}} I_{GRID} sin(\theta)\, d(\theta) \tag{A.9}$$

thus:

$$cos(\alpha) + cos(\beta) = cos(\delta) \tag{A.10}$$

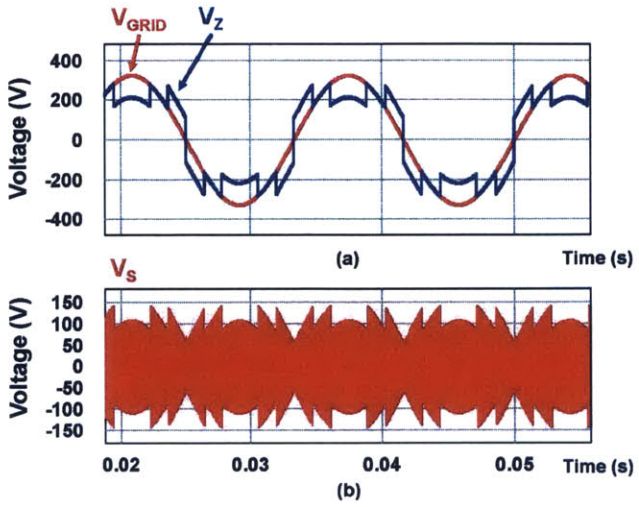


Figure A-1: Simulated waveforms for the MEB micro-inverter with the MEB stage on the ac side for $V_{\mathrm{GRID}} = 230$ V rms and $V_{\mathrm{BUF}} = 106$ V. (a) Line voltage V_{GRID} and the synthesized voltage v_{Z}. (b) the voltage at the transformer secondary, v_{S}. The amplitude variation of v_{S} over the line cycle has been significantly reduced.

A.4 MEB Stage on the AC Side

At the overall system level, an alternative implementation of the MEB micro-inverter can have the MEB stage on the ac side instead of the dc side. An example schematic of this implementation is shown in Fig. A-2. The MEB stage of this implementation also has SCEB and CCC. The difference is that the SCEB is split into two parts to facilitate connection with the grid. In this implementation, instead of synthesizing an approximated replica of the ac line voltage amplitude from the dc input, the MEB stage synthesizes an approximately constant voltage amplitude from the ac line. Hence, it also reduces the voltage conversion range of the high-frequency portion of the system. An example implementation with an ac-side MEB is shown in Fig. A-2. In this implementation, the MEB stage is combined with the cycloconverter. The full-bridge SCEB is split into two half-bridge versions for ease of interfacing with the ac line. the twice-line-frequency energy is now substantially buffered by $\mathrm{C_A}$ and $\mathrm{C_B}$, allowing the use of a much smaller $\mathrm{C_{IN}}$. In each half-line-cycle, $\mathrm{L_C}$, $\mathrm{C_C}$, and two MOSFETs ($\mathrm{Q_A}$&$\mathrm{Q_B}$, or $\mathrm{Q_C}$&$\mathrm{Q_D}$, depending on the half-line-cycle) function as the CCC, maintaining the voltage across $\mathrm{C_A}$ and $\mathrm{C_B}$. Figure A-1 shows the simulated waveforms of the MEB micro-inverter with the MEB stage on the ac side. Owing to the MEB stage, the amplitude variation of v_{Z} and v_{S} are significantly reduced.

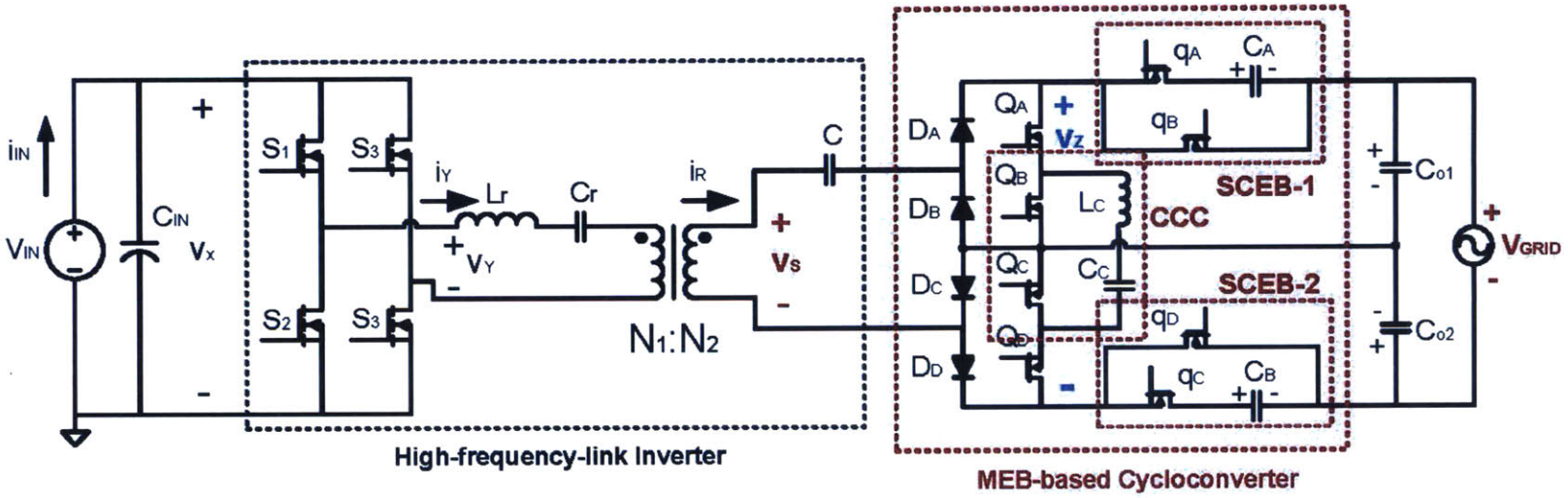


Figure A-2: A MEB micro-inverter with an ac-side MEB. The MEB stage in this implementation is combined with the cycloconverter. When v_{GRID} is in the positive half cycle, Q_C and Q_D are kept on. In this condition, if v_{GRID} is low, q_A and q_D are turned on to step-up the voltage seen by the rectifier; Q_A, Q_B and L_C charge C_C to reduce the current flow into the grid. If v_{GRID} is moderate, q_B and q_D are turned on to bypass C_A and C_B, and Q_A and Q_B are kept off. If v_{GRID} is high, q_B and q_C are switched on to step-down the voltage seen by the rectifier; Q_A, Q_B and L_C discharge C_C to inject more current into the grid. When v_{GRID} is in the negative half cycle, Q_A and Q_B are kept on, and the circuit operates in a symmetric manner to the one described above.

A.5 Bill of Materials (BOM)

Table A.1: Bill of Materials (BOM) of the MEB micro-inverter. Resistances and capacitances are not shown. Unused components with their pads placed on the board are not shown. Information about some critical components is also listed in Table 2.2

Designator	Comment	Device	Package
5VDC1	Isolated 5V Dc/Dc	RI0505S	RI0505S
5VDC2	Isolated 5V Dc/Dc	RI0505S	RI0505S
AND1	AND Gate	SN74LVC1G08	DCKR-PDSO-G5
AND2	AND Gate	SN74LVC1G08	DCKR-PDSO-G5
BUFF1	Signal Buffer	BUFF	SOT23-6
BUFF2	Signal Buffer	BUFF	SOT23-6
D1	Diode	STTH1R06DIODE	DO214AC
D2	Diode	STTH1R06DIODE	DO214AC
DAC2	DAC for Gating	AD558	PLCC20
DAC2CON	Signal Connector	MICROMATCH-8	MICROMATCH-8
DE	Diode	PMEG2005EB	SOD523
DF	Diode	PMEG2005EB	SOD523
DELAY7	Programmable Delay Chip	LTC6994	SOT23-6
DELAY8	Programmable Delay Chip	LTC6994	SOT23-6
DELAY9	Programmable Delay Chip	LTC6994	SOT23-6
DELAY10	Programmable Delay Chip	LTC6994	SOT23-6
DELAYA	Programmable Delay Chip	LTC6994	SOT23-6
DELAYB	Programmable Delay Chip	LTC6994	SOT23-6
DELAYC	Programmable Delay Chip	LTC6994	SOT23-6
DELAYD	Programmable Delay Chip	LTC6994	SOT23-6
DELAYZC	Programmable Delay Chip	LTC6994	SOT23-6
DIGIISO	Opto Isolator	SI8410	SOIC8
DIGIISO1	Opto Isolator	SI8410	SOIC8
DIGIISO2	Opto Isolator	SI8410	SOIC8
GD1	Input Side Gate Driver	LM5113D	LLP10
GD2	Input Side Gate Driver	LM5113D	LLP10
GD3	Input Side Gate Driver	LM5113D	LLP10
GD4	Input Side Gate Driver	LM5113D	LLP10
GD5	Input Side Gate Driver	LM5113D	LLP10
GDHB1	Output Side Gate Driver	FAN7390GD	SO08
GDHB2	Output Side Gate Driver	FAN7390GD	SO08
INV	Digital Inverter	INVSC70	SC70-5L
INV1	Digital Inverter	INVSC70	SC70-5L
OD1	Output SiC Diode	CREE CSD01060	DO214AC
OD2	Output SiC Diode	CREE CSD01060	DO214AC

OD3	Output SiC Diode	CREE CSD01060	DO214AC
OD4	Output SiC Diode	CREE CSD01060	DO214AC
ORA	OR Gate	SN74LVC1G08	DCKR-PDSO-G5
ORB	OR Gate	SN74LVC1G08	DCKR-PDSO-G5
ORC	OR Gate	SN74LVC1G08	DCKR-PDSO-G5
ORD	OR Gate	SN74LVC1G08	DCKR-PDSO-G5
SW1	Input Side Switch	EPC2001	EPC2015DIE
SW2	Input Side Switch	EPC2001	EPC2015DIE
SW2INV	Digital Inverter	INVSC70	SC70-5L
SW3	Input Side Switch	EPC2001	EPC2015DIE
SW4	Input Side Switch	EPC2001	EPC2015DIE
SW4INV	Digital Inverter	INVSC70	SC70-5L
SW5	Input Side Switch	EPC2001	EPC2015DIE
SW6	Input Side Switch	EPC2001	EPC2015DIE
SW7	Input Side Switch	EPC2001	EPC2015DIE
SW8	Input Side Switch	EPC2001	EPC2015DIE
SW9	Input Side Switch	EPC2001	EPC2015DIE
SW10	Input Side Switch	EPC2001	EPC2015DIE
SWA	Output Side Rectifier Switch (not used)	IPD65R380C6	TO252
SWB	Output Side Rectifier Switch (not used)	IPD65R380C6	TO252
SWC	Output Side Rectifier Switch (not used)	IPD65R380C6	TO252
SWD	Output Side Rectifier Switch (not used)	IPD65R380C6	TO252
SWE	Output Side 60Hz Switch	IPD65R380C6	TO252
SWF	Output Side 60Hz Switch	IPD65R380C6	TO252
U2	Inductor from Enphase	L-ENPHASE	
U3	CCC-Inductor	L-WE	
U4	Linear Regulator	MIC5239	SOT223
U5	Linear Regulator	MIC5239	SOT223
U14	Opto-coupler	4N35	SMD6
U15	Transformer	RM12	RM12T1
U16	LTC6992	PWM generator	SOT23-6

A.6 Schematics

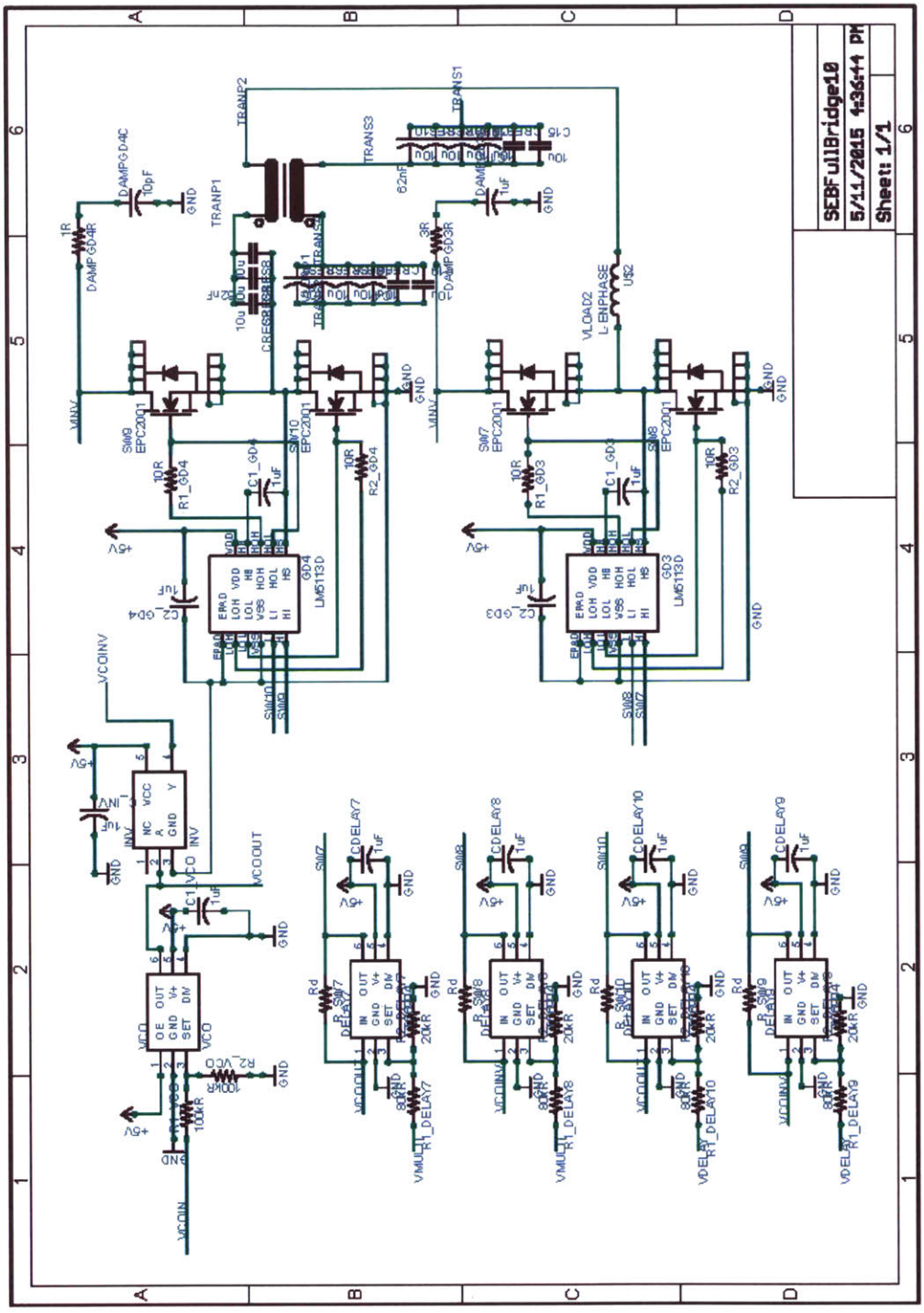


Figure A-3: Schematic of the MEB Micro-inverter (Part 1).

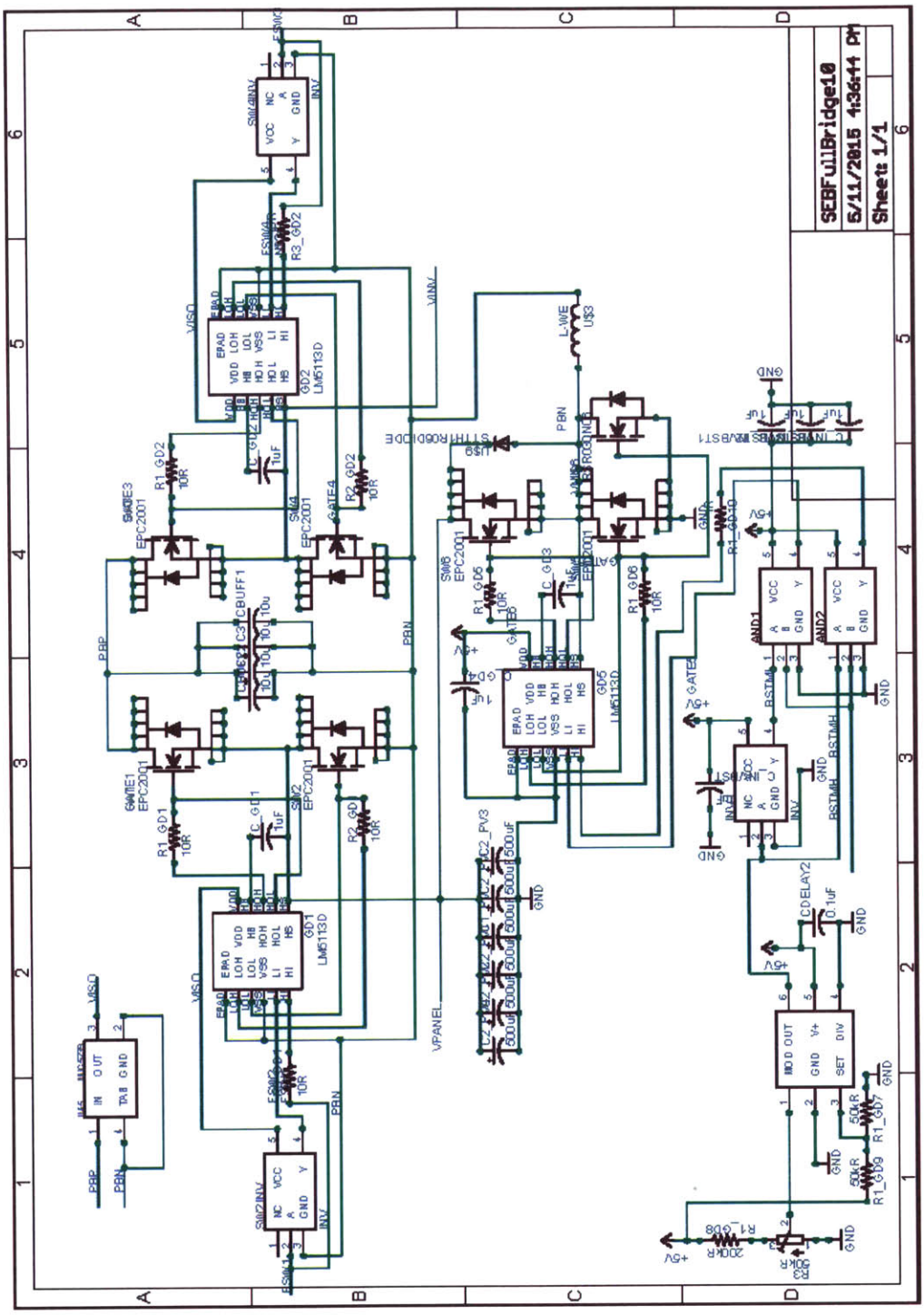


Figure A-4: Schematic of the MEB Micro-inverter (Part 2).

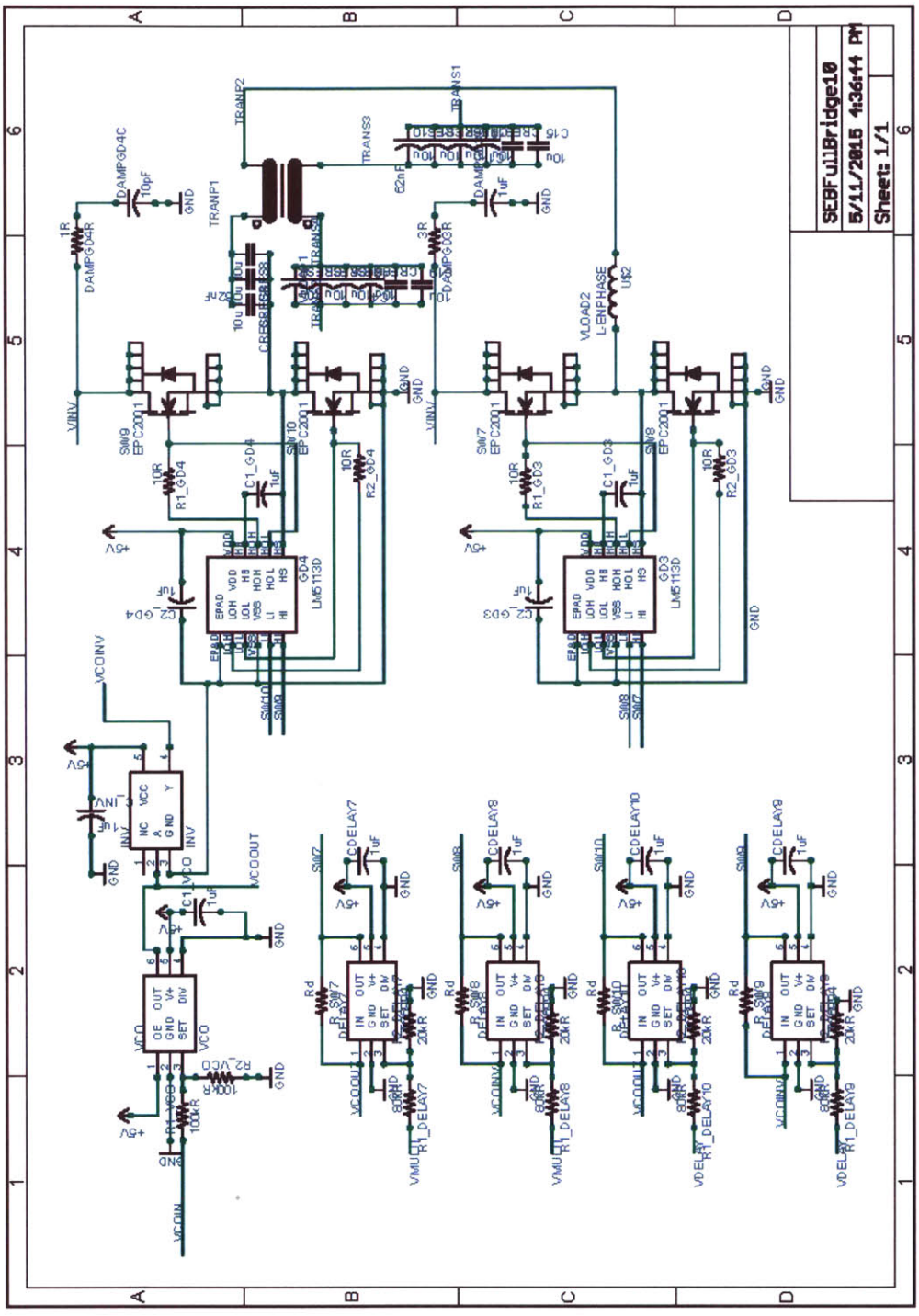


Figure A-5: Schematic of the MEB Micro-inverter (Part 3).

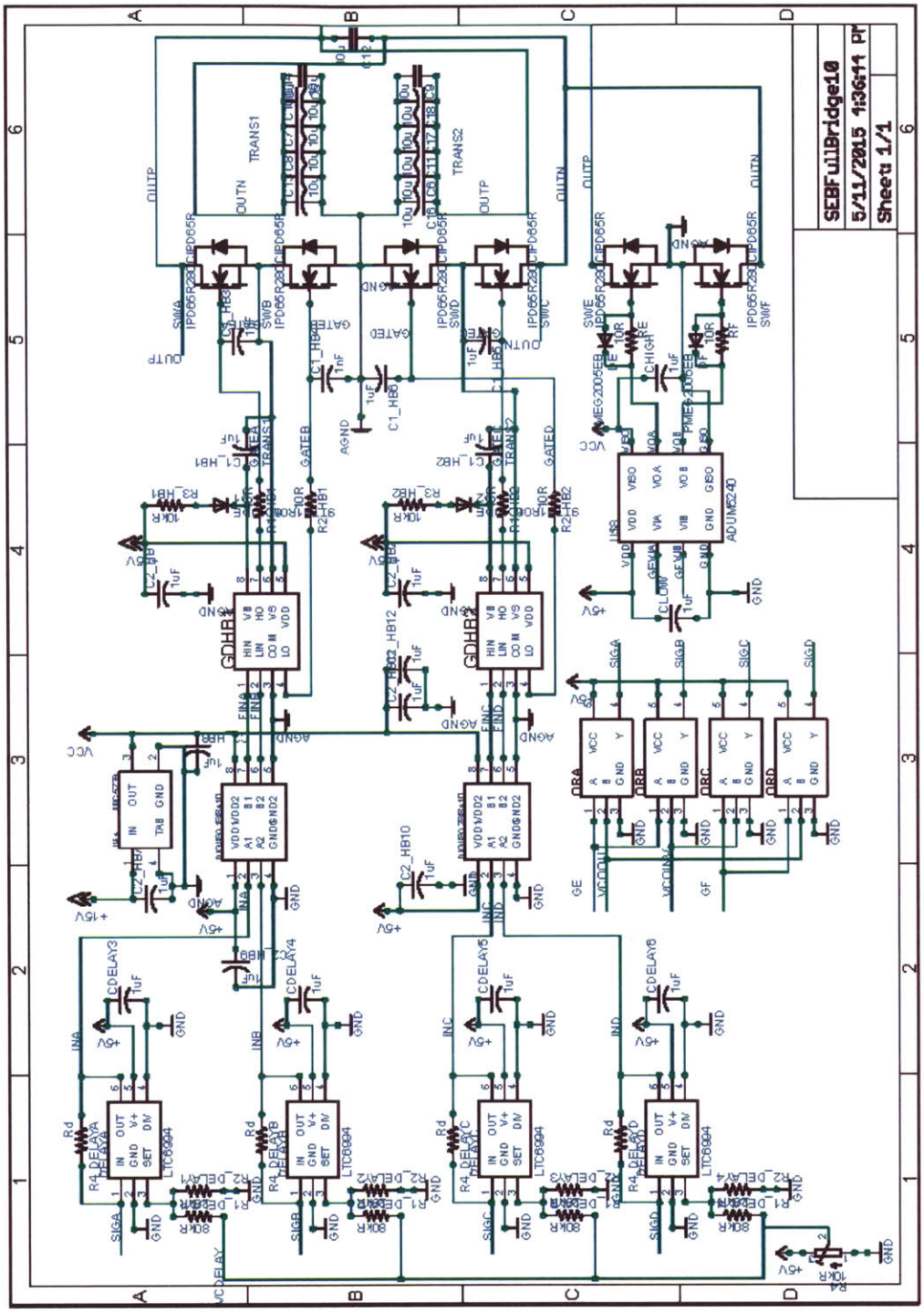
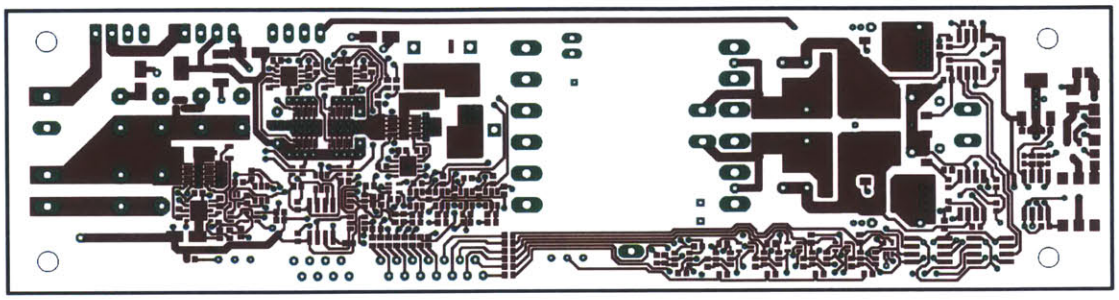
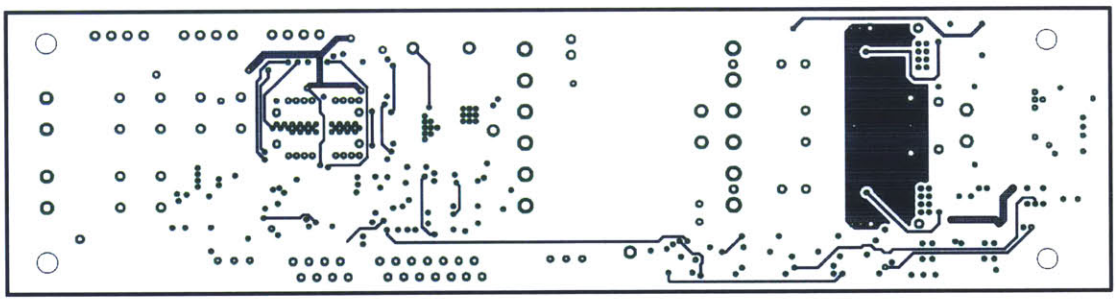


Figure A-6: Schematic of the MEB Micro-inverter (Part 4).

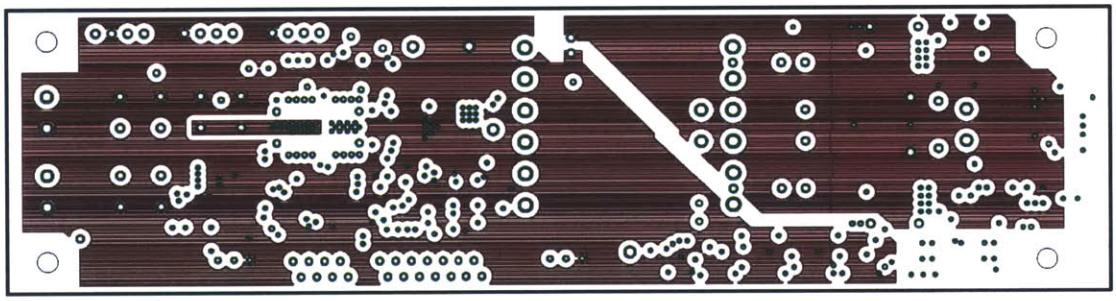
A.7 PCB Layouts



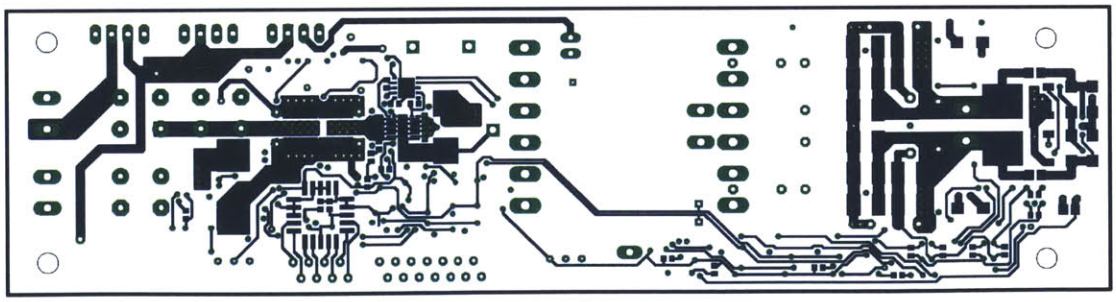
(a)



(b)



(c)



(d)

Figure A-7: Layers 1-4 of the MEB micro-interter PCB.

Appendix B

MultiTrack Power Conversion Architecture

B.1 Inductor Energy Buffering Ratio (Γ_E)

In the MultiTrack architecture, the full input voltage range is split by the n intermediate bus voltages ($V_{\mathrm{Xk}} = \frac{k}{n}V_{\max}$, k=1, ..., n) into n voltage domains. The inductor energy buffering ratio Γ_E is a piecewise function of the input voltage v_{in}. When v_{in} locates in the k-th voltage sub-section ($\frac{k-1}{n}V_{\max}<v_{\mathrm{in}}<\frac{k}{n}V_{\max}$), the regulation circuit can be modeled as a direct converter having v_{in} as the input voltage level, and $\frac{k-1}{n}V_{\max}$ and $\frac{k}{n}V_{\max}$ as the two output voltage levels, as illustrated in Fig. B-1a. Fig. B-1b shows the inductor current i_{R} assuming the converter works in critical continuous-conduction-mode (CCM)[1]. The average current of i_{R} is I_{avg}, and the peak current of i_{R} is $I_{\mathrm{pk}} = 2I_{\mathrm{avg}}$. The switching period is T_{sw}. The total energy that is processed by this circuit in each switching cycle is

$$E_{total} = v_{\mathrm{in}} \times I_{\mathrm{avg}} \times T_{\mathrm{sw}} = \frac{1}{2}V_{\mathrm{in}}I_{\mathrm{pk}}T_{\mathrm{sw}}. \tag{B.1}$$

The inductance value that allows the critical CCM operation is

$$L_{\mathrm{R}} = \frac{(V_{\mathrm{X}} - v_{\mathrm{in}})d_{\mathrm{X}}T_{\mathrm{sw}}}{I_{\mathrm{pk}}} = \frac{(V_{\mathrm{X}} - v_{\mathrm{in}})(v_{\mathrm{in}} - V_{\mathrm{Y}})T_{\mathrm{sw}}}{I_{\mathrm{pk}}(V_{\mathrm{X}} - V_{\mathrm{Y}})}. \tag{B.2}$$

[1] In critical CCM mode, the inductor is fully charged and discharged, yield the highest inductor utilization ratio.

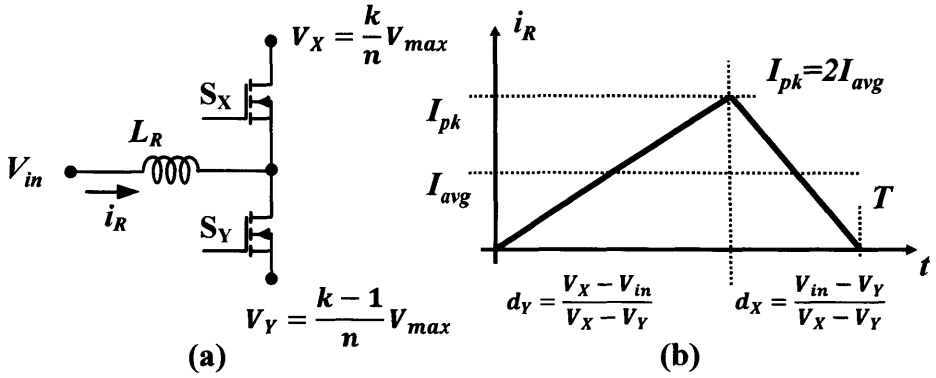


Figure B-1: The regulation circuit can be treated as a indirect converter having V_{in}, V_{X} and V_{Y} as the three nodal voltages.

The peak energy that is buffered in the inductor L_{R} is

$$E_{L_{\text{R}}} = \frac{1}{2} L_{\text{R}} I_{\text{pk}}^2 = \frac{1}{2} \frac{(V_{\text{X}} - v_{\text{in}})(v_{\text{in}} - V_{\text{Y}}) T_{\text{sw}} I_{\text{pk}}}{(V_{\text{X}} - V_{\text{Y}})}. \tag{B.3}$$

The percentage of energy that is buffered in the inductor when v_{in} belongs to $\frac{k-1}{n} V_{\text{max}} \leftrightarrow \frac{k}{n} V_{\text{max}}$ region, Γ_E, is

$$\begin{aligned} \Gamma_{\text{E,n-track}|\frac{k-1}{n}V_{\text{max}} < v_{\text{in}} < \frac{k}{n}V_{\text{max}}]} &= \frac{E_{L_{\text{R}}}}{E_{total}} \\ &= \frac{(V_{\text{X}} - v_{\text{in}})(v_{\text{in}} - V_{\text{Y}})}{(V_{\text{X}} - V_{\text{Y}})} \\ &= \frac{\left(\frac{k}{n} V_{\text{max}} - v_{\text{in}}\right)\left(v_{\text{in}} - \frac{k-1}{n} V_{\text{max}}\right)}{\frac{1}{n} V_{\text{max}} v_{\text{in}}}, \end{aligned} \tag{B.4}$$

By taking the derivative of Γ_E relative to v_{in}, it can be calculated that in each voltage sub-section, Γ_E reaches the local maximum when v_{in} equals the geometrical mean of the two adjacent intermediate voltages

$$v_{\text{in}} = \sqrt{V_{\text{X}} V_{\text{Y}}} = \sqrt{k(k-1)} \frac{V_{\text{max}}}{n}. \tag{B.5}$$

When $k > 1$, the maximum Γ_E when v_{in} locates in the k-th voltage domain is

$$\begin{aligned} &\max(\Gamma_{\text{E,n-track}|\frac{k-1}{n}V_{\text{max}} < v_{\text{in}} < \frac{k}{n}V_{\text{max}}]}) \\ &= \frac{\sqrt{\frac{k}{n} V_{\text{max}}} - \sqrt{\frac{k-1}{n} V_{\text{max}}}}{\sqrt{\frac{k}{n} V_{\text{max}}} + \sqrt{\frac{k-1}{n} V_{\text{max}}}} = \frac{\sqrt{k} - \sqrt{k-1}}{\sqrt{k} + \sqrt{k-1}}. \end{aligned} \tag{B.6}$$

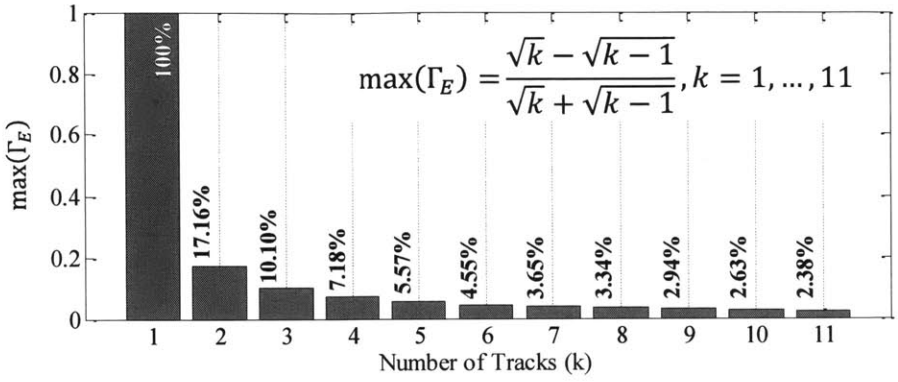


Figure B-2: Local maximum of Γ_E when v_{in} belongs to a subsection of the input voltage range. For example, for a 3-Track system, the three local maximum Γ_Es in the three subintervals - $[0, \frac{1}{3}V_{\text{max}}]$, $[\frac{1}{3}V_{\text{max}}, \frac{2}{3}V_{\text{max}}]$, $[\frac{2}{3}V_{\text{max}}, V_{\text{max}}]$ - are 100%, 17.16%, and 10.10%, respectively. This chart can be used to rapidly recreate Fig. 3-9 and Fig. 3-10.

Table B.1: Maximum Γ_E as a function of the input voltage range and the number of tracks in the MultiTrack architecture. Γ_E is the percentage of energy stored in the regulation inductor in each switching cycle.

$\frac{V_{\text{max}}}{V_{\text{min}}}$	1-Track	2-Track	4-Track	6-Track	8-Track	10-Track
2	50%	17.2%	10.1%	7.2%	5.6%	4.6%
4	75%	50%	17.2%	16.7%	10.1%	10.1%
6	83.4%	66.6%	33.3%	17.2%	17.2%	13.5%
8	87.5%	75%	50%	25%	17.2%	17.2%
10	90%	80%	60%	40%	20%	17.2%

White: adding more tracks would bring major inductor-size reduction;
Grey: adding more tracks would bring marginal inductor-size reduction;
Dark: adding more tracks would bring minor inductor-size reduction;

The results of this equation are plotted in Fig. B-2 as a list of values related to k. Fig. B-2 can be utilized to rapidly re-create Fig. 3-9. For example, according to Fig. 3-9, the six local maximum Γ_E of a 6-Track converter are 100%, 17.16%, 10.10%, 7.18%, 5.57%, and 4.55%, respectively. This six values are listed as the six values on the left side of Fig. B-2.

Fig. 3-10 can be presented in a different format as shown in Table B.1. $\max(\Gamma_E)$=17.2% can be utilized as an indicator for the saturation of marginal advantages. The minimum $v_{\text{in}}/V_{\text{max}}$ value that

When $k = 1$, the maximum $\Gamma_{E,1-track}$ is

$$\max(\Gamma_{\mathrm{E,1-track}}|_{v_{\mathrm{in}}\in[V_{\mathrm{min}},V_{\mathrm{X}}]}) = 1 - n\frac{V_{\mathrm{min}}}{V_{\mathrm{max}}}. \tag{B.7}$$

Utilizing Eq. B.6 and Eq. B.7, the threshold number of tracks, n_{th}, discussed in the *MultiTrack Design Guideline #1* in Chapter 3 is achieved when

$$1 - n_{th}\frac{V_{\mathrm{min}}}{V_{\mathrm{max}}} = \frac{\sqrt{2}-1}{\sqrt{2}+1}. \tag{B.8}$$

And thus

$$\frac{V_{\mathrm{max}}}{V_{\mathrm{min}}} = \frac{\sqrt{2}+1}{2}n_{th}. \tag{B.9}$$

In a boost-based two-stage (BTS) converter with an input voltage range $V_{\mathrm{min}}<v_{\mathrm{in}}<V_{\mathrm{max}}$, if the intermediate voltage is selected as V_{max}, the converter can be treated as a 1-track converter with $n = 1$ and $k = 1$. According to Eq. B.4, the Γ_E of a BTS converter is

$$\Gamma_{\mathrm{E,BTS}}|_{v_{\mathrm{in}}\in[V_{\mathrm{min}},V_{\mathrm{max}}]} = 1 - \frac{v_{\mathrm{in}}}{V_{\mathrm{max}}}, \tag{B.10}$$

which is a linear function of the input voltage as plotted in Fig. 3-9. Γ_E equals zero when the input voltage equals V_{max} (no voltage conversion), and reaches the maximum when the input voltage approaches the minimum V_{min} (i.e. the converter has the highest voltage conversion ratio). The maximum Γ_E in the V_{min} to V_{max} range is

$$\max(\Gamma_{\mathrm{E,buck}}|_{v_{\mathrm{in}}\in[V_{\mathrm{min}},V_{\mathrm{max}}]}) = 1 - \frac{V_{\mathrm{min}}}{V_{\mathrm{max}}}. \tag{B.11}$$

B.2 Transformer Parameter Extraction

The geometry file of the Planar Magnetics used in the MultiTrack prototype is shown below. The geometry information about the two foil layers on top and bottom of the PCB is estimated. This geometry file can be processed by the *M2Spice* presented in Appendix D.

```
Ac = 19.9e-6
gt = 0.33e-4
lindex = [2,1,1,2,2,2,2,3,3,2]
mus = [1.2e-6,1.2e-6,1.2e-6,1.2e-6,1.2e-6,...
1.2e-6,1.2e-6,1.2e-6,1.2e-6,1.2e-6,1.2e-6]
mur = 1000
nwinding = 3
h = [0.071e-3,0.071e-3,0.071e-3,0.071e-3,0.071e-3,...
,0.071e-3,0.071e-3,0.071e-3,0.071e-3,0.071e-3]
f = 800000
m = [1,2,2,1,1,1,1,2,2,1]
c = 1.1e-3
sigmac = [5.8e7,5.8e7,5.8e7,5.8e7,5.8e7, 5.8e7, 5.8e7, 5.8e7,5.8e7, 5.8e7]
s = [0.2e-3,0.2e-3,0.12e-3,0.10e-3,0.14e-3,...
0.10e-3,0.14e-3,0.10e-3,0.12e-3,0.2e-3,0.2e-3]
wstyle = [0,1,0]
gb = 0.33e-4
w = [3e-3,3e-3,3e-3,3e-3,3e-3,3e-3,3e-3,3e-3,3e-3,3e-3]
x = Prototype
nlayer = 10
d = 18e-3
```

Here is the netlist file generated by *M2Spice* using the previous provided geometry information. This netlists file can be utilized as a sub-circuit in SPICE (e.g. LTspice) to run open- and short-circuit simulations. Element values in a lumped circuit model can be extracted by these open- and short-circuit simulations.

```
*NetList for Layer 1
Le1 N1 P1 1 Rser=1f
Li1 G Md1 1 Rser=1f
Lg1 Mg1 Md1          -79.76p Rser=1f
```

```
Rg1 Mc1 Mg1        1333.67u
Rt1 Mc1 Mt1         177.98u
Rb1 Mb1 Mc1         177.98u
Lt1 T1 Mt1         242.26p Rser=1f
Lb1 Mb1 B1         242.26p Rser=1f
Ls1 B1 T2           1.40n  Rser=1f
K1 Le1 Li1 1
*NetList for Layer 2
Le2 N2 P2 4 Rser=1f
Li2 G Md2 1 Rser=1f
Lg2 Mg2 Md2         -79.76p Rser=1f
Rg2 Mc2 Mg2        1333.67u
Rt2 Mc2 Mt2         177.98u
Rb2 Mb2 Mc2         177.98u
Lt2 T2 Mt2         242.26p Rser=1f
Lb2 Mb2 B2         242.26p Rser=1f
Ls2 B2 T3           0.84n  Rser=1f
K2 Le2 Li2 1
*NetList for Layer 3
Le3 N3 P3 4 Rser=1f
Li3 G Md3 1 Rser=1f
Lg3 Mg3 Md3         -79.76p Rser=1f
Rg3 Mc3 Mg3        1333.67u
Rt3 Mc3 Mt3         177.98u
Rb3 Mb3 Mc3         177.98u
Lt3 T3 Mt3         242.26p Rser=1f
Lb3 Mb3 B3         242.26p Rser=1f
Ls3 B3 T4           0.70n  Rser=1f
K3 Le3 Li3 1
*NetList for Layer 4
Le4 N4 P4 1 Rser=1f
Li4 G Md4 1 Rser=1f
Lg4 Mg4 Md4         -79.76p Rser=1f
Rg4 Mc4 Mg4        1333.67u
Rt4 Mc4 Mt4         177.98u
Rb4 Mb4 Mc4         177.98u
Lt4 T4 Mt4         242.26p Rser=1f
Lb4 Mb4 B4         242.26p Rser=1f
Ls4 B4 T5           0.98n  Rser=1f
```

```
K4 Le4 Li4 1
*NetList for Layer 5
Le5 N5 P5 1 Rser=1f
Li5 G Md5 1 Rser=1f
Lg5 Mg5 Md5          -79.76p Rser=1f
Rg5 Mc5 Mg5         1333.67u
Rt5 Mc5 Mt5          177.98u
Rb5 Mb5 Mc5          177.98u
Lt5 T5 Mt5          242.26p Rser=1f
Lb5 Mb5 B5          242.26p Rser=1f
Ls5 B5 T6            0.70n  Rser=1f
K5 Le5 Li5 1
*NetList for Layer 6
Le6 N6 P6 1 Rser=1f
Li6 G Md6 1 Rser=1f
Lg6 Mg6 Md6          -79.76p Rser=1f
Rg6 Mc6 Mg6         1333.67u
Rt6 Mc6 Mt6          177.98u
Rb6 Mb6 Mc6          177.98u
Lt6 T6 Mt6          242.26p Rser=1f
Lb6 Mb6 B6          242.26p Rser=1f
Ls6 B6 T7            0.98n  Rser=1f
K6 Le6 Li6 1
*NetList for Layer 7
Le7 N7 P7 1 Rser=1f
Li7 G Md7 1 Rser=1f
Lg7 Mg7 Md7          -79.76p Rser=1f
Rg7 Mc7 Mg7         1333.67u
Rt7 Mc7 Mt7          177.98u
Rb7 Mb7 Mc7          177.98u
Lt7 T7 Mt7          242.26p Rser=1f
Lb7 Mb7 B7          242.26p Rser=1f
Ls7 B7 T8            0.70n  Rser=1f
K7 Le7 Li7 1
*NetList for Layer 8
Le8 N8 P8 4 Rser=1f
Li8 G Md8 1 Rser=1f
Lg8 Mg8 Md8          -79.76p Rser=1f
Rg8 Mc8 Mg8         1333.67u
```

```
Rt8 Mc8 Mt8          177.98u
Rb8 Mb8 Mc8          177.98u
Lt8 T8 Mt8          242.26p Rser=1f
Lb8 Mb8 B8          242.26p Rser=1f
Ls8 B8 T9            0.84n  Rser=1f
K8 Le8 Li8 1
*NetList for Layer 9
Le9 N9 P9 4 Rser=1f
Li9 G Md9 1 Rser=1f
Lg9 Mg9 Md9         -79.76p Rser=1f
Rg9 Mc9 Mg9         1333.67u
Rt9 Mc9 Mt9          177.98u
Rb9 Mb9 Mc9          177.98u
Lt9 T9 Mt9          242.26p Rser=1f
Lb9 Mb9 B9          242.26p Rser=1f
Ls9 B9 T10            1.40n  Rser=1f
K9 Le9 Li9 1
*NetList for Layer 10
Le10 N10 P10 1 Rser=1f
Li10 G Md10 1 Rser=1f
Lg10 Mg10 Md10         -79.76p Rser=1f
Rg10 Mc10 Mg10        1333.67u
Rt10 Mc10 Mt10         177.98u
Rb10 Mb10 Mc10         177.98u
Lt10 T10 Mt10         242.26p Rser=1f
Lb10 Mb10 B10         242.26p Rser=1f
Ls10 B10 T11           1.40n  Rser=1f
K10 Le10 Li10 1
Lft T0 G          692.69n Rser=1f
Lfb T11 G          692.69n Rser=1f
Ls0 T1 T0            1.40n Rser=1f
* -> Winding 1 is Series Connected
* -->Include layer 2
* -->Include layer 3
RexP2 PortP1 P2    1f
RexN3 PortN1 N3    1f
RexM2 N2 P3      1f
* -> Winding 2 is Parallel Connected
* -->Include layer 1
```

```
122 RexP1 PortP2 P1    1f
123 RexN1 PortN2 N1    1f
124 * —>Include layer 4
125 RexP4 PortP2 P4    1f
126 RexN4 PortN2 N4    1f
127 * —>Include layer 5
128 RexP5 PortP2 P5    1f
129 RexN5 PortN2 N5    1f
130 * —>Include layer 6
131 RexP6 PortP2 P6    1f
132 RexN6 PortN2 N6    1f
133 * —>Include layer 7
134 RexP7 PortP2 P7    1f
135 RexN7 PortN2 N7    1f
136 * —>Include layer 10
137 RexP10 PortP2 P10    1f
138 RexN10 PortN2 N10    1f
139 RexP8 PortP3 P8    1f
140 RexN9 PortN3 N9    1f
141 RexM8 N8 P9      1f
142 Rgnd G 0  1G
```

A three winding cantilever model shown in Fig. B-3 can be utilized to model the three winding transformer prototyped in the MultiTrack converter of Chapter 3. The transformer has three ports and six terminals: PortP1, PortN1, PortP2, PortN2, PortP3, PortN3. They map one-to-one to the six terminals in the netlists generated by *M2Spice*. They also map one-to-one to the six physical terminals of the implemented planar transformer. Here we first extract the parameters using an experiment-based approach, then extract the parameters using a SPICE-simulation-based approach.

Parameter extraction of a cantilever model is done by doing open- and short-measurements across the multiple ports. For this specific circuit with five inductances, the following impedance measurements were done:

1. Short PortP2-PortN2, Open PortP3-PortN3, measure PortP1-PortN1. Get L_1.
2. Short PortP2-PortN2, Open PortP1-PortN1, measure PortP3-PortN3. Get L_2.
3. Open PortP2-PortN2, Open PortP3-PortN3, measure PortP1-PortN1. Get L_3.

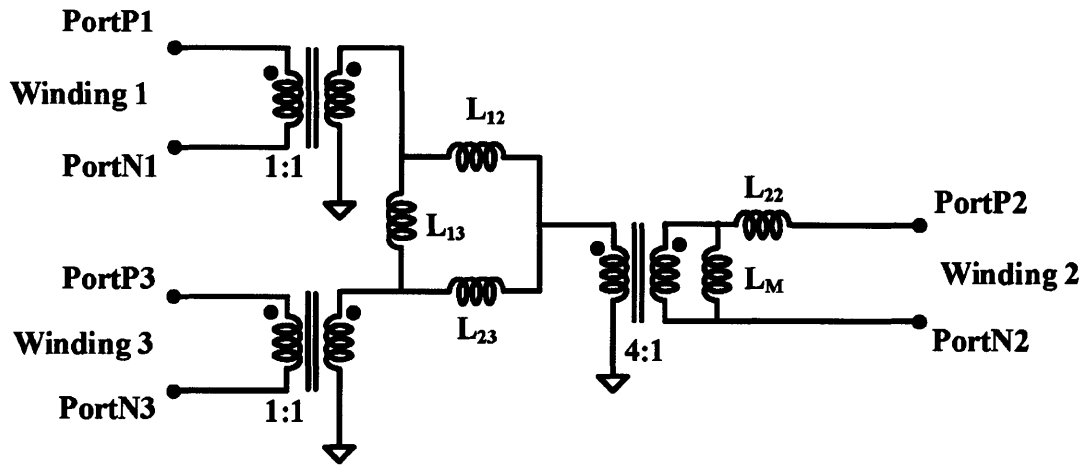


Figure B-3: Cantilever model of the implemented three-winding transformer with 4:4:1 turns ratio. Winding #1 and Winding #3 are the two primary windings, and Winding #2 is the secondary winding.

4. Open PortP1-PortN1, Open PortP3-PortN3, measure PortP2-PortN2. Get L_4.
5. Open PortP1-PortN1, Open PortP2-PortN2, measure PortP3-PortN3. Get L_5.
6. Short PortP1-PortN1, Short PortP2-PortN2, measure PortP3-PortN3. Get L_6.
7. Short PortP2-PortN2, Short PortP3-PortN3, measure PortP1-PortN1. Get L_7.
8. Short PortP1-PortN1, Short PortP3-PortN3, measure PortP2-PortN2. Get L_8.

The measured L_1-L_8 are listed in Table. B.2. Based on these impedance measurement results, the inductance values of the five inductors in the cantilever model can be estimated. The estimated inductance values are listed in Table B.3.

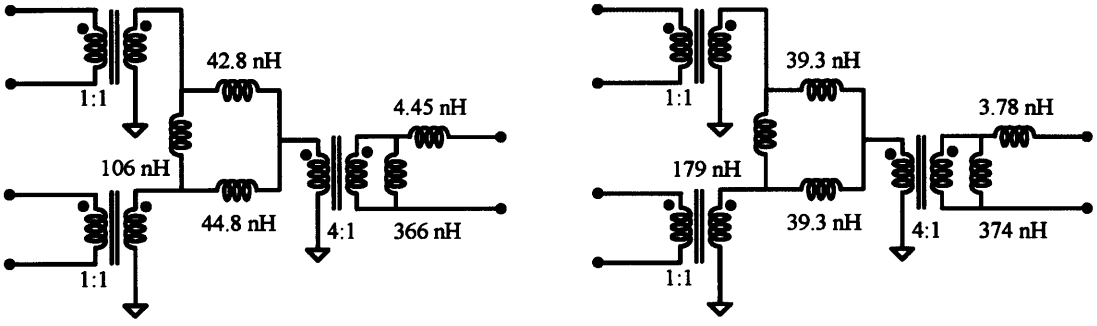
Similar open- and short- measurements can be done in SPICE simulations. By connecting the ports of the *M2Spice* generated SPICE netlists with voltage sources and measuring the magnitude and phase of the current (or connecting the ports to current sources and measuring the magnitude and phase of the voltage), the effective impedance of the port can be measured in the same way as it was in the physical circuit. Fig. B-5 shows an example screenshot of the LTspice simulation which extracts L_4.

Table B.2: Measured and simulated port inductance of the planar transformer in the MultiTrack converter.

Value	by Measurements	by Simulations	Equation
L_1	114 nH	100 nH	$L_1 = L_{12}\|\|(L_{13} + L_{23}) + 16(L_{22}\|\|L_M)$
L_2	116 nH	100 nH	$L_2 = L_{23}\|\|(L_{13} + L_{12}) + 16(L_{22}\|\|L_M)$
L_3	5.90 uH	6.02 uH	$L_3 = L_{12}\|\|(L_{13} + L_{23}) + 16L_M$
L_4	370 nH	378 nH	$L_4 = L_{22} + L_M$
L_5	5.80 uH	6.02 uH	$L_5 = L_{23}\|\|(L_{13} + L_{12}) + 16L_M$
L_6	54.7 nH	64.2 nH	$L_6 = L_{13}\|\|(L_{23} + 16(L_{22}\|\|L_M))$
L_7	55.8 nH	64.2 nH	$L_7 = L_{13}\|\|(L_{12} + 16(L_{22}\|\|L_M))$
L_8	5.70 nH	5.03 nH	$L_8 = L_{22} + L_M\|\|((L_{12}\|\|L_{23})/16)$

Table B.3: Extracted inductances of the Cantilever model based on data from measurements and data from simulations (Table B.2).

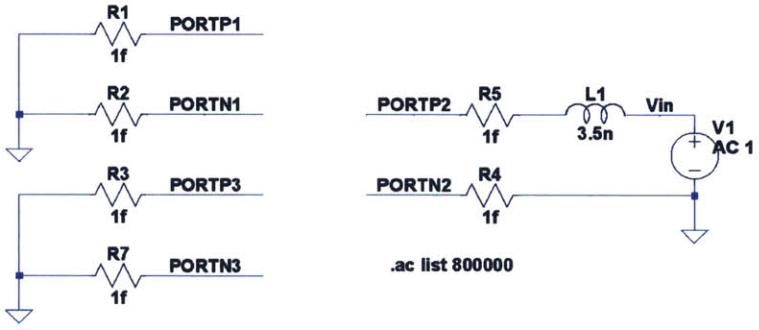
Component	by Measurements	by Simulations
L_{12}	42.8 nH	39.3 nH
L_{23}	44.8 nH	39.3 nH
L_{13}	106 nH	179 nH
L_{22}	4.45 nH	3.78 nH
L_M	366 nH	374 nH



(a) Cantilever model extracted from measurements

(b) Cantilever model extracted from simulations

Figure B-4: Cantilever model extracted from (a) measurements and (b) simulations.




```
*NetList for Layer 1
Le1 N1 P1 1 Rser=1f
Li1 G Md1 1 Rser=1f
Lg1 Mg1 Md1      -79.76p Rser=1f
Rg1 Mc1 Mg1      1333.67u
Rt1 Mc1 Mt1      177.98u
Rb1 Mb1 Mc1      177.98u
Lt1 T1 Mt1       242.26p Rser=1f
Lb1 Mb1 B1       242.26p Rser=1f
Ls1 B1 T2        1.40n  Rser=1f
K1 Le1 Li1 1
*NetList for Layer 2
Le2 N2 P2 4 Rser=1f
Li2 G Md2 1 Rser=1f
Lg2 Mg2 Md2      -79.76p Rser=1f
Rg2 Mc2 Mg2      1333.67u
Rt2 Mc2 Mt2      177.98u
Rb2 Mb2 Mc2      177.98u
Lt2 T2 Mt2       242.26p Rser=1f
Lb2 Mb2 B2       242.26p Rser=1f
Ls2 B2 T3        0.84n  Rser=1f
K2 Le2 Li2 1
*NetList for Layer 3
Le3 N3 P3 4 Rser=1f
Li3 G Md3 1 Rser=1f
Lg3 Mg3 Md3      -79.76p Rser=1f
Rg3 Mc3 Mg3      1333.67u
Rt3 Mc3 Mt3      177.98u
Rb3 Mb3 Mc3      177.98u
Lt3 T3 Mt3       242.26p Rser=1f
Lb3 Mb3 B3       242.26p Rser=1f
Ls3 B3 T4        0.70n  Rser=1f
K3 Le3 Li3 1
*NetList for Layer 4
Le4 N4 P4 1 Rser=1f
Li4 G Md4 1 Rser=1f
Lg4 Mg4 Md4      -79.76p Rser=1f
Rg4 Mc4 Mg4      1333.67u
Rt4 Mc4 Mt4      177.98u
Rb4 Mb4 Mc4      177.98u
Lt4 T4 Mt4       242.26p Rser=1f
Lb4 Mb4 B4       242.26p Rser=1f
Ls4 B4 T5        0.98n  Rser=1f
K4 Le4 Li4 1
*NetList for Layer 5
Le5 N5 P5 1 Rser=1f
Li5 G Md5 1 Rser=1f
Lg5 Mg5 Md5      -79.76p Rser=1f
Rg5 Mc5 Mg5      1333.67u
Rt5 Mc5 Mt5      177.98u
Rb5 Mb5 Mc5      177.98u
Lt5 T5 Mt5       242.26p Rser=1f
Lb5 Mb5 B5       242.26p Rser=1f
Ls5 B5 T6        0.70n  Rser=1f
K5 Le5 Li5 1
*NetList for Layer 6
Le6 N6 P6 1 Rser=1f
Li6 G Md6 1 Rser=1f
Lg6 Mg6 Md6      -79.76p Rser=1f
Rg6 Mc6 Mg6      1333.67u
Rt6 Mc6 Mt6      177.98u
Rb6 Mb6 Mc6      177.98u
Lt6 T6 Mt6       242.26p Rser=1f
Lb6 Mb6 B6       242.26p Rser=1f
Ls6 B6 T7        0.98n  Rser=1f
K6 Le6 Li6 1
*NetList for Layer 7
Le7 N7 P7 1 Rser=1f
Li7 G Md7 1 Rser=1f
Lg7 Mg7 Md7      -79.76p Rser=1f
Rg7 Mc7 Mg7      1333.67u
Rt7 Mc7 Mt7      177.98u
Rb7 Mb7 Mc7      177.98u
Lt7 T7 Mt7       242.26p Rser=1f
Lb7 Mb7 B7       242.26p Rser=1f
Ls7 B7 T8        0.70n  Rser=1f
K7 Le7 Li7 1
*NetList for Layer 8
Le8 N8 P8 4 Rser=1f
Li8 G Md8 1 Rser=1f
Lg8 Mg8 Md8      -79.76p Rser=1f
Rg8 Mc8 Mg8      1333.67u
Rt8 Mc8 Mt8      177.98u
Rb8 Mb8 Mc8      177.98u
Lt8 T8 Mt8       242.26p Rser=1f
Lb8 Mb8 B8       242.26p Rser=1f
Ls8 B8 T9        0.84n  Rser=1f
K8 Le8 Li8 1
*NetList for Layer 9
Le9 N9 P9 4 Rser=1f
Li9 G Md9 1 Rser=1f
Lg9 Mg9 Md9      -79.76p Rser=1f
Rg9 Mc9 Mg9      1333.67u
Rt9 Mc9 Mt9      177.98u
Rb9 Mb9 Mc9      177.98u
Lt9 T9 Mt9       242.26p Rser=1f
Lb9 Mb9 B9       242.26p Rser=1f
Ls9 B9 T10       1.40n  Rser=1f
K9 Le9 Li9 1
*NetList for Layer 10
Le10 N10 P10 1 Rser=1f
Li10 G Md10 1 Rser=1f
Lg10 Mg10 Md10     -79.76p Rser=1f
Rg10 Mc10 Mg10     1333.67u
Rt10 Mc10 Mt10     177.98u
Rb10 Mb10 Mc10     177.98u
Lt10 T10 Mt10      242.26p Rser=1f
Lb10 Mb10 B10      242.26p Rser=1f
Ls10 B10 T11       1.40n  Rser=1f
K10 Le10 Li10 1
* Modeling the Core and the Air Gap
Lft T0 G       692.69n Rser=1f
Lfb T11 G      692.69n Rser=1f
Ls0 T1 T0      1.40n  Rser=1f
* -> Winding 1 is Series Connected
* -->Include layer 2
* -->Include layer 3
RexP2 PortP1 P2   1f
RexN3 PortN1 N3   1f
RexM2 N2 P3    1f
* -> Winding 2 is Parallel Connected
* -->Include layer 1
RexP1 PortP2 P1   1f
RexN1 PortN2 N1   1f
* -->Include layer 4
RexP4 PortP2 P4   1f
RexN4 PortN2 N4   1f
* -->Include layer 5
RexP5 PortP2 P5   1f
RexN5 PortN2 N5   1f
* -->Include layer 6
RexP6 PortP2 P6   1f
RexN6 PortN2 N6   1f
* -->Include layer 7
RexP7 PortP2 P7   1f
RexN7 PortN2 N7   1f
* -->Include layer 10
RexP10 PortP2 P10   1f
RexN10 PortN2 N10   1f
* -> Winding 3 is Series Connected
* -->Include layer 8
* -->Include layer 9
RexP8 PortP3 P8   1f
RexN9 PortN3 N9   1f
RexM8 N8 P9    1f
Rgnd G 0  1G
```

rs\Minjie\Dropbox (Personal)\Research\MultiTrack DCDC\LTSPICE\Final Version\MagneticModel_inter

Figure B-5: An example screenshot of the LTspice simulation which extracts L_4.

B.3 PCB Layouts and Schematics

The top two layers (layers 1-2) of the PCB board are utilized to implement one set of primary windings. It has four turns in total, with two turns on each layer. Many switches and active devices are placed on the top layer. A majority of area on the right side of the top layer was is as the output negative plane. A majority of the area on the left side of the second layer is utilized as the input side ground plane. A majority of the area on the right side of the second layer is utilized as the output negative plane (connected in parallel with the top layer through blind vias).

The center four layers (layers 3-6) of the PCB board are utilized to implement the secondary winding. All four layers are connected in parallel. Auxiliary turns for the gate drive power supply were also implemented on these four layers with one turn per layer.

The bottom two layers (layers 7-8) of the PCB board are utilized to implement the other set of primary windings. It has four turns in total, with two turns on each layer. Many capacitors and auxiliary devices (LDOs and boot-strap diodes) are placed on the bottom layer. Two rectifier side switches are also placed on the bottom layer. A majority of the area on the right side of the layer 7 is utilized as the output positive plane. A majority of area on the left side of the bottom layer is utilized as the input side ground plane. A majority of the area on the right side of the bottom layer is utilized as the output positive plane (connected in parallel with the layer 7 through blind vias).

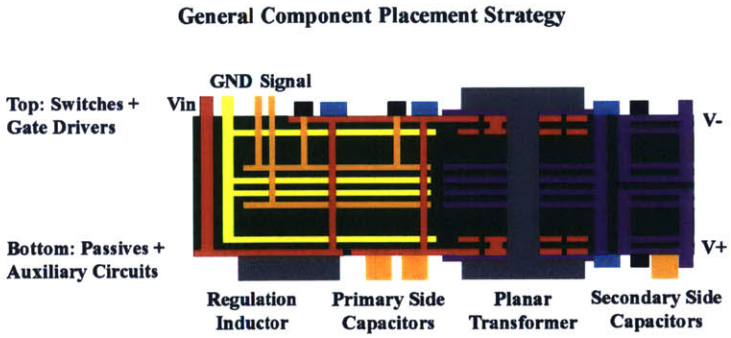


Figure B-6: General component placement strategy of the MultiTrack PCB board. Switches and gate drivers are placed on the top side of the PCB board. Passive components and auxiliary circuits are placed on the bottom side of the PCB board.

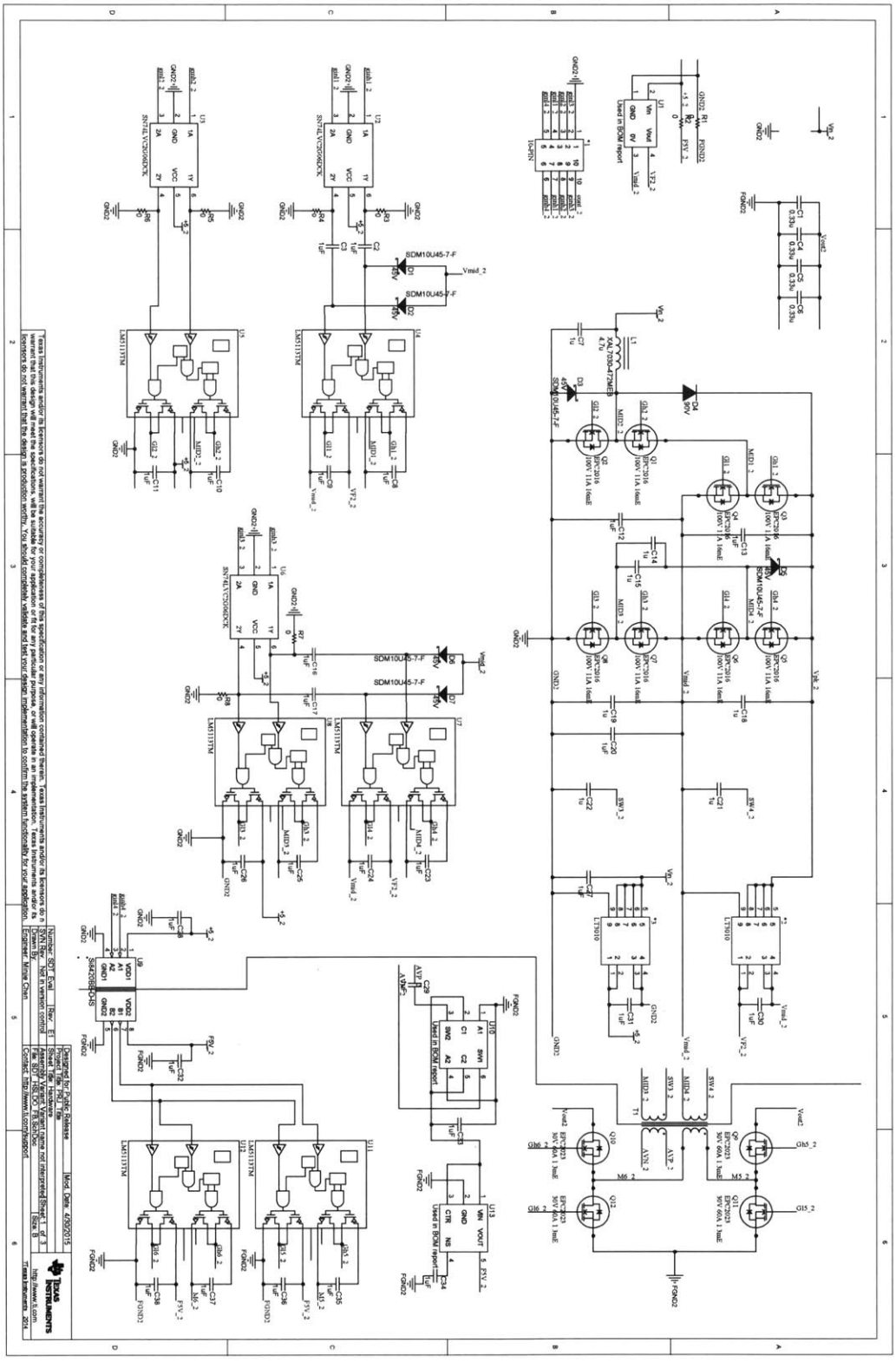
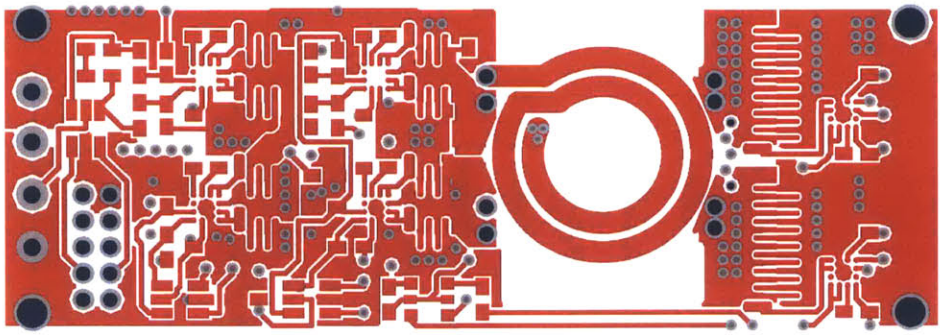


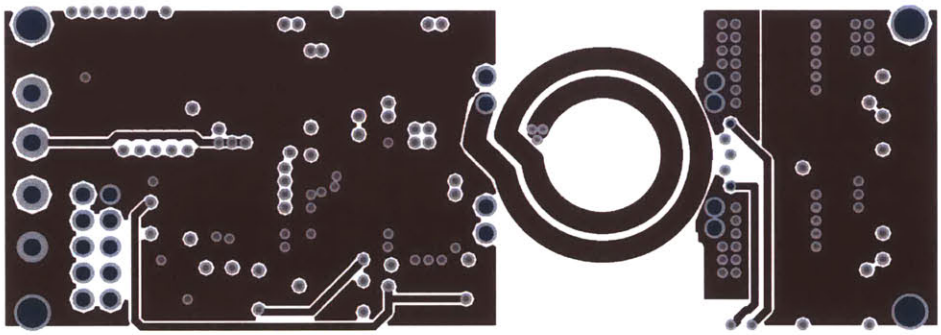
Figure B-7: Schematic of the MultiTrack prototype.

Table B.4: Bill of Materials (BOM) of the MultiTrack converter. Resistances and capacitances are not shown. Information about some critical components is also listed in Table 3.2.

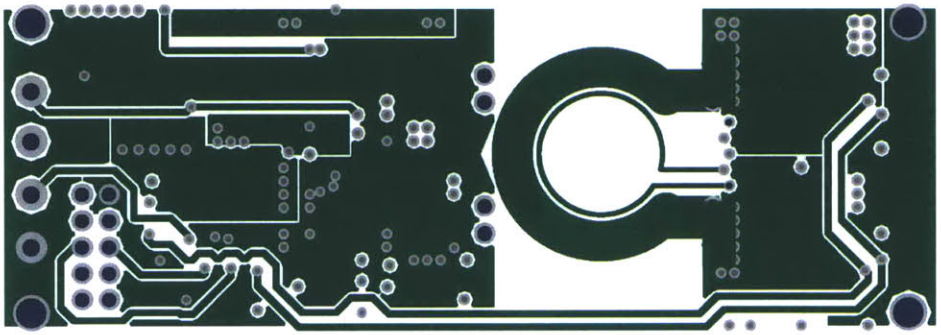
Part	Description	Designator	Footprint
LT3010	3V to 80V Linear Regulator	*2, *3	8MSOP
CD0603-S0180	Diode, Switching, 90V, 0.1A, 0603 Diode	D1, D2, D3, D5, D6, D7	Diode0603
CD1005-S0180	Diode, Switching, 90V, 0.1A, 1005 Diode	D4	Diode1005
XAL7030-472MEB	Inductor, Shielded, 5.2uH	L1	ThinL
EPC2016	100V 11A 16mE	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	EPC2x40M
EPC2023	40V 10A 16mE	Q9, Q10, Q11, Q12	EPC2x40XL
SN74LVC2G06DCK	IC, Dual Buffer/Driver w/Open-Drain Outputs	U2, U3, U6	SC70New
LM5113TM	eGaN 100V Half Bridge Gate Driver	U4, U5, U7, U8, U11, U12	uSMD12
Si8420BB-D-IS	ISOPro Low-Power Dual-Channel Digital Isolator	U9	SOIC127P600X175-8N
BAT54XY	Schottky barrier diodes	U10	SOT363
MIC5235	2.3V-24V, LDO Regulator	U13	SOT235
Through Hole Connectors	CONN SOCKET RCPT .014-.026 30AU	T1, T2, T3, T4	1.77mm



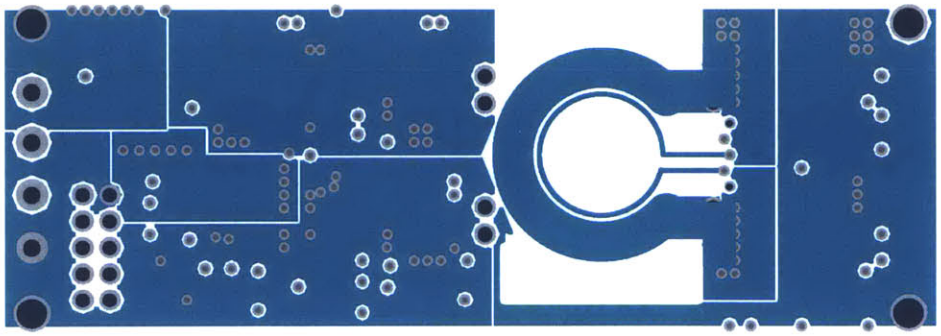
(a)



(b)

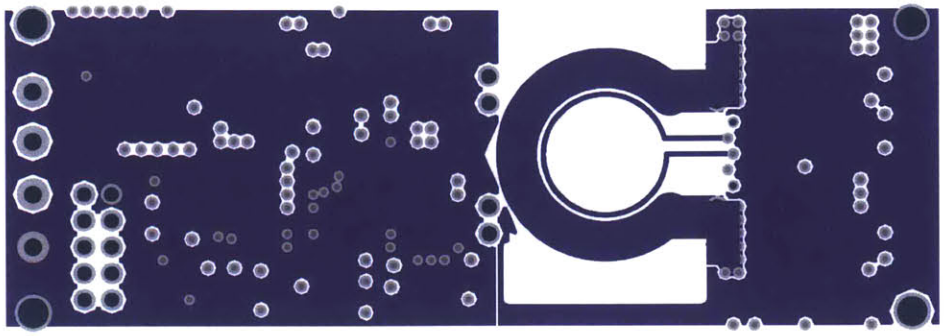


(c)

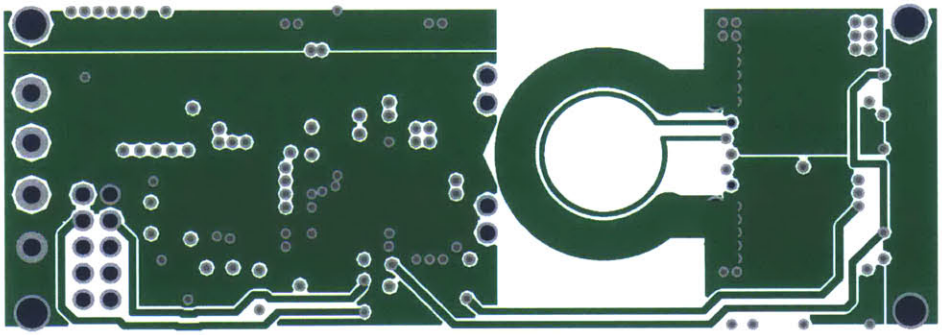


(d)

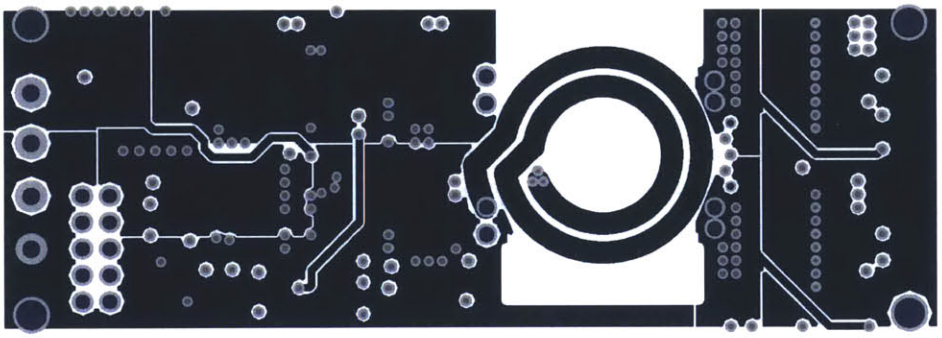
Figure B-8: Layers 1-4 of the MultiTrack PCB.



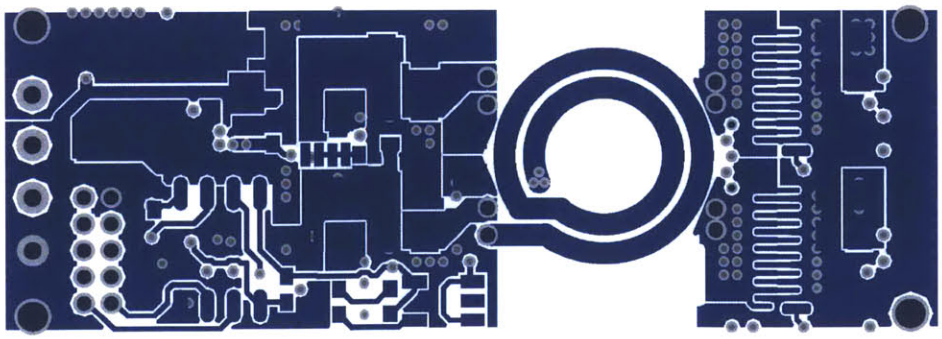
(a)



(b)



(c)



(d)

Figure B-9: Layers 5-8 of the MultiTrack PCB.

B.4 Micro-controller Codes

```
1  //-----------------------------------------------------
2  //  FILE:   AsymmetricPWM .C
3  //  Description: This file is for basic start-up and steady-state ...
       operation testing of
4  //              several dc-dc converter prototypes in open loop.
5  //  Target: TMS320F28069 (Piccolo controlStick)
6  //-----------------------------------------------------
7  //  Minjie Chen
8  //  EECS - MIT
9  //  Date: 4 May 2015
10 // PLEASE READ - Useful notes about this Project
11 // Although this project is made up of several files, the most important ...
       ones are:
12 //   "AsymmetricPWM .c",    this file
13 //      - Application Initialization, Peripheral config
14 //      - Application management
15 //      - Slower background code loops and Task scheduling
16 //   "AsymmetricPWM-DevInit_F28xxx.c"
17 //      - Device Initialization, e.g. Clock, PLL, WD, GPIO mapping
18 //      - Peripheral clock enables
19 // The other files are generally used for support and defining the ...
       registers as C
20 // structs. In general these files will not need to be changed.
21 //   "F28069_RAM_AsymmetricPWM.CMD" or "F28069_FLASH_AsymmetricPWM.CMD"
22 //      - Allocates the program and data spaces into the device's memory map.
23 //   "DSP2802x_Headers_nonBIOS.cmd" and "DSP2806x_GlobalVariableDefs.c"
24 //      - Allocate the register structs into data memory.  These register ...
       structs are
25 //        defined in the peripheral header includes (DSP2802x_Adc.h, ...)
26 //-----------------------------------------------------
27
28 #include "PeripheralHeaderIncludes.h"
29 #include "F2806x_EPwm_defines.h"      // useful defines for initialization
30
31 void DeviceInit(void);
32 void InitFlash(void);
```

```
33 void MemCopy(Uint16 *SourceAddr, Uint16* SourceEndAddr, Uint16* DestAddr);
34 // Used for running BackGround in flash and the ISR in RAM
35
36 extern Uint16 RamfuncsLoadStart, RamfuncsLoadEnd, RamfuncsRunStart;
37 Uint16 on_time_inv=40;
38 Uint16 on_time_syc=40;
39 Uint16 period_iso=80;
40 Uint16 period_bstH=80;
41 Uint16 period_bstL=80;
42 // define variables for the boost converter
43 Uint16 on_time_bstH=40;
44 Uint16 on_time_bstL=40;
45 //Define variables for Inverters
46 Uint16 delay_inv=0;     // Delay for the inverter stage
47 Uint16 high_res_inv=0;      // High resolution bits of PWM set to 0 ...
       initially;
48 Uint16 deadtime_inv_FE=2;   // Deadtime Falling Edge;
49 Uint16 deadtime_inv_RE=2;   // Deadtime Rising Edge
50 //Define variables for Rectifiers
51 Uint16 delay_syc=0;     // Delay for the rectifier stage
52 Uint16 high_res_syc=0;      // High resolution bits of PWM set to 0 ...
       initially;
53 Uint16 deadtime_syc_FE=2;// Deadtime Falling Edge;
54 Uint16 deadtime_syc_RE=2;// Deadtime Rising Edge;
55 //Define variables for the High Side Boost Converter
56 Uint16 delay_bstH=0;        // Delay for the boost stage
57 Uint16 high_res_bstH=0;     // High resolution bits of PWM set to 0 ...
       initially,
58 Uint16 deadtime_bstH_FE=2;// Deadtime Falling Edge;
59 Uint16 deadtime_bstH_RE=2;// Deadtime Rising Edge.
60 //Define variables for the Low Side Boost Converter
61 Uint16 delay_bstL=0;        // Delay for the boost stage
62 Uint16 high_res_bstL=0;     // High resolution bits of PWM set to 0 ...
       initially,
63 Uint16 deadtime_bstL_FE=2;// Deadtime Falling Edge;
64 Uint16 deadtime_bstL_RE=2;// Deadtime Rising Edge.
65 //Define variables
66 // MAIN CODE - starts here
67 void main(void)
```

```
68 {
69
70 //===================================
71 //  INITIALISATION - General
72 //===================================
73     DeviceInit();   // Device Life support & GPIO mux settings
74 // Only used if running from FLASH
75 // Note that the variable FLASH is defined by the compiler (-d FLASH)
76     #ifdef FLASH
77 // Copy time critical code and Flash setup code to RAM
78 // The  RamfuncsLoadStart, RamfuncsLoadEnd, and RamfuncsRunStart
79 // symbols are created by the linker. Refer to the linker files.
80     MemCopy(&RamfuncsLoadStart, &RamfuncsLoadEnd, &RamfuncsRunStart);
81 // Call Flash Initialization to setup flash waitstates
82 // This function must reside in RAM
83     InitFlash();    // Call the flash wrapper init function
84     #endif //(FLASH)
85     EPwm1Regs.TBPRD = period_bstL;
86     EPwm1Regs.TBPHS.half.TBPHS = 1;                // Set Phase register ...
          to zero
87     EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;     // Count up mode
88     EPwm1Regs.TBCTR = 0;                         // clear TB counter
89     EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;           // Master module
90     EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
91     EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;    // Sync down-stream ...
          module
92     EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
93     EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
94     EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
95     EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
96     EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;  // load on CTR=Zero
97     EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;  // load on CTR=Zero
98     EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
99     EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;           // set actions for EPWM1A
100    EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
101    EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;      // Active Hi ...
          complementary
102    EPwm1Regs.DBFED = deadtime_bstL_FE;
103    EPwm1Regs.DBRED = deadtime_bstL_RE;
```

```
104     EPwm1Regs.CMPA.half.CMPA = on_time_bstL;
105     EALLOW;
106     EPwm1Regs.HRCNFG.all = 0x0;                              //Initialize ...
            HiRes PWM Control Register
107     EPwm1Regs.HRCNFG.bit.EDGMODE = HR_BEP;                   //Enable HiRes ...
            control on Both edges
108     EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;                   // CMPAHR ...
            controls the MEP
109     EPwm1Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;      // Load CMPAHR when ...
            the counter is zero
110     EPwm1Regs.CMPA.half.CMPAHR   = high_res_bstL<<8;         // Set high ...
            res portion of duty cycle
111     EDIS;
112     // EPWM Module 2 config, PWM2B control S3 of Phase A
113     EPwm2Regs.TBPRD = period_iso;
114     EPwm2Regs.TBPHS.half.TBPHS = delay_syc;                  // Set initial state
115     EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;       // Symmetrical mode
116     EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;           // Slave module
117     EPwm2Regs.TBCTL.bit.PHSDIR = TB_UP;                  // Count UP on sync
118     EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
119     EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;       // sync flow-through
120     EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
121     EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
122     EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
123     EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
124     EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;    // load on CTR=Zero
125     EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;    // load on CTR=Zero
126     EPwm2Regs.AQCTLA.bit.ZRO = AQ_CLEAR;
127     EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;               // set actions for EPWM1A
128     EPwm2Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
129     EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;        // Active Hi ...
            complementary
130     EPwm2Regs.DBFED = deadtime_syc_FE;
131     EPwm2Regs.DBRED = deadtime_syc_RE;
132     EPwm2Regs.CMPA.half.CMPA = on_time_syc;
133     EALLOW;
134     EPwm2Regs.HRCNFG.all = 0x0;                              //Initialize ...
            HiRes PWM Control Register
```

```
135     EPwm2Regs.HRCNFG.bit.EDGMODE = HR_BEP;              //Enable HiRes ...
            control on both edges
136     EPwm2Regs.HRCNFG.bit.CTLMODE = HR_CMP;              // CMPAHR ...
            controls the MEP
137     EPwm2Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;     // Load CMPAHR when ...
            the counter is zero
138     EPwm2Regs.CMPA.half.CMPAHR   = high_res_syc<<8;     // Set high res ...
            portion of duty cycle
139     EDIS;
140     // EPWM Module 3 config, controlling S1 and S2 of Phase B
141     EPwm3Regs.TBPRD = period_bstH;
142     EPwm3Regs.TBPHS.half.TBPHS = delay_bstH;            // Set initial State
143     EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;      // Symmetrical mode
144     EPwm3Regs.TBCTL.bit.PHSEN = TB_ENABLE;          // Slave module
145     EPwm3Regs.TBCTL.bit.PHSDIR = TB_UP;                 // Count UP on sync
146     EPwm3Regs.TBCTL.bit.PRDLD = TB_SHADOW;
147     EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;      // sync flow-through
148     EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
149     EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV1;
150     EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
151     EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
152     EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;   // load on CTR=Zero
153     EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;   // load on CTR=Zero
154     EPwm3Regs.AQCTLA.bit.ZRO = AQ_SET;
155     EPwm3Regs.AQCTLA.bit.CAU = AQ_CLEAR;            // set actions for EPWM1A
156     EPwm3Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE;  // enable Dead-band ...
            module
157     EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;       // Active Hi ...
            complementary
158     EPwm3Regs.DBFED = deadtime_bstH_FE;
159     EPwm3Regs.DBRED = deadtime_bstH_RE;
160     EPwm3Regs.CMPA.half.CMPA = on_time_bstH;
161     EALLOW;
162     EPwm3Regs.HRCNFG.all = 0x0;                             //Initialize ...
            HiRes PWM Control Register
163     EPwm3Regs.HRCNFG.bit.EDGMODE = HR_BEP;              //Enable HiRes ...
            control on Both edges
164     EPwm3Regs.HRCNFG.bit.CTLMODE = HR_CMP;              // CMPAHR ...
            controls the MEP
```

```
165     EPwm3Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;      // Load CMPAHR when ...
            the counter is zero
166     EPwm3Regs.CMPA.half.CMPAHR   = high_res_bstH<<8;    // Set high res ...
            portion of duty cycle
167     EDIS;
168     // EPWM Module 4 config
169     EPwm4Regs.TBPRD = period_iso;
170     EPwm4Regs.TBPHS.half.TBPHS = delay_inv;             // Set Phase ...
            register to zero
171     EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;      // Symmetrical mode
172     EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE;          // Slave module
173     EPwm4Regs.TBCTL.bit.PHSDIR = TB_UP;                 // Count UP on sync
174     EPwm4Regs.TBCTL.bit.PRDLD = TB_SHADOW;
175     EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;      // Sync down-stream ...
            module
176     EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
177     EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;
178     EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
179     EPwm4Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
180     EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;   // load on CTR=Zero
181     EPwm4Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;   // load on CTR=Zero
182     EPwm4Regs.AQCTLA.bit.CAU = AQ_SET;              // set actions for EPWM4A
183     EPwm4Regs.AQCTLA.bit.ZRO = AQ_CLEAR;
184     EPwm4Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // enable Dead-band module
185     EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;       // Active Hi ...
            complementary
186     EPwm4Regs.DBFED = deadtime_inv_FE;
187     EPwm4Regs.DBRED = deadtime_inv_RE;
188     EPwm4Regs.CMPA.half.CMPA = on_time_inv;
189     EALLOW;
190     EPwm4Regs.HRCNFG.all = 0x0;                             //Initialize ...
            HiRes PWM Control Register
191     EPwm4Regs.HRCNFG.bit.EDGMODE = HR_BEP;              //Enable HiRes ...
            control on both edges
192     EPwm4Regs.HRCNFG.bit.CTLMODE = HR_CMP;              // CMPAHR ...
            controls the MEP
193     EPwm4Regs.HRCNFG.bit.HRLOAD  = HR_CTR_ZERO;     // Load CMPAHR when ...
            the counter is zero
```

```
194     EPwm4Regs.CMPA.half.CMPAHR   = high_res_inv<<8;     // Set high res ...
            portion of duty cycle
195     EDIS;
196     //FOREVER Loop, Refresh the Phase Registers for Active Tuning Modes
197     for(;;)
198     {
199      EPwm1Regs.TBPRD = period_bstL;
200      EPwm1Regs.CMPA.half.CMPA = on_time_bstL;
201      EPwm1Regs.DBFED = deadtime_bstL_FE;
202      EPwm1Regs.DBRED = deadtime_bstL_RE;
203      EPwm1Regs.CMPA.half.CMPAHR = high_res_bstL<<8;
204      EPwm2Regs.TBPRD = period_iso;
205      EPwm2Regs.TBPHS.half.TBPHS = delay_syc;
206      EPwm2Regs.CMPA.half.CMPA = on_time_syc;
207      EPwm2Regs.DBFED = deadtime_syc_FE;
208      EPwm2Regs.DBRED = deadtime_syc_RE;
209      EPwm2Regs.CMPA.half.CMPAHR = high_res_syc<<8;
210      EPwm3Regs.TBPRD = period_bstH;
211      EPwm3Regs.TBPHS.half.TBPHS = delay_bstH;
212      EPwm3Regs.CMPA.half.CMPA = on_time_bstH;
213      EPwm3Regs.DBFED = deadtime_bstH_FE;
214      EPwm3Regs.DBRED = deadtime_bstH_RE;
215      EPwm3Regs.CMPA.half.CMPAHR = high_res_bstH<<8;
216      EPwm4Regs.TBPRD = period_iso;
217      EPwm4Regs.TBPHS.half.TBPHS = delay_inv;
218      EPwm4Regs.CMPA.half.CMPA = on_time_inv;
219      EPwm4Regs.DBFED = deadtime_inv_FE;
220      EPwm4Regs.DBRED = deadtime_inv_RE;
221      EPwm4Regs.CMPA.half.CMPAHR = high_res_inv<<8;
222     }
223 }
```

```
1 //===========================
2 //
3 // FILE:    AsymmetricPWM-DevInit_F2802x.c
4 //
5 // TITLE:   Device initialization for F2802x series
6 //
```

```
7  // Version: 1.0
8  //
9  // Date:    22 Oct 08   BRL
10 //===========================
11 #include "PeripheralHeaderIncludes.h"
12 // Functions that will be run from RAM need to be assigned to
13 // a different section.  This section will then be mapped to a load and
14 // run address using the linker cmd file.
15 #pragma CODE_SECTION(InitFlash, "ramfuncs");
16 #define Device_cal (void   (*)(void))0x3D7C80
17 void DeviceInit(void);
18 void PieCntlInit(void);
19 void PieVectTableInit(void);
20 void WDogDisable(void);
21 void PLLset(Uint16);
22 void ISR_ILLEGAL(void);
23 //---------------------------------------------------------------------------
24 //  Configure Device for target Application Here
25 //---------------------------------------------------------------------------
26 void DeviceInit(void)
27 {
28     WDogDisable();  // Disable the watchdog initially
29     DINT;           // Global Disable all Interrupts
30     IER = 0x0000;   // Disable CPU interrupts
31     IFR = 0x0000;   // Clear all CPU interrupt flags
32 // The Device_cal function, which copies the ADC & oscillator calibration ...
       values
33 // from TI reserved OTP into the appropriate trim registers, occurs ...
       automatically
34 // in the Boot ROM. If the boot ROM code is bypassed during the debug ...
       process, the
35 // following function MUST be called for the ADC and oscillators to ...
       function according
36 // to specification.
37     EALLOW;
38     SysCtrlRegs.PCLKCR0.bit.ADCENCLK = 1; // Enable ADC peripheral clock
39     (*Device_cal)();                      // Auto-calibrate from TI OTP
40     SysCtrlRegs.PCLKCR0.bit.ADCENCLK = 0; // Return ADC clock to original ...
           state
```

```
41      EDIS;
42  // Switch to Internal Oscillator 1 and turn off all other clock
43  // sources to minimize power consumption
44      EALLOW;
45      SysCtrlRegs.CLKCTL.bit.INTOSC1OFF = 0;
46      SysCtrlRegs.CLKCTL.bit.OSCCLKSRCSEL=0;  // Clk Src = INTOSC1
47      SysCtrlRegs.CLKCTL.bit.XCLKINOFF=1;     // Turn off XCLKIN
48      SysCtrlRegs.CLKCTL.bit.XTALOSCOFF=1;    // Turn off XTALOSC
49      SysCtrlRegs.CLKCTL.bit.INTOSC2OFF=1;    // Turn off INTOSC2
50      EDIS;
51      // SYSTEM CLOCK speed based on internal oscillator = 10 MHz
52      // 0x10=  80    MHz     (16)
53      // 0xF =  75    MHz     (15)
54      // 0xE =  70    MHz     (14)
55      // 0xD =  65    MHz     (13)
56      // 0xC =  60    MHz     (12)
57      // 0xB =  55    MHz     (11)
58      // 0xA =  50    MHz     (10)
59      // 0x9 =  45    MHz     (9)
60      // 0x8 =  40    MHz     (8)
61      // 0x7 =  35    MHz     (7)
62      // 0x6 =  30    MHz     (6)
63      // 0x5 =  25    MHz     (5)
64      // 0x4 =  20    MHz     (4)
65      // 0x3 =  15    MHz     (3)
66      // 0x2 =  10    MHz     (2)
67      PLLset( 0x10 ); // choose from options above
68  // Initialise interrupt controller and Vector Table
69  // to defaults for now. Application ISR mapping done later.
70      PieCntlInit();
71      PieVectTableInit();
72      EALLOW; // below registers are "protected", allow access.
73  // LOW SPEED CLOCKS prescale register settings
74     SysCtrlRegs.LOSPCP.all = 0x0002;     // Sysclk / 4 (15 MHz)
75     SysCtrlRegs.XCLK.bit.XCLKOUTDIV=2;
76  // PERIPHERAL CLOCK ENABLES
77  //---------------------------------------------------
78  // If you are not using a peripheral you may want to switch
79  // the clock off to save power, i.e. set to =0
```

```
80  //
81  // Note: not all peripherals are available on all 280x derivates.
82  // Refer to the datasheet for your particular device.
83
84      SysCtrlRegs.PCLKCR0.bit.ADCENCLK = 1;     // ADC
85      //--------------------------------------------------
86      SysCtrlRegs.PCLKCR3.bit.COMP1ENCLK = 0;   // COMP1
87      SysCtrlRegs.PCLKCR3.bit.COMP2ENCLK = 0;   // COMP2
88      //--------------------------------------------------
89      SysCtrlRegs.PCLKCR0.bit.I2CAENCLK = 0;    // I2C
90      //--------------------------------------------------
91      SysCtrlRegs.PCLKCR0.bit.SPIAENCLK = 0;    // SPI-A
92      //--------------------------------------------------
93      SysCtrlRegs.PCLKCR0.bit.SCIAENCLK = 0;    // SCI-A
94      //--------------------------------------------------
95      SysCtrlRegs.PCLKCR1.bit.ECAP1ENCLK = 0;   //eCAP1
96      //--------------------------------------------------
97      SysCtrlRegs.PCLKCR1.bit.EPWM1ENCLK = 1;   // ePWM1
98      SysCtrlRegs.PCLKCR1.bit.EPWM2ENCLK = 1;   // ePWM2
99      SysCtrlRegs.PCLKCR1.bit.EPWM3ENCLK = 1;   // ePWM3
100     SysCtrlRegs.PCLKCR1.bit.EPWM4ENCLK = 1;   // ePWM4
101     //--------------------------------------------------
102     SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;    // Enable TBCLK
103     //--------------------------------------------------
104     SysCtrlRegs.PCLKCR3.bit.DMAENCLK = 0;     // DMA
105     //--------------------------------------------------
106     SysCtrlRegs.PCLKCR3.bit.CLA1ENCLK = 0;    // CLA
107     //--------------------------------------------------
108 //--------------------------------------------------
109 // GPIO (GENERAL PURPOSE I/O) CONFIG
110 //--------------------------------------------------
111 //---------------------------
112 // QUICK NOTES on USAGE:
113 //---------------------------
114 // If GpioCtrlRegs.GP?MUX?bit.GPIO?= 1, 2 or 3 (i.e. Non GPIO func), then ...
        leave
115 //  rest of lines commented
116 // If GpioCtrlRegs.GP?MUX?bit.GPIO?= 0 (i.e. GPIO func), then:
117 //  1) uncomment GpioCtrlRegs.GP?DIR.bit.GPIO? = ? and choose pin to be ...
```

```
        IN or OUT
118  //  2) If IN, can leave next to lines commented
119  //  3) If OUT, uncomment line with ..GPACLEAR.. to force pin LOW or
120  //             uncomment line with ..GPASET.. to force pin HIGH or
121  //---------------------------------------------------
122  //---------------------------------------------------
123  //  GPIO-00 - PIN FUNCTION = --Spare--
124       GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;     // 0=GPIO,  1=EPWM1A,  ...
           2=Resv,  3=Resv
125       GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;      // 1=OUTput,  0=INput
126  //   GpioDataRegs.GPACLEAR.bit.GPIO0 = 1;    // uncomment if --> Set Low ...
       initially
127  //   GpioDataRegs.GPASET.bit.GPIO0 = 1;      // uncomment if --> Set High ...
       initially
128       GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;      // Disable pull-up on GPIO0 ...
           (EPWM1A)
129  //---------------------------------------------------
130  //  GPIO-01 - PIN FUNCTION = --Spare--
131       GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;     // 0=GPIO,  1=EPWM1B,  ...
           2=EMU0,  3=COMP1OUT
132       GpioCtrlRegs.GPADIR.bit.GPIO1 = 1;      // 1=OUTput,  0=INput
133  //   GpioDataRegs.GPACLEAR.bit.GPIO1 = 1;    // uncomment if --> Set Low ...
       initially
134  //   GpioDataRegs.GPASET.bit.GPIO1 = 1;      // uncomment if --> Set High ...
       initially
135  //---------------------------------------------------
136  //  GPIO-02 - PIN FUNCTION = --Spare--
137       GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;     // 0=GPIO,  1=EPWM2A,  ...
           2=Resv,  3=Resv
138       GpioCtrlRegs.GPADIR.bit.GPIO2 = 1;      // 1=OUTput,  0=INput
139  //   GpioDataRegs.GPACLEAR.bit.GPIO2 = 1;    // uncomment if --> Set Low ...
       initially
140  //   GpioDataRegs.GPASET.bit.GPIO2 = 1;      // uncomment if --> Set High ...
       initially
141  //---------------------------------------------------
142  //  GPIO-03 - PIN FUNCTION = --Spare--
143       GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;     // 0=GPIO,  1=EPWM2B,  ...
           2=Resv,  3=COMP2OUT
144       GpioCtrlRegs.GPADIR.bit.GPIO3 = 1;      // 1=OUTput,  0=INput
```

```
145 //  GpioDataRegs.GPACLEAR.bit.GPIO3 = 1;     // uncomment if --> Set Low ...
        initially
146 //  GpioDataRegs.GPASET.bit.GPIO3 = 1;       // uncomment if --> Set High ...
        initially
147 //--------------------------------------------------------------
148 //  GPIO-04 - PIN FUNCTION = --Spare--
149     GpioCtrlRegs.GPAMUX1.bit.GPIO4 = 1;      // 0=GPIO,  1=EPWM3A, 2=Resv, ...
            3=Resv
150     GpioCtrlRegs.GPADIR.bit.GPIO4 = 1;       // 1=OUTput,  0=INput
151 //  GpioDataRegs.GPACLEAR.bit.GPIO4 = 1;     // uncomment if --> Set Low ...
        initially
152 //  GpioDataRegs.GPASET.bit.GPIO4 = 1;       // uncomment if --> Set High ...
        initially
153 //--------------------------------------------------------------
154 //  GPIO-05 - PIN FUNCTION = --Spare--
155     GpioCtrlRegs.GPAMUX1.bit.GPIO5 = 1;      // 0=GPIO,  1=EPWM3B,  ...
          2=Resv,  3=ECAP1
156     GpioCtrlRegs.GPADIR.bit.GPIO5 = 1;       // 1=OUTput,  0=INput
157 //  GpioDataRegs.GPACLEAR.bit.GPIO5 = 1;     // uncomment if --> Set Low ...
        initially
158 //  GpioDataRegs.GPASET.bit.GPIO5 = 1;       // uncomment if --> Set High ...
        initially
159 //--------------------------------------------------------------
160 //  GPIO-06 - PIN FUNCTION = --Spare--
161     GpioCtrlRegs.GPAMUX1.bit.GPIO6 = 1;      // 0=GPIO,  1=EPWM4A,  ...
          2=SYNCI,  3=SYNCO
162     GpioCtrlRegs.GPADIR.bit.GPIO6 = 1;       // 1=OUTput,  0=INput
163 //  GpioDataRegs.GPACLEAR.bit.GPIO6 = 1;     // uncomment if --> Set Low ...
        initially
164 //  GpioDataRegs.GPASET.bit.GPIO6 = 1;       // uncomment if --> Set High ...
        initially
165 //--------------------------------------------------------------
166 //  GPIO-07 - PIN FUNCTION = --Spare--
167     GpioCtrlRegs.GPAMUX1.bit.GPIO7 = 1;      // 0=GPIO,  1=EPWM4B,  ...
          2=SCIRX-A,  3=Resv
168     GpioCtrlRegs.GPADIR.bit.GPIO7 = 1;       // 1=OUTput,  0=INput
169 //  GpioDataRegs.GPACLEAR.bit.GPIO7 = 1;     // uncomment if --> Set Low ...
        initially
170 //  GpioDataRegs.GPASET.bit.GPIO7 = 1;       // uncomment if --> Set High ...
```

```
        initially
171  //-------------------------------------------------------
172  //  GPIO-08 - GPIO-11 Do Not Exist
173  //-------------------------------------------------------
174  //  GPIO-12 - PIN FUNCTION = --Spare--
175       GpioCtrlRegs.GPAMUX1.bit.GPIO12 = 0;     // 0=GPIO,  1=TZ1,  ...
             2=SCITX-A,  3=Resv
176       GpioCtrlRegs.GPADIR.bit.GPIO12 = 0;      // 1=OUTput,  0=INput
177  //   GpioDataRegs.GPACLEAR.bit.GPIO12 = 1;    // uncomment if --> Set Low ...
        initially
178  //   GpioDataRegs.GPASET.bit.GPIO12 = 1;      // uncomment if --> Set High ...
        initially
179  //-------------------------------------------------------
180  //  GPIO-13 - GPIO-15 Do Not Exist
181  //-------------------------------------------------------
182  //-------------------------------------------------------
183  //  GPIO-16 - PIN FUNCTION = --Spare--
184       GpioCtrlRegs.GPAMUX2.bit.GPIO16 = 0;     // 0=GPIO,  1=SPISIMO-A,  ...
             2=Resv,  3=TZ2
185       GpioCtrlRegs.GPADIR.bit.GPIO16 = 0;      // 1=OUTput,  0=INput
186  //   GpioDataRegs.GPACLEAR.bit.GPIO16 = 1;    // uncomment if --> Set Low ...
        initially
187  //   GpioDataRegs.GPASET.bit.GPIO16 = 1;      // uncomment if --> Set High ...
        initially
188  //-------------------------------------------------------------
189  //  GPIO-17 - PIN FUNCTION = --Spare--
190       GpioCtrlRegs.GPAMUX2.bit.GPIO17 = 0;     // 0=GPIO,  1=SPISOMI-A,  ...
             2=Resv,  3=TZ3
191       GpioCtrlRegs.GPADIR.bit.GPIO17 = 0;      // 1=OUTput,  0=INput
192  //   GpioDataRegs.GPACLEAR.bit.GPIO17 = 1;    // uncomment if --> Set Low ...
        initially
193  //   GpioDataRegs.GPASET.bit.GPIO17 = 1;      // uncomment if --> Set High ...
        initially
194  //-------------------------------------------------------------
195  //  GPIO-18 - PIN FUNCTION = --Spare--
196       GpioCtrlRegs.GPAMUX2.bit.GPIO18 = 0;     // 0=GPIO,  1=SPICLK-A,  ...
             2=SCITX-A,  3=XCLKOUT
197       GpioCtrlRegs.GPADIR.bit.GPIO18 = 0;      // 1=OUTput,  0=INput
198  //   GpioDataRegs.GPACLEAR.bit.GPIO18 = 1;    // uncomment if --> Set Low ...
```

```
        initially
199 //  GpioDataRegs.GPASET.bit.GPIO18 = 1;     // uncomment if --> Set High ...
        initially
200 //--------------------------------------------------------------------------
201 //  GPIO-19 - PIN FUNCTION = --Spare--
202     GpioCtrlRegs.GPAMUX2.bit.GPIO19 = 0;    // 0=GPIO,  1=SPISTE-A,  ...
          2=SCIRX-A,  3=ECAP1
203     GpioCtrlRegs.GPADIR.bit.GPIO19 = 0;     // 1=OUTput,  0=INput
204 //  GpioDataRegs.GPACLEAR.bit.GPIO19 = 1;   // uncomment if --> Set Low ...
        initially
205 //  GpioDataRegs.GPASET.bit.GPIO19 = 1;     // uncomment if --> Set High ...
        initially
206 //--------------------------------------------------------------------------
207 //  GPIO-20 - GPIO-27 Do Not Exist
208 //--------------------------------------------------------------------------
209 //  GPIO-28 - PIN FUNCTION = --Spare--
210     GpioCtrlRegs.GPAMUX2.bit.GPIO28 = 0;    // 0=GPIO,  1=SCIRX-A,  ...
          2=I2C-SDA,  3=TZ2
211     GpioCtrlRegs.GPADIR.bit.GPIO28 = 0;     // 1=OUTput,  0=INput
212 //  GpioDataRegs.GPACLEAR.bit.GPIO28 = 1;   // uncomment if --> Set Low ...
        initially
213 //  GpioDataRegs.GPASET.bit.GPIO28 = 1;     // uncomment if --> Set High ...
        initially
214 //--------------------------------------------------------------------------
215 //  GPIO-29 - PIN FUNCTION = --Spare--
216     GpioCtrlRegs.GPAMUX2.bit.GPIO29 = 0;    // 0=GPIO,  1=SCITXD-A,  ...
          2=I2C-SCL,  3=TZ3
217     GpioCtrlRegs.GPADIR.bit.GPIO29 = 0;     // 1=OUTput,  0=INput
218 //  GpioDataRegs.GPACLEAR.bit.GPIO29 = 1;   // uncomment if --> Set Low ...
        initially
219 //  GpioDataRegs.GPASET.bit.GPIO29 = 1;     // uncomment if --> Set High ...
        initially
220 //--------------------------------------------------------------------------
221 //  GPIO-30 - GPIO-31 Do Not Exist
222 //--------------------------------------------------------------------------
223 //--------------------------------------------------------------------------
224 //  GPIO-32 - PIN FUNCTION = --Spare--
225     GpioCtrlRegs.GPBMUX1.bit.GPIO32 = 0;    // 0=GPIO,  1=I2C-SDA,  ...
          2=SYNCI,  3=ADCSOCA
```

```
226     GpioCtrlRegs.GPBDIR.bit.GPIO32 = 0;     // 1=OUTput,  0=INput
227 //  GpioDataRegs.GPBCLEAR.bit.GPIO32 = 1;   // uncomment if --> Set Low ...
        initially
228 //  GpioDataRegs.GPBSET.bit.GPIO32 = 1;     // uncomment if --> Set High ...
        initially
229 //--------------------------------------------------------------
230 //  GPIO-33 - PIN FUNCTION = --Spare--
231     GpioCtrlRegs.GPBMUX1.bit.GPIO33 = 0;    // 0=GPIO,  1=I2C-SCL,  ...
            2=SYNCO,  3=ADCSOCB
232     GpioCtrlRegs.GPBDIR.bit.GPIO33 = 0;     // 1=OUTput,  0=INput
233 //  GpioDataRegs.GPBCLEAR.bit.GPIO33 = 1;   // uncomment if --> Set Low ...
        initially
234 //  GpioDataRegs.GPBSET.bit.GPIO33 = 1;     // uncomment if --> Set High ...
        initially
235 //--------------------------------------------------------------
236 //  GPIO-34 - PIN FUNCTION = LED for F28027 USB dongle
237     GpioCtrlRegs.GPBMUX1.bit.GPIO34 = 0;    // 0=GPIO,  1=COMP2OUT,  ...
            2=EMU1,  3=Resv
238     GpioCtrlRegs.GPBDIR.bit.GPIO34 = 1;     // 1=OUTput,  0=INput
239 //  GpioDataRegs.GPBCLEAR.bit.GPIO34 = 1;   // uncomment if --> Set Low ...
        initially
240     GpioDataRegs.GPBSET.bit.GPIO34 = 1;     // uncomment if --> Set High ...
            initially
241 //--------------------------------------------------------------
242     EDIS;   // Disable register access
243 }
244 //================================
245 // NOTE:
246 // IN MOST APPLICATIONS THE FUNCTIONS AFTER THIS POINT CAN BE LEFT UNCHANGED
247 // THE USER NEED NOT REALLY UNDERSTAND THE BELOW CODE TO SUCCESSFULLY RUN ...
        THIS
248 // APPLICATION.
249 //================================
250 void WDogDisable(void)
251 {
252     EALLOW;
253     SysCtrlRegs.WDCR= 0x0068;
254     EDIS;
255 }
```

```
256 // This function initializes the PLLCR register.
257 //void InitPll(Uint16 val, Uint16 clkindiv)
258 void PLLset(Uint16 val)
259 {
260    volatile Uint16 iVol;
261    // Make sure the PLL is not running in limp mode
262    if (SysCtrlRegs.PLLSTS.bit.MCLKSTS != 0)
263    {
264       EALLOW;
265       // OSCCLKSRC1 failure detected. PLL running in limp mode.
266       // Re-enable missing clock logic.
267       SysCtrlRegs.PLLSTS.bit.MCLKCLR = 1;
268       EDIS;
269       // Replace this line with a call to an appropriate
270       // SystemShutdown(); function.
271       asm("        ESTOP0");     // Uncomment for debugging purposes
272    }
273    // DIVSEL MUST be 0 before PLLCR can be changed from
274    // 0x0000. It is set to 0 by an external reset XRSn
275    // This puts us in 1/4
276    if (SysCtrlRegs.PLLSTS.bit.DIVSEL != 0)
277    {
278        EALLOW;
279        SysCtrlRegs.PLLSTS.bit.DIVSEL = 0;
280        EDIS;
281    }
282    // Change the PLLCR
283    if (SysCtrlRegs.PLLCR.bit.DIV != val)
284    {
285       EALLOW;
286       // Before setting PLLCR turn off missing clock detect logic
287       SysCtrlRegs.PLLSTS.bit.MCLKOFF = 1;
288       SysCtrlRegs.PLLCR.bit.DIV = val;
289       EDIS;
290       // Optional: Wait for PLL to lock.
291       // During this time the CPU will switch to OSCCLK/2 until
292       // the PLL is stable.  Once the PLL is stable the CPU will
293       // switch to the new PLL value.
294       //
```

```
295         // This time-to-lock is monitored by a PLL lock counter.
296         //
297         // Code is not required to sit and wait for the PLL to lock.
298         // However, if the code does anything that is timing critical,
299         // and requires the correct clock be locked, then it is best to
300         // wait until this switching has completed.
301         // Wait for the PLL lock bit to be set.
302         // The watchdog should be disabled before this loop, or fed within
303         // the loop via ServiceDog().
304         // Uncomment to disable the watchdog
305         WDogDisable();
306         while(SysCtrlRegs.PLLSTS.bit.PLLLOCKS != 1) {}
307         EALLOW;
308         SysCtrlRegs.PLLSTS.bit.MCLKOFF = 0;
309         EDIS;
310         }
311         //divide down SysClk by 2 to increase stability
312         EALLOW;
313         SysCtrlRegs.PLLSTS.bit.DIVSEL = 2;
314         EDIS;
315 }
316
317 // This function initializes the PIE control registers to a known state.
318 //
319 void PieCntlInit(void)
320 {
321     // Disable Interrupts at the CPU level:
322     DINT;
323     // Disable the PIE
324     PieCtrlRegs.PIECTRL.bit.ENPIE = 0;
325     // Clear all PIEIER registers:
326     PieCtrlRegs.PIEIER1.all = 0;
327     PieCtrlRegs.PIEIER2.all = 0;
328     PieCtrlRegs.PIEIER3.all = 0;
329     PieCtrlRegs.PIEIER4.all = 0;
330     PieCtrlRegs.PIEIER5.all = 0;
331     PieCtrlRegs.PIEIER6.all = 0;
332     PieCtrlRegs.PIEIER7.all = 0;
333     PieCtrlRegs.PIEIER8.all = 0;
```

```
334     PieCtrlRegs.PIEIER9.all = 0;
335     PieCtrlRegs.PIEIER10.all = 0;
336     PieCtrlRegs.PIEIER11.all = 0;
337     PieCtrlRegs.PIEIER12.all = 0;
338     // Clear all PIEIFR registers:
339     PieCtrlRegs.PIEIFR1.all = 0;
340     PieCtrlRegs.PIEIFR2.all = 0;
341     PieCtrlRegs.PIEIFR3.all = 0;
342     PieCtrlRegs.PIEIFR4.all = 0;
343     PieCtrlRegs.PIEIFR5.all = 0;
344     PieCtrlRegs.PIEIFR6.all = 0;
345     PieCtrlRegs.PIEIFR7.all = 0;
346     PieCtrlRegs.PIEIFR8.all = 0;
347     PieCtrlRegs.PIEIFR9.all = 0;
348     PieCtrlRegs.PIEIFR10.all = 0;
349     PieCtrlRegs.PIEIFR11.all = 0;
350     PieCtrlRegs.PIEIFR12.all = 0;
351 }
352 void PieVectTableInit(void)
353 {
354     int16 i;
355     PINT *Dest = &PieVectTable.TINT1;
356     EALLOW;
357     for(i=0; i < 115; i++)
358     *Dest++ = &ISR_ILLEGAL;
359     EDIS;
360     // Enable the PIE Vector Table
361     PieCtrlRegs.PIECTRL.bit.ENPIE = 1;
362 }
363 interrupt void ISR_ILLEGAL(void)   // Illegal operation TRAP
364 {
365   // Insert ISR Code here
366   // Next two lines for debug only to halt the processor here
367   // Remove after inserting ISR Code
368   asm("          ESTOP0");
369   for(;;);
370
371 }
372 // This function initializes the Flash Control registers
```

```
373 //                    CAUTION
374 // This function MUST be executed out of RAM. Executing it
375 // out of OTP/Flash will yield unpredictable results
376 void InitFlash(void)
377 {
378    EALLOW;
379    //Enable Flash Pipeline mode to improve performance
380    //of code executed from Flash.
381    FlashRegs.FOPT.bit.ENPIPE = 1;
382    //                CAUTION
383    //Minimum waitstates required for the flash operating
384    //at a given CPU rate must be characterized by TI.
385    //Refer to the datasheet for the latest information.
386    //Set the Paged Waitstate for the Flash
387    FlashRegs.FBANKWAIT.bit.PAGEWAIT = 3;
388    //Set the Random Waitstate for the Flash
389    FlashRegs.FBANKWAIT.bit.RANDWAIT = 3;
390    //Set the Waitstate for the OTP
391    FlashRegs.FOTPWAIT.bit.OTPWAIT = 5;
392    //                CAUTION
393    //ONLY THE DEFAULT VALUE FOR THESE 2 REGISTERS SHOULD BE USED
394    FlashRegs.FSTDBYWAIT.bit.STDBYWAIT = 0x01FF;
395    FlashRegs.FACTIVEWAIT.bit.ACTIVEWAIT = 0x01FF;
396    EDIS;
397    //Force a pipeline flush to ensure that the write to
398    //the last register configured occurs before returning.
399    asm(" RPT #7 || NOP");
400 }
401 // This function will copy the specified memory contents from
402 // one location to another.
403 //
404 //  Uint16 *SourceAddr        Pointer to the first word to be moved
405 //                           SourceAddr < SourceEndAddr
406 //  Uint16* SourceEndAddr     Pointer to the last word to be moved
407 //  Uint16* DestAddr          Pointer to the first destination word
408 //
409 // No checks are made for invalid memory locations or that the
410 // end address is > then the first start address.
411 void MemCopy(Uint16 *SourceAddr, Uint16* SourceEndAddr, Uint16* DestAddr)
```

```
412 {
413     while(SourceAddr < SourceEndAddr)
414     {
415         *DestAddr++ = *SourceAddr++;
416     }
417     return;
418 }
419 //==============================
420 // End of file.
421 //==============================
```

Appendix C

Planar Magnetics Modeling Approach

C.1 Derivation of the Lumped Circuit Model

This appendix derives the lumped circuit model in detail. All variables are the same as those utilized in Section 4.3.

C.1.1 Modeling a one-turn layer

Under the 1-D approximation, the magnetic field within a conductive layer satisfies the 1-D diffusion equation [116]

$$\frac{1}{\mu\sigma}\nabla^2 H_x = \frac{dH_x}{dt}. \tag{C.1}$$

Its solution is

$$H_x(z) = \frac{[H_T \sinh(\Psi z) + H_B \sinh(\Psi(h-z))]}{\sinh(\Psi h)}. \tag{C.2}$$

Here $\Psi = \frac{1+j}{\delta}$, $\delta = \sqrt{\frac{2}{\omega\mu_r\mu_0\sigma}}$. Using *Ampere's Law* under the MQS approximation: $\nabla \times H_x(z) = J_y(z) = \sigma E_y(z)$, gives

$$E_y(z) = \frac{\Psi}{\sigma}\left[\frac{H_T e^{\Psi h} - H_B}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi(h-z)} - \frac{H_B e^{\Psi h} - H_T}{e^{\Psi h} - e^{-\Psi h}} e^{-\Psi z}\right]. \tag{C.3}$$

At the top and bottom surface of the conductor (i.e. when $z = 0$ and $z = h$), (C.3) gives

$$\begin{aligned} E_T = E_y(h) &= \frac{\Psi}{\sigma}[\frac{H_T e^{\Psi h} - H_B}{e^{\Psi h} - e^{-\Psi h}} - \frac{H_B - H_T e^{-\Psi h}}{e^{\Psi h} - e^{-\Psi h}}] \\ E_B = E_y(0) &= \frac{\Psi}{\sigma}[\frac{H_T - H_B e^{-\Psi h}}{e^{\Psi h} - e^{-\Psi h}} - \frac{H_B e^{\Psi h} - H_T}{e^{\Psi h} - e^{-\Psi h}}]. \end{aligned} \tag{C.4}$$

Defining impedance Z_a and Z_b as

$$\begin{aligned} Z_a &= \frac{\Psi(1 - e^{-\Psi h})}{\sigma(1 + e^{-\Psi h})} \\ Z_b &= \frac{2\Psi e^{-\Psi h}}{\sigma(1 - e^{-2\Psi h})}, \end{aligned} \tag{C.5}$$

allows (C.4) to be simplified to

$$\begin{aligned} E_T &= Z_a H_T + Z_b(H_T - H_B) \\ E_B &= Z_b(H_T - H_B) - Z_a H_B. \end{aligned} \tag{C.6}$$

Also by *Ampere's Law*

$$(H_T - H_B)w = I = Kw, \tag{C.7}$$

combining (C.6) and (C.7), we get

$$\begin{aligned} E_T &= Z_a H_T + Z_b K \\ E_B &= Z_b K - Z_a H_B. \end{aligned} \tag{C.8}$$

This yields (4.1) and (4.3) in Section 4.3.1.

C.1.2 Modeling two adjacent one-turn layers

In Fig. 4-3a, consider a closed loop surrounding the center post that includes the bottom surface of layer 1 and the external voltage source V_1. Applying *Faraday's Law* to the loop gives

$$E_{B1}d - V_1 = -\frac{d\Phi_{B1}}{dt}, \tag{C.9}$$

where Φ_{B1} is the magnetic flux in the center post across the bottom surface of layer 1. Similarly, consider a closed loop surrounding the center post that includes the top surface of layer 2 and the external voltage source V_2,

$$E_{T2}d - V_2 = -\frac{d\Phi_{T2}}{dt}, \tag{C.10}$$

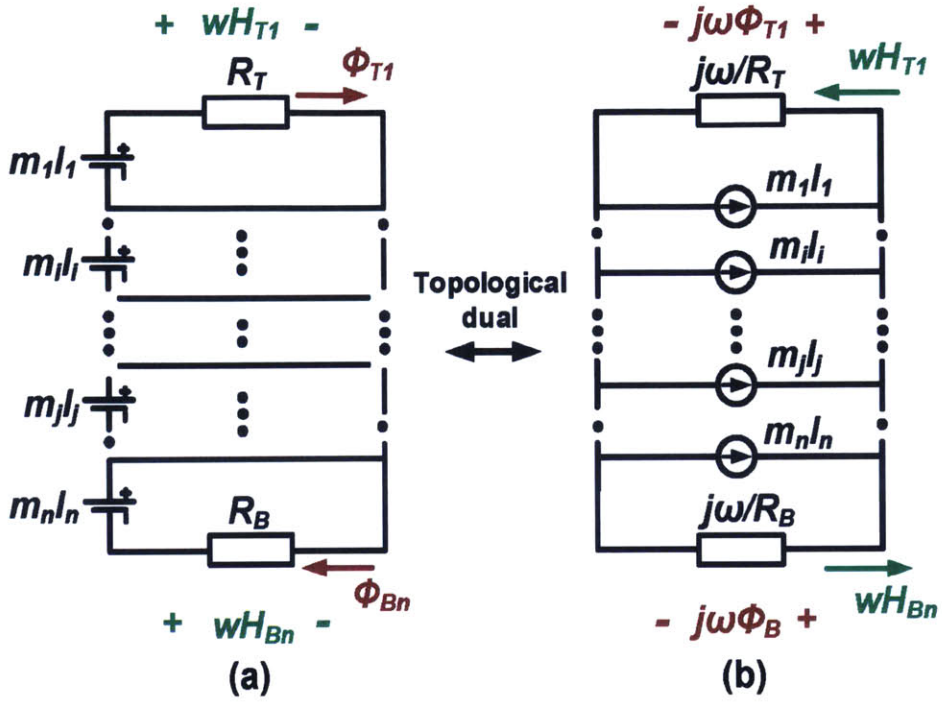


Figure C-1: Magnetic reluctance circuit model of a planar structure with (a) MMFs modeled as voltage sources, and (b) its topological dual with MMFs modeled as current sources. All reluctance values are replaced by the time derivative of the corresponding permeances ($j\omega\frac{1}{\Re}$). If complex reluctances are used, the core loss is naturally captured by the model. Fig. C-1b can be merged with Fig. 4-4b becoming Fig. 4-6, with across ($j\omega\Phi$) and through (wH) variables mapped one-by-one with each other.

where Φ_{T2} is the magnetic flux in the center post across the top surface of layer 2. Now, the magnetic flux penetrating into the center post through the spacing between the two layers (Φ_{S12}), equals $\mu_0 a_1 dH_{S12}$. Using flux continuity, $\Phi_{T2} = \Phi_{B1} + \Phi_{S12}$, and taking the derivative gives

$$\frac{d\Phi_{T2}}{dt} = \frac{d\Phi_{B1}}{dt} + \frac{d\Phi_{S12}}{dt}. \tag{C.11}$$

Combining (C.9)-(C.11) gives

$$H_{S12} = \frac{1}{j\omega\mu_0 a_1}\left(\frac{V_2}{d} - E_{T2} - \frac{V_1}{d} + E_{B1}\right). \tag{C.12}$$

This yields (4.6) in Section 4.3.2.

C.1.3 Modeling the magnetic core and the air gaps

The modeling of the magnetic core and air gaps in the MLM approach was derived directly using Maxwell's equations in a following appendix . Here we present a more generally applicable derivation closely related to the conventional magnetic reluctance circuit model, to highlight a different way of interpreting this model, and to tie this work with other reluctance-based core models, especially the Gyrator-Capacitor approaches which utilize the concept of magnetic and electrical circuit duality [127,128]. This derivation also releases the requirement of 1-D field distribution from the core region, leaving the 1-D assumption only required in the winding region.

Assuming $\mathcal{R}_T$ is the reluctance of the top side of the core, and $\mathcal{R}_B$ is the reluctance of the bottom side of the core, a magnetic circuit model as shown in Fig. C-1a can be generated. This model captures the electromagnetic interactions related the core, but doesn't capture those in the windings. To make this model compatible with the modeling of the winding stack, we take the topological dual of this circuit by modeling the Magneto-Motive-Force (MMF) generators as current sources and taking the time derivative of all permeances ($j\omega\frac{1}{\mathcal{R}}$), as shown in Fig. C-1b. This circuit, which models the core and the air gaps, can be merged with the circuit in Fig. 4-4b (using n modular impedance networks to model n layers), which captures the conductors and spacings, with all across ($j\omega\Phi$) and through (wH) variables mapped one-by-one with each other. The merged circuit contains all information and is shown in Fig. 4-6. Specifically, Φ_{T1} is the magnetic flux carried by the top side of the core; Φ_{B1} is the magnetic flux carried by the bottom side of the core; wH_{T1} equals the integral of the H field strength along any trace through the top side of the magnetic core; wH_{Bn} equals the integral of the H field strength along any trace through the bottom side of the magnetic core. By relating the E, V, Φ, H, and $\mathcal{R}$,

$$\begin{aligned} dE_{T1} - \frac{V_1}{m_1} &= -j\omega\Phi_{T1} = -\frac{j\omega}{\mathcal{R}_T} wH_{T1} \\ dE_{Bn} - \frac{V_n}{m_n} &= -j\omega\Phi_{Bn} = \frac{j\omega}{\mathcal{R}_B} wH_{Bn}. \end{aligned} \tag{C.13}$$

This yields (4.9) in Section 4.3.3.

C.2 An Alternative Way of Modeling the Core and the Air Gap

Here we present an alternative way to model the magnetic core and the air gap in the lumped model. Loop 1 in Fig. C-2 comprises the spacing between the top surface of layer 1 and the core, the center post, the spacing between bottom surface of layer n and the core, and the outer surface. Integrating the magnetic field in this loop gives

$$(H_{T1} - H_{Bn})w = \sum_{i=1}^{n} I_i. \tag{C.14}$$

Here we only include the top and bottom sides of the loop, because either the high permeability of the core makes the H value inside of it negligible, or the length of the core legs is much smaller than the window width. Loop 2 in Fig. C-2 comprises the top of the core, the center post, the air gap and the bottom of the core. Integrating the magnetic field along this loop gives

$$H_{Ag}(g_1 + g_2) - H_{FB}w + H_{FT}w = \sum_{i=1}^{n} I_i. \tag{C.15}$$

Here H_{Ag} is the field strength in the air gap, H_{FT} is the field strength in the top magnetic core, H_{FB} is the field strength in the bottom magnetic core, and $(g_1 + g_2)$ is the total length of the air gap. Using flux continuity,

$$\begin{aligned} H_{T1} &= H_{FT} \\ \mu_0\mu_r c_b d H_{FB} &= -\mu_0 A_c H_{Ag}. \end{aligned} \tag{C.16}$$

Combining (C.14)-(C.16), H_{Ag} can be calculated from H_{Bn}

$$H_{Ag} = -\frac{H_{Bn}w}{g_1 + g_2 + \frac{A_c w}{\mu_r cd}}. \tag{C.17}$$

The magnetic flux that flows through the center post and across the top surface of layer 1, Φ_{T1}, is

$$\Phi_{T1} = \mu_r\mu_0 cd H_{FT} + \mu_0 b_t d H_{T1} = (\mu_r\mu_0 cd + \mu_0 b_t d)H_{T1}. \tag{C.18}$$

Using Faraday's law and integrating the electric field along the top surface of layer 1 and

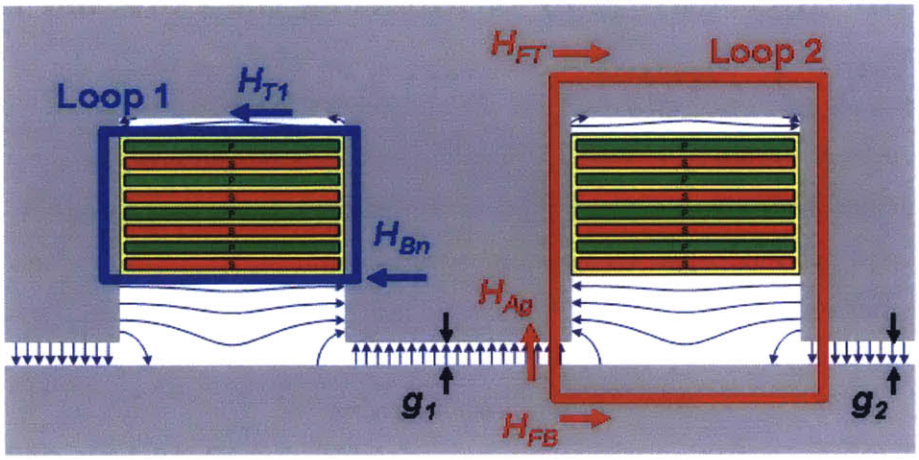


Figure C-2: Two H field loops for deriving the impedances representing the core and the air gap.

the external voltage source V_1

$$E_{T1} - \frac{V_1}{d} = -j\omega\mu_r\mu_0 c_b H_{T1} - j\omega\mu_0 b_t H_{T1}. \tag{C.19}$$

Similarly, the magnetic flux flowing through the center post and across the bottom surface of layer n, Φ_{Bn}, is

$$\Phi_{Bn} = \mu_0 A_c H_{Ag} - \mu_0 b d H_{T1} = -\frac{\mu_0 A_c w}{g + \frac{A_c w}{\mu_r c_b d}} H_{Bn} - \mu_0 b_b d H_{Bn}. \tag{C.20}$$

Integrating the electric field along the bottom surface of layer n, and the external voltage source V_n, gives

$$E_{Bn} - \frac{V_n}{d} = j\omega \frac{\mu_0 A_c w}{g + \frac{A_c w}{\mu_r c_b d} d} H_{Bn} + j\omega\mu_0 b_b H_{Bn}. \tag{C.21}$$

(C.19) and (C.21) are two specific formats of (4.9) in Section 4.2 for the magnetic core utilized in this example (Fig. C-2).

C.3 Cantilever Model Parameter Extraction

Figure C-3a shows the widely used cantilever model for magnetic structures with multiple windings [94]. This model is closely related to the inductance matrix description, which comprises self and mutual inductances of the multiple windings. The proposed lumped circuit model integrally-captures the self and mutual inductances and resistances (i.e. impedances), enabling the development of an impedance-based cantilever model, as an enhancement to the inductance-based cantilever model. Figure C-3b shows the proposed impedance-based cantilever model for an N winding structure. A resistance element is added in series with each inductance element to model the self and mutual resistances. For example, R_{11} and L_{11} model the self resistance and self inductance of winding W_1; and L_{jk} and R_{jk} (connects windings W_j and W_k) model the mutual resistance and mutual inductance between winding W_j and W_k (referred as mutual impedance $Z_{jk} = R_{jk} + j\omega L_{jk}$). The effective turns ratios, n_2 to n_N, represent the ratios of the voltages of winding W_2 to W_N to the voltage of winding W_1 under open-circuit conditions. With the presence of impedance elements in the model, the effective turns ratios, n_2 to n_N, are no longer real, but instead complex.

With the lumped circuit model, parameters of the impedance-based cantilever model can be extracted from circuit simulations, which are usually easier to implement and much faster than experimental measurements or FEM simulations. For a planar structure with N windings, the lumped circuit model uses N winding ports to represent the N physical ports. All layer connections, electrical vias, field couplings, etc., are modeled and encapsulated behind the N ports. Each winding port in the lumped circuit model can be treated like a physical port in open- and short-circuit simulations. As a result, the parameter extraction method described in [94] (based on open and short circuit measurements) can be directly applied to the lumped circuit model.

These parameter extractions can be conducted by applying small-signal ac analysis in circuit simulations. The self impedance Z_{11} is determined by open-circuiting windings W_2 to W_N, and measuring the voltage and current of winding W_1. To measure the effective turns ratios n_2 to n_N, a voltage is applied to winding W_1. The open-circuit voltage of winding W_2-W_N are measured and recorded as v_1 to v_N. The effective turns ratio n_k is

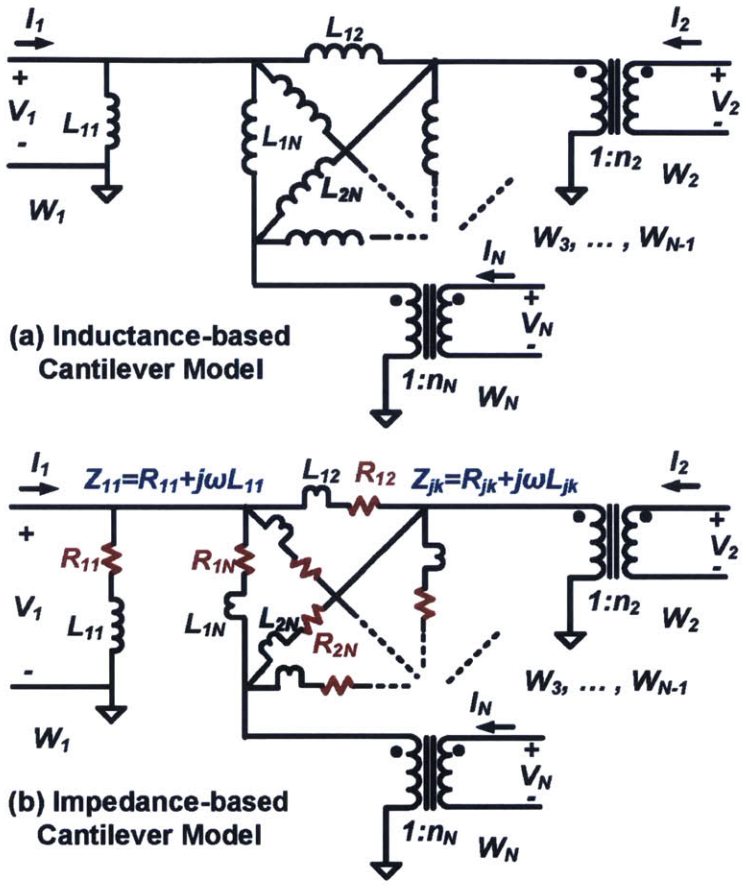


Figure C-3: (a) Conventional inductance-based cantilever model [94], and (b) proposed impedance-based cantilever model with self and mutual impedances.

given by

$$n_k = \frac{v_k}{v_1}, k = 2, ..., N. \tag{C.22}$$

Note that n_k is complex as v_k and v_1 are both complex (n_k may have negative real and/or imaginary parts).

To measure the mutual impedance Z_{jk}, winding W_j is driven with a voltage source v_j, with all other windings short-circuited, and the current i_k in winding W_k is measured. The effective mutual impedance Z_{jk} is given by

$$Z_{jk} = \frac{v_j}{n_j n_k i_k}. \tag{C.23}$$

To normalize the model, n_1 is taken as 1. It is possible for Z_{jk} to have negative real

and/or imaginary parts. Similar open- and short-circuit simulations can also be conducted to extract elements of the impedance matrix and the admittance matrix using the lumped circuit model [117,119].

The impedance matrix $\{z_{jk}\}_{N\times N}$, admittance matrix $\{y_{jk}\}_{N\times N}$, the winding voltage vector $V_{N\times 1} = [v_1;...;v_N]_{N\times 1}$, and the winding current vector $I_{N\times 1} = [i_1;...;i_N]_{N\times 1}$ are related by

$$\begin{cases} V_{N\times 1} = \{z_{jk}\}_{N\times N} I_{N\times 1} \\ \{y_{jk}\}_{N\times N} V_{N\times 1} = I_{N\times 1} \\ \{z_{jk}\}_{N\times N} = \{y_{jk}\}^{-1}_{N\times N}. \end{cases} \tag{C.24}$$

The impedance-based cantilever model is closely related to the impedance matrix and the admittance matrix. Using Eq. C.22 and Eq. C.23 and corresponding measurement setups, the parameters of the impedance-based cantilever model can be found from $\{z_{jk}\}_{N\times N}$ and $\{y_{jk}\}_{N\times N}$ using

$$\begin{cases} Z_{11} = z_{11} \\ n_j = \frac{z_{1j}}{z_{11}} \\ Z_{jk} = -\frac{1}{n_j n_k y_{jk}}. \end{cases} \tag{C.25}$$

Conversely, the elements of $\{z_{jk}\}_{N\times N}$ and $\{y_{jk}\}_{N\times N}$ can be expressed in terms of the parameters of the impedance-based cantilever model by

$$\begin{cases} y_{jk} = -\frac{1}{n_j n_k Z_{jk}}, \text{when j} \neq \text{k} \\ y_{jj} = \frac{1}{n_j}\sum_{k=1}^{N}\frac{1}{z_{kj}}, \text{with } z_{jj} = \begin{cases} \infty \text{ if j} \neq 1 \\ Z_{11} \text{ when j} = 1 \end{cases} \\ \{z_{jk}\}_{N\times N} = \{y_{jk}\}^{-1}_{N\times N}. \end{cases} \tag{C.26}$$

Hence, the impedance-based cantilever model is interchangeable with the impedance matrix and the admittance matrix. As demonstrated, all parameters of the cantilever model, the impedance matrix, and the admittance matrix can be extracted from the lumped circuit model by rapid simulations.

C.4 An Automatic Parameter Extraction Algorithm

Assume the ferrite core has infinite permeability, the impedances on the two sides of the lumped circuit model, which represent the top and bottom ferrite, can be eliminated. The simplified lumped circuit model for a m-layer planar magnetic structure is shown in Figure C-4. It consists m iterating cells, representing the m layers, and an impedance Z, representing the air gap. Each iterating cell has two impedances, X_i and Y_i. These m layers are configured into n windings through vias. The goal of this algorithm is to find the "Winding-to-Winding" impedance matrix in a general case.

"Layer-to-Layer" impedance matrix - M_{L2L}

The "Layer-to-Layer" impedance matrix (M_{L2L}) correlates the voltages and currents of the m layer ports. It can be written as:

$$\begin{bmatrix} V_1 \\ \cdots \\ V_i \\ \cdots \\ V_m \end{bmatrix} = M_{L2L} \begin{bmatrix} I_1 \\ \cdots \\ I_i \\ \cdots \\ I_m \end{bmatrix} = \begin{bmatrix} Z_{11} & \cdots & Z_{1j} & \cdots & Z_{1m} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{i1} & \cdots & Z_{ij} & \cdots & Z_{im} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Z_{m1} & \cdots & Z_{mj} & \cdots & Z_{mm} \end{bmatrix} \begin{bmatrix} I_1 \\ \cdots \\ I_i \\ \cdots \\ I_m \end{bmatrix} \tag{C.27}$$

Based on the lumped circuit model of Fig. C-4, using superposition rules, each elements of M_{L2L} can be calculated by:

$$\begin{cases} Z_{ii} = X_i + \sum_{k=i}^{m} Y_k + Z. \\ Z_{ij} = Z_{ji} = \sum_{k=\max(i,j)}^{m} Y_k + Z. \end{cases} \tag{C.28}$$

Voltage conversion matrix - Q_V

Suppose there are m layer ports, n winding ports, the voltage conversion matrix Q_V converts the voltage of each layer port ($[V_{L1} \sim V_{Lm}]$) into the voltage of each winding port ($[V_{W1} \sim V_{Wn}]$). As a result, the Q_V is a $n \times m$ matrix which satisfies:

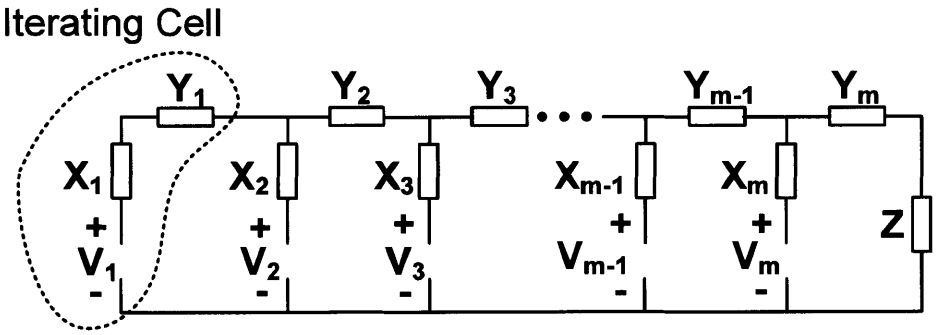


Figure C-4: Lumped circuit model for a m layer planar structure with iterating cells and ideal magnetic coupling.

$$\begin{bmatrix} V_{W1} \\ \cdots \\ V_{Wi} \\ \cdots \\ V_{Wn} \end{bmatrix} = \begin{bmatrix} Q_{V11} & \cdots & Q_{V1j} & \cdots & Q_{V1m} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Q_{Vi1} & \cdots & Q_{Vij} & \cdots & Q_{Vim} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Q_{Vn1} & \cdots & Q_{Vnj} & \cdots & Q_{Vnm} \end{bmatrix}_{n \times m} \begin{bmatrix} V_{L1} \\ \cdots \\ V_{Lj} \\ \cdots \\ V_{Lm} \end{bmatrix} \tag{C.29}$$

Each element of Q_{Vij} can be found by applying the following two rules:

- if winding i consists series-connected layers, and layer j belongs to winding i, then $Q_{Vij} = 1$; Otherwise, $Q_{Vij} = 0$. This rule represents a constraint that the voltage across a winding that contains series-connected layers are the summation of the voltages of all individual layers.

- if winding i consists parallel-connected layers, and layers j, k, l belong to winding i, then set any one of Q_{Vij}, Q_{Vik}, or Q_{Vil} be 1, and all other Qs on the same row as 0 (only one element in a row can be 1). This rule represents a constraint that the voltage across a winding that consists parallel-connected layers equals the voltage of any layer that belongs to this winding.

Current conversion matrix - Q_C

Suppose there are m layer ports, n winding ports, the current conversion matrix Q_C converts the voltage of each winding port ($[I_{W1} \sim I_{Wn}]$) into the current of each layer port ($[I_{L1} \sim$

I_{Lm}]). As a result, the Q_C is a $m \times n$ matrix which satisfies:

$$\begin{bmatrix} I_{L1} \\ \cdots \\ I_{Li} \\ \cdots \\ I_{Lm} \end{bmatrix} = \begin{bmatrix} Q_{C11} & \cdots & Q_{C1j} & \cdots & Q_{C1n} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Q_{Ci1} & \cdots & Q_{Cij} & \cdots & Q_{Cin} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ Q_{Cm1} & \cdots & Q_{Cmj} & \cdots & Q_{Cmn} \end{bmatrix}_{m \times n} \begin{bmatrix} I_{W1} \\ \cdots \\ I_{Wj} \\ \cdots \\ I_{Wn} \end{bmatrix} \tag{C.30}$$

Each element of Q_{Cij} can be found by applying the following two rules:

- if layer i belongs to a series-connected winding j, then $Q_{Cij} = 1$; Otherwise, $Q_{Cij} = 0$. This rule represents a constraint that the current across all layers that belong to a series-connected winding has identical current which is equal to the winding current.
- if layer i, k, l all belongs to a parallel-connected winding j, then set Q_{Cij}, Q_{Ckj}, and Q_{Clj} be w_{ij}, w_{kj} and w_{lj}, respectively. w_{ij}, w_{kj} and w_{lj} are the current sharing weights among these layers, and $w_{ij} + w_{kj} + w_{lj} = 1$. This rule represents a constraint that the current of a parallel-connected winding equals the summation of the currents of all layers belonging to this winding.

"Winding-to-Winding" impedance matrix - M_{W2W}

Finally, the $n \times n$ "Winding-to-Winding" impedance matrix, M_{W2W}, is a product of the $n \times m$ voltage conversion matrix Q_V, the $m \times m$ "Layer-to-Layer" impedance matrix M_{L2L}, and the $m \times n$ current conversion matrix Q_C:

$$M_{W2W} = Q_V M_{L2L} Q_C. \tag{C.31}$$

This M_{W2W} represents the voltage and current couplings among windings, and can be used to generate equivalent circuit models for more complex planar structures (e.g. cantilever model for multiple winding transformers [94]).

Appendix D

M2Spice - A Magnetics to SPICE Netlists Conversion Tool

D.1 A Brief Software Tutorial

Based on the magnetic modeling approach derived in Chapter 4, a magnetics to SPICE netlists conversion tool has been written in Matlab and Python. It takes in the geometry information of the magnetic structure, and produces a circuit netlists that can be analyzed in a SPICE environment (currently supporting LTspice). Fig. D-1 shows a screenshot of the software graphical user interface (GUI).

The GUI of the software can be divided into two regions: a function region that has eight buttons, and a input region that can take in the geometry information. Here we briefly introduce the function of each the eight buttons.

1. **Load Geometry**: This button allows the user to load a geometry file that has been previously saved. Once this button is clicked, a standard dialog box will be opened to allow the user to select the desired geometry file. The geometry file should be in .txt format, with each row start with the variable name (listed in the first column of the input region), and finished with the real values. There should be 17 rows of variables with the 18th row (name of the component) optional. The software will perform a variable check on the 17 variables one row after another. If one row of data is correct, the information will be forwarded into the entries in the input region.
2. **Save Geometry**: This button allows the user to save a already typed geometry

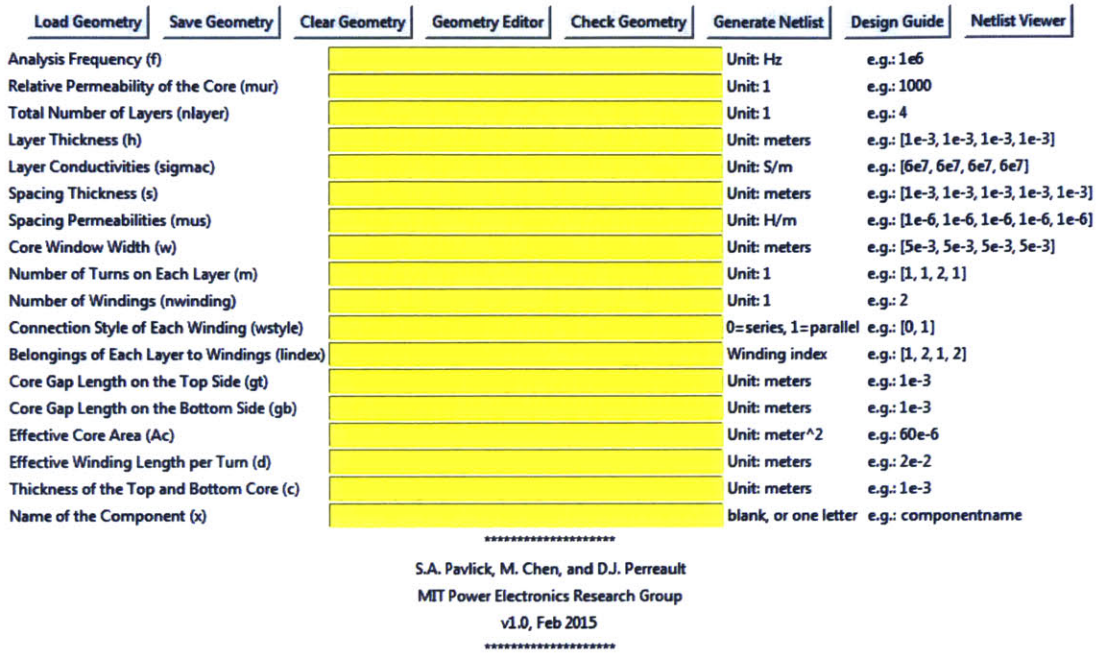


Figure D-1: The user interface of the magnetics to SPICE netlists conversion tool - *M2Spice*.

information for future use. All information that are listed in the input region will be saved into a .txt file that can be read by the Load Geometry button.

3. **Clear Geometry**: This button clears all information that is currently listed in the input region.

4. **Geometry Editor**: This button opens a new dialog box for the user to easily edit the geometry information (especially if the geometry information is long).

5. **Check Geometry**: This button performs a more detailed check on the geometry information that is already listed in the input region. For example, the number of windings (nwinding) should be equal to the length of the winding thickness variable (h). If there exist mismatches, the error will be indicated and a dialog box will be opened. If there is no mismatch, a dialog box will be opened to tell the user that the geometry has no error.

6. **Generate Geometry**: If the geometry information has no error, this button will produce a netlist that the user can save to a destination .txt file, or open in the netlist

viewer (through another dialog box). If the geometry information has errors, a dialog box will be opened to inform the user. In this case, the "Check Geometry" process should be run again.

7. **Design Guide**: This button provide some basic tutorial information.
8. **Netlist Viewer**: This button opens a dialog box that shows the generated netlists.

The input region has eighteen rows of variables that describe a 1-D planar magnetics. Names of the variables are listed in the first column from the left. Variable entries are in the second column from the left. The corresponding unit of the variables are listed in the third column from the left. The fourth column from the left lists the example variable formats.

An example geometry file with three conductor layers is shown as following:

```
Ac = 19.9e-6
gt = 0
lindex = [1,2,2]
mus = [1.2e-6,1.2e-6,1.2e-6,1.2e-6]
mur = 1000
nwinding = 2
h = [0.071e-3,0.071e-3,0.071e-3]
f = 800000
m = [1,2,2]
c = 1.1e-3
sigmac = [5.8e7,5.8e7,5.8e7]
s = [0.2e-3,1e-3,0.12e-3,0.10e-3]
wstyle = [0,1]
gb = 0
w = [3e-3,3e-3,3e-3]
x = one
nlayer = 3
d = 18e-3
```

This file should be saved as .txt format and can be read by the "Load Geometry" function of *M2Spice*. Once the information is read. The GUI looks like Fig. D-2. Click the "Check Geometry" button. A dialog box will be opened which tells the user that the geometry information is correct. Then click "Generate Netlist" and select the saving destination. A netlist will be produced. This netlist can be copied-and-pasted into a SPICE environment.

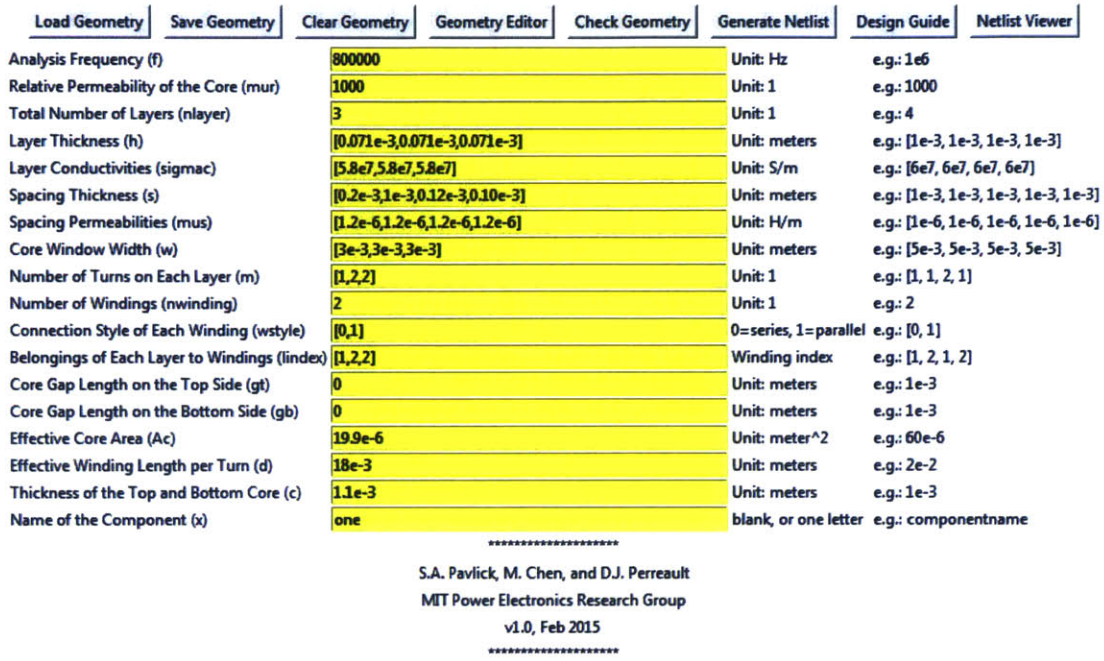


Figure D-2: A screen-shot of the *M2Spice* user interface after the magnetics geometry information being loaded.

Here is the generated netlist for the 3 layer planar magnetics structure.

```
1  **********************************************************************
2  *****         Mon May 04 02:48:53 2015 by Minjie           *****
3  **********************************************************************
4  **********************************************************************
5  ******* Comprehensive  Summary of the Magnetic Structure  ********
6  ******* Please double check the geometry information and  ********
7  **** use the external Port Name to interface with your circuit ***
8  **********************************************************************
9
10 * The name of the component is: _one. This name can only be used once in ...
       a circuit.
11
12 * This planar structure has 2 windings and 3 layers
13
14 * -> All layers in winding 1 are Series Connected;
```

```
15 * -> Its external Port Name: PortP1_one, PortN1_one
16 * ---> Includes Layer 1
17 * -----> thickness 71.00um, width 3.00mm, turns 1, spacing above 0.20mm, ...
       spacing below 1.00mm
18 * -> Winding 1 has 1 total turns;
19
20 * -> All layers in winding 2 are Parallel Connected;
21 * -> Its external Port Name: PortP2_one, PortN2_one
22 * ---> Includes Layer 2
23 * -----> thickness 71.00um, width 3.00mm, turns 2, spacing above 1.00mm, ...
       spacing below 0.12mm
24 * ---> Includes Layer 3
25 * -----> thickness 71.00um, width 3.00mm, turns 2, spacing above 0.12mm, ...
       spacing below 0.10mm
26 * -> Winding 2 has 4 total turns;
27 ****************************************************************
28
29 ****************************************************************
30 *****                    Netlist Starts                    ********
31 ****************************************************************
32
33 *NetList for Layer 1
34 Le1_one N1_one P1_one 1 Rser=1f
35 Li1_one G_one Md1_one 1 Rser=1f
36 Lg1_one Mg1_one Md1_one         -82.04p Rser=1f
37 Rg1_one Mc1_one Mg1_one        1371.77u
38 Rt1_one Mc1_one Mt1_one         183.06u
39 Rb1_one Mb1_one Mc1_one         183.06u
40 Lt1_one T1_one Mt1_one         249.18p Rser=1f
41 Lb1_one Mb1_one B1_one         249.18p Rser=1f
42 Ls1_one B1_one T2_one           7.20n  Rser=1f
43 K1_one Le1_one Li1_one 1
44
45 *NetList for Layer 2
46 Le2_one N2_one P2_one 4 Rser=1f
47 Li2_one G_one Md2_one 1 Rser=1f
48 Lg2_one Mg2_one Md2_one         -82.04p Rser=1f
49 Rg2_one Mc2_one Mg2_one        1371.77u
50 Rt2_one Mc2_one Mt2_one         183.06u
```

```
51 Rb2_one Mb2_one Mc2_one          183.06u
52 Lt2_one T2_one Mt2_one          249.18p Rser=1f
53 Lb2_one Mb2_one B2_one          249.18p Rser=1f
54 Ls2_one B2_one T3_one            0.86n  Rser=1f
55 K2_one Le2_one Li2_one 1
56
57 *NetList for Layer 3
58 Le3_one N3_one P3_one 4 Rser=1f
59 Li3_one G_one Md3_one 1 Rser=1f
60 Lg3_one Mg3_one Md3_one          -82.04p Rser=1f
61 Rg3_one Mc3_one Mg3_one         1371.77u
62 Rt3_one Mc3_one Mt3_one          183.06u
63 Rb3_one Mb3_one Mc3_one          183.06u
64 Lt3_one T3_one Mt3_one          249.18p Rser=1f
65 Lb3_one Mb3_one B3_one          249.18p Rser=1f
66 Ls3_one B3_one T4_one            0.72n  Rser=1f
67 K3_one Le3_one Li3_one 1
68
69 *NetList for Top and Bottom Ferrites, as well as the First Spacing on Top ...
       Side
70 Lft_one T0_one G_one         8293.80n Rser=1f
71 Lfb_one T4_one G_one         8293.80n Rser=1f
72 Ls0_one T1_one T0_one            1.44n Rser=1f
73
74 *NetList for Winding Interconnects
75 *A few 1f ohm resistors are used as short interconnects
76
77 * -> Winding 1 is Series Connected
78 * -->Include layer 1
79 RexP1_one PortP1_one P1_one    1f
80 RexN1_one PortN1_one N1_one    1f
81
82 * -> Winding 2 is Parallel Connected
83 * -->Include layer 2
84 RexP2_one PortP2_one P2_one    1f
85 RexN2_one PortN2_one N2_one    1f
86 * -->Include layer 3
87 RexP3_one PortP2_one P3_one    1f
88 RexN3_one PortN2_one N3_one    1f
```

```
89
90 *One 1G ohm resistor is used to ground the floating domain
91 Rgnd_one G_one 0  1G
92 **********************************************************************
93 *****                    Netlist Ends                          ********
94 **********************************************************************
```

D.2 Python Codes for *M2Spice*

```
1  from Tkinter import *
2  from Tkinter import Tk, Frame, BOTH
3  import tkFileDialog
4  import tkMessageBox
5  import math
6  import cmath
7  import numpy
8  import time
9  import Tkinter as tk
10 import ttk
11 import getpass
12 from ast import literal_eval
13 import sys,os
14 import ScrolledText as tkst
15 import tkFont
16
17 class GUI(Frame):
18   def __init__(self,root):
19     self.root=root
20     Frame.__init__(self,self.root, background="white")
21     self.root.title('M2Spice - Planar Magnetics to SPICE Netlist ...
           Conversion Tool')
22     self.file_opt=options={}
23     options['defaultextension']='.txt'
24     options['filetypes']=[('all files','.*'),('text files','.txt')]
25     #options['initialdir']='C:\\'
26     options['initialfile']='file.txt'
27     options['parent']=self.root
```

```
28      self.dir_opt=options={}
29      #options['initialdir']='C:\\'
30      options['mustexist']=False
31      options['parent']=self.root
32      #initialize variables for GUI input
33      self.f=StringVar()          #switching frequency
34      self.mur=StringVar()        #relative permeability
35      self.nlayer=StringVar()     #number of layers
36      self.h=StringVar()          #layer thickness
37      self.sigmac=StringVar()     #layer conductivity
38      self.s=StringVar()          #spacing thickness
39      self.mus=StringVar()        #spacing permeabilities
40      self.w=StringVar()          #window width
41      self.m=StringVar()          #turns per layer
42      self.nwinding=StringVar()   #number of windings
43      self.wstyle=StringVar()     #connection style of each winding
44      self.lindex=StringVar()     #layer indices
45      self.gt=StringVar()         #core gap length on the top side
46      self.gb=StringVar()         #core gap length on the bottom side
47      self.Ac=StringVar()         #effective gap area
48      self.d=StringVar()          #effective length
49      self.c=StringVar()          #thickness of top and bottom ferrite
50      self.x=StringVar()          #define the subcircuit name x
51      #create variables for entry objects
52      self.fentry=None
53      self.murentry=None
54      self.nlayerentry=None
55      self.hentry=None
56      self.sigmacentry=None
57      self.sentry=None
58      self.musentry=None
59      self.wentry=None
60      self.mentry=None
61      self.nwindingentry=None
62      self.wstyleentry=None
63      self.lindexentry=None
64      self.gtentry=None
65      self.gbentry=None
66      self.Acentry=None
```

```
67      self.dentry=None
68      self.centry=None
69      self.xentry=None
70      #create error messages
71      self.errorMsg=StringVar()
72      #call functions to display interface
73      self.createbuttons()
74      self.printlabels()
75      self.createentries()
76      #create dictionary of input values
77      self.entries={}
78      self.entries['f']=self.fentry
79      self.entries['mur']=self.murentry
80      self.entries['nlayer']=self.nlayerentry
81      self.entries['h']=self.hentry
82      self.entries['sigmac']=self.sigmacentry
83      self.entries['s']=self.sentry
84      self.entries['mus']=self.musentry
85      self.entries['w']=self.wentry
86      self.entries['m']=self.mentry
87      self.entries['nwinding']=self.nwindingentry
88      self.entries['wstyle']=self.wstyleentry
89      self.entries['lindex']=self.lindexentry
90      self.entries['gt']=self.gtentry
91      self.entries['gb']=self.gbentry
92      self.entries['Ac']=self.Acentry
93      self.entries['d']=self.dentry
94      self.entries['c']=self.centry
95      self.entries['x']=self.xentry
96      self.geofilename='geometry.txt'
97      self.netlistfilename='netlist.txt'
98      #variables for getImpe function
99      self.Ra=None
100     self.La=None
101     self.Rb=None
102     self.Lb=None
103     self.Ls=None
104     self.Lfb=None
105     self.Lft=None
```

```
106      #call functions to display interface
107      self.createbuttons()
108      self.printlabels()
109      self.centerWindow()
110      # always center the window in the middle of the screen
111    def centerWindow(self):
112      sw = self.root.winfo_screenwidth()
113      sh = self.root.winfo_screenheight()
114      w = int(sw*0.75)
115      h = int(sh*0.6)
116      x = (sw - w)/2
117      y = (sh - h)/2
118      self.root.geometry('%dx%d+%d+%d' % (w, h, x, y))
119    def OnFrameConfigure(self, event):
120      '''Reset the scroll region to encompass the inner frame'''
121      self.canvas.configure(scrollregion=self.canvas.bbox("all"))
122    def designref(self):
123      img = tk.Toplevel(self)
124      img.title("M2Spice - Design Reference")
125      def resource_path(relative_path):
126          """ Get absolute path to resource, works for dev and for ...
                PyInstaller """
127          try:
128          # PyInstaller creates a temp folder and stores path in _MEIPASS
129              base_path = sys._MEIPASS
130          except Exception:
131              base_path = os.path.abspath(".")
132          return os.path.join(base_path, relative_path)
133      path1 = resource_path("multiwinding.gif")
134      img.image1 = PhotoImage(file = path1)
135      img.display = Label(img, image = img.image1, bg='white')
136      img.display.grid(row=0,column=0, ...
137  columnspan=6,rowspan=12,sticky=W+E+N+S)
138      sw = self.root.winfo_screenwidth()
139      sh = self.root.winfo_screenheight()
140      w = int(sw*0.38)
141      h = int(sh*0.6)
142      x = sw-w
143      y = 0
```

```
144       img.geometry('%dx%d+%d+%d' % (w, h, x, y))
145       # ask for open geometry file name
146     def askopengeofilename(self):
147       self.geofilename=tkFileDialog.askopenfilename(**self.file_opt)
148       # ask for save geometry file name
149     def asksaveasgeofilename(self):
150       self.geofilename=tkFileDialog.asksaveasfilename(**self.file_opt)
151       # ask for save netlist file name
152     def asksaveasnetlistfilename(self):
153       self.netlistfilename=tkFileDialog.asksaveasfilename(**self.file_opt)
154     def askopennetlistfilename(self):
155       self.netlistfilename=tkFileDialog.askopenfilename(**self.file_opt)
156     def savegeom(self):
157       try:
158         self.asksaveasgeofilename()
159         if self.geofilename:
160           f=open(self.geofilename,'w')
161           for key in self.entries.keys():
162             f.write(key + ' = ' + self.entries[key].get() + '\n')
163           f.close()
164           tkMessageBox.showinfo('M2Spice - Save Geometry - Saved', ...
                 message='Successfully saved geometry to:\n\n' + self.geofilename)
165       except Exception as e:
166         tkMessageBox.showerror('M2Spice - Save Geometry - Failed', ...
167  message='Failed to save geometry.\n\nSystem reported the following ...
         errors:,...
168    \n\n' +e.message + '\n\nPossible reasons: 1. invalid saving address; ,...
169  2. invalid geometry format.' + '\n\nPlease check the saving address and ...
         geometry format.')
170     def resetgeom(self):
171       cleartag = tkMessageBox.askyesno('M2Spice - Clear Geometry', ...
172  message='Do you really want to clear the geometry information? All ...
         unsaved data will be lost.')
173       if cleartag==True:
174           for key in self.entries.keys():
175               self.entries[key].delete(0,END)
176     def loadgeom(self):
177       loadvar=""
178       try:
```

```
179         self.askopengeofilename()
180         if self.geofilename:
181           for key in self.entries.keys(): #clear up
182               self.entries[key].delete(0,END)
183           f=open(self.geofilename,'r')
184           for line in f:
185               line_cell=line.split()
186               if (len(line_cell)≥3):
187                   self.entries[line.split()[0]].insert(0,line.split(None,2)[2])
188                   loadvar = loadvar + line.split()[0] + ', '
189           f.close()
190           if (len(loadvar.split())==18):
191               tkMessageBox.showinfo('M2Spice – Load Geometry – Loaded', ...
                      message='Successfully loaded all parameters. Please ...
                      double check the geometry format in the GUI, then click ...
                      "Check Geometry").')
192           else:
193               tkMessageBox.showinfo('M2Spice – Load Geometry – Partially ...
                      Loaded', message='Some parameters are missing. Please ...
                      double check the geometry format.')
194       except Exception as e:
195         tkMessageBox.showerror('M2Spice – Load Geometry – Failed', ...
196  message='Failed to load geometry.\n\nSystem reported the following ...
       errors: \n\n' +e.message + '\n\nPossible reasons: 1. invalid loading ...
       address; 2.invalid geometry format.' + '\n\nPlease check the loading ...
       address and geometry format.')
197     def editgeom(self):
198       geoinfo=""
199       for key in self.entries.keys():
200           geoinfo = geoinfo + key + ' = ' + self.entries[key].get() + '\n'
201       editor = tk.Toplevel(self, bg='white', width=550,height=500)
202       editor.title("M2Spice – Geometry Editor")
203       #overall frame position
204       editorarea = tk.Frame(editor ...
            ,height=100,width=50,bg='white',borderwidth=1)
205       editorscrollbar=tk.Scrollbar(editorarea)
206       #size of the scrollbar
207       editArea=tk.Text(editorarea, width=70, height=30, wrap="word", ...
            yscrollcommand=editorscrollbar.set)
```

```
208     editorscrollbar.config(command=editArea.yview)
209     editorscrollbar.pack(side="right",fill="y")
210     editArea.pack(side="left",fill="both",expand=True)
211     #position of the editorial area
212     editorarea.place(x=20,y=40)
213     sw = editor.winfo_screenwidth()
214     sh = editor.winfo_screenheight()
215     w = int(sw*0.4)
216     h = int(sh*0.6)
217     x = 0
218     y = 0
219     editor.geometry('%dx%d+%d+%d' % (w, h, x, y))
220     #Write in the current geometry information
221     editArea.insert(tk.INSERT,geoinfo)
222     def askopengeofilename():
223         self.geofilename=tkFileDialog.askopenfilename(**self.file_opt)
224     # ask for save geometry file name
225     def asksaveasgeofilename():
226         self.geofilename=tkFileDialog.asksaveasfilename(**self.file_opt)
227     def reseteditgeom():
228         cleartag = tkMessageBox.askyesno('M2Spice - Clear Geometry', ...
229 message='Do you really want to clear the geometry information? All ...
      unsaved data will be lost.')
230         editor.lift()
231         if cleartag==True:
232             editArea.delete(1.0, END)
233     def loadeditgeom():
234         try:
235             askopengeofilename()
236             if self.geofilename:
237                 editArea.delete(1.0, END) #clear up
238                 f=open(self.geofilename,'r')
239                 netlist=f.read()
240                 editArea.insert(tk.INSERT,netlist)
241                 f.close()
242                 editor.lift()
243         except Exception as e:
244                 tkMessageBox.showerror('M2Spice - Load Geometry - ...
                    Failed', ...
```

```
245 message='Failed to load geometry.\n\nSystem reported the following ...
        errors:,...
246  \n\n' +e.message + '\n\nPossible reasons: 1. invalid loading address; ...
247 2.invalid geometry format.' + '\n\nPlease check the loading address and ...
        geometry format.')
248     def saveeditgeom():
249         geoinfo=""
250         try:
251             asksaveasgeofilename()
252             if self.geofilename:
253                 geoinfo = editArea.get(1.0,'end-1c')
254                 geoinfo = os.linesep.join([s for s in ...
                        geoinfo.splitlines() if s])
255                 f=open(self.geofilename,'w')
256                 f.write(geoinfo)
257                 f.close()
258                 tkMessageBox.showinfo('M2Spice - Save Geometry - Saved', ...
259 message='Successfully saved geometry to:\n\n' + self.geofilename)
260                 editor.lift()
261         except Exception as e:
262             tkMessageBox.showerror('M2Spice - Save Geometry - Failed', ...
263 message='Failed to save geometry.\n\nSystem reported the following ...
        errors: \n\n' +e.message + '\n\nPossible reasons:...
264  1. invalid saving address; 2. invalid geometry format.' + '\n\nPlease ...
         check the saving address and geometry format.')
265     def forwardeditgeom():
266         geoinfo=""
267         fwdvar="" #forwarded variable
268         try:
269             for key in self.entries.keys():
270                 self.entries[key].delete(0,END) #clear up
271             geoinfo = editArea.get(1.0,'end-1c')
272             geoinfo = os.linesep.join([s for s in geoinfo.splitlines() if s])
273             for line in geoinfo.splitlines():
274                 line_cell=line.split()
275                 if (len(line_cell)>=3):
276                     self.entries[line.split()[0]].insert(0,...
277 line.split(None,2)[2])
278                     fwdvar = fwdvar + line.split()[0] + ', '
```

```
279             if (len(fwdvar.split())==17):
280                 tkMessageBox.showinfo('M2Spice - Forward Geometry - ...
                        Forwarded',...
281  message='Successfully forwarded all parameters to the GUI. ...
282 Please double check the geometry format in the GUI, then click "Check ...
       Geometry".')
283                 editor.lower()
284             else:
285                 tkMessageBox.showinfo('M2Spice - Forward Geometry - ...
                        Partially Forwarded',...
286  message='Some parameters are missing. Please double check the geometry ...
        format.')
287         except Exception as e:
288             tkMessageBox.showerror('M2Spice - Forward Geometry - Failed', ...
289 message='Failed to forward geometry.\n\nSystem reported the following ...
       errors: \n\n'...
290  +e.message + '\n\nPossible reasons: 1. invalid loading address; ...
        2.invalid geometry format.'...
291  + '\n\nPlease check the loading address and geometry format.')
292     custom = tkFont.Font(family="Helvetica",size=12,weight="bold")
293     buttonframe=Frame(editor, bg='white', height=3)
294     Button(buttonframe, text='Load Geometry', ...
            command=loadeditgeom).pack(side=LEFT,padx=5,pady=5)
295     Button(buttonframe, text='Save Geometry', ...
            command=saveeditgeom).pack(side=LEFT,padx=5,pady=5)
296     Button(buttonframe, text='Clear Geometry', ...
            command=reseteditgeom).pack(side=LEFT,padx=5,pady=5)
297     Button(buttonframe, text='Forward Geometry', ...
            command=forwardeditgeom).pack(side=LEFT,padx=5,pady=5)
298     buttonframe.grid(row=0, columnspan=1)
299   def viewnetlist(self):
300     try:
301       self.askopennetlistfilename()
302       if self.netlistfilename:
303         f=open(self.netlistfilename,'r')
304         netlist=f.read()
305         viewer = tk.Toplevel(self, bg='white', width=700,height=500)
306         viewer.title("M2Spice - Netlist Viewer")
```

```
307         viewarea = ...
                tk.Frame(viewer,height=100,width=50,bg='white',borderwidth=1)
308         viewscrollbar=tk.Scrollbar(viewarea)
309         editArea=tk.Text(viewarea,width=100,height=30,wrap="word",...
310 yscrollcommand=viewscrollbar.set,borderwidth=0,highlightthickness=0)
311         viewscrollbar.config(command=editArea.yview)
312         viewscrollbar.pack(side="right",fill="y")
313         editArea.pack(side="left",fill="both",expand=True)
314         editArea.insert(tk.INSERT,netlist)
315         viewarea.place(x=20,y=20)
316         sw = viewer.winfo_screenwidth()
317         sh = viewer.winfo_screenheight()
318         w = int(sw*0.6)
319         h = int(sh*0.6)
320         x = w/2
321         y = h/2
322         viewer.geometry('%dx%d+%d+%d' % (w, h, x, y))
323     except Exception as e:
324       tkMessageBox.showerror('M2Spice - Netlist Viewer - Failed', message=...
325 'Failed to open netlist.\n\nSystem reported the following errors: \n\n' ...
        +e.message...
326  + '\n\nPossible reasons: 1. invalid netlist address; 2.invalid netlist ...
         file.' + '\n\nPlease check the netlist address and netlist file.')
327   def checkgeom(self):
328     self.errorMsg=''
329     self.errorNum=0
330     self.errorCheck()
331     # error format and value check
332   def errorCheck(self):
333     try:
334       len(literal_eval(self.h.get()))
335     except Exception:
336       self.errorMsg=self.errorMsg+'\n -- invalid winding thickness (h), ...
              please enter a list of float values (please include "[" and "]").'
337       self.errorNum=self.errorNum+1
338     try:
339       len(literal_eval(self.w.get()))
340     except Exception:
```

```
341         self.errorMsg=self.errorMsg+'\n -- invalid winding width (w), ...
                please enter a list of float values (please include "[" and "]").'
342         self.errorNum=self.errorNum+1
343       try:
344         len(literal_eval(self.s.get()))
345       except Exception:
346         self.errorMsg=self.errorMsg+'\n -- invalid winding spacing (s), ...
                please enter a list of float values (please include "[" and "]").'
347         self.errorNum=self.errorNum+1
348       try:
349         len(literal_eval(self.mus.get()))
350       except Exception:
351         self.errorMsg=self.errorMsg+'\n -- invalid spacing permeability ...
                (mus), please enter a list of float values (please include "[" ...
                and "]").'
352         self.errorNum=self.errorNum+1
353       try:
354         len(literal_eval(self.m.get()))
355       except Exception:
356         self.errorMsg=self.errorMsg+'\n -- invalid number of turns on each ...
                layer (m), please enter a list of integer values (please ...
                include "[" and "]").'
357         self.errorNum=self.errorNum+1
358       try:
359         len(literal_eval(self.wstyle.get()))
360       except Exception:
361         self.errorMsg=self.errorMsg+'\n -- invalid winding style (wstyle), ...
                please enter a list of integers (please include "[" and "]").'
362         self.errorNum=self.errorNum+1
363       try:
364         len(literal_eval(self.lindex.get()))
365       except Exception:
366         self.errorMsg=self.errorMsg+'\n -- invalid layer belongings ...
                (lindex), please enter a list of integers (please include "[" ...
                and "]").'
367         self.errorNum=self.errorNum+1
368       try:
369         len(literal_eval(self.sigmac.get()))
370       except Exception:
```

```
371       self.errorMsg=self.errorMsg+'\n -- invalid layer conductivity ...
              (sigmac), please enter a list of float values (please include ...
              "[" and "]").'
372       self.errorNum=self.errorNum+1
373     try:
374       float(self.mur.get())
375     except Exception:
376       self.errorMsg=self.errorMsg+'\n -- invalid relative permeability ...
              (mur), please enter a float value (no "[" or "]").'
377       self.errorNum=self.errorNum+1
378     try:
379       int(self.nlayer.get())
380     except Exception:
381       self.errorMsg=self.errorMsg+'\n -- invalid total number of layers ...
              (nlayer), please enter an integer (no "[" or "]").'
382       self.errorNum=self.errorNum+1
383     try:
384       int(self.nwinding.get())
385     except Exception:
386       self.errorMsg=self.errorMsg+'\n -- invalid total number of windings ...
              (nwinding), please enter an integer (no "[" or "]").'
387       self.errorNum=self.errorNum+1
388     try:
389       float(self.gt.get())
390     except Exception:
391       self.errorMsg=self.errorMsg+'\n -- invalid top gap length (gt), ...
              please enter a float value (no "[" or "]").'
392       self.errorNum=self.errorNum+1
393     try:
394       float(self.gb.get())
395     except Exception:
396       self.errorMsg=self.errorMsg+'\n -- invalid bottom gap length (gb), ...
              please enter a float value (no "[" or "]").'
397       self.errorNum=self.errorNum+1
398     try:
399       float(self.Ac.get())
400     except Exception:
401       self.errorMsg=self.errorMsg+'\n -- invalid effective core gap area ...
              (Ac), please enter a float value (no "[" or "]").'
```

```
402         self.errorNum=self.errorNum+1
403       try:
404         float(self.d.get())
405       except Exception:
406         self.errorMsg=self.errorMsg+'\n -- invalid effective core length ...
              (d), please enter a float value (no "[" or "]").'
407         self.errorNum=self.errorNum+1
408       try:
409         float(self.c.get())
410       except Exception:
411         self.errorMsg=self.errorMsg+'\n -- invalid top and bottom core ...
              thickness (c), please enter an integer (no "[" or "]").'
412         self.errorNum=self.errorNum+1
413           # finished format check, start value check
414       if self.errorMsg.strip()=='':
415         nwinding=int(self.nwinding.get())
416         nlayer=int(self.nlayer.get())
417         if nwinding!= max(literal_eval(self.lindex.get())):
418           self.errorMsg=self.errorMsg+'\n -- _nwinding_ mismatch with ...
                _lindex_, please check if list.length(lindex) equals ...
                _nwinding_ ?'
419           self.errorNum=self.errorNum+1
420         if nwinding!= len(literal_eval(self.wstyle.get())):
421           self.errorMsg=self.errorMsg+'\n -- _nwinding_ mismatch with ...
                _wstyle_, please check if list.length(wstyle) equals ...
                _nwinding_ ?'
422           self.errorNum=self.errorNum+1
423         if nlayer!=len(literal_eval(self.h.get())):
424           self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with _h_, ...
                please check if list.length(h) equals _nlayer_ ?'
425           self.errorNum=self.errorNum+1
426         if nlayer!=len(literal_eval(self.sigmac.get())):
427           self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with ...
                _sigmac_, please check if list.length(sigmac) equals _nlayer_ ?'
428           self.errorNum=self.errorNum+1
429         if nlayer!=(len(literal_eval(self.s.get()))-1):
430           self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with _s_, ...
                please check if list.length(s) equals _nlayer+1_ ? There is ...
                always one more spacing than the number of conductive layers.'
```

```
431         self.errorNum=self.errorNum+1
432       if nlayer!=(len(literal_eval(self.mus.get()))-1):
433         self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with _mus_, ...
                please check if list.length(mus) equals _nlayer+1_ ? There is ...
                always one more spacing than the number of conductive layers.'
434         self.errorNum=self.errorNum+1
435       if nlayer!=len(literal_eval(self.w.get())):
436         self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with _w_, ...
                please check if list.length(w) equals _nlayer_ ?'
437         self.errorNum=self.errorNum+1
438       if nlayer!=len(literal_eval(self.lindex.get())):
439         self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with ...
                _lindex_, please check if list.length(lindex) equals _nlayer_ ?'
440         self.errorNum=self.errorNum+1
441       if nlayer!=len(literal_eval(self.m.get())):
442         self.errorMsg=self.errorMsg+'\n -- _nlayer_ mismatch with _m_, ...
                please check if list.length(m) equals _nlayer_ ?'
443         self.errorNum=self.errorNum+1
444       if self.errorMsg.strip()=='':
445         tkMessageBox.showinfo('M2Spice - Check Geometry - Passed', ...
                message='Good! Geometry is correct! \n\nNow you can generate ...
                the netlist by clicking "Generate Netlist".')
446         self.errorNum=self.errorNum+1
447       else:
448         tkMessageBox.showerror('M2Spice - Check Geometry - Failed', ...
                message='Find ' + str(self.errorNum) +' geometry errors:\n' + ...
                self.errorMsg)
449     else:
450       tkMessageBox.showerror('M2Spice - Check Geometry - Failed', ...
              message='Find ' + str(self.errorNum) + ' geometry errors:\n'+ ...
              self.errorMsg)
451   def printlabels(self):
452     Label(self,text='Analysis Frequency ...
            (f)',bg='white').grid(column=0,row=1,sticky=W)
453     Label(self,text='Relative Permeability of the Core ...
            (mur)',bg='white').grid(column=0,row=2,sticky=W)
454     Label(self,text='Total Number of Layers ...
            (nlayer)',bg='white').grid(column=0,row=3,sticky=W)
```

```
455     Label(self,text='Layer Thickness ...
            (h)',bg='white').grid(column=0,row=4,sticky=W)
456     Label(self,text='Layer Conductivities ...
            (sigmac)',bg='white').grid(column=0,row=5,sticky=W)
457     Label(self,text='Spacing Thickness ...
            (s)',bg='white').grid(column=0,row=6,sticky=W)
458     Label(self,text='Spacing Permeabilities ...
            (mus)',bg='white').grid(column=0,row=7,sticky=W)
459     Label(self,text='Core Window Width ...
            (w)',bg='white').grid(column=0,row=8,sticky=W)
460     Label(self,text='Number of Turns on Each Layer ...
            (m)',bg='white').grid(column=0,row=9,sticky=W)
461     Label(self,text='Number of Windings ...
            (nwinding)',bg='white').grid(column=0,row=10,sticky=W)
462     Label(self,text='Connection Style of Each Winding ...
            (wstyle)',bg='white').grid(column=0,row=11,sticky=W)
463     Label(self,text='Belongings of Each Layer to Windings ...
            (lindex)',bg='white').grid(column=0,row=12,sticky=W)
464     Label(self,text='Core Gap Length on the Top Side ...
            (gt)',bg='white').grid(column=0,row=13,sticky=W)
465     Label(self,text='Core Gap Length on the Bottom Side ...
            (gb)',bg='white').grid(column=0,row=14,sticky=W)
466     Label(self,text='Effective Core Area ...
            (Ac)',bg='white').grid(column=0,row=15,sticky=W)
467     Label(self,text='Effective Winding Length per Turn ...
            (d)',bg='white').grid(column=0,row=16,sticky=W)
468     Label(self,text='Thickness of the Top and Bottom Core ...
            (c)',bg='white').grid(column=0,row=17,sticky=W)
469     Label(self,text='Name of the Component ...
            (x)',bg='white').grid(column=0,row=18,sticky=W)
470     Label(self,text='*'*20,bg='white').grid(column=0,row=19,columnspan=6)
471     Label(self,text='S.A. Pavlick, M. Chen, and D.J. ...
            Perreault',bg='white').grid(column=0,row=20,columnspan=6)
472     Label(self,text='MIT Power Electronics Research ...
            Group',bg='white').grid(column=0,row=21,columnspan=6)
473     Label(self,text='v1.0, Feb ...
            2015',bg='white').grid(column=0,row=22,columnspan=6)
474     Label(self,text='*'*20,bg='white').grid(column=0,row=23,columnspan=6)
475     Label(self,text='Unit: Hz',bg='white').grid(column=4,row=1,sticky=W)
```

```
476     Label(self,text='Unit: 1',bg='white').grid(column=4,row=2,sticky=W)
477     Label(self,text='Unit: 1',bg='white').grid(column=4,row=3,sticky=W)
478     Label(self,text='Unit: meters',bg='white').grid(column=4,row=4,sticky=W)
479     Label(self,text='Unit: S/m',bg='white').grid(column=4,row=5,sticky=W)
480     Label(self,text='Unit: meters',bg='white').grid(column=4,row=6,sticky=W)
481     Label(self,text='Unit: H/m',bg='white').grid(column=4,row=7,sticky=W)
482     Label(self,text='Unit: meters',bg='white').grid(column=4,row=8,sticky=W)
483     Label(self,text='Unit: 1',bg='white').grid(column=4,row=9,sticky=W)
484     Label(self,text='Unit: 1',bg='white').grid(column=4,row=10,sticky=W)
485     Label(self,text='0=series, ...
            1=parallel',bg='white').grid(column=4,row=11,sticky=W)
486     Label(self,text='Winding ...
            index',bg='white').grid(column=4,row=12,sticky=W)
487     Label(self,text='Unit: meters',bg='white').grid(column=4,row=13,sticky=W)
488     Label(self,text='Unit: meters',bg='white').grid(column=4,row=14,sticky=W)
489     Label(self,text='Unit: ...
            meter^2',bg='white').grid(column=4,row=15,sticky=W)
490     Label(self,text='Unit: meters',bg='white').grid(column=4,row=16,sticky=W)
491     Label(self,text='Unit: meters',bg='white').grid(column=4,row=17,sticky=W)
492     Label(self,text='blank, or one ...
            letter',bg='white').grid(column=4,row=18,sticky=W)
493     Label(self,text='e.g.: 1e6',bg='white').grid(column=5,row=1,sticky=W)
494     Label(self,text='e.g.: 1000',bg='white').grid(column=5,row=2,sticky=W)
495     Label(self,text='e.g.: 4',bg='white').grid(column=5,row=3,sticky=W)
496     Label(self,text='e.g.: [1e-3, 1e-3, 1e-3, ...
            1e-3]',bg='white').grid(column=5,row=4,sticky=W)
497     Label(self,text='e.g.: [6e7, 6e7, 6e7, ...
            6e7]',bg='white').grid(column=5,row=5,sticky=W)
498     Label(self,text='e.g.: [1e-3, 1e-3, 1e-3, 1e-3, ...
            1e-3]',bg='white').grid(column=5,row=6,sticky=W)
499     Label(self,text='e.g.: [1e-6, 1e-6, 1e-6, 1e-6, ...
            1e-6]',bg='white').grid(column=5,row=7,sticky=W)
500     Label(self,text='e.g.: [5e-3, 5e-3, 5e-3, ...
            5e-3]',bg='white').grid(column=5,row=8,sticky=W)
501     Label(self,text='e.g.: [1, 1, 2, ...
            1]',bg='white').grid(column=5,row=9,sticky=W)
502     Label(self,text='e.g.: 2',bg='white').grid(column=5,row=10,sticky=W)
503     Label(self,text='e.g.: [0, 1]',bg='white').grid(column=5,row=11,sticky=W)
```

```
504     Label(self,text='e.g.: [1, 2, 1, ...
            2]',bg='white').grid(column=5,row=12,sticky=W)
505     Label(self,text='e.g.: 1e-3',bg='white').grid(column=5,row=13,sticky=W)
506     Label(self,text='e.g.: 1e-3',bg='white').grid(column=5,row=14,sticky=W)
507     Label(self,text='e.g.: 60e-6',bg='white').grid(column=5,row=15,sticky=W)
508     Label(self,text='e.g.: 2e-2',bg='white').grid(column=5,row=16,sticky=W)
509     Label(self,text='e.g.: 1e-3',bg='white').grid(column=5,row=17,sticky=W)
510     Label(self,text='e.g.: ...
            componentname',bg='white').grid(column=5,row=18,sticky=W)
511   def createentries(self):
512     #defining the entries
513     self.fentry=Entry(self,textvariable=self.f,bg='yellow',width=50)
514     self.murentry=Entry(self,textvariable=self.mur,bg='yellow')
515     self.nlayerentry=Entry(self,textvariable=self.nlayer,bg='yellow')
516     self.hentry=Entry(self,textvariable=self.h,bg='yellow')
517     self.sigmacentry=Entry(self,textvariable=self.sigmac,bg='yellow')
518     self.sentry=Entry(self,textvariable=self.s,bg='yellow')
519     self.musentry=Entry(self,textvariable=self.mus,bg='yellow')
520     self.wentry=Entry(self,textvariable=self.w,bg='yellow')
521     self.mentry=Entry(self,textvariable=self.m,bg='yellow')
522     self.nwindingentry=Entry(self,textvariable=self.nwinding,bg='yellow')
523     self.wstyleentry=Entry(self,textvariable=self.wstyle,bg='yellow')
524     self.lindexentry=Entry(self,textvariable=self.lindex,bg='yellow')
525     self.gtentry=Entry(self,textvariable=self.gt,bg='yellow')
526     self.gbentry=Entry(self,textvariable=self.gb,bg='yellow')
527     self.Acentry=Entry(self,textvariable=self.Ac,bg='yellow')
528     self.dentry=Entry(self,textvariable=self.d,bg='yellow')
529     self.centry=Entry(self,textvariable=self.c,bg='yellow')
530     self.xentry=Entry(self,textvariable=self.x,bg='yellow')
531     #positioning the entries
532     self.fentry.grid(column=1,row=1,sticky=(W,E),columnspan=2)
533     self.murentry.grid(column=1,row=2,sticky=(W,E),columnspan=2)
534     self.nlayerentry.grid(column=1,row=3,sticky=(W,E),columnspan=2)
535     self.hentry.grid(column=1,row=4,sticky=(W,E),columnspan=2)
536     self.sigmacentry.grid(column=1,row=5,sticky=(W,E),columnspan=2)
537     self.sentry.grid(column=1,row=6,sticky=(W,E),columnspan=2)
538     self.musentry.grid(column=1,row=7,sticky=(W,E),columnspan=2)
539     self.wentry.grid(column=1,row=8,sticky=(W,E),columnspan=2)
540     self.mentry.grid(column=1,row=9,sticky=(W,E),columnspan=2)
```

```
541      self.nwindingentry.grid(column=1,row=10,sticky=(W,E),columnspan=2)
542      self.wstyleentry.grid(column=1,row=11,sticky=(W,E),columnspan=2)
543      self.lindexentry.grid(column=1,row=12,sticky=(W,E),columnspan=2)
544      self.gtentry.grid(column=1,row=13,sticky=(W,E),columnspan=2)
545      self.gbentry.grid(column=1,row=14,sticky=(W,E),columnspan=2)
546      self.Acentry.grid(column=1,row=15,sticky=(W,E),columnspan=2)
547      self.dentry.grid(column=1,row=16,sticky=(W,E),columnspan=2)
548      self.centry.grid(column=1,row=17,sticky=(W,E),columnspan=2)
549      self.xentry.grid(column=1,row=18,sticky=(W,E),columnspan=2)
550    def createbuttons(self):
551      buttonframe=Frame(self, bg='white', height=3)
552      Button(buttonframe, text='Load Geometry', ...
             command=self.loadgeom).pack(side=LEFT,padx=5,pady=5)
553      Button(buttonframe, text='Save Geometry', ...
             command=self.savegeom).pack(side=LEFT,padx=5,pady=5)
554      Button(buttonframe, text='Clear Geometry', ...
             command=self.resetgeom).pack(side=LEFT,padx=5,pady=5)
555      Button(buttonframe, text='Geometry Editor', ...
             command=self.editgeom).pack(side=LEFT,padx=5,pady=5)
556      Button(buttonframe, text='Check Geometry', ...
             command=self.checkgeom).pack(side=LEFT,padx=5,pady=5)
557      Button(buttonframe, text='Generate ...
             Netlist',command=self.try_generate_netlist).,...
558  pack(side=LEFT,padx=5,pady=5)
559      Button(buttonframe, text='Design ...
             Guide',command=self.designref).pack(side=LEFT,padx=5,pady=5)
560      Button(buttonframe, text='Netlist ...
             Viewer',command=self.viewnetlist).pack(side=LEFT,padx=5,pady=5)
561      buttonframe.grid(row=0, columnspan=7)
562    def getImpe(self):
563      d=float(self.d.get())
564      h=literal_eval(self.h.get())
565      NumofLayer=int(self.nlayer.get())
566      sigmac=literal_eval(self.sigmac.get())
567      mur=float(self.mur.get())
568      s=literal_eval(self.s.get())
569      mus=literal_eval(self.mus.get())
570      w=literal_eval(self.w.get())
571      gt=float(self.gt.get())
```

```
572      gb=float(self.gb.get())
573      f=float(self.f.get())
574      c=float(self.c.get())
575      Ac=float(self.Ac.get())
576      Xa=[]
577      Xb=[]
578      Xs=[]
579      for i1 in range(NumofLayer):
580        Δ=(2/(f*2*math.pi)/mus[i1]/sigmac[i1])**0.5
581        Psi=complex(1/Δ,1/Δ)
582        Z=Psi/sigmac[i1]
583        A=cmath.exp(-Psi*h[i1])
584        Za=Z*(1-A)/(1+A)
585        Zb=Z*2*A/(1-A**2)
586        Xa.append(d/w[i1]*Za)
587        Xb.append(d/w[i1]*Zb)
588        Xs.append(complex(0,1)*(f*2*math.pi)*mus[i1+1]*s[i1+1]*d/w[i1])
589      #impedance for the ferrite core
590      Xfb=complex(0,1)*(f*2*math.pi)*4*math.pi*1e-7*Ac/(gb+Ac*w[i1]/(mur*c*d))
591      Xft=complex(0,1)*(f*2*math.pi)*4*math.pi*1e-7*Ac/(gt+Ac*w[i1]/(mur*c*d))
592      Xts=complex(0,1)*(f*2*math.pi)*mus[0]*s[0]*d/w[i1]
593      #calculate output
594      self.Ra=numpy.array([e.real for e in Xa])
595      self.La=numpy.array([e.imag for e in Xa])/(f*2*math.pi)
596      self.Rb=numpy.array([e.real for e in Xb])
597      self.Lb=numpy.array([e.imag for e in Xb])/(f*2*math.pi)
598      self.Ls=numpy.array([e.imag for e in Xs])/(f*2*math.pi)
599      self.Lfb=Xfb.imag/(f*2*math.pi)
600      self.Lft=Xft.imag/(f*2*math.pi)
601      self.Lts=Xts.imag/(f*2*math.pi)
602      #start generating netlist
603    def generate_netlist(self):
604      self.asksaveasnetlistfilename()
605      if self.netlistfilename:
606          sigmac=literal_eval(self.sigmac.get())
607          mur=float(self.mur.get())
608          NumofLayer=int(self.nlayer.get())
609          NumofWinding=int(self.nwinding.get())
610          h=literal_eval(self.h.get())
```

```
611         s=literal_eval(self.s.get())
612         mus=literal_eval(self.mus.get())
613         w=literal_eval(self.w.get())
614         m=literal_eval(self.m.get())
615         WindingStyle=literal_eval(self.wstyle.get())
616         WindingIndex=literal_eval(self.lindex.get())
617         gt=float(self.gt.get())
618         gb=float(self.gb.get())
619         Ac=float(self.Ac.get())
620         d=float(self.d.get())
621         c=float(self.c.get())
622         x=self.x.get()    #x is a string value
623         x=x.replace('\n', '').replace('\r', '').replace(' ','') #get rid ...
                of all invalid string
624         if x != '':
625            x='_'+x
626         self.getImpe()
627         Serieslayers={}
628         #Repeat and summarizing the input information
629         f=open(self.netlistfilename,'w')
630         #Generate netlist identification information
631         localtime = time.asctime( time.localtime(time.time()))
632         user = getpass.getuser()
633         f.write('\n**************************************************')
634         f.write('\n*****         {0} by {1}          ...
                *****'.format(localtime,user))
635         f.write('\n**************************************************')
636         #Start describing the transformer structure
637         f.write('\n**************************************************')
638         f.write('\n******* Comprehensive  Summary of the Magnetic ...
                Structure  ********')
639         f.write('\n******* Please double check the geometry information ...
                and  ********')
640         f.write('\n**** use the external Port Name to interface with your ...
                circuit ***')
641         f.write('\n**************************************************')
642         f.write('\n\n* The name of the component is: {}. This name can ...
                only be used once in a circuit.'.format(x))
```

```
643         f.write('\n\n* This planar structure has {0} windings and {1} ...
                layers'.format(NumofWinding, NumofLayer))
644         for index_winding in range(NumofWinding):
645             #Parallel Connected
646           if WindingStyle[index_winding]==1:
647             f.write('\n\n* -> All layers in winding {0} are Parallel ...
                    Connected; \n* -> Its external Port Name: PortP{0}{1}, ...
                    PortN{0}{1}'.format(index_winding+1,x))
648             totalturn=0
649             for index_layer in range(NumofLayer):
650               if WindingIndex[index_layer]==index_winding+1:
651                 f.write('\n* --> Includes Layer {}'.format(index_layer+1))
652                 f.write('\n* ---> thickness {:4.2f}um, width {:4.2f}mm, ...
                        turns {}, spacing above {:4.2f}mm, spacing below ...
                        {:4.2f}mm'.format(h[index_layer]*1e6, ...
                        w[index_layer]*1e3, m[index_layer], ...
                        s[index_layer]*1e3, s[index_layer+1]*1e3))
653                 totalturn=totalturn+m[index_layer]
654             f.write('\n* -> Winding {0} has {1} total ...
                    turns;'.format(index_winding+1, totalturn))
655             #Series Connected
656           if WindingStyle[index_winding]==0:
657             f.write('\n\n* -> All layers in winding {0} are Series ...
                    Connected; \n* -> Its external Port Name: PortP{0}{1}, ...
                    PortN{0}{1}'.format(index_winding+1,x))
658             numSeriesLayers=1
659             totalturn=0
660             for index_layer in range(NumofLayer):
661               if WindingIndex[index_layer]==index_winding+1:
662                 f.write('\n* --> Includes Layer {}'.format(index_layer+1))
663                 f.write('\n* ---> thickness {:4.2f}um, width {:4.2f}mm, ...
                        turns {}, spacing above {:4.2f}mm, spacing below ...
                        {:4.2f}mm'.format(h[index_layer]*1e6, ...
                        w[index_layer]*1e3, m[index_layer], ...
                        s[index_layer]*1e3, s[index_layer+1]*1e3))
664                 numSeriesLayers+=1
665                 totalturn=totalturn+m[index_layer]
666             f.write('\n* -> Winding {0} has {1} total ...
                    turns;'.format(index_winding+1, totalturn))
```

```
667         f.write('\n*****************************\n')
668         f.write('\n*****************************')
669         f.write('\n*****                    Netlist Starts ...
                              ********')
670         f.write('\n*****************************')
671         #Generate the SPICE netlist
672         for index in range(NumofLayer):
673           ra=self.Ra[index]
674           la=self.La[index]
675           rb=self.Rb[index]
676           lb=self.Lb[index]
677           ls=self.Ls[index]
678           mx=m[index]
679           f.write('\n\n*NetList for Layer {}'.format(index+1))
680           f.write('\nLe{0}{2} N{0}{2} P{0}{2} {1} ...
                  Rser=1f'.format(index+1,mx**2,x))
681           f.write('\nLi{0}{2} G{2} Md{0}{2} {1} Rser=1f'.format(index+1,1,x))
682           f.write('\nLg{0}{2} Mg{0}{2} Md{0}{2} {1:14.2f}p ...
                  Rser=1f'.format(index+1,lb*1e12,x))
683           f.write('\nRg{0}{2} Mc{0}{2} Mg{0}{2} ...
                  {1:14.2f}u'.format(index+1,rb*1e6,x))
684           f.write('\nRt{0}{2} Mc{0}{2} Mt{0}{2} ...
                  {1:14.2f}u'.format(index+1,ra*1e6,x))
685           f.write('\nRb{0}{2} Mb{0}{2} Mc{0}{2} ...
                  {1:14.2f}u'.format(index+1,ra*1e6,x))
686           f.write('\nLt{0}{2} T{0}{2} Mt{0}{2} {1:14.2f}p ...
                  Rser=1f'.format(index+1,la*1e12,x))
687           f.write('\nLb{0}{2} Mb{0}{2} B{0}{2} {1:14.2f}p ...
                  Rser=1f'.format(index+1,la*1e12,x))
688           f.write('\nLs{0}{3} B{0}{3} T{1}{3} {2:14.2f}n  ...
                  Rser=1f'.format(index+1,index+2,ls*1e9,x))
689           f.write('\nK{0}{1} Le{0}{1} Li{0}{1} 1'.format(index+1,x))
690         #Print the ferrite cores and top spacing
691         f.write('\n\n*NetList for Top and Bottom Ferrites, as well as the ...
              First Spacing on Top Side')
692         f.write('\nLft{1} T0{1} G{1} {0:14.2f}n ...
              Rser=1f'.format(self.Lft*1e9,x))
693         f.write('\nLfb{2} T{0}{2} G{2} {1:14.2f}n ...
              Rser=1f'.format(NumofLayer+1,self.Lfb*1e9,x))
```

```
694         f.write('\nLs0{1} T1{1} T0{1} {0:14.2f}n ...
                Rser=1f'.format(self.Lts*1e9,x))
695         #Print the external connections
696         f.write('\n\n*NetList for Winding Interconnects')
697         f.write('\n*A few 1f ohm resistors are used as short interconnects')
698         #Create External Winding Ports
699         for index_winding in range(NumofWinding):
700           #Parallel Connected
701           if WindingStyle[index_winding]==1:
702             f.write('\n\n* -> Winding {} is Parallel ...
                  Connected'.format(index_winding+1))
703             for index_layer in range(NumofLayer):
704               if WindingIndex[index_layer]==index_winding+1:
705                 f.write('\n* -->Include layer {}'.format(index_layer+1))
706                 f.write('\nRexP{0}{2} PortP{1}{2} P{0}{2}    ...
                      1f'.format(index_layer+1,index_winding+1,x))
707                 f.write('\nRexN{0}{2} PortN{1}{2} N{0}{2}    ...
                      1f'.format(index_layer+1,index_winding+1,x))
708           #Series Connected
709           if WindingStyle[index_winding]==0:
710             f.write('\n\n* -> Winding {} is Series ...
                  Connected'.format(index_winding+1))
711             #identify which layers it contains
712             numSeriesLayers=1
713             for index_layer in range(NumofLayer):
714               if WindingIndex[index_layer]==index_winding+1:
715                 f.write('\n* -->Include layer {}'.format(index_layer+1))
716                 Serieslayers[numSeriesLayers]=index_layer+1
717                 numSeriesLayers+=1
718             #defining two wires from external port to the front and end ...
                  layers
719             f.write('\nRexP{0}{2} PortP{1}{2} P{0}{2}    ...
                  1f'.format(Serieslayers[1],index_winding+1,x))
720             f.write('\nRexN{0}{2} PortN{1}{2} N{0}{2}    ...
                  1f'.format(Serieslayers[numSeriesLayers-1],index_winding+1,x))
721             #defining the interconnects among series connected layers
722             for index_SeriesLayers in range(numSeriesLayers-2):
723               f.write('\nRexM{0}{2} N{0}{2} P{1}{2}     ...
724 1f'.format(Serieslayers[index_SeriesLayers+1],...
```

```
725 Serieslayers[index_SeriesLayers+2],x))
726         f.write('\n\n*One 1G ohm resistor is used to ground the floating ...
                domain')
727         f.write('\nRgnd{0} G{0} 0  1G\n\n'.format(x))
728         #netlist finalized
729         f.write('\n**********************************')
730         f.write('\n*****                    Netlist Ends ...
                                ')
731         f.write('\n**********************************')
732         f.close()
733         result=tkMessageBox.askyesno('M2Spice - Conversion Finished!', ...
                message='Successfully generated the netlist! The netlist is ...
                saved at:\n\n'  + self.netlistfilename +'\n\n Do you want to ...
                open the netlist now?')
734         if result==True:
735             f=open(self.netlistfilename,'r')
736             netlist=f.read()
737             f.close()
738             viewer = tk.Toplevel(self, bg='white', width=700,height=500)
739             viewer.title("M2Spice - Netlist Viewer")
740             viewarea = ...
                    tk.Frame(viewer,height=100,width=50,bg='white',borderwidth=1)
741             viewscrollbar=tk.Scrollbar(viewarea)
742             editArea=tk.Text(viewarea,width=100,height=30,wrap="word",...
743 yscrollcommand=viewscrollbar.set,borderwidth=0,highlightthickness=0)
744             viewscrollbar.config(command=editArea.yview)
745             viewscrollbar.pack(side="right",fill="y")
746             editArea.pack(side="left",fill="both",expand=True)
747             editArea.insert(tk.INSERT,netlist)
748             viewarea.place(x=20,y=20)
749             sw = viewer.winfo_screenwidth()
750             sh = viewer.winfo_screenheight()
751             w = int(sw*0.6)
752             h = int(sh*0.6)
753             x = sw-w
754             y = sh-h
755             viewer.geometry('%dx%d+%d+%d' % (w, h, x, y))
756   def try_generate_netlist(self):
757     try:
```

```
758         self.generate_netlist()
759       except Exception as e:
760         tkMessageBox.showerror('M2Spice - Conversion Failed', ...
                message='Failed to generate the netlist. System reported the ...
                following errors: \n\n' +e.message + '\n\nPossible reason: 1. ...
                invalid saving address; 2. invalid geometry format'+'\n\nPlease ...
                check the saving address and geometry status.')
761 class ScrollbarFrame(Frame):
762   def __init__(self, root):
763     Frame.__init__(self, root,height=800,width=900)
764     self.canvas = Canvas(root, borderwidth=2, bg='white')
765     self.frame = GUI(root)
766     self.hsb = Scrollbar(root, orient="horizontal", ...
            command=self.canvas.xview)
767     self.vsb = Scrollbar(root, orient="vertical", command=self.canvas.yview)
768     self.canvas.configure(xscrollcommand=self.hsb.set,...
769 yscrollcommand=self.vsb.set)
770     self.vsb.pack(side="right", fill="y")
771     self.hsb.pack(side="bottom",fill="x")
772     self.canvas.pack(side="top", fill="both", expand=TRUE, padx=30,pady=10)
773     self.canvas.create_window((4,4),window=self.frame, anchor="nw", ...
            tags="self.frame")
774     self.frame.bind("<Configure>", self.OnFrameConfigure)
775     #self.canvas.bind_all("<MouseWheel>", self._on_mousewheel)
776   def OnFrameConfigure(self, event):
777     '''Reset the scroll region to encompass the inner frame'''
778     self.canvas.configure(scrollregion=self.canvas.bbox("all"))
779   def _on_mousewheel(self, event):
780     self.canvas.yview_scroll(-1*(event.Δ), "units")
781 if __name__=='__main__':
782   root=Tk()
783   mainframe=ScrollbarFrame(root)
784   root.mainloop()
```

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