Electrochemical Charge Transfer Reaction Kinetics at the Silicon-Liquid Electrolyte Interface

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Electrochemical Charge Transfer Reaction Kinetics at the Silicon-Liquid Electrolyte Interface

Tushar Swamy\textsuperscript{a} and Yet-Ming Chiang\textsuperscript{b,*,z}

\textsuperscript{a}Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA
\textsuperscript{b}Department of Material Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

Since the gravimetric lithiation capacity of silicon is roughly ten times that of graphite, while their mass densities are comparable, for the same particle size the current density required to cycle a silicon electrode at a given C-rate is about ten times greater than that of graphite. Depending on the magnitude of the corresponding Butler-Volmer exchange current density, \( j_0 \), such high current densities may cause the charge transfer kinetics at the silicon-electrolyte interface to become rate limiting. Previously reported values of \( j_0 \) for Si differ by about 10 orders of magnitude. Here we report \( j_0 \) measurements using electrochemical impedance spectroscopy (EIS) for single crystal electronically conductive silicon wafers with well-defined (100) and (111) orientations and active surface areas. The electrochemical cycling regime was designed to avoid artifacts due to stress-induced surface cracking of Si upon lithiation. The exchange current density of the silicon-electrolyte interface is found to be 0.1 ± 0.01 mA/cm\(^2\) when using electrolyte consisting of 1 M LiPF\(_6\) in EC/DMC (1/1 by wt.) + FEC (10 wt\%)+ VC (2 wt\%). These results are then used to illustrate the dependence of kinetic overpotential on particle size and C-rate for silicon compared to lower volumetric capacity compounds such as graphite.

In order to satisfy the rising demand for high performance and affordable lithium-ion batteries for mobile energy storage applications, the development of high capacity active materials is necessary. Amongst anode candidates,\textsuperscript{1–6} silicon is especially attractive owing to its high specific capacity (3579 mAh/g for lithiation to the amorphous LiC\(_6\) phase) and high natural abundance.\textsuperscript{4,21–24} However, silicon electrodes suffer from accelerated capacity fade compared to established intercalation electrodes, which is attributed to losses originating from fracture and fragmentation induced by the nearly 300\% particle volume expansion upon lithiation.\textsuperscript{4,25} The general trend toward nanoscaling of silicon electrodes, which is attributed to losses originating from fracture and fragmentation induced by the nearly 300\% particle volume expansion upon lithiation,\textsuperscript{4,25} has been motivated almost entirely by these considerations. Novel electrode architectures\textsuperscript{3,16,26–32} and cycling regimes have been developed to limit capacity fade,\textsuperscript{4,23} and modeling\textsuperscript{22} can guide the design of fracture-resistant microstructures. However, an equally important, and to our knowledge overlooked consideration, is the high interfacial current density (current per area of particle/liquid electrolyte interface) required to access the exceptionally high volumetric capacity of Si (8.3 Ah/cm\(^3\) vs. 0.84 Ah/cm\(^3\) for graphite). Since the reduction of particle size (increase of surface area/volume ratio) also reduces the current density necessary to charge or discharge the particle at a given C-rate, nanoscaling has the additional consequence of lowering the interfacial overpotential required to drive the electrochemical charge-transfer reaction. In this work we seek to understand electrochemical charge transfer kinetics at the silicon-liquid electrolyte interface, and its role in determining the performance of silicon anodes.

A few studies have previously reported Butler-Volmer exchange current density values for the silicon electrode,\textsuperscript{11,22,33–36} wherein the current density is given by:\textsuperscript{37}

\[
\text{1)} \quad j = j_0 \left( e^{\frac{i\eta}{F} \alpha} - e^{\frac{i\eta}{F(1-\alpha)}} \right)
\]

where \( j \) is the current density, \( j_0 \) is the exchange current density (i.e., the materials-dependent parameter that encompasses structure and composition effects at the solid-liquid electrolyte interface), \( \alpha \) is the transfer coefficient (typically assumed to be 0.5), \( F \) is Faraday’s constant (96485 Jmol\(^{-1}\)), \( R \) is the universal gas constant (8.314 Jmol\(^{-1}\)K\(^{-1}\)), \( T \) is temperature, and \( \eta \) is the overpotential. Baggetto et al.\textsuperscript{34} reported exchange current density values as a function of state of charge, with an average value of \( j_0 \sim 1\) mA/cm\(^2\), obtained from periodic electrochemical impedance spectroscopy (EIS) experiments during galvanostatic intermittent titration tests (GITT) of a 50 nm thick polycrystalline silicon films deposited using low pressure chemical vapor deposition. The geometric planar area of the electrode was used to calculate the exchange current density. Since the electrode initially underwent a complete lithiation/delithiation cycle and the EIS experiments were conducted during delithiation of the fully lithiated Li\(_x\)Si\(_4\) phase, the silicon film will experience tensile stresses that may induce cracking and the creation of additional electroactive surface area.\textsuperscript{12} Sethuraman et al.\textsuperscript{31,38} reported density \( j_0 \) value of \( 10^{10}\) mAh/cm\(^3\) from fitting open-circuit relaxation data following galvanostatic cycling of silicon thin films deposited by pulse laser deposition. This \( j_0 \) value would imply that only very low C-rates can be used in practice; the kinetic overpotential calculated from the Butler-Volmer equation is \( \sim 1\) V at 1C rate for a Si particle diameter of 150 nm. In another study, Chandrasekaran et al.\textsuperscript{31} obtained \( j_0 \sim 10^{-5}\) mAh/cm\(^2\) upon tuning their single silicon particle model to fit experimental cyclic voltammetry (CV) and GITT data obtained from silicon composite and nanowire electrodes.\textsuperscript{33} A similar CV and potentiostatic intermittent titration technique (PITT) experimental data fitting approach was employed by the Cheng group, who however obtained hundredfold higher exchange current density of \( \sim 0.1\) mA/cm\(^2\).\textsuperscript{35,36} Exchange current density data from the reviewed literature is summarized in Table I. Clearly, there is enormous variability in the reported values of exchange current density for the silicon-liquid electrolyte interface.

Experimental

To overcome previous sample configuration uncertainties, we developed an experimental methodology that uses single-crystal silicon wafers of defined orientation and surface area, along with a cycling procedure that avoids electrode surface cracking but allows establishment of the solid-electrolyte interphase (SEI) representative of a
typical silicon-liquid electrolyte interface. Chon et al. studied stress and damage evolution in a crystalline silicon wafer during the initial lithiation-delithiation cycle, and found that in the first lithiation half cycle, a surface layer of amorphous lithiated silicon phase forms on the crystalline wafer. The volume expansion of the amorphous layer during lithiation is constrained by the underlying crystalline phase, giving rise to surface compressive stresses that do not cause mechanical damage. Subsequent delithiation of the amorphous layer creates tensile stresses leading first to plastic deformation followed by fracture at the end of delithiation. In the present work, we limited cycling to the first lithiation half-cycle down to 50 mV w.r.t. Li/Li⁺, during which SEI growth is facilitated and the quasi-equilibrium potential for lithiation/delithiation is reached. Thereafter, EIS experiments were conducted to measure the electron transfer reaction resistance from which the exchange current density is obtained.

**Table I. Exchange current density values at the silicon-liquid electrolyte interface reported in literature.**

<table>
<thead>
<tr>
<th>Exchange current density (mA/cm²)</th>
<th>Calculated kinetic overpotential at 1C at 5 μm particle diameter (mV)</th>
<th>Reference</th>
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<tbody>
<tr>
<td>~1</td>
<td>~20</td>
<td>34</td>
</tr>
<tr>
<td>10⁻¹⁰</td>
<td>1200</td>
<td>38</td>
</tr>
<tr>
<td>10⁻³</td>
<td>350</td>
<td>11</td>
</tr>
<tr>
<td>~0.1</td>
<td>~100</td>
<td>36</td>
</tr>
</tbody>
</table>

**Electrode/cell preparation.**—Single-side polished crystalline (100) and (111) silicon wafers (500 μm thickness and 0.001–0.005 Ω·cm resistivity, University Wafer, Inc. (Boston, Massachusetts, USA), were scribed and fractured into samples of 0.35–0.5 cm² area. The samples were washed with dimethyl carbonate (DMC), then assembled into two-electrode SwageLok type cells in an Ar-filled glove box. Results were obtained for two electrolyte formulations, a base electrolyte consisting of 1 M LiPF₆ dissolved in a 1:1 weight ratio of ethylene carbonate (EC) and DMC, and an electrolyte typical of current practice consisting of the base electrolyte plus 10 wt% and 2 wt% fluoroethylene carbonate (FEC) and vinylene carbonate (VC), respectively. This electrolyte formulation has been shown to improve Si electrode cycling performance and has been adopted by several research groups.23,32,39,40

**Electrode characterization.**—Silicon wafers with native SiO₂ films were used for all experiments. The thickness of the SiO₂ film was determined to be 15 ± 3 nm, using a variable angle ellipsometer from Gaertner Scientific Corp. (Skokie, Illinois, USA). The surface of the silicon wafer was imaged using a Zeiss Merlin high-resolution scanning electron microscope (SEM) operating under an accelerating potential of 3 kV and a working distance of 5 mm.

**Electrochemical experiments.**—Cyclic voltammetry (CV), potentiostatic cycling, and EIS experiments were conducted at room temperature using a Biologic VMP3 potentiostat. In the CV experiments, the cell voltage was swept from 1 MHz to 10 mHz. The impedance data was fit using least-squares regression analysis.

**Results and Discussion**

To verify when electrochemically-induced fracture does and does not occur, silicon wafers were galvanostatically cycled at a current density of 10 μA/cm² between 50 mV and 1 V w.r.t. Li/Li⁺. SEM images of a typical silicon wafer electrode surface taken immediately after the first lithiation half cycle (to 50 mV) and after the first delithiation half cycle (to 1 V) are shown in Figure 1a and Figures 1b–1d, respectively. The wafer surface is crack free after the first lithiation step, while clear cracks form after the subsequent delithiation step. This result is in agreement with Chon et al.’s stress evolution vs. time data shown in Figure 3 of Ref. 12. It is clear that these cracks form in the silicon itself and not the SEI, as the crack depth (>1 μm) far exceeds the thickness of the SEI (~10 nm). The effect of increasing surface area during repeated cycling was clearly observed in CV experiments (Figure 2). Beginning with a pristine silicon wafer, it is seen that with each successive CV cycle the peak positions are relatively unchanged, but the absolute value of current increases systematically. This behavior is due to the cycling-induced increase in active surface area of the electrode with each successive cycle, and illustrates how errors in geometric area can be readily introduced. In this case there is about a factor of three increase in current density between the second and four cycles, with corresponding errors in the calculated exchange current density.

It has been shown that majority of the SEI growth typically occurs during the first cycle on silicon. In order to measure exchange current densities in the presence of SEI that is typical of silicon anodes in use, the following electrochemical pretreatment was carried out. During the first lithiation (inset in Fig. 2), reduction peaks are observed at ~0.7 V and ~1.6 V w.r.t. Li/Li⁺, which have been attributed to reduction of EC and DMC, respectively. The sloped background showing increasing current with decreasing voltage during this first lithiation half cycle reflects further contributions from solvent and electrolyte salt reduction as the lithiation potential is reduced. In order to grow a stable SEI layer on the silicon wafer surfaces, the cell potential was first held at 150 mV vs. Li/Li⁺ until the current decayed to ~100 nA. Figure 3a. The total charge passed during this period is ~100 µAh or ~0.2 mAh/cm². Next, to lithiate the silicon wafer surface, the cell potential is decreased to 50 mV vs. Li/Li⁺, and held until 200 µAh or 0.4 mAh/cm² of charge has passed (Figure 3a). At
Figure 2. Cyclic voltammetry for a (100) silicon wafer in 1 M LiPF$_6$ in EC/DMC (1/1 by wt) + FEC (10 wt%) + VC (2 wt%) vs. Li metal counter electrode at a scan rate of 25 μV/s. The first lithiation half cycle and three subsequent delithiation/lithiation cycles are shown. While the peak positions remain relatively unchanged, the current systematically increases with each successive cycle as a result of newly formed electrochemically active surface area due to cycling-induced fracture. The inset figure highlights the electrolyte reduction peaks at ∼0.7 V and ∼1.6 V during the first lithiation step.

this area capacity, the depth of the lithiated silicon layer far exceeds the thickness of any SEI, as it is equivalent to ∼1 μm even for the most highly lithiated composition, Li$_{x}$Si. After the lithiation step, the cell was held under open-circuit conditions until the voltage decay rate is below 1 mV/hour, reaching an OCV of ∼0.25 V after 25 hours (Figure 3a). This OCV lies between the oxidation and reduction peaks in Figure 2, allowing lithiation and delithiation to be induced by small bias potentials during EIS.

Figures 3b and 3c show the EIS spectra obtained for (100) orientation wafers after the above pretreatment, for electrolytes with and without the FEC and VC additives, respectively. The equivalent circuit model used to fit the EIS data is shown as an inset in Figure 3b. The Nyquist spectra show the expected features which were fit using 6 circuit elements as follows: A high frequency intercept on the real impedance axis which represents the ohmic transport losses in the electrolyte and bulk-Si is modeled by the resistance, $R_{\text{ohmic}}$. Since highly conductive Si wafers were used, $R_{\text{ohmic}}$ comprises mostly the electrolyte resistance. A characteristic depressed semi-circle follows which is comprised of resistance from charge transport in the SEI film and the charge transfer reaction at the silicon electrode surface, both of which are modeled using parallel RC circuits in series with elements $R_{\text{SEI}}$, constant phase element $\text{CPE}_{\text{SEI}}$, and $R_{\text{ct}}$, $\text{CPE}_{\text{ct}}$, respectively. CPE’s are often used in models in place of capacitors to model the inhomogeneity in the system. It has been shown that charge transfer across the SEI film is activated at a higher characteristic frequency (∼10 kHz) compared to the surface electron transfer process (∼100 Hz), which can be estimated as $\omega_{\text{SEI}} = (R_{\text{SEI}}\text{CPE}_{\text{SEI}})^{-1}$ and $\omega_{\text{ct}} = (R_{\text{ct}}\text{CPE}_{\text{ct}})^{-1}$, respectively, where $\text{CPE}_{\text{SEI}}$ and $\text{CPE}_{\text{ct}}$ are the near capacitive impedance components of $\text{CPE}_{\text{SEI}}$ and $\text{CPE}_{\text{ct}}$, respectively. By evaluating and comparing the characteristic frequencies of the two RC circuits, circuit elements corresponding to SEI film resistance and the electron transfer process can be uniquely identified. The semi-circular arc is followed by a ∼45° line which is characteristic of lithium diffusion in bulk Si, and modeled using a Warburg circuit element, $W_{\text{diffusion}}$. Fitting parameter values are summarized in Table II. The average percentage error between the experimental data and the fit, calculated from the weighted sum of squares, is ∼3.3%.

Data for three separate samples are shown in each of Figures 3b and 3c, from which a high degree of reproducibility is evident.

Figure 3. (a) Cycling regime conducted prior to the EIS measurements. The Li-Si half-cell is held at 150 mV to grow the SEI layer until the current decays to 100 nA, followed by holding at 50 mV constant voltage to induce lithiation until 200 μAh (0.4 mAh/cm$^2$) of charge has passed. (b) EIS data and fitting using the equivalent circuit shown, for three silicon wafer electrodes, using 1 M LiPF$_6$ in EC/DMC (1:1 by weight) + 10 wt% FEC + 2 wt% VC. (c) Measurements as in (b), performed using 1 M LiPF$_6$ in EC/DMC (1:1 by weight) electrolyte. Note higher impedance compared to case of electrolyte with FEC and VC additives in (b).

The electron transfer reaction resistance, $R_{\text{ct}}$, is summarized in Table III for the nine samples measured, along with the exchange current density, $j_0$, obtained from the linearized Butler-Volmer equation.

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The charge transfer reaction is approximated as a one-electron process \((n = 1)\), and the surface area, \(A\), is assumed to be the geometric area (0.5 cm\(^2\) for (100) wafers and 0.35 cm\(^2\) for (111) wafers). \(j_o\) is thus found to be 0.1 ± 0.01 mA/cm\(^2\) and 0.09 ± 0.01 mA/cm\(^2\) for the electrolytes with and without FEC and VC, respectively, in the case of the (100) wafers. Note the very similar \(j_o\) despite the larger difference in the impedance intercept (Figs. 3b and 3c), which shows that in the equivalent circuit model there is a larger contribution from the lithium formed. Thus the dependence of \(j_o\) on SOC was not characterized in this study.

While it is known that \(j_o\) is generally a function of the electrode state of charge (SOC),\(^{37}\) an accurate determination of this relationship for silicon electrodes is challenging because of the uncertainty in estimating SOC during the first lithiation step due to the irreversible consumption of Li for SEI layer growth and the phase transformation from crystalline to amorphous silicon. As discussed earlier, the active area changes during subsequent cycles due to surface cracking, introducing further uncertainty into the exchange current density measurements. Thus the dependence of \(j_o\) on SOC was not characterized in this study.

The implications of these results for silicon negative electrodes are now considered. In Table IV, reported exchange current density values for several anode and cathode materials are listed. The current density \(j\) required to charge or discharge an isolated particle of volume \(V\), surface area \(A\), density \(\rho\), and specific capacity \(c\) is:

\[
j = \frac{i}{A} = \frac{Q \times \tau}{A} = \frac{(c \times \rho \times V) \times c}{A} = (c \times \rho) \left( \frac{V}{A} \right) C
\]

Here \(i\) is the current, \(Q\) is the charge passed, and \(C\) is the C-rate. For spherical particles Eq. 3 simplifies to:

\[
j \approx (c \times \rho) \frac{d}{6} \times C
\]

Consider specifically the cases of silicon and graphite. The product \((c \times \rho)\) in Eq. 4, containing the materials parameters, is about ten times greater for silicon compared to graphite (\(\sim 8.3\) Ah/cm\(^3\) for Si vs. \(\sim 0.84\) Ah/cm\(^3\) for graphite). The effect of lithiation on molar volume, although not explicitly written, results in nearly compensating effects of molar volume expansion and decreasing density upon lithiation. Therefore, for a given C-rate and particle diameter, the current density at a silicon particle surface is also about ten times greater than for a graphite particle. The usable conditions for each electrode material are related to the value of the kinetic overpotential, which for small overpotentials is given by:

\[
\eta \approx \left( \frac{RT}{F} \right) \left( \frac{j}{j_o} \right)
\]

In Figure 4, we plot the overpotential as a function of particle diameter (up to 5 \(\mu\)m) and C-rate (up to 10C rate) for silicon and graphite, respectively, using \(j_o\) values from the current work for silicon and from reference\(^{43}\) for graphite. We assume isotropic surface properties for the reasons discussed earlier, and neglect any SOC dependence of \(j_o\). For silicon, the overpotential at 1 \(\mu\)m and 2C rate is \(\sim 60\) mV, and at 5 \(\mu\)m and 10C rate is \(\sim 220\) mV. For graphite under the same conditions, the overpotential is \(\sim 1\) mV and \(\sim 20\) mV, respectively. These comparisons show the limitations presented by the combination of a low exchange current density and very high volumetric capacity for...
silicon (and by inference, other high capacity metal and metalloid anodes).

High overpotentials combined with low insertion potentials will result in lithium plating at the anode at a critical C-rate that can be determined for each material. Obrovac and Krause\(^4\) have shown that micron-sized silicon (325 mesh, 44\(\mu\)m maximum particle size) can be reversibly cycled at \(~0.25\) C if the composition is not allowed to reach a critical lithium concentration inducing crystallization of the amorphous alloy. The present results show that fracture aside, a low C-rate would be necessary to avoid lithium plating under such conditions. Liu et al. have argued that upon repeated cycling, large silicon primary particles crack and break into smaller particles until each particle reaches a critical diameter of approximately \(~150\) nm.\(^{25}\) Assuming isolated particles of this size at a 1C rate, the kinetic overpotential is tolerable at \(~5\) mV. However, since silicon nanoparticles are often strongly agglomerated, the effective particle size may be larger, and the exposed surface area correspondingly smaller, than that of the primary particles.

The exchange current density at the silicon-liquid electrolyte interface was measured by EIS on polished silicon wafers of (100) and (111) orientations. An electrochemical cycling regime was used that allowed fracture reduction to submicron primary particle size.

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### References


### Table IV. Reported exchange current density values for several electrode materials.

<table>
<thead>
<tr>
<th>Material</th>
<th>Exchange Current Density (mA/cm(^2))</th>
<th>Electrolyte</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>0.1</td>
<td>1 M LiPF(_6) in EC/DMC (1/1 by wt) + FEC (10 wt%)</td>
<td>Present work</td>
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<tr>
<td>Graphite</td>
<td>1-2.3</td>
<td>1 M LiPF(_6) in EC/DMC</td>
<td>44</td>
</tr>
<tr>
<td>LiTiO(_2)</td>
<td>0.81</td>
<td>1 M LiPF(_6) in EC/DEC</td>
<td>45</td>
</tr>
<tr>
<td>LiCoO(_2)</td>
<td>2.5-6.2</td>
<td>1 M LiPF(_6) in EC/EMC/DMC</td>
<td>46</td>
</tr>
<tr>
<td>LiFePO(_4)</td>
<td>0.17</td>
<td>1 M LiPF(_6) in EC/DEC</td>
<td>42</td>
</tr>
<tr>
<td>LiNi(<em>{0.33})Co(</em>{0.33})Mn(_{0.33})O(_2)</td>
<td>0.25-23.6</td>
<td>1 M LiPF(_6) in EC/EMC/DMC</td>
<td>47</td>
</tr>
</tbody>
</table>

### Figure 4.

Overpotential for (a) silicon, and (b) graphite, as a function of particle diameter (0–5 \(\mu\)m) and C-rate (0–10C). For silicon, the overpotential reaches \(~220\) mV at 5 \(\mu\)m and 10C rate, whereas for graphite, the overpotential is \(~20\) mV under the same conditions.