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Effect of Substrate Contact Shape and Placement on RF Characteristics of 45 nm Low Power CMOS Devices

Usha Gogineni¹, Hongmei Li², Susan Sweeney², Jing Wang³, Basanth Jagannathan³, Jesus del Alamo¹

¹Massachusetts Institute of Technology, Cambridge, MA, ²IBM Microelectronics, ³Essex Junction, VT, ³Hopewell Junction, NY

Abstract — The substrate resistance of 45 nm CMOS devices shows a strong dependence on the distance between the device edge and the substrate ring; as well as on the number of sides that the device is surrounded by the contact ring. We find that the unilateral gain is impacted by the substrate resistance (Rₛₓ) through the gate-body capacitance feedback path at low to medium frequencies (< 20GHz). At mm wave frequencies, the unilateral gain is affected by the Rₛₓ through the drain-body capacitance pole, and deviates from the ideal -20dB/dec slope. The impact of substrate resistance on fₜ, maximum available gain, high frequency noise and power characteristics of the devices is minimal.

Index Terms — Substrate resistance, Noise, RF CMOS, maximum oscillation frequency, power gain, unilateral gain.

I. INTRODUCTION

CMOS is becoming an increasingly popular choice for radio frequency (RF) circuits and system-on-chip designs. It is well known that parasitic substrate resistance adversely affects the high frequency performance of CMOS devices. A commonly used method for reducing substrate resistance is to place substrate contacts in a ring around the MOSFET. The dependence of substrate resistance on the number of device fingers has been extensively studied [1-3]. However, the effect of substrate contact ring shape and proximity has not been fully explored. In addition, previous work is limited to the modeling of substrate resistance; its impact on RF circuit design and power gain is not well explained.

This work presents a detailed study of the impact of substrate ring shape and placement on the substrate resistance and high frequency figures of merit of 45 nm CMOS devices. Section II presents measured results for substrate resistance, cut-off frequency (fₜ) and maximum oscillation frequency (fₘₐₓ) for structures with varying substrate ring shape and position relative to the device. Section III proposes an accurate model to explain the measured dependence of unilateral gain and fₘₐₓ on substrate resistance and section IV discusses the implications of substrate resistance on power gain, power added efficiency, unilateral gain, and high frequency noise of CMOS devices.

II. MEASUREMENTS

Device test structures with varying substrate contact ring shape and placement were designed and fabricated using IBM’s 45 nm low-power RFCMOS process [4]. All devices have a gate length of 0.04 µm, a total gate width of either 60 µm (20 fingers of 3 µm width) or 180 µm (60 fingers of 3 µm width) and a substrate ring width of either 0.16 µm or 0.32 µm. The devices are in a common-source configuration with body node tied to the source. S-parameter measurements from 1 GHz to 110 GHz were performed on these test structures at V₉S = 0 V and 0.8 V and VₐS = 1.1 V. The substrate resistance was estimated from the zero gate bias S-parameter data using the following expression [1]:

\[ R_{sx} = \frac{\text{real}(Y_{zz})}{(\text{imag}(Y_{zz} + Y_{11}))^2} \]

Fig. 1. Substrate resistance as a function of distance between device edge and substrate contact ring in the gate width (X) and gate length (Y) directions.

The first set of test structures have a gate width of 20x3 µm and are designed to explore the effect of sharing a substrate ring between adjacent devices. We vary the distance between the device edge and substrate ring, in a direction parallel to the gate (X) and perpendicular to the gate (Y). The reference device has a dedicated substrate ring with X=0.53 µm and Y=0.46 µm and a substrate ring width of 0.16 µm.

Keeping X constant at 0.53 µm and varying Y from 0.46 µm to 7 µm increases Rₛₓ by 16% (Fig. 1). Varying X, with

Y constant at 0.46 μm, results in a greater increase of $R_s$ by 23%. The biggest increase in $R_s$ is seen when both X and Y are simultaneously increased. An increase of 142% is observed for $X=Y=7$ μm, as compared to the reference device. These results can be explained as follows: When only X or Y is increased, the closest contact becomes the de facto contact to the substrate. Also, having the substrate contact perpendicular to the gate (the case of X short) ensures proximity of the contact to more of the drain fingers resulting in lower $R_s$. Fig. 1 also shows that wider substrate contact ring reduces $R_s$ (17% reduction when the ring width is increased from 0.16 μm to 0.32 μm).

Fig. 2. Substrate resistance for different substrate ring shapes. The red-white area in the ring contains both diffusion and metal 1 layers, while the solid red area contains only diffusion.

The second set of test structures have a gate width of 60x3 μm and are designed to explore the shape of the substrate ring. To facilitate wiring, designers may choose to omit portions of the substrate ring, either from both the diffusion and Metal 1 (M1) ring (RX+M1), or from the M1 ring alone. In one variation, RX+M1 ring is varying: either on all four sides (reference, in Fig.1), on three sides (RX+M1 U-shape), on two sides (RX+M1 L-shape), or on one side (RX+M1 top) of the device. An increase in $R_s$ of 64% is observed from a full substrate ring to a one-sided contact (Fig. 2).

Fig. 3. $f_T$ and $f_{max}$ (measured at $V_{GS}=0.8$ V and $V_{DS}=1.1$ V) as a function of device edge to substrate contact ring distance.

Fig. 2 also shows the substrate resistance for a set of designs that vary the M1 portions of the ring only: either on three sides of the device (M1 U-shape), on one side and perpendicular to the gate (M1 Top) or on one side and parallel to the gate (M1 Left). The diffusion ring is always present in this case. The substrate resistance for this set of devices is lower than when both diffusion and M1 are varied, as one would expect. Also $R_s$ is higher when the substrate contact is parallel to the gate direction than when it is perpendicular to the gate. This is because most fingers are far away from the contact bar when the contacts are in parallel with the gate.

Fig. 3 shows the change in the unity current gain cut-off frequency ($f_T$) and the maximum oscillation frequency ($f_{max}$) when the distance between the device edge and the substrate ring is varied. Fig. 4 shows $f_T$ and $f_{max}$ for variations in substrate ring shape. No significant difference is observed in $f_T$ in fig.3 and fig.4 because the variation in gate parasitic capacitance, for the structures studied here, is not significant enough to change $f_T$. The data also shows negligible variation in $f_{max}$ in spite of the relatively small change in substrate resistance (maximum increase 142%).

III. MODEL

A model for the high frequency figures-of-merit can be derived based on the small signal equivalent circuit shown in Fig. 5. The circuit includes gate resistance ($R_g$), gate-source ($C_{gs}$), gate-drain ($C_{gd}$), gate-body ($C_{gb}$), source-body ($C_{sb}$) and drain-body ($C_{db}$) capacitances, transconductance ($g_m$), output resistance ($r_o$), and substrate resistance ($R_s$). Previous studies [1-3] have ignored the presence of $C_{gb}$, which will be shown to affect unilateral gain significantly, even with a value as small as 2 fF arising from fringe capacitance.

The y-parameters for the above equivalent circuit can be derived as follows:

$$Y_1 = \frac{j\omega C_{gs} R_s}{1 + R_s j\omega C_{gs}}$$

$$Y_2 = \frac{-j\omega C_{gd} R_s}{1 + R_s j\omega C_{gs}} \left( \frac{1}{1 + R_s j\omega C_{gs}} \right) \frac{1}{\left(1 + R_s j\omega C_{gs} + C_{gb} + C_{db}\right)}$$

$$Y_3 = \frac{-j\omega C_{gb} R_s}{1 + R_s j\omega C_{gs}} \left( \frac{1}{1 + R_s j\omega C_{gs}} \right) \frac{1}{\left(1 + R_s j\omega C_{gs} + C_{gb} + C_{db}\right)}$$
\[
Y_{11} = \frac{j\omega C_{gs}(1 + g_{m} R_s + j\omega (C_{ps} + C_{ds}) R_s)}{1 + j\omega (C_{ps} + C_{ds}) R_s}
\]

\[
Y_{12} = \frac{j\omega C_{gs}(1 + j\omega (C_{ps} + C_{ds}) R_s)}{1 + j\omega (C_{ps} + C_{ds}) R_s}
\]

\[
Y_{21} = \frac{j\omega C_{gs} R_s}{1 + j\omega (C_{ps} + C_{ds}) R_s}
\]

\[
Y_{22} = \frac{1}{1 + j\omega (C_{ps} + C_{ds}) R_s}
\]

For the 20x3 μm reference device, the intrinsic parameters are extracted from S-parameter measurements at V_{GS}=0.8 V, V_{DS}=1.1 V as: C_{gs}=27 fF, C_{gd}=14 fF, g_{m}=48.4 mS, r_o=192 Ω, C_{db}=C_{sb}=37 fF, R_{sx}=76 Ω and C_{gb}=2 fF.

For these values, Y_{11}, Y_{12} and Y_{21} are found to be insensitive to R_{sx}. As a result, the substrate resistance has no effect on the current gain, maximum stable gain or f_{T} of these devices.

The unilateral power gain can be expressed in terms of y-parameters as [5]

\[
U = \left| Y_{11} - Y_{21} \right|^2 / \left[ \left( 4 |\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12})\text{Re}(Y_{21}) \right) \right]
\]

Retaining only the significant terms, U can be approximated as

\[
U = \frac{g_{m} r_o / (4 R_s C_{gs} \omega^2)}{C_{gs} + g_{m} C_{ps} + \omega^2 R_s C_{ps} R_s - R_s g_{m} C_{ps} C_{ds} + \omega ^2 C_{ps} R_s (1 + \omega^2 (C_{ds} + C_{ps} + C_{db}) R_s )}
\]

The traditional unilateral gain derivation only considers the first 2 terms in the denominator of (1). We include the new effect of R_{sx} and its interaction with C_{db} and C_{gb}. Fig. 6 plots the measured and modeled U for the reference device and the device with X=Y=7 μm. Our small-signal model is in excellent agreement with data in both the high frequency and low frequency regions. Note that U is negative at low to medium frequencies (up to 20 GHz). At this frequency range, the presence of substantial R_{sx} and C_{gb} causes the 4th term in the denominator of (1) to dominate and leads to negative U.

\[
U_{U_{\text{MAX}}} = \frac{g_{m} r_o / (4 R_s C_{gs} \omega^2)}{C_{gs} + g_{m} C_{ps} + \omega^2 R_s C_{ps} R_s - R_s g_{m} C_{ps} C_{ds} + \omega ^2 C_{ps} R_s (1 + \omega^2 (C_{ds} + C_{ps} + C_{db}) R_s )} < 0
\]

The physical mechanism is that C_{db}, C_{gb}, and R_{sx} create a positive feedback path between gate and drain, resulting in negative unilateral gain.

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**IV. CIRCUIT DESIGN IMPLICATIONS**

Power measurements were performed at 6 GHz by tuning the source and load impedances for maximum power gain. Fig. 8 shows the maximum power gain and the peak power added efficiency (PAE) as a function of distance between substrate contact ring and device edge. The increase in R_{sx} by 140% in going from the reference device to the X=Y=7 μm device has negligible effect on the power gain and the peak PAE. The maximum power gain is correlated to the maximum stable gain (MSG) and PAE is strongly correlated to f_{max}[6]. Since MSG and f_{max} are relatively insensitive to the change in substrate
resistance, it makes sense that the power characteristics are also insensitive to substrate resistance.

Fig. 8. Maximum power gain and peak power added efficiency at 6 GHz as a function of device edge to substrate ring distance. Device biased at V_GS=0.8 V and V_DS=1.1 V.

The drain noise spectral density as a function of frequency is shown in Fig. 9 for a 60x3 μm device with different substrate ring shapes. There is no discernable difference in the high frequency noise data with increasing substrate resistance (from 60 Ω to 98 Ω in this data set). This amount of variation in the substrate resistance is not significant enough to modulate the noise figure as the noise at the measured bias is dominated by other noise sources such as channel noise and gate induced noise.

The drain noise spectral density as a function of frequency for structures with different substrate contact ring shapes. Device biased at V_GS=0.8 V and V_DS=1.1 V.

The impact of substrate resistance on unilateral gain is an important consideration for designers. One popular design practice is to use feedback to cancel various loss paths in the device, thus achieving the highest gain in the circuit [7]. When R_xx C_gb is significant, unilateral gain becomes negative at the design frequency (<20 GHz), making the circuit unstable. A compensation network that cancels out the internal substrate resistance effect would then be required to stabilize the circuit. Hence, an accurate model for the substrate resistance and its impact on unilateral gain is essential for successful designs. A more comprehensive 5-resistor network substrate model is presented in [4].

The findings from this work can be used in making informed design trade-off decisions. For example, it has been shown that minimizing R_xx and parasitic C_gb capacitance is key to stabilizing U. One effective way to reduce R_xx is using a dedicated substrate contact ring for each device. A wider contact ring has been shown to reduce R_xx further, but may increase C_gb. C_gb can be reduced by optimizing the gate poly and metal wiring.

V. CONCLUSION

The impact of substrate contact ring shape and position on the substrate resistance, f_t, and f_max of 45 nm CMOS devices is presented. An increase of 140% in the substrate resistance is observed when the distance between the device edge and the substrate ring is increased from 0.46 μm to 7 μm on all sides of the device. R_xx increases by 64% in going from a ring contact to a one sided contact. f_t, high frequency noise, power gain and power added efficiency are relatively insensitive to the moderate changes in substrate resistance in the range that has been studied in this work. A small signal model is created to accurately predict the impact of R_xx on Y-parameters and unilateral gain. The low to medium frequency unilateral gain has a strong dependence on C_gb and R_xx, while the high frequency U and f_max are modulated by C_gb and R_xx.

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