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Radiation Effects in MIT Lincoln Lab 3DIC Technology


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MITLL has developed a three dimensional integrated circuit (3DIC) technology that exploits the advantages of SOI technology to enable wafer stacking and micrometer-scale vertical interconnection of fully fabricated circuit wafers [1,2]. This paper presents the first radiation test results on this 3DIC technology.

3D fabrication process

Devices and circuits are fabricated by transferring and interconnecting fully fabricated 150-mm SOI substrates to a base wafer, also a fully fabricated 150-mm SOI substrate. Wafer-level integration is enabled by bonding oxide films at low temperature. High circuit density is enabled by fabricating 3D-vias to interconnect the different tiers. Figure 1 shows a cross-section scanning electron micrograph of a 3DIC wafer showing three FDSOI CMOS tiers, eleven metal layers, and 3D vias interconnecting tiers 1, 2 and 3. On tiers 2 and 3, FETs are inverted so that front gates are below the SOI, the BOX is above the SOI, and the original silicon substrate was removed and replaced by deposited oxides.

Figure 1: Scanning Electron Micrographs of a 3DIC wafer with three FDSOI CMOS tiers, eleven metal interconnect layers, and 3D vias interconnecting tiers 1, 2 and 3. The dashed lines were drawn to mark the oxide-oxide bonding interface.

Description of the experiment

Total ionizing dose (TID) effects were characterized using an Aracor 4100, which produces 10-keV X-rays. FDSOI MOSFETs and multiplier circuits were biased during irradiation and characterized before and after dose increments up to a total dose of 2 Mrad (SiO2). We characterized n-channel MOSFETs (nFETs) fabricated on each tier of 3D wafers, each wafer fabricated on MITLL 0.18-μm FDSOI CMOS process. The process features a 45-nm-thick SOI, 400-nm-thick BOX, 4.2-μm-thick gate oxide, a mesa isolation, cobalt silicided source/drain/polysilicon gate, and three metal levels [3]. 10-keV X-rays are not attenuated when penetrating through the 20-μm-thick oxide layers down to the bottom FETs on tier 1.

Radiation test results

When exposed to ionizing radiation, MITLL FDSOI FETs degrade because of radiation-induced positive charges trapped in the BOX [4]. The gate and mesa oxides are both thin enough (4.2-nm) that holes generated by the radiation tunnel through them, and don’t get trapped. The positive charges trapped in the BOX cause the nFET (pFET) threshold voltage (Vth) to decrease (increase) because the SOI body is fully depleted, and the BOX is capacitively coupled to the front gate. A decrease in Vth causes an increase in nFET leakage current, which can yield to circuit parametric failure, or even permanent damage.

Figure 2 shows the threshold voltage shift (ΔVth) versus TID for W=8-μm, L=0.18-μm nFETs on a single tier wafer and on each of the three tiers of a 3DIC wafer. Vth was calculated by extrapolation at the maximum transconductance point at a drain voltage, VD, of 0.05 V. The increase in |ΔVth| with dose is similar on the single tier wafer and on 3DIC tier 1. This is not surprising because the nFETs have the same layer stack and design. Above 30 krad (SiO2), Figure 2 shows that ΔVth is smaller on tier 2 and 3 than on tier 1. Also ΔVth rebounds at lower dose on tier 2 and 3 than on tier 1. The rebound is due to the radiation-induced build-up of traps at the SOI/BOX interface becoming larger than the build-up of fixed positive charge [6]. Because interface traps are electron traps (negative charge), ΔVth becomes positive.

Figure 2: Threshold voltage shift versus TID for W=8-μm, L=0.18-μm nFETs on a single tier wafer and on each tier of a 3DIC wafer (offgate bias during irradiation, VD=1.5 V).

Figure 3 compares ΔVth for nFETs on the single tier wafer (same curve as on Figure 4) and on a single tier wafer that has been bonded to a bulk Si wafer (handle wafer) and after complete removal of the silicon substrate below the BOX. The BOX, now on top, was etched above the bondpads to probe the nFETs. The change in ΔVth with dose is analogous for the nFETs with no substrate/single tier wafer (Figure 3) and on tier 3 of a 3DIC wafer (Figure 2). This indicates that the absence of silicon substrate influences the density of positive charge trapped in the BOX.

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Figure 3: Threshold voltage shift versus TID for W=8-μm, L=0.18-μm nFETs on a single tier wafer and on a single tier wafer bonded to another wafer and substrate removed (offgate bias during irradiation).

Figure 4 shows that ΔV_t for nFETs on tier 3 is lower in ongate than in offgate bias during irradiation. This result is typical for MITLL FDSOI technology [4] because of the mesa isolation (no thick field oxide) and because the electric field in the BOX is higher when V_D=1.5 V than V_C=1.5 V, thereby yielding higher trap density offgate than ongate.

Figure 5 compares ΔV_t for W=0.6 and 8-μm wide nFETs on a single tier wafer and on tier 3 of a 3DIC wafer in offgate bias. On a single tier wafer, the polysilicon gate exerts a better control over the potential at the SOI/BOX interface when W=0.6-μm than when W=8-μm because the gate wraps around the body of the FET on the SOI mesa edge. This result is analogous to the characteristics of an omega-FETs (known as Fin-FETs) where positive charge build up in the BOX is reduced for narrow fins [7]. On 3DIC tier 3 and for W=8-μm nFETs, the absence of a silicon substrate below the BOX does not change how the gate controls the SOI/BOX potential, so we infer that the electric field distribution and or strength in the BOX itself has changed yielding less charge trapping. Furthermore, the dose at which ΔV_t rebounds appears to scale with the positive charge build-up rate. This seem to indicate that the electron-trap build-up rate has remained unchanged and similar on the integrated tiers as on the single tier wafer. On tier 2, the nFETs exhibit less positive charge build-up than on tier 3. Tier 2 transistors have a thicker oxide with different composition and a bonding interface behind the SOI which may affect their radiation response. We will continue studying circuits on 3DIC tier 2 in future fabrication runs.

Figure 6 shows the V_DD standby leakage current versus TID for multiplier circuits on a single tier wafer and on 3DIC tier 3. TID effects are similar on both circuits. Since the multiplier is designed with W=0.6-μm, L=0.18-μm FETs, this result is consistent with the nFETs TID data shown in Figure 5.

Figure 6: Multiplier standby leakage current vs. TID on V_DD for circuits on single tier and on tier 3 of a 3DIC wafer.

Conclusion

We characterized TID effects in MITLL 3DIC technology. We found that the effects were comparable for nFETs on the bottom tier with that on single tier wafers. Less positive charge build-up is observed for wide nFETs on the upper tiers, and this is due to the absence of silicon below the BOX. Other results indicate that MITLL 3DIC technology can be hardened to ionizing radiation by modifying the BOX [8].

Acknowledgement

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References