A low-voltage energy-sampling IR-UWB digital baseband employing quadratic correlation

The MIT Faculty has made this article openly available. Please share how this access benefits you. Your story matters.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>As Published</strong></td>
<td><a href="http://dx.doi.org/10.1109/JSSC.2010.2046245">http://dx.doi.org/10.1109/JSSC.2010.2046245</a></td>
</tr>
<tr>
<td><strong>Publisher</strong></td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td><strong>Version</strong></td>
<td>Final published version</td>
</tr>
<tr>
<td><strong>Accessed</strong></td>
<td>Wed Feb 13 10:27:10 EST 2019</td>
</tr>
<tr>
<td><strong>Citable Link</strong></td>
<td><a href="http://hdl.handle.net/1721.1/59998">http://hdl.handle.net/1721.1/59998</a></td>
</tr>
<tr>
<td><strong>Terms of Use</strong></td>
<td>Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.</td>
</tr>
<tr>
<td><strong>Detailed Terms</strong></td>
<td></td>
</tr>
</tbody>
</table>
14.2 A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with ±1ns Synchronization Accuracy

Patrick P. Mercier, Manish Bhardwaj, Denis C. Daly, Anantha P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

IR-UWB radios are finding increasing use in low data rate sensing applications, in part because they can be easily duty-cycled to achieve extreme energy efficiency. Within pulsed radios, non-coherent (NC) RF front ends that use simple square-and-integrate samplers offer significant energy-per-bit savings over their coherent counterparts [1]. However, such samplers lose phase information and accumulate squared noise over the integration period. While this increases the SNR required to relay a bit reliably, the greater challenge is achieving signal synchronization. Telemetry applications often have small payload sizes (10 to 100 bits) where synchronization time dominates. Furthermore, synchronization performance is being continually pushed to enable positioning capability. Hence, the ultimate advantage of NC receivers relies on their ability to synchronize efficiently.

Previously published NC solutions are deficient in three areas: synchronization algorithms, codes, and their reliance on high resolution clocks. Current algorithms disregard the effects of squaring noise, and use matched filters (MFs) [2] that are guaranteed to be optimum only when noise is additive, such as the case in coherent receivers [3, 4]. In NC systems, the use of MFs not only increases synchronization time, but make the system very sensitive to errors in estimating SNR. Repetition codes can simplify algorithms by eliminating the need for MFs, but require parallel or sliding integrators in addition to higher SNR or on-time [5]. Synchronization accuracy is also limited by clock speeds with these techniques, as a ±1ns resolution (corresponding to 30cm of positioning accuracy) typically requires a 500MHz clock.

The proposed digital baseband overcomes these shortcomings without any increase in RF front end power or complexity via the following techniques: 1) new synchronization codes that require 11× fewer samples than repetition codes, and which allow high synchronization accuracy (1ns) using slow clocks (32MHz); 2) a new quadratic correlation algorithm that requires 2 to 4dB lower SNR than MFs and is robust to parameter measurement uncertainties; 3) an algorithmic transformation that reduces computational complexity of correlations by up to 32×; and, 4) a low-voltage, highly-parallel VLSI implementation that offers low-latency synchronization. As a result of these techniques, the baseband achieves a peak synchronization accuracy of ±1ns at an SNR of 4dB within 16μs.

The packet structure is shown in Fig. 14.2.1. The preamble consists of repetitions of a PN code (S0) selected after a start-frame-delimiter (SFD), header, and payload bits. State-of-the-art codes for NC systems, as proposed in the IEEE 802.15.4a standard [6], are not necessarily alias-free, i.e. two chip period shifts of S0 produce an identical sequence of integrator outputs. Figure 14.2.1 demonstrates this with a toy, 4a-like code. To guarantee no aliasing, the receiver must be able to shift integration slots by a chip period of 1.95ns (or integrate over 1.95ns windows). A simple modification in pulse positions bestows the alias-free property, as Fig. 14.2.1 illustrates. The baseband uses alias-free codes of length 512 chips (0.998μs) with a 31.2ns integration period. This is achieved via an inner quadratic correlation with S0 and S1, and an outer linear correlation that accumulates inner results for all sequences in the codebook. Inner results are stored in a serial shift register (Fig. 14.2.4). Two pairs of QCORRs are used in a time-interleaved fashion to avoid throughput loss or excessive buffering. The search continues until the SFD has the highest correlation, or a pre-specified timeout is reached. In the high SNR regime, the circuit can also be programmed to search for a length 1 SFD to reduce preamble duration.

Implemented in 90nm CMOS, the digital baseband occupies 2.55mm2 on an SoC with an integrated RF front end and 5b ADC [7]. The baseband operates at a core supply voltage as low as 0.5V. During detection and synchronization processes, the baseband dynamically duty-cycles the RF front end to reduce system power. At a clock frequency of 32MHz, the chip can process an entire preamble in a minimum of 14μs and consumes an average of 1.6mW. A summary of results is shown in Fig. 14.2.6. A die photo is shown in Fig. 14.2.7.

Acknowledgments
This work is funded by DARPA Hi-MEMS program (Contract # F30602-07-C-1704). The authors thank STMicroelectronics for chip fabrication and Nathan Ickes for testing support.

References
Figure 14.2.1: Non-coherent UWB block diagram, with illustrated packet structure and alias-free codes.

Figure 14.2.2: Digital baseband block diagram.

Figure 14.2.3: Phase-correlation tile with 8 QCORRs.

Figure 14.2.4: SFD and QCORR circuits.

Figure 14.2.5: Synchronization error rates (SERs) for ±1ns accuracy with ideal and mismatched SNRs.

Figure 14.2.6: Table of measured results and power profile.
Figure 14.2.7: Die micrograph of the IR-UWB digital baseband processor.