A low-voltage energy-sampling IR-UWB digital baseband employing quadratic correlation
correlation tiles (PCTs). Each PCT, as shown in Fig. 14.2.3, consists of 8 parallel shifts of $S_0$ produce an identical sequence of integrator outputs. Figure 14.2.1 Every sample duration corresponds to 16 possible signal starts, or phases, $252 \times 2009$ IEEE International Solid-State Circuits Conference. The top-level architecture of the digital baseband is shown in Fig. 14.2.2. The baseband uses clock gating is employed during detection to reduce clock tree power of the unused PCTs. Overall, clock gating reduces dynamic power by 2.7× during idle mode.

Previously published NC solutions are deficient in three areas: synchronization algorithms, codes, and their reliance on high resolution clocks. Current algorithms disregard the effects of squaring noise, and use matched filters (MFs) [2] that are guaranteed to be optimum only when noise is additive, such as the case in coherent receivers [3, 4]. In NC systems, the use of MFs not only increases synchronization time, but make the system very sensitive to errors in estimating SNR. Repetition codes can simplify algorithms by eliminating the need for MFs, but require parallel or sliding integrators in addition to higher SNR or on-time [5]. Synchronization accuracy is also limited by clock speeds with these techniques, as a ±1ns resolution (corresponding to 30cm of positioning accuracy) typically requires a 500MHz clock.

The proposed digital baseband overcomes these shortcomings without any increase in RF front end power or complexity via the following techniques: 1) new synchronization codes that require 11× fewer samples than repetition codes, and which allow high synchronization accuracy (1ns) using slow clocks (32MHz); 2) a new quadratic correlation algorithm that requires 2 to 4dB lower SNR than MFs and is robust to parameter measurement uncertainties; 3) an algorithmic transformation that reduces computational complexity of correlations by up to 32×; and, 4) a low-voltage, highly-parallel VLSI implementation that offers low-latency synchronization. As a result of these techniques, the baseband achieves a peak synchronization accuracy of ±1ns at an SNR of 4dB within 16μs.

The packet structure is shown in Fig. 14.2.1. The preamble consists of repetitions of a PN code ($S_0$) followed by a start-frame-delimiter (SFD), header, and payload bits. State-of-the-art codes for NC systems, as proposed in the IEEE 802.15.4a standard [6], are not necessarily alias-free, i.e. two chip period shifts of $S_0$ produce an identical sequence of integrator outputs. Figure 14.2.1 demonstrates this with a toy, 4a-like code. To guarantee no aliasing, the receiver must be able to shift integration slots by a chip period of 1.95ns (or 8×). Since $n$ may be as large as 32, the 8 QCORR units in a PCT perform up to 4 sets of correlations. After all computations are complete, the inferred phase is conveyed to the RF front-end using a DLL, and the inferred shift is used to skip the right number of samples to achieve codeword alignment. Detection is treated like synchronization except that it is sufficient to use only 2 out of 16 PCTs. Custom, fine-grain, clock gating is employed during detection to reduce clock tree power of the unused PCTs. Overall, clock gating reduces dynamic power by 2.7× during idle mode.

The repeated $S_0$ codes are followed by the SFD ($S_0S_1S_1S_1S_0$) where $S_1$ is an all-zero code with the same length as $S_0$. The baseband searches for the SFD by correlating with all expected length 5 code sequences stored in a codebook. This is achieved via an inner quadratic correlation with $S_0$ and $S_1$, and an outer linear correlation that accumulates inner results for all sequences in the codebook. Inner results are stored in a serial shift register (Fig. 14.2.4). Two pairs of QCORRs are used in a time-interleaved fashion to avoid throughput loss or excessive buffering. The search continues until the SFD has the highest correlation, or a pre-specified timeout is reached. In the high SNR regime, the circuit can also be programmed to search for a length 1 SFD to reduce preamble duration.

Unlike conventionally used linear matched filters, the proposed quadratic correlation receiver achieves near-optimum performance, and is robust to SNR estimation errors. The baseband achieves a ±1ns synchronization accuracy with 10dB lower SNR, or, 11× shorter preambles, compared with repetition codes, and is within 1.5dB of the optimum ML receiver, as shown in Fig. 14.2.5. In the presence of SNR estimation errors, the baseband improves the ‘eye’ opening by 4dB compared with an ideal matched filter.

Implemented in 90nm CMOS, the digital baseband occupies 2.55mm² on an SoC with an integrated RF front end and 5b ADC [7]. The baseband operates at a core supply voltage as low as 0.55V. During detection and synchronization, the baseband dynamically duty-cycles the RF front end to reduce system power. At a clock frequency of 32MHz, the chip can process an entire preamble in a minimum of 14μs and consumes an average of 1.6mW. A summary of results is shown in Fig. 14.2.6. A die photo is shown in Fig. 14.2.7.

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References:
Figure 14.2.1: Non-coherent UWB block diagram, with illustrated packet structure and alias-free codes.

Figure 14.2.2: Digital baseband block diagram.

Figure 14.2.3: Phase-correlation tile with 8 QCORRs.

Figure 14.2.4: SFD and QCORR circuits.

Figure 14.2.5: Synchronization error rates (SERs) for ±1ns accuracy with ideal and mismatched SNRs.

Figure 14.2.6: Table of measured results and power profile.
Figure 14.2.7: Die micrograph of the IR-UWB digital baseband processor.