Guest Editorial for Special Issue on High-Performance Multichip Interconnections

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Guest Editorial for Special Issue on High-Performance Multichip Interconnections

This special issue on high-performance multichip interconnections illustrates a broad spectrum of challenges facing designers of high-speed communication circuits. Seeking to improve both the energy efficiency and throughput density of high-performance interconnects, designers have turned to the optimization of microcommunication systems across multiple design layers. The papers here represent this cross-layer approach and span novel transmitter and receiver equalization and data-recovery architectures, channel architecture organizations, comparisons with optical transmission techniques, advanced signal processing and coding concepts, and network optimization.

Kao and Liu present a 20-Gb/s adaptive transmitter preemphasis filter adjusted by detecting the propagation time through the channel, a technique that helps decouple the adaptation from transmitter/receiver collaboration on smooth channels with relatively high loss and low reflections. An adaptive receiver equalizer by Cheng et al. operates at 5 Gb/s and uses low-voltage zero generators to achieve high-frequency gain boosting without inductors, leveraging a spectrum-balancing technique and current-steering power detector circuits to adjust the equalization settings.

Amortizing the overhead of clock and data recovery in multiple parallel links, Nassar et al. introduce a new methodology for multichannel clock and data recovery, showing that the architecture can be reduced to an ensemble of weakly interacting delay-locked loops, asymptotically eliminating the jitter-peaking problem and allowing control of voltage-controlled oscillator jitter transfer to the recovered clock without affecting the data jitter transfer.

In order to improve overall link performance, channel redesign, where possible, also represents a powerful design knob. The papers by Lee et al. and Aryanfar and Amirkhaniy present advances in channel engineering for memory interfaces. The paper by Lee et al. optimizes reflection coefficients at branch junctions in a multislot memory system for post-DDR3 applications, creating an improved channel transfer function similar to that for point-to-point connections at rates up to 3.2 Gb/s. Ayanfar and Amirkhany introduce low-cost passive resonance mitigation techniques for multidrop memory channels, coupling transmission lines to prevent destructive signal resonance caused by reflections from capacitive loads and channel mismatches at rates up to 4 Gb/s.

Analyzing an alternative signaling medium, Palaniappan and Palermo compare various optical interconnect architectures for chip-to-chip applications. The brief considers the power efficiency of near-term vertical-cavity surface-emitting laser drivers and discrete photodetectors, as well as longer term single-mode integrated photonic solutions, promising to achieve data rates past 30 Gb/s/wavelength at energy efficiencies of 500 fJ/b in the 45-nm node. Han et al. present a 20-Gb/s transformer-based current-mode optical receiver with a common-gate transimpedance amplifier and a six-stage postamplifier. Employing source degeneration and interleaving active feedback techniques, they achieve 12.6-GHz bandwidth and flat-frequency response with a cumulative gain of 60 dBΩ.

In addition to these circuit- and channel-level design techniques, more advanced signal processing and coding methodologies can also help in eliminating channel artifacts and relaxing power/noise specifications for analog links. Namgoong presents receiver techniques that reconstruct the signal from a bank of low-frequency analog-to-digital converters operating on a frequency-channelized input signal. Using single-carrier cyclic-prefixed communication reduces the computational complexity in channels with moderate to large intersymbol interference. Narasimha and Shanbhag explore the utility of forward error correction (FEC) in shifting the power allocation from analog link blocks to a more scalable digital back end, trading off transmit swing, jitter, and receiver sensitivity for coding gain. The paper presents these tradeoffs using a scalable custom BCH decoder architecture, showing that FECs are on the brink of providing a net positive gain in high-speed link applications.

At the system level, the paper by Seiculescu et al. presents a comparative analysis of networks on chip (NOCs) for 2-D and 3-D integration, with multiple voltage and frequency islands. These emerging design techniques can provide relatively large energy-efficiency improvements but require careful design-space exploration at the NOC level.
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[10] C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, Comparative Analysis of NoCs for 2D vs 3D SoCs Supporting Multiple Voltage and Frequency Islands.

Vladimir M. Stojanovic (S’96–M’05) received the Dipl.Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2000 and 2005, respectively.

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