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A 0.6V 2.9µW Mixed-Signal Front-End for ECG Monitoring
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Abstract
This paper presents a mixed-signal ECG front-end that uses aggressive voltage scaling to maximize power-efficiency and facilitate integration with low-voltage DSPs. 50/60Hz interference is canceled using mixed-signal feedback, enabling ultra-low-voltage operation by reducing dynamic range requirements. Analog circuits are optimized for ultra-low-voltage, and a SAR ADC with a dual-DAC architecture eliminates the need for a power-hungry ADC buffer. Oversampling and ΔΣ-modulation leveraging near-Vth digital processing are used to achieve ultra-low-power operation without sacrificing noise performance and dynamic range. The fully-integrated front-end is implemented in a 0.18µm CMOS process and consumes 2.9µW from 0.6V.

Introduction
Symptoms of cardiovascular disease are often very intermittent, necessitating ultra-low-power wearable ECG monitors with long lifetimes. In order to minimize system power, digital signal processing (DSP) can accomplish feature extraction and data compression which reduces the power burden of data transmission or storage. Recent biomedical DSPs leverage voltage scaling (down to 0.5V) to improve energy-efficiency [1]. Additional size and power benefits can be obtained by integrating the analog front-end (AFE) with the DSP back-end [2]. However, current AFEs rely on high supply voltages [3, 4] to perform signal conditioning and accommodate aggressors like electrode offset (EO) and power-line interference (PLI), limiting their compatibility with low-voltage DSPs. Therefore, this paper presents a mixed-signal front-end (MSFE) that leverages a highly-digital architecture in order to operate from a 0.6V supply which improves power-efficiency through voltage scaling, and facilitates integration with low-voltage DSPs. This work focuses on the design of ultra-low-voltage front-end analog circuits aided by configurable and energy-efficient digital processing at near-Vth operation. A highly-integrated solution is presented to demonstrate feasibility of a 0.6V system.

System Description
Supply voltage scaling is an effective way to achieve linear and quadratic power reduction in analog and digital circuits respectively. However, for ECG acquisition, PLI can be a limiting factor for voltage scaling. For example, 5mVp-p of PLI with 40dB of front-end gain could easily saturate a sub-1V system before digitization by the ADC. Therefore, the system architecture in this work is based on [4], but uses ΔΣ-modulation to simultaneously achieve a larger PLI cancellation range and low-noise performance as a key enabler for ultra-low-voltage operation. The burden of signal processing is shifted to the digital domain which is suitable for low-voltage systems. Compared to [4], this work reduces the supply voltage from 1.5V to 0.6V and optimizes analog circuits for ultra-low-voltage operation.

Shown in Fig. 1, a low-noise amplifier (LNA) gains the input by 34.5dB, and ac-coupling achieves greater than ±300mV of EO rejection as required [5]. A sinc anti-aliasing filter (SAAF) provides an integrate-and-dump function at a sampling frequency of fs=10kHz, resulting in a sinc frequency response with notches placed at multiples of fs which are precisely in the center of the aliasing bands. At the end of each integration period, the signal is digitized by a 9b dual-DAC SAR ADC.

Low-Voltage Mixed-Signal Circuit Design
The LNA is fully-differential to maximize signal range, and uses passive feedback to accurately set gain and ensure good linearity at 0.6V. Although the CMRR is limited to 70dB by using passive feedback, the CMRR requirements are relaxed since the mixed-signal notch in this system filters out PLI. Switched-capacitor common-mode feedback (SC-CMFB) is used to avoid distortion from the CMFB loop with large signal swing at low voltage. Although SC-CMFB introduces spikes at the switching frequency of 10kHz, the SAFF in this system also acts as a spike reduction filter.

In addition to anti-aliasing and spike reduction, the SAFF shown in Fig. 2 also provides a gain of GS = GM/(2fSfINT) which is digitally tunable through GM and CINT. The SAFF uses negative feedback to implement a linear transconductor and avoids cascading in order to operate at 0.6V. CINT is the sum of a 4b switched-capacitor CD, and the sampling capacitance CS, of the SAR ADC whose block diagram is shown in

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*The authors acknowledge the funding support of Texas Instruments and the NSERC Fellowship.
D has features such as activity-based sampling, feature extraction, and signal integrity monitoring (power not included).

C Includes power and noise of LN A, BPF, and AD C.

Benef calculation based on 9.26µV rms input-referred noise integrated over 0.5Hz-50kHz, using a 2.93kHz 3dB bandwidth.

ω

Power of peripheral blocks

Single

Electrode offset tolerance

0 (IEC generator. The number of bits in the LUT is reduced by over 5 surprising a phase accumulator and a LUT as a phase to waveform

nusoids required for frequency translation are generated on-chip

when compared to [4] by storing only a quarter period and using

ADC full-scale is digitally tunable, providing up to 4.9dB of

a power-hungry ADC buffer which is usually needed to drive

the input capacitor of a conventional SAR ADC. Finally, the

ADC full-scale is digitally tunable, providing up to 4.9dB of

embedded gain.

Fig. 3 shows the block diagram of the programmable digital BPF based on [4], but optimized for area and integrated for

near-V operation. The BPF takes the form of a frequency-

translated accumulator, and its center frequency and width

are tunable through ω and G P L respectively. In this work, the

sincosoids required for frequency translation are generated on-chip

using a direct-digital synthesizer (DDS) with 9b outputs, com-
pared to a phase accumulator and a LUT as a phase to waveform
generator. The number of bits in the LUT is reduced by over 5

when compared to [4] by storing only a quarter period and using

the sine-phase difference technique [6], requiring only 4Kgates.
The cosine phase is generated by adding an offset of π/2 and

the LUT is used for both sine and cosine by time-multiplexing.

Fig. 3. Block diagram of the programmable digital BPF and DDS.

Fig. 4. Measured frequency response at the output of the SAAF.

Fig. 2. The ADC uses dual capacitive DACs, where switches S1

and S2 are complementary so that DAC1 and DAC2 alternate

between bit cycling and sampling so that only one of them adds

C 0 to during any given period. The interleaved dual-DAC

architecture effectively merges the ADC sampling capacitance

with the SAAF integrating capacitor, eliminating the need for

a power-hungry ADC buffer which is usually needed to drive

the input capacitance of a conventional SAR ADC. Finally, the

ADC full-scale is digitally tunable, providing up to 4.9dB of

embedded gain.

Fig. 3 shows the block diagram of the programmable digital

BPF based on [4], but optimized for area and integrated for

near-V operation. The BPF takes the form of a frequency-

translated accumulator, and its center frequency and width

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The cosine phase is generated by adding an offset of π/2 and

the LUT is used for both sine and cosine by time-multiplexing.

Measurement Results

A prototype was fabricated in a 0.18µm CMOS process. The

closed-loop frequency response of the SAAF output shown in

Fig. 4 demonstrates the digital programmability of the PLI

notch frequency and width. The total gain of the system can be

set between 34.5dB and 69.4dB by selecting one of the 60

SAAF and 4 ADC gain settings. At the lowest gain setting,

the MSFE can accommodate PLI up to 12.6mV

input, and (b) ECG, with the PLI notch off and on.

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