A +10dBm 2.4GHz Transmitter with sub-400pW Leakage and 43.7% System Efficiency

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Typically, high-\(V_T\) leakage reduction without affecting its on-performance. Increasing switch size will in turn increase leakage. Negative gate-biasing of the gating switch has been shown to give significant leakage reduction [3]. However, in this work, we study the effect of negative-gate biasing of the low-\(V_T\) active device itself, thereby eliminating a switch in the direct path of active current and simultaneously reducing leakage. This is especially useful for the PA in our work, which operates at +10dBm and is the largest active power consumer.

Fig. 13.7.1 shows the measured drain current (\(I_D,PA\)) and gate current (\(I_G,PA\)) of the NMOS PA transistor as a function of the negative gate bias applied. The 65nm CMOS transistor, because of its thin gate oxide, has significant gate leakage. It is exponential with the gate bias. The drain current, which is the sum of sub-threshold current and gate leakage, decreases exponentially with increasing gate bias while the sub-threshold current is dominant, but increases as gate leakage becomes larger. The red curve (in solid) shows the achievable total PA assuming the negative bias is supplied by an ideal \(-5\text{\,V}\) charge pump (\(I_{LEAK} = I_{DS,PA} - I_{GS,PA}\)). The minimum, 430\,\mu\text{A}, occurs at \(-200\text{\,mV}\) and represents a 30\times reduction in leakage. Fig. 13.7.1 also shows a histogram of the minimum (\(I_D,PA\)\(-\frac{1}{2}\)\(V_{TH,INV}\)) current for 25 measured chips. Simulations indicate that the minimum leakage points range from \(-150\text{\,mV}\) to \(-300\text{\,mV}\), which implies that a \(-\frac{1}{2}\)\(V_{TH,INV}\) charge pump generating \(V_{NEG} = -\frac{1}{2}\)\(V_{DD}\) is sufficient. Low VDD ensures device reliability even with \(V_{NEG}\) biasing (\(V_{VCC} - V_{NEG} < 1.2\text{\,V}\)).

Fig. 13.7.2 shows the complete TX system block diagram. The RF signal path has a 12MHz crystal oscillator feeding a divided 1MHz clock to an integer-N PLL. The PLL provides 2MHz-spaced BLE channels at 2.4GHz. The PLL output is then buffered onto a +10dBm power amplifier. The TX applies direct modulation to the VCO control voltage for 1Mps GFSK. A digital baseband, running at 6MHz, implements an SPI interface and BLE packet generation logic including CRC, data whitening, and Gaussian pulse shaping. A voltage doubler charge pump running at \(\approx 1.2\text{\,V}\) to enable high-Q RF capacitor banks for use in VCO frequency tuning and matching network tuning.

The TX also implements extensive power gating. The RF transistor in the PA uses negative gate biasing for leakage reduction without RF performance degradation. A 32Hz gate-leakage-based oscillator drives the \(-\frac{1}{2}\)\(V_{TH,INV}\) charge pump to generate \(V_{NEG}\). All other blocks have either a PMOS or NMOS thick-oxide high-\(V_T\) power switch. Simulations show that driving an NMOS power switch with \(V_{VDD}\) and \(V_{NEG}\) instead of \(V_{DD}\) and \(V_{SS}\) results in 10\times smaller voltage drop in active mode and 10\times lower sleep leakage. Similarly, PMOS power switches are turned on strongly enabling the low power consumption in spite of the slow rise times of \(V_{DD}\) and \(V_{SS}\).

Fig. 13.7.7 shows the die photo of the TX fabricated in a 65nm LP CMOS process. The die area is 2.5\times2.5\text{\,mm}^2 while the core area is 1.6\text{\,mm}^2. The crystal oscillator, PLL and VCO consume 32\,\mu\text{W}, 132\,\mu\text{W} and 510\,\mu\text{W} respectively. The VCO buffer consumes 102\,\mu\text{W} while the resonant buffer draws 1mW. The PA delivers a wide range of output power ranges from \(+10.9\text{\,dBm}\) to \(-5\text{\,dBm}\) depending on the supply voltage and bias voltage applied to it. Fig. 13.7.5 plots the overall TX efficiency for various \(V_{DD}\) values. At 0.68\,\text{\,V}, it generates an output power of \(+10.9\text{\,dBm}\) with a PA efficiency of 46.4\% and overall TX efficiency of 43.7\%. At a lower voltage of 0.25\,\text{\,V}, the PA has a peak efficiency of 47.2\% while delivering 2.6dBm with the TX efficiency at 31.6\%. Fig. 13.7.5 also plots the spectrum of 1Mbps GFSK modulation. The adjacent channel power is well below the BLE spec. The TX was able to successfully communicate with a commercial off-the-shelf BLE receiver from Texas Instruments.

Fig. 13.7.6 shows leakage measurements of the full TX. The pie chart breaks down the contribution of the various components with the PA being the dominant one. The total leakage power is around 370\,\mu\text{W}. Fig. 13.7.6 also shows the measurement of total TX leakage at various temperatures. This experiment was performed bypassing the gate leakage oscillator in order to characterize the true minimum power points. At high temperatures, the effectiveness of the leakage management techniques is better because the sub-threshold current at \(V_{NEG} = 0\text{\,V}\) is higher while the gate leakage is relatively constant with temperature. For example, at +80\,\text{\,C}, there is a 100\times reduction in leakage current at an optimal \(V_{NEG} = -300\text{\,mV}\).

In conclusion, a 2.4GHz BLE-compatible transmitter architecture for use in ultra-low duty cycle applications has been presented. Low voltage operation, extensive power gating and a negative gate biasing technique help in achieving a peak TX efficiency of 43.7\% at an output power of \(+10.9\text{\,dBm}\) while also reaching a leakage power of 370\,\mu\text{W}, for an on/off ratio of 7.6\times. The TX delivers a peak total TX efficiency of 43.7\% at 0.68\,\text{\,V}.

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References:
Figure 13.7.1: Measured drain and gate currents for the PA showing minimum leakage point and its distribution across 25 measured chips.

Figure 13.7.2: Block diagram of the transmitter showing RF signal chain, power gating switches and leakage management blocks.

Figure 13.7.3: RF signal chain from VCO to the antenna showing the VCO buffer running from \( V_{DOUB} \), the resonant buffer, the power amplifier and capacitor bank tuning.

Figure 13.7.4: Gate-leakage oscillator that provides the clock for the negative voltage charge pump that generates \( V_{NEG} \). All devices are thick-oxide devices except for the gate-leakage current sources.

Figure 13.7.5: RF performance of the transmitter showing overall transmit efficiency at various \( V_{DD,PA} \) values. Also shown is the 1Mbps GFSK spectrum from the transmitter.

Figure 13.7.6: Pie chart with the contribution of various blocks to system leakage and variation of the minimum leakage with temperature.
Figure 13.7.7: Die photo of the transmitter fabricated in 65nm LP CMOS. Die size is 2.5×2.5mm² and core area is 1.6mm².