GaN Electronics for High-Temperature Applications

by

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Abstract

Gallium nitride (GaN) is a promising candidate for harsh environment electronics, thanks to its excellent material properties, which have given rise to high performance (room-temperature) transistors for radio frequency (RF), power, micro-electromechanical systems (MEMS), and mixed-signal applications. Previous works on high temperature (HT) electronics have been typically limited to two aspects, namely, high temperature robustness of discrete transistors, and basic circuit building blocks, which are mainly combinational logic. While these studies offer strong indication of the potential of GaN transistor technology for HT applications, the development of HT (500 °C) GaN integrated circuits (ICs) is still at its early stage due to the low degree of complexity and integration demonstrated so far. Major challenges in the realization of GaN HT-robust sequential logic circuits or more complex systems is the lack of a scalable technology.

This thesis aims to advance the integration technology of GaN HT electronics by demonstrating a comprehensive HT (500°C) enhancement-mode (E-mode) GaN-on-Si technology from device to circuit perspectives: (1) a scalable device technology based on p-GaN-gate AlGaN/GaN high-electron-mobility transistors (HEMTs) with high uniformity, which is optimized for HT operation and demonstrated to offer robust performance at least up to 500 °C with the help of in-house developed packaging technology and characterization platform, (2) compact modeling of monolithically integrated enhancement/depletion-mode HEMTs up to 500 °C HEMTs, (3) robustness-driven circuit design based on GaN technology, (4) demonstration of GaN-based combinational and sequential building blocks including inverter, NAND, NOR, ring oscillators, read-only memory (ROM), static random-access memory (SRAM), D Latch, D Flip-Flop operational up to 500 °C.

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Chapter 1

Introduction

Emerging applications such as deep well drilling in both geothermal and petroleum industry, hypersonic aircrafts, and space exploration, require high temperature (HT, 500 °C)-rated electronics beyond the Si-on-insulator (SOI) technology's typical temperature limit of 300 °C. Traditionally, additional thermal management approaches, namely, active or passive cooling, are required to maintain the normal operation above the specified temperature range [19, 20]. These cooling methods introduces extra size, cost, power consumption, complexity, noise, and reliability issues. Thus, devices capable of direct high-temperature operation without external cooling are highly desirable to reduce the cost and improve system reliability.

1.1 Opportunities for High-Temperature Electronics

High-temperature electronics are commonly required in applications where high ambient temperature is present. Self-heating effects could also significantly increase the channel temperature of electronics and should be taken into account in systems with high power dissipation and dense packaging. In this section, several common high temperature applications and opportunities are illustrated below.

One of the major obstacles to the exploration of planet Venus is its high surface temperature ($\sim$ 460 °C), Despite the use of complex cooling systems, data transmission in this environment has only been demonstrated for a couple of hours before the complete failure of the silicon electronics [21], indicating the strong need for a more robust device technology in the future. High-temperature electronics are also critical in other aerospace applications. For example, it is desirable to put the monitor and control electronics close to the jet engine in order to reduce the complexity of interconnections [22]. In this situation, the ambient temperature can exceed 225 °C, and a new generation of HT electronics could improve the system efficiency and reliability.

The underhood temperature of traditional automotive could easily reach 140 °C either on the engine or in the transmission [23, 24]. The integration of power electronics with electric motors will increase the operating temperature above 200 °C. The proliferation of hybrid, fuel cell, and fully electric automobiles, it also drives incremental demand for higher temperature electronics.

Deep oil/gas extraction is one of the most traditional applications of high-temperature

electronics. The operating temperature of electronics used to in-situ monitor or control drilling operation increases with the underground depth of the well and could exceed 300 °C for deep wells with high pressure involved. In such applications, cooling systems are usually not efficient and quite complex, and therefore it is quite challenging to ensure the system reliability, which is critical considering the high cost of potential failures and delays. The development of high-temperature electronics would enable drilling deeper and avoid redundant cooling systems.

Geothermal energy is a key renewable energy resource in many regions. In 2015, it was reported that it produced 587,786 TJ of energy per year, with an annual growth rate of 6.8% [25]. The critical point of water occurs at 374 °C and 22. mPa, while the critical point of seawater is even higher at 407 °C and 29.8 mPa with salt dissolved [26]. An Iceland Deep Drilling Project (IDDP) study showed that a geothermal well producing supercritical fluid with a temperature over 400 °C would have one order of magnitude higher power-producing potential than a conventional geothermal well producing steam [27]. With the help of high-temperature electronics, it is possible to access hotter and deeper geothermal resources and further improve the power output of the existing geothermal fields.

1.2 Challenges for High-Temperature Electronics

Commercially available Si electronics based on silicon on insulator technology is limited to 300 °C maximum [22]. At temperatures above 300 °C, several fundamental

limitations of traditional semiconductors make Si-based device operation inherently impossible. Those limiting factors are well summarized by several review papers [19, 20, 22] in the past few decades and will be briefly discussed below. Furthermore, in addition to HT-robust device technology, operating electronics at HT (500 °C) also presents challenges in device integration, packaging, characterization methodology, and design techniques.

1.2.1 Increasing Intrinsic Carrier Density with Temperature

One of the most dominant physical limitations for high-temperature operation is the increasing number of thermally-generated electron and hole carriers, also known as intrinsic carriers, in the semiconductor crystal. Traditional semiconductor devices operate thanks to the careful control of the conductivity of different semiconductor regions through the introduction of free electron and hole carriers by intentionally doping impurities into designed regions. Typically, the concentration of free electrons or holes is roughly equal to the dopant concentration due to the small ionization energies and high activation ratios of the dopant impurities at room temperature. Depending on the specific device structure and design, the doping level might vary between 10^{13} cm^{-3} to 10^{18} cm^{-3}. Unfortunately, when the temperature increases, the concentration of intrinsic carriers (n_i in cm^{-3}), not related to thermal ionization of

dopants but to direct thermal generation, also increases exponentially, [28],

$$n_i = \sqrt{N_c N_v} \exp\left(-\frac{E_G}{2kT}\right) \tag{1.1}$$

where T is the temperature in Kelvin, k is the Boltzmann constant (8.62×10^{-5} eV/K), E_G is the energy bandgap in eV, N_C and N_V are, respectively, the effective density of states of the conduction/valence band in cm^{-3} and they both have a weaker temperature dependence [28],

$$N_C = 2\left(\frac{2\pi m^*_{de} kT}{h^2}\right)^{3/2} \tag{1.2}$$

$$N_V = 2\left(\frac{2\pi m^*_{dh} kT}{h^2}\right)^{3/2} \tag{1.3}$$

where h is the Planck constant (4.14×10^{-15} eV·s), m^*_{de} and m^*_{dh} are the density of state effective mass for electrons and holes in $\text{eV}\cdot\text{s}^2/\text{cm}^2$. Notice that, both m^*_{de} and m^*_{dh} are not quite constant in temperature but much less dominant because N_C and N_V do not exactly follow $T^{3/2}$.

Intrinsic carrier concentrations from different materials are shown in Fig. 1-1. For standard Si devices working at room temperature, the n_i around 10^{10} cm^{-3} is negligible compared to the doping levels typically used in device engineering. When the temperature increases well beyond 300 °C, the device will gradually move to the intrinsic region where intrinsic carriers become dominant, and p-n junction becomes irrelevant. Wide bandgap materials have much lower intrinsic carrier concentrations

with much wider bandgaps (> 3 eV) than silicon for a given temperature, as seen from Fig. 1-1.

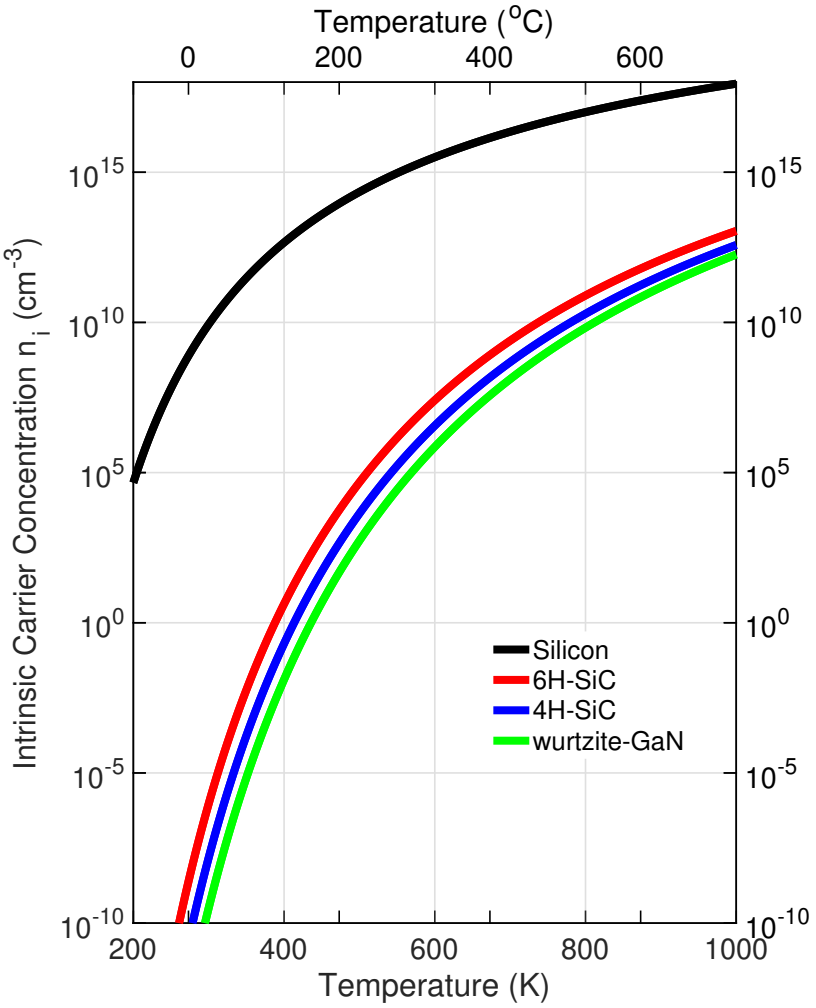


Figure 1-1: Semiconductor intrinsic carrier concentration (n_i) versus temperature for silicon, 6H-SiC, 4H-SiC and wurtzite GaN which has a weaker polytype dependence.

it should be noted that, unlike conventional dopants in Si devices where the very shallow donors and acceptors show almost 100% activation ratio at room temperature, the large ionization energy of Mg in GaN, a common p-type dopant, make Mg

activation typically incomplete at room temperature with a typical activation ratio of 1–2 % [29]. During the high temperature operation, the further activation of p-type dopant in the GaN devices will introduce a significant temperature variation of Fermi-levels, and thus cause extra variation in device performance.

1.2.2 Increasing Junction Leakage with Temperature

Junctions, such as p-n junction, Schottky junction, are the fundamental components of almost all the semiconductors devices, like diodes and transistors. All these devices strongly rely on the rectifying property of junctions for regular operation. The ideal current-voltage (I-V) characteristics of a common p-n diode structure with a "long" diode assumption can be modeled approximately as [28],

$$\begin{aligned} J &= (J_{es} + J_{hs}) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \\ &= qn_i^2 \left(\frac{1}{N_A}\sqrt{\frac{D_e}{\tau_e}} + \frac{1}{N_D}\sqrt{\frac{D_h}{\tau_h}} \right) \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \end{aligned} \tag{1.4}$$

where J_{es} and J_{hs} are, respectively, the saturation currents of electrons and holes, V is the bias voltage applied, N_A and N_D are acceptor and donor concentrations, D_e and τ_e are diffusion coefficient and minority carrier lifetime for electrons in the p-doped region and vice versa.

When space charge generation and recombination are taken into account, the upper limit of space charge region (SCR) current in the p-n diode can be computed

by assuming that the maximum recombination rate applies everywhere [28],

$$J_{SCR,max} = \frac{qn_i x_{SCR}}{2\sqrt{\tau_{eo}\tau_{ho}}} \left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \tag{1.5}$$

where x_{SCR} is the width of space charge region (depletion region), τ_{eo} and τ_{ho} are constants scaling inversely with trap concentration. And the total current of p-n diode is the sum of Eq. (1.4) and (1.5).

Other than the p-n junction, another important junction structure is the metal-semiconductor junction, also known as the Schottky junction. A Schottky diode is a majority-carrier device as opposed to the p-n diode driven by minority carrier injection. The I-V characteristics could be described by a thermal emission model in which the current is limited by the electron emission process over the tip of the energy barrier at metal-semiconductor interface [28],

$$J = A^* T^2 \exp\left(\frac{-q\varphi_B}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{1.6}$$

where A^* is Richardson constant, and φ_B is the effective barrier height between metal and semiconductor.

From Eq. (1.4)-(1.5), we see a strong relationship between reverse saturation current and intrinsic carrier concentration n_i, which means that the leakage current will increase exponentially with temperature and greatly influence the normal operation of devices with such structure. As a consequence of low energy bandgap and high

intrinsic carrier concentration, the increase of junction leakage currents of traditional semiconductors will further degrade device performance.

From Eq. (1.6), it is known that, the leakage current could be kept relatively low by increasing junction barrier height, which is more feasible with wide bandgap materials. Again, thanks to their wider bandgaps and lower intrinsic carrier concentrations, wide bandgap materials are considered to be promising candidates for high-temperature operation over 300 °C.

1.2.3 Decreasing Carrier Mobility with Temperature

Sheet resistance is one of the dominant components of device on-resistance and scales inversely with carrier mobility. For a non-zero temperature, the atoms in the lattice of a semiconductor vibrate around their equilibrium positions. The vibration is usually modeled through phonons to simplify the energy-exchange process between lattice and electrons. The interaction between phonons and electrons is known as phonon (lattice) scattering. At higher temperature, phonon scattering is the dominant scattering mechanism over ionized impurity scattering, which dominates at low temperature. When the temperature increases, the phonon scattering tends to increase with more phonons generated, leading to lower mobility for both traditional semiconductors and wide bandgap materials as shown in Fig. 1-2 [30, 31, 32].

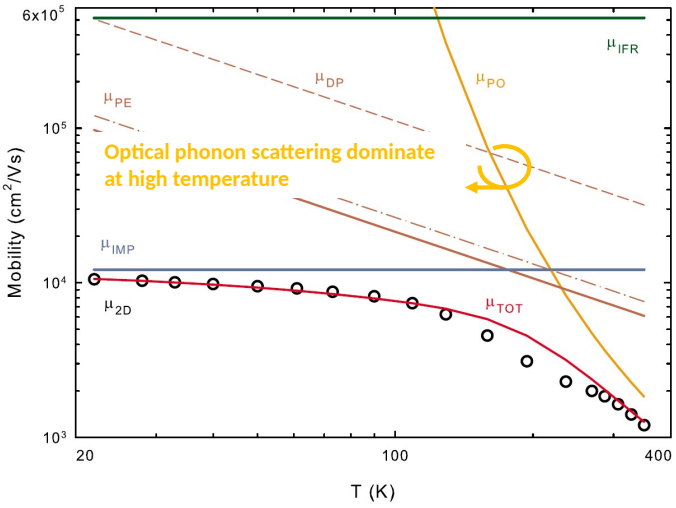


Figure 1-2: Scattering analysis of temperature dependent mobility of the 2DEG carrier in AlGaN/GaN HEMTs over temperature, namely, polar optical phonon scattering (PO), acoustic phonon scattering (AC, including deformation potential scattering (DP), and piezoelectric scattering (PE)), impurity scattering (IMP), interface roughness scattering (IFR) [1].

1.2.4 Other Issues

In addition to all the carrier-related issues discussed in the previous sections, semiconductor devices operating at high temperatures also suffer from problems with the extrinsic parts of the devices, such as ohmic degradation and accelerated dielectric breakdown [33, 34]. Those issues lead to a early failure well before the failure resulted from increasing intrinsic carrier concentration. While the initial results of time-dependent dielectric-breakdown (TDDB) measurement up to 375 °C indicates good reliability of dielectric in 4H-SiC (one of the major SiC polytypes) MOS capacitor, the reliability of the same dielectric in MOSFET is significantly poorer due to the additional process steps [35]. Furthermore, the TDDB measurement was also performed in GaN MISHEMTs up to 150 °C [36]. They offer little indication of dielec-

tric stability up to 500 °C. Therefore, it is preferable to use device structure without dielectrics such as JFETs, MESFETs.

The development of high-temperature electronics is not only a problem at the device level which could be solved right away by choosing proper semiconductor materials and structures, but a system problem involving growth, fabrication, packaging techniques, device models of a wide temperature range for circuit design, and reliability evaluation.

1.3 Wide Bandgap Materials for High-Temperature Applications

As discussed above, wide bandgap materials show fundamental advantages over standard semiconductors such as Si and GaAs for high-temperature operation. Silicon Carbide (SiC), III-Nitride (III-N), Gallium Oxide (Ga_2O_3), Diamond are the most common wide bandgap materials [19, 20, 22, 37, 38, 39]. Some of the key properties of SiC and GaN compared to that of Si are shown in Fig. 1-3 [40, 41]. Due to the difficulty in crystal growth, low material quality, lack of process technology, and difficulty in make both high performance n- and p-channel transistors, Ga_2O_3- and Diamond-based devices are significantly less mature than SiC and III-Nitrides and will not be considered in this thesis.

1.3.1 GaN *vs.* SiC

SiC has been considered a promising candidate for high temperature electronics for the last couple of decades and it has been studied for this application by a number of groups [3, 15, 16, 14, 42, 43] because SiC has a slightly better thermal conductivity than GaN although it drops quickly with temperature. Its material quality is excellent, with very low or even zero micropipe density [44], which is good for device operation and to improve the yield for both large area and vertical devices. 4-inch SiC wafers have been commercialized more than a decade ago, and 6-inch SiC wafers are now also available in the market, while 8-inch SiC wafers are in research and development (R&D) by several companies. There are currently several kinds of SiC diodes and switches available [45, 46], including SiC Schottky diode, junction barrier Schottky (JBS) diode, PIN diode, junction FET (JFET) and metal-oxide-semiconductor FET (MOSFET). SiC-based HT ICs have been demonstrated in different device structures, such as JFETs ($>$ 500 °C) [42], BJTs (500 °C) [3], CMOS (400 °C) [15], MESFET (300 °C) [43]. The SiC JFETs reported by NASA Glenn Research Center is by far the most mature technology platform with high operating temperature (up to $\sim$ 1000 °C) and excellent reliability. The stable operation of 6H-SiC and 4H-SiC (two major SiC polytypes) JFETs and ICs at 500 °C over a year was reported in 2008 [47] and 2018 [42]. However, they typically require complicated power supplies, and are lower in switching speed. For example, SiC JFETs ICs are constructed using resistor-transistor-logic, due to the lack of normally-off transistor

technology, requiring a V_{DD} of +25 V, and V_{SS} of −25 V. It is also challenging for SiC JFETs ICs to achieve a high level of complexity and device density integration, resulting from the nature of resistor-transistor logic (RTL).

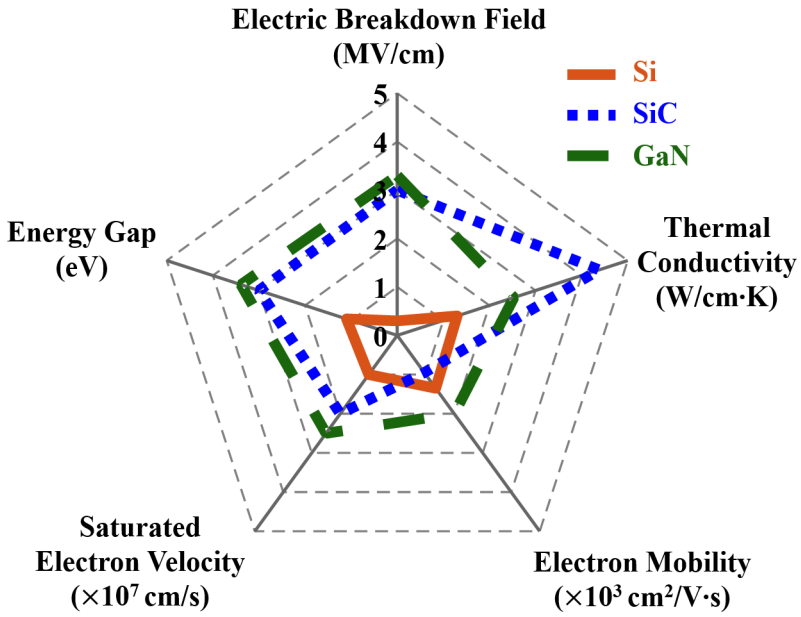


Figure 1-3: Materials properties of Si, SiC and GaN.

Meanwhile, Gallium Nitride is first known as a wide bandgap material for high brightness blue light-emitting diode (LED). Due to its high critical electric field, it then became a promising candidate for electrical devices as well [48]. As shown in Fig. 1-3, both SiC and GaN show better performance than Si, GaN still has a higher breakdown electrical field than SiC. Besides, the polarization nature of GaN [40] enables AlGaN/GaN high electron mobility transistors (HEMTs) by forming a high-quality two-dimensional electron gas (2DEG) at the AlGaN/GaN interface, providing an order of magnitude higher mobility.

Most common AlGaN/GaN HEMTs are grown along the Ga-face with the wurtzite crystal structure, which is inherently non-centrosymmetric. The intrinsic asymmetry of wurtzite lattice and difference of spontaneous polarization between AlGaN and GaN lead to a net spontaneous polarization charge in the AlGaN/GaN interface, as shown in Fig. 1-4. Besides, AlN is known to have a smaller lattice constant than GaN and the same for AlGaN, which could be approximated by linear interpolation between lattice constants of AlN and GaN [49]. Thus, the AlGaN layer grown on the GaN channel is typically under tensile stress, and a piezoelectric polarization charge is then induced by such mechanical stress inside the AlGaN layer, while there is no piezoelectric polarization present from the relaxed GaN channel due to the lack of strain. The piezoelectric polarization induced by tensile stress in AlGaN is parallel to the spontaneous polarization, which means that both of them have negative signs along the axis [0001], as shown in Fig. 1-4. The net charge in the interface is then the sum of charges induced by both spontaneous polarizations from AlGaN and GaN and piezoelectric polarization from AlGaN [18],

$$\sigma = \left(P_{SP,GaN} - P_{SP,Al_xGa_{(1-x)}N}\right) - P_{PZ,Al_xGa_{(1-x)}N} \tag{1.7}$$

where σ is the net polarization charge in the interface, x is the Al composition, P_{SP} and P_{PZ} are spontaneous and piezoelectric polarization, respectively. By substituting

the parameters in Table 1.1 and linear interpolation,

$$\sigma = \left(P_{SP,GaN} - P_{SP,Al_xGa_{(1-x)}N}\right) - P_{PZ,Al_xGa_{(1-x)}N}$$

$$= \left[P_{SP,GaN} - (1-x)\,P_{SP,GaN} - xP_{SP,AlN}\right] - 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{1.8}$$

$$= \left\{5.2x - 2\frac{0.077x}{3.189 - 0.077x}\left[-11x - 49 - (73x+73)\,\frac{5x+103}{-32x+405}\right]\right\} \times 10^{-6}\ \mathrm{C/cm^2} \tag{1.9}$$

$$\approx \left[5.2x + \left(3.32x + 1.65x^2\right)\right] \times 10^{-6}\ \mathrm{C/cm^2} \tag{1.10}$$

where a_0 is the lattice constant of AlGaN in the thermal equilibrium, a is the lattice constant of the AlGaN grown on the GaN channel which in this case is equal to the equilibrium lattice constant of GaN, e_{31} and e_{33} are piezoelectric coefficients, C_{13} and C_{33} are elastic constants. All the $Al_xGa_{1-x}N$ parameters above are approximated by linear interpolation. Considering x is in the range of $[0, 1]$, Eq. (1.9) could be simplified to Eq. (1.10) by using linear approximation (first-degree Taylor Polynomial). With an assumption of $x = 0.2$ in this case, the net polarization charge is positive, which means there will be the same amount of free electrons in the AlGaN/GaN interface to compensate the fixed polarization charge, and the charge density σ/q is around 1.1×10^{13} $\mathrm{cm^{-2}}$. This polarization-induced 2DEG shows high drift velocity and high electron mobility, which, when combined with the high critical electric field of wide bandgap materials, make GaN transistors ideal for high voltage and low on-resistance applications.

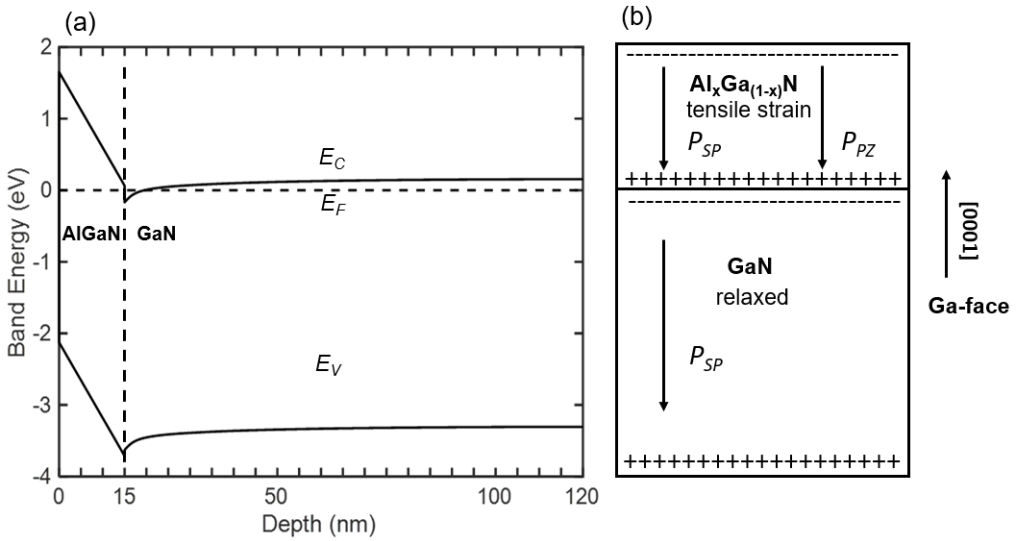


Figure 1-4: (a) Band diagram of the most common Ga-face AlGaN/GaN heterostructure; (b) Directions of spontaneous and piezoelectric polarization in the same structure.

Table 1.1: Spontaneous and piezoelectric parameters of AlN and GaN [18].

Parameters	P_{SP} $[C/cm^2]$	a_0 [Å]	e_{31} $[C/cm^2]$	e_{33} $[C/cm^2]$	C_{13} [GPa]	C_{33} [GPa]
GaN	-2.9×10^{-6}	3.189	-49×10^{-6}	73×10^{-6}	103	405
AlN	-8.1×10^{-6}	3.112	-60×10^{-6}	146×10^{-6}	108	373

GaN is mostly grown on SiC, sapphire, and silicon substrates. Among all those possible substrate materials, Si is the most attractive choice due to its large wafer diameter (8-inch and beyond) and lower cost compared to other candidates. However, due to the large mismatch in lattice constants and coefficients of thermal expansion (CTEs) between GaN and Si (111) substrate, it is quite challenging to grow high-quality GaN buffers on large Si substrates. 650 V GaN-on-Si enhancement-mode devices in a 200 mm CMOS fab were demonstrated by IMEC in 2015 [50, 51]. Mean-

while, 750 V fully vertical GaN-on-Si power diodes were reported by MIT in 2018 [52], which shows the potential and possibility of fully vertical GaN devices. Recently, p-channel GaN transistors were also successfully demonstrated with the capability of integration with n-channel e-mode GaN HEMTs on the same chip [53, 54, 55, 56, 57]. Stable operation of GaN-based devices up to 1000 °C was also reported [58, 59]. Meanwhile, high temperature operation of GaN-based ICs was reported by Hassan *et al.* [60] with the highest reported operating temperature for a D Flip-Flop of up to 160 °C based on the depletion-mode resistor-load-logic.

While SiC HT digital circuits based on several transistor types have been proposed [14, 15, 3, 16], its operating frequency is typically 10–100× lower than GaN-based devices. Moreover, most of the SiC-based circuits are implemented by resistor-transistor-logic (RTL) [42, 61], which is known to have low speed, large area overhead, complex power supply system with limited voltage swing, and noise margin. GaN and III-N materials offer significant advantages in a *wider* range of applications from power [62] and RF [6, 63, 64], to MEMS [65, 66, 67] and digital circuits [55, 8] across a large range of temperatures (from deep cryogenic temperature of 4 K to HT $>$ 1000 °C).

Given the rapid development of GaN technology in recent years and the intrinsic properties mentioned above, GaN could be an important enabler in the field of high-temperature electronics, especially on high frequency applications.

1.4 Challenges of GaN and Scope of Thesis

Despite the excellent performance shown by early high-temperature prototypes [68, 69, 58], several issues in traditional lateral AlGaN/GaN HEMTs could cause early degradation and failure under high-temperature operation (500 °C), namely, dielectric breakdown for GaN MISFETs, surface leakage current, temperature variation in device parameters, buffer leakage current, increased diffusion of dopants and ohmic contacts, degradation of heterostructure due to the mismatch of CTE, decreased stability of conductors and insulators. Moreover, the development of high temperature GaN-based electronics is a complex problem also involving compact modeling, high temperature specific circuit design and simulation, integration, packaging, and reliability evaluation.

This thesis aims to solve the problems mentioned above and demonstrates a comprehensive GaN high temperature technology, which spans from device to circuits. The main contributions are divided in the following 3 chapters:

- **Chapter 2**: A scalable GaN high temperature device technology with stable performance over 20 days at 500 °C;

- **Chapter 3**: Compact modeling and robustness-driven circuit design based on the proposed device technology up to 500 °C;

- **Chapter 4**: Key building blocks based on the GaN device technology in chapter 2 towards complex GaN ICs including inverter (500 °C), ring oscillator (500 °C),

memory (300 °C).

- **Chapter 5**: Design of GaN computer and failure analysis.

Chapter 2 demonstrates a self-aligned gate-first technology based on the E-mode p-GaN/AlGaN/GaN wafer platform. This technology incorporates refractory metal gate and etch-stop process. The physics behind the high temperature degradation of I_{on}, I_{off}, I_G, and V_{TH}, will be studied and explained. Uniformity and yield will be evaluated, and the process will be extended with aggressive channel length scaling to explore the ultimate potential of our device technology. To test the transistors, this work demonstrates an in-house packaging technology and measurement platform up to 500 °C. Device performance will then be evaluated by both in-situ and ex-situ measurements.

Chapter 3 focuses on the compact modeling of the proposed HT device technology. Different logic families and configurations will be evaluated and compared. Circuit design will be conducted prioritizing the high temperature robustness and tolerance on device parameters.

Chapter 4 presents a systematic study of GaN for high temperature (HT, up to 500 °C) digital circuits based on the reported high temperature platform, including inverters with different configurations, ring oscillators, SRAM, ROM, D Latch, and D Flip-Flop up to 500 °C with monolithic integration over 350 transistors. The performance will be evaluated and benchmarked with other GaN implementations and SiC devices.

Chapter 5 presents the design of GaN one-instruction-set computer (OISC) with over 1110 transistors based on the proposed simulation platform. On-chip instruction memory, data memory, and buffer were implemented with ROM, SRAM, and D-latch demonstrated in the previous chapter. The simulation results matched the expected outputs, indicating the proper electrical behavior and thus feasibility of GaN computer. However, the first generation of the GaN OISC, fabricated using the proposed process flow, failed to operate. The potential issues leading to the GaN OISC failure were analyzed and discussed, which may be mainly attributed to the IR drop on the power distribution network. The simulation results reflect the feasibility of GaN computer and the experiment results point out the direction for future optimization towards the integration of GaN transistors with higher complexity.

Chapter 2

High Temperature GaN Device Technology

2.1 Introduction

Traditional GaN HEMTs are depletion-mode (D-mode, i.e. normally-on) devices. However, for GaN digital circuits, an Enhancement-mode (E-mode) transistor is highly desired to avoid the need of an additional negative voltage power supply (V_{SS}) [60] and simplify the circuit design. This E-mode transistor could be realized using a number of technology options as shown in the Fig. 2-1, including, (1) F-plasma treatment of gate region [7]; (2) recessed MIS gate [70]; (3) tuning the fin width of FinFETs [71]; (4) p-GaN gate [9].

Among these, the p-GaN-gate is especially interesting for HT robust operation

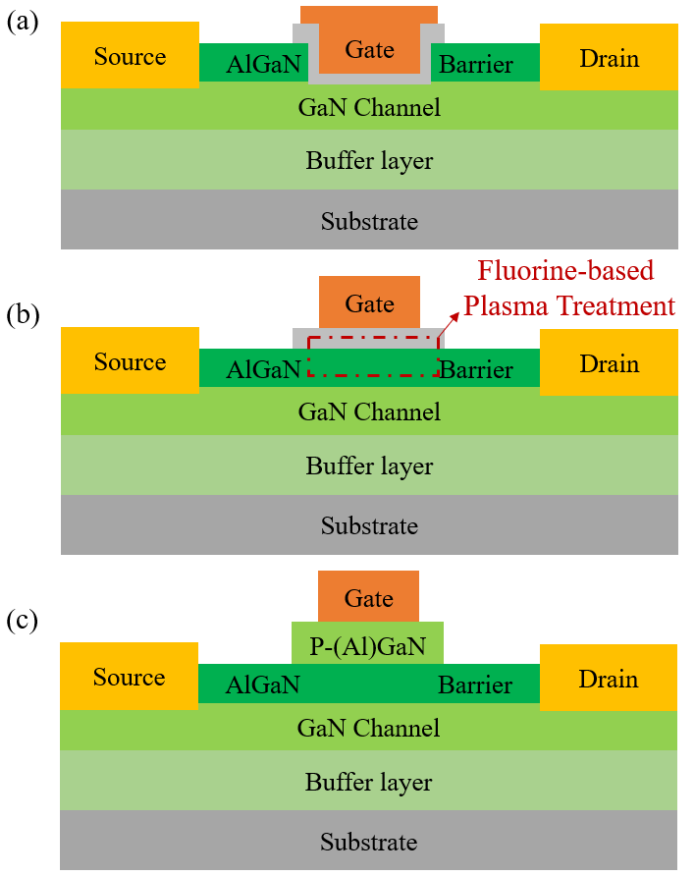


Figure 2-1: Illustration of the E-mode transistor with different implementations, namely (a) gate-recess AlGaN/GaN MIS-HEMTs, (b) AlGaN/GaN MIS-HEMTs using fluorine-plasma based treatment, (c) p-(Al)GaN-gate AlGaN/GaN HEMTs.

thanks to the lack of gate dielectric, and could introduce traps at the dielectric/semiconductor interface, and simplicity in process flow. Furthermore, at the technology platform level, the p-GaN-gate AlGaN/GaN HEMT offers the possibility of monolithic integration with both depletion-mode (D-mode) n-FETs and E-mode p-FETs. As compared to emerging p-FETs, E/D-mode n-FET-only logic is still the preferable choice for high temperature applications thanks to its high operating frequency, inherently matched temperature behaviors, low drive/load ratio, lack of dielectrics, and process

simplicity.

In this chapter, a comprehensive GaN high temperature (HT) technology from device- to circuit-level is presented. A self-aligned gate-first process flow with an etch-stop process and tungsten gate was demonstrated based on the p-GaN/AlGaN/GaN-on-Si platform. The proposed monolithically integrated E/D-mode transistors show stable operation up to 500 °C. The temperature dependent device parameters were systematically studied using device physics models. Furthermore, the uniformity and yield of the proposed technology were evaluated with the optimized etch stop process. Aggressive channel length scaling was then performed to explore the ultimate potential of our HT device technology.

2.2 Device Fabrication

The schematic of a monolithically integrated E/D-mode GaN HEMTs is depicted in Fig. 2-2. The epitaxial structure used in this work was grown on a 6 inch Si (111) substrate using metal organic chemical vapor deposition (MOCVD), comprising an 70-nm p-GaN layer with a Mg doping concentration of 3×10^{19} cm^{-3}, a 15 nm AlGaN barrier, a 150 nm UID-GaN channel, and a proprietary III-Nitride buffer. The activation of p-GaN is performed in the MOCVD chamber after the growth in N_2 atmosphere.

The self-aligned gate-first process started with the blank sputtering of 100 nm tungsten (W). Next, W, as E-mode gate metal, was patterned and dry etched by

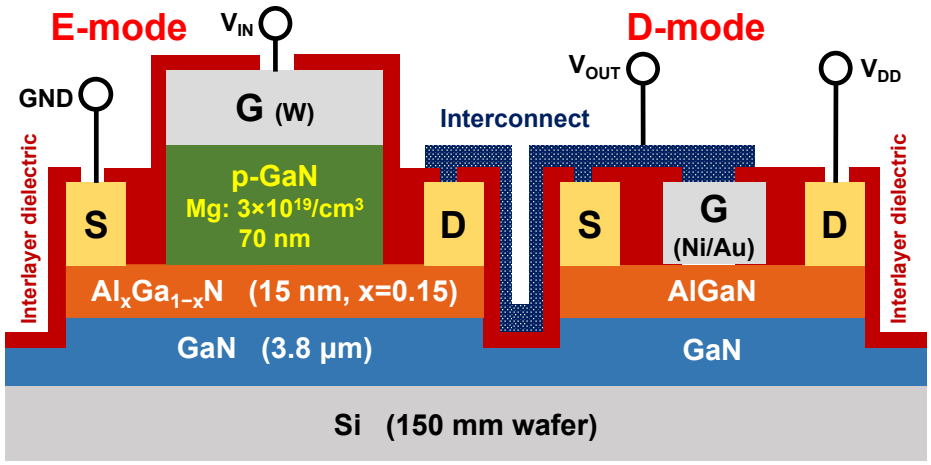


Figure 2-2: Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter.

SF_6/O_2 plasma using a Reactive-Ion Etching (RIE) system. With the same resist mask for W etch, the selective etch of p-GaN over AlGaN was then achieved using BCl_3/SF_6 plasma in the same chamber. W was chosen for (1) its excellent thermal stability as a refractory metal, as it had to stand the high temperature anneal process needed for ohmic contact formation [72], and (2) Schottky behavior with p-GaN gate [73]. The proposed self-aligned gate-first process simplifies the process with good potential for further gate length scaling, and reduces the hysteresis and trapping issues by preserving the as-grown p-GaN surface.

Next, a Ti (20 nm)/Al (100 nm)/Ni (25 nm)/ Au(50 nm) ohmic contact was deposited and patterned by a lift-off process. The similar ohmic contact scheme was used for InAlN/GaN lattice-matched transistors with stable operation up to 1000 °C [6]. An ohmic contact to the 2-DEG was then formed by annealing the metal stack at 800°C in N_2 ambient for 30 s, following with a mesa etch by Cl_2/BCl_3-based

Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) using photo-resist mask to define the active region of both E/D-mode HEMTs. The specific contact resistance was measured to be 0.46 Ω·mm. Afterward, a Ni (30 nm)/Au (200 nm) metalization was patterned and deposited by a lift-off process to act as both D-mode Schottky gate and the first layer of interconnect. Subsequently, the SiO_2 insulation layer was formed by tetraethoxysilane (TEOS) and opened through a via mask over the transistor electrodes. The fabrication was finished by a Ti (20 nm)/Au (300 nm) contact pad deposition, which also serves as the second layer of interconnect. It worth mentioning that, a further study is still required to choose the insulator with matched coefficient of thermal expansion to reduce the potential mechanical stress at elevated temperature.

Fig. 2-3 shows the cross-sectional image of the fabricated E-mode transistor. The sheet resistance of the AlGaN/GaN channel is 460 Ω/□. Both E/D-mode transistors share the same $L_G = L_{GD} = L_{GS} = 2$ µm with a minimum $W_D/W_E = 6/18$ µm/µm, yielding a drive/load ratio $\beta = (W/L)_{\mathrm{E}}/(W/L)_{\mathrm{D}} = 3$.

2.3 Device Characteristics from Room Temperature to 500 °C

The dc output and transfer characteristics of monolithically integrated E/D-mode HEMTs are shown in Fig. 2-4(a)–(d). Both E/D-mode devices have a gate width of $W_G = 100$ μm. At room temperature, the threshold voltage V_{TH} is +1.4 V for

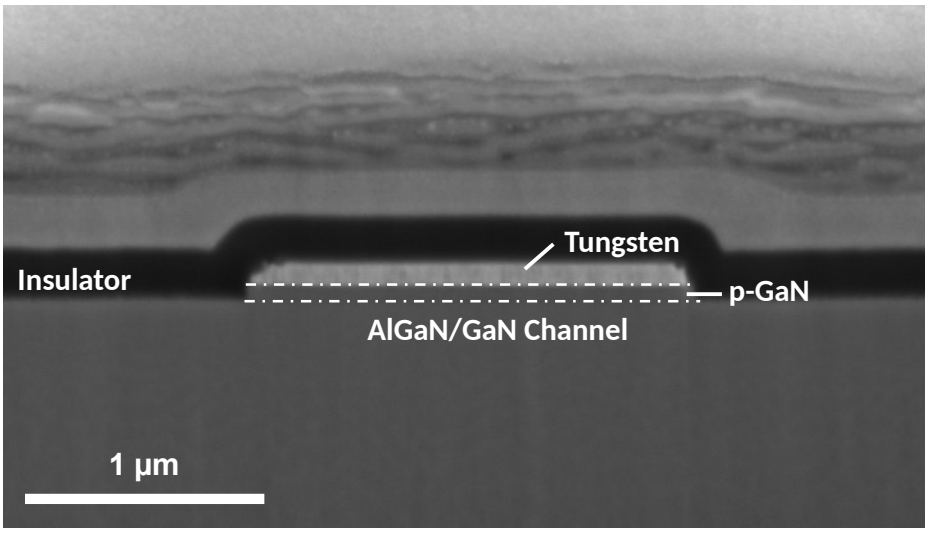


Figure 2-3: TEM of a fabricated E-mode transistor. Good self-alignment of the metal gate with p-GaN gate was achieved.

the E-mode HEMT and −1 V for the D-nmode HEMT by linear extrapolation. The maximum drain current of $I_{DS} = 270$ mA/mm (at $V_{GS} = 5$ V) and $R_{on} = 9.0$ Ω·mm for the E-mode HEMT, and $I_{DS} = 332$ mA/mm (at $V_{GS} = 1$ V) and $R_{on} = 5.1$ Ω·mm for the D-mode HEMT. Both E/D-mode devices show near-ideal subthreshold swings (SS) of 75 mV/dec and 73 mV/dec, respectively.

2.3.1 On- and Off-Current

Fig. 2-4(a) plots the transfer characteristics of a E-mode device over temperature. At 500 °C, the maximum drain current dropped to 15% compared to its value at room temperature. The reduction of on-current can be attributed to the decreased mobility as illustrated in Fig. 1-2, which is dominated by the optical phonon scattering [1]. The increase of off-current is due to the increased gate leakage current at higher

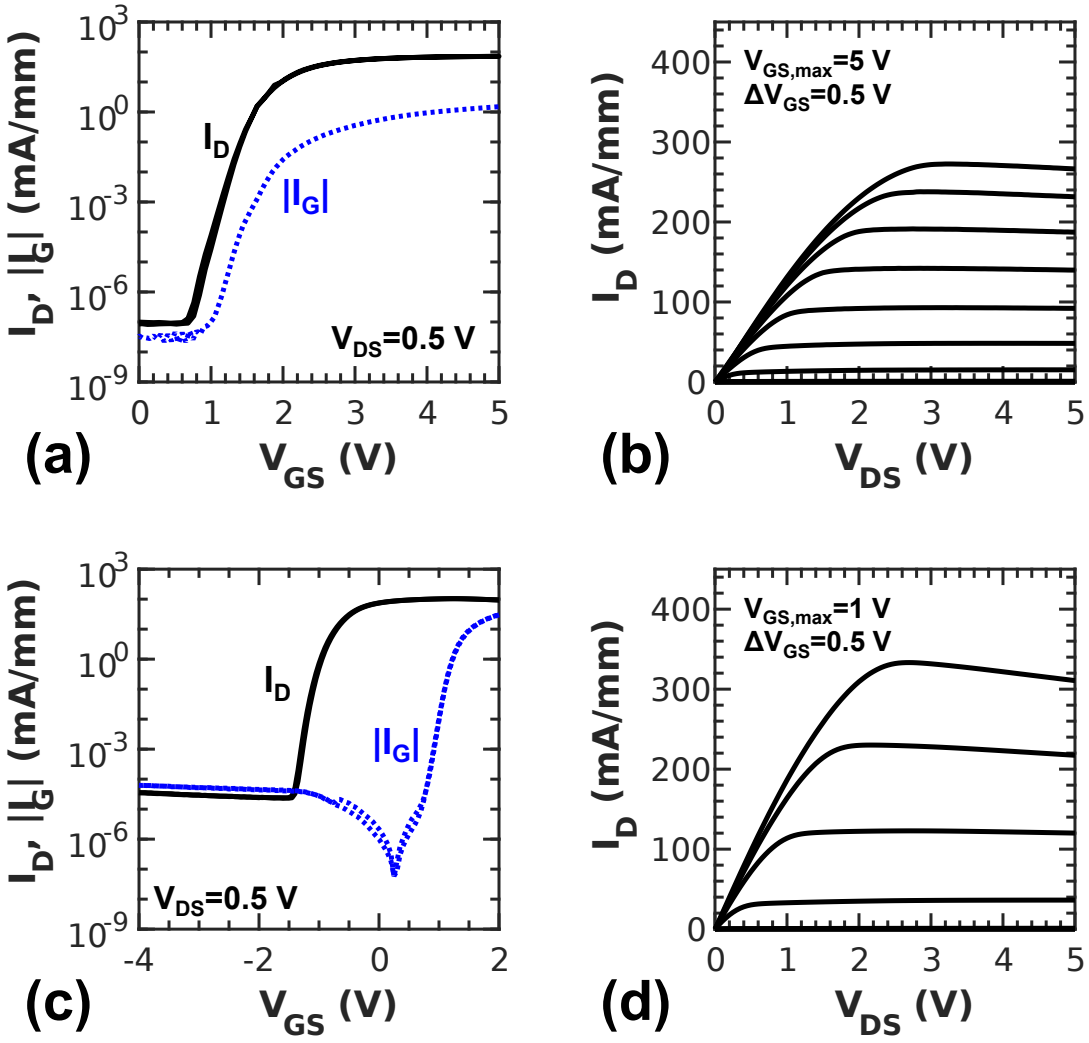


Figure 2-4: Characteristics of typical E-mode transistors (p-GaN gate AlGaN/GaN HEMTs) and D-mode transistors (conventional AlGaN/GaN HEMTs) fabricated on the p-GaN/AlGaN/GaN platform. (a) Transfer characteristics of an E-mode transistor, V_{TH} = 1.4 V, $I_{\text{ON}}/I_{\text{OFF}} > 10^8$, SS = 75 mV/dec. (b) Output characteristics of an E-mode transistor, $I_{D,max}$ = 270 mA/mm, R_{ON} = 9.0 Ω·mm. (c) Transfer characteristics of a D-mode transistor, V_{TH} = −1 V, $I_{\text{ON}}/I_{\text{OFF}} > 10^6$, SS = 73 mV/dec. (d) Output characteristics of a D-mode transistor, $I_{D,max}$ = 332 mA/mm, R_{ON} = 5.1 Ω·mm. $I_{D,max}$ and R_{ON} are extracted at V_{GS} = 5 V (E-mode) and V_{GS} = 1 V (D-mode). The transistors are measured at room temperature.

temperature, as it is limited by the gate leakage current.

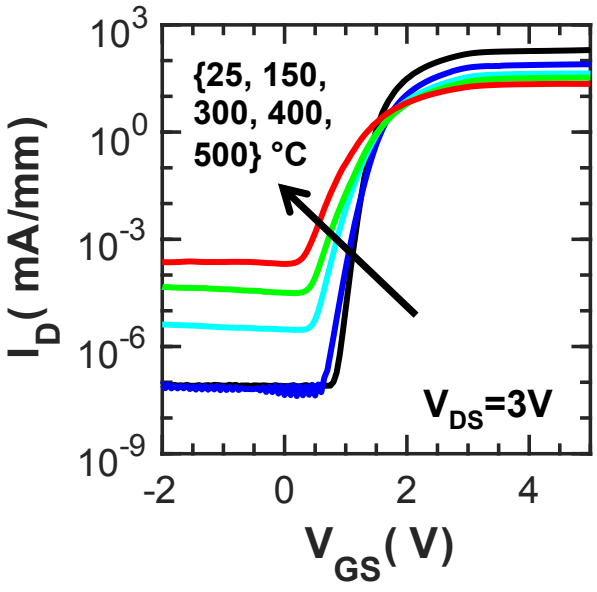


Figure 2-5: Transfer characteristics of E-mode HEMTs from room temperature to 500 °C.

Both analog and digital applications require components with closely-matched temperature-behavior to ensure a stable operation across the entire temperature range. One advantage of direct-coupled FET logic is the inherently matched temperature behavior, resulting from the same AlGaN/GaN channel. The trend of maximum on-current reduction for both E/D-mode transistors are plotted in Fig. 2-8, where $V_{GS} = 5$ V for E-mode transistor, and $V_{GS} = 0$ V for D-mode transistor (in the E/D-mode logic DCFL configuration, D-mode transistor serves as an active load with gate-source tied together). A similar trend is observed from across temperature, indicating an excellent thermal-matched behavior.

2.3.2 Gate Leakage Current

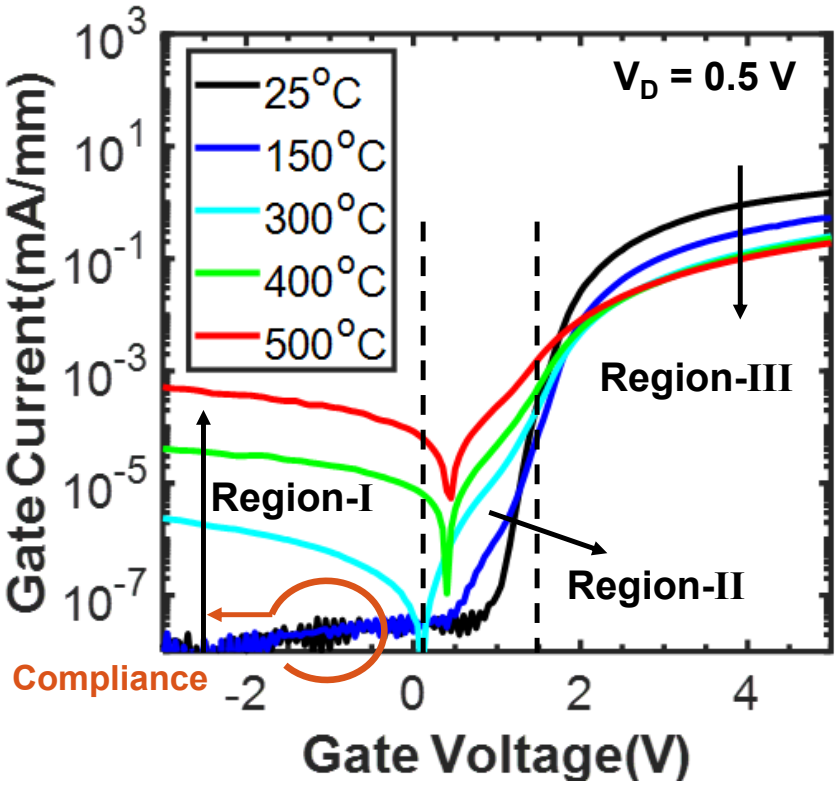


Figure 2-6: Trend of gate leakage current over temperature [1]. The $I_G - V_G$ characteristics can be divided in to three regions, namely, reverse bias region (region-I), low-forward bias region (region-II), and large forward bias region (region-III).

The gate leakage current characteristics are shown in Fig. 2-6. The $I_G - V_G$ characteristics can be divided in to three regions, namely, reverse bias region (region-I), low-forward bias region (region-II), and large forward bias region (region-III). As can be seen, the I_G in both region-I and region-II increases linearly as $|V_G|$ increases, leading to a constant conductance. Due to the traps introduced during the p-GaN removal, it is believed that two-dimensional variable range hopping (2D-VRH) model is the main gate leakage mechanism, leading to the increase of I_G over temperature,

as described by the following equation [74]:

$$\sigma \propto \exp\left(-T^{-1/3}\right) \tag{2.1}$$

where $\sigma = \partial I_G/\partial V_G$ is the conductance, and T is the absolute temperature in K. The linear relationship between $I_G \propto \ln(\sigma)$ and $T^{-1/3}$ from 423 K to 773 K indicates the applicability of the 2D-VRH model (Fig. 2-7(b)).

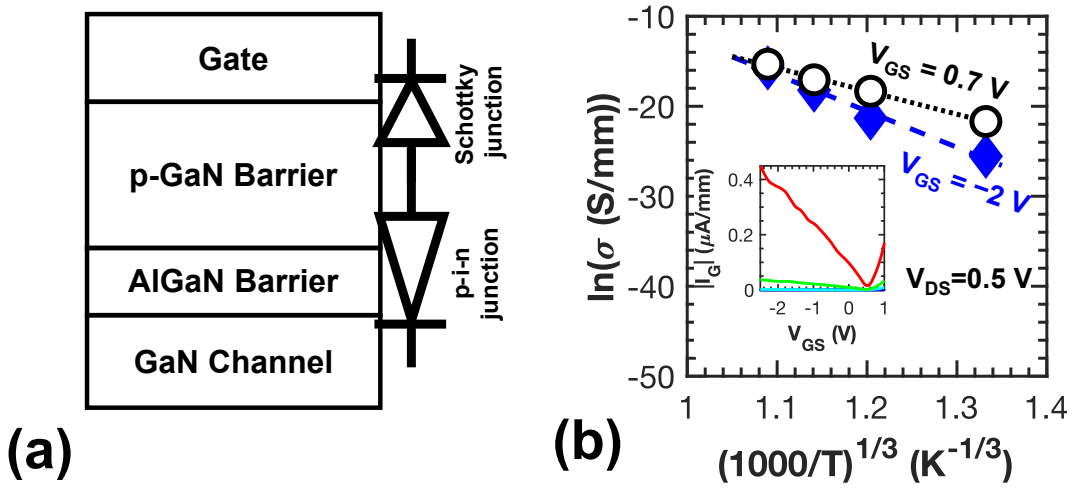


Figure 2-7: (a) Schematic of gate structure (tungsten/p-GaN/AlGaN/GaN). It can be modeled as two back-to-back junctions, namely, Schottky junction and p-i-n junction. (b) lnσ at $V_G = -2$ V and $V_G = +0.7$ V as a function of $T^{-1/3}$ showing straight lines. The inset shows the I_G over V_G in linear scale.

Different from the increasing I_G in region-III reported by N. Xu *et al.* in [74], the turn on current I_G in region-III decreases with increasing temperature due to increased resistance in the drift region of p-i-n junction. As can be seen in the Fig. 2-8, both I_G at $V_{GS} = 5$ V and on-current at $V_{DS} = 5$ V decreases from room temperature to 500 °C due to the reduced mobility resulting from increased optical

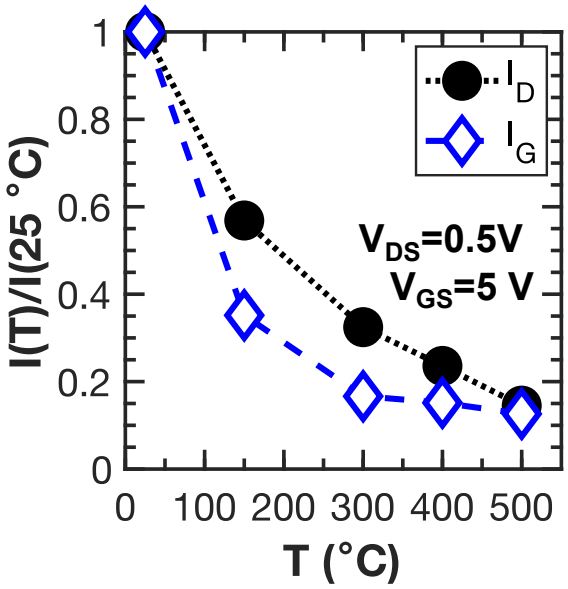


Figure 2-8: Both I_G and I_D decreases over temperature, indicating that the degradation mechanism resulting from decreased mobility caused by photon scattering (difference in trend may be explained by the difference of phonon scattering in bulk and 2DEG).

phonon scattering. The difference in the trend could be explained by the difference in difference of optical phonon scattering in bulk and 2DEG.

2.3.3 Threshold Voltage

As seen in Fig. 2-9, V_{TH} of E-mode transistor is relatively stable below 300 °C with gate structure shown in Fig. 2-7(a). The small initial increase of V_{TH} from room temperature to 200 °C can be attributed to the incomplete ionization of p-type dopant in the p-GaN at room temperature and higher ionization efficiency at increasing temperature [75]. The reason for the decrease of V_{TH} at temperature above 300 °C may be explained as follows: (1) the increase in intrinsic carrier concentration, (2) increase in

tungsten work function, (3) decrease in E_g of GaN, leading to a temperature variation of fermi level, lower forward turn-on voltage of p-i-n junction, and reduced Schottky barrier height ($V_{bi} = \chi + E_g/q - kT \ln(N_v/p)/q - \Phi_W$, where χ is the electron affinity of GaN, N_V is the valence band density of states, p is the activated p-type dopant concentration, and Φ_W is the work function of W).

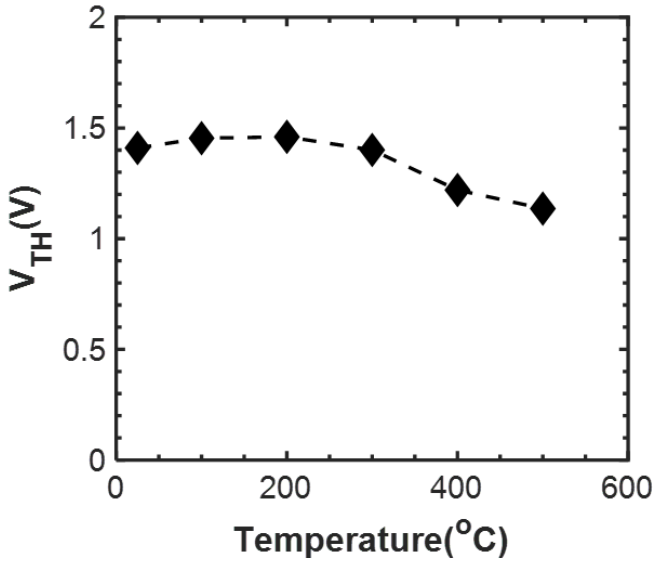


Figure 2-9: V_{TH} over temperature. It first increases below 200 °C, and then start to decrease up to 500 °C. The gate structure is shown in Fig. 2-7(a).

Both E/D-mode transistors can operate safely at 500 °C. A slightly higher gate leakage current of the D-mode transistor is observed. Due to the nature of DCFL logic, the gate leakage current of D-mode device has minimal impact on the circuit performance. The results show the promising potential of the proposed technology for emerging HT applications at 500 °C and beyond.

2.4 Yield, Uniformity, and Gate Leakage Suppression

A major challenge in the realization of GaN HT-robust sequential logic circuits is the lack of a scalable process technology, which determines the level of integration of GaN HT electronics, as is the case in previous experiments [76]. In order to address this issue, an optimized process flow was demonstrated with improved uniformity. Furthermore, as illustrated in the previous section, the source of large forward gate leakage current, which will have negative impact on the transistor gate drive capability, may be attributed to the vertical junction current. The vertical junction current can be further reduced with the reduction of gate pad size.

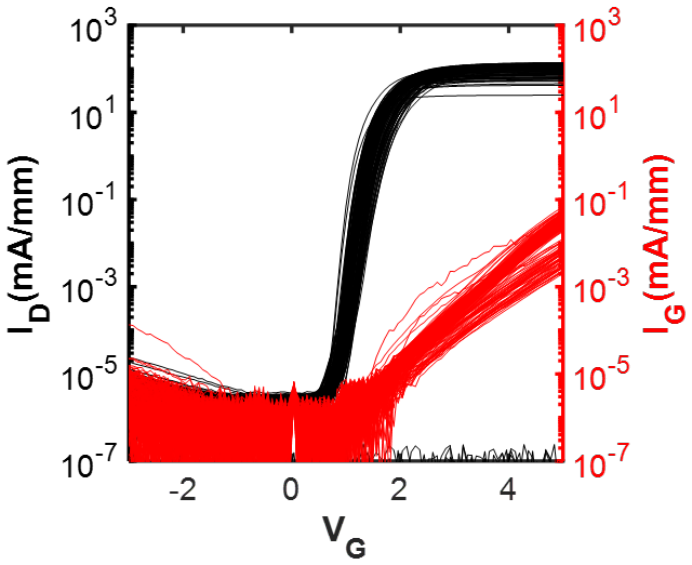


Figure 2-10: Transfer characteristics with V_{DS} = 0.5 V of a total of 192 E-mode transistors across a 1.2 cm × 1.2 cm sample with excellent average ON/OFF ratio $> 3 \times 10^7$. Measurements were conducted at 25°C.

Same wafer platform was used here (Fig. 2-2(a)), which allows for monolithic integration of enhancement-mode (E-mode) and depletion-mode (D-mode) transistors with up to two metal layers for interconnect. The sheet resistance of the AlGaN/GaN channel is 460 Ω/□. The E/D-mode HEMTs share the same $L_G = L_{GS} = L_{GD} = 2$ µm. Multi-finger topology is adopted to achieve a compact design for integration. In order to achieve significantly higher uniformity, a key improvement in the process flow is the use of BCl_3/SF_6-based etch stop process for the selective removal of p-GaN over AlGaN. Good uniformity was observed across 192 E-mode transistors on a 1.2 cm × 1.2 cm sample with $V_{TH} = 1.35 \pm 0.094$ V, $I_{D,max} = 490 \pm 40$ mA/mm (Fig. 2-11).

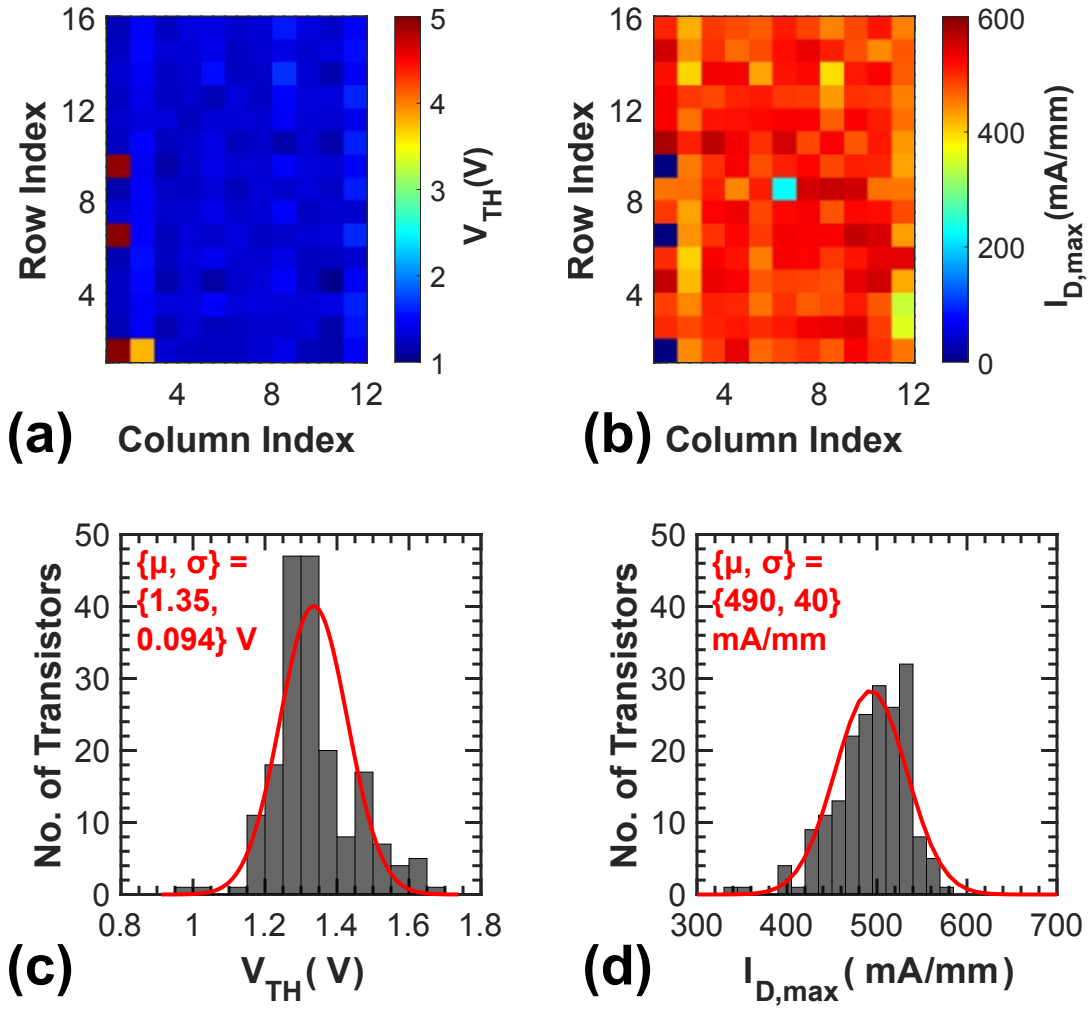


Figure 2-11: (a) distribution and (c) histogram of V_{TH}, and (b) distribution and (d) histogram of $I_{D,max}$ of a total of 192 E-mode transistors across a 1.2 cm × 1.2 cm sample. V_{TH} is measured at $V_{GS} = 0.5$ V. $I_{D,max}$ is measured at $V_{GS} = 5$ V.

2.5 Channel Length Scaling

A scaling bottleneck in the p-GaN-gated HEMT is the lack of self-alignment (SA) between the gate metal and the p-GaN gate. A longer p-GaN gate would increase gate

capacitance, which is highly undesired for high-speed low/medium-voltage power ICs and future analog mixed-signal applications. Various techniques to achieve SA gate p-GaN etch have been proposed [77]. Here a simple process flow was proposed to achieve self-aligned p-GaN gate with scaled gate lengths, which can also be integrated with p-channel GaNFETs as illustrated in Fig. 2-12 and detailed process flow described in Fig. 2-13. The SA gate process begins with the sputtering of W (100 nm). Ni/Au/Ni

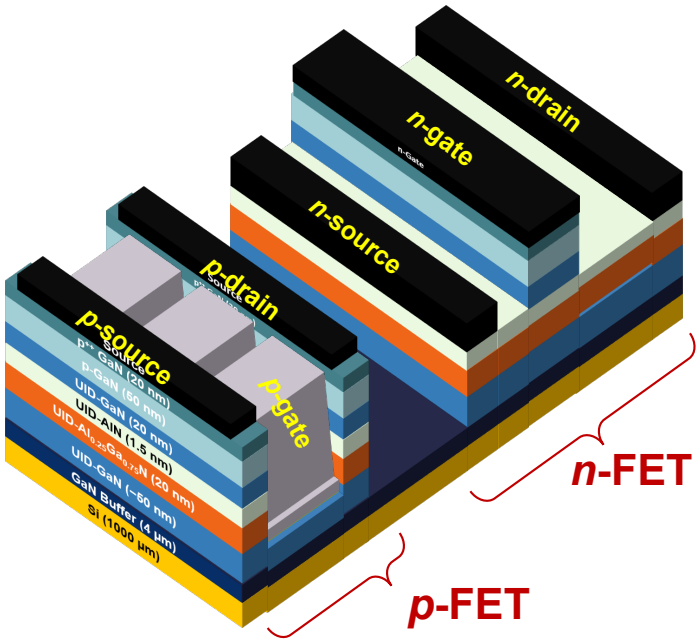


Figure 2-12: Concept of monolithic integration of n-FET and p-FET on the same platform without the need of any regrowth.

(30/120/80 nm) was patterned by electron beam lithography and lift-off (Fig. 2-13(b)). W was then etched. Selective etching of p-GaN over AlGaN was achieved using SF_6/BCl_3 plasma (Fig. 2-13(c)). Ti/Al/Ni/Au (20/100/25/50 nm) was alloyed at 800°C to form ohmic contacts (Fig. 2-13(d)). The typical contact resistance is 0.75 Ω·mm, which could be further optimized for the AlN/AlGaN barrier (Fig. 2-13(e)).

The use of Ni/Au/Ni allows for, (1) the top Ni to act as the hard mask for gate definition; (2) the reduction of gate resistance from 10 Ω/□ (W only) to < 0.5 Ω/□ (W + Ni/Au/Ni). A scaled SA p-GaN-gated HEMT is illustrated in Fig. 2-13(e).

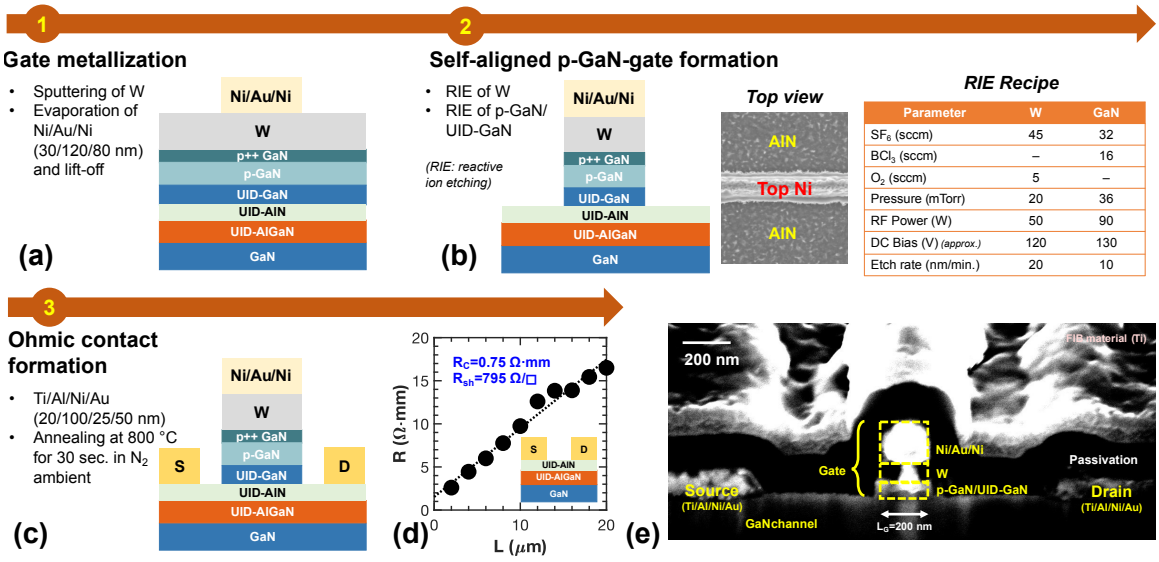


Figure 2-13: (a) The advantage of the use of an as-grown gate interface (p-GaN gate) instead of etch removal of p-GaN is reflected in a simple experiment using a conventional p-GaN/AlGaN/GaN epitaxial structure, where the AlGaN/GaN HEMT (with etched AlGaN surface) shows significantly worse ON/OFF ratio (limited by gate leakage current) compared to the p-GaN/AlGaN/GaN HEMT (with as grown gate surface). This is likely caused by the etch-induced damage to the gate region. Process flow: (b) Conformal deposition of W, then patterning of Ni/Au/Ni (30/120/30 nm) using electron beam lithography and lift-off. (c) Self-aligned (SA) p-GaN gate with gate metal is achieved using subsequent etch of W and GaN layers. AlN layer aids the etch stop to prevent damage to the n-channel. (d) Deposition of Ti/Al/Ni/Au contacts. (e) TLM measurement of ohmic contacts (with all p-GaN removed). (f) Cross-section image of the highly scaled SA p-GaN-gated HEMT.

A scaled n-FET with L_G/L_{SD} = 0.2/1.1 μm shows good current saturation with $I_{D,max}$=525 mA/mm, R_{ON}=2.9 Ω·mm (Fig. 2-15(b)). In p-GaN-gated AlGaN/GaN HEMTs, the maximum achievable I_D would be limited by (1) gate leakage which becomes significant after $\sim 3-4$ V (hence limiting gate overdrive); (2) in the case of

short-channel transistors, the carrier velocity saturation. E-mode operation ($V_{TH} \approx$ 1.6 V) was achieved (Fig. 2-15(b)). Peak g_m of 265 mS/mm reflects the good gate control and channel accumulation.

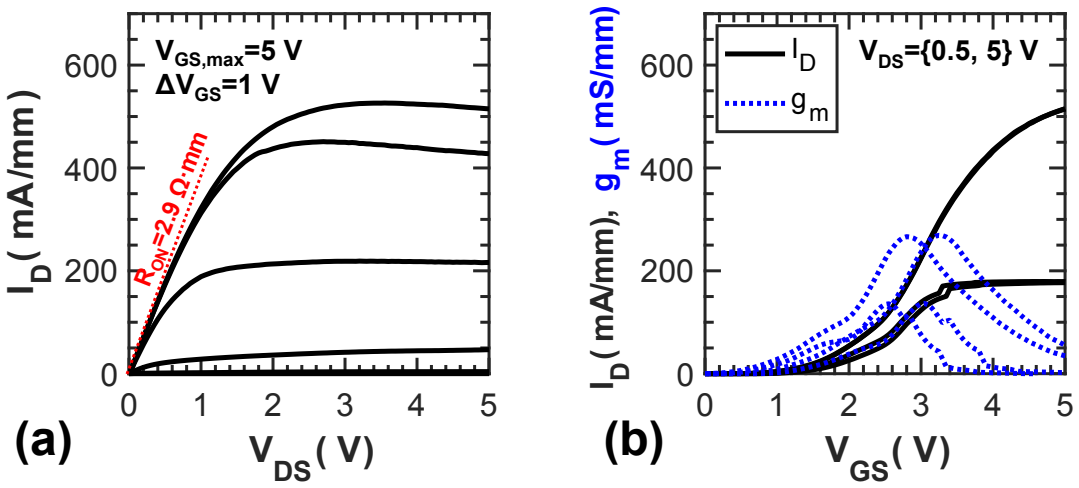


Figure 2-14: Performance of n-FET with $L_G = 200$ nm, $L_{SD} = 1.1$ mum on epitaxial structure optimized for p-GaN performance as reported in Fig. 2-13. (a) Output characteristics, showing $R_{ON} = 2.9$ Ω·mm and good current saturation with $I_{D,max} =$ 525 mA/mm (calculated at $V_{GS} = 5$ V). (b) Transfer characteristics, showing $V_{TH} \approx$ 1.6 V and peak g_m=265 mS/mm.

While the epitaxial structure with additional unintentionally-dope (UID)-GaN between p-GaN and AlGaN in Fig. 2-15 is designed to achieve a better p-FET performance, the n-FET performance on a conventional epitaxial structure (Fig. 2-2) is also demonstrated here. Better output characteristics ($I_{D,max} = 750$ mA/mm, $R_{ON} = 1.3$ Ω·mm) were observed in the n-FETs based on the conventional epi-structure (Fig. 2-15(a)). The results indicate the robustness of the proposed highly scaled SA p-GaN gate process and its applicability to similar epitaxial structures. Fig.

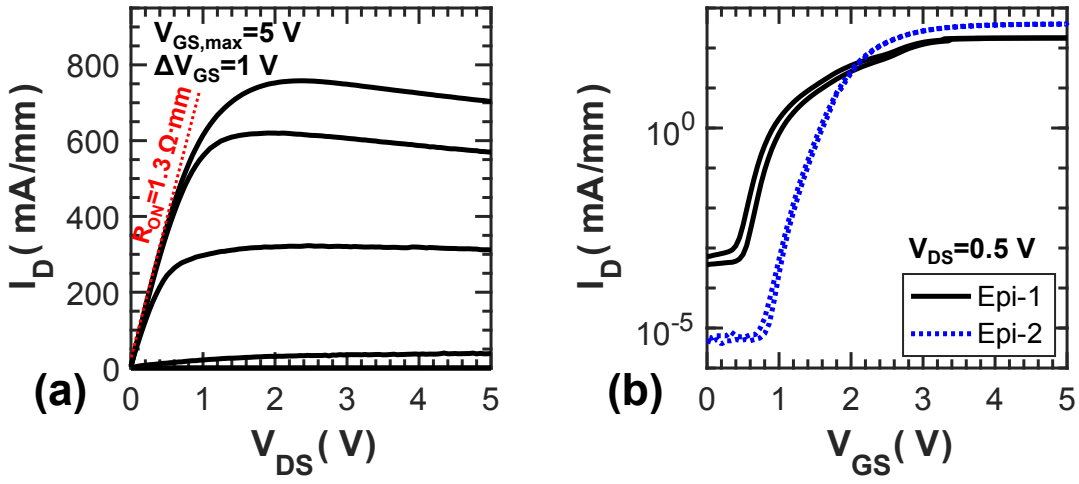


Figure 2-15: Performance of n-FET with $L_G = 200$ nm, $L_{SD} = 1.1$ µm on conventional epi-structure (Fig. 2-2). (a) Output characteristics, showing $R_{ON} = 1.3$ Ω·mm and good current saturation with $I_{D,max} = 750$ mA/mm (calculated at $V_{GS} = 5$ V). (d) Comparison of the performance of n-FETs based on the two structures, in terms of the transfer characteristics. By using conventional epi-structure, a more positive V_{TH} (E-mode), an improvement in current ON/OFF ratio (by more than two orders of magnitude) and a sharper ON/OFF transition was achieved. This is attributed to the location of the gate metal closer to the channel at the AlGaN/GaN interface, as well as better gate electrostatic control due to a simpler epitaxial structure above the AlGaN barrier.

2-15(b) reveals that, by using conventional epitaxial structure, a more positive V_{TH} (E-mode), a higher current ON/OFF ratio (by more than two orders of magnitude), a sharper ON/OFF transition, and a negligible hysteresis (< 0.1 V) were observed. The above improvements are attributed to the location of the gate metal closer (by 25 nm) to the n-channel at the AlGaN/GaN interface, and better gate electrostatic control due to a simpler epitaxial structure (absence of UID-GaN and AlN) above the thinner AlGaN layer.

The OFF-state characteristics of the scaled n-FETs on the p-FET epi-structure

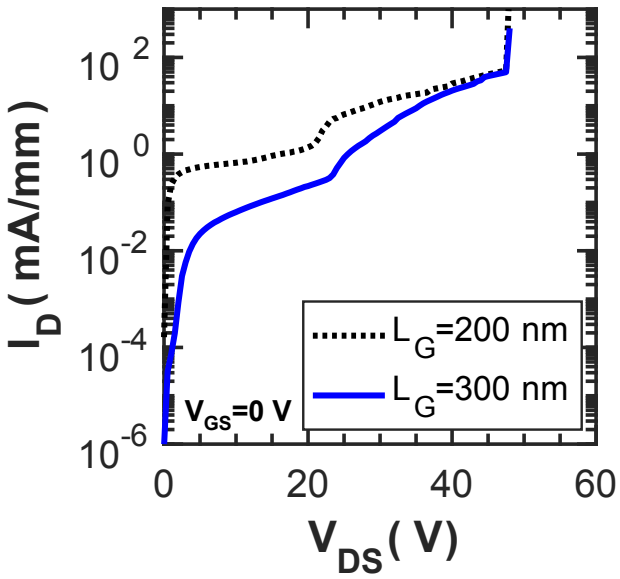


Figure 2-16: OFF-state characteristics of n-FETs (Epi-1), without any electric field management structures (e.g. field plate, edge termination). A slightly longer gate length would improve the gate control and therefore reduce the leakage current before destructive breakdown (both at ∼50 V due to destruction of probe pad).

(Fig. 2-13) were studied (Fig. 2-16). A slightly longer gate length would improve the gate control and therefore reduce the leakage current before destructive breakdown (both at $\sim$ 50 V due to destruction of probe pad). The above devices did not feature any electric field management structure (e.g. field plate). With further optimization of the electric field management in both n-FET and p-FET (limited by drain-induced barrier lowering, DIBL), the scaled CFETs would be desirable for use in lower voltage GaN complementary circuits.

2.6 High Temperature Robustness

Early reports indicate p-GaN-gated HEMT operation up to 420 °C, as well as their integration in E/D-mode HT (maximum of 500 °C) digital circuits such as ring oscillators and memory cells [78, 76]. While the initial demonstrations are encouraging, it is equally important to understand the long-term robustness (beyond quick measurements in a laboratory setting) at HT (> 500 °C) of the transistor, in order to further evaluate their potential for HT electronics. Thus both in-situ measurement and ex-situ measurement were conducted to evaluate the performance degradation.

For in-situ measurement, an in-house developed packaging technology and measurement setup were used. The sample was first diced and attached to a 96% Alumina PCB through ceramic adhesives. 1 mil Au Wire bonding was then performed between the device under test (DUT) and PCB pins, and gold-plated copper wires with a American wire gauge (AWG) of 28 were then press-fit to the other terminal of PCB pins (Fig. 2-18(b)). The gold-plated wires, wrapped in 3M™ Nextel™ sleeving for isolation, were extended outside furnace and connected to the measurement setup. The in-situ measurement was performed when the DUT stayed in the furnace up to 500 °C under N_2 ambient.

As shown in Fig. 2-19, at HT (in-situ measurement, i.e. device is measured at 500 °C), the maximum drain current (I_{Dmax}) is reduced and ON-resistance (R_{ON}) is increased. This reflects the degradation of mobility due to the increase of phonon scattering. The drain current in OFF-state is dominated by the gate leakage current

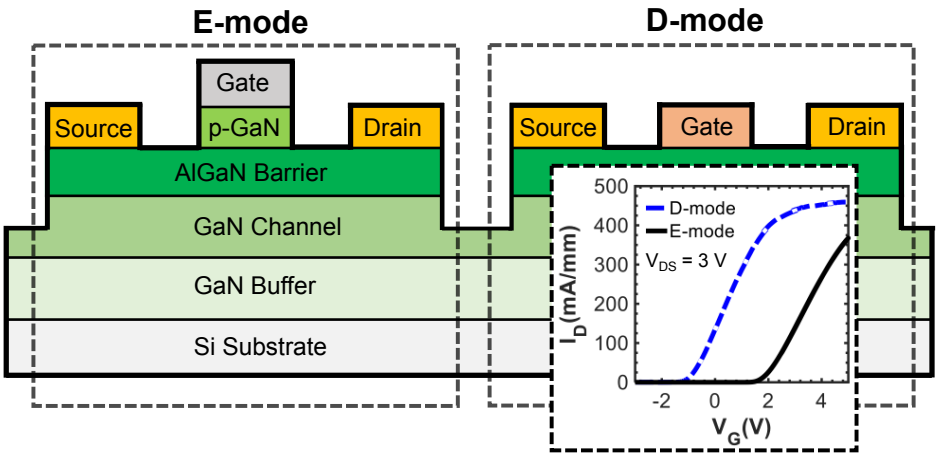


Figure 2-17: Illustration of the E-mode p-GaN-gated AlGaN/GaN HEMT in this work. Its monolithic integration with a D-mode AlGaN/GaN HEMT is also illustrated. Typical transfer characteristics of both transistors are shown in the inset, with $V_{TH\{E,D\}} = \{1.8, -1\}$ V.

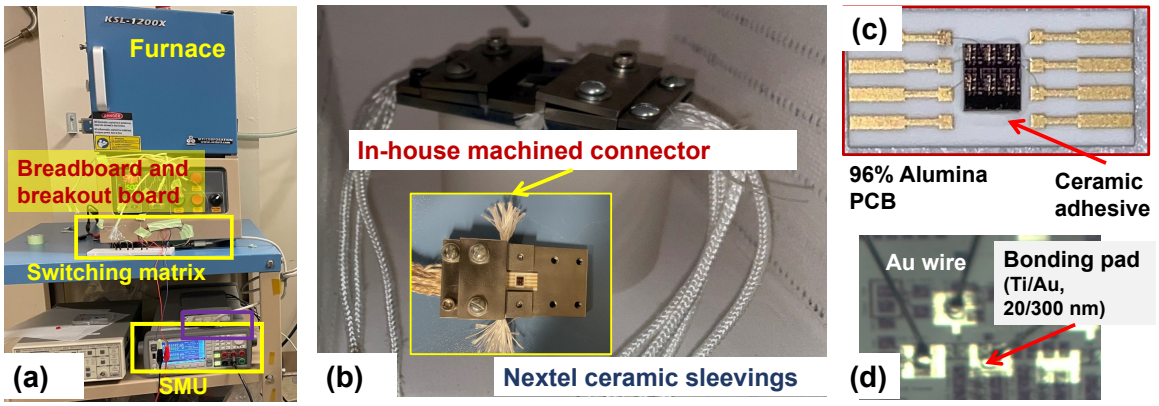


Figure 2-18: Experimental setup for HT (up to 500 °C) measurement. (a) Overview of the setup. The DUT is placed in the furnace in N_2 ambient. The switching matrix is used if more than one DUT needs to be measured. (b) Custom-made packaging for HT measurement, showing the in-house machined connectors and wires which are wrapped in 3M™ Nextel™ sleeving. (c) Printed circuit board (PCB) made of 98% alumina. The bare die is attached using a ceramic adhesive. (d) DUT. The transistor electrodes are connected to Ti/Au bonding pads.

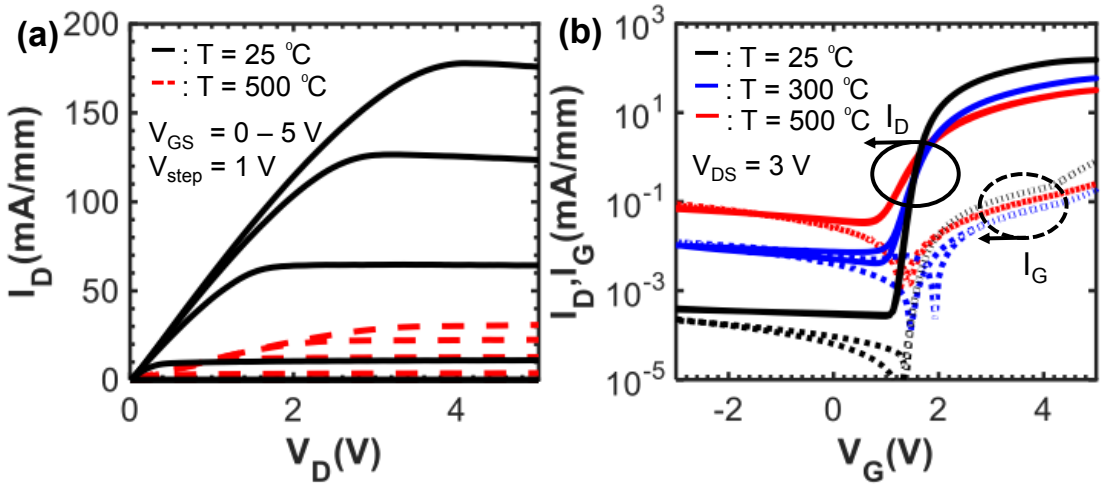


Figure 2-19: (a) Output and (b) Transfer characteristics (double sweep) of the packaged DUT ($L_{SD} = 6$ µm, $L_G = 2$ µm) from RT up to 500 °C.

(Fig. 2-19(b)). At HT, hole activation in p-GaN increases significantly. In the gate diode reverse bias (negative V_{GS}) and weak forward bias (small positive V_{GS}) regimes, the gate leakage current increases due to two-dimensional variable range hopping (2DVRH) as illustrated in the previous section. In the strong forward bias (highly positive V_{GS}) regime, it is believed that, the gate current first decreases up to 300 °C due to reduced mobility of carriers which is same as what was found in Section 2.3.2, then increases at higher temperature primarily due to the passivation or packaging (not intrinsic DUT) as the large forward gate leakage current is no longer dominated by the vertical junction current. Instead, the surface leakage current might be the dominant factor as suggested by the symmetrical gate leakage current in the Fig, 2-19. Further studies would be required to fully understand the mechanisms.

The DUTs were subjected to HT (500 °C) robustness studies. Firstly, an in-situ measurement of the DUT was conducted over 24 hours. As shown in Fig. 2-20,

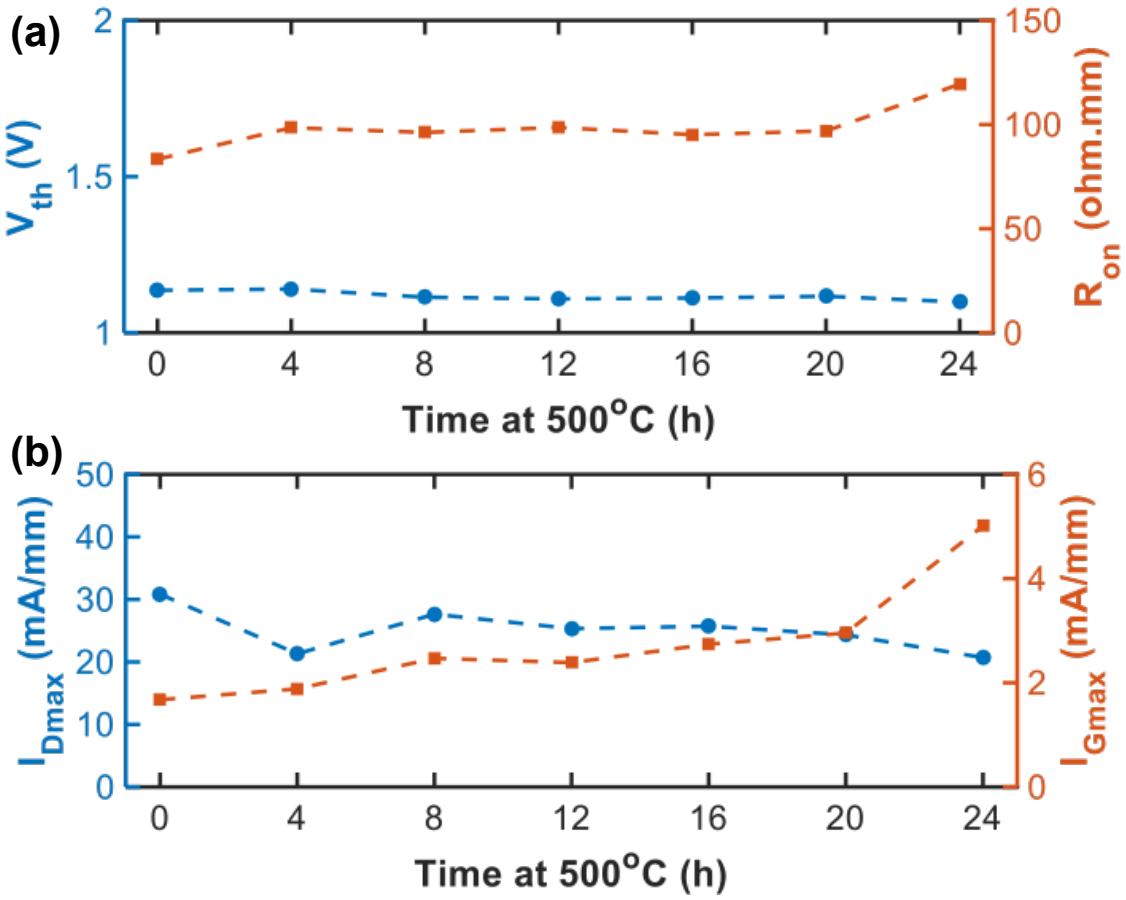


Figure 2-20: In-situ measurement of packaged DUT at 500 °C in N_2 over 24 h: (a) V_{TH} and R_{ON} (V_{GS} = 5 V), (b) I_{Dmax} ($V_{DS} = V_{GS}$ = 5 V) and I_{Gmax} (V_{DS} = 0 V, V_{GS} = 5 V).

the V_{TH} and I_{Dmax} remained relatively stable (< 5% variation) for over 20 hours. Interestingly, some degradation in I_{Dmax} was observed after 20 hours together with the increase in I_{Gmax}. The physical origins of the degradation would require further material characterization of the DUT.

Having established the relative stability of the DUT using in-situ measurement, a survival test for 20 days was conducted. During this experiment, the DUT was regularly taken out of the furnace and cooled to RT for ex-situ measurement. Given

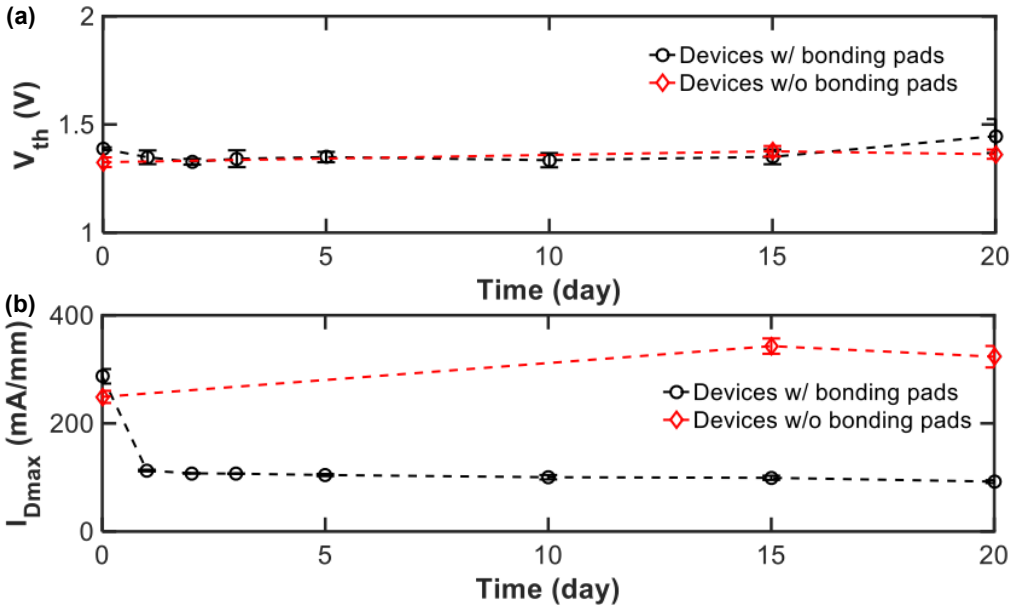


Figure 2-21: Survival test of several DUTs with/without packaging (bonding pads) over 20 days in N_2 ambient. Ex-situ measurements were performed at RT: (a) V_{TH}, (b) I_{Dmax} ($V_{DS} = V_{GS} = 5$ V). To the best of the author's knowledge, this is the first report of long-term survivability of p-GaN-gated AlGaN/GaN HEMT at HT (500 °C). The results show great stability in both V_{TH} and I_{Dmax}. However, the use of bonding pads caused significant degradation to the measured I_{Dmax}.

that the packaging (used in in-situ measurement) might contribute to some degradation, DUTs with and without packaging were subjected to the same experiment. As presented in Fig. 2-21, the DUTs were again found to exhibit stable DC performance over 20 days. An interesting observation is the difference between the DUTs with and without packaging, where the packaging caused a degradation of the measured current level even on the first day.

At the end of the tests, a visual inspection of the DUT revealed minimal damage in the intrinsic device (Fig. 2-22(a)). As shown in Fig. 2-22(b), no noticeable difference in the epitaxial structure was observed. These results establish that, the epitaxial

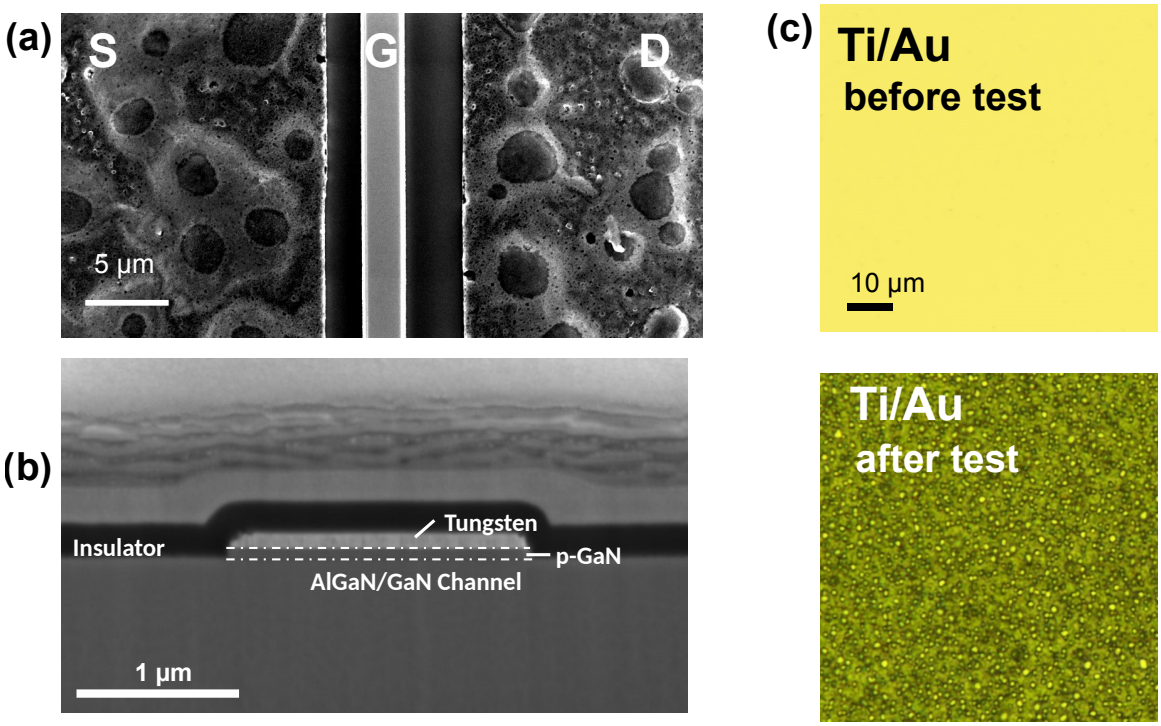


Figure 2-22: (a) Scanning electron microscopy (SEM) image of DUT after survival test (500 °C for 20 days in N_2 ambient). No noticeable degradation was observed in the alloyed ohmic contacts and the gate, indicating the robustness of the proposed transistor technology. (b) Cross-sectional image of the gate region. (c) Optical images of the Ti/Au bonding pad before and after HT survival test. The change in color indicates the change from a predominantly gold top layer to an inter-diffused Ti/Au alloy. The degradation of the Ti/Au bonding pad indicates the need for HT-robust BEOL structures.

structure and the device processing of this work are suitable for building a platform for HT-robust electronics.

In terms of the back-end-of-line (BEOL) structures, significant inter-diffusion was observed in the Ti/Au layers (Fig. 2-22(c)), which serve as bonding pads (Fig. 2-18(d)). This is identified as the main cause for the current degradation of the packaged DUT after being exposed to HT. Metallization schemes which are less susceptible to inter-diffusion, such as Ni/Au, should be used. This observation highlights the need

for HT-robust BEOL.

A benchmarking of HT performance variation with published / commercially available wide band gap transistors is presented in Fig. 2-23 [2, 3, 4, 5, 6, 7]. Two parameters, namely relative change in I_{Dmax} and V_{TH}, are chosen due to their significance for eventual application of the proposed transistors for circuit design. The reported p-GaN-gated AlGaN/GaN-on-Si HEMT, similar to other GaN-on-Si HEMTs, exhibit more HT current degradation than other transistors. The The key factors that explain this variation include, (1) at RT, higher lattice mismatch (2) with rising temperature, higher mismatch of coefficient of thermal expansion (CTE), both of which exist in the heterostructure (AlGaN/GaN *vs.* InAlN/GaN) and in the GaN buffer layer grown on the non-native substrate (Si *vs.* SiC/sapphire). Besides, V_{TH} is relatively stable from RT to 300 °C, and a decrease of $\sim 0.3 - 0.4$ V from 300 °C to 500 °C. Nevertheless, an E-mode operation is maintained from RT to 500 °C and the total temperature variation of V_{TH} is relatively small, which greatly simplify the design of mixed-signal circuits intended to work over a wide temperature range.

It is worth mentioning that for both traditional long-channel and short-channel AlGaN/GaN HEMTs (long-channel: orange circle, short-channel: dark blue square), short-channel AlGaN/GaN HEMTs exhibits significantly better on-current at high temperature. It can be explained by the slower degradation in R_C compared to the faster degradation in *mobility*. Therefore, short-channel HEMTs, whose R_{ON} is dominated by R_C, has less on-current degradation, compared to long-channel HEMTs

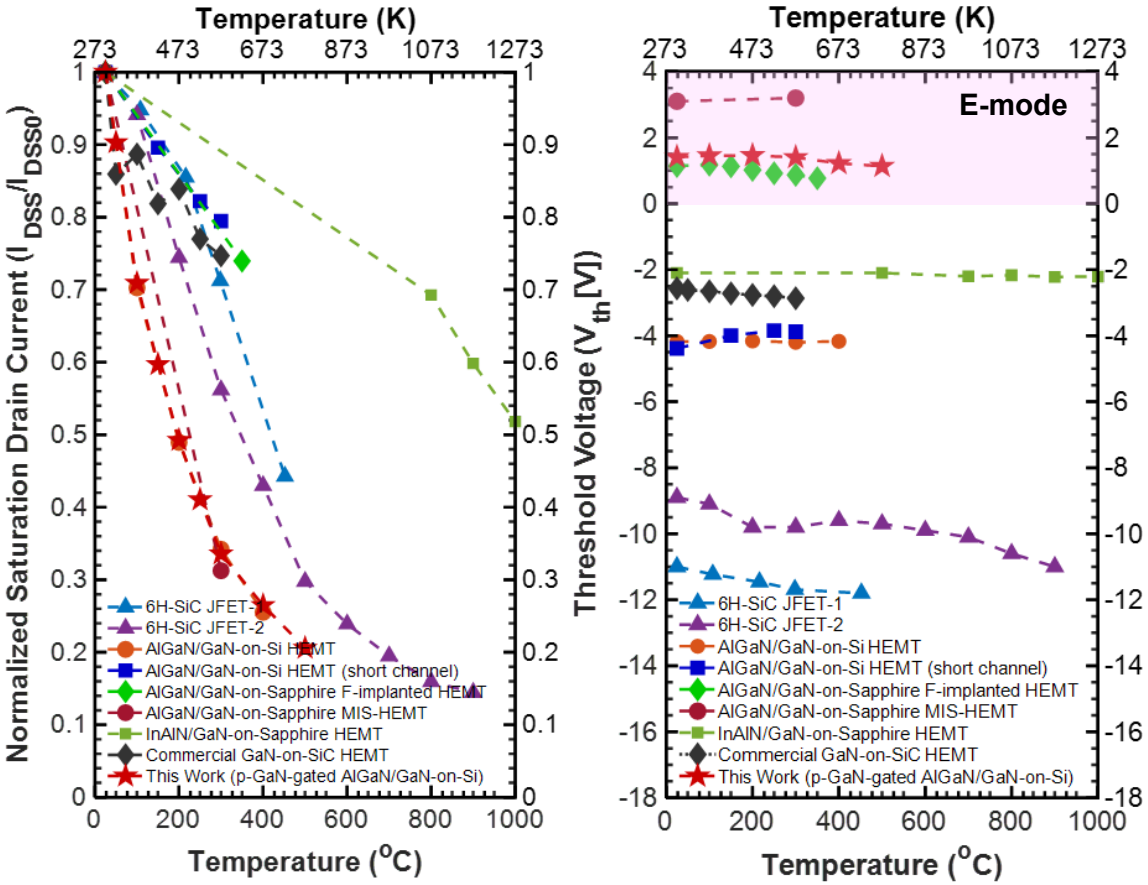


Figure 2-23: Benchmarking of performance variations at HT of the reported DUT with other published and commercially available wide band gap transistors, (a) saturation drain current as a function of temperature, normalized to value at RT. The DUT shows similar current degradation trend with typical AlGaN/GaN-on-Si HEMTs. (b) V_{TH}, which is relatively stable and exhibits E-mode characteristics from RT to 500 °C. All of the listed devices are bare die devices [2, 3, 4, 5, 6, 7].

whose R_{ON} is dominated by channel mobility. The explanation is further verified by the MIT virtual source GaN-FET model, a charge-based physical model that can be used for GaN transistors, and will be illustrated in chapter 3. The results indicate that in addition to using lattice-matched heterostructure, channel length scaling could be an another potential approach to achieve less on-current degradation over temperature.

2.7 Conclusion

In this chapter, a GaN high temperature device technology based on the p-GaN/AlGaN/GaN wafer platform was demonstrated. The fabricated device show stable operation up to 500 °C. The physics behind the performance degradation was studied and explained. A high uniformity, a critical metric for large-scale integration, was achieved with the optimization of selective-etch process, Furthermore, the potential of aggressive channel length scaling was also studied based on the similar process, and better R_{ON}, I_{ON} were observed. Besides, an in-house developed packaging technology and measurement platform with high temperature ratings were proposed. An in-situ measurement at 500 °C over 24 h was successfully demonstrated. The fabricated transistors exhibited stable performance over 20 days at 500 °C.

Chapter 3

Compact Modeling and Circuit Design

The compact model serves as a critical bridge between device and circuit level simulation [79, 80]. Driven by the need to realize GaN ICs with a higher degree of complexity and integration, compact modeling is unsurpassed in its ability to allow complex circuit designs, even though other techniques such as technology computer-aided design (TCAD) mixed-mode simulation are also available. Based on the proposed device technology, the next step is to develop accurate compact models for both E/D-mode devices over the entire temperature range (RT to 500 °C). However, the main focus in this section is placed on the compact modeling of the E-mode device, as the D-mode device only serves as an active load in the DCFL configuration and can be simplified as a two terminal device which greatly reduce the modeling effort.

3.1 Compact Modeling of E/D-mode HEMT

In this section, temperature-dependent compact models were developed for the in-house fabricated E/D-mode transistors based on the industry-standard MIT virtual source GaNFET (MVSG) models [81]. MVSG model is a charge-based physical model that can be used for GaN-based transistors. For the room temperature fitting, the IC-CAP simulator would first be used to extract and optimize parameters from IV and CV measurements. A Verilog-A model will then be generated based on those parameters to fit experimental data. The entire optimization procedure might need several iterations from optimizing parameters to fitting the experimental data. The fitting results are shown in the Fig. 3-1. They are connected as E/D-mode DCFL configuration with a drive/load ratio $\beta = 3$ (Fig. 3-1(b)).

Although the model is physics-based, the fitting of temperature dependency is mostly empirical based on the measurement results obtained in the previous section. The model was calibrated as shown in the Fig. 3-2(a)–(c) from RT to HT. An excellent fitting was achieved and the calibrated model will be used in the next section. The key parameter related to temperature dependency are (1) threshold voltage (V_{TH}), (2) carrier velocity, (3) mobility, (4) contact and sheet resistance, (5) subthreshold swing. From the previous chapter, V_{TH} first slightly increases and then decreases across temperature due to a combination effects. However, due to the small variation in the V_{TH} from room temperature up to 500 °C, the threshold voltage of GaNFETs is simplified as a linear decrease over temperature. The other parameters follow the

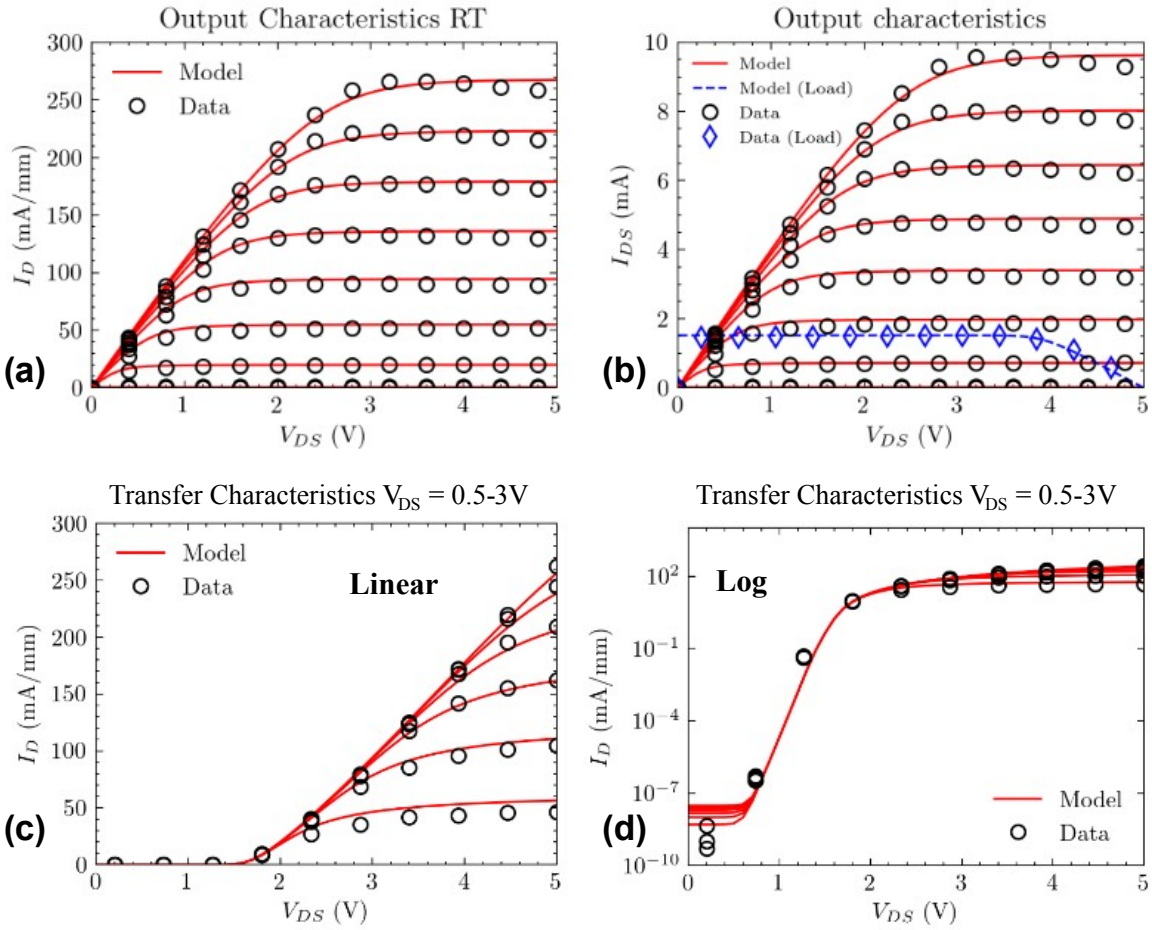


Figure 3-1: Device characteristics at room temperature. (a) Normalized output characteristics of the E-mode transistors with V_{DS} = 0 to 5 V, V_{GS} = 0 to 5 V, and ΔV_{GS} = 0.5 V. (b) Output characteristics of E/D-mode inverter with a drive/load ratio $\beta = 3$, $\{W_E, W_D\} = \{36, 12\}$ μm. Normalized transfer characteristics of E-mode transistors in (c) linear scale and (d) log scale at room temperature.

following expressions:

$$V_x(T) = V_x(T_0) \times \frac{1 + V_\zeta T_0}{1 + V_\zeta T} \tag{3.1}$$

$$\mu(T) = \mu(T_0) \times \left(\frac{T}{T_0}\right)^{\epsilon} \tag{3.2}$$

$$SS(T) = SS(T_0) \times \frac{T}{T_0} \tag{3.3}$$

$$R(T) = R(T_0) \times \left[1 + R_{c1}(T - T_0) + R_{c2}(T - T_0)^2\right] \tag{3.4}$$

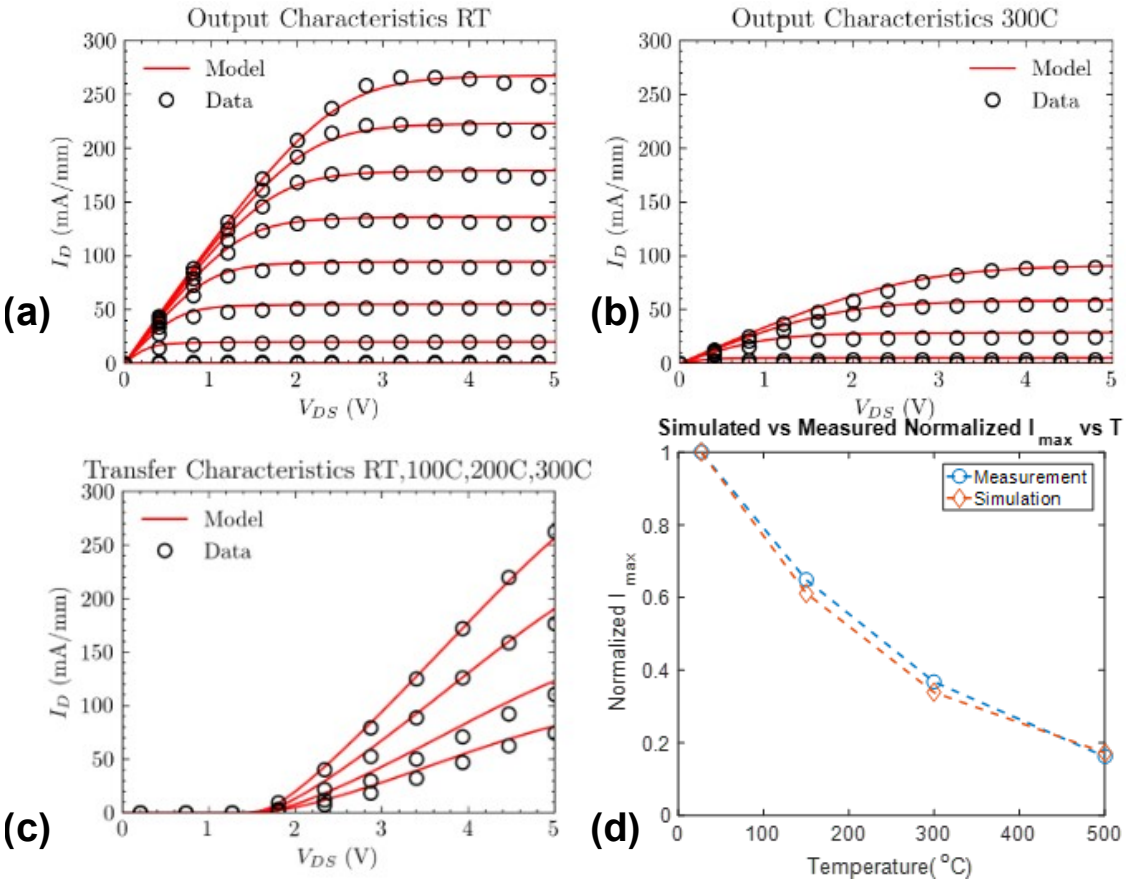


Figure 3-2: Device characteristics from room temperature to 500 °C. Output characteristics at (a) RT, (b) 300 °C. (c) Linear transfer characteristics. (d) Extrapolated $I_{D,max}$ with measurement data up to 500 °C.

where T_0 is the room temperature, V_ζ and ϵ are empirical values extracted from the measurement data. The output and transfer characteristics is shown in the Fig. 3-2(c) up to 300 °C. The model is extrapolated to 500 °C and still shows excellent agreement with measurement data as plotted in the Fig 3-2(d). It should be noted that a ϵ of 2.7 is used in this model, indicating a faster degradation of mobility of than the degradation of contact resistance which has a quadratic relationship over temperature. This results explains the less degradation of on-current of short-channel

AlGaN/GaN HEMTs with R_{on} dominated by R_C in Fig. 2-23.

3.2 Robustness-Driven Circuit Design for High Temperature Applications

The Verilog-A compact models demonstrated above, are used for building a variety of logic circuits. Both E/D-mode are available for simulation. The minimum device width (labeled as 1 in the schematic) is 6 µm in this work. All the circuit implementation in this work are based on the n-FET-only logic.

3.2.1 Combinational Logic

Depletion-load inverter *vs.* enhancement-load inverter

In this section, depletion-load and enhancement-load inverters are compared. Their circuit schematics are shown in Fig. 3-3. The pull-down network (PDN) of both inverters is a E-mode GaNFET; the pull-up network (PUN) of the depletion-load and enhancement-load inverters is a D-mode GaNFET with gate and source shorted and a E-mode GaNFET with gate and drain shorted, respectively. The supply voltage (V_{DD}) and width ratio (WR) of the transistors in PUN to PDN (WR) are two key parameters during designing the combinational logic circuit. To determine the best inverter configuration and design parameters, two groups of tests were conducted.

For the first group, the V_{DD} was swept from 3.5 V to 5 V with 0.5 V increment

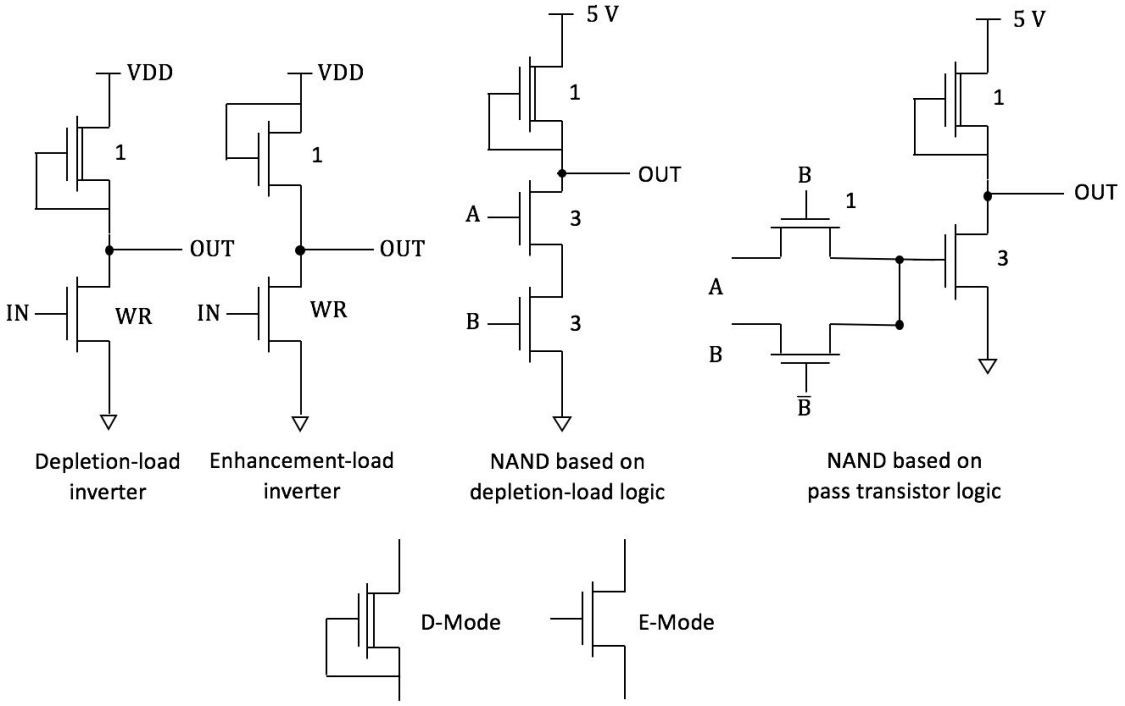


Figure 3-3: Schematics of combinational logic design. minimum width (1) here is 6 µm.

while fixing WR at 1:3; the width of top and bottom GaNFET are set as 6 µm and 18 µm, respectively. For the second group, WRs were changed from 2 to 4 while fixing V_{DD} at 5 V. Propagation delay and consumed power are measured in each test; Voltage Transfer Characteristics (VTC) are also generated so that noise margin and voltage swing for each case can be determined.

Depletion-load logic *vs.* pass transistor logic

In this section, depletion-load NMOS logic (DPL) and pass transistor logic (PTL) are used to build the same logic gate, which is the basic element of the arithmetic logic unit; schematics of the two gates are shown as Fig. 3-3. Simulations were run from 27 °C to 327 °C and various properties were extracted in each case. By comparing the simulation results of two gates, the logic that can give better performance can be determined. NAND gate is chosen to demonstrate the comparison since any combinational logic can be achieved by only using combinations of NAND gates. It should be noted that in general, NOR gate, as the other universal gate, is actually more preferred for the real applications using n-FET-only logic as the sizing of pull-down network is smaller compared to NAND gate to achieve the same performance.

3.2.2 Sequential Logic

Registers (flip-flops) and latches are the key timing elements for digital circuits. Here three common implementations of positive-edge registers in CMOS technology were

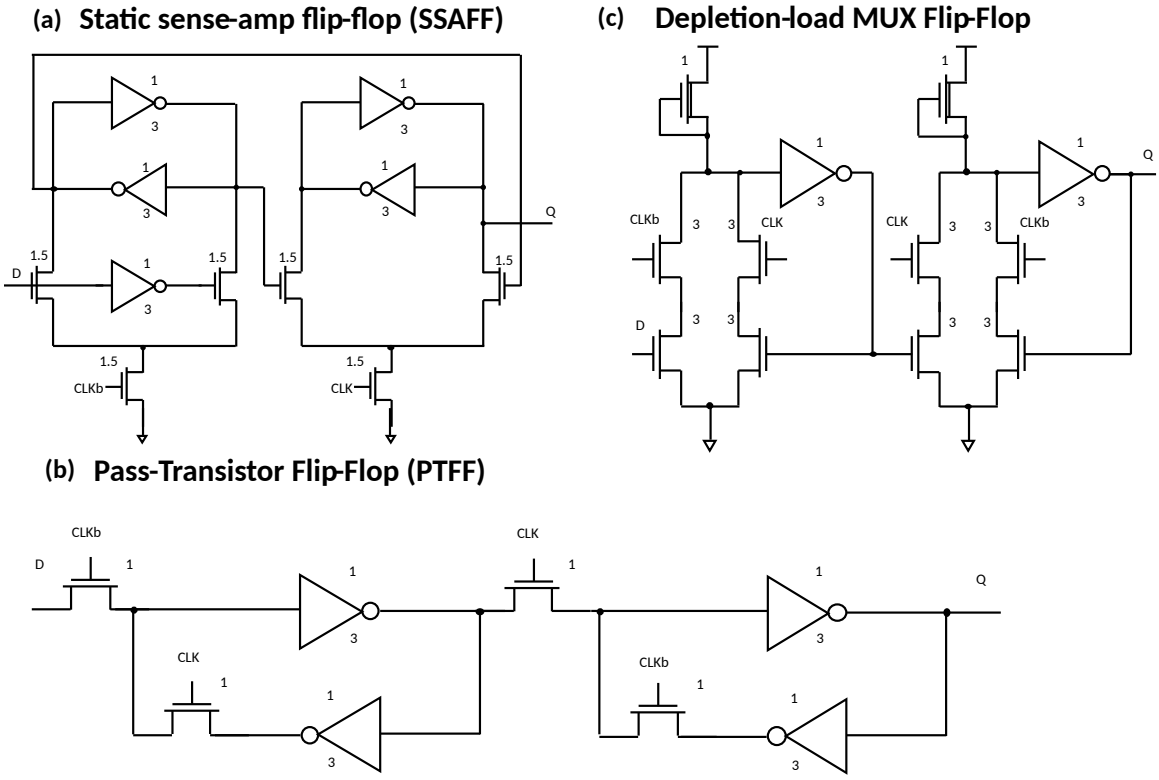


Figure 3-4: Schematics of (a) static sense-amp flip-flop, (b) pass-transistor flip-flop, (c) depletion-load MUX flip-flop.

compared. Fig. 3-4 presents the schematics for the flip-flops analyzed in this work. The designs were restricted to the fully static structures with single-rail inputs and outputs and skip input and output buffers in all three designs to make a fair comparison.

Unlike traditional circuit designs that focus on either low power or high speed, design principles here are to accommodate the needs of high robustness for HT operation. The reason that the static design is preferred over dynamic design is the tighter time constraint of dynamic structure at elevated temperature. As the temperature increases, lower on-current increases the delay and reduces the maximum frequency,

and higher leakage current implies a higher minimum frequency to refresh the floating nodes.

In this section, (a) Static sense-amp flip-flop (SSAFF); (b) Pass-transistor flip-flop (PTFF); and (c) depletion-load multiplexer filp-flop (DPMFF) were simulated and benchmarked.

SSAFF is chosen for its low clock load; PTFF is known to have reasonably fast speed and low power, while DPMFF is a variant of PTFF with higher noise margin and larger area.

3.3 Results and Discussions

3.3.1 Combinational Logic

Depletion-load *vs.* enhancement-load inverter

Results of V_{DD} sweeping are shown in Table 3.1. When the input is logic 1, the PDN and PUN of both inverters should be operated in linear and saturation regime, respectively. In this case, the R_{on} of the PDN decreases as V_{DD} increases, while the R_{on} of the D-mode load stays constant. Therefore, lower V_{OL} can be achieved by using larger V_{DD} for E/D-mode logic, leading to larger voltage swing and noise margin. When the input is logic 0, the PDN is off. While the PUN in the enhancement-load inverter is always in the saturation regime until input close to $V_{DD} - V_{TE}$, the D-mode GaNFET in the depletion-load (DEP) inverter is now operated in linear

Table 3.1: Comparison of depletion-load inverter and enhancement-load inverter at various V_{DD} with a fixed width ratio of 1:3.

V_{DD} (V)	Properties	D-Load	E-load
3.5	Voltage Swing (%)	88.26	67.29
	Noise Margin (%)	66.26	35.57
	Ave. t_p (ps)	122.9	158.8
	Ave. Total Power (mW)	1.369	1.147
4.0	Voltage Swing (%)	90.20	68.83
	Noise Margin (%)	70.95	36.52
	Ave. t_p (ps)	134.1	114.5
	Ave. Total Power (mW)	1.569	1.729
4.5	Voltage Swing (%)	91.53	70.00
	Noise Margin (%)	74.42	38.00
	Ave. t_p (ps)	145.2	97.87
	Ave. Total Power (mW)	1.770	2.427
5.0	Voltage Swing (%)	92.54	70.94
	Noise Margin (%)	77.14	39.44
	Ave. t_p (ps)	155.4	88.91
	Ave. Total Power (mW)	1.970	3.240

regime. Therefore, the E/D-mode has better noise margin and voltage swing than the E/E-mode logic as shown in Table 3.1.

Large V_{DD}, however, also brings out the larger propagation power consumption. The power consumption (P_{tot}) is calculated by:

$$P_{tot} = \alpha E_{trans} \cdot f_{out} + D_{OL} \cdot P_{stat} \tag{3.5}$$

where α is the probability of each transition case, E_{trans} is the averaged transition

energy, f_{out} is the frequency of output signal, D_{OL} is the duty cycle of output voltage in low state, and P_{stat} is the static power consumed by the inverter. Here, α is set to 0.25 and f_{out}, D_{OL} are set to 125 MHz and 0.5, respectively. The total power consumption is dominated by the static power consumption when input is logic 1. As V_{DD} increases, the E/D-mode inverter has constant static current, while the E/E-mode has the static current proportional to V_{DD}^2. Therefore, the E/D-mode inverter compared to the E/E-mode couterpart has less power consumption at higher V_{DD}. Meanwhile, the average propagation delay is dominated by the PUN (t_{pLH}) due to the nature of n-FET-only logic. The E/E-mode inverter has better propagation delay, especially at higher V_{DD}. Results of WR sweep is shown in Table 3.2. As WR increases, the ON-resistance of PUN in both inverters decreases when the input is logic 1, thus improving the voltage swing and noise margin; the power consumption of inverters, however, also increases due to the larger static current. Besides, ON-resistance of PUN of two inverters is independent on WR while the parasitic capacitance becomes larger as WR increases, making t_{pHL} as well as the averaged propagation delay larger.

Considering that the functionality of the inverter is very sensitive to voltage swing and noise margin, E/D-mode logic should be more favorable than E/E-mode logic in order to achieve stable operation from RT to HT. Besides, since larger V_{DD} and WR give a larger voltage swing and noise margin, 5 V V_{DD} and 1:3 WR will be used in the later section; here 1:4 WR is not used since it requires 25% more area but only provides 2.5% more noise margin comparing to 1:3 WR. The 1:2 WR is not chosen

Table 3.2: Comparison of depletion-load inverter and enhancement-load inverter at various width ratios (WRs) at $V_{DD} = 5$ V.

WR	Properties	D-Load	E-load
1:2	Voltage Swing (%)	88.76	66.32
	Noise Margin (%)	70.04	30.84
	Ave. t_p (ps)	139.4	80.35
	Ave. Total Power (mW)	1.970	2.925
1:2.5	Voltage Swing (%)	91.04	69.98
	Noise Margin (%)	73.48	35.38
	Ave. t_p (ps)	148.1	84.65
	Ave. Total Power (mW)	1.973	3.106
1:3	Voltage Swing (%)	92.54	70.94
	Noise Margin (%)	77.14	39.44
	Ave. t_p (ps)	155.4	88.91
	Ave. Total Power (mW)	1.970	3.240
1:4	Voltage Swing (%)	94.42	75.54
	Noise Margin (%)	79.08	46.38
	Ave. t_p (ps)	167.3	96.5
	Ave. Total Power (mW)	1.978	3.424

due to poor tolerance of different process corners.

Depletion-load *vs.* Pass Transistor Logic

According to results from previous section, a NAND gate is built based on the depletion-load logic (DPL) with a 6 µm D-mode n-FET as PUN and two series-connected 18 µm E-mode n-FETs as PDN. For a pass transistor logic (PTL)-based NAND, two 6 µm E-mode n-FETs are used as the pass transistor (one for passing the input signal, one for preventing the floating node) and a standard 1:3 DPL inverter

Table 3.3: Comparison of NAND gate based on DPL and PTL from RT to 327 °C

T (°C)	Properties	D-Load	E-load
27	Voltage Swing (V)	4.249	4.627
	Ave. t_p (ps)	264.7	320.1
	Ave. Total Power (mW)	2.030	2.035
127	Voltage Swing (V)	4.244	4.626
	Ave. t_p (ps)	391.4	496.4
	Ave. Total Power (mW)	1.423	1.415
227	Voltage Swing (V)	4.185	4.598
	Ave. t_p (ps)	592.4	752.1
	Ave. Total Power (mW)	0.958	0.943
327	Voltage Swing (V)	4.125	4.569
	Ave. t_p (ps)	871.0	1077.3
	Ave. Total Power (mW)	0.658	0.638

to achieve a better voltage swing. Simulation results are listed in Table 3.3. Both NAND gates can work reliably from RT to HT with a stable voltage swing. However, due to the nature of PTL, the internal nodes can only be pulled up to $V_{DD} - V_{TH,E}$, resulting in a smaller noise margin. The DPL is chosen because of smaller propagation delay, better noise margin, despite of the larger area overhead. The increase of t_p and decrease of P are attributed to the increase of R_{on} of GaN FETs due to the higher lattice scattering at elevated temperature.

3.3.2 Sequential Logic

Area

As seen in Fig. 3-4, schematic Reg A has 16 transistors, Reg B has 12 transistors, and Reg C has 14 transistors, respectively. The numbers labeled on the component are the device dimensions (W) normalized to the minimum device width (6 µm). The Reg A has an estimated area of 29, while Reg B is 20 and Reg C is 34. Widths can be optimized for low power or high speed. It is worth mentioning that Reg A is similar to SR-latch which is ratioed. Strong driving transistors are required to overpower the cross-coupled inverters.

Power

Total power of depletion-load n-FET-only logic can be divided into static power and switching power. 8 different tests as shown in Fig. 3-6(a) are performed on all the registers at RT and 300 °C with clock frequency from 10 MHz to 33.3 MHz. The results are shown in Fig. 3-6(b-c). $V_{DD} = 5$ V is applied here and for the subsequent simulations.

Over 98% of power is from static power at the RT consumed by inverters. Reg A has higher static power than the other two designs due to its high inverter numbers. As expected, switching power is sensitive to the data and clock activity and increases linearly with the frequency. It almost stays constant over a wide temperature range due to the constant capacitance. Static power decreases as the temperature increases

due to lower on-current. Power consumption can be further reduced by reducing the number of inverters and resizing them to an optimum value.

Time Constraint

Here the basic timing parameters including setup time, hold time, CLK to Q time and its value with the presence of clock skew of each register were compared. Typically, the simulation is just needed at the highest designated working temperature, where worst cases happen due to the highest delay as the consequence of reduction in mobility and increase of contact resistance over temperature. The simulation is limited to 300 °C in this section due to the lack of experimental results of complex memory cell over 300 °C, which will be demonstrated in the next chapter. As shown in the Fig. 3-5, Reg A has the highest t_{su} of 6-7 ns based on transition type due to its SR-latch like mechanisms. It needs to overpower the cross-coupled inverters to flip the stored signal. While the Reg B and Reg C have similar t_{su} of 2-3 ns due to their similar feedback path. All three designs without input buffers have the same $t_h = 0$. Regarding clk to q time, Reg A has the highest t_{cq} of 3.7-4.7 ns as well due to the same reason as described in t_{su}, while the Reg B and Reg C has t_{cq} of 1.5-2 ns and 1.7 ns, respectively. It is worth mentioning that, due to the asymmetric delay time design, timing parameters here are data dependent. All the timing parameters can be adjusted based on need, such as inserting input buffers to increase t_{su} and decrease t_h . The tradeoff is power and area.

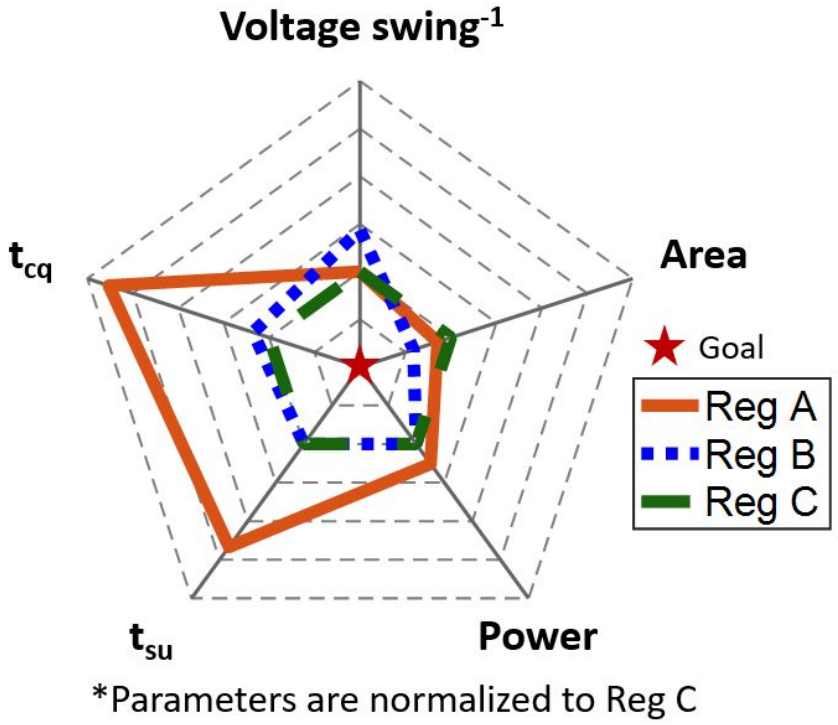


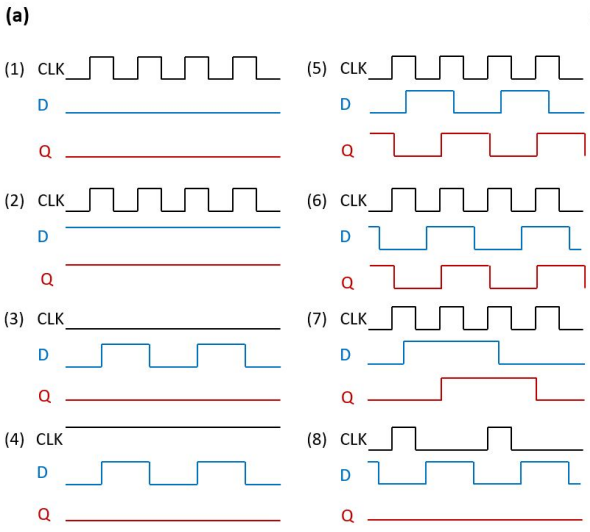
Figure 3-5: Benchmark of (a) SSAFF, (b) PTFF, (c) DLMFF.

When there is clock skew, there is a certain limit of skew time:

$$t_h > t_{skew} > -t_{D-Q,1st-latch}$$

Voltage Swing and Benchmark

All the nodes in Reg A and Reg C have a nearly full swing of 4.6 V, while the Reg C has a lowest voltage swing of 3.6 V due to pass transistors. All three designs are benchmarked in Fig. 3-5. Reg C is the optimal choice due to high voltage swing while keeping power and delay low.



(b) Total Power Consumption (Unit: mW)

27°C CLK: T=100n

	Reg#1	Reg#2	Reg#3
1	7.59	7.59	7.59
2	11.39	7.59	7.59
3	9.57	7.61	7.63
4	9.51	7.59	7.59
5	9.65	7.64	7.67
6	9.64	7.64	7.67
7	9.63	7.60	7.61
8	9.57	7.61	7.63

300°C CLK: T=100n

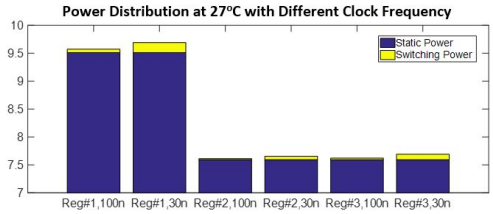
	Reg#1	Reg#2	Reg#3
1	2.67	2.67	2.67
2	4.01	2.67	2.67
3	3.43	2.69	2.71
4	3.36	2.67	2.67
5	3.53	2.73	2.75
6	3.52	2.73	2.75
7	3.42	2.68	2.69
8	3.44	2.70	2.72

27°C CLK: T=30n

	Reg#1	Reg#2	Reg#3
1	7.59	7.59	7.59
2	11.39	7.59	7.59
3	9.73	7.66	7.73
4	9.51	7.59	7.60
5	10.00	7.76	7.84
6	9.97	7.76	7.83
7	9.6	7.63	7.66
8	9.73	7.66	7.73

300°C CLK: T=30n

	Reg#1	Reg#2	Reg#3
1	2.67	2.67	2.67
2	4.01	2.67	2.67
3	3.65	2.75	2.8
4	3.38	2.67	2.68
5	3.95	2.85	2.92
6	3.93	2.85	2.91
7	3.49	2.71	2.74
8	3.65	2.75	2.81



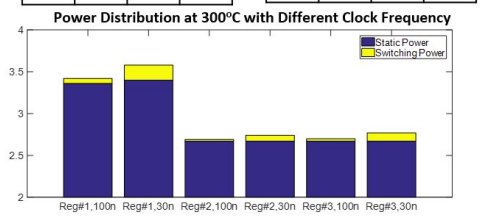


Figure 3-6: (a) 8 test conditions with different data/clk activity; (b) Total power at different temperatures and clk frequency, (c) Average power distribution of three designs.

3.3.3 Experimental Verification

In spite of the excellent fitting results of DC characteristics shown in Fig. 3-1 and 3-2 up to 500 °C. They offer little indication of the accuracy of transient simulation. In order to validate the potential of our compact models for complex circuit simulation, the experimental data was compared to the simulation results in terms of both DC and transient performance. Two representative circuit building blocks were explored, namely inverter (combinational logic) and Data Flip-Flop (sequential logic / memory) using E/D-mode n-FET-only logic.

The simulated and measured VTC of a E/D-mode inverter with a V_{DD} of 5 V and $\beta = 3$ was plotted with a good agreement as shown in Fig. 3-7(a) at room temperature. The variation observed at 500 °C may be attributed to the difference of D-mode transistors. The details of the experimental data will be illustrated in the next chapter. While an excellent fitting of E-mode transistor up to 500 °C was found with extrapolation in the Fig. 3-2, further study is needed on the performance degradation of the D-mode transistor on the proposed monolithic integration platform. A potential explanation is the increased gate leakage current from drain to gate side as the gate and source are shorted in the n-FET-only configuration. The increased D-mode load current leads to the increased V_{OL} and reduced gain.

Direct measurement of the propagation delay t_p of the fabricated inverter was limited to the load impedance introduced from the measurement setup. Therefore a t_p was extracted from the ring oscillators using $t_p = T_{RO}/2N_{stage}$. A great agreement

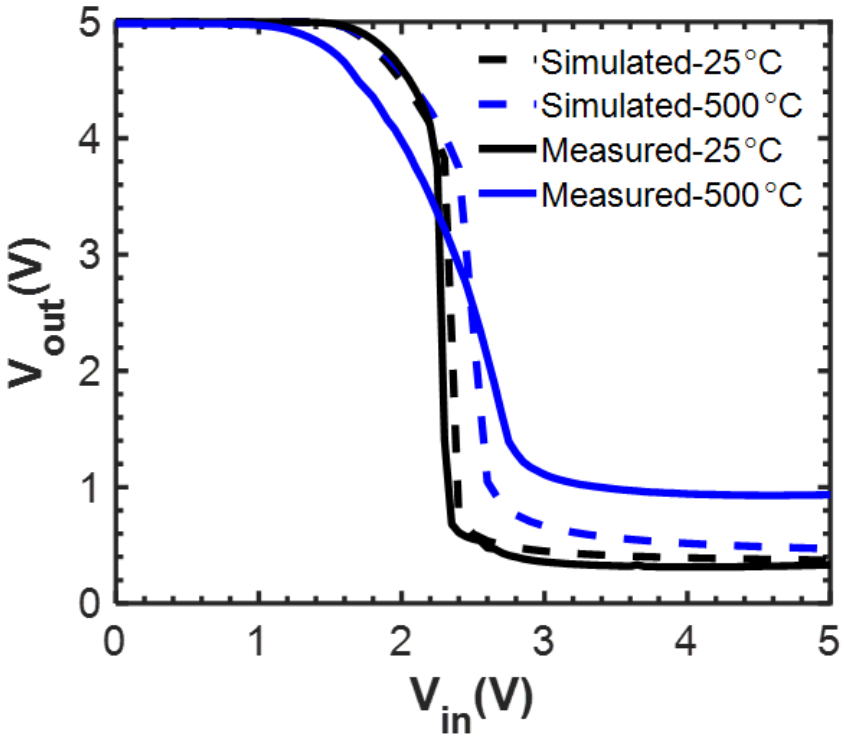


Figure 3-7: Comparison between simulated and experimental voltage transfer curve at room temperature and 500 °C.

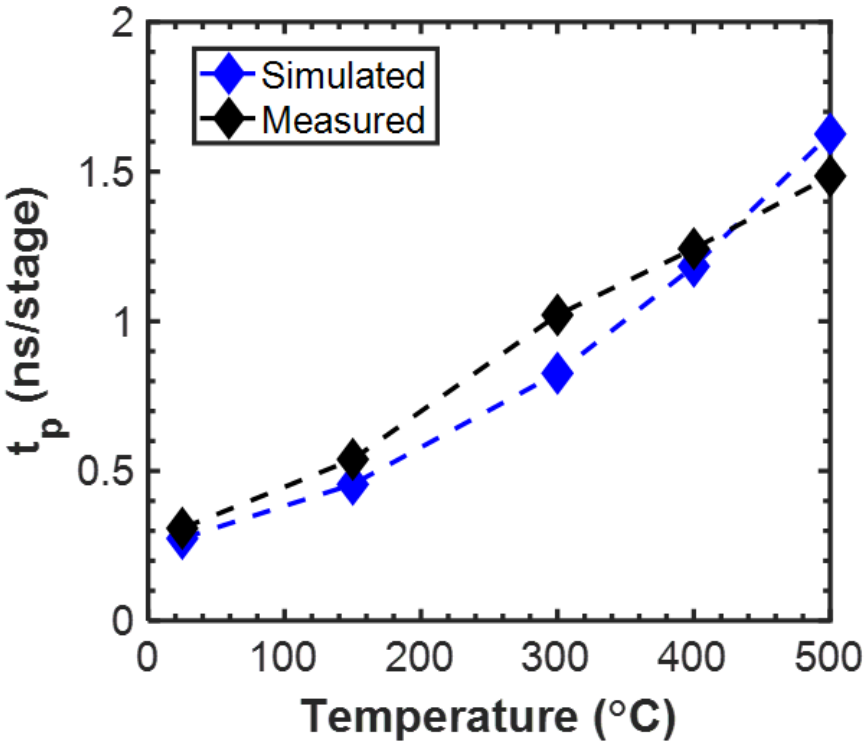


Figure 3-8: Comparison between simulated and experimental propagation delay (t_p) per stage from room temperature up to 500 °C.

between experimental and simulation data was observed in Fig. 3-8. Below 400 °C, the simulated t_p was slightly lower than the measured data, which may be attributed to the extra delay introduced from the parasitics. The lower measured t_p at 500 °C compared to the simulation results was mainly caused by the lower t_{pLH} resulted from the higher D-mode transistor on-current as observed in Fig. 3-7.

To further explore the limit of our compact models, the temperature dependency of t_{su} of Data Flip-Flop (circuit diagram shown in Fig. 3-4(c) with additional input and output buffer) was studied based on both simulation results and experimental data. The details of the measured DFF will be illustrated in the next chapter. As

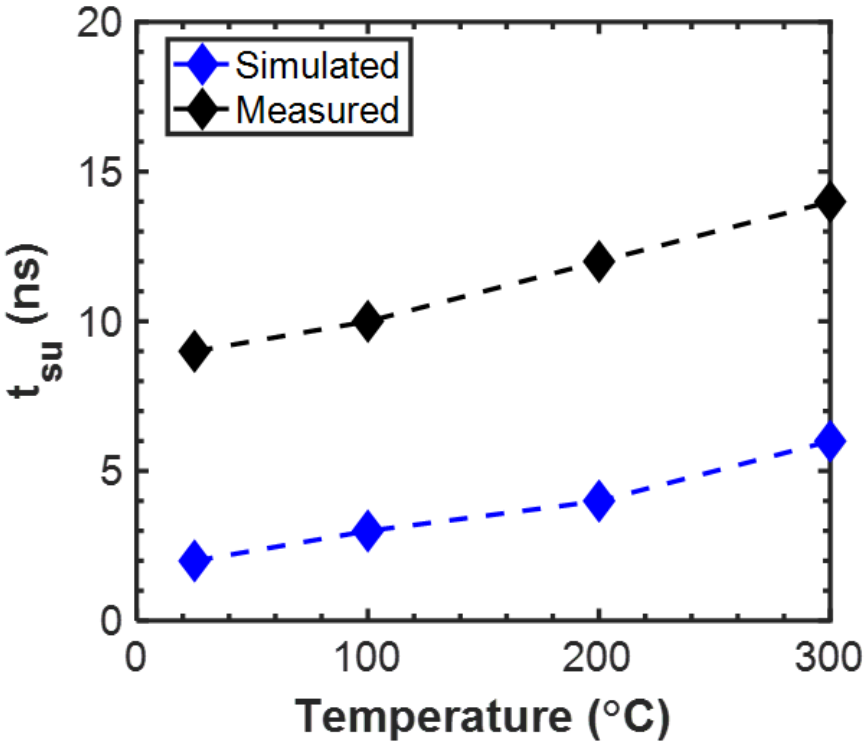


Figure 3-9: Comparison between simulated and experimental setup time (t_{su}) of the DFF from room temperature up to 300 °C.

shown in Fig. 3-9, both the simulation and measurement results show similar temperature dependency. However, the simulation results is significantly lower than the measurement results for around 6 ns. The discrepancy may be attributed to the parasitics introduced by the layout. Compared to the compact layout design of the ring oscillator shown in the Fig. 4-3(a), which showed great agreement with simulated data (Fig. 3-8), the design of DFF (Fig. 4-6) has significantly higher parasitics, leading to a higher extra delay. The results indicate the importance of parasitics extraction.

3.4 Conclusion

In chapter 2, a HT GaN technology was demonstrated, namely, the monolithic integration of E/D-mode n-FETs with self-aligned gate-first process, and refractory metal contact. This chapter extends our HT technology from device to circuit level, and present a thorough analysis to explore the design space of GaN digital circuit from RT to HT based on the n-FET only logic. Different V_{DD}, WR, and implementation of both combinational and sequential logic were compared, in terms of power, area, t_p, noise margin, voltage swing. In general, depletion-load design is more favorable than enhancement-load design; among different register implementations, the depletion load multiplexer flip-flop is preferred choice due to its low power, area, and good tolerance of different design corners.

To validate the compact models, the difference between experimental data and simulation results based on the proposed simulation framework was explored. A great agreement was observed between the simulation and measurement of simple building blocks such as inverters and ring oscillators, while further study of the D-mode transistor behavior at 500 °C is still needed. For a more complicated building blocks like DFF, the simulation still showed a similar trend compared to the measurement, although these results are significantly lower than the measurement results due to the lack of parasitic extraction.

Chapter 4

Experimental Results for High-Temperature GaN Digital Circuits

Chapter 2 reported on the high temperature (HT) robustness of enhancement-mode (E-mode) p-GaN-gated AlGaN/GaN high electron mobility transistors (HEMTs), with an emphasis on the key transistor-level parameters for digital and analog mixed-signal applications. In-situ measurements from room temperature (RT) to 500 °C indicate trends in the V_{th}, R_{ON}, $I_{D,max}$ and $I_{G,max}$ are largely as expected based on first-order changes in the semiconductor properties. The fabricated transistors exhibited stable performance over 20 days at 500 °C. Furthermore, the self-aligned gate-first process shows great scalability and uniformity, paving the way for a complex GaN-

based ICs. In chapter 3, compact modeling of E/D-mode HEMTs was performed with excellent fitting up to 500 °C. A general guideline is given for robustness-driven GaN-based circuit design in the aspects of critical parameters, and topology, which will further advance the VLSI of GaN HT electronics.

4.1 Choice of Inverter Circuit Configuration

As illustrated in Fig. 4-1(a), the wafer platform used in this work is p-GaN/AlGaN/GaN-on-Si and allows for the monolithic integration of two types of transistors, E-mode p-GaN-gate AlGaN/GaN HEMTs and D-mode AlGaN/GaN HEMTs, using the process flow described in chapter 2. Here, HT transistors with refractory metal gate and self-alignment in p-GaN-gate were fabricated. The typical transfer characteristics of the E-mode and D-mode transistors are shown in Fig. 4-1(b). Good ON-OFF ratio ($> 3 \times 10^7$, limited by gate leakage) and V_{th} of +1.4 V at room temperature are obtained for the E-mode transistors. The D-mode transistor shows a V_{th} of -1 V.

In order to identify the optimal implementation of the GaN high temperature logic, the characteristics of two classic inverter configurations (E/D-mode and E/E-mode inverters) (Fig.4-1(c)) were experimentally evaluated at high temperature. In principle, the E/E-mode inverter offers: (1) higher simplicity, (2) higher current, and (3) higher speed at higher V_{DD}, while the E/D inverter features (1) lower power consumption, (2) better gain, voltage swing (V_{swing}), and noise margin (NM), and (3) higher speed at lower V_{DD}.

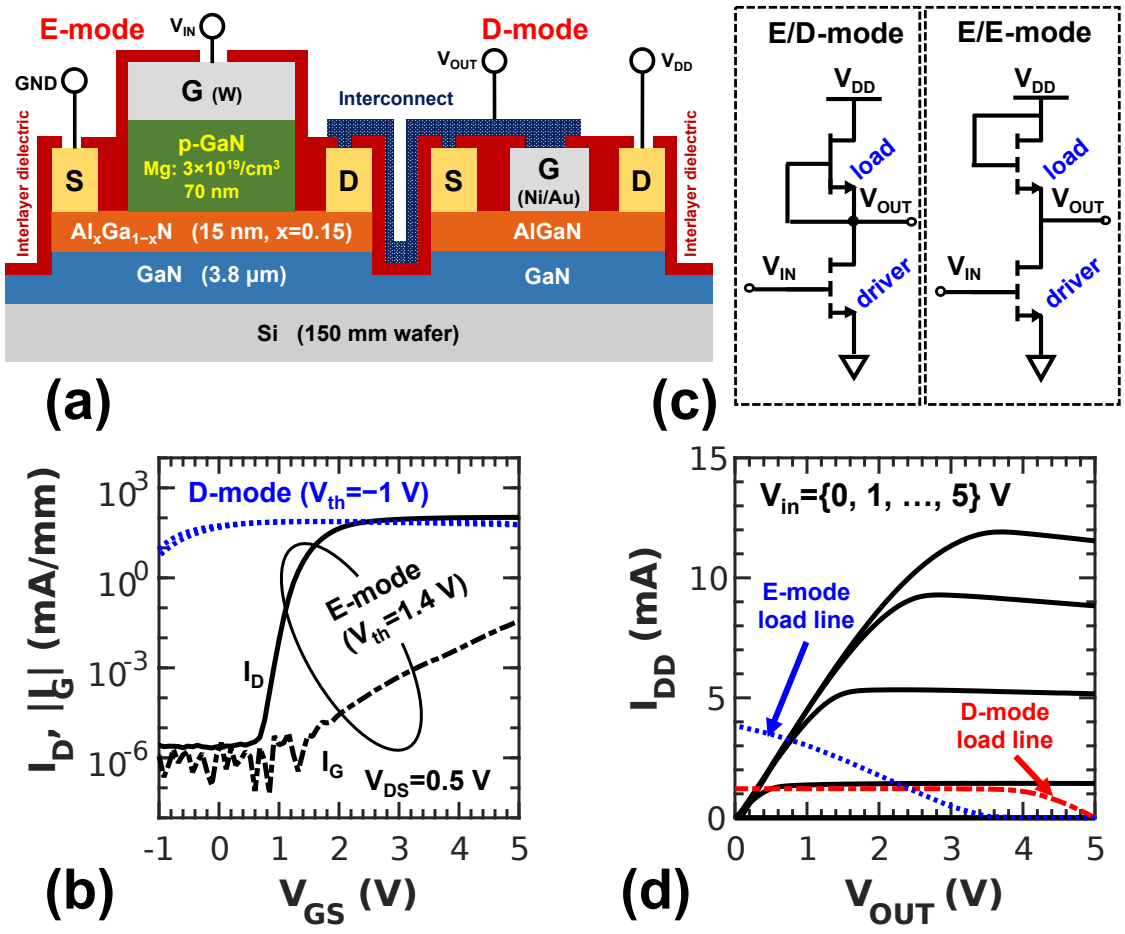


Figure 4-1: Transistor technology and circuit configurations of n-FET only logic. (a) Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter. (b) Typical transfer characteristics. (c) Circuit configurations of E/D-mode and E/E-mode logic. (d) IV curves of an E-mode transistor ($W/L = 36/2$ µm/µm). $I_{D,max} = 330$ mA/mm, $R_{ON} = 12$ Ω·mm (measured at $V_{GS} = 5$ V). The load line, realized using a either D-mode or E-mode transistor ($W/L = 12/2$ µm/µm), is also included.

A comparison of the voltage transfer curves (VTCs, Fig. 4-2(a)) at 300 °C reveals that, the E/D-mode inverter features significantly better performance than the E/E-mode inverter, in terms of $V_{swing}\,(= V_{OH} - V_{OL})$, gain, and NM. This is because: (1) In E/D-mode, $V_{OH} = V_{DD}$, whereas in E/E-mode, $V_{OH} = V_{DD} - V_{th(E)}$; (2) In both circuit configurations, V_{OL} is limited by the voltage drop across the E-mode driver. While the R_{ON} of both drivers is similar, the current drive of the E-mode load (diode-connected), when input is HIGH, is significantly stronger than that of the D-mode load (GS-tied) (Fig. 4-1(d)).

The above observations are also valid with the scaling of V_{DD}, an important design parameter in digital circuits (Fig. 4-2(b)–(c)). With the increase in V_{DD}, the V_{swing} of E/D-mode and E/E-mode inverters generally improves. However, the magnitude of improvement is better for the E/D-mode, thanks to the constant V_{OL} across different V_{DD}. When the output is LOW, the R_{ON} of the E-mode driver is almost independent of V_{DD} (Fig. 4-1(d)). To first order, the D-mode load supplies a constant current, compared to the current of E-mode load with V_{DD}^2 dependency, leading to a better V_{OL} at higher V_{DD}.

Having established that E/D-mode technology offers significantly better performance in GaN digital circuits at 300 °C, the temperature dependence of E/D-mode was further studied for higher temperatures. Measurements beyond 300 °C were conducted using a probe station with a hot chuck (maximum rating of 500 °C) and sealed chamber in N_2 ambient. As presented in Fig. 4-2(d), the VTC of the E/D-mode re-

mains largely constant up till 400 °C, though NM_L is reduced slightly (by ∼0.15 V) due to the faster degradation in the ON-resistance of the E-mode driver transistor than in the D-mode load transistor. At 500 °C, an increase in V_{OL} (hence reduction of V_{swing} by 0.6 V_{PP}) was observed, which can also be explained by the faster degradation of the E-mode device ON-resistance.

4.2 GaN Ring Oscillators Operational at 500 °C

In order to estimate the t_p of the proposed GaN E/D-mode technology, ROs were fabricated with $(W/L)_{\{E,D\}} = \{36/2, 12/2\}$ µm/µm (Fig. 4-3(a)). The V_{DD} scaling trends of ROs were compared at 25 °C (Fig. 4-3(b)). The t_p may be modeled as $\frac{1}{2}C_L \times V_{DD}/I_{ave}$, where C_L is the load capacitance, and I_{ave} is the average charge/discharge current. To first order, the charge current through the D-mode load is constant with V_{DD} (refer to Fig. 4-1(d)), therefore t_p from LOW to HIGH (t_{pLH}) is proportional to V_{DD}. The discharge current through the E-mode driver, same as Si CMOS circuits, is roughly proportional to V_{DD}^2, therefore $t_{pHL} \propto 1/V_{DD}$. Due to the significantly lower charge current, t_{pLH} dominates t_p. Hence, a lower V_{DD} results in a lower t_p. However, the reduction of V_{DD} results in trade-offs in NM and V_{swing} (Fig. 4-2(c)–(d)). Therefore, V_{DD} of 5 V was chosen for the RO as a compromise.

The ROs were operational at 500 °C, as shown in Fig. 4-3(c). The degradation of t_p from 0.31 ns/stage (25 °C) to 1.48 ns/stage (500 °C) (Fig. 4-3(d)) may be attributed to the performance degradation of both E/D-mode transistors (increase in

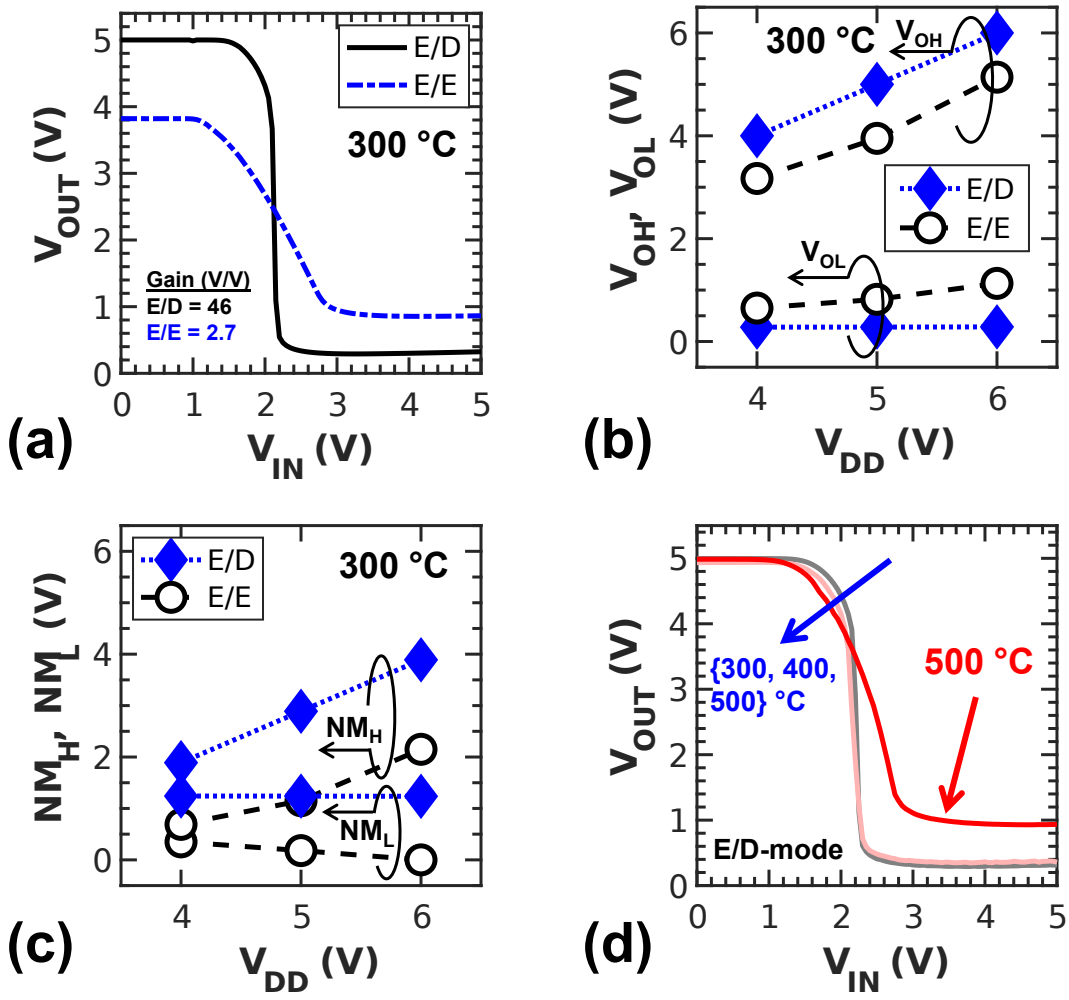


Figure 4-2: Comparison of E/D-mode and E/E-mode inverters. (a) VTC at 300 °C. Maximum voltage gains of E/D-mode and E/E-mode are 46 V/V (at V_{in} = 2.1 V) and 2.7 V/V (at V_{in} = 2.6 V), respectively. (b) $V_{swing} = V_{OH} - V_{OL}$ *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. (c) Noise margins (NM_L, NM_H) *vs.* V_{DD} for E/D-mode and E/E-mode at 300 °C. (d) VTC of E/D-mode up to 500 °C.

R_{ON} of the E-mode driver, reduction in current drive capability of the D-mode load) and an increase in parasitics.

The reported RO was benchmarked against other ROs based on wide band gap electronics (GaN [8, 7, 9, 10, 11, 12, 13] and SiC [14, 15, 3, 16]). As shown in Fig. 4-4(a), to the best of the author's knowledge, at room temperature, the proposed technology sets a new boundary of t_p *vs.* L_G^2, which typically follows the well-known relationship of $t_p \propto L_G^2$ [82]. Furthermore, as shown in Fig. 4-4(b), the reported RO is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology, which is based on p-GaN-gate AlGaN/GaN HEMTs optimized for HT ($\geq$ 500 °C) applications. The measured t_p of 1.48 ns/stage should be considered as an upper limit for the actual t_p, given that it is widely known and as verified in Fig. 4-3(d), ROs with more stages would give a more accurate estimation of the intrinsic t_p. In this experiment, the number of stages in the RO was limited by the uniformity and yield of the process flow.

A systematic study of E/D-mode and E/E-mode inverters based on a HT optimized E-mode GaN-on-Si platform was conducted. E/D-mode inverters were found to offer significantly higher performance than E/E-mode inverters at 300 °C. The reported RO set a new boundary for the t_p *vs.* L_G^2 at room temperature, and revealed an intrinsic $t_p < 1.48$ ns/stage at 500 °C with $L_G = 2$ µm. Further advancement of the proposed technology, for example by aggressive channel length scaling and HT-rated

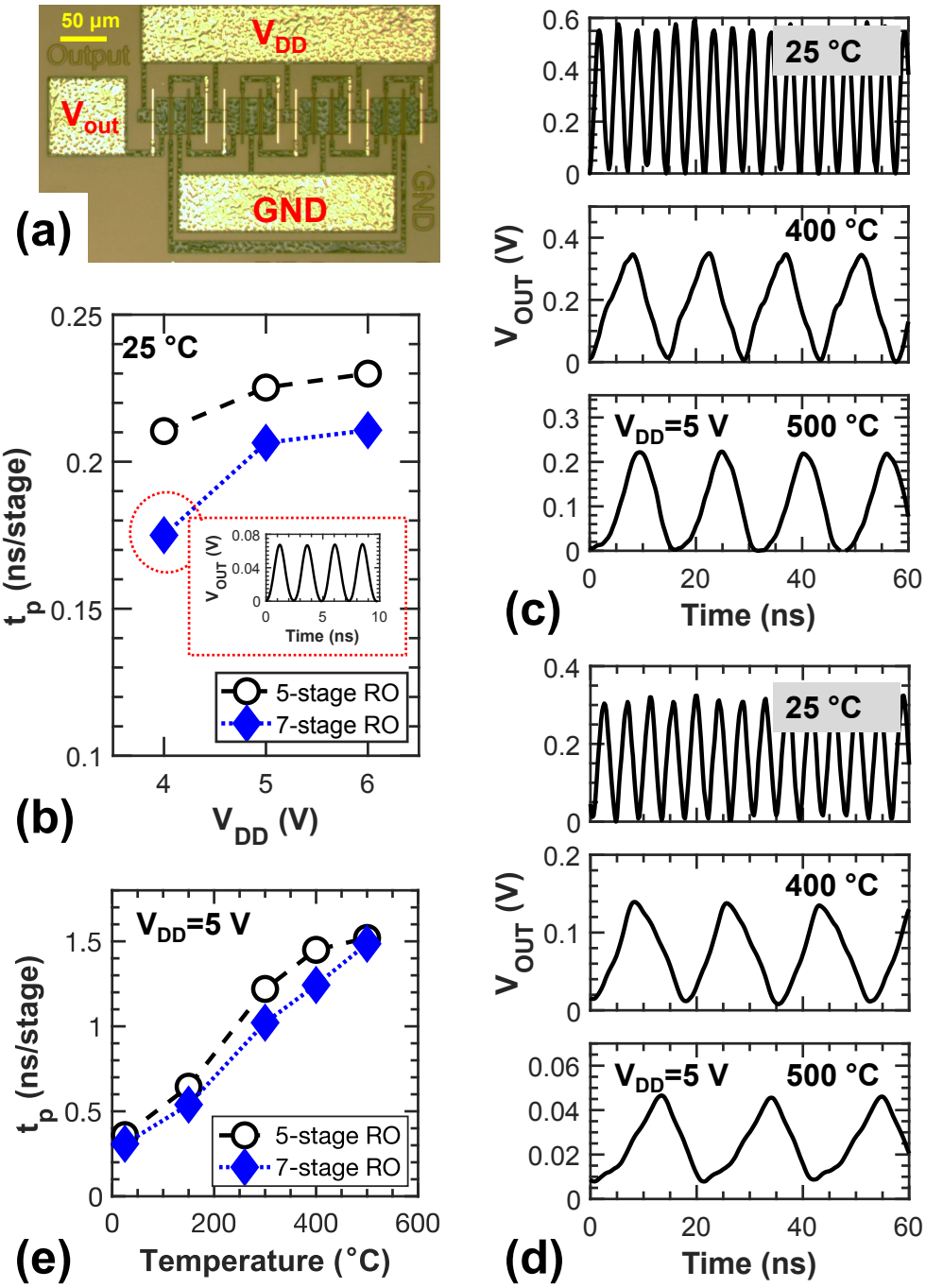


Figure 4-3: GaN ring oscillators (RO). (a) Micrograph of a 7-stage RO. (b) V_{DD} scaling trend of RO oscillation frequency at 25 °C. (c) Waveforms of a 5-stage RO at various temperatures. (d) t_p estimated from the waveforms of a 5-stage RO and a 7-stage RO. In the above measurements, $V_{DD} = 5$ V.

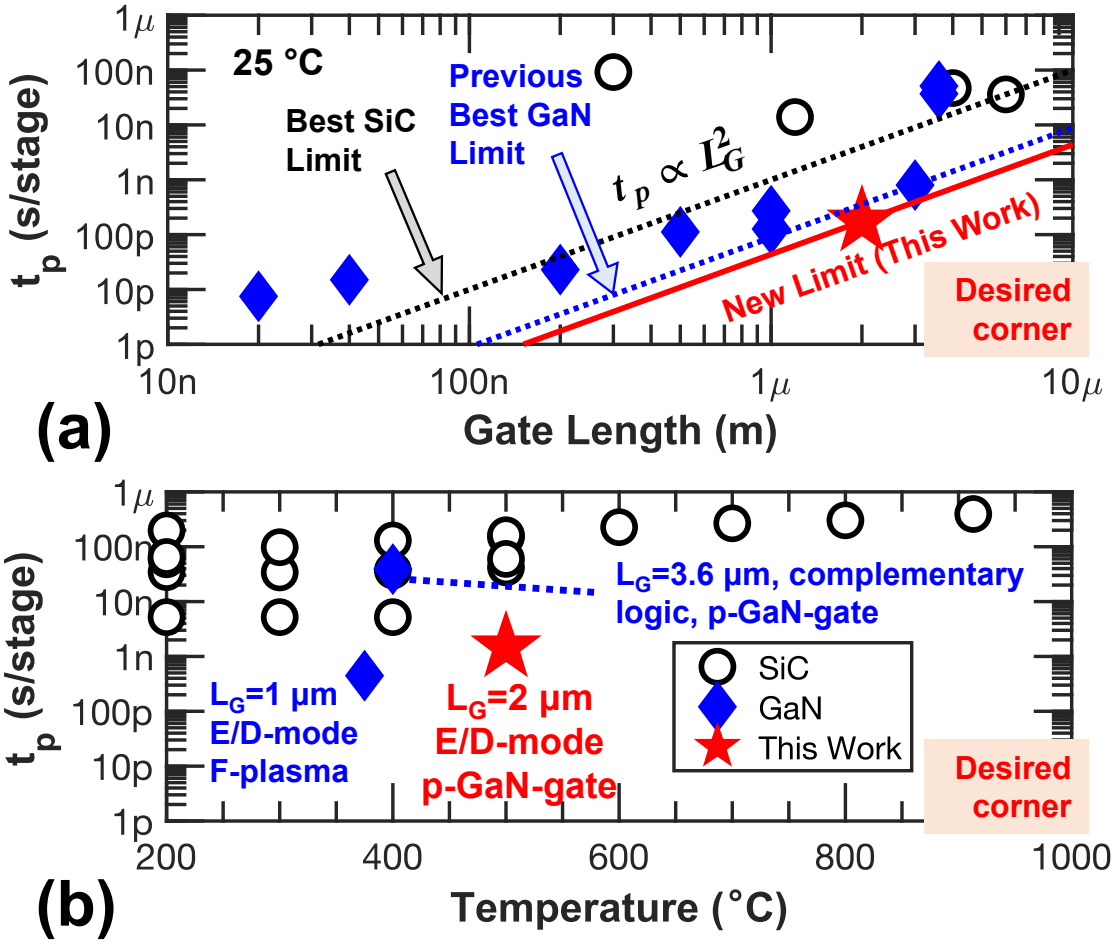


Figure 4-4: A summary of ROs reported in the literature based on wide band gap electronics (GaN [8, 7, 9, 10, 11, 12, 13] and SiC [14, 15, 3, 16]). (a) t_p *vs.* L_G. The general scaling trends ($t_p \propto L_G^2$) for the best SiC demonstration, previous best GaN demonstration and the best result of this work (Fig. 4-3(b) inset) are included for reference. The L_G of the pull-down transistor is chosen. (b) t_p *vs.* temperature. The data points showing GaN RO demonstrations are labelled with the L_G of the pull-down transistor, the logic family/circuit configuration and the type of E-mode n-FET. To the best of the author's knowledge, the proposed technology in this work defines a new boundary of t_p *vs.* L_G^2, as well as the operating temperature of GaN digital circuits.

advanced packaging [83], would significantly push GaN HT electronics to new limits.

4.3 GaN Memory Operational at 300 °C

The memory cells were implemented based on the proposed GaN-on-Si platform using monolithically integrated E/D-mode n-FETs only logic with V_{DD} = 5 V, and $(W_G/L_G)_{\{E,D\}} = \{36/2, 12/2\}$ µm/µm, yielding a drive/load ratio $\beta = (W/L)_{\mathrm{E}}/(W/L)_{\mathrm{D}} =$ 3. All the memory cells were measured up to 300 °C on a probe station with a hot chuck. The schematic of those cells are presented in chapter 3.

A 32 bit × 10 bit NOR-based mask ROM array is constructed as shown in Fig. 4-5(a) with a total number of 350 transistors. The 1$^{\mathrm{st}}$ 10-bit instruction is enabled. The measured output matched the expected instruction with $BL[0:9] = [1000110001]$ at 300 °C (Fig. 4-5(b)). The maximum voltage of the output is limited to 4.5 V due to the static-current induced voltage drop (IR drop) through the interconnect. The minimum voltage is above 0 V due to the nature of n-FET-only logic.

The core unit of a standard 6T-SRAM is constructed from a pair of cross-coupled E/D-mode inverters as shown in Fig. 4-5(c) without two extra transistors for word line control. A voltage source is first applied to input with V_{IN} = 0 V at $t = -50$ ms, driving V_{OUT} to logic state '1' ($\sim$ 4.2 V) as shown in Fig. 4-5(d). At $t = 0$, the V_{IN} = 5 V is then applied to the input to write a logic state '0' ($\sim$ 0.5 V) into V_{OUT}. The above results demonstrate that the 4T-SRAM cell fabricated on the proposed platform functions as a stable memory cell at 300 °C.

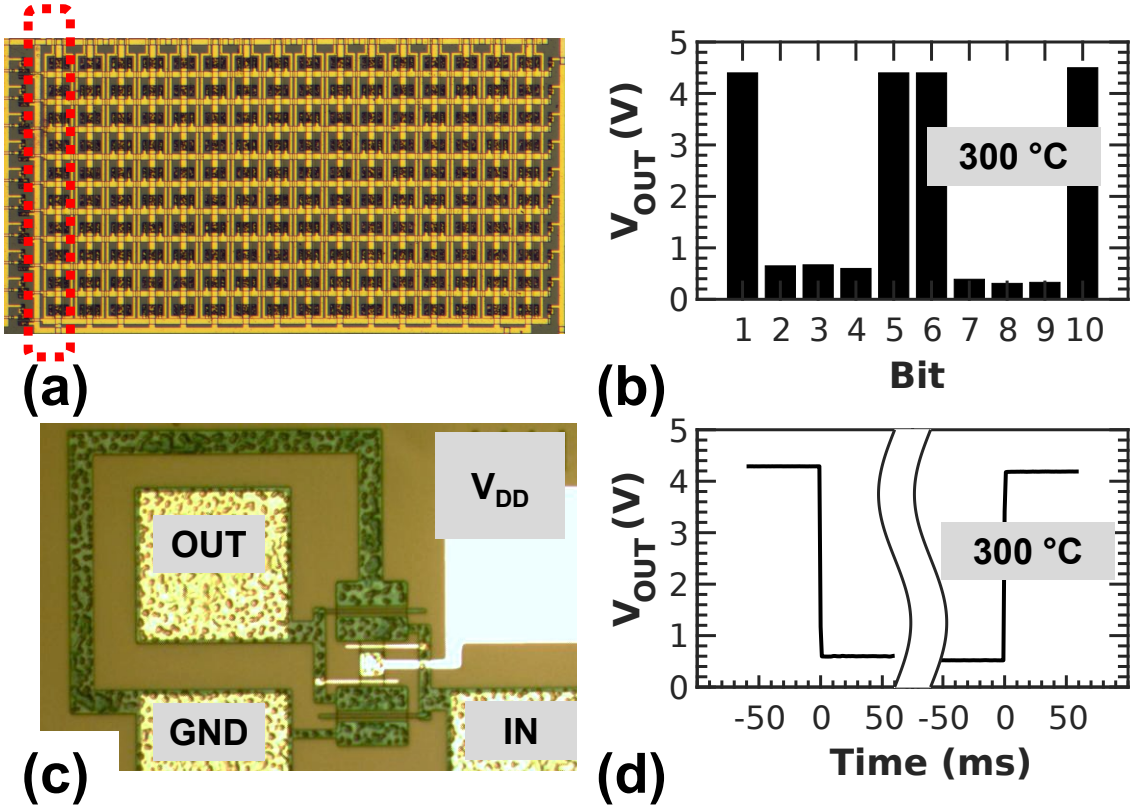


Figure 4-5: GaN ROM and 4T-SRAM. (a) Micrograph of a 32-bit × 10-bit NOR-based ROM array. (b) The measured output of the 1st instruction stored in the ROM. (c) Micrograph of a 4-transistor SRAM. (d) Waveform of SRAM operating at 300 °C with input transition from logic state '1' to '0' (left) and '0' to '1' (right).

Table 4.1: Summary of published GaN FFs.

Ref.	**Semiconductor**	**Driver (Transistor)**	**Logic Family**	L_G **(µm)**	V_{DD}/V_{SS} **(V/V)**	**Temp. (°C)**	f_{CLK} **(MHz)***
[84]	GaN	F implanted HEMT	E/D-mode, DCFL	0.8	+2/GND	25	–
[85]	GaN	–	E/D-mode, DCFL	1.2	+12/GND	25	10
[60]	GaN	Conventional HEMT	D-mode, RTL	0.5	$+14/-14$	25 160	2.5 1.6
[61]	SiC	MESFET	D-mode, RTL	2	$+5/-12$	300	–
[42]	SiC	JFET	D-mode, RTL	6	$+25/-25$	500	–
[86]	SiC	MOSFET	E/D-mode, DCFL	–	+20/GND	300	–
This Work	GaN	p-GaN gate	E/D-mode, DCFL	2	+5/GND	25 300	55 36

DCFL: direct coupled FET logic; RTL: resistor-transistor logic. * Estimated lower bound value.

A multiplexer-based negative D latch is constructed with input and output buffer (Fig. 4-6(a)). A total of 13 transistors were used in this implementation. As shown in Fig. 4-6(c), the latch becomes transparent while CLK is LOW, and holds its value while CLK is HIGH with $f_{CLK} = 1$ kHz and $f_{DATA} = 1.5$ kHz. Furthermore, A positive DFF is constructed using a *primary-secondary* (*master-slave*) configuration with a total of 20 transistors. For the fabricated positive flip-flop, the value of output (Q) is the value of input (D) sampled at the rising edge of CLK as shown in Fig. 4-6(c). A large voltage swing over 4 V can still be achieved for both D latch and DFF at 300 °C due to the matched temperature behaviour of on-resistance for both E/D-mode transistors.

To evaluate the performance of the DFF across temperature, setup time (t_{su}), an important metric to estimate maximum clock frequency ($f_{CLK} \approx 1/(t_{cq} + t_{su})$), was characterized up to 300 °C, while the measurement of CLK to Q time is limited due to the large load capacitance (350 pF) introduced by the measurement setup. Based on the schematic of the fabricated DFF, the estimated value of t_{cq} should be similar to the value of t_{su}, and thus $f_{CLK} = 1/(2 \times t_{su})$ is used to estimated the maximum clock frequency.

t_{su} increased from 9 ns to 14 ns, leading to a decrease of f_{CLK} from 55 MHz to 36 MHz (all values from 25 °C to 300 °C). The decrease in performance is mainly due to the reduction of channel mobility and increase in parasitics at higher temperatures.

A summary of the GaN- and SiC-based FFs is presented in Table 4.1. The re-

ported DFF prototype based on the proposed GaN HT-robust technology features a simple bias condition and competitive performance at room temperature, and to the best of the author's knowledge, is operational at the highest temperature among all the GaN-based FFs. The f_{CLK} may be further improved with advancement in the proposed technology by aggressive channel length scaling, optimized layout and advanced packaging [**?**].

4.4 Conclusion

In this chapter, first, a systematic study of E/D-mode and E/E-mode inverters based on a HT optimized E-mode GaN-on-Si platform was conducted. E/D-mode inverters were found to offer significantly higher performance than E/E-mode inverters at 300 °C. The reported RO set a new boundary for the t_p *vs.* L_G^2 at room temperature, and revealed an intrinsic $t_p < 1.48$ ns/stage at 500 °C with $L_G = 2$ μm. Further advancement of the proposed technology, for example by aggressive channel length scaling and HT-rated advanced packaging [83], would significantly push GaN HT electronics to new limits.

Furthermore, a comprehensive study of four most commonly used implementations for memory cells, namely ROM, SRAM, D latch, DFF was conducted for high temperature (HT, up to 300 °C) GaN-based digital circuits. A HT-robust technology with improved uniformity ($\sigma(V_{TH}) < 0.1$ V, and $\sigma(I_{D,max}) = 40$ mA/mm, E-mode) was proposed and used to implement those memory cells. To the best of the author's

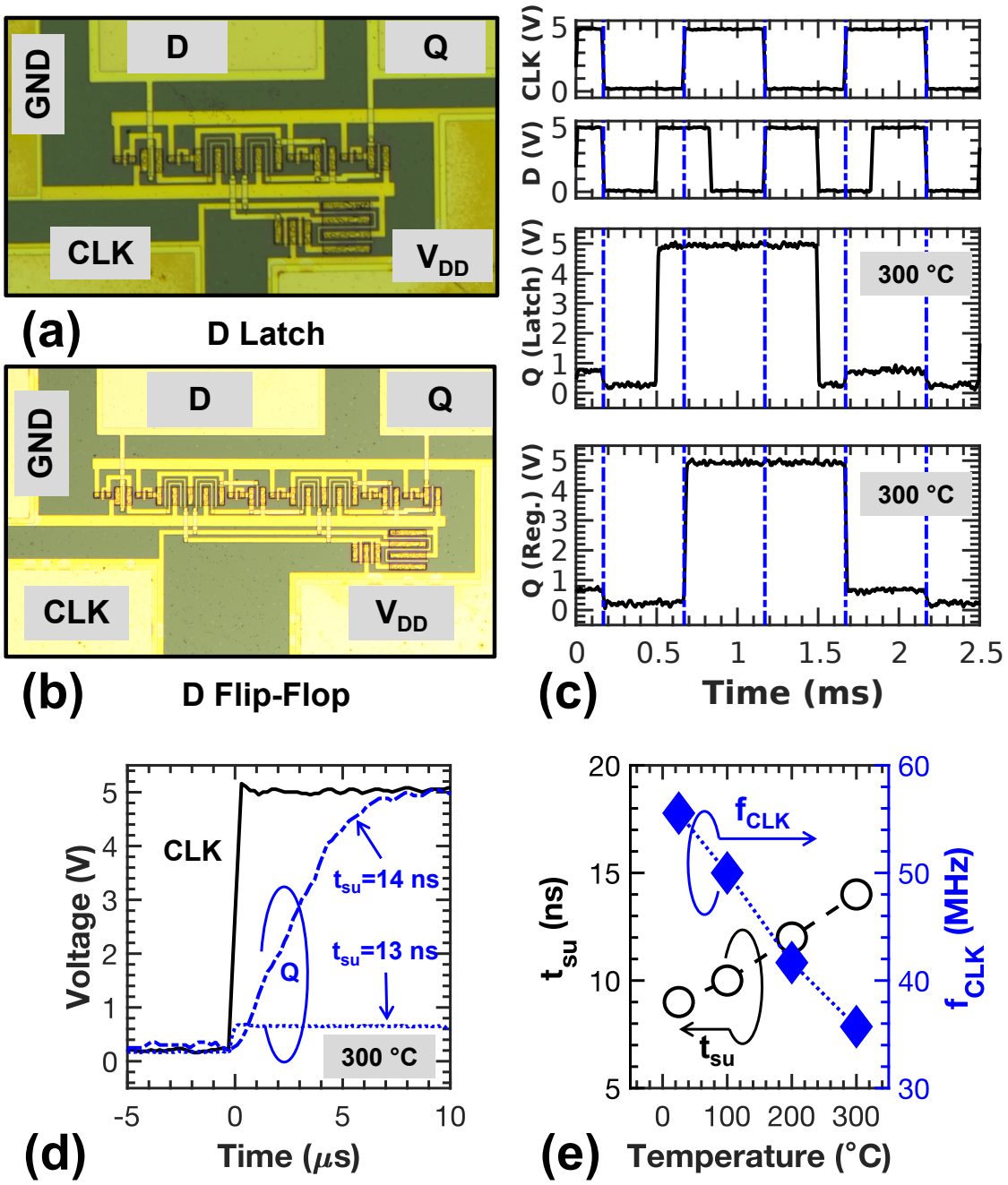


Figure 4-6: GaN negative D latch and positive DFF. (a) Micrograph of a negative multiplexer-based latch. (b) Micrograph of a positive DFF using a *primary-secondary* configuration. (c) Waveforms of CLK at 1 kHz, D at 1.5 kHz, and outputs (Q) of both latch and DFF with V_{DD} = 5 V. (d) Determination of t_{su}, using the output waveform of DFF at 300 °C as an example. (e) Trend of t_{su} and the estimated f_{CLK} *vs.* temperature. In the above measurements, V_{DD} = 5 V.

knowledge, this work is the first demonstration of all the basic GaN memory cells at high temperature (300 °C) and the operational temperature of the reported GaN memory cells is the highest value recorded of its kind. The setup time of the fabricated DFF increases from 9 ns (room temperature, RT) to 14 ns (300 °C) with an estimated maximum clock frequency of 36 MHz at 300 °C. By validating the potential of GaN memory cells, this work paves the way for the realization of a robust microprocessor entirely based on GaN.

Chapter 5

Path towards a GaN Computer

With the demonstration of high temperature (HT) device technology with low gate leakage current and high yield and uniformity, simulation framework over a wide temperature range, and stable operation of key building blocks up to 500 °C, the GaN high temperature technology paves the way towards the GaN ICs with a higher level of complexity and device density integration. The next big leap of GaN HT technology is symbolized by the vision of a GaN computer.

Similar to the first Silicon-based and CNT-based computers, GaN HT computer designed in this chapter, with entire system built from GaN transistors, runs a basic operating system that execute stored instructions from the commercial MIPS instruction set and is programmable.

The GaN computer, using the similar design described in [17], is a one-instruction-set computer (OISC), implementing the SUBNEG (subtract and branch if negative)

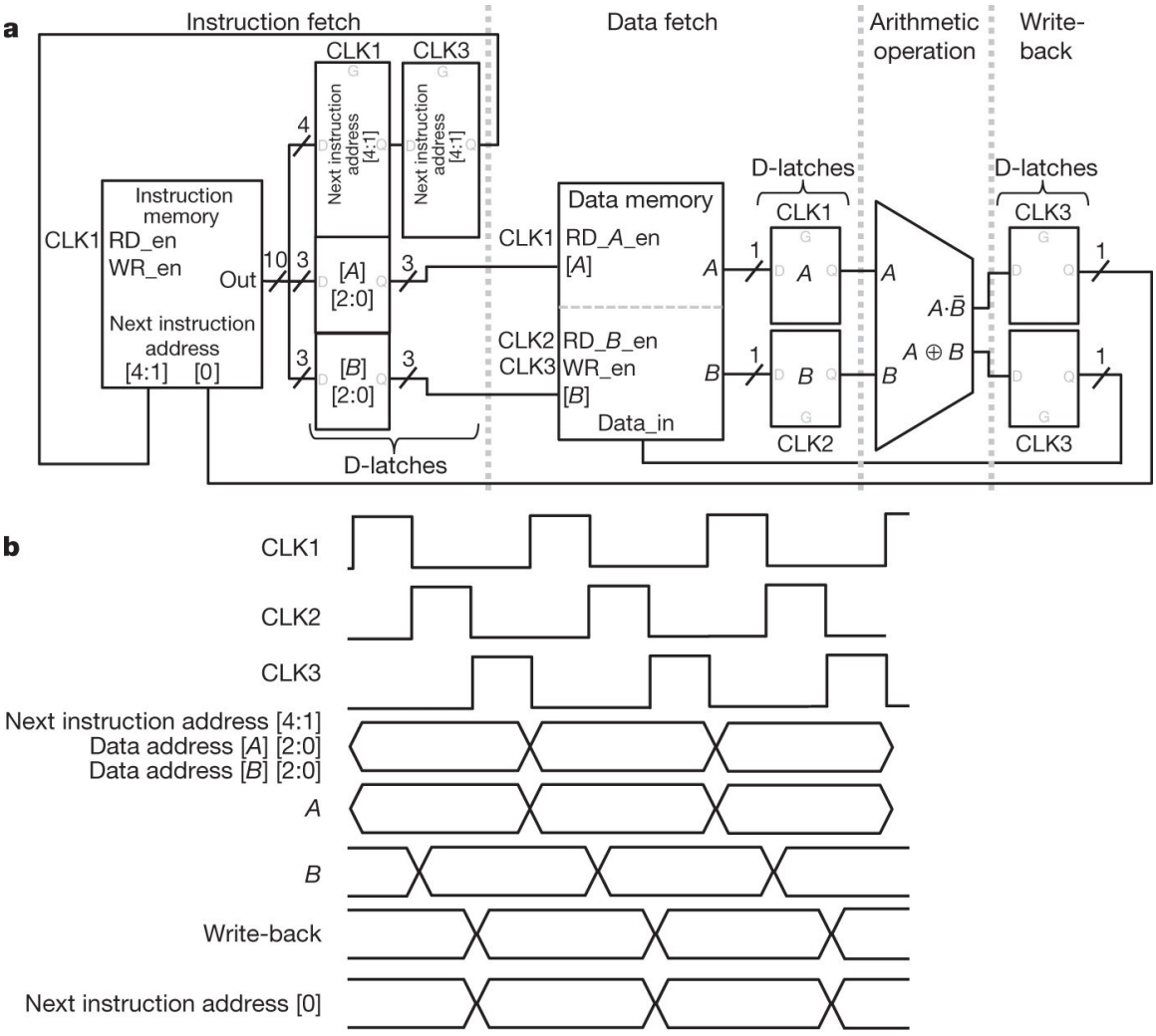


Figure 5-1: (a) Schematic of the GaN computer, composed of the four subunits: instruction fetch, data fetch, arithmetic operation and write-back. All components are implemented entirely using GaN transistors. CLK1–CLK3, Clock1–Clock3; D, D-latch input; Q, D-latch output; G, D-latch clock; RD_en, read enable (instruction memory); WR_en, write enable (instruction memory); RD_A_en, read enable address A (data memory); RD_B_en, read enable address B (data memory); Data_in, data for data memory write. (b), Timing diagram of the GaN computer. The lines show the waveforms corresponding to each signal; of particular note are the transitions of the lower five signals with respect to the clock signals [17].

instruction. The difference here is that the GaN computer is implemented using n-FET-only logic compared to the CNT computer based on the p-FET-only logic. Furthermore, unlike CNT computer with external data and instruction memory, the GaN computer includes on-chip memory which is also implemented by GaN transistors. The SUBNEG instruction is chosen here as it is turing complete and thus can be used to re-encode and perform any arbitrary instruction. The SUBNEG instruction consists of two 3-bit data address and one 4-bit partial next instruction address. The SUBNEG instruction subtracts the value of the data stored in the first data address from the value of the data stored in the second data address, and writes the result at the location of the second data address. The architecture of the GaN computer is shown in Fig. 5-1(a). The detailed description of SUBNEG OISC operation can be found in [17].

5.1 Design of GaN Computer

5.1.1 Overview

The GaN OISC consists of over 1110 transistors and can be divided as the following parts: (1) three-phase clock generator to generate three non-overlapping clocks as shown in Fig. 5-1(b), (2) 5-to-32 decoder for instruction memory and 3-to-8 decoder for data memory, (3) instruction memory, (4) data memory, (5) D-Latch, and (6) 1-bit arithmetic-logic unit (ALU). The 1-bit ALU is constructed with a NAND and

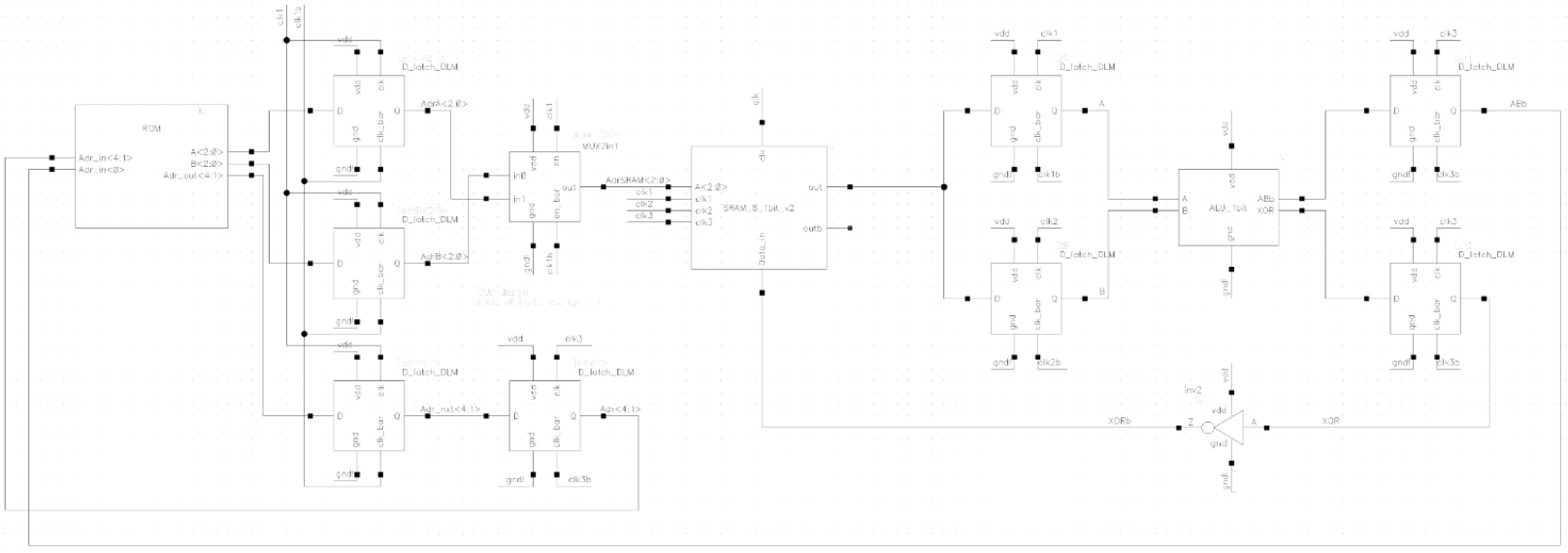


Figure 5-2: Schematic of the GaN OISC.

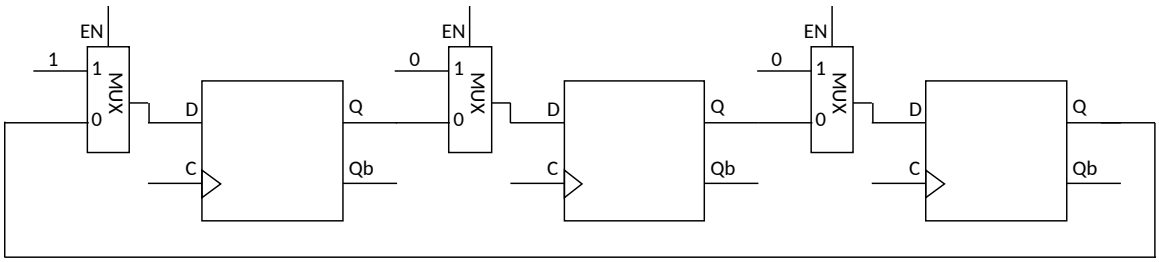


Figure 5-3: Schematic of the three-phase clock generator.

XNOR gate, and the implementation of D-latch was depicted in the previous chapter and will be omitted here. The schematic of the GaN OISC is shown in Fig. 5-2. The implementations of rest of units are depicted in the following sections. The functionality of all of the present circuits has been verified at simulation level using Virtuoso® UltraSim simulator at 300 °C.

5.1.2 Three-Phase Clock Generator

The three non-overlapping clocks are generated using a 3-bit shift register with the output of the third stage connected to the input of the first stage as shown in Fig. 5-3. A mux is used to select the input for each flip-flop between the output signal from the previous flip-flop and hard-coded reset signal (one of [100] in this case). An additional flip-flop is used to synchronize the reset signal.

The output is connected to cascaded inverters with progressive sizing to provide enough gate drive to the rest of digital blocks. The maximum fan-out used in this design is 6 to avoid potential contention.

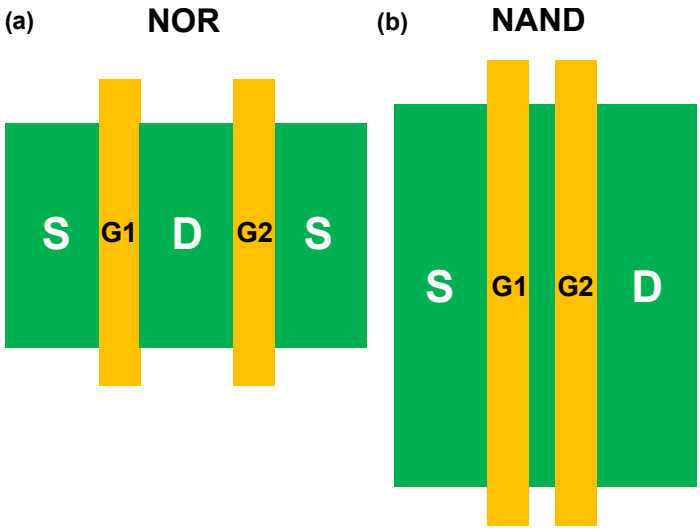


Figure 5-4: Schematic of pull-down network (PDN) of (a) NOR and (b) NAND gates using the optimized layout by sharing drain/source.

5.1.3 Decoder

5-to-32 and 3-to-8 decoders are used in the instruction memory and data memory, respectively, to select the right word line for read and write operation based on the address. The 3-to-8 decoder is implemented with NOR gate, while the 5-to-32 decoder is implemented with a predecoder and both NAND and NOR gates to reduce the total number of transistors. The optimized layouts with the shared drain/source area of the pull-down network of both NAND and NOR gates are depicted in Fig. 5-4. The schematic of both decoder is shown in the Fig. 5-5(a)–(b). The simulation was performed at 300 °C as shown in Fig. 5-5(c). The results indicate a successful operation of decoders at least up to 300 °C.

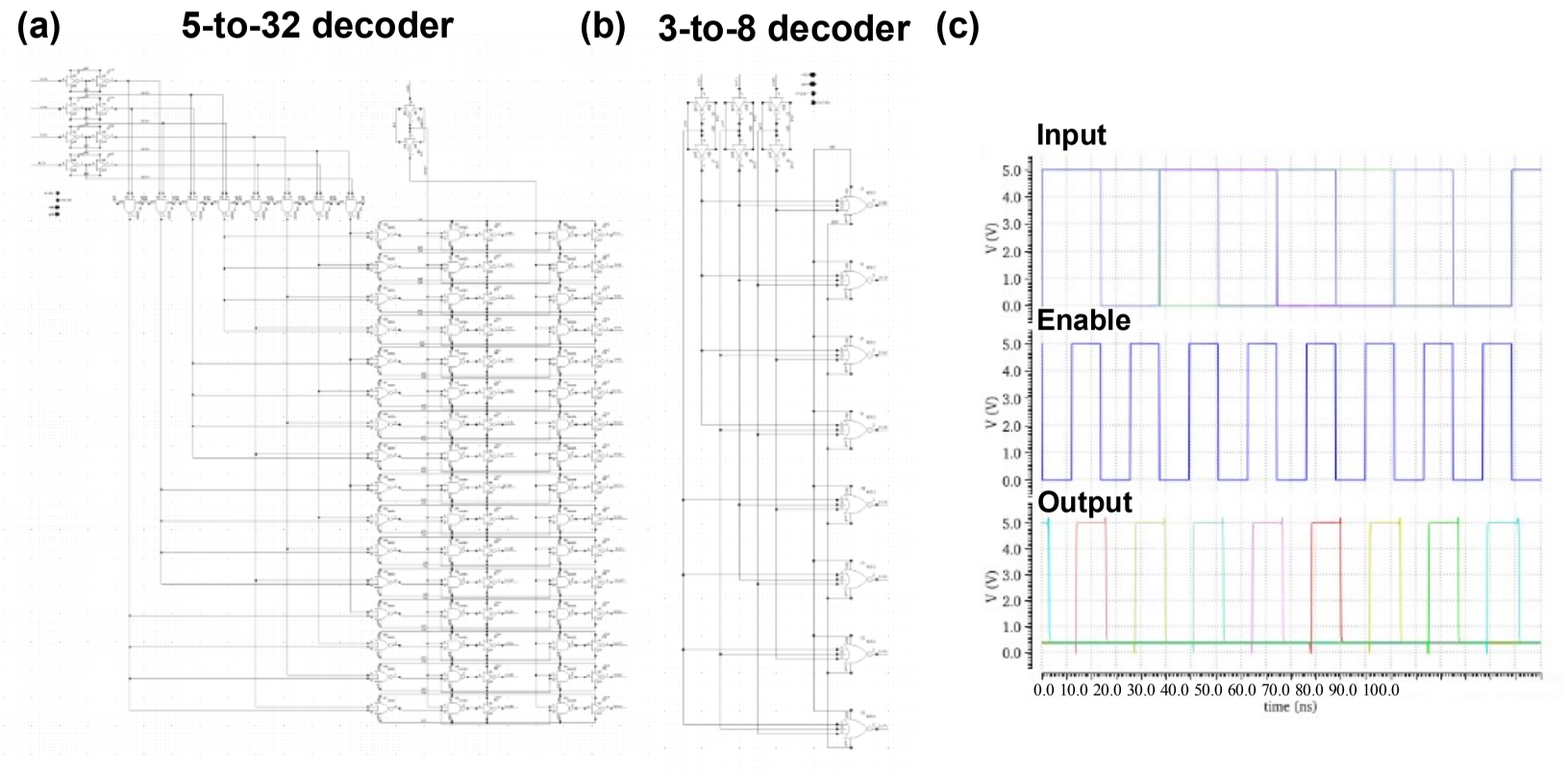


Figure 5-5: Schematic of (a) 5-to-32 decoder and (b) 3-to-8 decoder. (c) Simulation results of 3-to-8 decoder at 300 °C.

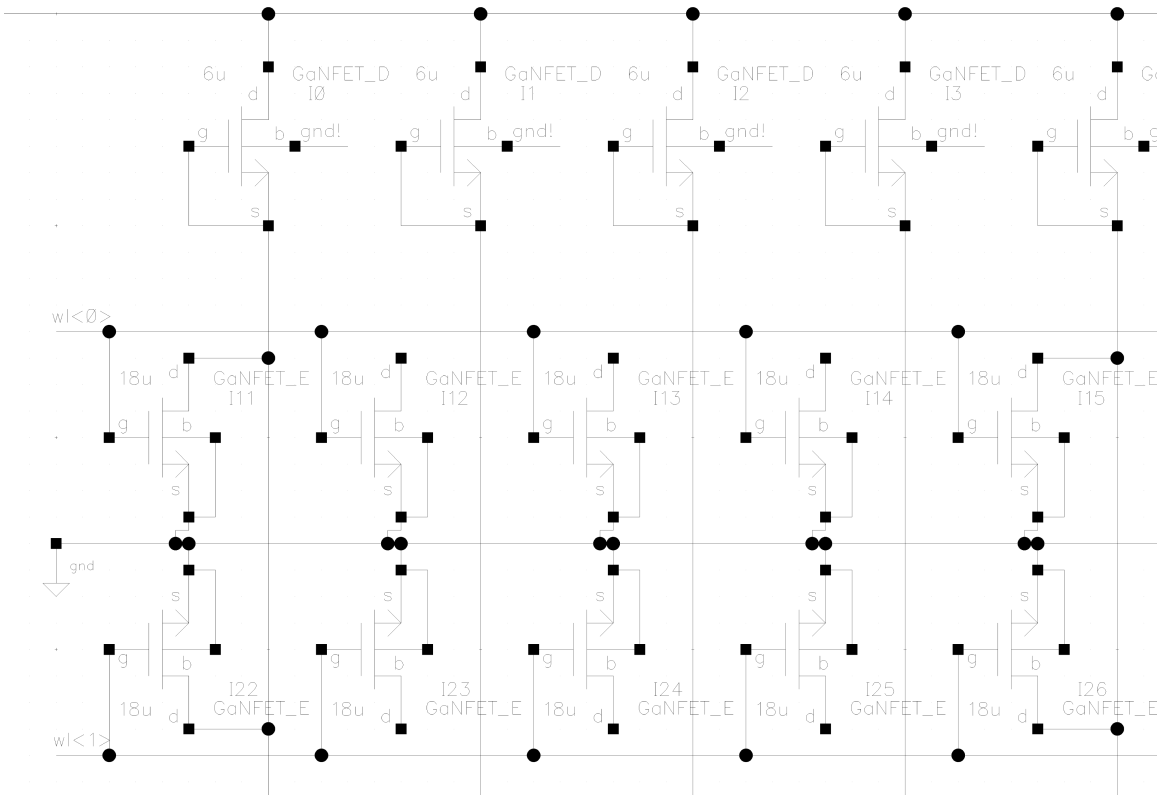


Figure 5-6: Part of schematic of NOR-based mask ROM array.

5.1.4 Instruction Memory

The instruction memory used in this design, implemented by a read-only-memory array and a 5-to-32 decoder, is the second most complex digital block with over 600 transistors. The same 32-bit × 10-bit NOR-based mask ROM array was constructed in chapter 4 (Fig. 4-5) with a total number of 350 transistors. This cell can store 32 10-bit instructions, which are physically encoded in the circuit by programming the via mask between individual ROM cell and interconnect during fabrication. The NOR-based implementation is chosen here to reduce the max on-resistance of pull-down-network and thus reduce V_{OL} to achieve a sufficient voltage swing.

5.1.5 Data Memory

The data memory is the most complex digital block in the GaN OISC. It was implemented by a 8-bit × 1-bit static random-access memory (SRAM) array with precharge and control circuits. The standard 6T-SRAM configuration was used here with a pull ratio (W_{T1}/W_{T3}) of 0.5 and a cell ratio (W_{T2}/W_{T3}) of 2 as depicted in Fig. 5-8(a). A large cell ratio was chosen to limit voltage rising in the cross-couple inverters during read operation, while a small pull-up ratio was chosen to overdrive the cross-coupled inverters to ensure the successful write operation. As a ratioed and sequential logic circuit, the data memory is extremely sensitive to the non-uniformity of transistor performance and potential variations in timing constraints. Therefore, the design of data memory should prioritize the tolerance to variations in transistor parameters

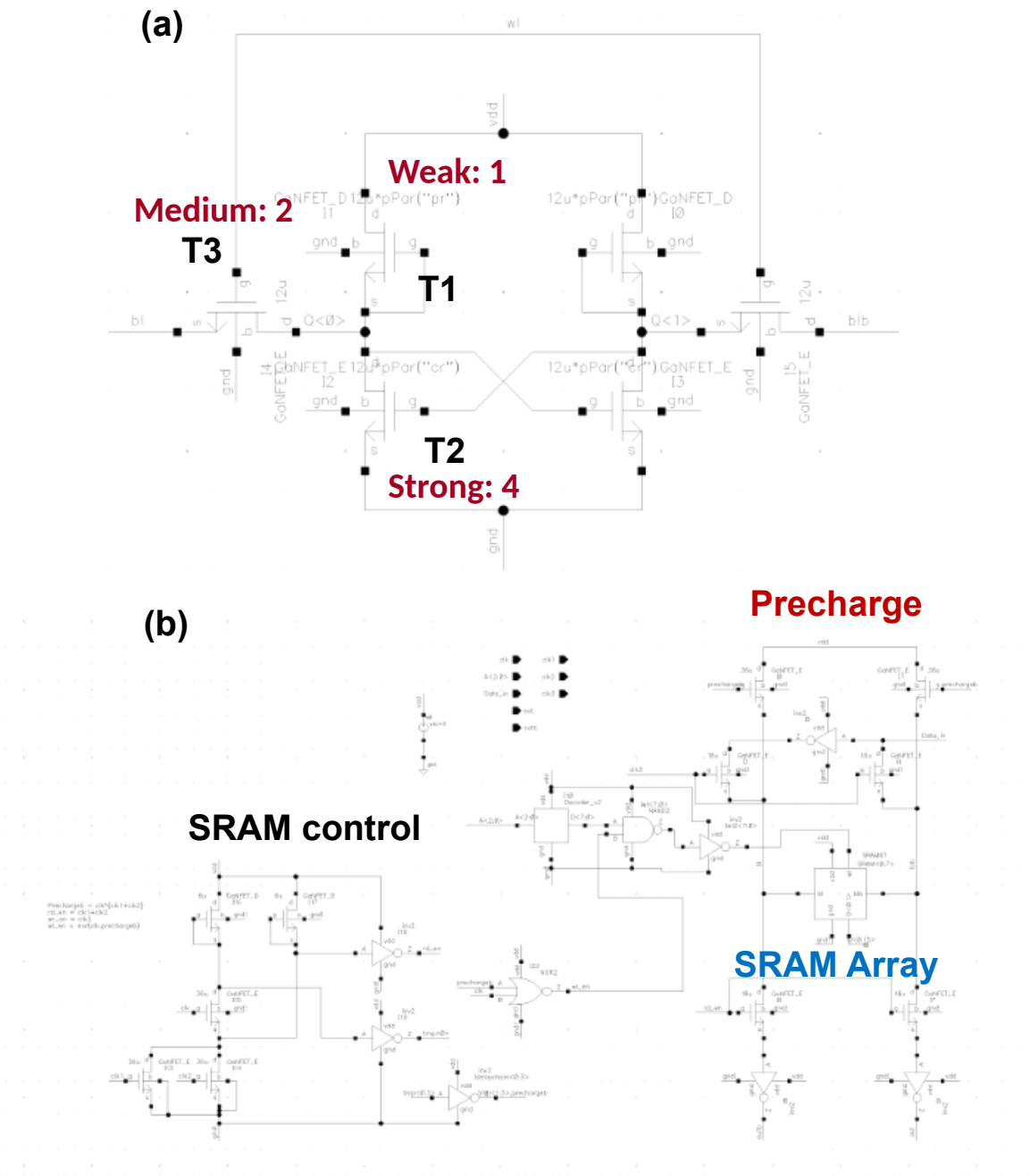


Figure 5-7: Schematic of (a) 6T-SRAM cell, and (b) Data memory with precharge, SRAM, and control circuits.

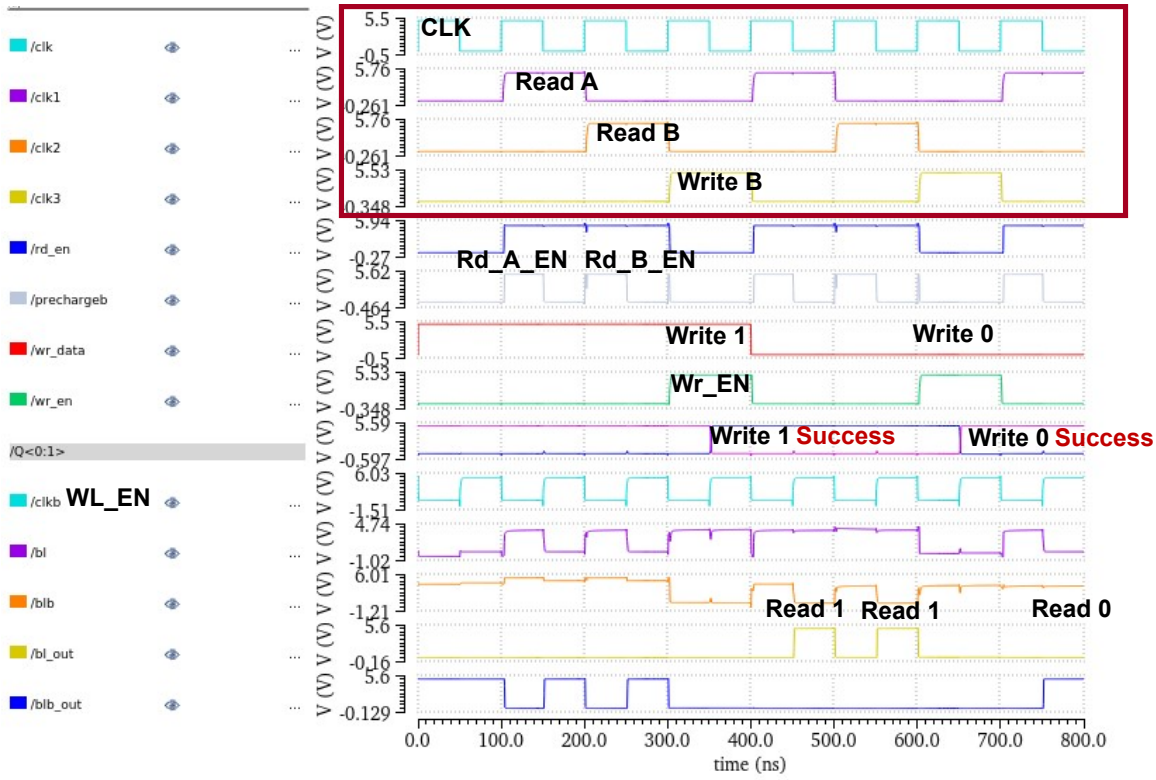


Figure 5-8: Simulation results of 8 1-bit SRAM array. Clock 1: Read A; Clock 2: Read B; Clock 3: Write B; Read: First precharge bitline to logic 1 ($V_{DD} - V_{TH,E}$), then disable precharge and enable work line to read; Write: Write to signal to bitline, and then enable wordline to write.

and timing constraints.

While the precharge of bitline is implemented with pass transistors, the control circuit is designed to avoid 1-1 overlap between precharge and WD_EN signals, which may cause the unwanted flip of the stored value.

5.1.6 Simulation Results of GaN Computer

The simulation results of GaN OISC are depicted in Fig. 5-9. The simulated next instruction address matches the expected output, forecasting a proper electrical func-

tionality of GaN OISC at least up to 300 °C.

5.2 Fabrication of GaN Computer and Failure Analysis

The fabrication of the GaN computer designed in previous section followed the same process flow described in section 2.2. The micrograph of the fabricated GaN computer is shown in the Fig. 5-10 and Fig. 5-11. While all the key building blocks were demonstrated in the previous chapter with a stable operation at least up to 300 °C. The GaN OISC failed to function even at room temperature. The parasitics were found to be the major limiting factor.

Table 1 shows the calibrated sheet resistance (R_{sh}) of interconnects in different metal stacks. A 1 mm Ti/Au (20/200 nm) metal trace with a width of 10 µm can have a resistance of $\sim 20\ \Omega$. A baseline inverter with $W_E/W_D = 18/6$ µm/µm has a static current around 2–3 mA. Assuming a total of 100 mA static current and 1 mm metal trace for power distribution, a decreased V_{DD} and a increased gnd will be seen at the end of line with a voltage drop of 2 V on each terminal as depicted in Fig. 5-12(a) using the simplest model. The voltage drop can be reduced to half using the model with evenly-distributed current. This effect is known as IR drop.

The experimental results of two cascaded and progressively-sized inverters on the GaN OISC for clock signal amplification showed the impact of IR drop as seen in

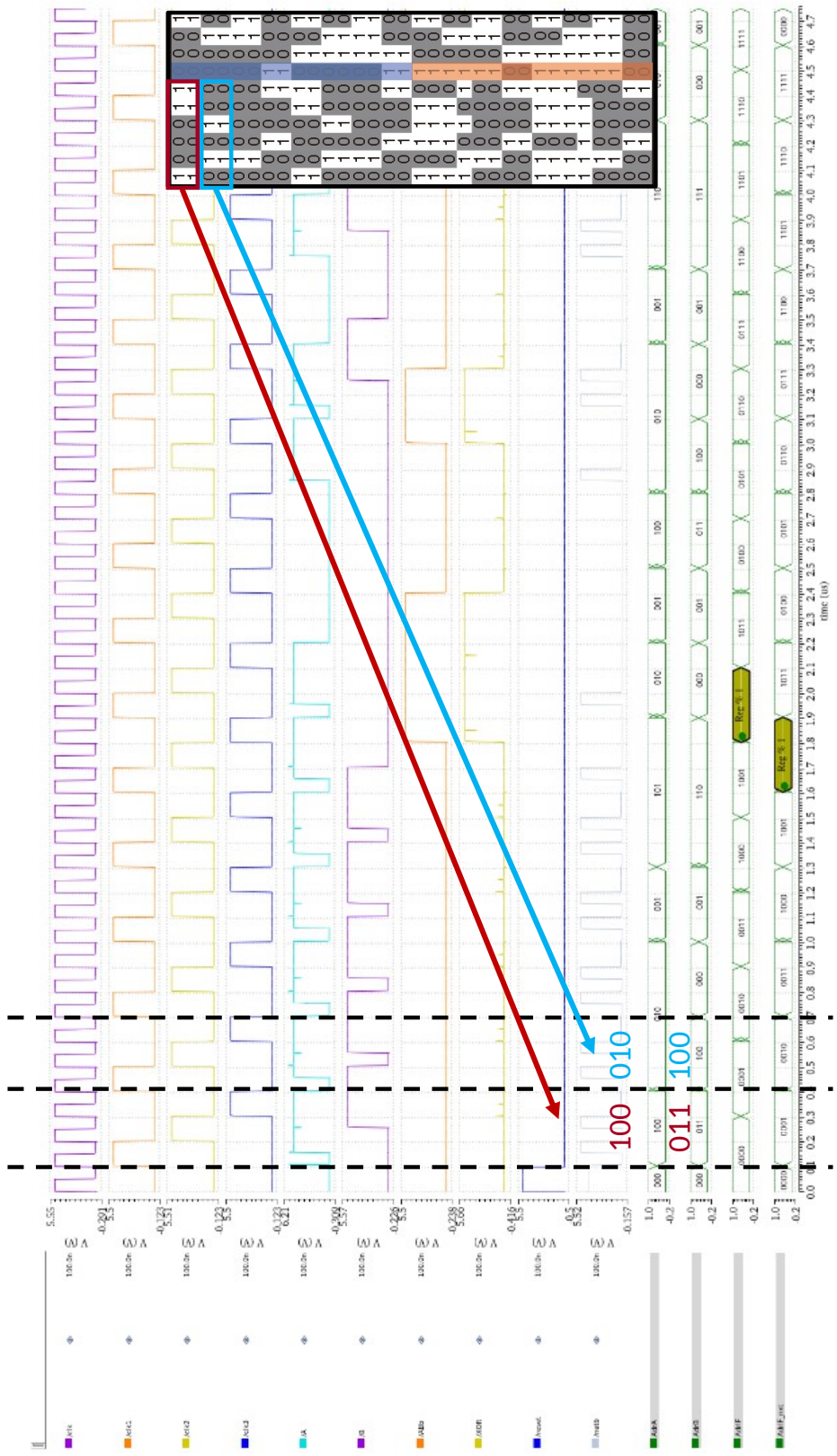


Figure 5-9: Simulation results of GaN OISC.

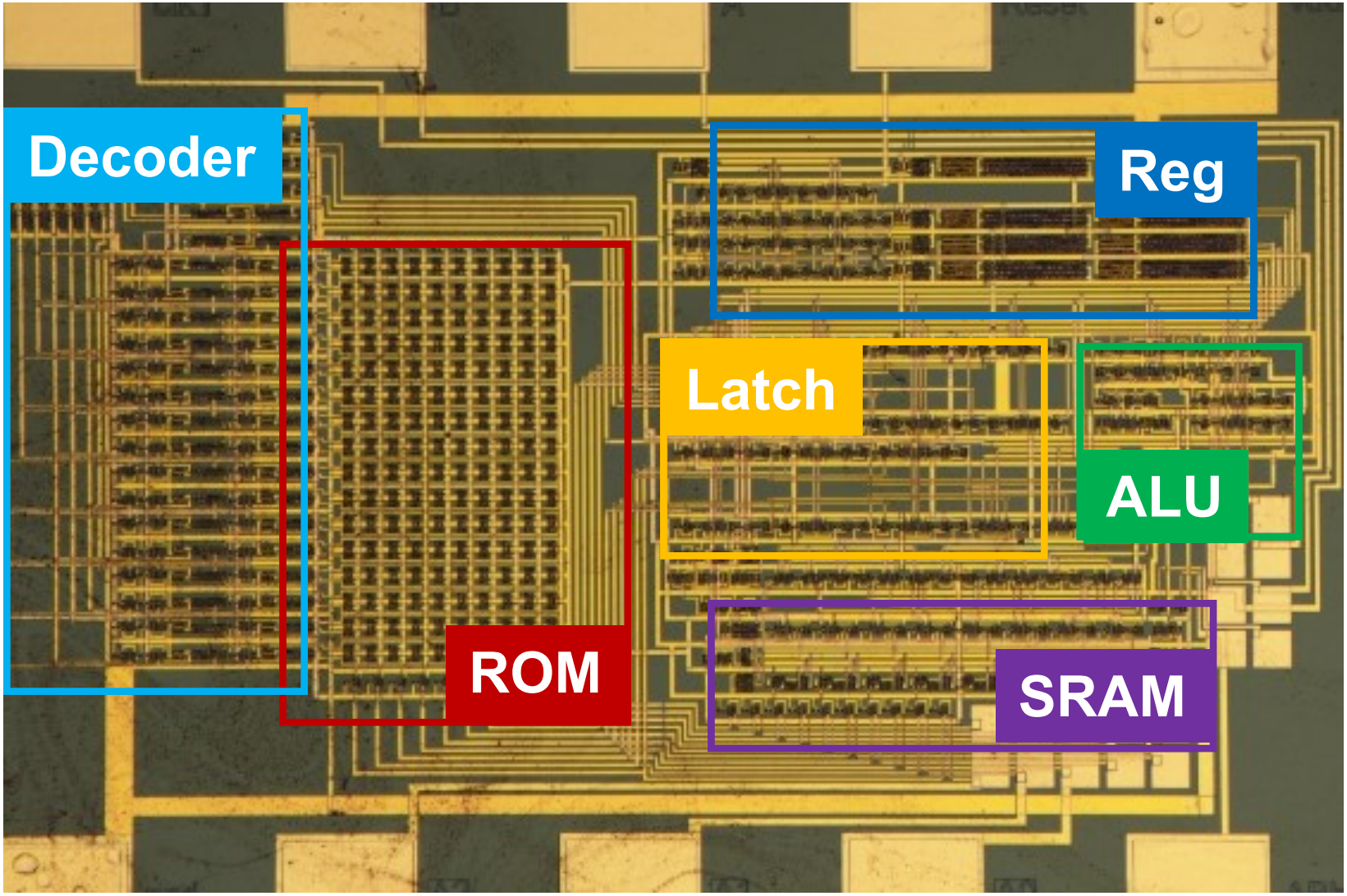


Figure 5-10: Micrograph of the entire fabricated GaN computer.

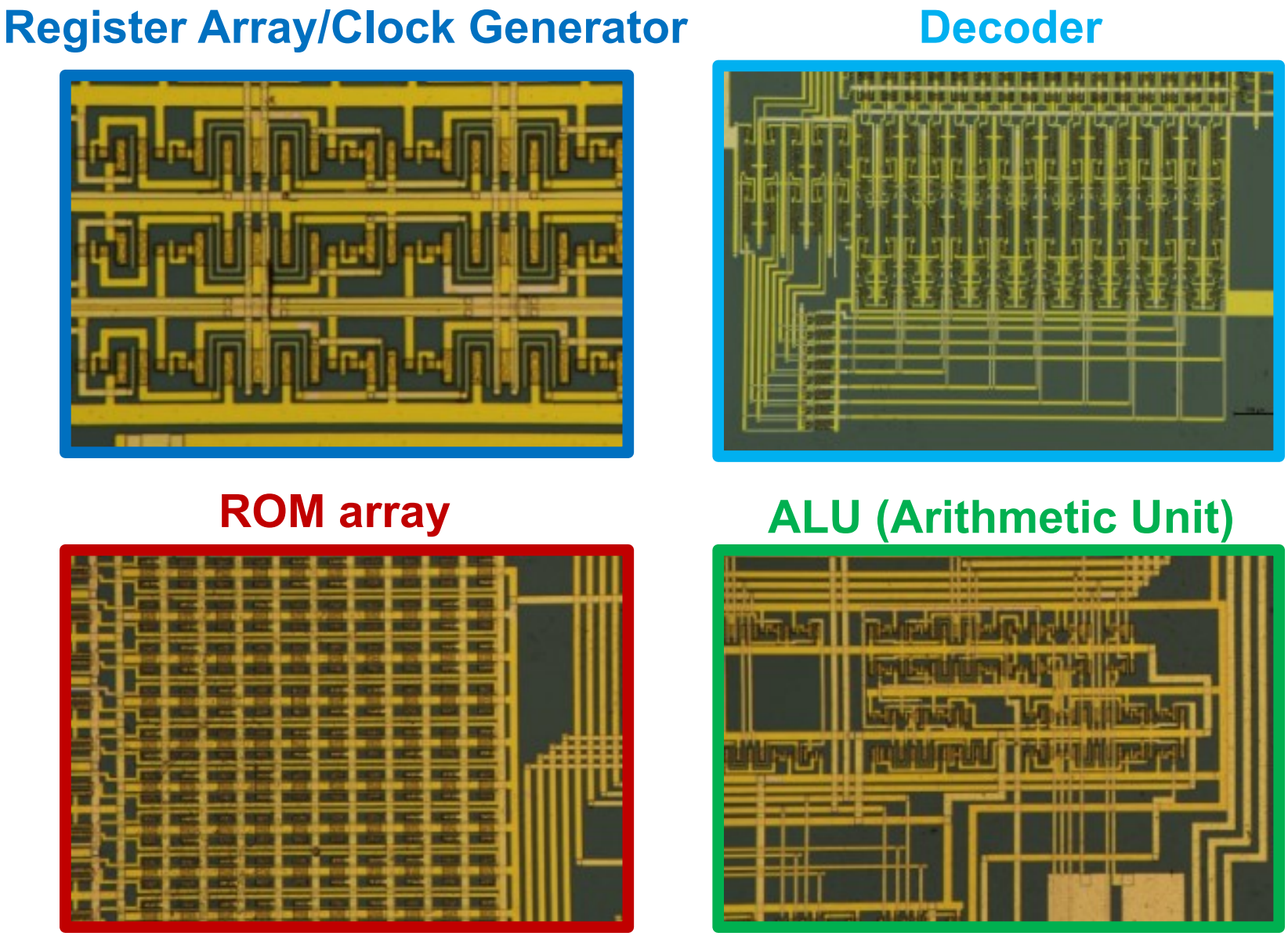


Figure 5-11: Micrograph of three-phase clock generator, decoder, ROM array, and ALU of the fabricated GaN computer.

Table 5.1: R_{sh} of interconnects in different metal stacks.

Interconnect	R_{sh} ($\Omega/\square$)
Ni/Au (30/80 nm)	0.59
Ti/Au (20/100 nm)	0.52
Ti/Au (20/200 nm)	0.21

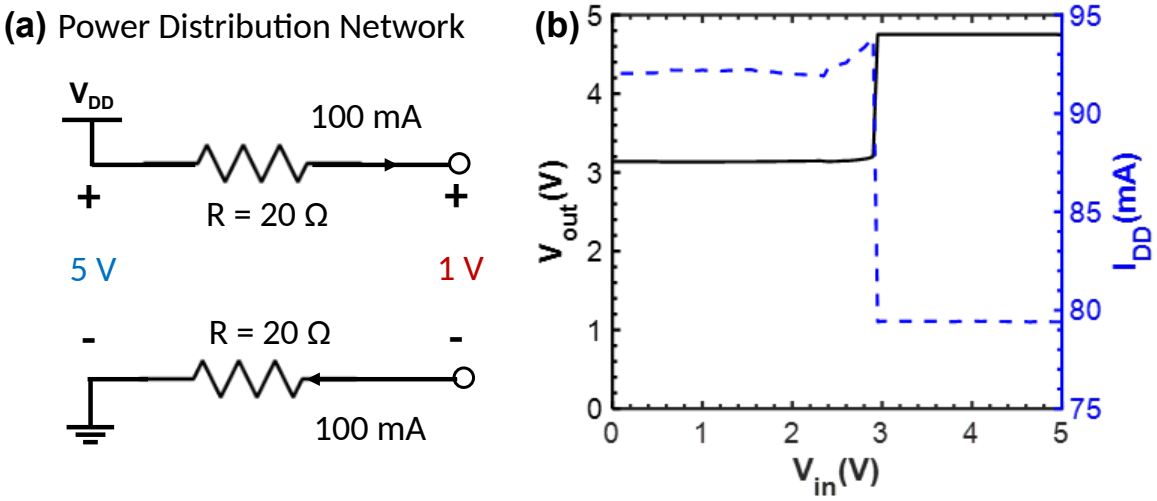


Figure 5-12: (a) Explanation of IR drop using a simplified model. (b) IR drop observed in the two cascaded progressively-sized inverters on the fabricated GaN OISC with reduced voltage swing.

Fig. 5-12(b). A reduced voltage swing around 1.5 V was observed due to the increase of gnd voltage level mainly resulted from the position of gnd input which is located far from the inverters. The results indicate the significance of parasitic extraction, which can help to catch the potential issues at an early stage. Further optimization is required to find the proper interconnect metal stack with low sheet resistance and good thermal stability. It should be noted that the increase of the width of metal wire, which will help to reduce sheet resistance, is generally undesirable considering the potential increase of parasitic capacitance.

Besides, as illustrated in the chapter 3 (Fig. 3-9), the extra parasitics, including both resistor and capacitor, will introduce extra delay and lead to the malfunction of the fabricated ICs, especially on the sequential logic circuits with tight timing constraints.

5.3 Conclusion

In this chapter, the design of a one-instruction-set computer (OISC) built from over 1110 GaN transistors was presented based on the proposed simulation platform up to 300 °C. The functionality of all of the key blocks including three-phase clock generator, data memory, instruction memory, decoder was verified at simulation level. The failure of the first generation of the fabricated GaN OISC was analyzed and discussed, which may be mainly attributed to the IR drop on the power distribution network. The simulation results reflect the feasibility of GaN computer and the experiment results point out the direction for future optimization towards the integration of GaN transistors with higher complexity.

Chapter 6

Conclusion and Future Work

6.1 Thesis Conclusion

Driven by the primary need to realize GaN-ICs with high complexity and device density integration for high temperature operation, this thesis aims to conduct a comprehensive study on GaN High temperature technology from device to circuits.

Chapter 1 introduced the opportunities for high-temperature electronics. The fundamental physical limitations of conventional semiconductors like Si, GaAs were discussed and compared with those of wide bandgap materials. SiC and GaN were introduced and compared regarding material properties, technology infrastructures, and potential applications, explaining why GaN would be a superior choice for high-temperature operation, especially high frequency applications.

Chapter 2 demonstrated a GaN high temperature device technology based on

the E-mode p-GaN/AlGaN/GaN wafer platform. The fabricated device show stable operation up to 500 °C. The physics behind the performance degradation was studied and explained. A high uniformity, a critical metric for large-scale integration, was achieved with the optimization of selective-etch process, Furthermore, the potential of aggressive channel length scaling was also studied based on the similar process, and better R_{on}, I_{on} were observed. Besides, an in-house developed packaging technology and measurement platform with high temperature ratings were proposed. An in-situ measurement at 500 °C over 24 h was demonstrated. The fabricated transistors exhibited stable performance over 20 days at 500 °C.

Chapter 3 explored the extension of the device technology and demonstrated a temperature-dependent compact models of the E/D-mode transistors characterized in chapter 2. Besides, a high temperature specific circuit design was conducted based on the existing device technology. A general guideline was developed to highlight in the aspects of critical parameters, and most important considerations when selecting circuit topology. Furthermore, the simulated key metrics to evaluate the performance of inverter, ring oscillator, and DFF were compared with experimental data to validate the proposed simulation platform.

Chapter 4 demonstrated key building blocks designed with our high temperature platform, including inverters with different configurations, ring oscillators, SRAM, ROM, D-Latch, and DFF operational up to 500 °C demonstrating monolithic integration of more than 350 transistors. The performance was evaluated and benchmarked

against other GaN implementations and SiC counterparts. The proposed technology sets a new boundary of t_p *vs.* L_G^2 in wide band gap digital logic, and is operational at the highest reported temperature (500 °C) of a GaN digital circuit. The results reflect the promising potential of the proposed technology for emerging HT applications at 500 °C and beyond.

Chapter 5 presented the design of GaN one-instruction-set computer (OISC) with over 1110 transistors based on the proposed simulation platform. On-chip instruction memory, data memory, and buffer were implemented with ROM, SRAM, and D-latch demonstrated in the previous chapter. The simulation results matched the expected outputs, indicating the proper electrical behavior and thus feasibility of GaN computer. However, the first generation of the GaN OISC, fabricated using the proposed process flow, failed to operate. The potential issues leading to the GaN OISC failure were analyzed and discussed, which may be mainly attributed to the IR drop on the power distribution network. The simulation results reflect the feasibility of GaN computer and the experiment results point out the direction for future optimization towards the integration of GaN transistors with higher complexity.

6.2 Future Work

In this thesis, work has been done to prove the potential of GaN electronics in high-temperature digital and mixed-signal circuits. Here, the future work is proposed to further improve the performance and complexity for GaN ICs.

- As discussed in chapter 2 and 3, the degradation of mobility is typically faster than that of resistance. The short channel device, with R_{on} dominated by R_C instead of mobility, is found to have less on-current degradation. By further scaling down the channel length, better high temperature device performance can be achieved. Further exploration is needed to study the short-channel gate leakage current mechanism across temperature and improve the yield and uniformity.

- In spite of the excellent high temperature performance shown by E-mode transistors, the optimization of D-mode transistors is also needed for high temperature operation on the proposed monolithic integration platform. A common misconception is that the performance of D-mode transistors has little impact on circuit operation. Unlike complementary logic, D-mode transistors in the circuits using n-FET-only logic, typically serve as the loads with gate-source shorted. Besides, the thermal stability of D-mode transistor has been studied extensively over the past few decades. However, as demonstrated in chapter 3, the D-mode transistor can also affect circuit operation and most of the previous study on D-mode transistors is based on the conventional D-mode wafer platform without additional p-GaN threshold voltage modulation layer. Further study is required for high temperature D-mode transistor technology on the p-GaN/AlGaN/GaN wafer platform.

- One of the major advantages that distinguishes GaN from its major wide

bandgap competitor (i.e. SiC), is its high saturation velocity and mobility, making them an ideal candidate for RF applications. While the Si substrate will become conductive and degrade RF performance, further study can be focused on the demonstration of GaN RF transistors for high temperature applications on SiC, sapphire, or any semi-insulating substrate.

- A key limiting factor of integration of GaN transistor integration with higher complexity for high temperature application is the lack of high temperature BEOL technology, leading a early failure well below the intrinsic limit. Further exploration is needed to find the optimum interconnect metal and insulator with good thermal stability and matched coefficients of thermal expansion.

- While the GaN one-instruction-set computer was successfully designed based on the proposed simulation framework, the fabricated GaN OISC still can not function properly due to the parasitics. Further study and calibration are required from device to circuit level, namely, TCAD simulation to extract the potential device-level parasitics and parasitic-extraction from the circuit layout.

- Furthermore, a complete process design kit (PDK) is needed to advance the VLSI of GaN transistors with design rule checking (DRC), layout versus schematic (LVS) checking, and parasitic extraction, which require further calibration of both front-end-of-line (FEOL) and BEOL process across temperature.

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