Hybrid Integration of III–V Solar Microcells for High-Efficiency Concentrated Photovoltaic Modules

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***Abstract*— The design, fabrication and performance of InGaAs and InGaP/GaAs microcells are presented. These cells are integrated with a Si wafer providing a path for insertion in hybrid concentrated photovoltaic modules. Comparisons are made between bonded cells and cells fabricated on their native wafer. The bonded cells showed no evidence of degradation in spite of the integration process which involved significant processing including the removal of the III-V substrate.**

***Index Terms*—multi-junction solar cells, wafer bonding, photovoltaic cells, III-V solar cells, hybrid integration**

I. Introduction

THE marrying of disparate material systems through hybrid integration leads to more innovative devices. This is particularly true in optoelectronic devices where the electrical as well as optical properties of the devices must be taken into consideration. There have been reports of combining Si and III-V devices for communications and here we discuss the hybrid integration of Si and III-V photovoltaics for high efficiency solar modules in a variety of environmental conditions.

The path to higher solar cell efficiencies has focused on collecting photons as close to their energy level as possible to minimize the solar energy lost to heat. This has been done with multi-junction cell stacks of varying bandgaps spanning the entire solar spectrum. The typical method of integrating these junctions is monolithic epitaxial integration requiring current matching through all the junctions. These types of cells have demonstrated the highest efficiencies to date [1-3]. However, as the number of junctions increase beyond three to four or more epitaxial growth becomes more difficult due to lattice mismatch between materials. Also, current matching becomes more challenging. Although there have been demonstrations of the growth of lattice mismatched materials on the same substrate to form multijunction cells [1,4], this approach requires tradeoffs in the material quality and achievable bandgaps. Such limitations can be overcome through direct wafer bonding or wafer bonding using a dielectric bond layer. Most of the demonstrations of hybrid integration of solar cells have focused on using the integration as a means to achieve higher efficiencies in traditional concentrated photovoltaic (CPV) systems. However, these integration techniques can also be used to enable new CPV systems applicable to a wider variety of environments than traditional CPV. Sandia and others have explored new PV modules and systems by scaling down the size of the photovoltaic cells below 1 mm dimensions [4-9]. These smaller cells enable new optical designs based on refractive optics and advanced module architectures which allow for a larger field of view, higher concentrations, reduced heating, and higher efficiencies. When coupled with a diffuse collection system, these architectures have the potential to make concentrated photovoltaics viable in areas beyond the typical high DNI (direct normal incidence) areas such as the southwest United States. In some cases, these systems could be replacements for Si flat plate panels with much higher energy production. Two proposed examples of these systems include

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hybrid microscale photovoltaic systems as described in [5,8] with separately connected junctions for maximum efficiency. Another concept is wafer integrated photovoltaics [9] which utilizes a multi-functional Si platform which acts as a cell, optical concentration element and integration platform for a molded lens array [10], a multi-junction micro-cell array and the interconnection layer. Calculations presented in [8] have shown that compared to conventional flat plate PV and CPV, there is the potential for an energy production boost of 40-50% and 15-40% across the U.S., respectively**,** with the collection of diffuse light as well as direct light in a concentrated system.

High-performance, multi-junction microcells are key to the feasibility of these module approaches. However, these systems push unique requirements on the microcells. Intimate integration is required between the III-V cells and Si cells including low-loss optical transparent transitions between cells and electrical connections to a common interconnection plane. Cost models [11] for such systems require the judicious use of the expensive compound semiconductor material meaning only the epitaxial layers are used in the module while the substrate should be available for reuse. The optical designs push to smaller and smaller cell sizes. Wafer level bonding of cells or solder bump bonding of III-V cells to Si provides a path to achieving these requirements.

In this paper we discuss important aspects of microcell design in Section II. In Sections III and IV demonstrations of GaAs/InGaP dual junction cells and InGaAs single-junction cells respectively are presented. Data from cells fabricated on their native growth wafer are compared to cells bonded to Si in both instances.

II. Microcell Design

Two things drive unique design considerations for microcells – the small size and the integration with a holding platform. The small size of the cell and its intimate integration with Si pushes towards cells with gridless designs and therefore the spreading resistance of cells contact layers need to be considered. Properly designing the cell contact layers to take this into account can mitigate the resistive losses. Since most designs don't lend themselves well to backside processing even if optical transparency isn't an issue – the spreading resistance is important for both the top and bottom contacts. These resistance sources are seen in Figure 1. We have done extensive analysis of the effects of spreading resistance with cell size. There is a tradeoff in the thickness of the window and contact layers to minimize resistance and the absorption characteristics which effect the overall device efficiency. A simulation of the resistive power losses for a gridless circular cell as a function of device size and total resistance is shown in Figure 2. Figures 5 and 9 show the chosen epitaxial layer structures to balance these effects. A more complete analysis of these effects is reported in [12].

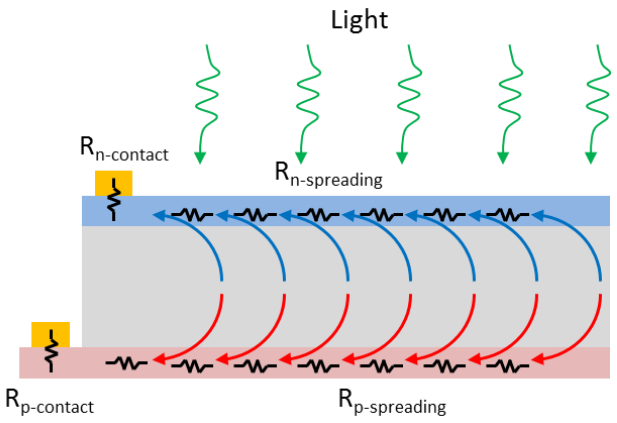


Figure 1: Diagram of the sources of excess resistance in a single junction for a stacked junction solar cell. The extra resistance includes contact and spreading resistance for both the p-contact and n-contact.

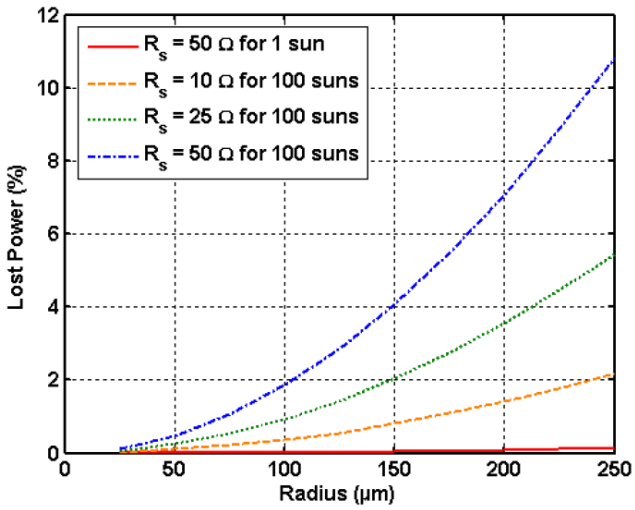


Figure 2: Simulated power lost due to spreading resistance vs. optical aperture radius. Simulation assumes maximum current extraction from an InGaP/GaAs dual junction cell with a gridless circular aperture.

The parasitic dark current contributions from the sidewall and non-illuminated areas under the contacts can become quite significant in microcells due to their small size. The semiconductor contact area should be reduced to the smallest feasible area as dictated by lithography and resistance. This will also reduce the overall III-V material used which is important for cost considerations. The contact area may also shade the cell, further reducing overall module efficiency.

The sidewall can also play a significant role in contributing to parasitic dark current which reduces the cell efficiency. The sidewall is particularly sensitive to fabrication processes including the methods used to etch the cell mesa and how the sidewall is encapsulated. A study of the effects of encapsulating the sidewall was run. This study looked at InGaAs cells from two process runs. In the first, the mesa was dry etched and the sample went through another lithography

process prior to protecting the sidewalls with SiN. In the second process variation, the sidewalls were immediately protected with SiN after being defined with dry etch. The dark current at -0.3 V was then recorded for cells with radiuses ranging from 50 to 1200 µm. The dark current recorded for the smallest cells was an order of magnitude less for the cells with the immediate encapsulation of the sidewalls. This shows the importance of sidewall passivation as the cells continue through the process. These results are shown in Figure 3.

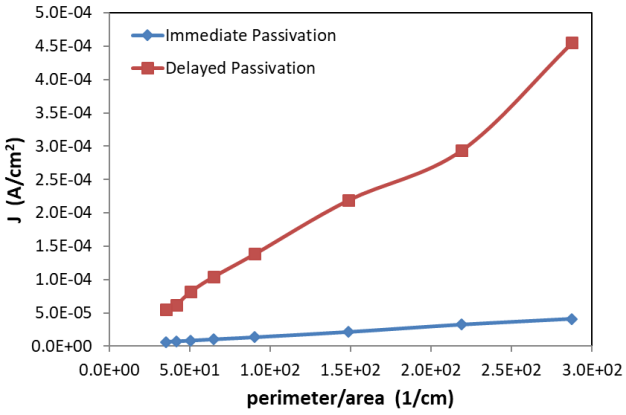


Figure 3: Comparison of dark leakage current density for InGaAs cells fabrication with an immediate SiN passivation following the mesa etch (diamonds) and for a delayed passivation (squares). Leakage current is recorded at a bias voltage of -0.3 V for both cell types.

III. Dual Junction InGaP/GaAs Cells

Sandia has designed and fabricated InGaP/GaAs dual junction cells for integration via solder bump bonding as well as wafer bonding. Figure 4a shows InGaP/GaAs cells wafer bonded to Si and Figure 4b shows an image of InGaP/GaAs cells for integration with Si for integration using solder bump bonds. The cell epitaxial design was an n-on-p design with an n-type emitter for both cells and a tunnel junction between the two cells. The epitaxial structure for the two cells is nominally the same, although as grown the structure was flipped for the bonded cell so the cell would be right side up following bonding. The epitaxial structure of the cell is shown in figure 5. This configuration prevents a direct comparison between bonded and unbonded cells with the same epitaxy. However, since the cells share nominally the same epitaxy they can be compared to look at the effects of bonding on cell performance.

(a) (b)

Figure 4: (a) Micrograph InGaP/GaAs cell bonded to Si substrate (b) Micrograph InGaP/GaAs cell for solder bump integration

Layer	*Material*	*Thickness (nm)*
InGaP cell contact	n-GaAs	800
InGaP cell window	n-AlInP	20
InGaP emitter	n-InGaP	100
InGaP base	p-InGaP	760
InGaP BSF	p-AlGaInP	40
Tunnel Junction		
GaAs window	n-AlGaAs	40
GaAs emitter	n-GaAs	100
GaAs base	p-GaAs	3100
GaAs BSF	p-AlGaAs	50
GaAs contact	p-GaAs	1500

Figure 5: InGaP/GaAs cell epitaxial structure.

For the cell bonded to Si, the cell mesas were defined prior to bonding using a combination of wet and dry etches. The cells are bonded to the Si wafer with a SiN dielectric bond interface which allows for electrical isolation between the InGaP/GaAs cell and the Si. A 30 nm layer of PECVD SiN was deposited on the InGaP/GaAs cell wafer. While a 10 nm layer of thermal oxide was grown on the Si wafer. The dielectric on both wafers were activated with an O_2 plasma in an RIE. The two wafers were then bonded together at room temperature forming a Van der Waals bond. This bond was strengthened by using a bladder bonder to apply pressure of 25 psi and heating to 150° C for 12 hours. The thickness of the dielectric bond interface was designed to have reflective losses of <3% across the relevant solar spectrum. The GaAs substrate was then removed by etching an InAlP sacrificial layer to release the cells. The cell design employs a topside n-GaAs contact layer which is designed to accommodate the diffusion of AuGe/Ni/Au contacts and a bottom p-type contact layer of GaAs with a Ti/Pt/Au metallization. A citric acid wet etch is used to remove the GaAs contact layer and expose the AlInP window layer in the optical aperture due the high selectivity between GaAs and AlInP. The cells fabricated on their native GaAs substrate used the same contact metallization. The cell mesas were defined using a dry etch.

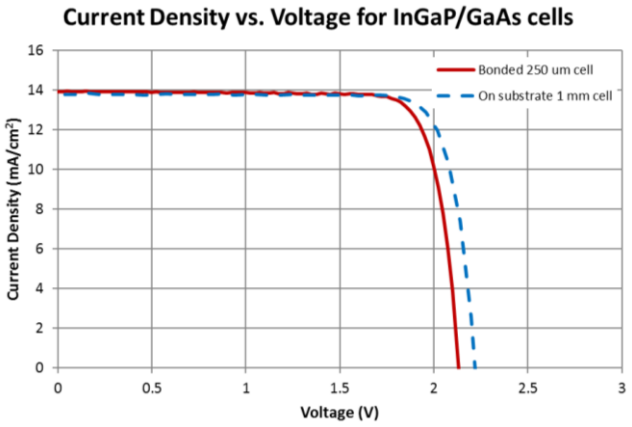


Fig. 6. InGaP/GaAs micro-cell bonded on Si (red solid line) and on-wafer (blue dashed line) one sun J-V measurement curves.

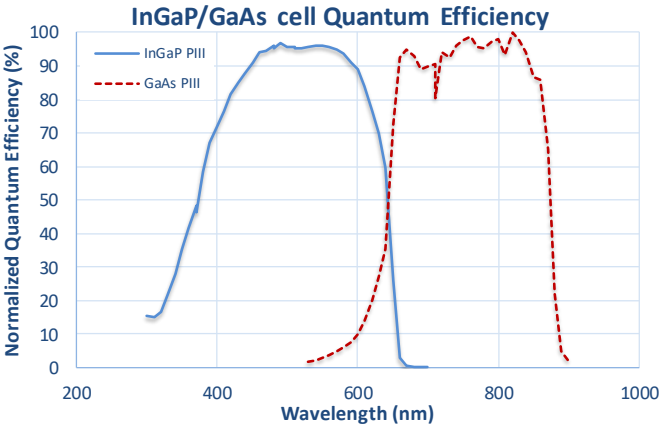
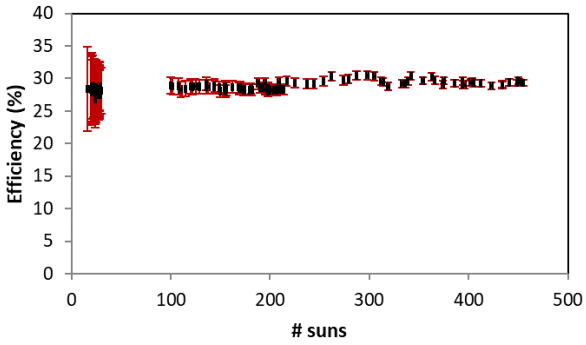


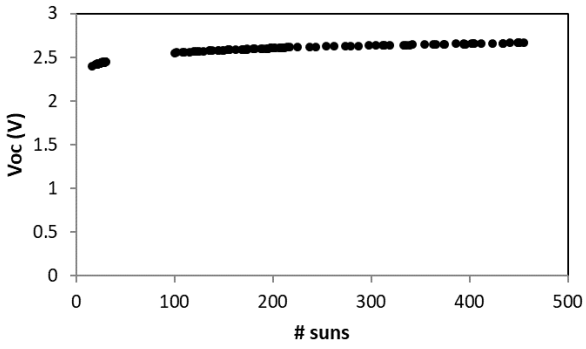
Figure 7: Normalized external quantum efficiency measurement for InGaP/GaAs cells bonded on Si

Following fabrication, the cells were tested in a solar simulator to access the cell performance. The one sun measurements were done using an OAI class AAA solar simulator (from 300 to 1800 nm) with an intensity of 1 sun and spectrum AM 1.5 calibrated using a silicon reference solar cell. The output of the cell was measured using an Agilent B1500a semiconductor device parameter analyzer. Cell efficiency, open circuit voltage (V_{oc}) and short circuit current density (J_{sc}) were extracted from the current-voltage curves obtained for each device. The current density vs. voltage curves for bonded and on-substrate cells are shown in figure 6. The bonded cell has a circular aperture with a radius of 125 µm for an optical aperture area of 0.049 mm^2, the on-substrate cell has a 1 mm^2 optical aperture. The bonded cell efficiency, fill factor, open circuit voltage, V_{oc}, and short circuit current density, J_{sc}, were measured to be 24.4%, 82.4%, 2.13 V and 13.9 mA/cm^2 respectively. The on-wafer cell efficiency, fill factor, open circuit voltage, V_{oc}, and short circuit current density, J_{sc}, were measured to be 25.4%, 82.3%, 2.22 V and 13.8 mA/cm^2 respectively. The curves are very similar in shape with nearly identical fill factors and short circuit current densities. The increase in V_{oc} and thus efficiency for the on-wafer cell can be attributed to the larger cell size. As outlined in Section II, the contribution for bulk dark current is significant for the 250 µm radius device as the junction area under the contact metal outside the optical aperture accounts for 15.5% of the device junction area while this area accounts for 44.5% of the junction area for 1 mm square on-substrate device. This increased bulk dark current contribution results in the lower V_{oc} seen for the smaller cell. This is all consistent with the InGaAs data shown in Section IV.

The bonded cells were also tested under concentration and the measurements are shown in Figure 8. The scatter in the concentration data at low concentrations is due to the single cell measured current being near the noise floor of the current meter. A fit is applied to the efficiency data and used to extract a maximum efficiency of 29.5% at 200 suns. As expected the open circuit voltage increases with concentration. The decrease in fill factor observed with higher concentration is expected due to spreading resistance in the optical aperture. We have previously reported on the tradeoffs of cell size with resistance under concentration and showed the advantages of micro-scale cells with concentration without reducing the cell efficiency due to shading of electrical gridlines [13]. The external quantum efficiency of the cells was measured and is shown in Figure 7. The efficiencies of these bonded cells match the design very closely and there isn't any obvious degradation from the bonding and substrate removal of the cells. This is also shown in the InGaAs cells as is discussed in Section IV.



(a)



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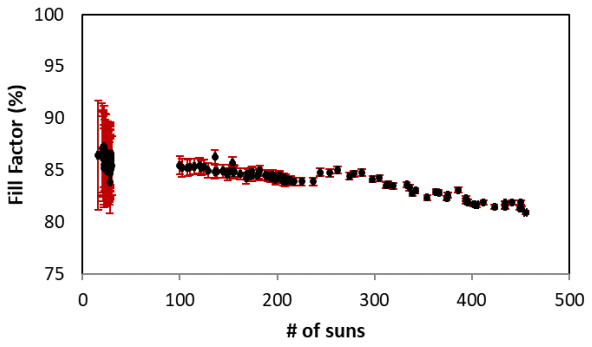


(c)

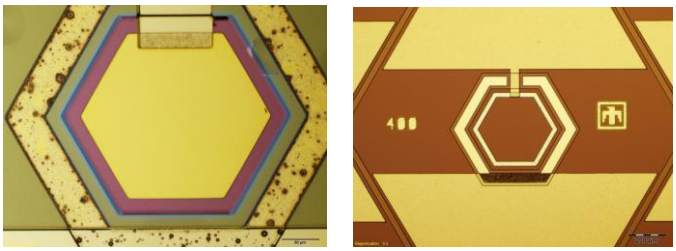
Figure 8: InGaP/GaAs bonded cell performance measurements under concentration. The scatter in the data at low concentration is due to the current being near the noise limit of the current meter as is seen with the larger measurement error bars. a) # suns vs. efficiency. Line is a fit to the data. b) # suns vs. V_{oc}, c) # of suns vs. fill factor.

IV. InGaAs Cells

InGaAs cells were designed for integration below an active Si cell to provide an added boost of efficiency at long wavelength IR. These cells would be especially relevant in hybrid microscale systems where the Si cell is used in the stack. They could also be an important component of a multi-junction wafer stack.

Layer	*Material*	*Thickness (nm)*
Window	n-InGaAsP	100 (Structure 1) 30 (Structure 2)
Emitter	n-InGaAs	300
Base	p-InGaAs	3,000
BSF	p-InAlGaAs	50
Contact	p-InGaAs	1,400

Figure 9: Cross section of bonded InGaAs cell including the epitaxial layer structure.



(a) (b)

Figure 10: (a) Bottomside micrograph of InGaAs cell bonded to Si. (b)Topside micrograph of InGaAs cell fabricated on InP substrate.

Two single junction InGaAs solar cells were fabricated. [11] One design was optimized for on wafer fabrication and testing. The other design was for cells bonded to a Si wafer. Although both material stacks are similar, there were differences in material thicknesses and doping levels to accommodate the fabrication differences. The epitaxial layer structure of the bonded cells (Structure 1) and on substrate cells (Structure 2) is shown in figure 9. Both stacks were an n-on-p design with an n-type emitter. Micrographs of both cell types are shown in Figure 10.

Initially, the overall material stack shared by both will be discussed. The entire material stack is designed to be lattice matched to the InP substrate. This improves the overall material quality and allows for the smooth surfaces needed for bonding cells. The absorber is lattice-matched InGaAs with a bandgap of 0.75 eV. The thickness of the layer was chosen based on the absorption of light between the Si and InGaAs bandgaps, growth limitations, and carrier diffusion lengths. The 3.3 µm thick absorber will absorb 95% of the available light without being limited by the diffusion length.

The window layer is lattice-matched InGaAsP with a bandgap of 1.11 eV. InGaAsP is chosen for its high valance band offset with InGaAs while maintaining a modest conduction band offset for the electrons. In the bonded cell design, the window layer also acts as the n-contact layer. Therefore, it is significantly thicker to reduce the spreading resistance and to maintain mechanical strength when the layer is exposed for electrical contacts.

The back-surface field (BSF) layer is lattice-matched InAlGaAs with a bandgap of 1.11 eV. This is chosen over InGaAsP for the higher conduction band offset with the InGaAs absorber. In both cell designs the InAlGaAs layer was a 40 nm thick.

The p-contact layer for both cells was lattice matched InGaAs. Since this layer is below the absorber, excess optical absorption is not an issue and p-type InGaAs is a good choice for its ability to produce a high quality ohmic contact. The final epitaxial layers were InGaAs and an InP etch stop below the cell to facilitate substrate removal.

A PECVD SiN layer of 40 nm was deposited on the InP wafer containing Cell Structure 1. A 10 nm layer of thermal oxide was grown on an inactive Si wafer. The dielectric on both wafers were activated with an O_2 plasma in an RIE. The two wafers were then bonded together at room temperature forming a Van der Waals bond. This bond was strengthened by using a bladder bonder to apply pressure of 25 psi and heating to 150° C for 12 hours. Subsequently, the entire InP substrate was removed using a selective HCl:H_3PO_4 wet etchant which stops on the InGaAs stop etch layer. Individual hexagonal cells were defined with a wet selective etch, stopping on the 1.2-eV InGaAsP window layer. Hexagonal cell shapes were chosen for their close approximation to the circular aperture of mating optics and to reduce the number of crystal faces exposed to the mesa wet etchant. The small size of the cells allows us to make contacts around the cell perimeter and to avoid the necessity of having electrical connections through the bonding interface. Cells ranging from 50 to 1200 µm were generated to evaluate the effect of cell size on performance. Contacts around the mesa perimeter were made to the n-type InGaAsP window using Ti\Au\Ag\Au. The p-type InGaAs layer was contacted using Ti\Pt\Au. Plated Au was used for probe pads and to ensure step coverage down the mesa. A single layer SiN anti-reflection

(AR) coating was applied to the topside of the Si substrate to improve coupling of the light into the cell.

Cell Structure 2 was fabricated on substrate. The mesa was dry etched using HBr:N_2 to expose the buried p-contact. The n-type InGaAs contact layer was removed from the window area using a selective wet etch. Contacts were deposited using e-beam deposition with Ti/Au/Ag/Au for the n-contact and Ti/Pt/Au for the p-contact. Plated Au was used for the probe pads and to ensure step coverage down the mesa. A metal on BCB was used to create a more accurately defined optical aperture for improved characterization.

Both sets of cells were characterized for quantum efficiency and performance with one sun illumination. For Cell Structure 1, all the measurements were done with the Si substrate side up. This causes the substrate to act like an optical filter and the InGaAs cell performance is the same as one would expect with an active Si cell above the InGaAs cell. For Cell Structure 2, the measurements were done without any filtering between the optical aperture and the light sources.

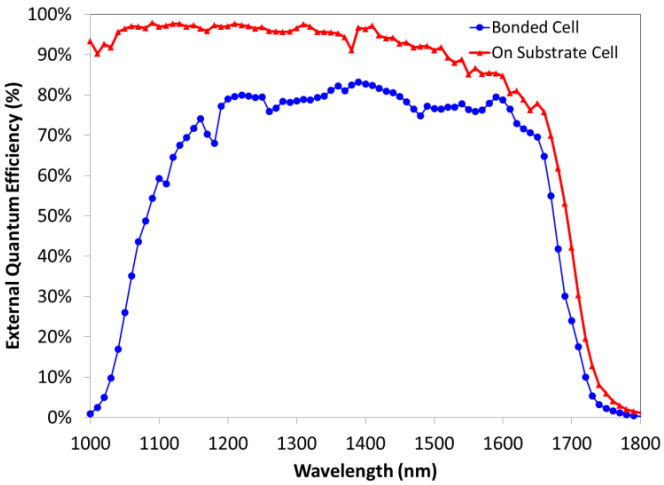


Figure 11: External quantum efficiency measurements for InGaAs cells

The external quantum efficiency of both cells was taken and data is shown in Figure 11. A large 4 mm by 4 mm square cell was used for this measurement to ensure under filling the aperture with the 1.5 mm spot size. The change in shape of the bonded cell compared with the on-substrate cell can be attributed to the imperfect single layer AR coating on the Si, the Si absorption and the bonding dielectric layer. Once these have been accounted for there is still about a 10% difference in the expected quantum efficiency. This is attributed to small bubbles in the bond interface which has a broadband transmission of ~70%. Therefore, the low hanging fruit to increase the device efficiency would be to improve the bond interface and use a broadband, multi-layer top AR coating.

The one sun measurements were done using an OAI class AAA solar simulator (from 300 to 1800 nm) with an intensity of 1 sun and spectrum AM 1.5 calibrated using a silicon reference solar cell. The output of the cell was measured using an Agilent B1500a semiconductor device parameter analyzer. Cell efficiency, fill factor, open circuit voltage (V_{oc}) and short circuit current density (J_{sc}) were extracted from the current-voltage curves obtained for each device. These parameters were then plotted as a function of device area for both cell structures (Figures 12-15).

Cell Structure 1 shows little variation in short circuit current density with area as one would expect. However, Structure 2 shows an increase in J_{sc} for smaller device areas. This is due to the cells absorbing light from outside of the optical aperture, including light that is reflected off the substrate. The metal aperture mask was an attempt to alleviate this effect, but the results indicate that the light scatter is beyond the mask extent. The much lower Jsc for Structure 1 is due to the portion of the spectrum absorbed by the Si substrate before the InGaAs cell.

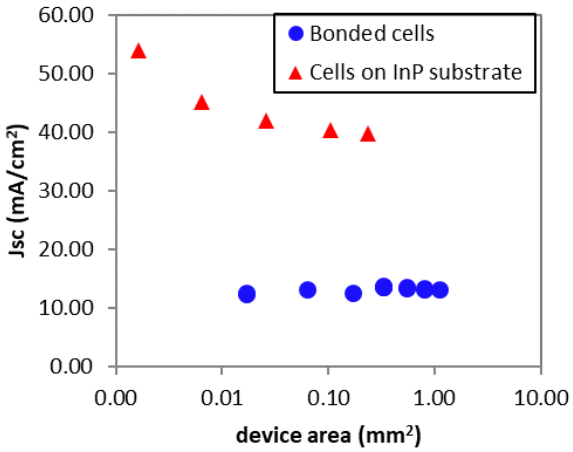


Figure 12: Device active area vs. short circuit current density for bonded cells and cells fabricated on substrate (1 sun with AM1.5 Global)

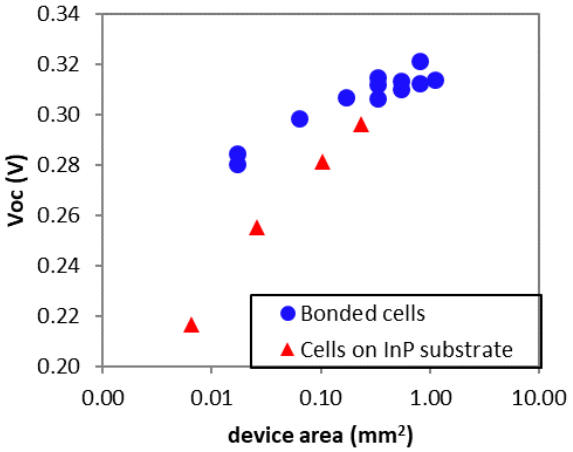


Figure 13: Device area vs. open circuit voltage for bonded cells and cells fabricated on substrate (1 sun with AM1.5 Global)

Both cell structures demonstrate a reduction in Voc as the device area decreases. This can be attributed to two separate

effects: perimeter current and excess dark current from absorber under the contacts. Cell Structure 2 has unilluminated absorber regions under the n-contact which contributes to the dark current. This area is proportionally larger as the cell size decreases. This is not applicable in Cell Structure 1 because there are no absorber areas shaded with contacts since the cell is back-contacted. The second cause for the decrease in V_{oc} is perimeter dark currents which is applicable to both cells. The perimeter to area ratio increases as the cell size decreases leading to a larger relative contribution by these dark currents and causing the decrease in V_{oc}. Fill factors and efficiency follow the same trends as V_{oc}. The lower efficiency for Structure 1 is again due to the optical filtering by the Si wafer.

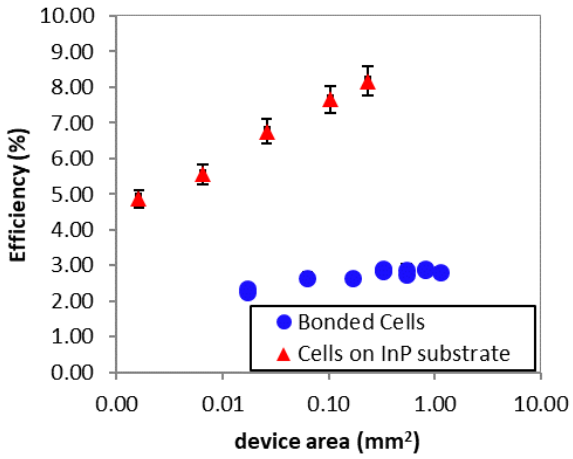


Figure 14: Device area vs. efficiency for bonded cells and cells fabricated on substrate (1 sun with AM1.5 Global)

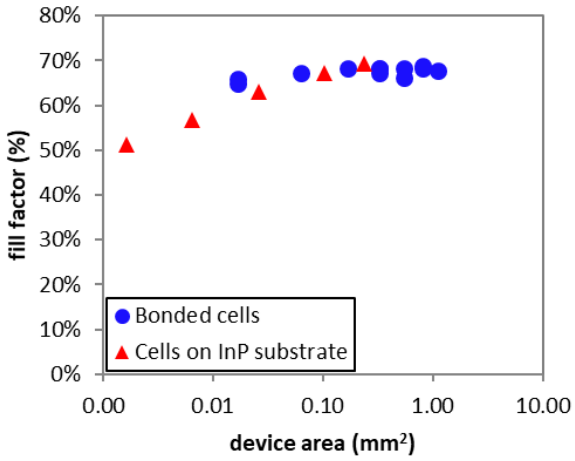


Figure 15: Device active area vs. fill factor for bonded cells and cells fabricated on substrate (1 sun with AM1.5 Global)

A theoretical maximum efficiency of 6% was expected for the Structure 1 cells. These cells demonstrated efficiencies of 2.25-3% mostly limited by the low open circuit voltage and fill factor. However, we know this comes from the material or cell design performance limitations since similar devices fabricated on substrate exhibit similar V_{oc} and fill factors.

Simulations were done to calculate the maximum short circuit current from the cell taking into account reflection losses from the air-Si interface, absorption in the Si substrate and absorption in the cell itself. The anti-reflection coating reduces the reflection losses to 1.75% of the solar spectrum with energy below the bandgap of Si. There will also be some loss associated with the bonded interface although that is not taken into account in the simulations. From these calculations, the expected current from the cell with an ideal global AM1.5 spectrum is 13.2 mA/cm^2. However, our testing lamp deviates from ideal and adjusting the spectrum according to the manufactures data gives an expected current of 14 mA/cm^2. This correlates well with the 12.5-13.6 mA/cm^2 measured in the actual devices indicating the bonded interface has maintained a low loss optical path.

V. Conclusions

Unique design considerations for microcells were introduced including how to design around the potentially increased spreading resistance from thin contact layers with perimeter contacts and parasitic dark current contributions from etched mesa perimeters. We have demonstrated III-V microcells intimately integrated with Si which could be utilized in next generation concentrated photovoltaic modules. Results from InGaP/GaAs and InGaAs hybrid cell configurations were reported. These cells employed integration techniques including wafer level bonding of processed cells and solder bonding of the cells. The cells themselves showed no evidence of degradation despite the integration process, which involved significant processing including the removal of the III-V substrate. It is expected that such integration approaches could be extended to more advanced multi-junction cells such as triple junction solar cells.

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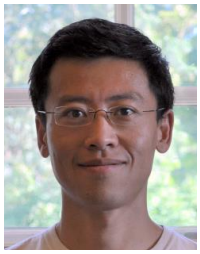

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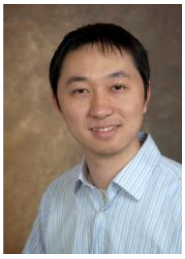

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