Supply Chain Management for Low-Volume, High-Variation Manufacturing

by

David Parry

B.S. Mechanical Engineering
Worcester Polytechnic Institute of Technology

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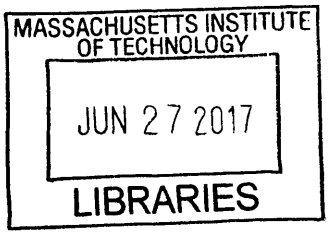

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Author: ..... Signature redacted

David Parry
System Design and Management Program

Certified by: ..... Signature redacted

Steven Spear
Thesis Supervisor
Senior Lecturer, Massachusetts Institute of Technology

Accepted by: ..... Signature redacted

Joan Rubin
Director, System Design and Management Program

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Abstract

This thesis introduces a low-volume, high variation manufacturing company that is experiencing issues managing its supply chain. Issues include lack of process ownership, poor requirements flow down to vendors, and an ineffective supplier selection process. This example uses a systematic approach for addressing re-occurring problems related to supply chain management. The premise underlying the approach exemplifies that modern process improvement techniques such a Lean Manufacturing boast large efficiency gains in operations, but fail to address pre-operation process issues such as supplier selection based on capability alignment.

By breaking down the current condition, issues within the current process and their associated root causes were identified. These included: inadequate internal processes, lack of access to information on supplier capabilities, and responsibility ambiguity. Corrective actions and countermeasures to these root causes such as: defined roles for the supplier selection process; a Supplier Capability Matrix; and internal requirements for supplier selection serve as a basis for a redesigned process. This results in a target condition that differs from the current in organizational structure, internal process requirements for supplier selection, and fewer non-conformance identified at incoming inspection.

This thesis also provides a proposal for transitioning towards the target condition via an incremental implementation. This process utilizes the scientific method as a methodology for incorporating new processes, and to validate their effectiveness on the overall system in a step by step fashion. Verification of improvement can serve as a business case for additional change and implementation.

This case study of a small electronics manufacturing company demonstrates the method in practical application. Results suggest that application is best suited for organizations that are looking to optimize their supply chain by reducing the risk of receiving non-conforming, or unusable material from their suppliers. The approach for identifying process issues, determining root causes, and implementing countermeasures provides a robust example for process improvement efforts.

Thesis Supervisor: Steven Spear

Title: Senior Lecturer, Massachusetts Institute of Technology

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Chapter 1: Background

Company Overview

Synergy Labs is a not-for-profit research and development company that designs, develops, and deploys computer electronics. They provide engineering services directly to government, industry, and academia. A primary focus of the laboratory's programs throughout its history has been the development and application of advanced technologies to for the U.S. Department of Defense. The lab's achievements include the design and development of accurate and reliable systems for wide range of aerospace, military, and commercial applications. Synergy Labs is a recognized world leader in engineering precision instrumentation, fault-tolerant systems, secure and assured systems, autonomous systems, and micro-fabrication. They build working prototypes for field-testing, accelerating design iterations, and small production runs.

While Synergy Labs' core expertise has been in D.O.D. and military systems, additional emphasis has recently been focused on research and development in innovative commercial applications. This is common trend among other D.O.D. contractors as they face new challenges due to a steep decline in federal spending, evolving customer needs, and the rise of new competitors.[i] The lab's position in the market place is for high quality, effective, and reliable electronics products that are highly customized to unique customer needs. In this regard, it distinguishes itself from companies like Lockheed Martin, Raytheon, and General Dynamics, which position themselves with higher volume offerings to a much broader market. Synergy Labs business expansion in mix and volume has created pressure to meet customer needs related to quality, costs, mix, volume, and delivery timing while also requiring the management of a more complex supply network. A variety of approaches are popular in practice for gaining control over manufacturing operations, Lean Manufacturing among these. The problem is, these techniques are often framed in terms of high-volume, low-variety repeatable manufacturing.[ii] Even when exclusively considering Synergy Labs' printed circuit assembly (PCA) business, customers expect vastly different functional requirements and design specifications.

Synergy Labs' role in the industry is to act as a technology accelerator by providing engineering services, and bring conceptual ideas into the real world. While they design and build physical products or prototypes, they are ***not*** a large scale, high-volume manufacturing organization. Synergy Labs works with commercial partners to transition technology from a low volume, proof of concept phase, to commercial large-volume production. Collectively, this creates an environment of low volume, high variation manufacturing for product builds at Synergy Labs.

Low-volume / High-variation Supply Chain Challenge

The advantages of low-volume, high-variation production are better tailoring to specific customer demand, improved responsiveness, and lower inventory requirements for finished goods. However, this production scheme has traditionally yielded lower quality output because of variation. Historically, low-variation, high-volume production is the optimal way to gain efficiencies and significant improvements in product quality. These benefits are not recognized by low volume, high variation manufacturers.[iii] While strategies like just-in-time manufacturing and demand-flow technology are important to high-volume, low-mix production, they may be inappropriate for high-mix, low-volume assembly. In contrast, high-mix manufacturers earn business based primarily on how quickly they can deliver exactly what their customers want. Cost and schedule are qualifiers for business, but are not always the most important considerations. Customers are expected to pay a premium to get what they want.[iv] The high-variation, low-volume scenario at Synergy Labs presents a particularly difficult challenge of producing customized products, being cost effective, and delivering extraordinarily high quality products without the typical benefits of large scale manufacturing. Synergy's business model has not changed in the regard that it is still engineering cutting edge, tailored designs to specific applications, with some measure of manufacturing the tailored product. However, expanding from the defense market to the commercial market, it has to simultaneously support a greater mix and volume of work than has been the case previously. While Synergy's management processes were sufficient for previous mixes and volume combinations, those management processes have not scaled easily for the greater complexity.

The ability to realize gains from a more efficient supply chain is not the same among companies with different product mixes and volume ratios. Some of the highly popular Lean concepts and tools such as level loading orders, using pull systems like Kanban, and demand forecasting, may not address the complexity of a high-variation, low-volume environment.[v] These methodologies are not applicable at Synergy Labs where highly customized products require the procurement of new materials on a case by case basis. Identifying value is trying to deliver to the customer what they want, when they want it, and at a competitive price. But, it is not that easy to achieve quality, cost and delivery when the benefit of learning by repeating the same work over and over again is absent, as is the case in any low-volume, high-variation production line.

One aspect of low-volume, high-variation manufacturing that can be particularly difficult is supply chain management. A high-volume, low-variation manufacturer producing consumer electronics for a broad global market has different leverage points and advantages within the supply chain than a low volume / high mix manufacturer who builds specialized technology products for a narrower market.[vi] For example, a high-volume, low-variation manufacturer producing standard personal computer motherboards can be expected to have relatively stable and predictable end-product demand. This can result in a small supply base providing many standard ship-to-stock components and materials. High volumes can be leveraged to reduce the ordering frequency, lower costs, and increase product quality. Conversely, a low-volume, high-variation manufacturer will require a larger variety of suppliers with highly unpredictable product demand, which increases the risk of receiving non-conforming or unacceptable material from their suppliers. This additional challenge amplifies the importance of having a robust supply chain management process, or system, with ability to select suppliers that can support a low-volume, high-variation manufacturer.

This challenge is prominent throughout Synergy Labs' PCA manufacturing business. Synergy Labs designs and develops electronic components and systems that integrate commercial-off-the-shelf (COTS) technology with internally developed custom packaging technology. PCAs are customized computer electronics that consist of a printed circuit board (PCB) and electronic components, such as resistors and capacitors. Designing and developing cutting edge technology via PCA manufacturing is one of Synergy Labs' core competencies and account for a significant

percentage of its annual revenue. Due to the fact of PCAs being highly customized in order to meet customer requirements, Synergy Labs relies on its suppliers to also provide customized PCBs to enable highly specific form, fit, and function.

The dual focus of cultivating cutting edge technology tailored to specific customer needs, and delivering high quality products requires a unique systematic approach to supply chain management. The value generated from receiving good from suppliers exceeds the benefits of shortened delivery schedules or lower cost of goods. The challenge presented at Synergy Labs creates an opportunity to develop a robust process for low-volume, high-variation manufacturers that are dedicated to fabricating exceptional quality products.

The purpose of this thesis is present a solution for the challenges at Synergy Labs as well as offering ideas about how to approach supply chain management, and more specifically supplier selection, for low-volume, high-variation manufacturers. The finding in this paper suggest solutions that can be implemented with minimal capital investment. The primary solution is a systematic approach to qualitatively and quantitatively mapping product requirements directly to defined supplier capabilities.

Chapter 2: Re-occurring Supply Chain Issues

Problem Introduction

Synergy Labs is discovering a high rate of PCB non-conformances at incoming inspection, which served as the catalyst for this project. Non-conformances negatively impact projects with respect to cost and schedule due to the time taken for investigation and disposition of non-conformances. There is also technical risk to programs should non-conformances not be discovered during incoming inspection, or simply accepted as-is. A key metric for measuring a successful supply chain at Synergy Labs is percentage of non-conforming material identified at incoming inspection. 86% of incoming PCB lots were identified as potentially non-conforming from June through December of 2016. 81% of those identified were confirmed as non-conforming. This alarming rate demonstrates the need for a closer look at the supply chain management process at Synergy Labs.

By pursuing a greater range of customers, coupled with the shift in technological focus to the commercial sector from primarily D.O.D. contracts, Synergy Labs has come to depend on a greater range of suppliers for a broader variety of component parts. This has exposed the company to the risk of supplier unreliability, particularly in terms of quality but also in terms of accuracy by mix, volume, and timing. Figure 1 below shows the average numbers of days for PCB incoming inspection steadily increasing over the 6 months of data collection provided by Synergy Labs employees. The trend of fewer inspections completed each month coinciding with more time spent at inspection provided the basis for an initial hypothesis.

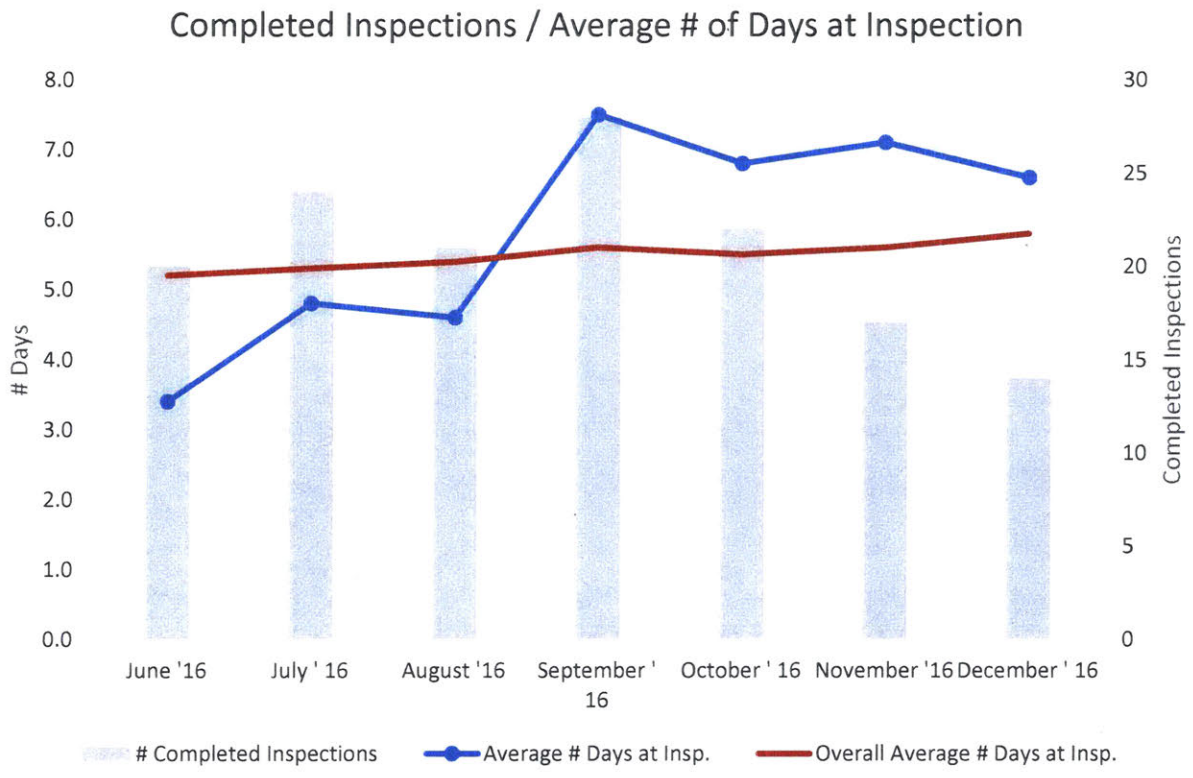

Figure 1 - Inspection Metrics

Initial Hypothesis

The source of difficulty with suppliers and the high rate of non-conformances links back to the supplier selection process. If Synergy Labs were more adroit at screening highly reliable suppliers, it would be less vulnerable to supplier caused disruptions and delays. In particular, the break down in supplier capability assessment results from a the fragmented fashion in which various internal stakeholders express their priorities and criteria, such that a holistic set of standards is not created.

Method for Testing Initial Hypothesis

The initial hypothesis was tested by documenting a detailed process description, mapping the process flow and compartmentalizing "what work was done, by whom, in what order". The "current condition" of commercial PCB supplier selection was recreated based on interviews with Synergy Labs employees, personal experience, observations, and internal documentation. The process was decomposed to the extent that every process generates an 'output' (in this case, criteria for evaluating supplier candidates) through a pathway of connected activities. The reconstruction will look for breakdowns in the flow of work (e.g., interruptions and unperformed tasks), connections (loss of information as it transits from one party doing one task to another), and activities (how individual work is performed to generate intermediate results).[vii]

This deep dive into the current condition for supplier selection enables root cause analysis for the issues and symptoms experience at Synergy Labs. The root causes identified by this approach can be assessed to confirm or disprove the initial hypothesis stated above. Chapter 3 initiates the approach to identifying root causes.

Chapter 3: Current Condition

Detailed Process Description

Below is a chronological list of the process steps currently involved with the product development, supplier selection, procurement, and inspection processes for Synergy Labs' PCA projects. Data was gathered via a combination of internal requirements documentation, quality assurance process maps, and interviews with the functional groups involved with the tasks. The list identifies the phase of product development, method of obtaining data, as well as functional groups and their responsibilities.

1. Planning Phase[1]

    a. Program Management (PM) works directly with customers to gain knowledge of the problem and obtain requirements for new product development projects. PM identifies customer's fundamental success criteria, identifies design goals, and establishes high-level product requirements. Requirements include technical specifications such as product dimensions, material preferences or restrictions, and physical and electrical functionality expectations.

    b. PM consults with engineering teams to formulate design approach and devise a preliminary PCA architecture. The team analyzes design feasibility, risks, and trade-offs.

    c. PM determines project scope, creates a preliminary design schedule, and finalizes product delivery requirements with the customer. PM holds a kick-off meeting all subsequent phases of product development and delivery.

[1] Detailed information about the Planning Phase was gathered via internal quality assurance process maps.

2. Concept Phase[2]

   a. The Design Team, which consists of Electrical and Mechanical Engineers, defines design options, researches technologies and potential solutions, and performs trade studies. The Design Team creates a preliminary design package that includes schematics, assembly drawings, parts lists, Computer Aided Drawing (CAD) models, and updates the project schedule with PM.

   b. The Design Team gathers input from other engineering groups such as Packaging and Systems Engineers to create a Conceptual Design Data Package for peer review. This includes more detailed CAD models, component and material specifications, and internal / external interface requirements.

3. Design Phase

   a. The Design Team refines the high-level design and creates a detailed Design Data Package. This data package includes items such as block diagrams, circuit concepts, interface designs, and interconnect diagrams (ICDs). All aspects of the PCB design must be documented during this step, including placement rules, layer stack up, grounding and shielding requirements, dimensional tolerances, and Institute for Printed Circuits (IPC) hardware classification.[3]

   b. The Design Team collaborates with Manufacturing Engineers to conduct an internal Design for Manufacturability (DFM) review. During the internal DFM review, the team assesses manufacturability of the PCBs, determines material availability and/or lead times for electrical components, and reviews difficulty of PCA assembly at Synergy Labs. The project team makes any necessary revisions to the contents of the Design Data Package based on internal DFM review.[4]

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[2] Roles, responsibilities and requirements for the Concept Phase were gathered from internal documentation for conducting product development.

[3] Requirements for contents of the Design Data Package were also derived from internal documentation for conducting product development.

[4] The process for DFM reviews was determined via several interviews with Synergy Labs Manufacturing Engineers.

c. Manufacturing Engineers identify potential PCB suppliers and conduct an external DFM. The Design Team and Manufacturing Engineers work with potential suppliers to determine feasibility, cost, and lead times based on requirements and expectations for PCBs. Revisions may be made to the contents of Design Data Package based on external DFM review if permissible. The suppliers submit quotes and expected delivery dates to Synergy Labs.

d. The Design Team, Program Management, and Manufacturing Engineers select a supplier(s) for PCBs. Suppliers selection is based on schedule, cost, and supplier capability. Schedule and cost inputs are provided directly from suppliers. Supplier capability is determined by a combination of supplier input and knowledge from Manufacturing Engineers. Manufacturing Engineers utilize anecdotal information within their department about a supplier's previous performances on other programs (if available). The Design Team, Program Management, and Manufacturing Engineers may opt to utilize two separate vendors to mitigate risk of missing delivery dates or receiving non-conforming material.

4. Procurement Phase[5]

a. Manufacturing Engineers collaborate with the Fabrication Team to create a Process Control Sheet that includes all process steps for assembly, inspection, and test. The Process Control Sheet is reviewed the Design Team, technicians, and Quality Assurance Engineers. The PCS includes build drawings, schematics, bill of materials (BOM) and interconnect diagrams (ICDs) for PCA fabrication.

b. The Design Team and Manufacturing Engineers submit the finalized the Design Data Package and Process Control Sheet to the Procurement and Fabrication Teams. The Procurement Team places orders with the selected supplier for PCBs utilizing the Design Data Package. *The Fabrication Team is responsible for ordering electrical components such as resistors and capacitors, however, the*

[5] The process for the Procurement Phase was gathered via additional interviews with Synergy Labs Manufacturing Engineers, as well as members from the Design, Fabrication, and Procurement Teams.

subsequent processes for components are beyond the scope of this thesis. The Fabrication Team builds an electronic Process Control Sheet within Synergy Labs' MRP system. The MRP system automatically generates Inspection Reports (IR) for each line item on the BOM, including PCBs.

5. Inspection Phase[6]

   a. Quality Assurance Inspectors (Inspectors) inspect PCBs received at Synergy Labs. Inspectors perform visual, mechanical, cross-section, and data package inspections. *Table* I *below includes a description of each type of inspection.* Inspectors inspect PCBs to ensure the hardware conforms to assembly drawings for the PCB, IPC standards, and any additional program instructions. If Inspectors identify any aspect of the PCBs to be non-conforming, the material is rejected in the Inspection Report that was created within the MRP system, and is physically segregated the hardware for dispositioning. Inspectors record high level details of any non-conformances found in the Inspection Report. A Discrepant Material Report (DMR) is automatically generated within the MRP system for any non-conforming material. Accepted PCBs are delivered to the stockroom and the process routes directly to step 17.

   b. Inspection Phase – Quality Assurance Engineers (QAE) work with members of the Design Team and Manufacturing Engineers to disposition DMRs in the MRP system. Material can be dispositioned as *not-a-defect*, *accept-as-is*, *return to vendor*, or *scrap*. QAEs record high level details of disposition reasoning in the DMR. DMRs dispositioned as *not-a-defect* or *accept-as-is* are delivered to the stockroom and the process routes directly to step 17. DMRs dispositioned as *return to vendor* or *scrap* automatically generate a Corrective Action Report (CAR) within the MRP system.

[6] Detailed information about the Inspection Phase was gathered via internal quality assurance process maps.

c. Inspection Phase – The Design Team and Manufacturing Engineers contact the PCB supplier to communicate issues and disposition the CAR. The Design Team and Manufacturing Engineers work with the supplier to clarify expectations and re-order PCBs, make adjustments to the Design Data Package and place a new order, or potentially revisit the supplier selection process identified in step 8. Synergy Labs may also issue a Supplier Corrective Action Request (SCAR) to the supplier regardless of CAR disposition.

d. Inspection Phase – QAEs drive additional root cause analysis and corrective actions in another software system at Synergy Labs, if funding from the program is available.

e. Inspection Phase – Inspectors are required to inspect additional orders for PCBs received as a result of the CAR. Any non-conformances follow process steps 12 through 15 again. Accepted PCBs are delivered to the stockroom.

6. Fabrication Phase[7]

   a. The Fabrication Team schedules assembly of the PCA and assigns the fabrication effort to Technicians. Material listed on the BOM, including accepted PCBs is issued to the Technicians to assemble the PCA. The Technicians deliver assembled PCAs to Inspectors for final inspection.

7. Final Inspection Phase

   a. Inspectors inspect PCAs to ensure the hardware conforms to assembly drawings for the Process Control Sheet, IPC standards, and any additional program instructions. Any non-conformances identified are routed through the DMR and CAR process. Accepted PCA are delivered to the stock room to be routed subsequent testing, integration into a higher level systems, or delivery to the customer.

[7] The process for the Fabrication Phase was collected during the interviews with the Fabrication Team.

The purpose of inspection is to efficiently identify and remove defects from products developed at Synergy Labs. Inspections are performed by Quality Assurance Inspectors as an impartial auditor, and are required on all programs at Synergy Labs that delivery products to customers. Table I identifies the four types of inspection that are performed for incoming PCBs. The table also includes why inspections are performed, the sampling plan, inspection requirements, and acceptable criteria for each type of inspection. Additional details on IPC standards are included in the Appendix.

Inspection	Why We Do It	Sample Plan	Requirements*	What Does Success Look Like?
Visual	• To examine for defects on the exterior surface of the PCB. Some internal defects are also detectable from the exterior. These defects can affect the reliability of the PCB. • To ensure the PCB finish is compliant with the drawing and thus meets customer requirements	100% (All PCBs inspected)	Purchase Order Drawing MIL-PRF-31032+ IPC-6010 series IPC-A-600 (Section 2)	• PCBs packaged & marked according to the drawing • PCB solder mask is compliant with requirements on the drawing • PCBs do not display any of the non-conformances described in IPC-A-600 Section 2
Mechanical	• To ensure the dimensions/ features of the PCB are compliant with the drawing and thus meet customer requirements	1 PCB per lot**, unless otherwise specified by QA#	Purchase Order Drawing IPC-A-600 (Section 2)	• Every dimension measured is within the tolerance specified on the drawing
Cross Section	• To examine for defects/ imperfections on the interior of the PCB. Internal defects can affect reliability • To ensure the PCB stack-up is compliant with the drawing and thus meets customer requirements	All coupons provided (1 set per Panel)	Purchase Order Drawing MIL-PRF-31032+ IPC-6010 series IPC-A-600 (Section 3)	• Dielectric thicknesses and conductor line/space widths are complaint with the requirements on the drawing • Plating and the final finish are compliant with the requirements on the drawing • PCBs do not display any of the non-conformances described in IPC-A-600 Section 3
Data Package	• To ensure the supplier has provided all documentation and test samples (for traceability purposes)	100% inspection	Purchase Order Drawing MIL-PRF-31032+ IPC-2221 (Section 12)	• All documentation (C of Cs, material certs, test reports) and samples (A/B Coupons, IST coupons) are delivered upfront (with the PCBs) • Documents are consistent (P/Ns, Date/Lot codes, WO #'s, etc. match on all) • Test Reports – Passing results • Samples are properly labeled, represent all panels and applicable features

Notes
* In order of precedence
** Lot = PCBs come from the same Supplier date/lot code
+ If applicable
# QA can request that additional PCBs be measured

Table I - Inspection Type Details

Process Mapping and Workflow

Figure 2Figure 2 below is a depiction of the PCA development and supplier selection process at Synergy Labs. While the chronological process flow appears relatively linear, the actual flow of information and hardware is high intertwined. The figure identifies all of the functional groups involved with design, procurement, inspection, and fabrication phases. The process steps are identified by the orange circles with corresponding number from the chronological list and arrows indicating the flow of information, data, or hardware The bulleted list below each functional group identify the types and formats of information or data that each group is required to use.

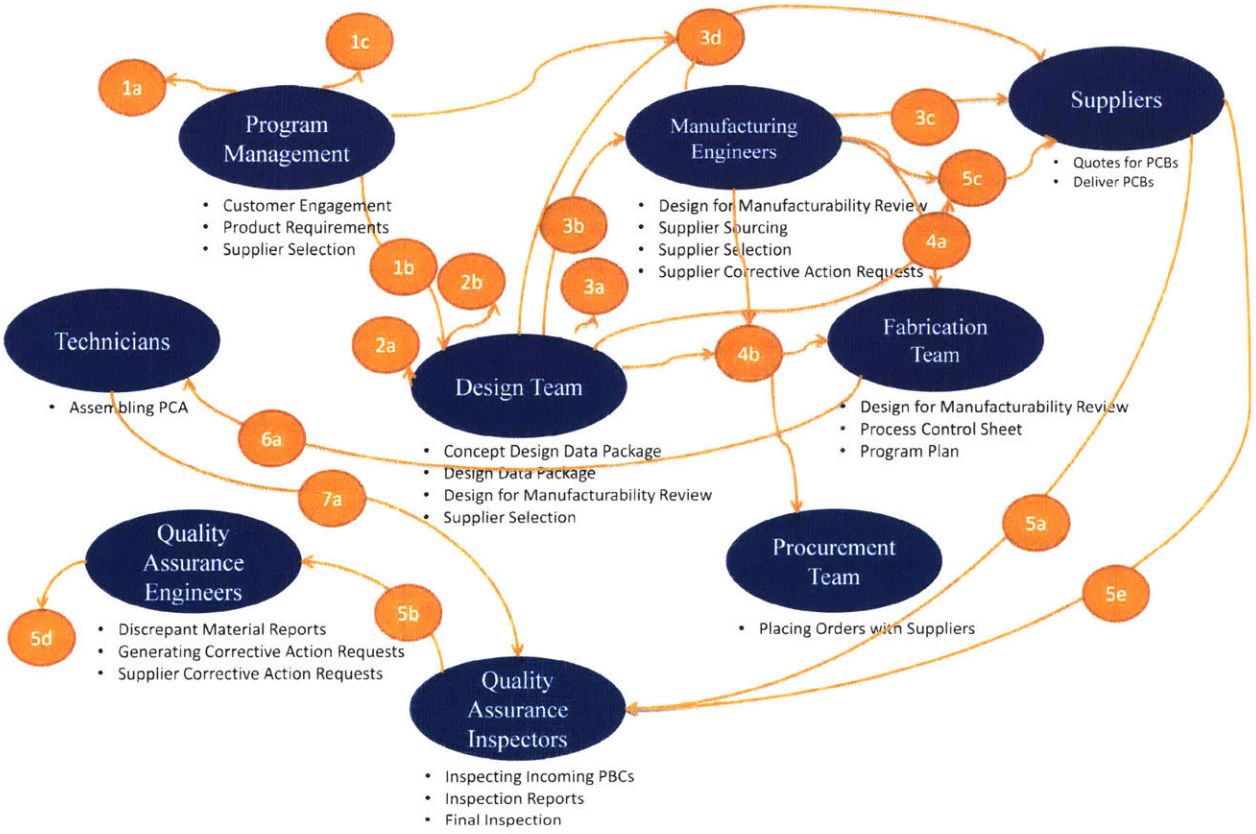

Figure 2 - Current Condition Process Flow Diagram

Functional Group Task Breakdown

Figure 3 below is the first step towards mapping out the current condition and identify which tasks are perform by whom. The figure lists all functional groups involved with the process and all of their associated tasks lined up in the corresponding row. This figure is also useful for identifying the distribution of workload throughout the process.

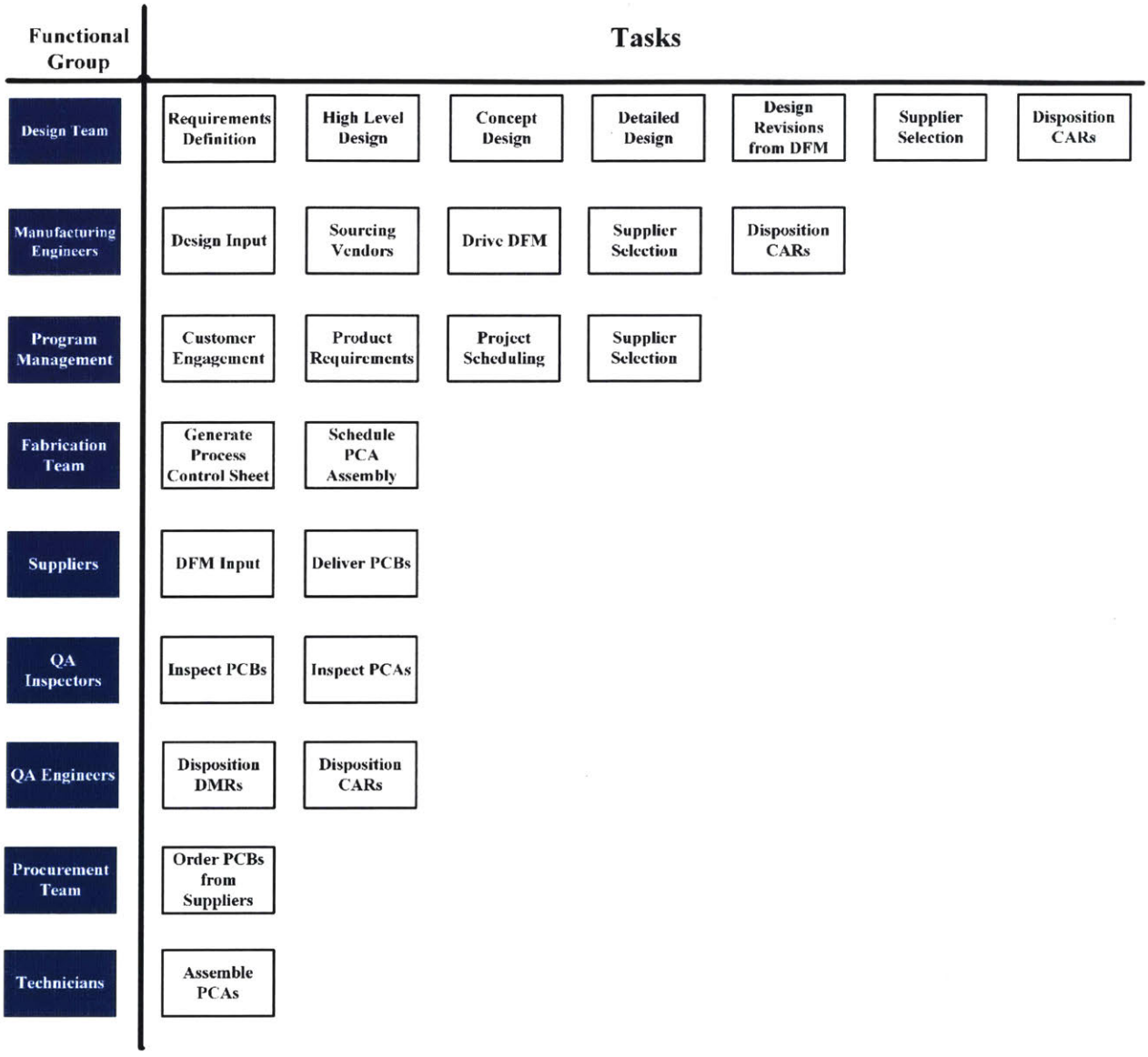

Figure 3 - Current Process Responsibility Breakdown

Chronological Workflow

Figure 4 is mapping of the current condition by identifying what tasks are perform, by whom, and in what order. The figure lists all functional groups involved with the process and all of their associated functions lined up in the corresponding row. This figure is also useful for identifying the phase and timeline of specific tasks throughout the process. The time table in terms of hours, days, or weeks may be highly varied based on complexity of the project, costs/funding, and availability of team members.

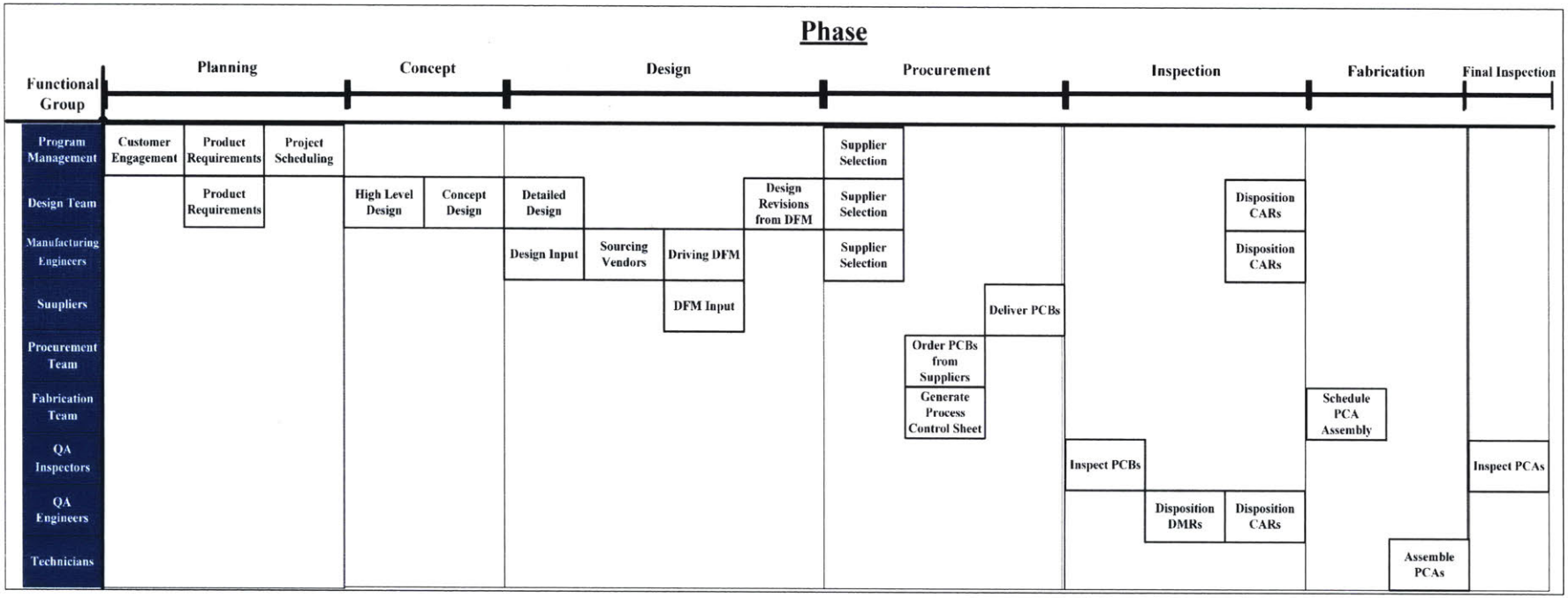

Figure 4 - Current Condition Chronological Workflow

Interdependencies

Figure 5 below represents the interdependencies within the inventory control process at Synergy Labs. The table shows which functional group is delivering information and to whom. The functional groups sending hardware, information, or data are on the left axis and the functional groups receiving hardware, information, or data are on the right axis. The orange circles indicate the associated process step from the chronological list and diagram.

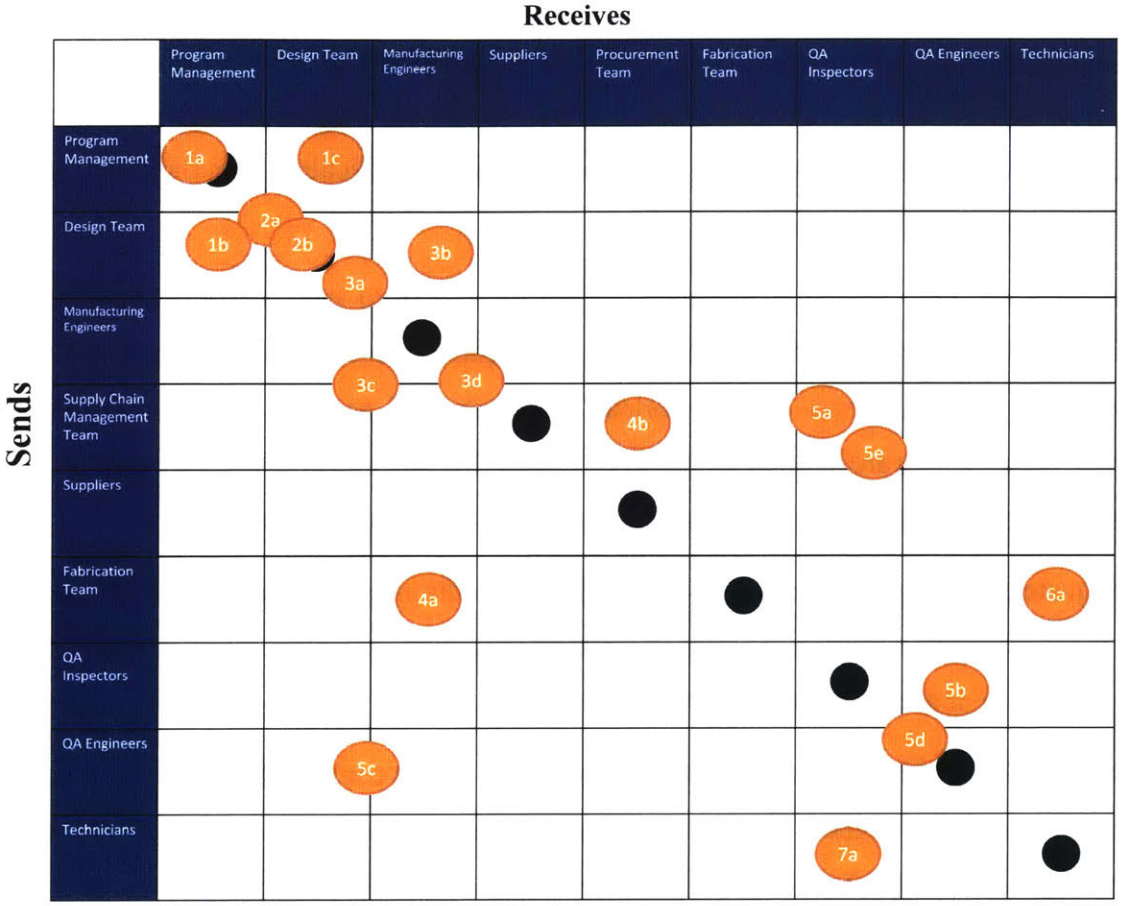

Figure 5 - Current Condition Interdependencies

The table reiterates the fact that overall process and flow of information is non-linear. This table also demonstrates that information is often passed to and from multiple functional groups at different steps. The lack of a clear process owner creates ambiguity and confusion which can lead to errors, omissions, and inefficiencies in the process.

Chapter 4: Process Diagnosis

Issues With the Current Condition

The process at Synergy Labs presents multiple issues like inefficiencies, lack of process ownership, and risk of improper supplier selection. The primary symptoms of these problems are listed below:

1. Programs are creating requirements and design specifications that cannot be fabricated by available suppliers. The Design Team is not properly assessing Design for Manufacturability early enough in the development process. While the Design Team ensures that features of the PCB are possible to manufacture, unique combinations of difficult to manufacture features can present problems for suppliers.
2. Suppliers are not adequately evaluated based on ability to meet requirements and design criteria. Supply Chain Management and supplier selection is primarily driven by Manufacturing Engineers with historical knowledge of previous supplier performances. Approved suppliers are defined for larger programs, but other smaller programs are responsible for picking suppliers without access to robust supplier capability identification.
3. Adequate defect analysis data is not being collected during the inspection, DMR disposition, or CAR disposition processes. Data and information from previous supplier performances is not available or accessible during the DFM process.
4. Over than 25% of PCB's delivered to Synergy Labs do not contain all required components of the data package needed for incoming inspection. The data package includes coupons, certificates of compliance, inspection/test results, and serial number identifications.
5. Lack of a robust supply chain management system or process does not currently exist. There is no central repository for qualitatively and quantitatively evaluating suppliers prior to selection, placing orders, communicating issues found at inspection, and issuing Supplier Corrective Action Requests.

Exchanges and Connections

Figure 6 below is the next step for mapping the current condition and identifying where issues occur throughout the current condition. The dashed **blue** lines indicate the flow of information, hardware, or data between the functional groups. The **red**, numbered kaizen bursts indicate where the problems occur throughout the process are labeled by the corresponding number for each problem listed in the "Problems" section above. Problem #5 occurs throughout the entire process. This kaizen burst is located at one example of where the problem occurs rather than each spot to avoid redundancy. The **black** kaizen bursts (labeled with L's) indicate where the process loops back and creates a less efficient, non-linear flow. The **red** arrow depicts where the process may be repeated due to receiving non-conforming PCBs from suppliers.

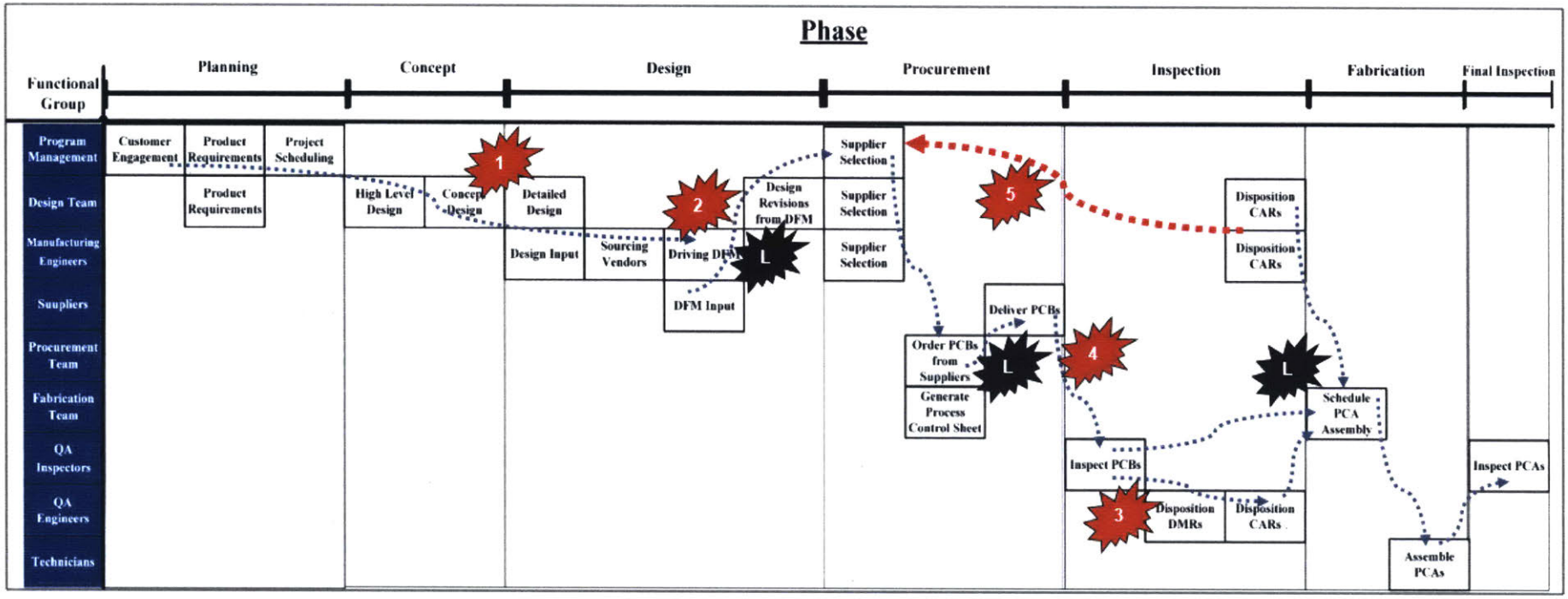

Figure 6 - Current Condition Chronological Workflow with Exchanges and Connections

Root Cause Analysis

Between June 2016 and December 2016, programs were affected by non-conforming PCBs from 25 different suppliers with a 5 day average delay due to investigation of non-conforming product. Efforts to determine root causes for non-conforming PCBs were kicked off in January of 2017 by Manufacturing Engineers at Synergy Labs. Initial root causes and contributing factors were identified based on existing non-conformance data and anecdotal information from functional groups involved with the overall process. The existing data was very limited and did not have enough resolution for useful trending analysis. Suspected root causes and contributing factors were identified by Manufacturing Engineers at the projects inception, and are included below:

Preliminary Root Causes

1. Design of PCB's not taking "Design for Manufacturability" into account
2. Self-imposed non-value added requirements; Over-specification of PCB's
3. Suspected lack of process control at PCB suppliers

Preliminary Contributing Factors

1. Insufficient understanding of supplier capabilities and core competencies
2. Poor flow down of documentation/traceability requirements to suppliers
3. Lack of issuance of Corrective Actions to suppliers (IPC-A-600)
4. Data being captured for defect identification is not sufficient to support root cause analysis of PCB non-conformances
5. Number of PCB suppliers (Total Qty. 28) exceeds current bandwidth of Supplier Quality to support

Upon further investigation, with the help of Quality Assurance Engineers, root causes were agreed upon for each of the major problems that Synergy Labs was experiencing. Table II below identifies the problems listed above, and identifies root causes for each issue.

Problem #	Problem Description	Root Cause
1	Programs are creating requirements and design specifications that cannot be fabricated by available suppliers. The Design Team is not properly assessing Design for Manufacturability early enough in the development process.	The Design Team does not have access to adequate information required to properly account for feature combinations and supplier capabilities.
2	Suppliers are not adequately evaluated based on ability to meet requirements and design criteria.	Supply Chain Management and supplier selection is primarily driven by Manufacturing Engineers without adequate supplier capability knowledge and previous supplier performance data.
3	Adequate defect analysis data is not being collected during the inspection, DMR disposition, or CAR disposition processes.	There is no process in place to ensure useful information is generated during disposition. The current instance of the MRP does not support the ability to collect this information.
4	Over 25% of PCBs delivered to Synergy Labs do not contain all required components of the data package needed for incoming inspection.	Multiple points of contact between Synergy Labs and suppliers without a standardized request process for data package requirements.
5	Lack of a robust supply chain management system or process does not currently exist.	Responsibilities for supply chain management are spread across several functional groups without standardized procedures in place.

Table II - Problems and Root Causes

Chapter 5: Initial Conclusions

Hypothesis Confirmation

Based on the exercise from Chapter 3, root causes were identified for the problems that are occurring with PCB suppliers at Synergy Labs. The chronological process mapping and workflow diagrams helped to diagnose the symptoms of the current condition. Table II lists the root causes identified for each issue that occurs throughout the overall process. All of the root causes confirm the initial hypothesis that "If Synergy Labs were more adroit at screening highly reliable suppliers, it would be less vulnerable to supplier caused disruptions and delays. In particular, the break down in supplier capability assessment results from a the fragmented fashion in which various internal stakeholders express their priorities and criteria, such that a holistic set of standards is not created." While each of these root causes correlate directly to a specific problem with the current system, they are also validate the original hypothesis of several breakdowns in the supplier selection process.

The root causes in Table II also provide an opportunity to address each problem individually with a corrective action or countermeasure. **Error! Reference source not found.** below includes the root causes from Table II, and suggested countermeasures for each associated root cause. Each countermeasure is intended to alleviate the symptoms of the current condition, and provide a foundation for developing a new process. These countermeasures suggest incorporating new technology to standardize the flow of information, restructuring the organization to clearly define roles and responsibilities, and creating a streamlined process. Collectively, these countermeasures also serve as a support for a new hypothesis.

Suggested Countermeasures

RC#	Root Cause	Countermeasure / Corrective Action
1	The Design Team does not have access to adequate information required to properly account for feature combinations and supplier capabilities.	Provide Design Team with access to supplier capabilities during the design phase through a Supply Chain Management (SCM) system
2	Supply Chain Management and supplier selection is primarily driven by Manufacturing Engineers with adequate supplier capability knowledge and previous supplier performance data.	Establish a Supplier Capability Matrix to select suppliers based objectively on capability mapping and proven success via previous performances.
3	There is no process in place to ensure useful information is generated during disposition. The current instance of the MRP does not support the ability to collect this information.	Implement a SCM system to utilize information gathered during inspection processing and DMR / CAR disposition
4	Multiple points of contact between Synergy Labs and suppliers without a standardized request process for data package requirements.	Establish a single point of contact between Synergy Labs and suppliers via a Supply Chain Management Team.
5	Responsibilities for supply chain management are spread across several functional groups without standardized procedures in place.	Establish a Supply Chain Management functional group that are responsible for developing and carrying out best practices for all procurement efforts

Table III - Root Causes and Countermeasures

A Need for Change

Considering the suggested countermeasures identified in **Error! Reference source not found.**, the supply chain management process is in need of a significant change. The suggested approach to these issues would be to establish a supply chain management department at Synergy Labs, and utilize software tools to manage supplier capabilities and performance in a systematic way. The lack of a supply chain management team places the responsibilities across several other functional groups, which has led to a high rate of non-conformances on incoming PCBs. A Supply Chain Management Team that spanned the development, procurement, and inspection processes could be capable of aggregating useful data and information generated at each step. While the supply chain management team would support multiple steps throughout the process, the ideal setup would not require direct involvement with each one. Utilization of a Supply Chain Management (SCM) System could provide information that is readily available to all functional groups at any point in the process. The role of the supply chain management team would be to support product design, drive supplier selection, and gather data from incoming inspection and non-conformances.

The overall goal of implementing a new process and system would be to adequately evaluate suppliers based on capability and performance. This iterative process may also lead to narrowing the field of potential suppliers, which in turn would increase the volume of orders through each supplier. This would give Synergy Labs more leverage for negotiating costs, schedule, and issuing SCARs to drive process improvement.

Value Proposition for Change

Managing risk is a key responsibility for business leaders, and supply chain management systems allow for the identification of critical risk factors in an organization or with their suppliers. Supply chain methodologies assist management with organizing risks and ascertaining the potential for internal or external failures. Without effective supply chain management systems, many companies are exposed to product quality, cost, schedule, and even legal risks.[viii]

Effective supply chains give businesses a competitive advantage in the marketplace and help mitigate risks associated with acquiring raw materials and delivering products or services. By implementing supply chain management systems, businesses are able reduce waste, overhead costs and shipping delays. The benefits of this systematic approach impacts areas ranging from product quality to order turn-around times.[ix] The value of improving a supply chain for a small scale manufacturer of highly customized products can be a significant differentiator that provides a competitive advantage. The benefits from cost reduction and shorter lead times can passed along to Synergy Labs' customers, which in turn can bring in more business.[8]

Product quality within the supply chain has become a pressing issue at Synergy Labs. Defects and rework attributable to supplier selection are raising the costs of doing business. One of the advantages of supply chain management is that it incorporates quality techniques to improve operations and reduce the risk of receiving defective or non-conforming material from suppliers.[x]

The matrixed organization of Synergy Labs leads to many internal programs working in isolation of one another. This setup creates enables various programs to select suppliers and place orders without the knowledge of their capability to meet the rigorous standards set for Synergy Labs products. As e-commerce continues to grow globally, more options are available for supplier selection than ever before. More options coupled with siloed efforts further compounds the challenge of effective supplier selection.[9]

A more effective supply chain could help Synergy Labs increase customer confidence; bring in new customers; enable a quicker process for supplier selection; and meet deliverables more consistently. The suggested target conditional also utilizes information feedback from incoming inspection to be utilized for supplier selection, effective creating an environment of continual improvement.

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[8] Based on interviews with Synergy Labs Program and Senior Management
[9] Based on interviews with Synergy Labs Procurement Team and Quality Assurance Engineers

Business Case for Change

The current process opens several opportunities for human error and hardware processing delays. Improved supply chain management and supplier selection helps to mitigate the risk of receiving non-conforming material. A more effective process will enable Synergy Labs reduce unnecessary costs for labor hours associated with defect detection, non-conformance disposition, and the risk of product failures. "Doing more with less" has been the trend year after year for many government, military, or defense contracts, which increases the pressure to become more cost effective. Improved supply chain management and quality will increase our customer's confidence in Synergy Labs to produce reliable systems. Both aspects will help to ensure that the lab maintains its competitive edge over competitors.

If a systematic process for supplier selection results in utilizing fewer, more successful suppliers, the same volume of orders would distributed across a narrower field. This could potentially lead to more leverage for lowering costs of boards given repeated partnership with suppliers. Other potential benefits include information system integration with suppliers for advanced ordering and forecasting; standard methods of procurement to ensure requirements and expectations are met; and overall improved relationships between Synergy Labs and suppliers. Lastly, establishing processes and procedures for procurement of PCBs can be used to procure other hardware types at Synergy Labs and open new business opportunities.

Chapter 6: Target Condition

Second Hypothesis

Given the findings in Chapter 3, revisions in the process flow, information exchanges, and task execution, and improved supplier selection will dramatically reduce the occurrence of non-conformances. This chapter identifies the suggested target condition for supply chain management at Synergy Labs. This approach assumes the implementation of a supply chain management team, new software tools, and programs utilizing supplier selections generated based on capability, rather than cost or schedule. With the suggested countermeasures in place, the second hypothesis can be established: If Synergy Labs incorporates a new Supply Chain Management Team, coupled with an effective SCM system, it can reduce the percentage of non-conforming PCBs identified at incoming inspection from 85% to less than 25%.

Target Condition: Detailed Process Description

Below is a ***revised*** chronological list of the process steps involved with the product development, supplier selection, procurement, and inspection processes for Synergy Labs' PCA projects. The list identifies the phase of product development, as well as the associated functional groups and their responsibilities.

1. Planning Phase

    a. Program Management (PM) works directly with customers to gain knowledge of the problem and obtain requirements for new product development projects. PM identifies customer's fundamental success criteria, identifies design goals, and establishes high-level product requirements.

    b. PM consults with engineering teams to formulate design approach and devise a preliminary PCA architecture. The team analyzes design feasibility, risks, and trade-offs.

c. PM determines project scope, creates a preliminary design schedule, and finalizes product delivery requirements with the customer. PM holds a kick-off meeting all subsequent phases of product development and delivery.

2. Concept Phase

   a. The Design Team generates a preliminary design package that includes schematics, assembly drawings, parts lists, Computer Aided Drawing (CAD) models, and updates the project schedule with PM.

   b. The Design Team gathers input from other engineering groups such as Packaging and Systems Engineers to create a Conceptual Design Data Package for peer review. This includes identification of any key design parameters and features. The Design Team is responsible for verifying that the combination of features is feasible for manufacturing by querying the SCM system prior to completing the Concept Phase.

3. Design Phase

   a. The Design Team refines the high-level design and creates a detailed Design Data Package. All detailed aspects of the PCB design must be translated into key features and verified for feasible within the SCM system again.

   b. The Design Team collaborates with Manufacturing Engineers to conduct an internal Design for Manufacturability (DFM) review. During the internal DFM review, the team assesses manufacturability of the PCBs based on supplier capabilities identified within the SCM system. The project team makes any necessary revisions to the contents of the Design Data Package based on internal DFM review.

4. Procurement Phase

   a. The Design Team and Manufacturing Engineers submit the finalized the Design Data Package to the SCM system. The Supply Chain Management Team validates information from the Design Data Package into the SCM system.

b. The SCM generates PCB supplier suggestions based on an evaluation of design parameters, required key features, and supplier capabilities. The Supply Chain Management Team works with the Suppliers to confirm feasibility, cost, and lead times based on requirements and expectations for PCBs. The suppliers submit quotes and expected delivery dates and are recorded in the SCM system.

c. The Supply Chain Management Team select a supplier(s) for PCBs. Suppliers selection is based on supplier capability, cost, and schedule in respective order. Two separate suppliers may be utilized to mitigate risk of missing delivery dates based on input from Program Management. The Supply Chain Management Team places orders for all material (including PCBs) through the SCM systems and updates expected delivery dates. Information from the Design Data Package information within the SCM system is automatically delivered to Synergy Labs' MRP system.

5. Fabrication Planning Phase

   a. The Fabrication Team builds an electronic Process Control Sheet within Synergy Labs' MRP system utilizing the Design Data Package information sent from the SCM system. The Process Control Sheet that includes all process steps for assembly, inspection, and test. The MRP system automatically generates Inspection Reports (IR) for each line item on the BOM, including PCBs.

6. Inspection Phase

   a. Suppliers deliver PCBs to Synergy Labs and electronically send all required data package information to the SCM system. The data package information is automatically attached to the associated Inspection Reports in the MRP system. The SCM system automatically notifies the Supplier of any missing information.

   b. Quality Assurance Inspectors (Inspectors) inspect PCBs received at Synergy Labs. Inspectors perform visual, mechanical, cross-section, and data package inspections. If Inspectors identify any aspect of the PCBs to be non-conforming, the material is

rejected in the Inspection Report within the MRP system, and is physically segregated the hardware for dispositioning. Inspectors record specific details utilizing pre-populated drop-down options to identify specific reasons for rejecting material. Data inputs from the Inspection Report are automatically delivered to the SCM system. A Discrepant Material Report (DMR) is automatically generated within the MRP system for any non-conforming material. Accepted PCBs are delivered to the stockroom and the process routes directly to step 16.

c. Quality Assurance Engineers (QAE) work with members of the Design Team and Manufacturing Engineers to disposition DMRs in the MRP system. Material can be dispositioned as *not-a-defect*, *accept-as-is*, *return to vendor*, or *scrap*. QAEs record specific details utilizing pre-populated drop-down options to identify specific reasons for DMR disposition. DMRs dispositioned as *not-a-defect* or *accept-as-is* are delivered to the stockroom and the process routes directly to step 16. DMRs dispositioned as *return to vendor* or *scrap* automatically generate a Corrective Action Report (CAR) within the MRP system. Data inputs from the DMR are automatically delivered to the SCM system.

d. The Supply Chain Management Team contacts the PCB supplier to communicate identified non-conformances. The Supply Chain Management Team works with the supplier to clarify expectations and re-order PCBs, make adjustments to the Design Data Package and place a new order, or potentially revisit the supplier selection process identified in step 8 based on input from Program Management and the Design Team. The Supply Chain Management Team may also issue a Supplier Corrective Action Request (SCAR) to the supplier regardless of CAR disposition.

e. Inspectors are required to inspect additional orders for PCBs received as a result of the CAR. Any non-conformances follow process steps 12 through 14 again. Accepted PCBs are delivered to the stockroom.

7. Fabrication Phase

    a. The MRP system automatically schedules assembly of the PCA and assigns the fabrication effort to Technicians. Material listed on the BOM, including accepted PCBs is issued to the Technicians to assemble the PCA. Completed PCAs automatically generate Final Inspection Reports within the MRP system.

8. Final Inspection Phase

    a. Inspectors inspect PCAs to ensure the hardware conforms to assembly drawings for the Process Control Sheet, IPC standards, and any additional program instructions. Any non-conformances identified are routed through the DMR and CAR process. Accepted PCA are delivered to the stock room to be routed subsequent testing, integration into a higher level systems, or delivery to the customer.

Target Condition: Process Mapping and Workflow

Figure 7 below is a depiction of the predicted target condition for inventory control. The figure identifies all of the functional groups involved with inventory control for piece parts. The process steps are identified by the orange circles with corresponding number from the chronological list and arrows indicating the flow of information, data, or hardware.

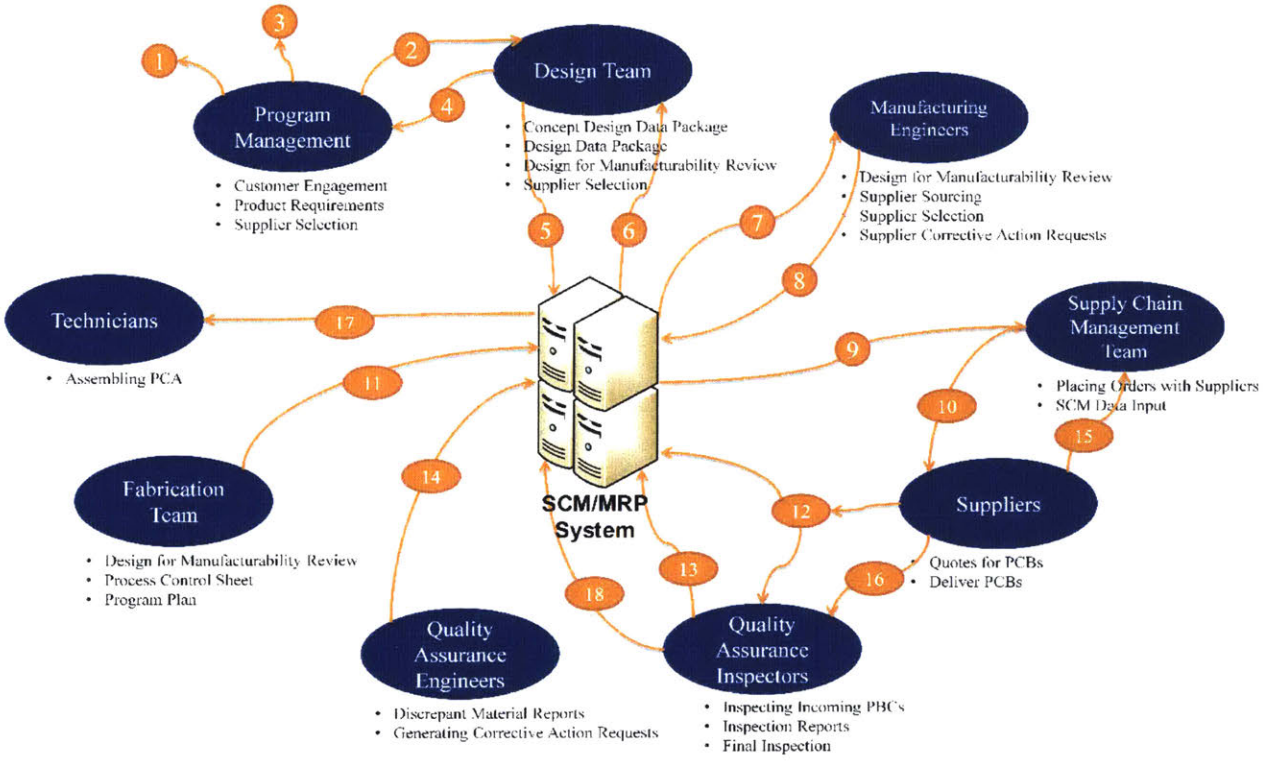

Figure 7 - Target Condition Process Flow Diagram

Target Condition: Chronological Workflow with Exchanges & Connections

Figure 8 maps out the predicted target condition and identifies "what work by whom in what order". The figure lists all functional groups involved with the process and all of their associated functions lined up in the corresponding row. The dashed **green** lines indicate the flow of hardware, information, or data between the functional groups. The kaizen bursts from Figure 4 have been removed, as the symptoms in the current condition have been alleviated. The **red** arrow lines are only part of the process flow when non-conforming PCBs are received from suppliers. The likelihood of requiring this step is significantly reduced due to improved supplier selection based on capability and proven success. The predicted target condition maintains a linear progression of tasks throughout the entire process. The use of a SCM system as the "central hub" eliminates the need for any loops in the process flow. This creates a steady progression and exchanges between functional groups.

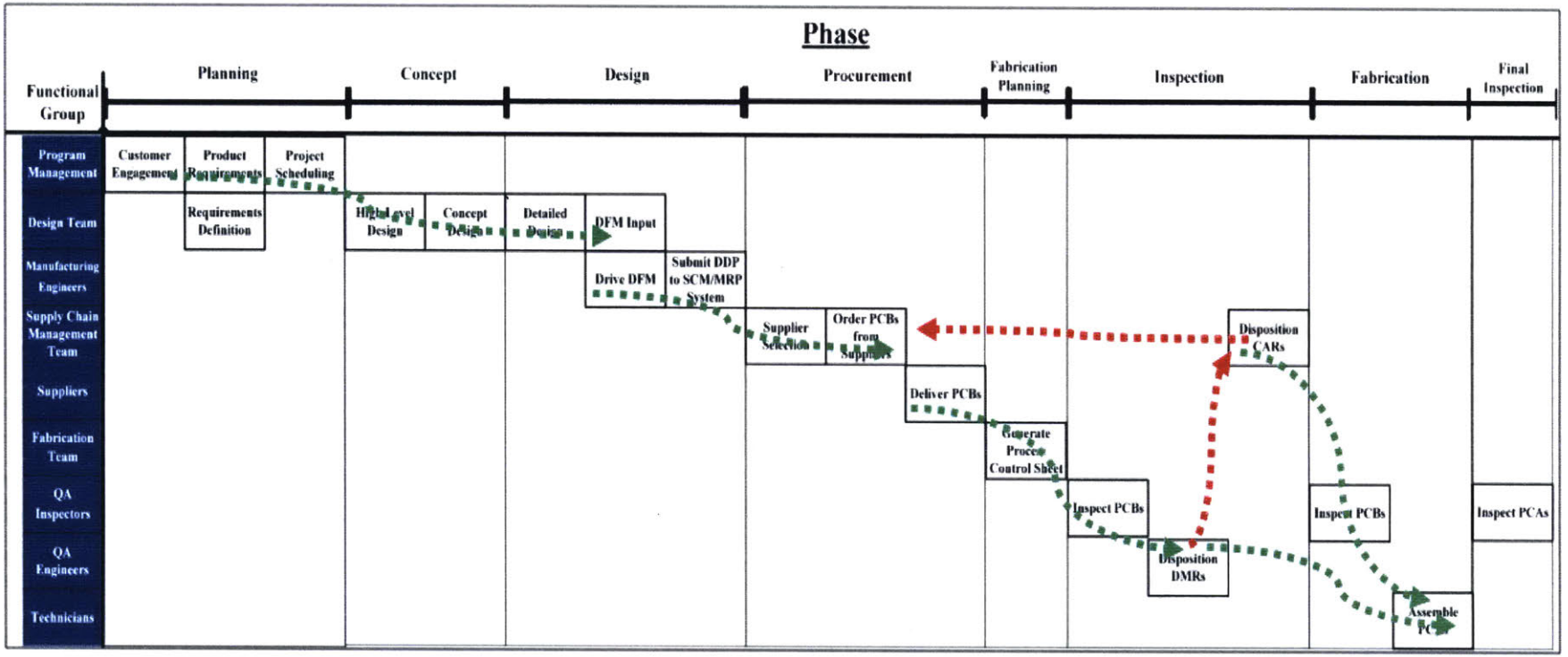

Figure 8 - Target Condition: Chronological Workflow with Exchanges & Connections

Target Condition: Interdependencies

Figure 9 below represents the interdependencies for the predicted target condition and new process flow for supply chain management at Synergy Labs. The table shows which functional group is delivering information and to whom. The orange circles indicate the associated process step from the chronological list and diagram.

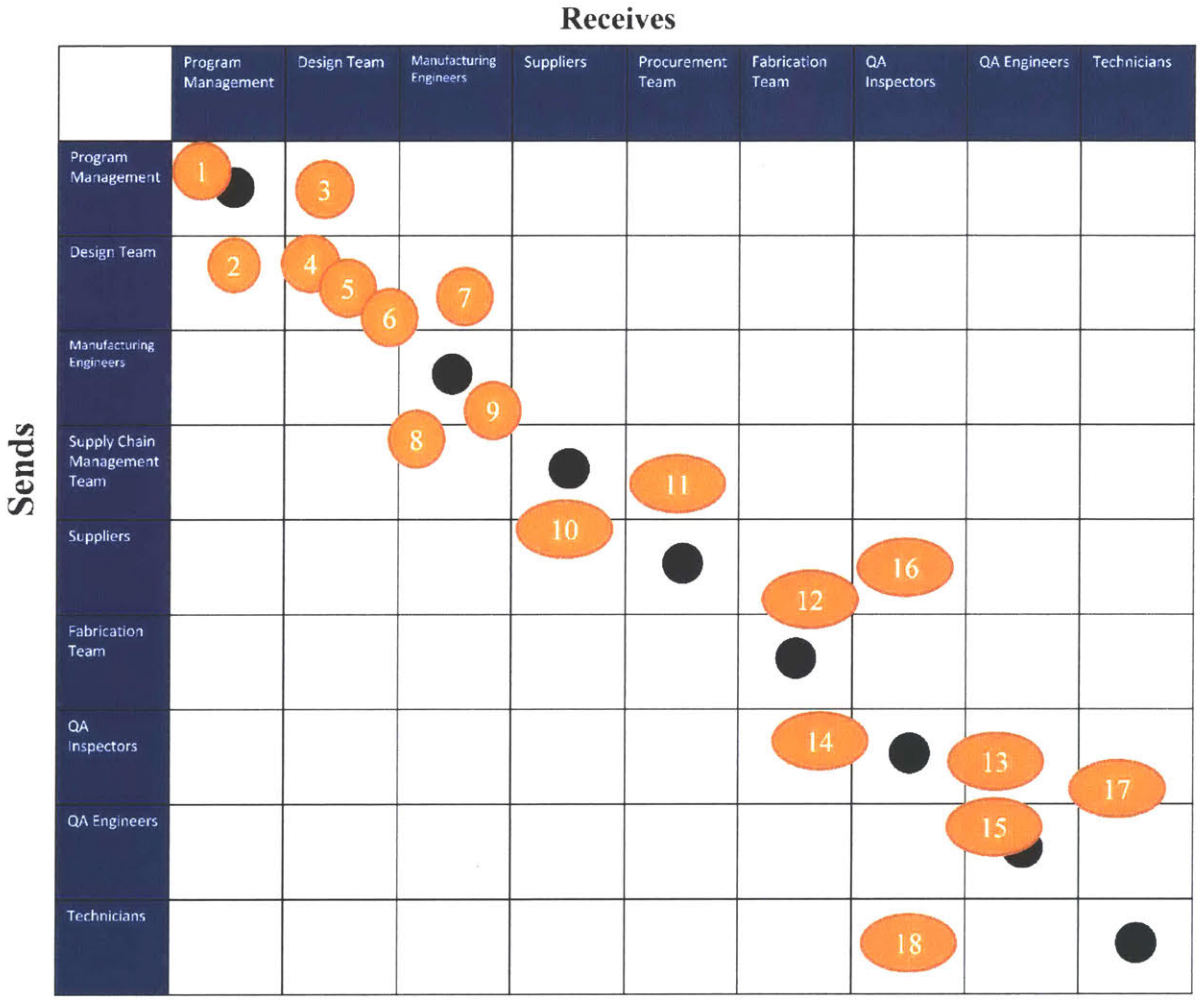

Figure 9 - Target Condition Interdependencies

Chapter 7: Incremental Implementation

Method for Testing Second Hypothesis

Chapter 6 describes the suggested process for supply chain management to address the root causes that are creating issues at Synergy Labs. However, the implementation of this new process would be an extensive project with significant capital investment required. This would require stakeholder buy-in, as well as senior management approval and funding. Therefore, an incremental approach and implementation is the most likely scenario. Chapter 7 describes two discrete test cases to help validate the second hypothesis. Test Case #1 defines a standardized procurement process, while Test Case #2 simulates the utilization of a Supplier Capability Matrix during the DFM process. The approach for each process improvement will follow the scientific method to ensure proper monitoring and useful information for adjustments and iterations. The results from each test case can then serve as a basis for additional implementation and a business case to be presented to senior management.

The process for DFM is failing to ensure proper supplier selection based on their capabilities. The main objective for DFM in the current condition is to validate that the design of the PCB's are theoretically possible based on features than can be manufactured. However, this process falls short in considering the actual capabilities of potential suppliers. While suppliers provide some feedback on their capabilities, an adequate evaluation is not being conducted. These two test cases provide an opportunity to address the root causes #2 and #4 identified in Table II, and implement countermeasures to improve the current condition incrementally. The suggested changes require minimal investment costs in terms of both time and dollars. These suggestions are intended to be a pathfinder case for future process changes and potential migration towards the recommended target condition. The goal of these process changes is to reduce the number of non-conformances found at incoming inspection. Any improvements can be quantified in terms of cost savings, and act as a the rationale for subsequent changes and any required capital investment. While the results from these test cases cannot be precisely displayed in terms of dollars, the level of quality control also strengthens the relationship with customers and bolsters the reputation of Synergy Labs for processing strategic hardware. This reputation is an invaluable asset for bringing in new customers.

Test Case #1 – Standard Procurement Process

In an effort to combat the re-occurring non-conformances that are found at incoming inspection, the Synergy Labs needs to have a standardized process for supplier selection and communicating requirements. Suppliers are currently selected by engineers during the DFM process, but orders are placed by the procurement team. The multiple points of contact leads to confusion and ambiguity in requirements for delivery. Suppliers receive requirements via a wide range of documents, which causes data package non-conformances at incoming inspection. While data package omissions or errors are not directly attributed to issues with the hardware itself, the traceability and validation process is required for any material used for a product that is delivered to customers. The hardware cannot be accepted and used for PCA builds if any discrepancies are found. Non-conformances identified due to data package issues can and should be easily avoidable with improved communication between Synergy Labs and suppliers.

Test Case #1 - Hypothesized Impact

Simply stated, the hypothesis for this is improvement is: if Synergy Labs utilizes a standardized process for supplier selection and requirement communication, the percentage of non-conforming material identified at incoming inspection will drop 20% from 85% to 65%.

The most significant impact will come from standardizing data package requirements flow down to suppliers. The current process includes requirements given to suppliers via assembly drawings, purchase order requests, online order forms, and even phone conversations during DFM. A clear order of precedence and standardized order is not provided to suppliers, which is the root cause identified for this problem. By standardizing the ordering process to include a clear direction of all required data package contents to suppliers, the percentage of non-conformances identified should lower dramatically. While 25% of non-conformances are solely attributed to data package issues, a 20% reduction is a realistic target for this implementation. Any reduction over 10% would be considered to be extraordinarily successful given the minimal investment cost.

Test Case #1 - Experiment

This process can be implemented by the Procurement Team for all PCB orders. During the ordering process, they would be responsible for cleared communicating the requirements and expectations for delivered material. Quality Assurance Inspectors and Engineers would be able to provide input to clearly define all of the requirements for data packages at incoming inspection. The requirements should be a comprehensive list of criteria that is currently being communicated via assembly drawings, purchase order requests, online order forms, and DFM. These requirements should be communicated to suppliers via a standardized purchase order. This purchase order would serve as the primary source of requirements for suppliers. Any questions or communication between Synergy Labs and suppliers should be routed directly through the Procurement Team to establish a single point of contact.

Furthermore, conditions of the purchase order should clearly state that any omissions in the data package would result in immediate return-to-vendor disposition without any payment for products received. This would be a fundamental change for Synergy Labs given that payment is provided upon ordering, rather than accepted shipments. However, it would provide Synergy Labs with more leverage to ensure data package requirements are consistently met. This process step could be performed at receiving which would reduce the time spent by Quality Assurance Inspectors and Engineers to identify and disposition issues due to data packages.

This test case should be run over the course of six months so that the results can compared to the data collected for the current condition. The process must be implemented for all PCB orders so that the data will verify or disprove the hypothesis of a 20% reduction in non-conformances overall. The process for data collection would utilize the current method for capturing non-conformance data and generating metrics. The percentage of non-conformances caused solely by data package issues can be expected to drop from 25% to 5%. This would effectively lower the overall percentage from 85% to 65%.

Test Case #1 - Results Analysis

A baseline cost can be determined based on the duration of the non-conformance dispositioning from the current condition process identified in Figure 3. While the actual hours spent may vary greatly on a case by case basis, the average duration between non-conformance identification and disposition is 5 business days. Non-conformances are typically processed during an hour long meeting on a daily basis. Representatives for QA Inspectors, QA Engineers, Manufacturing Engineers, and the Design Team are responsible for providing input. Assuming that one member from each functional group attends on a daily basis, the total number of hours spent on a disposition is 20 hours (4 people x 1 hour per day x 5 days).

While the hourly rates for different functional groups can vary, a standard rate of $200 per hour can be assumed as an average hourly labor cost. This results is a total labor cost of $4,000 each time that PCBs are identified as non-conforming current process.

In 2016, Synergy Labs placed over 1,200 orders for PCBs. Given that 25% of incoming orders are found to have data package non-conformances, roughly 300 total orders were found to have some type of data package issue. Processing these 300 non-conformances at an average rate of $5,600 results in a total yearly cost of approximately $1,200,000 for dispositioning.

The target condition from the hypothesis predicts that the percentage of data package non-conformances will be lowered from 25% to 5% as a result of the new process. This would yield an 80%, or $960,000 ***annual*** cost reduction. Lowering the amount of non-conformance by each percentage point results in $12,000 in recovered costs. This astonishing cost savings would be tremendously valuable to Synergy Labs and its customers.

The actual results of this experiment can be utilized to validate the root cause of problem #4 in the current condition. If the revised process resulted in a non-conformance reductions lower than 20%, additional root cause analysis would need to be performed as there would likely be other factors contributing to the problem that were not previously identified.

Test Case #2 – Supplier Capability Matrix

Assuming the data collected over the course of 6 month confirmed the original hypothesis and yielded a 20% reduction in non-conformances, additional process improvements could be initiated utilizing the same scientific method process. The next problem identified in **Error! Reference source not found.** to be addressed would be #2 - suppliers not adequately evaluated based on ability to meet requirements and design criteria. This problem is significantly more complex and difficult to address. The suggested countermeasure of establishing a Supplier Capability Matrix would require more time and resources than the improved procurement process. This would require senior management support and stakeholder buy-in. The suggested process would impact many of the functional groups involved with current process and create additional responsibilities for each group. The ideal process would also include an automated feedback loop from incoming inspection results that would update the Supplier Capability Matrix based on actual results. This would require some modifications to the existing MRP system to enforce specific data entry and analysis. Fortunately the cost savings generated by the new standardized procurement process could as a business case to obtain additional funds for MRP system improvements and customizations.

The initial development of the supplier capability matrix could be based on a supplier survey sent to all of the suppliers utilized during the previous year. The goal of the supplier survey would be baseline their capabilities that could be mapped directly to functional design requirements and features for PCBs. This effort would require collaboration from the Design Team, Manufacturing Engineers, Quality Assurance Inspectors and Engineers. An example of a supplier survey and potential criteria is included in the Appendix.

The responses from the supplier survey could then be mapped into a Supplier Capability Matrix. The Supplier Capability Matrix should include all of the suppliers surveyed, and their corresponding responses for each discrete capability. Figure 10 below is an example of supplier capability mapping. The left hand column identifies the suppliers while the top two rows identify each discrete capability included in the survey.

Process/ Capability		Board Type				Quality Certifications/Standards												Lines/Spaces		Microvias (MV)							
Company	Capability Level (Associated Yield)	Rigid	Rigid-Flex	Flex	RF/MW/mmWave	AS9100 (Expiration Date)	ISO 9001 (Expiration Date)	IPC-6012 (Rigid) (Highest Class Certified To	IPC-6013 (Flex) (Highest Class Certified To	ITAR	MIL-PRF-31032							Min Outer Line/ Space (mils)	Min Inner Line/ Space (mils)	MV Capability ?	MV Drill in House?	Copper Filled MV Capability ?	Copper Filled MV Capability in House?	Min. Laser Drilled MV Diameter (mils)	MV Aspect Ratio (Diameter: Length	Stacked MV Capability ?	# Stacked MVs
											/1	/2	/3	/4	/5	/6										
Draper Requirements Orange = Important Capability Red = Critical Capability	Standard (>85%) Advanced (50-84%) In Development (< 50%)							Class 3	Class 3									2.5 / 2.5 minimum	2.5 / 2.5 minimum	Yes, Standard		Yes, Standard		3	1:1	Yes, Standard	
Supplier #1	Standard	Yes	Yes	Yes	Yes	Active Cert 9/15/18	Active Cert 9/15/18	Class 3A	Class 3	Yes	Yes	Yes	Yes	Yes	No	No		4.0 / 4.0	4.0 / 4.0	Standard	Yes	Standard	Yes	4	0.85:1	Standard	2
	Advanced																	3.0 / 5.0	3.0 / 3.0					---	---		3
	In Development																	3.0 / 3.0	2.5 / 2.5					---	---		---
Supplier #2	Standard	Yes	No	No	No	None	Active Cert 9/14/18	Class 3A	N/A	Yes	No	No	No	No	No	No		3.0 / 3.0	3.0 / 3.0	Standard	Yes	Standard	Yes	5	0.5:1	Standard	3
	Advanced																	2.0 / 2.0	2.0 / 2.0					4	0.9:1		4
	In Development																	< 2.0 / 2.0	< 2.0 / 2.0					3	> 1:1		5+
Supplier #3	Standard																										
	Advanced																										
	In Development																										
Supplier #4	Standard	Yes	Yes	Yes	Yes	Active Cert 9/14/18	Active Cert 9/14/18	Class 3A	Class 3A	Yes	Yes	No	Yes	No	Yes	Yes		3.5 / 3.5	3.0 / 3.0	Standard	Yes	Standard	Yes	5	1.5:1	Advanced	0
	Advanced																	2.5 / 2.5	2.5 / 2.5					4	1.25:1		3
	In Development																	2.0 / 2.0	2.0 / 2.0					3	01:01		4
Supplier #5	Standard																										
	Advanced																										
	In Development																										
Supplier #6	Standard	Yes	No	Yes	Yes	Active Cert 9/15/18	Active Cert 9/15/18	Class 3A	Class 3A	Yes	Yes	Yes	No	No	No	No		3.0 / 3.0	3.0 / 3.0	Standard	Yes	Standard	Yes	4	1:01	Standard	2
	Advanced																	2.0 / 2.0	2.0 / 2.0					4	01:01.5		4
	In Development																	< 2.0 / 2.0	< 2.0 / 2.0					2	---		As required
Supplier #7	Standard																										
	Advanced																										
	In Development																										

Figure 10 - Supplier Capability Matrix Example

The MRP system development effort would require the most investment in terms of time and money. The Inspection Reports that are completed by Quality Assurance Inspectors would need to be customized such that input would be mapped directly to supplier capabilities. Similar customizations would also need to be added to the DMR and CAR processing screens to enable automated Supplier Capability Matrix updates based on actual performances. However, the funding required for such efforts would only be a small fraction of the cost savings from implementing the standardized procurement process.

The Supplier Capability Matrix could then be utilized for supplier selection during the DFM process step in the current condition. Manufacturing Engineers and the Design Team would responsible for clearly identifying which capabilities are required in order to manufacture the newly designed PCB. The Supplier Capability Matrix could then be filtered based on capability requirements to generate a list of potential suppliers. Other considerations such as cost and schedule could be the basis for supplier selection if filtering yielded more than a single supplier.

Test Case #2 – Hypothesized Impact

The hypothesis for this process implementation can be stated as: if an effective Supplier Capability Matrix is utilized for supplier selection, the percentage of non-conforming material identified at incoming inspection will drop and additional 20%, from 65% to 45%.

The goal of a 20% reduction is relatively conservative given that the current process for vendor selection is purely anecdotal in the current condition. Detailed capability mapping and an enhanced supplier selection process could result in a significant reduction in non-conforming PCBs. However, any level over 20% would be considered as extremely effective. The known cost savings of a 20% reduction would result in an additional $960,000 in recovered costs.

Test Case #2 – Experiment

This process can be implemented for the programs that account for 80% of Synergy Labs annual volume of PCB orders. 80% of the PCB volume comes from 15 suppliers, which is a manageable amount of suppliers to be survey and evaluated based on capability. The test case should run for another 6 month duration to ensure that a similar sample size of data can be compared against the original baselined data. During the DFM process, Manufacturing Engineers would be responsible for completing the Supplier Capability Matrix filtering for supplier selection. The programs would be required to make their decision on suppliers using this process as a first pass. Other factors like cost and schedule can only considered after the filtering process. Any programs that selected a supplier without using the Supplier Capability Matrix would be omitted from the data.

Despite the process being implemented for a subset of all PCB orders, the results would verify or disprove the hypothesis of a 20% reduction in non-conformances overall. The process for data collection would utilize the current method for capturing non-conformance data and would be represented in terms of PCBs non-conformances per opportunities.

Test Case #2 – Results Analysis

The results of this test could provide a justification for surveying and mapping the capabilities of the remaining suppliers. A portion of the cost savings from a 20% reduction in non-conformances could be utilized to fund the additional effort required to map the capabilities of additional suppliers.

The target condition from the hypothesis predicts that the percentage of overall non-conformances will be lowered from 65% to 45% as a result of the new process. This would generate an another $960,000 annual cost reduction. The results of this experiment could then be utilized to validate the root cause of problem #2 in the current condition. If the revised process did not result in a 20% reduction of non-conformances, additional root cause analysis would need to be performed as there would likely be other factors contributing to the problem that were not previously identified.

Chapter 8: Final Conclusion / Discussion

Second Hypothesis Validation

The results generated by the two process improvement test cases could be analyzed and represented in terms of cost savings. The cost savings calculated by these efforts would be fairly conservative since they are not accounting for schedule impacts or customer satisfaction, which is significantly more difficult to quantify. However, if both hypotheses were to be validated, the annual cost savings would exceed $1.8 million dollars. This cost reduction could help justify additional process improvements to establish a Supply Chain Management Team and implement a more robust SCM system. Collectively, Test Case #1 and Test Case #2 could reduce the overall percentage of non-conformance from 85% to 45%. The incorporation of a Supply Chain Management Team and SCM could potentially reduce that figure by another 20%. Thus confirming second hypothesis, which stated that a new process would result in a rate of non-conformance lower than 25% overall.

Applications

This incremental rollout process could be self-funded using the cost savings generated by each successful implementation phase. Problems 1, 3, and 5 from Table II can all be addressed by a new Supply Chain Management Team and an effective SCM system. These countermeasures are by far the most resource intensive, coupled with a significant change in Synergy Labs organizational structure. However, the case for implementing an dramatic change like this could be justified with demonstrated success of the previous efforts.

In a matrixed organization, such as Synergy Labs, each program may not have the funding required to proactively perform supplier quality control efforts. This thesis presents an alternative method for systematically evaluating supplier capability and performance without placing the cost burden on each program to source their suppliers appropriately. This iterative process will continue to generate useful information for supplier selection based on actual performance. In turn, this could narrow the field of potential suppliers and subsequently increase the volume of orders through effective suppliers. This increased volume could lead to other opportunities for cost reduction.

Lessons Learned

The Synergy Labs case study is intended to describe the unique challenges of supply chain management for low-volume, high-variation manufacturers. While the problems, root causes, and suggested counter measures may be tailored towards a specific environment and set of conditions, the process for proposing a hypothesis, constructing a method to test that hypothesis, and analyzing the results can yield tremendous benefits for resigning a problematic system. The methodology described in this thesis provides an example of how to map the current process, identify problems and associated root causes, suggest countermeasures, and implement process improvements utilizing the scientific method. This overall process is a highly structured approach for identifying and addressing problems regardless of the environment or conditions.

The suggestions made in thesis were geared towards a mid-sized electronics manufacturer that develops highly customized products with extraordinarily high quality. However, the use of a Supplier Capability Matrix can utilized by a wide range of companies looking to reduce the risk of receiving unacceptable material from their suppliers. The costs associated with dispositioning non-conforming material can be easily calculated and provide a justification for process improvement efforts. The survey questions and inspection results may be catered towards fundamentally different supplier criteria, but the process can remain constant. A Supplier Capability Matrix could be implemented using a single spreadsheet with minimal investment costs. The use of this tool could provide a foundation for a more effective supplier selection process, particularly at other electronics manufacturers that utilize IPC standards for design considerations.

Appendix

A. Supplier Survey

Supplier Information **Date:**

Supplier			
Address			
Primary Point(s) of Contact			
Name	**Position**	**Email**	**Phone**

Board Type(s)

Type	Check One		Comments
Rigid		Yes	
		No	
Rigid-Flex		Yes	
		No	
Flex		Yes	
		No	

Certifications/Standards

Certifications/Standards	Check One		Comments	
AS9100		Active Cert		Certification Exp. Date
		Expired Cert		
		None		
ISO 9001		Active Cert		Certification Exp. Date
		Expired Cert		
		None		
IPC-6012 Class 3		Yes		
		No		
IPC-6013 Class 3		Yes		
		No		
ITAR		Yes		
		No		
MIL-PRF-31032		Yes		
		No		
Other (Specify)				

Capabilities

Capability	Standard*	Advanced**	In Development***
Lines/Spaces			
Min Outer Line/Space	/	/	/
Min Inner Line/Space	/	/	/
HDI			
Microvia Capability?			
Copper Filled MVs?			
Smallest MV Diameter			
MV Aspect Ratio			
Other			
Thinnest Cu (oz.)			
Thinnest Dielectric (in)			
Thinnest Overall Board Thickness (in)			
PTH Aspect Ratio			
SM tenting?			
Additional Comments			

* Standard = Can achieve with little process fall-out (Yield
** Advanced = Can achieve with some process fall-out
*** In Development = Can achieve, but with high process fall-out

Materials/Finishes

Material/Finish	Check One		In House?		Comment
Deep Ni or Au (Hard)		**Yes**		**In House**	
				Out of House	
		No			
Deep Ni or Au (Soft)		**Yes**		**In House**	
				Out of House	
		No			
ENIG		**Yes**		**In House**	
				Out of House	
		No			
ENEPIG		**Yes**		**In House**	
				Out of House	
		No			
HASL		**Yes**		**In House**	
				Out of House	
		No			

Dry Film Solder-mask		Yes		In House	
				Out of House	
		No			
PTFE / RF		Yes		In House	
				Out of House	
		No			
		Yes		In House	
				Out of House	
		No			
		Yes		In House	
				Out of House	
		No			
Other (Specify)					

Testing/Measurement

Material/Finish	Check One		In House?		Comment
IST Testing?		Yes		In House	
				Out of House	
		No			

B. Supplier Capability Breakdown and IPC Standards

Visual Inspection

IPC-A-600: 46 non-conformances to check for on Rigid, 53 on Flex/Rigid-Flex

Printed Board Edges (IPC-A-600 2.1): 5

Base Material Surface (IPC-A-600 2.2): 4

Base Material Subsurface (IPC-A-600 2.3): 4

Solder Coatings and Fused Tin Lead (IPC-A-600 2.4): 2

Holes – Plated-Through – General (IPC-A-600 2.5): 6

Holes – Unsupported (IPC-A-600 2.6): 1

Printed Contacts (IPC-A-600 2.7): 4

Marking (IPC-A-600 2.8): 2

Solder Mask (IPC-A-600 2.9): 11

Pattern Definition – Dimensional (IPC-A-600 2.10): 6

Flatness (IPC-A-600 2.11): 1

Flexible and Rigid-Flex Printed Boards (IPC-A-600 4.1): 7

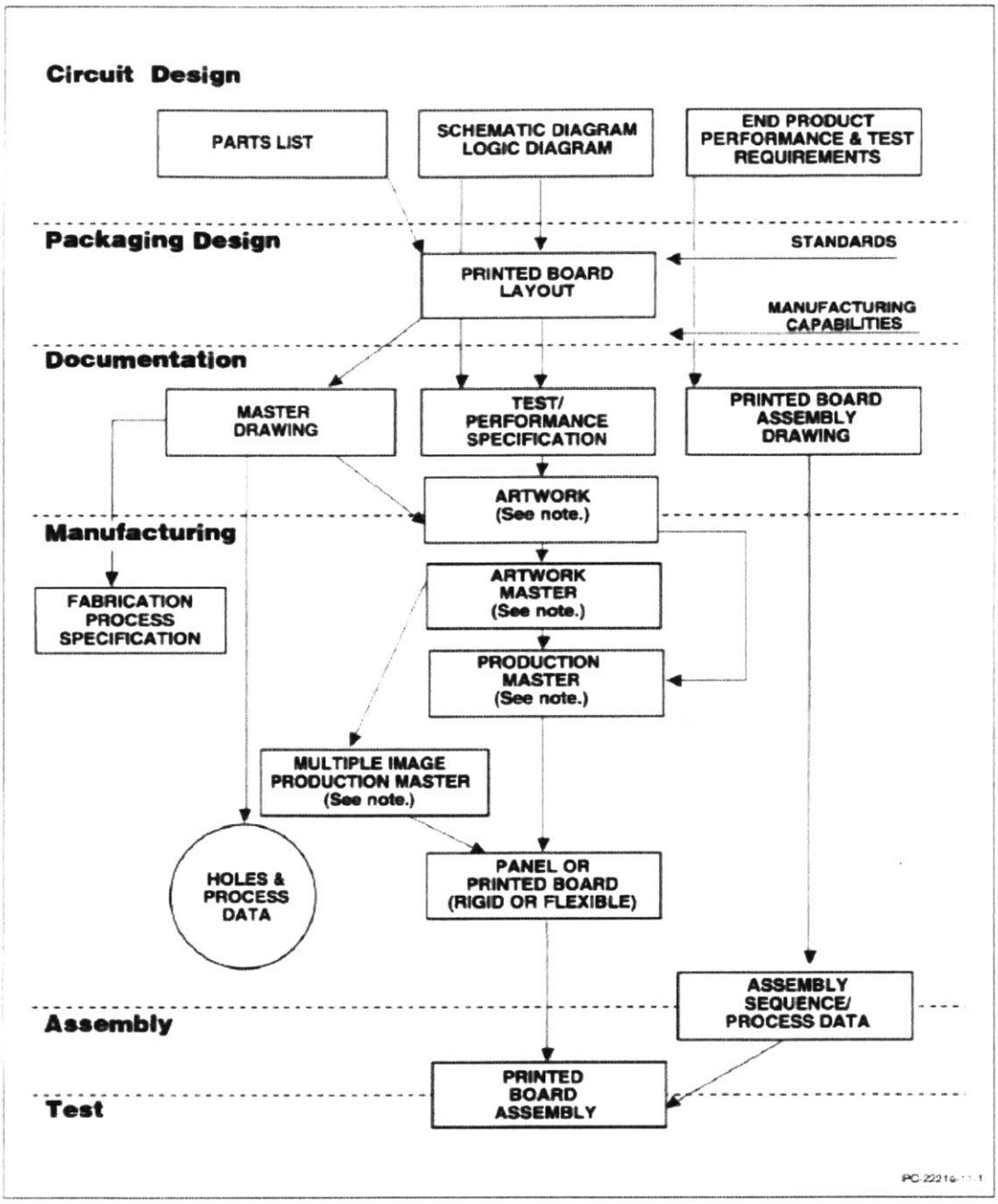
Circuit Design
PARTS LIST
SCHEMATIC DIAGRAM LOGIC DIAGRAM
END PRODUCT PERFORMANCE & TEST REQUIREMENTS
Packaging Design
STANDARDS
PRINTED BOARD LAYOUT
MANUFACTURING CAPABILITIES
Documentation
MASTER DRAWING
TEST/ PERFORMANCE SPECIFICATION
PRINTED BOARD ASSEMBLY DRAWING
ARTWORK (See note.)
Manufacturing
FABRICATION PROCESS SPECIFICATION
ARTWORK MASTER (See note.)
PRODUCTION MASTER (See note.)
MULTIPLE IMAGE PRODUCTION MASTER (See note.)
HOLES & PROCESS DATA
PANEL OR PRINTED BOARD (RIGID OR FLEXIBLE)
ASSEMBLY SEQUENCE/ PROCESS DATA
Assembly
PRINTED BOARD ASSEMBLY
Test

Table 3-1 PCB Design/Performance Tradeoff Checklist

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Dielectric Thickness to Ground	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
Line Spacing	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk		X	X	
	MP	Physical Size/Weight	X			X
	M/Y	Electrical Isolation	X		X	
Coupled Line Length	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
Line Width	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance		X	Design Driven	
	MP	Physical Size/Weight	X		Design Driven	
	R	Signal Conductor Integrity	X		X	
	M/Y	Electrical Continuity	X		X	
Line Thickness	EP	Lateral Crosstalk	X			X
	R	Signal Conductor Integrity	X		X	
Vertical Line Spacing	EP	Vertical Crosstalk		X	X	
Z_o of PCB vs. Z_o of Device	EP	Reflections		X	X	
Distance between Via Walls	R	Electrical Isolation	X		X	
Annular Ring (capture and target land to via)	M/Y	Productivity	X		X	
Signal Layer Quantity	MP	Physical Size/Weight	X			X
	M/Y	Layer-to-Layer Registration		X		X

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Component I/O Pitch Board Thickness	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	M/Y	Via Plating Thickness		X		X
Copper Plating Thickness	R	Via Integrity	X		X	
Aspect Ratio	R	Via Integrity		X		X
	M/Y	Producibility		X		X
Overplate (Nickel -Kevlar only)	R	Via Integrity	X		X	
Via Diameter	M/Y	Via Plating Thickness	X		X	
	R	Via Integrity	X		X	
Laminate Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability	X		X	
Prepreg Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	EP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
Dielectric Constant	EP	Reflections	X			X
	EP	Characteristic Impedance		X	Design Driven	
	EP	Signal Speed		X	Design Driven	
CTE (out-of-plane)	R	Via Integrity		X		X
CTE (in-plane)	R	Solder Joint Integrity		X		X
	R	Signal Conductor Integrity		X		X
Resin T_g	R	Via Integrity	X		X	
	R	PTH Solder Joint Integrity	X		X	
Copper Ductility	R	Via Integrity	X		X	
	R	Signal Conductor Integrity	X		X	
Copper Peel Strength	R	Component Land Adhesion to Dielectric	X		X	
Dimensional Stability	M/Y	Layer-to-Layer Registration	X		X	
Resin Flow	M/Y	PWB Resin Voids		X	X	
Rigidity	MP	Flexural Modulus	X		Design Driven	
Volatile Content	M/Y	PWB Resin Voids	X			X

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Component I/O Pitch	MP	Physical Size/Weight	X			X
Board Thickness	R	Via Integrity		X		X
	M/Y	Via Plating Thickness		X		X
Copper Plating Thickness	R	Via Integrity	X		X	
Aspect Ratio	R	Via Integrity		X		X
	M/Y	Producibility		X		X
Overplate (Nickel -Kevlar only)	R	Via Integrity	X		X	
Via Diameter	M/Y	Via Plating Thickness	X		X	
	R	Via Integrity	X		X	
Laminate Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability	X		X	
Prepreg Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	EP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
Dielectric Constant	EP	Reflections	X			X
	EP	Characteristic Impedance		X	Design Driven	
	EP	Signal Speed		X	Design Driven	
CTE (out-of-plane)	R	Via Integrity		X		X
CTE (in-plane)	R	Solder Joint Integrity		X		X
	R	Signal Conductor Integrity		X		X
Resin T_g	R	Via Integrity	X		X	
	R	PTH Solder Joint Integrity	X		X	
Copper Ductility	R	Via Integrity	X		X	
	R	Signal Conductor Integrity	X		X	
Copper Peel Strength	R	Component Land Adhesion to Dielectric	X		X	
Dimensional Stability	M/Y	Layer-to-Layer Registration	X		X	
Resin Flow	M/Y	PWB Resin Voids		X	X	
Rigidity	MP	Flexural Modulus	X		Design Driven	
Volatile Content	M/Y	PWB Resin Voids	X			X

Table 4-3 Final Finish, Surface Plating Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	Electrodeposited Tin-Lead (fused) (min)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
TLU	Electrodeposited Tin-Lead Unfused (min)	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold (min) for edge-board connectors and areas not to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold (max) on areas to be soldered	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) (min)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) (min)	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
N	Nickel - Electroplate for Edge Board Connectors (min)	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier to Copper-Tin Diffusion[1] (min)	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	Organic Solderability Preservative	Solderable	Solderable	Solderable
ENIG	Electroless Nickel	3 µm [118 µin] (min)	3 µm [118 µin] (min)	3 µm [118 µin] (min)
	Immersion Gold	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)
IS	Immersion Silver	Solderable	Solderable	Solderable
IT	Immersion Tin	Solderable	Solderable	Solderable
C	Bare Copper	As indicated in Table 10-1 and/or Table 10-2		
	Surface and Holes			
	Copper[2] (min.avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin areas[3]	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Blind Vias			
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Low Aspect Ratio Blind Vias[4]			
	Copper (min. avg.)	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Min. thin area	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Buried Via Cores			
	Copper (min. avg.)	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	Min. thin area	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
	Buried Vias (> 2 layers)			
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]

Table 4-3 Final Finish, Surface Plating Coating Thickness Requirements

Code	Finish	Class 1	Class 2	Class 3
S	Solder Coating over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	Electrodeposited Tin-Lead (fused) (min)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
TLU	Electrodeposited Tin-Lead Unfused (min)	8.0 µm [315 µin]	8.0 µm [315 µin]	8.0 µm [315 µin]
G	Gold (min) for edge-board connectors and areas not to be soldered	0.8 µm [31.5 µin]	0.8 µm [31.5 µin]	1.25 µm [49.21 µin]
GS	Gold (max) on areas to be soldered	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]	0.45 µm [17.72 µin]
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) (min)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) (min)	0.3 µm [11.8 µin]	0.3 µm [11.8 µin]	0.8 µm [31.5 µin]
N	Nickel - Electroplate for Edge Board Connectors (min)	2.0 µm [78.7 µin]	2.5 µm [98.4 µin]	2.5 µm [98.4 µin]
NB	Nickel - Electroplate as a barrier to Copper-Tin Diffusion[1] (min)	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]	1.3 µm [51.2 µin]
OSP	Organic Solderability Preservative	Solderable	Solderable	Solderable
ENIG	Electroless Nickel	3 µm [118 µin] (min)	3 µm [118 µin] (min)	3 µm [118 µin] (min)
	Immersion Gold	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)
IS	Immersion Silver	Solderable	Solderable	Solderable
IT	Immersion Tin	Solderable	Solderable	Solderable
C	Bare Copper	As indicated in Table 10-1 and/or Table 10-2		
	Surface and Holes			
	Copper[2] (min.avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin areas[3]	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Blind Vias			
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Low Aspect Ratio Blind Vias[4]			
	Copper (min. avg.)	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Min. thin area	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Buried Via Cores			
	Copper (min. avg.)	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
	Min. thin area	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
	Buried Vias (> 2 layers)			
	Copper (min. avg.)	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Min. thin area	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]

Table 9-3 Minimum Drilled Hole Size for Buried Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.25 mm [<0.00984 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.15 mm [0.00591 in]
0.25 - 0.5 mm [0.020 in]	0.15 mm [0.00591 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]
0.5 mm [0.020 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.25 mm [0.00984 in]

Table 9-4 Minimum Drilled Hole Size for Blind Vias

Layer Thickness	Class 1	Class 2	Class 3
<0.10 mm [<0.00393 in]	0.10 mm [0.00393 in]	0.10 mm [0.00393 in]	0.2 mm [0.0079 in]
0.10 - 0.25 mm [0.00984 in]	0.15 mm [0.00591 in]	0.20 mm [0.00787 in]	0.3 mm [0.012 in]
0.25 mm [0.00984 in]	0.20 mm [0.00787 in]	0.30 mm [0.0118 in]	0.4 mm [0.016 in]

Table 10-2 External Conductor Thickness After Plating

Weight, oz. [µm]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin]	Plus minimum plating for Class 1 and 2 (20 µm)	Plus minimum plating for Class 3 (25 µm)	Maximum Variable Processing Allowance Reduction*	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz. [5.10]	4.60 [181]	24.60	29.60	1.50	23.1 [909]	28.1 [1,106]
1/4 oz. [8.50]	7.70 [303]	27.70	32.70	1.50	26.2 [1,031]	31.2 [1,228]
3/8 oz. [12.00]	10.80 [425]	30.80	35.80	1.50	29.3 [1,154]	34.3 [1,350]
1/2 oz. [17.10]	15.40 [606]	35.40	40.40	2.00	33.4 [1,315]	38.4 [1,512]
1 oz. [34.30]	30.90 [1,217]	50.90	55.90	3.00	47.9 [1,886]	52.9 [2,083]
2 oz. [68.60]	61.70 [2,429]	81.70	86.70	3.00	78.7 [3,098]	83.7 [3,295]
3 oz. [102.90]	92.60 [3,646]	112.60	117.60	3.00	109.6 [4,315]	114.6 [4,512]
4 oz. [137.20]	123.50 [4,862]	143.50	148.50	4.00	139.5 [5,492]	144.5 [5,689]

Table 12-1 Coupon Frequency Requirements

Coupon Purpose	I.D.[2]	Class 1	Class 2	Class 3
Conformance Testing				
Rework Simulation	A/B or A	Not required	Twice per panel	Twice per panel, opposite corners
Thermal Stress, Plating Thickness, and Bond Strength Type 1	A/B or A or B	Twice per panel, opposite corners	Twice per panel, opposite corners	Twice per panel, opposite corners
Thermal Stress, Inner Layer Interconnect Integrity	A or A/B	Not required	As agreed upon between user and supplier	Required
Hole Solderability	S[3]	Optional	Preferred, 1 per panel	Preferred, 1 per panel
Hole Solderability	A/B or A	Not Required	Optional	Optional
Solder Resist Tenting (if used)	T	Not required	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Peel Strength	C	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel location optional, pattern defined by artwork
Solder Resist (if used)	G	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional	Once per panel with solder resist, location optional
Surface Mount Solderability (Optional for SMT)	M	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Reliability Assurance Inspection				
Peel Strength, Surface Mount Bond Strength (Optional for SMT)	N	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Surface Insulation Resistance	H	Once per panel, location optional	Twice per panel, opposite corners	Twice per panel, opposite corners
Moisture and Insulation Resistance	E	Once per panel, location optional	Twice per panel, opposite corners	Twice per panel, opposite corners
Optional or Process Control				
Registration (Option 1 or 2)	F	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Registration (Optional)	R	Not required	Four per panel, opposite sides defined by artwork	Four per panel, opposite sides defined by artwork
Interconnect Resistance (Option 1 or 2)	D	Not required	Once per panel, location optional, pattern defined by artwork	Once per panel, location optional, pattern defined by artwork
Bending Flexibility, Flexible Endurance	X	Optional, pattern defined by artwork	Optional, pattern defined by artwork	Optional, pattern defined by artwork

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