A Manufacturing Methodology for Carbon Nanotube-based Digital Systems: from Devices, to Doping, to System Demonstrations

By

Christian Lee Lau

B.A., The University of Southern California (2017)

S.M., Massachusetts Institute of Technology (2020)

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Author……………………………………………………………...
Department of Electrical Engineering and Computer Science
January 26, 2022

Certified by…………………………………………..……………
Max M. Shulaker
Associate Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by………………………………………………...…...
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

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Abstract

Electronics is approaching a major paradigm shift because silicon transistor scaling no longer yields historical energy-efficiency benefits, spurring research towards beyond-silicon nanotechnologies. In particular, carbon nanotube field-effect transistor (CNFET)-based digital circuits promise substantial energy-efficiency benefits, but the inability to perfectly control intrinsic nanoscale defects and variability in carbon nanotubes has precluded the realization of very-large-scale integrated systems. In this thesis, I overcome these defects and variations to enable, for the first time, a demonstration of a beyond-silicon modern microprocessor: RV16X-NANO, designed and fabricated entirely using CNFETs. RV16X-NANO is a 16-bit microprocessor based on the open-source and commercially available RISC-V instruction set processor, running standard RISC-V 32-bit instructions on 16-bit data and addresses. It integrates >14,000 CMOS CNFETs, and operates as modern microprocessors do today (for example, it can run compiled programs; in addition, we demonstrate its functionality by executing all types and formats of instructions in the RISC-V instruction-set architecture). This is made possible by the manufacturing methodology for CNTs (MMC)—a set of original processing and circuit design techniques that are combined to overcome the intrinsic CNT challenges.

Importantly, the entire MMC and all of the work in this thesis are wafer-scale, VLSI-compatible and is seamlessly integrated within existing infrastructures for silicon CMOS—both in terms of design and of processing. Together, the contributions of this thesis establish a robust CNT CMOS technology and represent a major milestone in the development of beyond-silicon electronics.

Thesis Supervisor: Max M. Shulaker

Title: Associate Professor of Electrical Engineering and Computer Science

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Beyond my colleagues and mentors at MIT, I want to thank my undergraduate advisor Professor Chongwu Zhou at the University of Southern California. He was the only professor to hire me as a first semester Freshman—at a time when I had thought MOSFETs to be quaint characters from the original Star Wars trilogy, rather the essential components comprising most digital systems today. By hiring me, Prof. Zhou jumpstarted my career in carbon nanotube electronics, which has culminated so far in this thesis.

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Chapter 1: Introduction

1.1 Background

As physical and equivalent scaling of silicon field-effect transistors (FETs)[1] yield diminishing returns, alternative beyond-silicon technologies are being investigated. Carbon nanotubes (CNTs, nanoscale cylinders made of a single sheet of carbon atoms with diameters of approximately 10–20 Å) are prominent among a variety of nanotechnologies that are being considered for next-generation energy-efficient electronic systems[2,3,4]. Owing to the nanoscale dimensions and simultaneously high carrier transport of CNTs[5,6], digital systems built from FETs fabricated with CNTs as the transistor channel (that is, CNFETs) are projected to improve the energy efficiency of today's silicon-based technologies by an order of magnitude[3,13,14,15,7,8]. A schematic of a CNFET is shown in Figure 1.1. Additionally, CNFETs enable new opportunities for additional energy efficiency benefits (*e.g.*, for new system architectures such as monolithic three-dimensional integrated systems.)

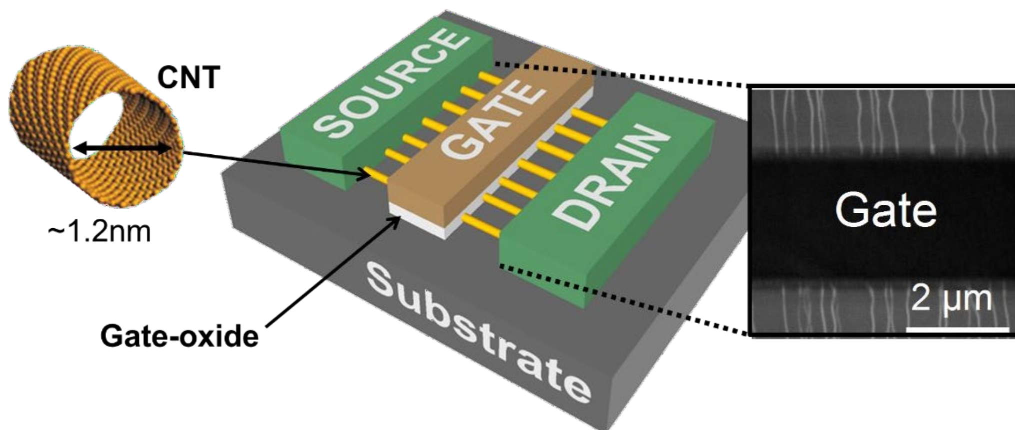


Figure 1.1. Schematic of a carbon nanotube field effect transistor (CNFET) with semiconducting CNTs bridging the channel.

Over the last decade, significant progress with CNT technology has transformed them from a scientifically-interesting material to a potential supplement to silicon CMOS for next-generation high performance digital systems: high performance PMOS CNFETs competitive with silicon FETs, [5,46–49] controlled CNT

placement,[5,50,51] and complete digital systems (the largest demonstration comprising of 178 PMOS CNFETs) [2,14,43,52] have all been experimentally demonstrated.

Despite this progress, a major remaining obstacle facing CNFETs is the ability to dope CNTs to realize CNFET CMOS circuits (integrating PMOS and NMOS CNFETs). Specifically, it remains a challenge to dope CNTs to reliably form NMOS CNFETs. Moreover, as with all emerging nanotechnologies, there remained a substantial disconnect between these small-scale demonstrations and modern systems comprising tens of thousands of FETs (for example, microprocessors) to billions of FETs (for example, high-performance computing servers). Perpetuating this divide is the inability to achieve perfect atomic-level control of nanomaterials at macroscopic scales (for example, yielding CNTs of consistent 10-Å diameter uniformly across industry-standard wafer substrates of diameter 150–300 mm). The resulting intrinsic defects and variations have made the realization of such modern systems infeasible. Finally, comprehensive reliability tests (*i.e.,* measuring the long-term degradation and any recovery of the device's transfer characteristics after elevated temperature and electrical stress conditions) are required to advance CNFETs beyond proof-of-concept demonstrations to become a commercially-viable CMOS technology.

In this thesis, we address the key challenges that have precluded the realization of very-large-scale integrated CMOS CNFET systems. As a demonstration, we experimentally realize the first beyond-silicon modern microprocessor: RV16X-NANO, designed and fabricated entirely using CNFETs. To experimentally realize the RV16X-NANO processor, this work shows the following: (1) an electrostatic CNT *n*-type doping technique that satisfies all of the requirements for a CNFET CMOS technology (*i.e*. a CNT doping technique that is tunable, silicon CMOS compatible, air stable, uniform, and robust), (2) a comprehensive manufacturing methodology for CNTs (MMC)—a set of original processing and circuit design techniques that are combined to overcome the intrinsic CNT challenges of variability, manufacturing defects, and material defects, and (3) the first reliability stress-testing of electrostatically doped CNFETs in a commercial semiconductor fabrication and testing facility, demonstrating that their reliability can be comparable to that of commercial silicon FETs. By leveraging these combined processing and design

techniques to realize the first beyond-silicon modern microprocessor, this thesis experimentally validates a promising path towards realizing practical next-generation beyond-silicon electronic systems.

1.2 Outline

Chapter 2 presents an electrostatic doping technique that leverages atomic-layer deposition (ALD) to encapsulate CNTs with nonstoichiometric oxides. We show that ALD allows for precise control of oxide stoichiometry, which translates to direct control of the amount of CNT doping. This tunable electrostatic doping technique is then combined with low work function contact engineering to achieve CNFET CMOS with symmetric NMOS and PMOS transfer characteristics.

Chapter 3 details a comprehensive manufacturing methodology for CNTs—a set of original processing and circuit design techniques that are combined to overcome the intrinsic CNT challenges that have precluded the realization of very large-scale CMOS CNFET systems. As a demonstration of the feasibility of this manufacturing methodology, we experimentally show RV16X-NANO, the first modern microprocessor built from complementary carbon nanotube transistors.

Chapter 4 demonstrates that electrostatic doping can meet all of these requirements for a reliable CMOS technology. We perform the first ever reliability characterization of CNFETs in a commercial semiconductor fabrication and testing facility, following the same standard reliability testing protocols used for evaluating commercial silicon MOSFETs

Chapter 5 concludes this thesis by summarizing key results and discussing the broader impact of this work.

Chapter 2: Tunable n-Type Doping of Carbon Nanotubes through Engineered Atomic Layer Deposition HfO_X Films

2.1 Background

Over the last decade, significant progress with CNT technology has transformed them from a scientifically-interesting material to a potential supplement to silicon CMOS for next-generation high performance digital systems: high performance PMOS CNFETs competitive with silicon FETs,[5,46–49] controlled CNT placement,[5,50,51] and complete digital systems (fabricated entirely with PMOS CNFETs)[2,14,43,52] have all been experimentally demonstrated. Despite this progress, a major remaining obstacle facing CNFETs is the ability to dope CNTs to realize CNFET CMOS circuits (integrating PMOS and NMOS CNFETs). Specifically, it remains a challenge to dope CNTs to reliably form NMOS CNFETs. While a range of previous efforts have fabricated NMOS CNFETs, no prior work satisfies allof the following requirements for a CNFET CMOS technology:

(1) tunable doping: simply realizing NMOS and PMOS CNFETs is insufficient; digital systems require a range of doping values to precisely set device parameters, such as threshold voltage (V_T),

(2) silicon CMOS compatible: solid-state and silicon CMOS compatible materials are required for ease of integration in current commercial fabrication facilities,

(3) air stable: the process should be air stable (both during and post-processing), to avoid changing device performance and/or increased variability,

(4) uniform and robust: to yield digital VLSI systems, potentially comprising billions of CNFETs, any doping must be highly reproducible and uniform across devices on the same sample and devices across multiple samples.

For instance, many existing techniques for realizing NMOS CNFETs rely on low work function metal source/drain contacts (such as Scandium, Erbium, Lanthanum, or Calcium).[53,54,66] These materials are extremely air-reactive, are not silicon CMOS compatible, and due to their reactivity, are also not uniform or robust (*e.g.*, they either significantly increase device variability compared to PMOS CNFET variability,[66] or do not always successfully realize NMOS CNFETs). Alternative doping strategies leveraging reactive molecular dopants[24,25,55] similarly rely on materials not used in conventional silico CMOS processing and contain contaminants (*e.g.*, ionic salts) that are prohibited from commercial fabrication facilities, are often not air stable, and are not solid-state. NMOS CNFETs have also been realized by encapsulating CNTs with dielectrics,[26,59–61] but such methods have not simultaneously demonstrated both tunable and robust n-type doping.[†]

Here we demonstrate an electrostatic CNT doping technique that meets all of the requirements for realizing a CNFET CMOS technology (Figure 2.1). Specifically, this work demonstrates that precise engineering of the stoichiometry of dielectrics (referred to as the “nonstoichiometric doping oxide” NDO, in this instance HfO_X) deposited over exposed CNTs in the channel of CNFETs results in tunable and robust CNT doping. To accomplish this, we experimentally show that atomic layer deposition (ALD) allows for precise engineering of the stoichiometry of the NDO (*e.g.*, modifying the Hf contentat the HfO_X-CNT interface), which in turn results in fine-grained control over the amount of n-type doping, the relative strengths of the p-type and n-type conduction, and the threshold voltage. We also present a model that directly relates the stoichiometry of the HfO_X NDO to an effective Schottky barrier height (Φ_{SB}^*), enabling designers to engineer a given NDO stoichiometry to achieve a precise quantity of CNT doping.

[†] For instance, references [59] and [60] rely on 20 Å electron-beam evaporated Aluminum or 50 Å of Yttriumover the CNTs which is then allowed to oxidize in ambient; this lacks the control and uniformity afforded by atomic layer deposition (ALD).

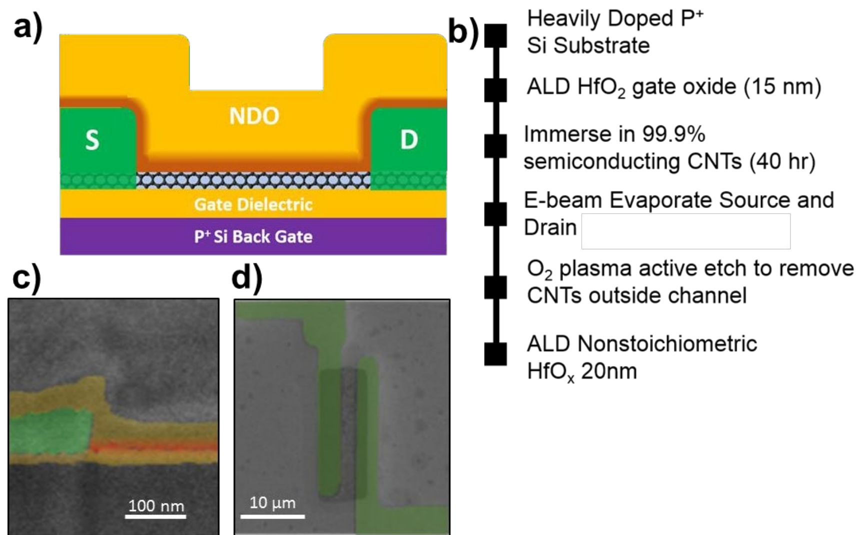


Figure 2.1. CNFET structure. (a) Schematic of NMOS CNFET encapsulated by nonstoichiometric doping oxide (NDO). The region shaded in red underneath the NDO represents the hafnium-rich oxide at the CNT−NDO interface. (b) Process flow for CNFETs. (c) Cross-sectional and (d) top-view scanning electron microscopy (SEM) images of a fabricated global back-gate CNFET encapsulated in NDO.

Moreover, we experimentally demonstrate the following key attributes: (1) our technique can be combined with other doping schemes. As an illustration, we combine NDO electrostatic doping with low work function contact engineering to achieve CNFET CMOS with NMOS and PMOS that achieve similar ON-current, OFF-current, and threshold voltage magnitudes (referred to as "symmetric" NMOS and PMOS CNFETs). Due to the combined doping strategy, the contact metal does not need to have extremely low work function (<4 eV, such as Scandium), but rather can have a work function >4 eV, such as Titanium (a silicon CMOS compatible metal) while still realizing symmetric NMOS and PMOS. (2) The NDO electrostatic doping does not degrade performance (*e.g.*, V_T variations, inverse subthreshold-slope, I_{ON}/I_{OFF}, and gate leakage are statistically similar to PMOS CNFETs); and (3) we demonstrate CNFET static CMOS digital logic gates with rail-to-rail swing (>99% of supply voltage) and high gain[‡] (>15). Thus, this work provides a path for integrating CNFET CMOS within standard fabrication processes today by realizing a solid-state, air-stable, VLSI and silicon-CMOS compatible doping strategy.

[‡] Gain is defined as the maximum absolute value of change in the output voltage with respect to the input voltage (ΔVOUT/ΔVIN)

2.2 Doping Technique: ALD-Engineered NDO

Figure 2.1 (a-d) shows the schematic, fabrication flow, and scanning electron microscope (SEM) images of a typical CNFET. Multiple CNTs comprise the channel with lithographically defined source, drain, and gate contacts. The gate metal and high-*k* gate dielectric (different oxide from the NDO, whichis physically located on the other side of the channel compared to the high-*k* gate dielectric) is fabricated beneath the CNT channel, forming a back-gate device structure. Following the initial CNFET fabrication, an ALD-deposited HfO_X is deposited over the CNTs (*i.e.*, the NDO). The HfO_X dopes the CNT through electrochemical reduction (redox) of the CNTs in contact with Hafnium,[60] as well as through field-effect doping owing to the fixed charges in the HfO_X.[26,61] By controlling the stoichiometryof the first atomic layers of the NDO, as well as the stoichiometry of the bulk NDO, we can precisely control both the amount of redox reaction at the HfO_X-CNT interface and the fixed charge, respectively.

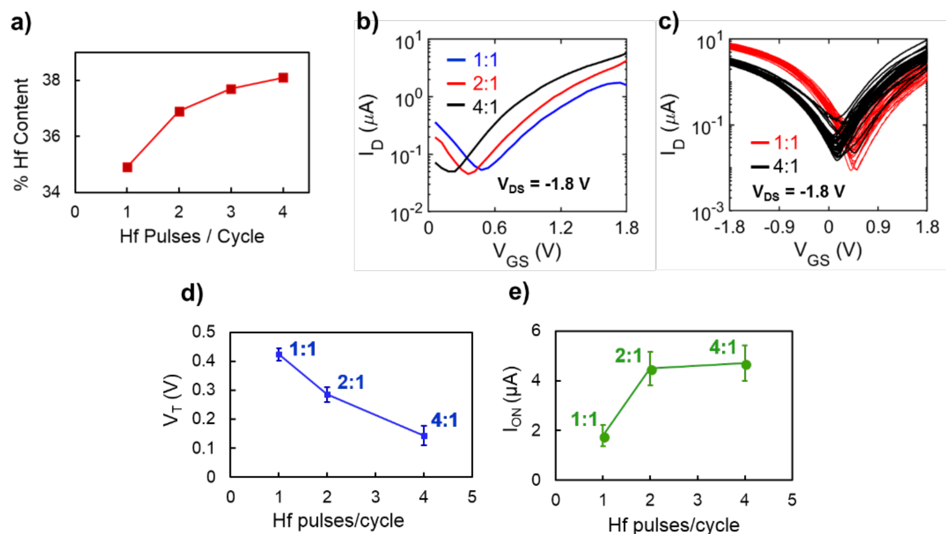


Figure 2.2. Controlling HfO_X stoichiometry for tunable doping. (a) Hf content with increasing Hf precursor/H_2O pulse ratio. (b) I_D−V_{GS} characteristics for CNFETs doped with Hf precursor/H_2O ratios of 1:1, 2:1, and 4:1 (measured with VDS = −1.8 V). (c) Comparison of two sets of 35 CNFETs doped with 4:1 and 1:1 Hf/H_2O ratios. (d) Corresponding average V_T shift and (e) average n-branch ON- current (I_{ON}) for each type of NMOS CNFET with error bars indicating 99% confidence interval (sample size: 105 CNFETs). ON-current is extracted as the drain current at $|V_{GS}| = |V_{DS}| = |V_{DD}|$.

ALD is key for engineering the stoichiometry of each atomic layer within the NDO. ALD HfO_X is deposited by alternating pulses of the precursor (Tetrakis(dimethylamido) hafnium(IV)) and H_2O into a process

chamber. The duration of the pulses, time between pulses, as well as the ratio of the Hf precursor:H_2O pulses change the amount and time the wafer is exposed to the Hf precursor,[30] resulting in fine-grained control over the HfO_X stoichiometry. Moreover, ALD is an industry-standard capability, and HfO_X dielectrics are already used in front-end-of-line silicon CMOS fabrication. To demonstrate the ability to fine-tune the stoichiometry of the NDO, we vary the pulse ratio of Hf:H_2O during the HfO_X deposition. As shown in Figure 2.2 (a), as the pulse ratio of Hf:H_2O increases from 1:1, 2:1, 3:1,and 4:1, the bulk Hf concentration increases from 34.9% to 36.9% to 37.7% to 38.1% (measured by x-ray photoelectron spectroscopy, XPS). Importantly, the ability to vary NDO stoichiometry results in the ability to fine-tune CNT doping (resulting in varying relative strengths of the p-type and n-type branches in CNFET current-voltage characteristics, as well as control of the threshold voltage). We deposit each of the different NDO stoichiometries over back-gated CNFETs. Figure 2.2 (b-e) illustrates how the slight increase in Hf concentration results in increasingly strong n-type doping of CNTs. As the Hf concentration increases, the strength of the n-type conduction branch increases, as evident by increasing drive current (average drive current (I_{ON}) of 1.8 µA, 4.5 µA, and 4.7 µA respectively), as well as a reduction in the p-type conduction branch which manifests as an increasingly negative shift in the V_T (average V_T of 0.40 V, 0.22 V, and 0.12 V respectively). Moreover, this doping scheme is robust due to the high reproducibility and tight process control afforded by ALD: Appendix A1 Figure A1.1.1 shows how two different wafers with the same NDO result in statistically similar doping (average V_T for the two wafers are 0.32 V and 0.35 V).

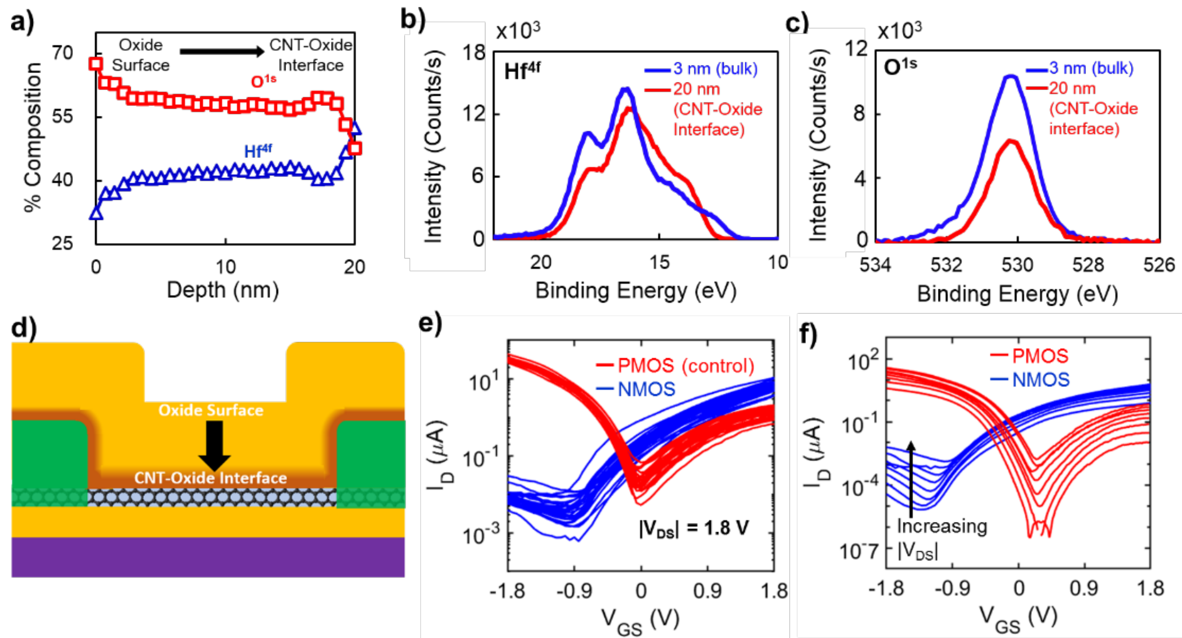


Figure 2.3. Material and electrical characterization of CNFETs with engineered Hf-rich HfO_X−CNT interface. (a) XPS depth profile of HfO_X film from surface to HfO_X−CNT interface. To increase Hf concentration in the first atomic layers, the wafer is pretreated with 50 pulses of Hf precursor (no H_2O), followed by 20 nm 3:1 HfO_X deposition. XPS confirms that the first few atomic layers reach >52% Hf, whereas the bulk has ~38% Hf. (b) Hf^{4f} and (c) O^{1s} peaks at 3 nm depth (bulk HfO_2 film) and 20 nm depth (CNT−HfO_2 interface). (d) Schematic of CNFET identifying the NDO oxide surface and CNT−oxide interface. (e) I_D−V_{GS} curves of 35 CNFETs before and after n-type doping with Hf-rich CNT−oxide interface measured at $V_{DS} = -1.8$ V and $V_{DS} = 1.8$ V, respectively. The difference in ON-current between the PMOS and NMOS CNFETs is caused by all of these CNFETs using platinum metal source and drain contacts (see Figure 2.4 for additional details). (f) I_D−V_{GS} curves with V_{DS} swept from −0.2 to −1.8 V in −0.2 V steps for the PMOS and 0.2 to 1.8 V in 0.2 V steps for the NMOS CNFETs.

To drastically increase the amount of n-type doping and realize unipolar NMOS CNFETs, the first several atomic layers (at the HfO_X-CNT interface) can be engineered with significantly higher Hf concentration. This is another key benefit of leveraging ALD, as the stoichiometry of each atomic layer can be independently controlled. The wafer is pre-treated with 50 repeated pulses of Hf precursor (without H_2O pulses), followed by HfO_X deposition. As shown in Figure 2.3 (a-d) XPS confirms that the first few atomic layers at the CNT-Oxide interface reach >52% Hf, while the bulk has ~38% Hf. Electrical characterization

of the back-gate CNFETs encapsulated with this NDO (*e.g.*, 50 repeated pulses of Hf precursor) in Figure 2.3 (e,f) shows strongly unipolar NMOS CNFETs, increasing the n- type conduction branch by ~500× while decreasing the p-type conduction branch by >2,500× compared to the as-fabricated initial PMOS CNFETs (prior to NDO deposition). A key advantage of this doping scheme is that while such a Hf-rich atomic layer is a strong reducer (resulting in the strong n-type doping), it is encapsulated *in-situ* within the low-pressure ALD chamber during the subsequent HfO_X deposition and is thus air-stable. Figure A2.1.2 shows CNFETs measured after 4, 12, and 30 days exposed to air; there is negligible change in the CNFET electrical characteristics. Moreover, Figure A2.1.3 shows this nonstoichiometric oxide does not increase gate leakage.

Having demonstrated how NDO encapsulation enables tunable doping of CNTs, we present a method for quantifying the degree of n-type doping resulting from an NDO-encapsulated CNFET. Quantifyingthe amount of CNT doping is critical for circuit design, as the amount of doping determines key parameters such as V_T. To quantify the amount of CNT doping, we define an effective Schottky barrier height (Φ_{SB}^{*}) between the CNT and the source/drain metal contacts (energy band diagram shown in Appendix A1, Figure A1.2.1 (c)). We use an effective Schottky barrier height as the p-type and n-type conduction in CNFETs is largely determined by the Schottky barrier height at the interface between the CNT and source/ drain metal contacts.[31] In the band diagram drawn in Supplemental Information FigureA1.2.1 (c), Φ_{SB}^{*} is the height of the potential barrier inhibiting electron transport from the source metal to semiconducting CNT channel. Higher values of Φ_{SB}^{*} result in a greater tunneling barrier for conduction electrons, reducing n-branch current. By calibrating our experimental I_D-V_{GS} data to a Schottky barrier transport model,[64] we calibrate each fabricated CNFET to an associated value for Φ_{SB}^{*}, determining a relationship between NDO stoichiometry and the Φ_{SB}^{*}. The Landauer formulation was used to define the transport equations and the Wentzel-Kramer-Brillouin (WKB) approximation (see Supplemental Information, Figure A1.2.1 (a,b)) was used to solve the tunneling probability across the Schottky barrier of height Φ_{SB}^{*}. As shown in Supplemental Information Figure A1.2.1 (d), increasing the Hafnium content in the NDO layer lowers from 0.3 eV to 0.15 eV, thereby bolstering n-type conduction in CNFETs. Therefore, analogous to how the degree of

doping in silicon is quantified by the dopant concentration (interstitial dopants per cm^3), we likewise can quantify (and modulate) the degree of CNFET doping by tuning the NDO stoichiometry (by calculating the corresponding effective Schottky barrier height).

2.3 Symmetric CNFET CMOS Characterization

To achieve NMOS and PMOS CNFETs with similar I_{ON}, I_{OFF}, and V_T, previous works have relied on extremely low work function metals (such as Scandium and Erbium) to reduce the Schottky barrier for electron injection into the CNT channel.[53,54,66] However, as discussed previously, the high reactivity of these materials precludes their integration into a silicon CMOS compatible fabrication process. Unfortunately, prior works attempting to use the lowest work function metals readily available in standard silicon CMOS processing – such as Titanium – report significantly degraded n-type CNFET conduction[65] (as Titanium's work function (4.33 eV) is lower than typical contact metals used for PMOSCNFETs such as Palladium (5.22-5.64 eV), Gold (5.31-5.47 eV), or Platinum (5.12-5.93 eV), but still higher than Scandium (3.5 eV), Erbium (3.0 eV), *etc*.).

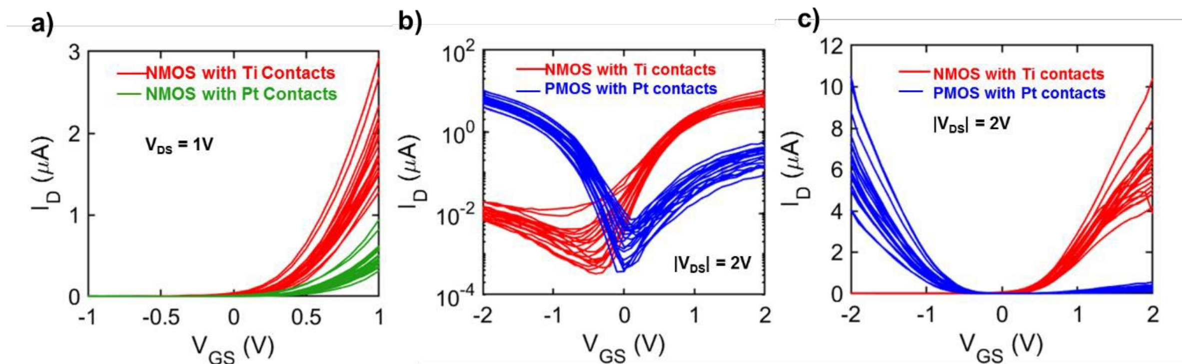


Figure 2.4. Combining NDO encapsulation with low work function contacts to achieve symmetric NMOS/PMOS CNFETs with similar I_{ON}, I_{OFF}, and V_T magnitude. (a) I_D−V_{GS} (linear scale) for NDO-encapsulated NMOS CNFETs with titanium contacts (red) and platinum contacts (green). (b,c) I_D−V_{GS} curves comparing 20 NDO-encapsulated NMOS CNFETs with titanium contacts (red) and 20 PMOS CNFETs with platinum contacts (blue).

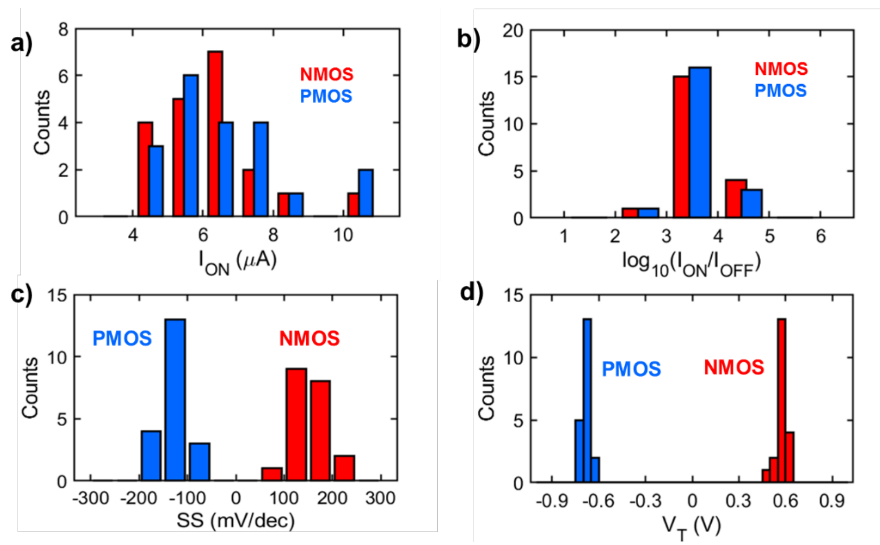


Figure 2.5. Summary statistics for 20 NMOS and 20 PMOS CNFETs measured with $V_{DS} = 2$ V (for NMOS) and $V_{DS} = -2$ V (for PMOS) and VGS swept from 2 to −2 V for both NMOS and PMOS. (a) ON-current distribution for NMOS CNFETs, measured with $V_{DS} = V_{GS} = 2$ V (average, $\mu_{ION,N} = 6.24$ μA; standard deviation, $\sigma_{ION,N} = 1.42$ μA) and PMOS CNFETs, measured with $V_{DS} = V_{GS} = -2$ V (average, $\mu_{ION,P} = 6.60$ μA; standard deviation, $\sigma_{ION,P} = 1.74$ μA). (b) Distribution of $\log_{10}(I_{ON}/I_{OFF})$ for NMOS CNFETs (average, 3.63; standard deviation, 0.42) and PMOS CNFETs (average, 3.58; standard deviation, 0.35). (c) Distribution of maximum subthreshold slope for NMOS (mean, $\mu_n = 153.7$ mV/decade; standard deviation, $\sigma_n = 38.1$ mV/decade) and PMOS (mean, $\mu_P = 125.4$ mV/decade; standard deviation, $\sigma_P = 24.5$ mV/decade) CNFETs. (d) Threshold voltage distribution for NMOS CNFETs (mean, $\mu_{VT,N} = 0.57$ V and $\sigma_{VT,N} = 0.03$ V) and PMOS CNFETs (mean, $\mu_{VT,P} = -0.68$ V; standard deviation, $\sigma_{VT,P} = 0.03$ V). The threshold voltage of each CNFET was calculated using the extrapolation in linear region method, where the I_D−V_{GS} characteristic is linearly extrapolated at its point of highest slope and intersects the gate voltage axis at the threshold voltage.

We show that, when combined with NDO encapsulation, NMOS CNFETs employing Titanium contacts show symmetric performance as PMOS CNFETs fabricated with Platinum contacts (a conventional source and drain metal for PMOS CNFETs[2,13,18,43,49]). Figure 2.4 (a) shows the IV characteristics of a set of NMOS CNFETs with Titanium contacts and a set of NMOS CNFETs with Platinum contacts, all of which have been encapsulated with the same NDO. The NMOS CNFETS with Titanium contacts achieve a 3× improvement in n-type conduction ON-current compared to NMOS CNFETs with Platinum contacts (*e.g.*, the average I_{ON} increases by 3×). This enhanced n-type conduction allows us to fabricate, in a silicon CMOS compatible fashion, PMOS and NMOS CNFETs with symmetric IV characteristics (I_D-V_{GS} curves in Figure 2.4 (b,c)).

Importantly, in contrast to previously reported doping methods, our combined doping technique neither degrades key device characteristics nor introduces significant device variability. Figure 2.5 shows distributions for a set of NMOS and PMOS CNFETs to demonstrate how key device characteristics such as I_{ON}, I_{ON}/I_{OFF}, inverse sub-threshold slope, and $|V_T|$ are unchanged after n-type doping. As seen in Figure 2.5 (a,b), both the NMOS and PMOS devices exhibit nearly identical drive current and I_{ON}/I_{OFF} distributions (average I_{ON} and $\log_{10}(I_{ON}/I_{OFF})$ differ by <6% and <2% respectively).The NMOS and PMOS CNFETs also exhibit similar inverse sub-threshold slope and threshold voltage distributions (quantified by the mean and standard deviation, see Figure 2.5 (c,d)), while having a minimal effect on device-to-device variations. Whereas previously reported doping techniques that usedunstable and air-reactive materials introduce large variations in IV characteristics,[60,66] this combined doping technique avoids these variations by using only air-stable materials (HfO_2 and Ti) that are already integrated within standard silicon-based fabrication processes.

2.4 CNFET CMOS Logic

As a demonstration, we integrate local back gate NMOS and PMOS CNFETs on the same substrate, and demonstrate static CMOS logic gates: inverters, 2-input "not-or" (NOR2), and 2-input "not-and" (NAND2) logic gates with rail-to-rail swing and high gain. Figure 2.6 shows the voltage transfer curve of a fabricated CMOS inverter. It achieves near-rail-to-rail swing (the output voltage swing is >99% ofV_{DD}), with a maximum gain of >10 (Figure 2.6(c,d)). Figure 2.7 shows fabricated two-input CMOS logic gates: CMOS NAND2 and CMOS NOR2 logic gates (circuit schematics in Figure 2.7 (a,e)). In Figure 2.7 (b-d, f-h) both the NAND2 and NOR2 gates achieve near-rail-to-rail swing (the output voltage swing is >99% of V_{DD}), with a maximum gain of >11 and >15 respectively. Importantly, all ofthese logic gates are measured at a scaled supply voltage of 1.2 V_{DD}, without any external biasing.

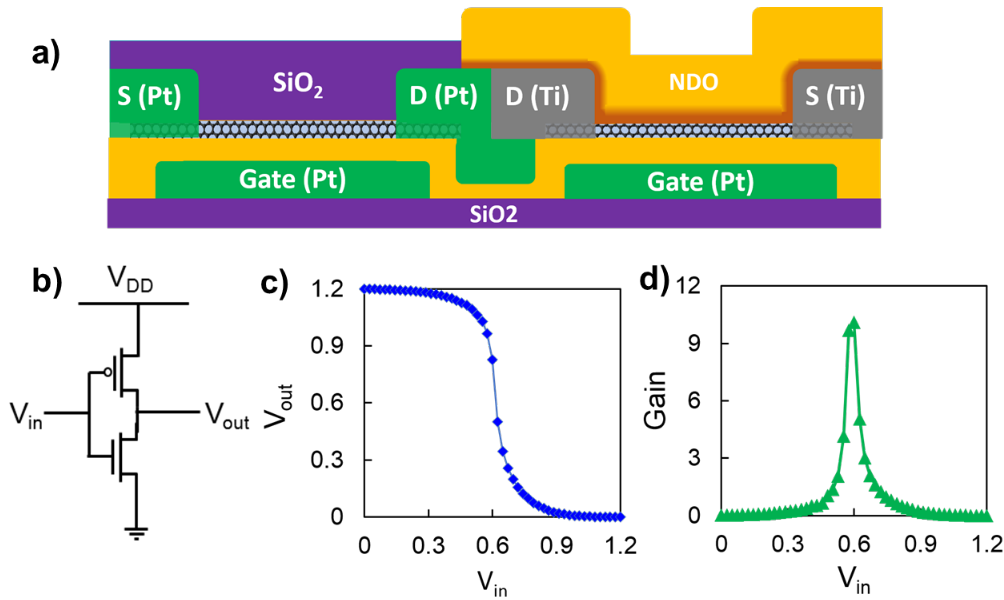


Figure 2.6. Static CMOS inverter fabricated by combing NDO encapsulation with lower work function contact engineering. (a) Cross sectional schematic of local back-gate PMOS and NMOS CNFETs fabricated on the same die. (b) Circuit schematic for CMOS inverter. (c) Voltage transfer curve for fabricated CNFET inverter operating at a V_{DD} of 1.2 V. When $V_{in} = 0$ V, V_{out} reaches 99.92% of V_{DD} and when $V_{in} = V_{DD}$, V_{out} reaches 0.03% of V_{DD}. (d) Plot of inverter gain (change in V_{out} over change in V_{in}) versus V_{in}, where the gain reaches a maximum of 10.

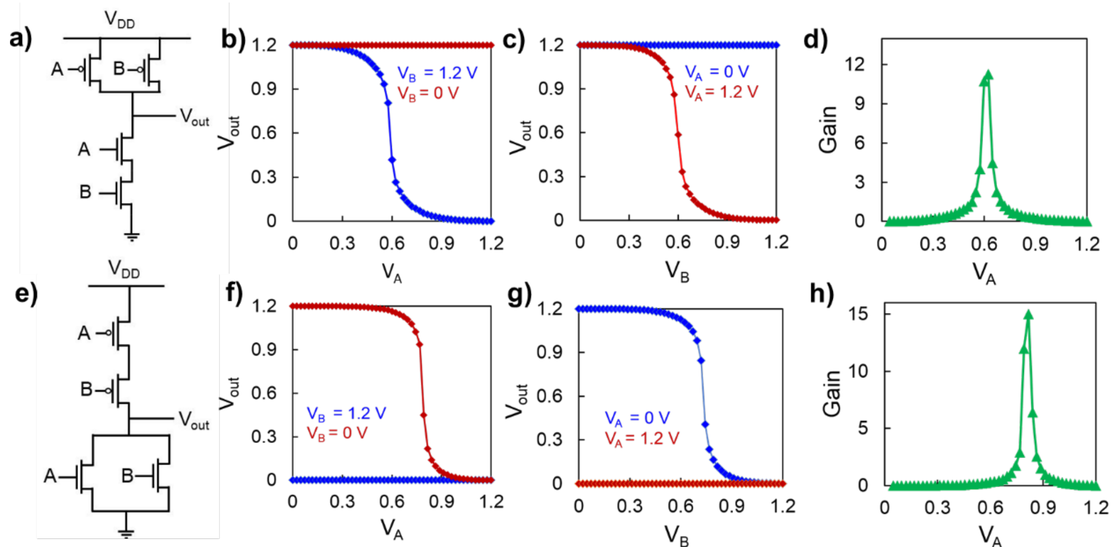


Figure 2.7. Two-input logic gates fabricated by combing NDO encapsulation with lower work function contact engineering. (a) Circuit diagram for static CMOS "not-and" (NAND2) logic gate. Voltage transfer curve for a NAND2 gate (b) when input V_A is swept from 0 to 1.2 V and (c) when input V_B is swept from 0 to 1.2 V. (d) Plot of NAND2 gate gain versus V_A (with $V_B = V_{DD}$), where a maximum gain of 11 is achieved. (e) Circuit diagram for CMOS NOR2 logic gate. Voltage transfer curve for a NOR2 gate (f) when the input V_A is swept from 0 to 1.2 V and (g) when the input V_B is swept from 0 to 1.2 V. (h) Plot of NOR2 gate gain versus V_A, where a maximum gain of 15 is achieved.

2.5 Conclusion

We demonstrate a CNT doping technique that meets all of the requirements for realizing a future CNFET CMOS technology. The key to our technique is leveraging atomic-layer deposition (ALD) to encapsulate CNTs with nonstoichiometric oxides, which can be seamlessly combined with additional techniques (such as work-function engineering). Using this approach, we demonstrate symmetric NMOS and PMOS CNFETs, as well as CMOS logic gates that achieve rail-to-rail output voltage swings of >99.9% and gains of >10 at a supply voltage of 1.2 V_{DD}. Moreover, the results from this work are applicable to a wide range of emerging one-dimensional and two-dimensional nanomaterials (as electrostatic doping is applicable to many ultra-thin body materials[56-58,67]). Therefore, this work realizes a solid-state, air stable, VLSI and silicon-CMOS compatible doping strategy, enabling integration of CNFET CMOS within standard fabrication processes today.

Chapter 3: Modern Microprocessor Built from Complementary Carbon Nanotube Transistors

3.1 Background

Over the past decade, CNT technology has matured: from single CNFETs[9] to individual digital logic gates[10,11] to small-scale digital circuits and systems[7,12,13,14,15,16]. In 2013, this progress led to the demonstration of a complete digital system: a miniature computer[2] comprising 178 CNFETs that implemented only a single instruction operating on only a single bit of data (see Supplementary Information for a full discussion of previous work). However, as with all emerging nanotechnologies, there remained a substantial disconnect between these small-scale demonstrations and modern systems comprising tens of thousands of FETs (for example, microprocessors) to billions of FETs (for example, high-performance computing servers). Perpetuating this divide is the inability to achieve perfect atomic-level control of nanomaterials at macroscopic scales (for example, yielding CNTs of consistent 10-Å diameter uniformly across industry-standard wafer substrates of diameter 150–300 mm). The resulting intrinsic defects and variations have made the realization of such modern systems infeasible. For CNTs, there are three major intrinsic challenges: material defects, manufacturing defects and variability.

(1) Material defects. Although semiconducting CNTs form energy-efficient FET channels, the inability to precisely control CNT diameter and chirality results in every CNT synthesis containing some percentage of metallic CNTs. Metallic CNTs have little to no bandgap and therefore their conductance cannot be sufficiently modulated by the CNFET gate, resulting in high leakage current and potentially incorrect logic functionality[17].

(2) Manufacturing defects. During wafer fabrication, CNTs inherently 'bundle' together, forming thick CNT aggregates[18,19]. These aggregates result in CNFET failure (reducing CNFET circuit yield), as well as prohibitively high particle contamination rates for very-large-scale integration (VLSI) manufacturing.

(3) Variability. Energy-efficient complementary metal–oxide–semiconductor (CMOS)[20] digital logic requires the ability to fabricate CNFETs of complementary polarities (p-CNFETs and n-CNFETs) with well-controlled characteristics (for example, tunable and uniform threshold voltages, and p- and n- CNFETs with matching on- and off-state current). Previous techniques for realizing CNT CMOS haverelied on either extremely reactive, non-air-stable, non-silicon CMOS-compatible materials[21,22,23,24,25] or have lacked tunability, robustness and reproducibility[26]. This has severely limited the complexity of CNT CMOS demonstrations (a complete CNT CMOS digital system has not yet been fabricated).

Although much previous work has focused on overcoming these challenges, none meets all of the strict requirements for realizing VLSI systems. In this work, we overcome the intrinsic CNT defects and variations to enable a demonstration of a beyond-silicon modern microprocessor: RV16X-NANO, designed and fabricated entirely using CNFETs. RV16X-NANO is a 16-bit microprocessor based on the open-source and commercially available RISC-V instruction set processor, running standard RISC-V 32-bit instructions on 16-bit data and addresses. It integrates >14,000 CMOS CNFETs, and operates as modern microprocessors do today (for example, it can run compiled programs; in addition, we demonstrate its functionality by executing all types and formats of instructions in the RISC-V instruction-set architecture). This is made possible by our manufacturing methodology for CNTs (MMC)—a set of original processing and circuit design techniques that are combined to overcome theintrinsic CNT challenges. The key elements of MMC are:

(1) RINSE (removal of incubated nanotubes through selective exfoliation). We propose a method of removing CNT aggregate defects through a selective mechanical exfoliation process. RINSE reduces CNT aggregate defect density by >250× without affecting non-aggregated CNTs or degrading CNFET performance.

(2) MIXED (metal interface engineering crossed with electrostatic doping). Our combined CNT doping process leverages both metal contact work function engineering as well as electrostatic doping to realize a robust wafer-scale CNFET CMOS process. We experimentally yield entire dies with >10,000 CNFET

CMOS digital logic gates (2-input 'not-or' gates with functional yield 14,400/14,400, comprising 57,600 total CNFETs), and present a wafer-scale CNFET CMOS uniformity characterization across 150-mm wafers (such as analyzing the yield for more than 100 million possible combinations of cascaded logic gate pairs).

(3) DREAM (designing resiliency against metallic CNTs). This technique overcomes the presence of metallic CNTs entirely through circuit design. DREAM relaxes the requirement on metallic CNT purity by about 10,000× (relaxed from a semiconducting CNT purity requirement of 99.999999% to 99.99%),without imposing any additional processing steps or redundancy. DREAM is implemented using standard electronic design automation (EDA) tools, has minimal cost, and enables digital VLSI systems with CNT purities that are available commercially today.

Importantly, the entire MMC is wafer-scale, VLSI-compatible and is seamlessly integrated within existing infrastructures for silicon CMOS—both in terms of design and of processing. Specifically, RV16X-NANO is designed with standard EDA tools, and leverages only materials and processes that are compatible with and exist within commercial silicon CMOS manufacturing facilities. Together, these contributions establish a robust CNT CMOS technology and represent a major milestone in the development of beyond-silicon electronics.

3.2 RV16X-NANO

Figure 3.1 shows an optical microscopy image of a fabricated RV16X-NANO die alongside three-dimensional to-scale rendered schematics of the physical layout. It is the largest CMOS electronic system realized using beyond-silicon nanotechnologies: comprising 3,762 CMOS digital logic stages, totaling 14,702 CNFETs containing more than 10 million CNTs, and includes logic paths comprising up to 86 stages of cascaded logic between flip-flops (that is, that must evaluate sequentially in a single clock cycle). It operates with supply voltage (VDD) of 1.8 V, receives an external referenced clock (generating local clock

signals internally), receives inputs (instructions and data) from and writes directly to an off-chip main memory (dynamic random-access memory, DRAM), and stores data on- chip in a register file. No other external biasing or control signals are supplied. Furthermore, RV16X- NANO has a three-dimensional (3D) physical architecture, as the metal interconnect layers are fabricated both above and below the layer of CNFETs; this is in contrast to silicon-based systems in which all metal routing can only be fabricated above the bottom layer of silicon FETs (see Methods). In RV16X-NANO, the metal layers below the CNFETs are primarily used for signal routing, while themetal layers above the CNFETs are primarily used for power distribution (Fig. 3.1c, d). The fabrication process implements five metal layers and includes more than 100 individual processing steps (see Methods and section 'MMC' for details). This 3D layout, with routing above and below the FETs promises improved routing congestion (a major challenge for today's systems[27]), and is uniquely enabled by CNTs (owing to their low-temperature fabrication; see Methods).

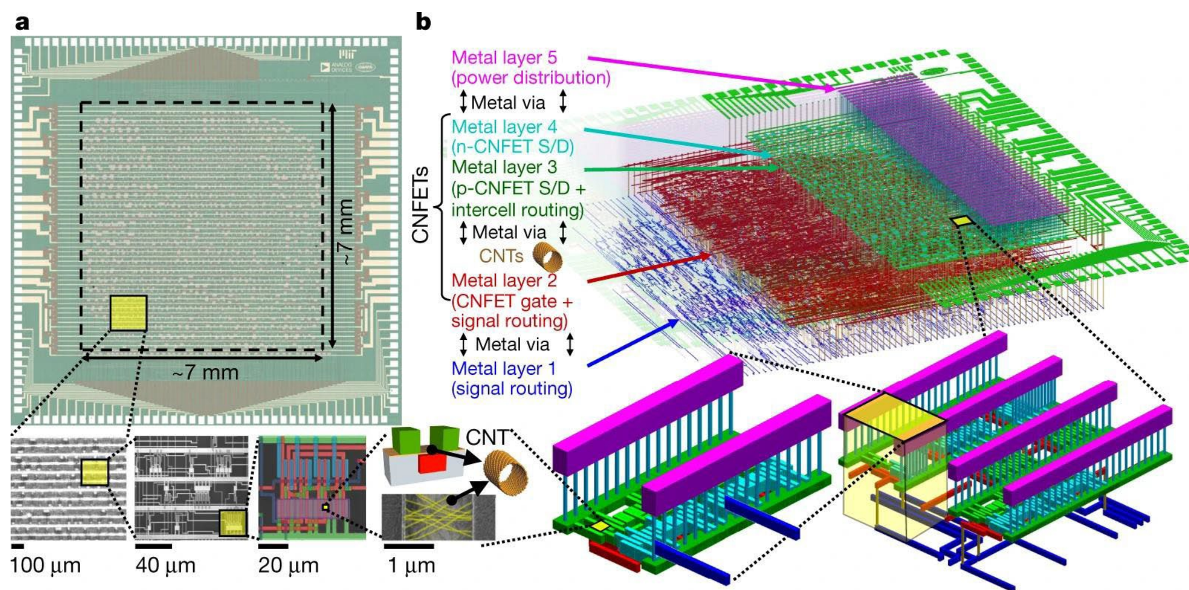


Figure 3.1. RV16X-NANO. a) Image of a fabricated RV16X-NANO chip. The die area is 6.912 mm ×6.912 mm, with input/output pads placed around the periphery. Scanning electron microscopy images with increasing magnification are shown below (one image is false-coloured to match the colouring inthe schematic in b). RV16X-NANO is fabricated entirely from CNFET CMOS, in a wafer-scalable, VLSI-compatible, and silicon-CMOS compatible fashion. b) Three-dimensional to-scale rendered schematic of the RV16X-NANO physical layout (all dimensions are to scale except for the z axis, whichis magnified to clarify each individual vertical layer). RV16X-NANO leverages a new three-dimensional (3D) physical architecture in which the CNFETs are physically located in the middle of the stack, with metal routing both above and below.

3.3 Physical Design

The design flow of RV16X-NANO leverages only industry-standard tools and techniques: we create a standard process design kit (PDK) for CNFETs as well as a library of standard cells for CNFETs that is compatible with existing EDA tools and infrastructure without modification. Our CNFET process design kit includes a compact model for circuit simulations that is experimentally calibrated to our fabricated CNFETs. The standard cell library comprises 63 unique cells, and includes both combinational and sequential circuit elements implemented with both static CMOS and complementary transmission-gate digital logic circuit topologies (see Supplementary Information for a full list of standard library cells, including circuit schematics and physical layouts). We use the CNFET process design kit to characterize the timing and power for all of the library cells, which we experimentally validate by fabricating and measuring all cells individually (see Supplementary Information for full description and experimental characterization of the standard cell library). A full description of our industry-practice VLSI design methodology, including how we implement DREAM during logic synthesis and place-and-route, is provided in the Methods.

3.4 Computer Architecture

Figure 3.2 illustrates the architecture of RV16X-NANO, which follows conventional microprocessor design (implementing instruction fetch, instruction decode, register read, execute/memory access, and write-back stages). It is designed from RISC-V, a standard open instruction-set architecture used in commercial products today and gaining widespread popularity in both academia and industry[28,29]; see https://riscv.org/wp-content/uploads/2017/05/Tue1345pm-NVIDIA-Sijstermans.pdf and https://www.westerndigital.com/company/innovations/risc-v). RV16X-NANO is derived from a full 32-bit RISC-V microprocessor supporting the RV32E instruction set (31 different 32-bit instructions, see Supplementary Information), while truncating the data path width from 32 bits to 16 bits, and reducing the number of registers from 16 to 4. It is designed using the publicly available software Bluespec

(https://bluespec.com/), and is verified using a Satisfiability Modulo Theories (SMT)-based bounded model checking against a formal specification of the RISC-V instruction-set architecture (see Supplementary Information). To demonstrate the correct functionality of the microprocessor, we experimentally run and validate correct functionality of all types and formats of instructions on the fabricated RV16X-NANO. Figure 3.3 shows the first program executed on RV16X-NANO: the famous 'Hello, World'. See Methods and Supplementary Information for schematics, operational details and experimental measurements.

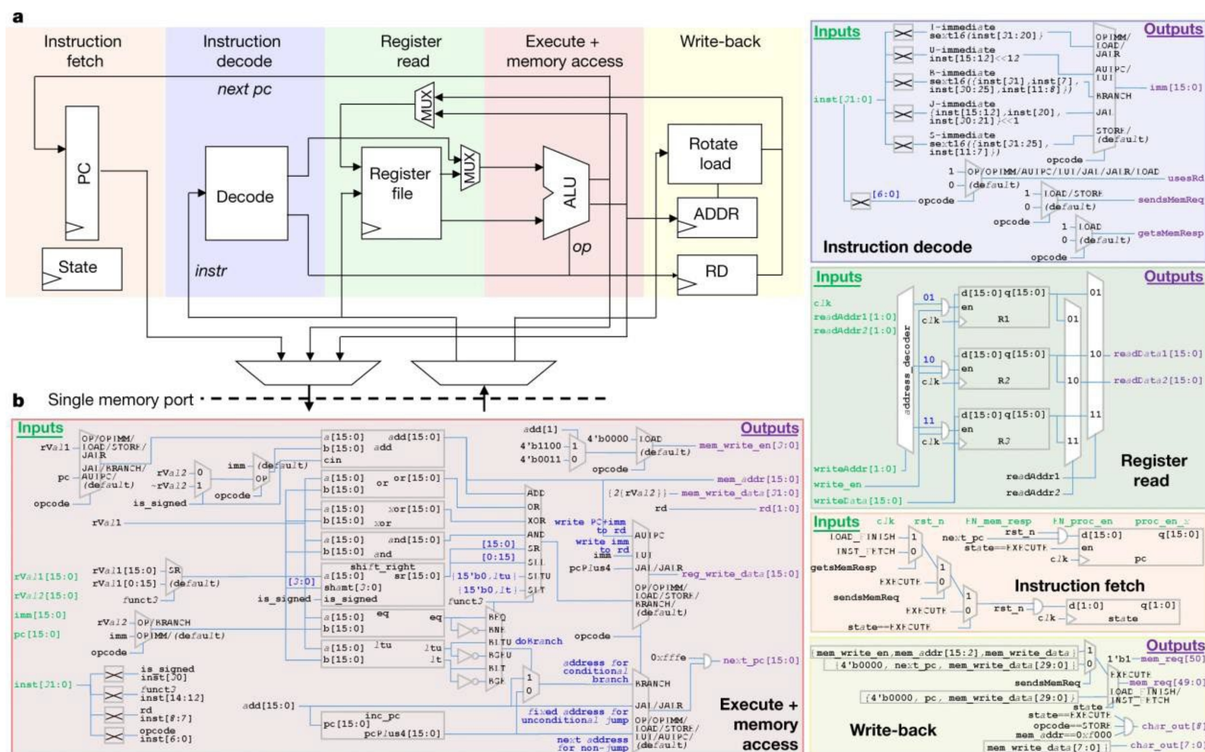


Figure 3.2. Architecture and design of RV16X-NANO. a) Block diagram showing the organization of RV16X-NANO, including the instruction fetch, instruction decode, register read, execute + memory access, and write-back stages. See Supplementary Information section 'RISC-V: Operational Details' for definitions of terms. **b)** Schematics describing the high-level register transfer level (RTL) description of each stage, including inputs, outputs and signal connections. Additional information on the RV16X-NANO is in the Supplementary Information.

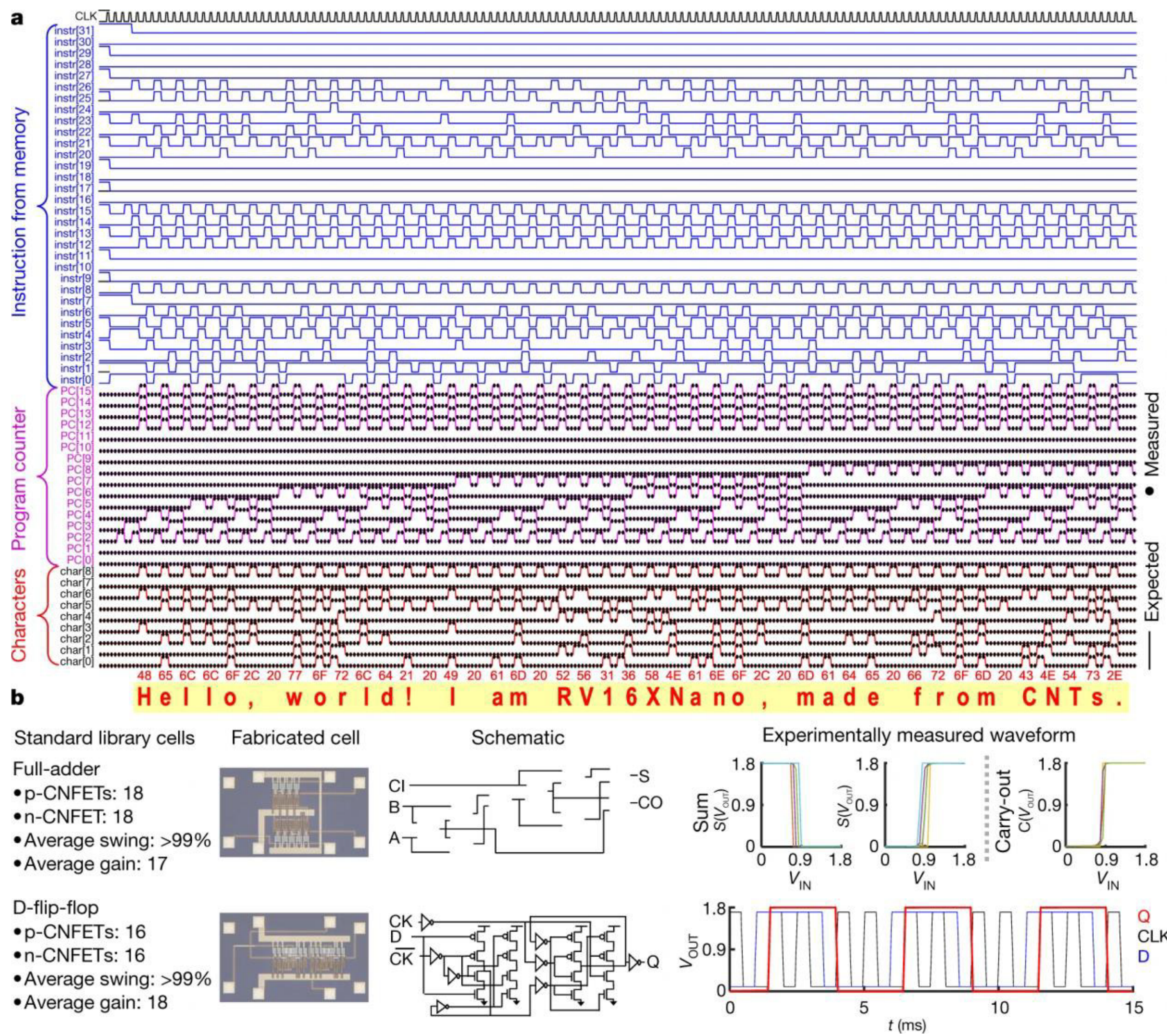


Figure 3.3. RV16X-NANO experimental results**. a)** Experimentally measured waveform from RV16X-NANO, executing the famous 'Hello, World' program. The waveform shows the 32-bit instruction fetched from memory, the program counter stored in RV16X-NANO, as well as the character output from RV16X-NANO. Below the waveform, we convert the binary output (shown in red in hexadecimal code) to their ASCII characters, showing RV16X-NANO printing out "Hello, world! I am RV16XNano, made from CNTs." In addition to this program, we test functionality by executing all of the 31 instructions within RV32E (see Supplementary Information). **b**) RV16X-NANO is designed using conventional electronic design automation (EDA) tools, leveraging our CNT process design kit and CNT CMOS standard cell library. An example combinational cell (full-adder) and example sequentialcell (D-flip-flop) are shown alongside an optical microscopy image of the fabricated cells, their schematics, as well as their experimentally measured waveforms. For the full-adder, we show the outputs (sum and carry-out outputs) for all possible biasing conditions in which sweeping the voltage of input (from 0 to V_{DD}) causes a change in the logical state of the output (that is, for the full adder, with $C_{OUT} = A*B + B*C_{IN} + A*C_{IN}$, with A = logical '0' and B = logical '1', then sweeping C_{IN} from '0'to '1' causes C_{OUT} to change from logical '0' to logical '1'). (CI indicates C_{IN} and CO indicates C_{OUT}.) For the sum output $S(V_{OUT})$, there are 12 such

conditions: six where V_{OUT} has the same polarity as the swept input (positive unate) and six where V_{OUT} has the opposite polarity to the swept input (negative unate). For the carry-out output $C(V_{OUT})$ there are six such conditions (all positive unate); the measurements are overlaid over one another in **b**). Gain for all transitions is >15, with output voltage swing >99%. The D-flip-flop waveform (voltage versus time) illustrates correct functionality of the positive edge-triggered D-flip-flop (output state Q shows correct functionality based on data input D and clock input CLK). CK and C¯K¯C¯K¯ are the clock input and the inverse of the clock input, respectively.

3.5. MMC

Here we describe our MMC—a set of combined processing and design techniques that are the foundation for enabling the realization of RV16X-NANO (Fig. 3.4a). All design and fabrication processes are wafer-scale and VLSI-compatible, not requiring any per-unit customization or redundancy.

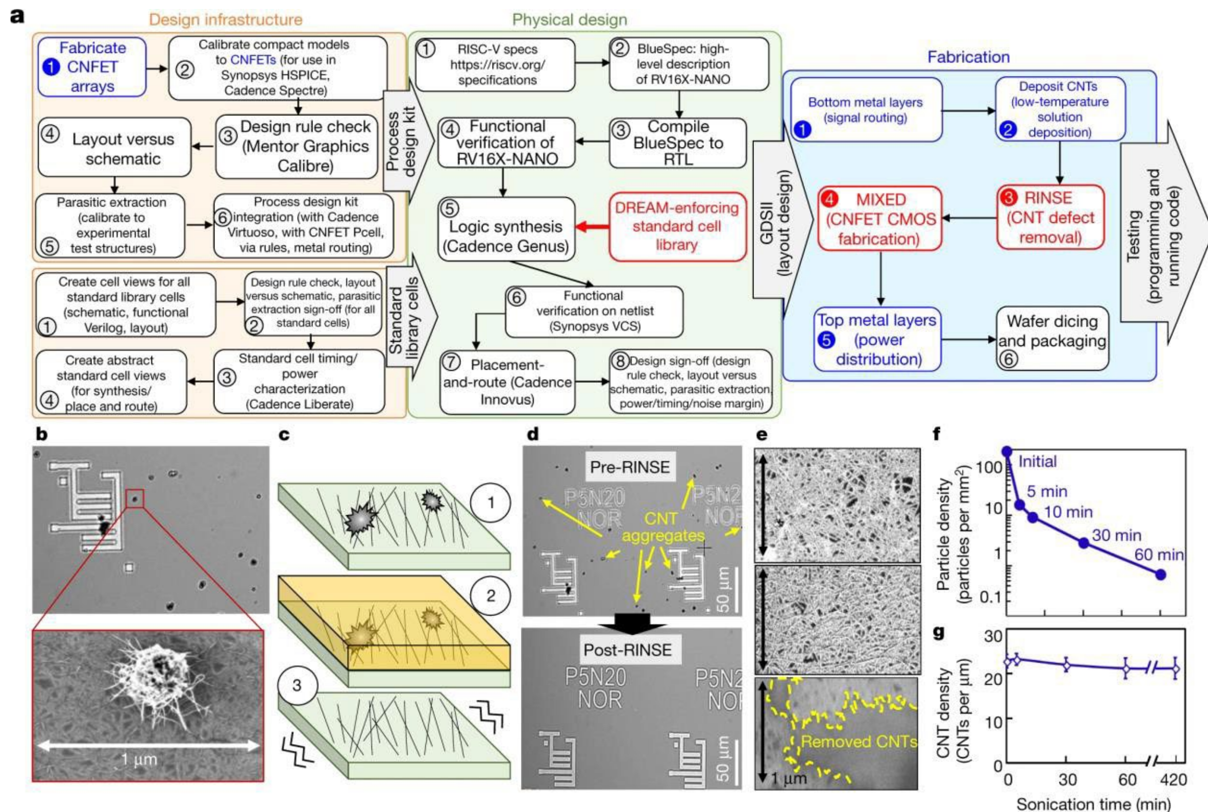


Figure 3.4. MMC. **a**) Design and manufacturing flow for RV16X-NANO, illustrating how MMC seamlessly integrates within conventional silicon-based EDA tools. Black boxes show conventional steps in silicon-CMOS design flows. Blue text indicates steps that are adjusted for CNTs instead of silicon, and red text represents the additions needed to implement the MMC. RV16X-NANO is the first hardware demonstration of a beyond-silicon emerging nanotechnology leveraging a complete RTL-to-GDS physical design flow that uses only conventional EDA tools. Software packages are from Synopsys (https://www.synopsys.com/), Cadence (https://www.cadence.com/) and Mentor Graphics (https://www.mentor.com/). **b**) RINSE. As shown in the scanning electron microscopy images, CNTs

inherently bundle together, forming thick CNT aggregates. These aggregates result in CNFET failure (reduced CNFET yield) as well as prohibitive particle contamination for VLSI manufacturing. **c**) The RINSE process steps: (1) CNT incubation, (2) adhesion coating, (3) mechanical exfoliation (see text for details). **d**, **e**.) RINSE results. After performing RINSE, CNT aggregates are removed from the wafer (as shown in **d**). Importantly, the individual CNTs not in aggregates are not removed from the wafer, while without RINSE, sonication inadvertently removes large areas of all CNTs from the wafer(in **e**, where the top shows CNT incubation pre-RINSE, the middle shows CNTs left on the wafer post-RINSE, and the bottom shows CNTs inadvertently removed from the wafer after sonicating a wafer to remove CNT aggregates without performing the critical adhesion-coating step in RINSE). **f.)** Particle contamination reduction due to RINSE: RINSE decreases particle density by >250×. **g**.) Ideally, individual CNTs are not inadvertently removed during RINSE; increasing the time of step 3 (sonicationtime) to over 7 h results in no change in CNT density across the wafer.

RINSE

The CNFET fabrication process begins by depositing CNTs uniformly over the wafer. 150-mm- diameter wafers (with the bottom metal signal routing layers and gate stack of the CNFET already fabricated for the 3D design) are submerged in solutions containing dispersed CNTs (Methods). Although CNTs are uniformly deposited over the wafer, the CNT deposition also inherently results in manufacturing defects: CNT aggregates deposited randomly across the wafer (Fig. 3.4b). These CNT aggregates act as particle contamination, reducing die yield. Several existing techniques have attempted to remove these aggregates before CNT deposition, but none is sufficient to meet wafer-level yield requirements for VLSI systems: (1) excessive high-power sonication for dispersing aggregates in solution damages CNTs, which results in degraded CNFET performance and does not disperse all CNTs; (2) centrifugation, which does not remove all smaller aggregates (and aggregates can re-form post-centrifugation), (3) excessive filtering, which removes both aggregates and the CNTs themselves from the solution, and (4) etching the aggregates, which is not feasible owing to lack of selectivity versus the underlying CNTs themselves. Instead, to remove these aggregates, we developed a process that we call RINSE, consisting of three steps (Fig. 3.4c):

(1) CNT incubation. Solution-based CNTs are deposited on wafers pre-treated with a CNT adhesion promoter (hexamethyldisilazane, bis(trimethylsilyl)amine).

(2) Adhesion coating. A standard photoresist (polymethylglutarimide) is spin-coated onto the wafer and cured at about 200 °C.

(3) Mechanical exfoliation. The wafer is placed in solvent (N-methylpyrrolidone) and sonicated.

The key to RINSE is the adhesion coating (step 2): without it, sonicating the wafer inadvertently removes sections of CNTs in addition to the aggregates (Fig. 3.4d). The adhesion coating leaves an atomic layer of carbon that remains after step 3, which exerts sufficient force to adhere the CNTs to thewafer surface while still allowing for the removal of the aggregates. Experimental results for RINSE are shown in Fig. 3.4d–g; by optimizing the adhesion-coating cure temperature and time as well as the sonication power and time, RINSE reduces the CNT aggregate density by >250× (quantified by the number of CNT aggregates per unit area) without damaging the CNTs or affecting CNFET performance (see Supplementary Information).

MIXED

After using RINSE to overcome intrinsic CNT manufacturing defects, CNFET circuit fabrication continues. Unfortunately, while energy-efficient CMOS logic requires both p-CNFETs and n-CNFETs with controlled and tunable properties (such as threshold voltage), techniques for realizing CNT CMOStoday result in large FET-to-FET variability that has made the realization of large-scale CNFET CMOS systems infeasible. Moreover, the vast majority of existing techniques are not air-stable (for example, they use materials that are extremely reactive in air[23]), are not uniform or robust (for example, they do not always successfully realize CMOS[22]), or rely on materials not compatible with conventional silicon CMOS processing (for example, molecular dopants that contain ionic salts prohibited in commercial fabrication facilities[24,25]). These challenges are overcome by our processing technique, MIXED, described in Fig. 3.5. The key to MIXED is a combined doping approach that engineers both the oxide deposited over the CNTs to encapsulate the CNFET as well as the metal contact to the CNTs[30]. First, we encapsulate the CNFETs in oxide (deposited by atomic-layer deposition) to isolate them from their surroundings. By leveraging the atomic-layer control of atomic-layer deposition, we also engineer the precise stoichiometry of this oxide encapsulating the CNTs, which enables us to simultaneously electrostatically dope the CNTs (the stoichiometry dictates both the amount of redox reaction at the oxide–CNT interface and the fixed charge

in the oxide). In addition, we engineer the metal source/drain contacts to the CNTs to further optimize the p- and n-CNFETs. We use a lower-work-function metal (titanium) for the contacts to n- CNFETs and a higher-work-function metal for the contacts to p-CNFETs (platinum), improving the on-state drive current of both (for a given off-state leakage current). In contrast to previous approaches, MIXED has the following key advantages: it leverages only silicon CMOS-compatible materials, it allows for precise threshold voltage tuning through controlling the stoichiometry of the atomic-layer deposition doping oxide, and it is robust owing to tight process control by using atomic-layer deposition and only air-stable materials.

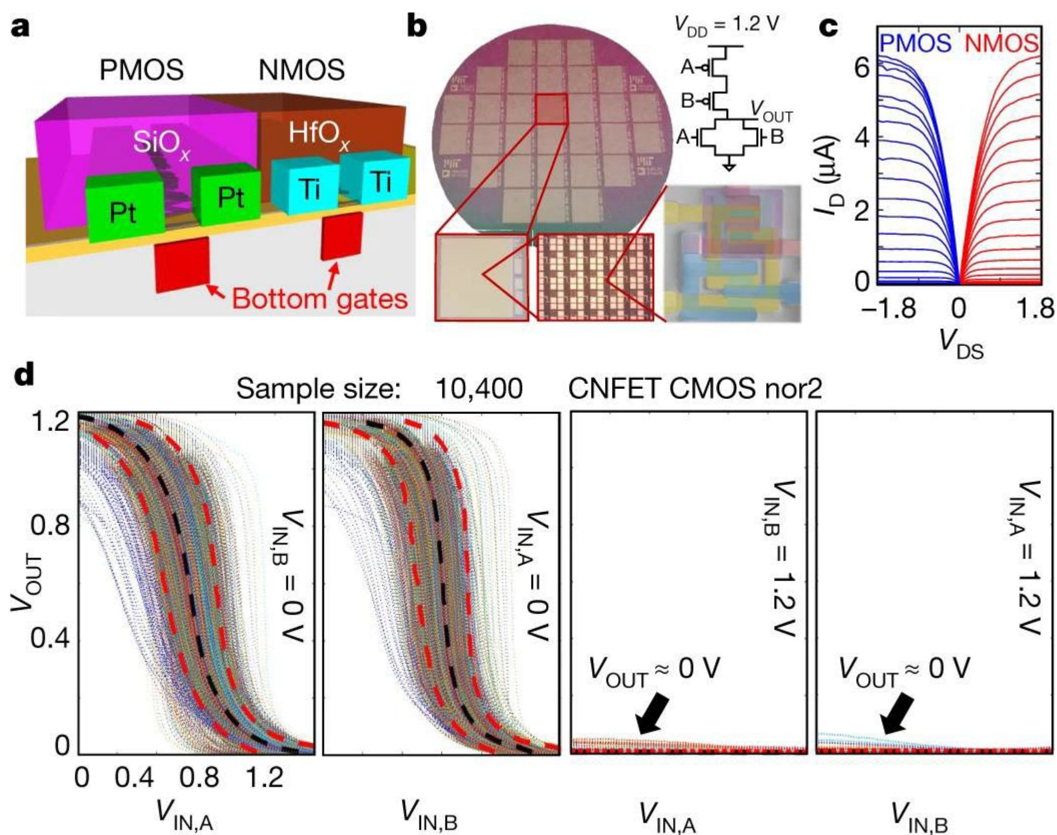


Figure 3.5. MIXED. **a**) Schematic of CNFET CMOS fabricated using MIXED. MIXED is a combined doping process that leverages both metal contact work-function engineering as well as electrostatic doping to realize a robust wafer-scale CNFET CMOS process. We use platinum contacts and SiO_x passivation for p-CNFETs, and titanium contacts and HfO_x passivation for n-CNFETs (see Appendix A2.1 for details). To characterize MIXED, we fabricated dies with 10,400 CNFET CMOS digital logic gates across 150-mm wafers (**b**). **c**, **d**) Experimental results. **c**, I_D versus V_{DS} characteristics showing p-CNFETs and n-CNFETs that exhibit similar I_D– V_{DS} characteristics (for opposite polarity of input bias conditions, for example, $V_{DS,P} = -V_{DS,N}$), achieved with MIXED. The gate-to-source voltage V_{GS} is swept from $-V_{DD}$ to V_{DD} in increments of 0.1 V. See Appendix A2.7 for I_D–V_{GS} and additional CNFET characteristics. **d**) Output voltage transfer curves(VTCs, V_{OUT} vs V_{IN}) for all 10,400 CNT CMOS logic gates

(nor2) within a single die. Each VTC illustrates V_{OUT} as a function of the input voltage of one input (V_{IN}), while the other input is held constant. For each nor2 logic gate (with logical function OUT = !(IN_A|IN_B), we measure the VTC for each of two cases: V_{OUT} versus $V_{IN,A}$ with $V_{IN,B}$ = 0 V and V_{OUT} versus $V_{IN,B}$ with $V_{IN,A}$ = 0 V). All 10,400/10,400 exhibit correct functionality (which we define as having output voltage swing >70%). The black dotted line represents the average VTC (average V_{IN} across all measured VTC for each valueof V_{OUT}), while the red dotted line represents the boundary of ±3 standard deviations (again, acrossall V_{IN} values for each value of V_{OUT}). See Appendix A2.8 for extracted distributions of key metrics from these experimental measurements (gain, output voltage swing and SNM analyzing >100 million possible cascaded logic gates pairs formed from these 10,400 samples), as well as uniformity characterization across the 150-mm wafer. Importantly, despite the high yield and robust CNFET CMOS enabled by MIXED and RINSE, we note that there are outlier gates with degraded output swing (the blue lines in **d**). These outliers are caused by CNT CMOS logic gates that contain metallic CNTs; the third component of the MMC (DREAM; see Fig. 3.6), is a design technique that is essential for overcoming the presence of these metallic CNTs.

Figure 3.5c shows the current–voltage (I–V) characteristics of p-CNFETs and n-CNFETs, demonstrating well-matched characteristics (such as on- and off-state currents). To demonstrate the reproducibility of MIXED at the wafer scale, Fig. 3.5 shows measurements from 10,400/10,400 correctly functioning 2-input ‘not-or’ (nor2) CNFET logic gates within a single die, and 1,000/1,000 correctly functioning nor2 gates randomly selected from across a 150-mm wafer. Additional characterization results (including output voltage swing, gain, and SNM for >100 million possible combinations of cascaded logic gate pairs), are in Appendix A2.8. This demonstrates solid-state, air- stable, VLSI- and silicon-CMOS compatible CNFET CMOS at the wafer scale.

DREAM

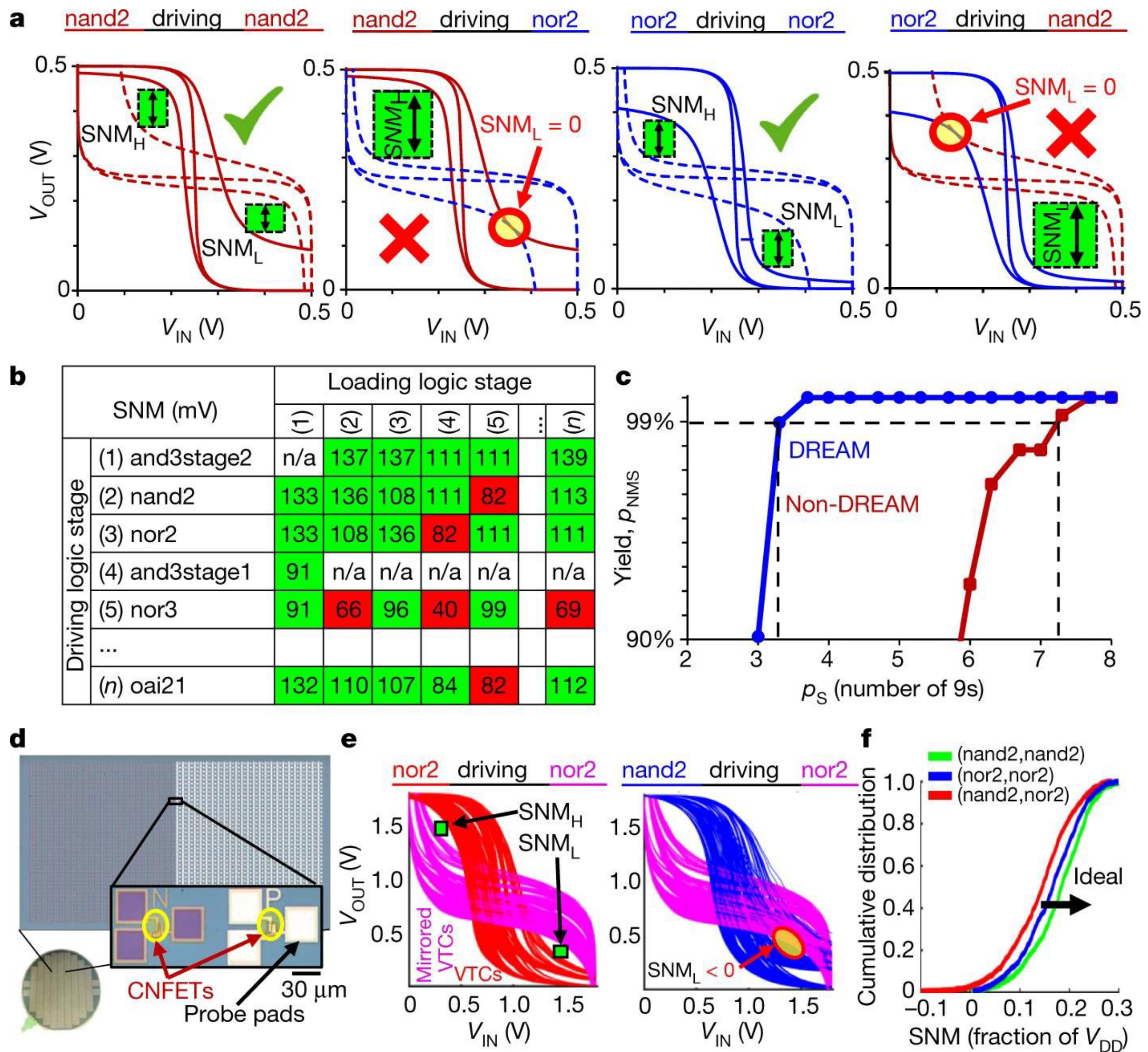
Despite the robust CNFET CMOS enabled by RINSE and MIXED, a small percentage (around 0.01%) of CNTs are metallic CNTs. Unfortunately, a metallic CNT fraction of 0.01% can be prohibitively large for VLSI-scale systems, owing to two major challenges—increased leakage power, which degrades energy-delay product (EDP) benefits, and degraded noise immunity, which potentially results in incorrect logic functionality. To quantify the noise immunity of digital logic, we extract the static noise margin (SNM) for each pair of connected logic stages, using the voltage transfer curves (VTCs) of eachstage (details in Fig. A.2.9.2). The probability that all connected logic stages meet a minimum SNM requirement (SNMR, typically chosen by the designer as a fraction of VDD, for example, SNMR = VDD/4) is p_{NMS}: the probability

that all noise margin constraints are satisfied (Appendix A2.3. Although previous works have set requirements on semiconducting-CNT purity (p_S) based on limiting metallic- CNT-induced leakage power, no existing works have provided VLSI circuit-level guidelines for p_S based on both increased leakage and the resulting degraded SNM. Although p_S of 99.999% is sufficient to limit EDP degradation to ≤5%, SNM imposes far stricter requirements on purity: p_S must be about 99.999999% to achieve $p_{NMS} \geq 99\%$ (analyzed for 1 million gate circuits, Appendix A2.9).

Unfortunately, typical CNT synthesis today achieves a p_S value of only about 66%. While many different techniques have been proposed to overcome the presence of metallic CNTs (Appendix A2.9), the highest reported purity is a p_S of about 99.99%: this is 10,000× below the requirement for VLSI circuits[31,32,33]. Moreover, these techniques have substantial cost, requiring either additional processing steps (for example, applying high voltages for electrical ‘breakdown’ of metallic CNTs during fabrication[10]) or redundancy (incurring substantial energy-efficiency penalties[34]). Here we present and experimentally validate a new technique, DREAM, that overcomes the presence of metallic CNTs entirely through circuit design. The key contribution of DREAM is that it reduces the required p_S by around 10,000×, allowing 99% p_{NMS} with p_S = 99.99% (for circuits with one million logic gates). This enables digital VLSI circuits to use CNT processing available today: p_S = 99.99% is already commercially available (and can also be achieved through several means, including solution-based sorting, which we use in our process for fabricating RV16X-NANO; see Appendix A2.9).

The key insight for DREAM is that metallic CNTs affect different pairs of logic stages uniquely depending on how the logic stages are implemented (considering both the schematic and physical layout). As a result, the SNM of specific combinations of logic stages is more susceptible to metallic CNTs. To improve overall p_{NMS} for a digital VLSI circuit, DREAM applies a logic transformation during logic synthesis to achieve the same circuit functionality, while prohibiting the use of specific logic stage pairs whose SNM is most susceptible to metallic CNTs. As an example, let (GD, GL) be a logic stage pair with driving logic stage GD and loading logic stage GL. Figure 3.6 shows that some logic stage pairs have better SNM in the

presence of metallic CNTs than others, despite using exactly the same VTCs for the logic stages comprising the circuit (in this instance, logic stage pairs (nand2, nand2) and (nor2, nor2) have better SNM than (nand2, nor2) or (nor2, nand2)). Thus, a designer can improve p_{NMS} by prohibiting the use of logic stage pairs that are more susceptible to metallic CNTs, while permitting logic stage pairs that maintain better SNM despite the presence of metallic CNTs.



SNM (mV)		Loading logic stage (1)	(2)	(3)	(4)	(5)	...	(n)
Driving logic stage	(1) and3stage2	n/a	137	137	111	111		139
	(2) nand2	133	136	108	111	82		113
	(3) nor2	133	108	136	82	111		111
	(4) and3stage1	91	n/a	n/a	n/a	n/a		n/a
	(5) nor3	91	66	96	40	99		69
	...							
	(n) oai21	132	110	107	84	82		112

Figure 3.6. DREAM. DREAM overcomes the presence of metallic CNTs entirely through circuit design, and is the final component of the MMC. DREAM relaxes the requirement on metallic CNT purity by about 10,000×, without imposing any additional processing steps or redundancy. DREAM isimplemented using standard EDA tools, has minimal cost (≤10% energy, ≤ 10% delay and ≤ 20% area),and enables digital VLSI systems with CNT purities that are available commercially today (99.99% semiconducting CNT purity). **a**)

VTCs for driving logic stages and mirrored VTCs for loading logic stages, showing SNM simulated for 4 different logic stage pairs (SNM is defined in the Appendix A2.9),with up to two metallic CNTs in all CNFETs. The logic stage pairs: (nand2, nand2) and (nor2, nor2) have better SNM than do (nand2, nor2) and (nor2, nand2) despite all logic stages having exactly the same VTCs. We note that we distinguish logic stages (for example, an inverter) from logic gates (for example, a buffer, by cascading two inverters); a logic gate can comprise multiple logic stages. **b**) Example DREAM SNM table (see Appendix A2 for details, analyzed for a projected 7-nm node with ascaled *V*DD of 500 mV), which shows the minimum SNM for each pair of connected logic stages. As anexample, values less than 83 mV are highlighted in red, indicating that these combinations would not be permitted during design, to reduce overall susceptibility to noise at the VLSI circuit level. **c**) Yield (*p*NMS) versus semiconducting CNT purity for a required SNM level (SNMR) of SNMR = *V*DD/5, shown for the OpenSparc 'dec' module designed using the 7-nm node CNFET standard library cells derived from the ASAP7 process design kit with a scaled *V*DD of 500 mV (details in Appendix A2). **d**) Fabricated CNT CMOS die, comprising 1,000 NMOS CNFETs and 1,000 PMOS CNFETs. Semiconducting CNT purity is *p*S ≈ 99.99%, with around 15–25 CNTs per CNFET. **e**, **f**) Experimental demonstration of DREAM. VTCs for nand2 and nor2 generated by randomly selecting two NMOS andtwo PMOS CNFETs from **d** (some of which contain metallic CNTs). This is repeated to form 1,000 unique nor2 and nand2 VTCs. We then analyze the SNM for over one million logic stage pairs (shown in **f**), corresponding to all combinations of 1,000 VTCs for the driving logic stage and 1,000 VTCs forthe loading logic stage. **e**) A subset of these logic stage pairs; the (nor2, nor2) maintains minimum SNM > 0, while (nand2, nor2) suffers from minimum SNM < 0 in the presence of metallic CNTs; >99.99% of (nor2, nor2) and (nand2, nand2) logic stage pairs achieve SNM > 0 V, while only about 97% of (nand2, nor2) achieve SNM > 0 V. **f**) Cumulative distributions of SNM over one million logic stage pairs.

Beyond this simple example to illustrate DREAM, we also quantify the benefit of DREAM using both simulation and experimental analysis for VLSI-scale circuits; in simulation, we leverage a compact model for CNFETs (derived from ref. 8), which accounts for both semiconducting CNTs and metallic CNTs, to analyze the effect of metallic CNTs on the leakage power, energy consumption, speed and noise susceptibility of physical designs of VLSI-scale circuits at a 7-nm technology node designed using standard EDA tools, with and without DREAM (results are shown in Fig. 3.6; see additional discussion in Supplementary Information). Experimentally, we fabricate and characterize 2,000 CMOS CNFETs fabricated with MIXED (1,000 p-type metal-oxide-semiconductor (PMOS) and 1,000 n-type metal- oxide-semiconductor (NMOS) CNFETs; see Fig. 3.6). Using I–V measurements from these 2,000 CNFETs, we analyze one million combinations of CNFET digital logic gates (whose electrical characteristics are solved using the I–V characteristics of the measured CNFETs; Fig. A.2.9.2) to show the benefits of DREAM in reducing circuit susceptibility to noise. In the Methods, we provide extensivedetails of these analyses and

the implementation of DREAM for arbitrary digital VLSI circuits, including how to implement DREAM using standard industry-practice physical design flows, how we implement DREAM for RV16X-NANO, and an efficient algorithm to satisfy target p_{NMS} constraints (such as $p_{NMS} \geq 99\%$), while minimizing energy, delay and area costs.

3.6 Conclusion

These combined processing and design techniques overcome the major intrinsic CNT challenges. Our complete manufacturing methodology for CNTs (MMC) enables a demonstration of a beyond-silicon modern microprocessor fabricated from CNTs, RV16X-NANO. In addition to demonstrating the RV16X-NANO microprocessor, we thoroughly characterize and analyze all facets of MMC, illustrating the feasibility of our approach and more broadly of a future CNT technology. This work is a major advance for CNTs, paving the way for next-generation beyond-silicon electronic systems.

Chapter 4: Comprehensive Study and Techniques for Improving Carbon Nanotube Field-Effect Transistor Reliability

4.1 Background

As continued silicon transistor scaling yields diminishing gains in computing performance, new beyond-silicon nanotechnologies are being explored. Low-dimensional nanomaterials are promising due to their nearly ideal carrier transport with simultaneously ultra-thin body (~1 nm thickness). Carbon nanotubes (CNTs) are prominent among low-dimensional nanomaterials for next-generation digital very-large-scale-integration (VLSI) integrated circuits (ICs), as CNT field-effect transistors (CNFETs) are projected to improve the energy efficiency of digital VLSI circuits by an order of magnitude *versus* that of silicon CMOS (quantified by EDP, energy-delay product).[††] Moreover, CNFETs can be fabricated at low-temperature (<400°C), and thus are back-end-of-line (BEOL)-compatible, providing further EDP benefits by enabling monolithic three-dimensional (3D) ICs.[43,52,68] Importantly, CNFETs have matured rapidly over recent years with recent demonstrations including the first modern microprocessor built from CNFETs, increasingly complex monolithic 3D ICs,[68] as well as CNFETs integrated within commercial semiconductor manufacturing facilities.[2,43,68-72]

Despite their exciting potential, the inability to controllably dope CNTs using conventional substitutional

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[††] The ability to fabricate CMOS CNFETs at low temperatures using electrostatic doping enables the fabrication of monolithic 3D circuits with multiple vertical tiers of computing circuitry. Each vertical tier of devices must be fabricated <400 °C, as temperatures >400 °C can damage and destroy bottom-layer devices and metal interconnects. Realizing monolithic 3D circuits with CNFETs is projected to yield substantial additional benefits beyond the 10× energy efficiency benefits of using CNFETs in standard single-layer chips.[106]

doping has hindered the development of complementary CNFET circuits that integrate both PMOS and NMOS CNFETs (CNFET CMOS).[3‡‡] To address the challenges of doping CNTs, prior works have focused on several alternatives. For example, low work function metal source/drain contacts (such as scandium, erbium, lanthanum, or calcium) and reactive molecular dopants (*e.g.* ionic salts and organometallic compounds that are not solid-state materials) have been used to achieve *n*-type CNTs.[22,24,47,59] However, due to their high reactivity, these doping materials exacerbate device-to-device variability and show poor stability in air.

In contrast to the previously mentioned doping techniques, "electrostatic doping" is a promising approach for doping low-dimensional materials. Electrostatic doping involves encapsulating nanomaterials in dielectric films, using either interface- or fixed- charges within the dielectric to electrostatically dope the channel region.[56,58,60,61,67] Prior works have shown that solid-state dielectrics can beused to tunably dope a wide array of low-dimensional materials through electrostatic doping.[30,73] Moreover, experimental demonstrations have shown that electrostatic doping can be achieved by depositing dielectric films such as HfO_2, Al_2O_3, and Si_3N_X at low temperatures (<250 °C), allowing this doping technique to be used to fabricate complementary metal oxide semiconductor (CMOS) circuits in the BEOL.[30,58,61] Due to the compatibility of this doping method with low-temperature BEOL processing, electrostatic doping is a viable strategy for fabricating CMOS circuits over previously- fabricated layers of circuitry to realize novel monolithic 3D IC architectures.[68,71,72]

While these advantages make electrostatic doping a promising approach for doping CNTs, there has been no in-depth characterization of the reliability of electrostatic doping. Such comprehensive reliability tests (*i.e.,* measuring the long-term degradation and any recovery of the device's transfer characteristics after elevated temperature and electrical stress conditions) are required to advance electrostatic doping beyond

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‡‡ Inserting dopants directly into the CNT lattice through substitutional doping has been shown to disrupt the stable sp^2 structure of the CNT. By disrupting the pristine CNT lattice, substitutional dopants have led to increased scattering and lower carrier mobility. Moreover, a controllable process for substitutional doping ofCNTs has yet to be realized due to the difficulty of inserting dopants into the ultrathin body of the CNT.[104-106]

proof-of-concept demonstrations to become a commercially-viable CMOS technology. In particular, demonstrating the reliability of a commercial CMOS technology requires the following:

(1) low device-to-device variations.

(2) after achieving low device-to-device variations, variability must not increase over time (*e.g.,* devices must show long-term stability when in an idle state).

(3) devices must pass comprehensive reliability stress testing (*i.e.* show stable transfer characteristics under operating conditions, *e.g*., when the devices are subject to elevated temperature and electrical bias stress).

Here we show that, with optimizations discussed in this work, electrostatic doping can meet all of these requirements for a reliable CMOS technology. We perform the first ever reliability characterization of CNFETs in a commercial semiconductor fabrication and testing facility, following the same standard reliability testing protocols used for evaluating commercial silicon MOSFETs. Moreover, we elucidate a path for achieving robust electrostatically doped CNFETs that are resilient to temperature and bias stresses and discuss the differences between the reliability degradation of CNFETs versus commercial silicon FETs. To demonstrate the compatibility of this approach with BEOL CMOS processing, we integrate the above techniques into a full CNFET CMOS fabrication process flow, realizing static random access memory (SRAM) CNFET-based memory cells and show correct operation over 90 days. By systematically evaluating the reliability of electrostatically doped CNFETs, this work addresses key concerns regarding the robustness and reliability of both electrostatic doping and CNFETs, critical considerations when considering the eventual adoption of a technology.

4.2 Electrostatically Doped CNFET Process Flow

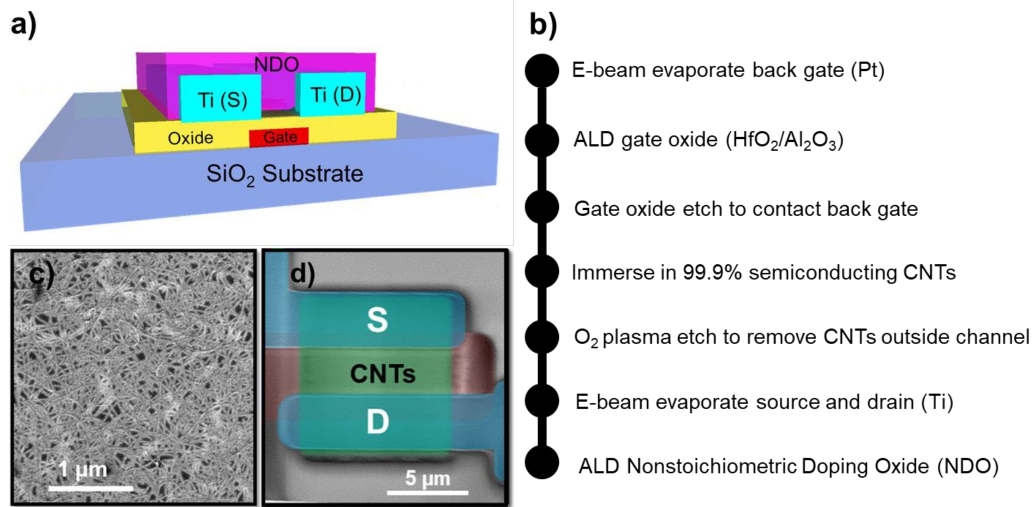


Figure 4.1: Electrostatically doped CNFET. (a) Schematic of a local back-gated NMOS CNFET encapsulated with a Nonstoichiometric Doping Oxide (NDO) layer. (b) Process flow for fabricating NMOS CNFETs. Top-view scanning electron microscope (SEM) images of the wafer (c) immediately after CNT deposition (CNT density ~20 CNTs/µm) over the gate dielectric and (d) after Ti source and drain contacts (false-colored blue) are deposited over the semiconducting CNT channel (false-colored light green).

Figure 4.1a illustrates a typical local back-gate CNFET fabricated in this work. We leverage back-gate geometries as recent works establishing CNFETs within commercial manufacturing facilities similarly use back-gate geometries.[70,71] Figure 4.1b outlines the fabrication steps for electrostatic doping. First, the gate metal is lithographically patterned over a starting conventional 150 mm silicon substrate. A bilayer gate dielectric comprising of Al_2O_3 and HfO_2 is uniformly deposited over the wafer using atomic layer deposition (ALD). Vias are lithographically defined and etched using a dry reactive ion etch (RIE) through the gate dielectric to contact the underlying gate metal. The wafer is then immersed in >99.9% semiconducting CNT solution (modified Nanointegris IsoSol-100) to uniformly deposit a monolayer film of CNTs on the surface, see Figure 4.1c. After CNT deposition, CNTs outside the CNFET channel regions are removed by an oxygen plasma etch. Source and drain metal electrodes (titanium, a lower- work function metal used for NMOS CNFET source and drain contacts, see ref. 20) are then lithographically patterned. Figure 4.1c

shows a SEM image of the fabricated CNFET after source drain deposition. To electrostatically dope the CNTs *n*-type, a HfO_X nonstoichiometric doping oxide[5§§] (NDO, see ref. 20) is deposited uniformly over the wafer by ALD as shown in Figure 4.1a. The entire CNFET fabrication process flow is <300 °C, rendering it BEOL-compatible.

4.3 Experimental Results and Discussion

Uniformity and Air-stability of Electrostatically Doped CNFETs

While the previously described process flow realizes electrostatically doped CNFETs, the resulting devices can suffer from large device-to-device variability (see Figure 4.2a). In identifying the origin of CNFET variability, previous studies have highlighted the role of randomly distributed fixed oxide charges in exacerbating threshold voltage (V_{TH}) variability.[74,75] In addition to large variability, the electrostatically doped CNFETs also show poor stability in air (see Figure 4.3b). Since the V_{TH} of an electrostatically doped CNFET is highly sensitive to the stoichiometry of the NDO layer, we hypothesized that the NDO stoichiometry may be susceptible to oxygen in the ambient. For example, increasing the oxygen content in the HfO_2 NDO layer has been previously shown to decrease *n*-type doping (increase the V_{TH}) of electrostatically doped CNFETs.[30]

[§§] The stoichiometry of the HfO_X NDO layer can be tuned by controlling the reactant pulsing parameters (ie. by carefully controlling pulse time, pulse sequence, temperature, etc.). Previous work has shown that modifying the stoichiometry of the HfO_X NDO enables device engineers to tune the degree of n-type doping of the semiconducting CNTs in the channel[20].

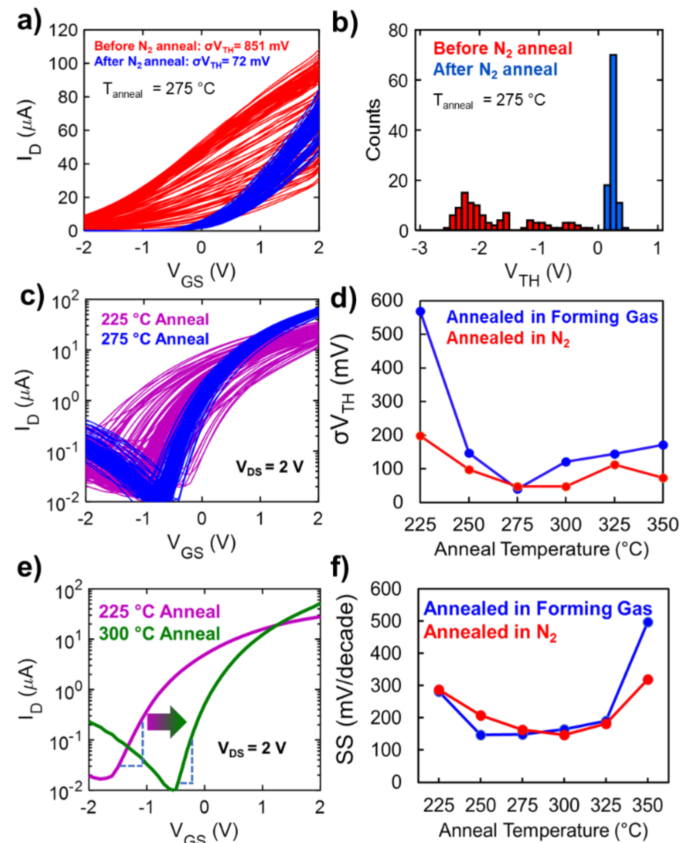


Figure 4.2: Effect of thermal annealing on electrostatically doped CNFET transfer characteristics. (a) I_D-V_{GS} curves of 100 electrostatically doped CNFETs before and after 275 °C N_2 anneal for 5 min. (b)V_{TH} histogram distribution before and after the anneal is performed, where V_{TH} is determined by extracting the linear I_D-V_{GS} region to the x-axis and finding the x-intercept point. (c) I_D-V_{GS} curves for100 CNFETs annealed in forming gas at 225 °C and 100 CNFETs annealed at 275 °C. (d) Line plot of V_{TH} standard deviation (σV_{TH}) vs. annealing temperature for devices annealed in forming gas and N_2 ambients. (e) I_D-V_{GS} curves of an electrostatically doped CNFET annealed in N_2 at 225 °C and a separate electrostatically doped CNFET annealed in N_2 at 300 °C for 5 min. The dashed blue lines indicate the approximate region where the inverse subthreshold slope is measured. (f) Line plot of average inverse subthreshold slope (SS) vs. annealing temperature for devices annealed in forming gas and N_2 environments. Each data point in (d) and (f) is extracted using the I_D-V_{GS} data from 100 measured electrostatically doped CNFETs for each annealing condition (1,200 distinct devices measured in total). No devices are excluded from the plotted data.

To test these hypotheses and resolve the variability and air-instability of CNFETs, we leverage multiple techniques inspired by existing processing steps employed to mitigate fixed charges in silicon MOSFETs.[76,77] First, we perform an annealing step to reduce the density of fixed charges, thereby minimizing their contribution to V_{TH} variability. To test the effectiveness of annealing on electrostatically doped CNFETs, we characterize the impact of different annealing gas ambients and temperatures on device-to-device variations (Figure 4.2c and 4.2d). Through these tests, we find that an optimal annealing temperature of 275 °C lowers the V_{TH} standard deviation (σV_{TH}) by >10× and that, in contrast to silicon MOSFETs,[78-83] the annealed CNFETs are not affected by the introduction of H_2 in the annealing ambient (*i.e.* both N_2 and N_2+H_2 anneals achieve a minimum σV_{TH} at 275ºC, discussed below). Moreover, in Figure 4.2f we show that annealing at this optimized temperature simultaneously improves inverse subthreshold slope (SS) by 2×. Since SS improves with the reduction of trap states near the channel,[84] the correlation between SS improvement and lower V_{TH} variations further suggests that these trap states are indeed a significant source of variability in CNFETs and can be mitigated by annealing. To then achieve long-term CNFET air-stability, we test our hypothesis that the NDO stoichiometry is sensitive to ambient oxygen and encapsulate our electrostatically doped CNFETs in silicon nitride immediately after annealing in N_2 environment (see encapsulated device schematic in Figure 4.3a). Figure 4.3 shows that nitride encapsulation effectively shields the NDO layer from the ambient oxygen and thus significantly reduces long-term drift (nitride encapsulation reduces V_{TH} drift to <1.7% of V_{DD} over a 56 day period, whereas the unencapsulated CNFETs' V_{TH} shifts by >100% of V_{DD} after just 8 days).

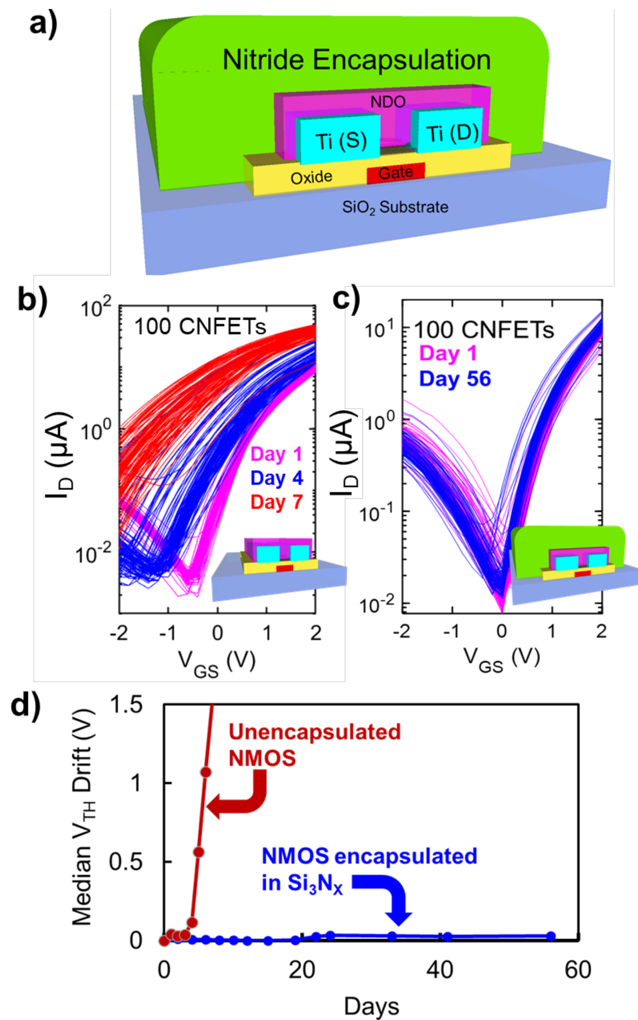


Figure 4.3: Silicon nitride encapsulation technique. (a) Schematic of an electrostatically doped CNFET that has been encapsulated in silicon nitride. (b) I_D-V_{GS} curves for 100 unencapsulated electrostatically doped CNFETs 1,4, and 7 days after annealing in N_2 at 275 °C. (c) I_D-V_{GS} curves for 100 electrostatically doped CNFETs 1 day and 56 days after having been encapsulated in silicon nitride. (d) Median V_{TH} shift for annealed electrostatically doped CNFETs that have been exposed to air (red) and encapsulated in silicon nitride (blue). All I_D-V_{GS} curves are measured at a V_{DS} = 2V.

These experimental results highlight four key outcomes:

1) Both the thermal anneal and nitride encapsulation techniques can be effective at temperatures <400 °C and are still BEOL compatible for monolithic 3D ICs.

times in between process steps, such in-situ processing improves the manufacturability of electrostatically doped CNFETs by eliminating this queue time.

3) Electrostatic doping that leverages control of the NDO stoichiometry can be air-stable when the NDO is encapsulated by an oxygen diffusion barrier such as nitride.

4) The fact that adding H_2 to the annealing ambient resulted in no significant improvement provides important insights concerning the reliability of electrostatically doped CNFETs (discussed below).

Evaluating Reliability in a Commercial Semiconductor Fabrication and Testing Facility

Ensuring the long-term air stability of electrostatically doped films is an essential first step in demonstrating the reliability of electrostatically doped CNFETs. However, evaluating the feasibility of electrostatic doping as a commercial CMOS technology requires comprehensive stress testing of electrostatically doped CNFETs following the same standard reliability testing protocols used for evaluating commercial silicon MOSFETs. To ensure that commercial CMOS technologies meetstringent product lifetime requirements, standard reliability testing protocols stress the device at or above the device's normal electrical bias and temperature operating conditions to accelerate degradation mechanisms. A conventional reliability test that is essential for estimating the operating lifetime of MOSFETs is bias temperature instability (BTI)[85-89]. In NMOS devices, positive bias temperature instability (PBTI) mimics the positive bias stress applied to the NMOS gate during normal device operation[90-94]. When a MOSFET is stressed at these conditions, changes in I_D-V_{GS} characteristics (*i.e.* inverse subthreshold slope, drive current (I_{ON}), and V_{TH}) are measured to evaluate the MOSFET's reliability to PBTI stress. In this section, we evaluate the PBTI reliability of the previously described electrostatically doped CNFETs in a commercial semiconductor fabrication and testing facility using the same testing protocols used for evaluating commercial silicon MOSFETs in that facility (see Figure 4.4 for PBTI test setup).

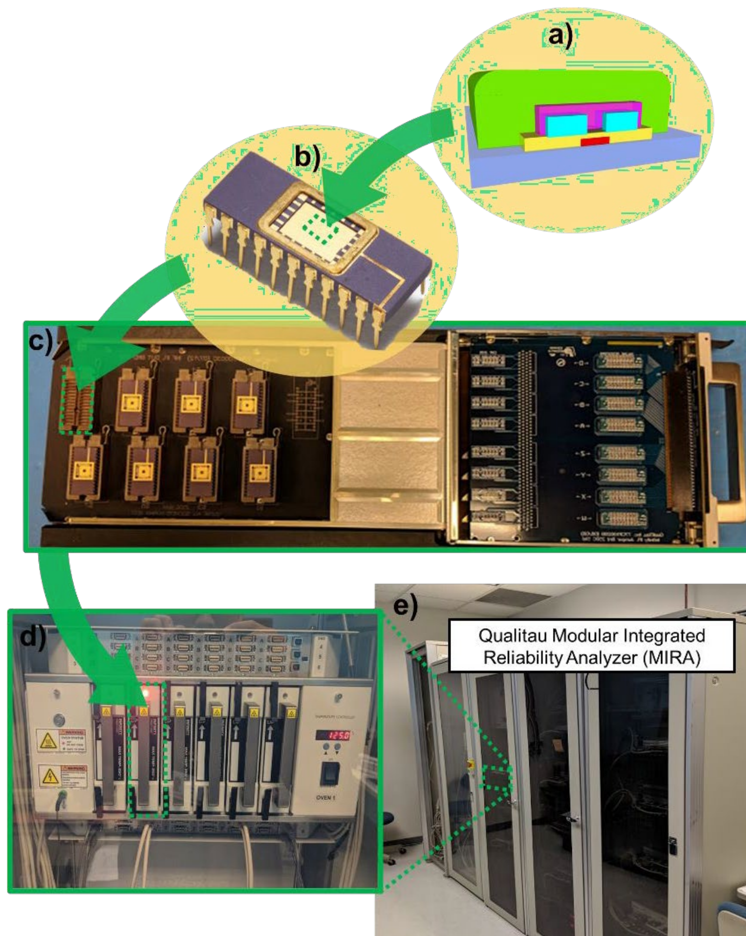


Figure 4.4: Reliability testing setup in a commercial semiconductor fabrication and testing facility. Dies containing fabricated CNFETs (a) are attached and wire bonded to a ceramic dual in-line package (b). The packaged device is then inserted into the testing board (c), which is then inserted into a slot of the QualiTau Modular Integrated Reliability Analyzer (d, e) for programmable temperature and electricalbias control.

First, we evaluate the reliability of electrostatically doped CNFETs by performing detailed analysis of changes in the CNFET's inverse subthreshold slope during PBTI stress. Since changes to SS can distort measurements of I_{ON} and V_{TH} (*i.e.* in practice, it is difficult to meaningfully compare the V_{TH} of two transfer characteristics with vastly different SS), we must first ensure that SS remains stable before measuring degradation of V_{TH} and I_{ON}. We extract SS using the "slow I_D-V_{GS} method", which interrupts the PBTI stress biasing in order to take a full I_D-V_{GS} transfer sweep to measure SS (for ~10 seconds). In Figure 4.5a and

4.5b, we use the slow I_D-V_{GS} method to obtain full transfer sweeps of electrostatically doped NMOS CNFETs that are stressed at a gate bias of 1.8V ($V_{GS,stress}$=1.8V) and a chamber temperature of 85 °C throughout a 30,000 second stress period. Figure 4.5a shows substantial changes in the transfer characteristics of exposed CNFETs (where the electrostatic doping layer is exposed to air),while Figure 4.5b shows relatively stable transfer characteristics for nitride encapsulated CNFETs duringthe stress period. To quantify these changes, Figure 4.5d plots the corresponding changes in SS for the devices measured in Figure 4.5a and 4.5b throughout the stress period. The unencapsulated (e.g., ambient-exposed) CNFETs suffer a >2× increase in SS. In stark contrast, the CNFETs encapsulated with nitride experience minimal SS degradation of <6% versus their initial value. Thus, nitride encapsulation is anessential step for ensuring the SS stability of electrostatically doped films during stress conditions.

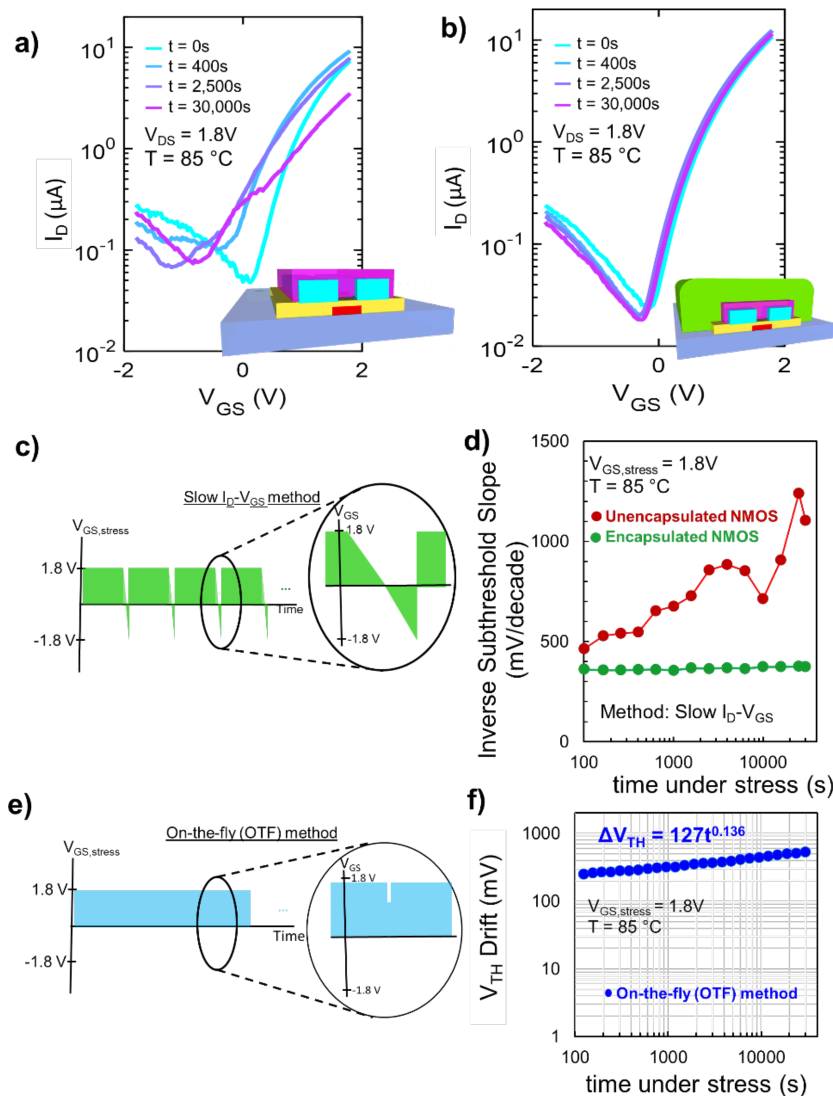


Figure 4.5: Reduction in PBTI degradation after nitride encapsulation. (a) Degradation of I_D-V_{GS} characteristics of an unencapsulated CNFET stressed for 30,000s. (b) Degradation of I_D-V_{GS} characteristics of a nitride encapsulated CNFET stressed for 30,000s. (c) Voltage plot showing how $V_{GS,stress}$ changes over time when using the slow I_D-V_{GS} method. (d) Corresponding changes in subthreshold slope for devices in (a,b) measured using the slow I_D-V_{GS} method. (e) Voltage plot showing how $V_{GS,stress}$ changes over time when using the on-the-fly method. (f) V_{TH} drift for a nitride encapsulated CNFET subject to PBTI stress measured using the on-the-fly method. During the stress period, $V_{GS,stress}$= 1.8V and T = 85 °C.

Having demonstrated SS stability in nitride encapsulated CNFETs, we can now measure the degradation of I_{ON} and V_{TH} (the most commonly measured transfer characteristics in BTI reliability benchmarking[87,90,95,96]). Measuring these additional metrics requires a more precise measurement technique than the slow I_D-V_{GS}

method. While the slow I_D-V_{GS} measurements are necessary to determine the overall transfer characteristics and SS degradation throughout the stress period, taking this full transfer sweep measurement perturbs the applied gate bias stress ($V_{GS,stress}$) whenever a measurement is performed during the stress period (see voltage plot in Figure 4.5c). When $V_{GS,stress}$ is lowered during this perturbation, the device can rapidly recover device degradation (discussed in greaterdetail below), causing the slow I_D-V_{GS} method to underestimate degradation in I_{ON} and V_{TH}. To mitigatethe effect of this perturbation, we use the "on-the-fly" (OTF) method to extract I_{ON} and V_{TH}. During the OTF method, a single current measurement is performed at a single V_{GS} and V_{DS} value instead of requiring a full transfer sweep (see Figure 4.5e). Supporting Information Figure 4.6a illustrates how, givena single I_D-V_{GS} sweep obtained before stress is applied, a single current point measurement can be usedto extract changes in I_{ON} and V_{TH} during stress. Since the commercial testing setup used in this study can perform an OTF current measurement in ~600 μs, the perturbation of $V_{GS,stress}$ is minimized and the OTF measurements are less susceptible to underestimating degradation.

The OTF measurements of I_{ON} and V_{TH} degradation can be fit to an underlying power law, which can be leveraged to identify potential mechanisms responsible for the degradation. In Figure 4.5f, we use the OTF method to calculate V_{TH} drift of a nitride encapsulated CNFET under the same stress conditions as Figure 4.5b. The CNFET degradation closely followed a power law dependence after fitting the V_{TH} drift measurements in Figure 4.5f (a power law is also fit to I_{ON} degradation measurements in Figure A3.3.2). A similar power law dependence has been widely reported for silicon MOSFETs when stressed at elevated electrical and temperature conditions.[90,95,96] However, whereas the power law dependence of silicon MOSFET V_{TH} degradation is commonly attributed to the diffusion of hydrogen that passivates dangling bonds in the channel, the dominant degradation mechanism in CNFETs has yet to be elucidated. To identify the dominant degradation mechanism in a FET, the timedecay exponent in the power law is often used. In silicon MOSFETs, this time decay exponent is typically ~0.17, which is correlated to the rate of hydrogen diffusion through SiO_2.[97,98] In contrast, the CNFET measured in Figure 4.5f exhibits a lower time decay exponent (n = 0.136), suggesting a differentlong-term degradation mechanism than hydrogen diffusion in

the electrostatically doped CNFETs. Our hypothesis that stress induced V_{TH} degradation in CNFETs is not dominated by hydrogen diffusion is similarly supported by the annealing tests discussed previously, where the addition of H_2 during the N_2anneal had a negligible impact on passivating defect states responsible for V_{TH} variability.

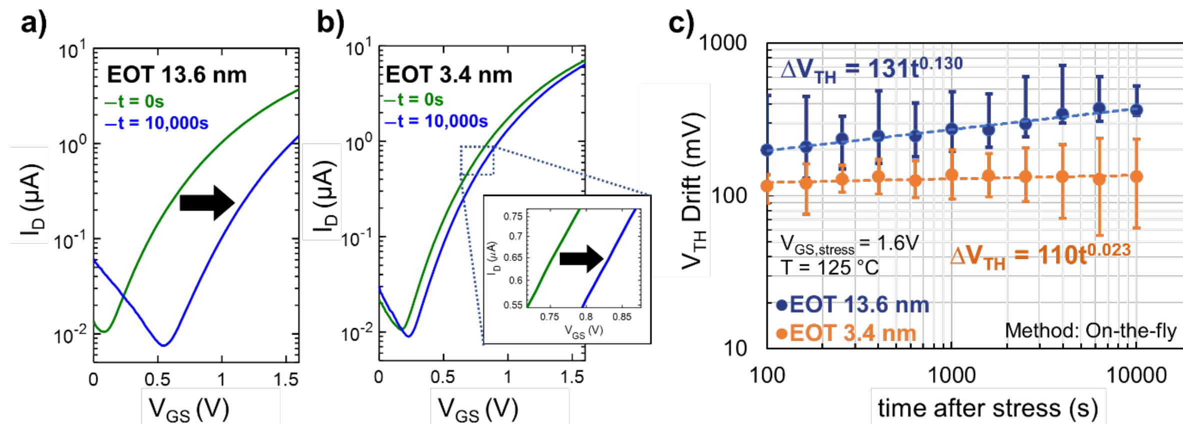


Figure 4.6: Mitigating PBTI degradation through EOT scaling of gate oxide. (a) I_D-V_{GS} curves of an encapsulated CNFET with EOT of 13.6 nm before and after stress is applied. (b) I_D-V_{GS} curves of an encapsulated CNFET with EOT of 3.4 nm before and after stress is applied. Inset shows a shift in thetransfer characteristics in the region where the on-the-fly voltage is measured. (c) Corresponding mean V_{TH} shifts for 8 CNFETs with a gate oxide EOT of 3.4 nm and 8 CNFETs with a gate oxide EOT of 13.6nm, where V_{TH} is extracted using on-the-fly method. Error bars indicate maximum and minimum V_{TH} shifts measured in each sample. All data collected in (a, b, c) is obtained at a stress condition of $V_{GS,stress}$ = 1.6V and T = 125 ºC.

To identify the long-term CNFET degradation mechanism and further improve the reliability of electrostatically doped CNFETs, in Figure 4.6 we study the dependence of CNFET PBTI degradation on the effective oxide thickness (EOT) of the gate oxide. EOT scaling has improved PBTI reliability in high-*k* metal gate (HKMG) silicon MOSFETs by reducing the contribution of bulk oxide traps to PBTI degradation. Moreover, these EOT scaling studies helped to identify bulk oxide traps in the high-*k* gate oxide as a significant source of PBTI degradation in HKMG silicon MOSFETs.[90,95] To measure the degradation of I_D-V_{GS} characteristics in CNFETs, a full I_D-V_{GS} transfer sweep is obtained once immediately before bias stress is applied and a second time immediately after bias stress is removed. Figure 4.6a and Figure 4.6b

show the pre-stress and post-stress I_D-V_{GS} transfer curves for nitride encapsulated CNFETs with a gate oxide EOT of 13.6 nm and 3.4 nm respectively. The device with the thinner gate oxide in Figure 4.6b shows noticeably less long-term V_{TH} drift compared to the thicker gate oxide devices. This conclusion is confirmed by the OTF measurements in Figure 4.6c, which are performed at intermittent points during the stress period on multiple CNFETs with gate oxide EOTs of 13.6 nm and 3.4 nm. Fitting a power law to these OTF data points reveals a higher time decay exponent ($n = 0.130$) for the thicker gate oxide devices compared to the thinner gate oxide devices ($n = 0.023$). As was the case with highly scaled HKMG silicon MOSFETs, the dependence of the time decay exponent on gate oxide thickness suggests that the underlying long-term PBTI degradation mechanismin CNFETs is associated with the bulk traps and charges in the gate oxide, rather than at the channel interface.[35,38,43,44] This insight into the long-term degradation mechanism of CNFETs provides a viablepath for further reducing PBTI degradation in CNFETs by scaling the gate oxide below an EOT of 3.4nm.

Whereas EOT scaling is a promising path for further reducing V_{TH} drift over long periods of unperturbed PBTI stress, normal operation of MOSFETs in integrated circuits include periods where stress is removed when the MOSFET turns off and V_{GS} approaches zero. As discussed previously, MOSFETs recover from degradation during the relaxation phase when electrical bias stress is removed (*i.e.* by gradually returning to its initial V_{TH} value before stress was applied[47]). Since poor BTI recovery can cause V_{TH} degradation to accumulate over repeated cycles of BTI stress and relaxation,[48] the rate at which MOSFETs recover from stress is critical for evaluating their reliability in IC applications. We evaluate the recovery of nitride encapsulated CNFETs after stress is removed in Figure 4.7. In this case, we employ the OTF method to obtain fast data point readouts needed to capture the rapid recovery that occurs immediately after initiating the relaxation phase. Figure 4.7a shows the relaxation phase for a CNFET after $V_{GS,stress}$= 3.6 V is removed. As a reference, in Figure 4.7a, we overlaid data from literature for the recovery of a HKMG *p*-MOSFET stressed at comparable gate oxide electric field (E_{ox}) and measured using a similar OTF method.[96] In Figure 4.7b and 4.7c, we normalize the rate of recovery (normalizing recovery with respect to the maximum V_{TH}

drift at the end of the stress period) to compare the rate of recovery in different test conditions. Figure 4.7b-4.7c shows that the normalized rate of recoveryis independent of applied bias stress yet improves with thinner gate oxide EOT. Thus, scaling EOT in CNFETs helps by both reducing long term PBTI degradation (by lowering the time decay exponent) and simultaneously improving the rate of recovery from PBTI stress.

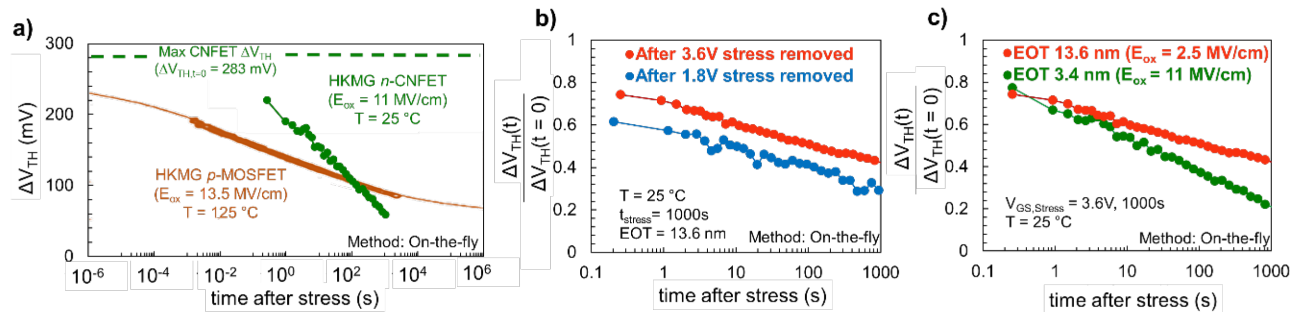


Figure 4.7: Electrostatically doped CNFET recovery after PBTI stress is removed. (a) V_{TH} recovery after stress has been removed for an electrostatically doped CNFET (green) and HKMG p-MOSFET[44] (orange). (b) Recovery of normalized V_{TH} degradation after different levels of gate bias stress are removed from the device. (c) Recovery of normalized V_{TH} degradation for electrostatically doped CNFETs with different gate oxide thicknesses. All measurements of CNFETs in (a,b,c) were made using the OTF method at T = 25 °C and all CNFETs were encapsulated in nitride.

Robustness of Electrostatically Doped CMOS Circuits

As a final demonstration of these approaches, we integrate the nitride encapsulation technique with electrostatic doping to experimentally realize a robust CMOS 6T-SRAM cell. The false-colored SEM of the 6T-SRAM cell is shown in Figure 4.8a and its corresponding circuit diagram in Figure 4.8b. We measure the read and write capabilities of the SRAM immediately after fabrication in Figure 4.8c and after 90 days left unbiased in ambient air in Figure 4.8d. The read and write waveforms recorded in Figure 4.8c and 4.8d demonstrate continued functionality of the SRAM cells after the 90 day period.

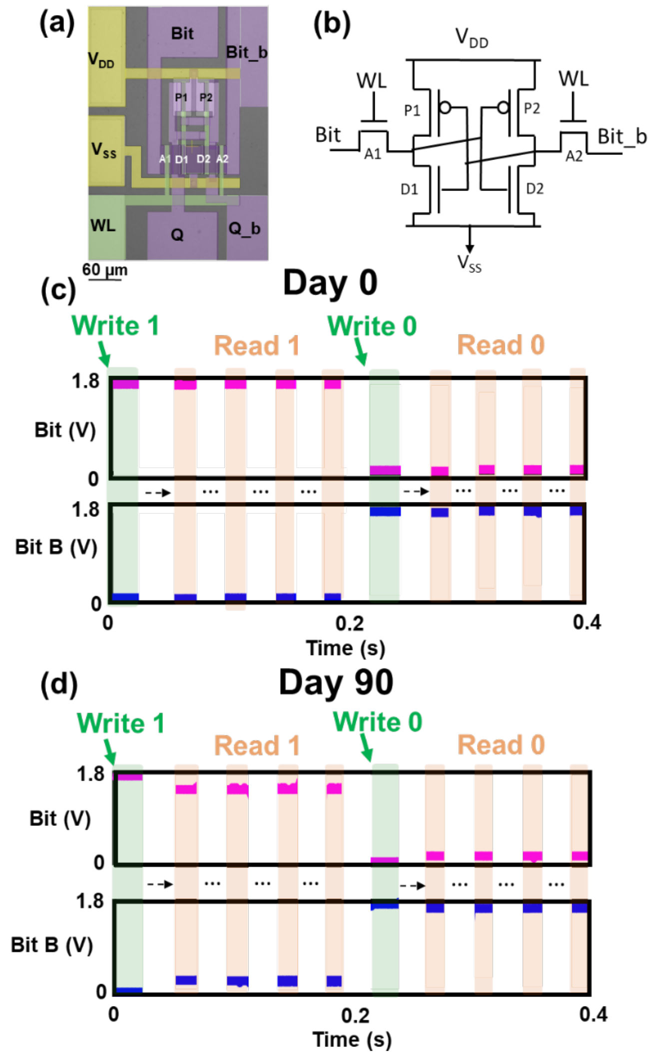


Figure 4.8: 6T-SRAM stability with silicon nitride encapsulation. (a) False-colored SEM of a fabricated 6T-SRAM cell where the NMOS CNFETs are encapsulated in nitride. (b) Circuit diagram for the 6T-SRAM cell. Read and write waveforms for a single 6T-SRAM cell measured on (c) day 0 and (d) day 90.

4.4 Conclusion

Through performing a comprehensive study of the reliability of electrostatically doped CNFETs, this work identifies a future path to enable electrostatic doping to meet the requirements of a commercial CMOS technology. Moreover, the results from this work are applicable to a variety of emerging one- dimensional and two-dimensional nanomaterials that can be controllably doped using electrostatic doping. Additionally, all the processing required to achieve low variations and long-term stability is performed at low temperature <400 °C, making these techniques compatible with BEOL processing. This work thus addresses key concerns regarding the robustness of electrostatic doping and its feasibility as a commercial CMOS technology.

Chapter 5: Concluding Remarks

Carbon nanotubes are prominent among a variety of nanotechnologies that are being considered for next-generation energy-efficient electronic systems[2,3,4]. Owing to the nanoscale dimensions and simultaneously high carrier transport of CNTs[5,6], digital systems built from FETs fabricated with CNTsas the transistor channel are projected to improve the energy efficiency of today's silicon-based technologies by an order of magnitude. However, the inability to (1) fabricate complementary metal– oxide–semiconductor (CMOS) CNFET circuits that integrate both PMOS and NMOS CNFETs, (2) perfectly control intrinsic nanoscale defects and variability in carbon nanotubes, and (3) the absence ofcomprehensive reliability testing of CNFETs have precluded the realization of very-large-scale integrated CMOS systems built from CNFETs and the adoption of CNFETs as a commercially-viable CMOS technology.

In this thesis, we have presented and experimentally validated a path for next-generation beyond-silicon electronics systems. We introduce a novel approach for achieving CMOS CNFET circuits through leveraging a tunable electrostatic doping technique. This work also presents a comprehensive manufacturing methodology for CNTs, which encompasses a set of original processing and circuit design techniques that are combined to overcome the intrinsic CNT challenges of variability, manufacturing defects, and material defects. As a demonstration of the feasibility of implementing thismanufacturing methodology, we experimentally demonstrated RV16X-NANO, a beyond-silicon modern microprocessor fabricated from CNTs. Moreover, we perform the first ever reliability characterization of CNFETs in a commercial semiconductor fabrication and testing facility, following the same standard reliability testing protocols used for evaluating commercial silicon MOSFETs. Importantly, this work illustrates how developing a comprehensive manufacturing methodology that spans the entire chip development stack – from the initial design infrastructure to the ultimate fabrication of the chip – is needed to realize VLSI systems built from emerging nanotechnologies.

Beyond this thesis, the MMC has already been used by industry to realize the first large-scale commercial CNFET electronic systems. To date, the BEOL-compatible processing techniques of the MMC have been used by a US foundry to enable, for the first time, heterogeneous integration of logic and memory within the BEOL within a commercial foundry leveraging emerging nanotechnologies.[71] The MMC has also been employed to successfully fabricate new system architectures, including a monolithic 3D imaging system that integrates CNFET computing circuitry directly over the silicon imager.[68] Further adoption of the MMC within the high-volume manufacturing facilities of a US foundry will enable even more exciting new system architectures beyond these promising initial demonstrations. Future work should continue to build upon this progress by leveraging these new manufacturing capabilities to experimentally realize a broad range of novel monolithic 3D systems that are made possible through the MMC. The manufacturing methodology for CNTs described in this thesis thus paves the way for next-generation beyond-silicon electronic systems.

Appendix A1: Extended Discussion on Electrostatic Doping of CNTs using Nonstoichiometric Doping Oxides

Appendix 1.1 Additional CNFET electrical characterization

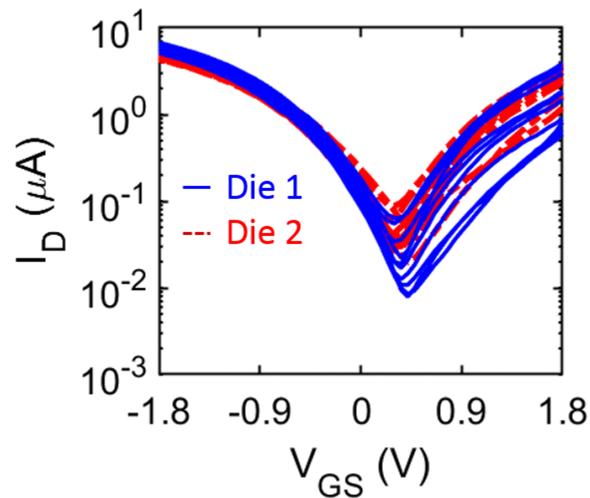


Figure A1.1.1: Comparison of 2 independently processed wafers containing CNFETs identically doped with 3:1 Hf:H_2O ratios, demonstrating reproducibility. I_D-V_{GS} plots are measured at V_{DS}= 1.8V.

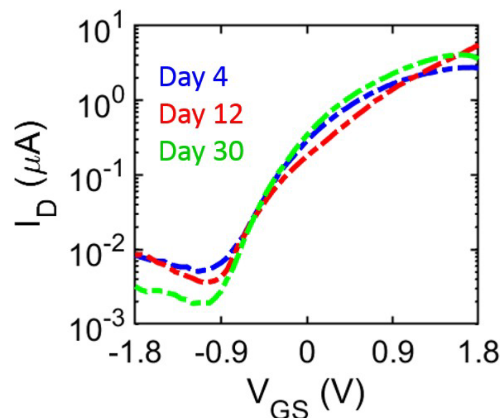


Figure A1.1.2: CNFET measured at V_{DS}=1.8V at different time intervals after fabrication, demonstrating air-stability.

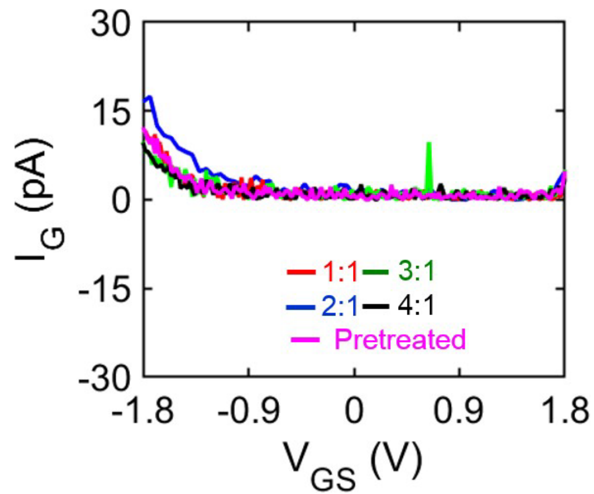


Figure A1.1.3: Gate leakage of CNFETs doped with nonstoichiometric HfO_X.

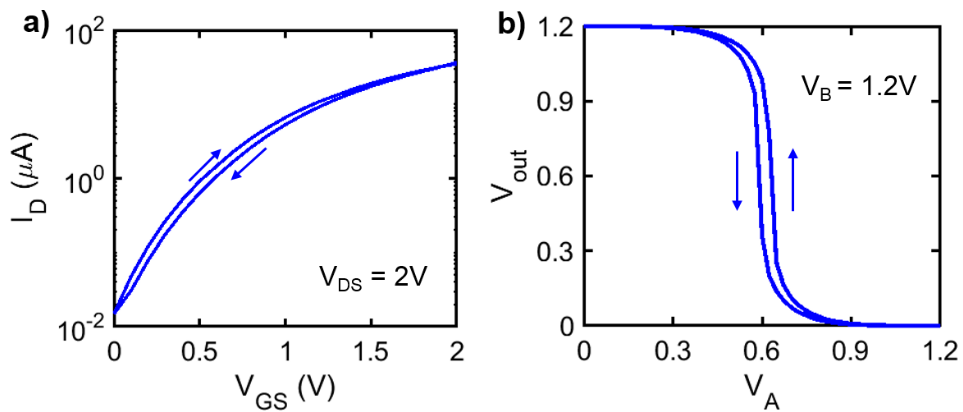


Figure A1.1.2: Hysteresis in NDO encapsulated CNFETs. a) Hysteresis of a local back-gatedCNFET (CNFET fabricated with the same process as described in Figure 2.4b). b) Hysteresisof CMOS NAND2 logic gate (see Figure 2.7). Arrows indicate direction of sweep.

Appendix 1.2 Effective Schottky Barrier Height Modeling

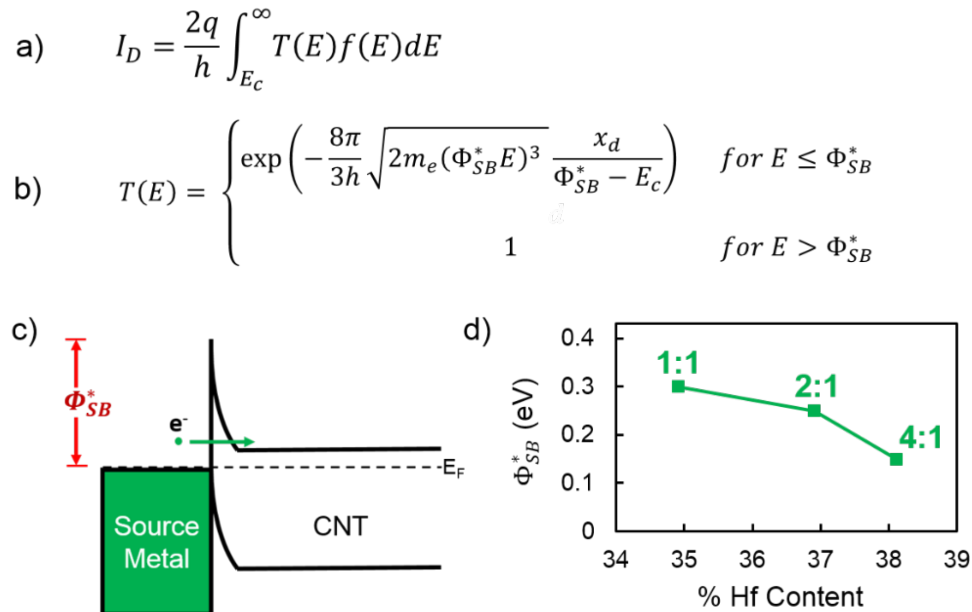


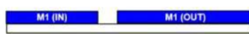
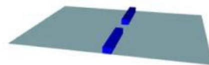
Figure A1.2.1: Effective Schottky Barrier Height. (a) Landauer formulation for calculating the currentdue to carrier transport across a potential barrier where *f*(E) is the Fermi-Dirac distribution and T(E) isthe transmission coefficient through the barrier. (b) WKB approximation of the probability of electrontransmission through a triangular Schottky barrier. We take the effective Schottky barrier height (Φ^{*}_{SB})as a fitting parameter to determine the appropriate effective Schottky barrier height for an experimentalCNFET. m_e is the effective tunneling mass for electrons, E_c is the conduction band which is modulated by the gate voltage, and x_d is the depletion width of the Schottky barrier. (c) Band diagram illustrating the effect of Φ^{*}_{SB} on the carrier transport from the source metal to CNT. (d) Plot relating Φ^{*}_{SB} to the hafnium content in HfO_X NDO films encapsulating NMOS CNFETs. NDO films with greater Hf content exhibit a lower Φ^{*}_{S}, reducing the barrier for electron transport and strengthening n-type conduction. Similar relations can be calibrated to other oxides besides HfO_X for the NDO layer.

Appendix A2: Extended Discussion onRV16X-NANO and the ManufacturingMethodology for CNTs

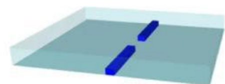
Appendix 2.1 RV16X-NANO Fabrication process

The fabrication process is shown in Fig. A2.1.1, and a final fabricated 150-mm wafer is shown inFig. A2.1.3. It uses five metal layers and over 100 individual processing steps.

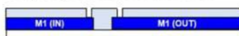
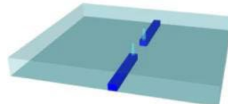
(a) M1 metal layer: for signal routing

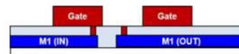
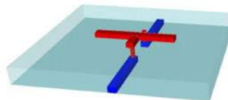
(b) Interlayer Dielectric (300 °C)



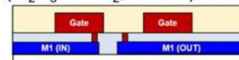
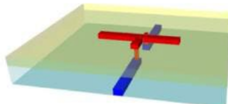
(c) Via definition (M1 to M2):
BCl_3/Cl_2 Reactive Ion Etch

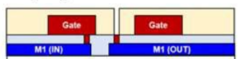
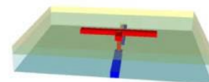
(d) M2 metal layer: for signal routing
+ local bottom gates

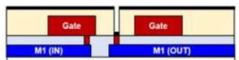
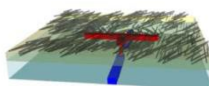
(e) Gate dielectric:
Atomic layer deposition (ALD):
(Al_2O_3 + HfO_2, 300 °C)

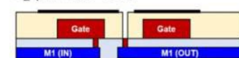
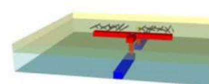
(f) Via definition (M2 to M3):
BCl_3/Cl_2 Reactive Ion Etch

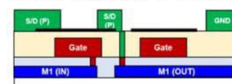
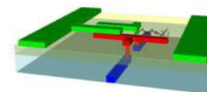
(g) CNT deposition:
~99.99% s-CNT solution

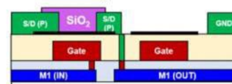
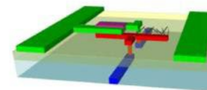
(h) Active Etch: remove CNTs outside CNFETs
O_2 plasma etch

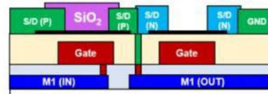
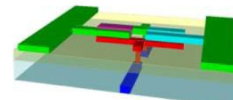
(i) M3 metal layer: for PMOS source/drain
0.6 nm Titanium / 85 nm Platinum

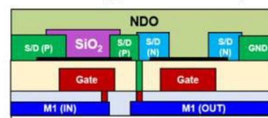
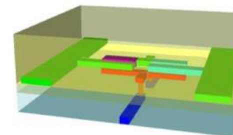
(j) PMOS passivation:
100 nm SiO_2

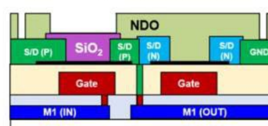
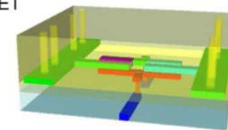
(k) M4 metal layer: NMOS source/drain
90 nm Titanium

(l) Nonstoichiometric doping oxide (NDO):
ALD HfO_X (20 nm, 200 °C)

(m) Via definition (M4 to M5):
+ remove NDO over PMOS CNFET

(n) M5 metal layer: power distribution

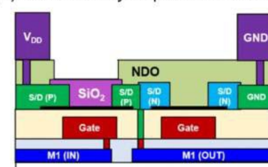
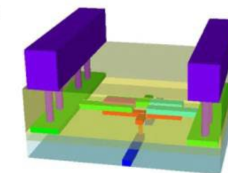



Figure A2.1.1 The fabrication process is a 5-metal-layer (M1 to M5) process and involves >100 individual process steps. s-CNT, semiconducting CNT; S/D, source/drain.

Bottom metal routing layers

The starting substrate is a 150-mm silicon wafer with 800-nm-thick thermal oxide for isolation. The bottom metal wire layers are defined using conventional processing (for example, lithographic patterning, metal deposition, etching, and so on). After the first metal layer is patterned (Fig. A2.1.1a),an oxide spacer (300 °C) is deposited to separate this first metal layer from the subsequent second metallayer (Fig. A2.1.1b). To produce interlayer vias between the first and second metal layer, vias are lithographically patterned and etched through this spacer dielectric using dry reactive ion etching (RIE)that stops on the bottom metal layer (Fig. A2.1.1c). The second metal layer is then defined lithographically and deposited. The vias are formed simultaneously with the second metal wire layer, because the vias are filled during the metal deposition (Fig. A2.1.1d). RV16X-NANO has two bottom metal layers, which are used for signal routing. The second metal layer also acts as the bottom gate forthe CNFETs

Bottom gate CNFETs

The second metal layer (Fig. A2.1.1d) provides both signal routing (local interconnect) as well as the bottom gate for the CNFETs. To fabricate the remaining bottom gate CNFET structure, a high-*k* (*k* is the dielectric constant) gate dielectric (a dual-stack of AlO_2 and HfO_2) is deposited through atomic layerdeposition (at 300 °C) over the bottom metal gates (Fig. A2.1.1e). The HfO_2 is used for the majority ofthe dielectric stack owing to its high-*k* dielectric constant, while the AlO_2 is used for its improved seeding and increased dielectric breakdown voltage. Following gate dielectric deposition, contact vias through the gate dielectric are patterned, and again RIE is used to etch the contact vias, stopping on thelocal bottom gates (Fig. A2.1.1f). These contact vias are used by the

top metal wiring to contact and route to the bottom gates and bottom metal routing layers. Post-etch, the surface is cleaned with both asolvent rinse as well as oxygen plasma, in preparation for the CNT deposition. Before CNT deposition,the surface is treated with hexamethyldisilazane, a common photoresist adhesion promoter, which improves the CNT deposition (both density and uniformity) over the high-*k* gate dielectric. The 150- mm wafer is then submerged in a toluene-based solution of purified CNTs (similar to the commercial Isosol-100 available from NanoIntegris; http://nanointegris.com/), containing approximately 99.99% semiconducting-CNTs. The amount of time the wafer incubates in the solution, as well as the concentration of the CNT solution, both affect the final CNT density; this process is optimized to achieve approximately 40–60 CNTs per linear micrometre (Fig. A2.1.1g). Immediately before CNT incubation, the CNT solution is diluted to the target concentration and is horn-sonicated briefly to maximize CNT suspension (importantly, some CNT aggregates will always remain). Post-CNT deposition, we perform the RINSE method (the first step of our MMC) to remove CNT aggregates thatdeposit on the wafer, leaving CNTs uniformly deposited across the 150-mm wafer. Importantly, RINSEdoes not degrade the remaining CNTs or remove the non-aggregated CNTs on the wafer (Fig. A2.7.1).After CNT incubation, we perform the CNT active etch in order to remove CNTs outside the active region of the CNFETs (that is, the channel region of the CNFETs). To do so, we lithographically patternthe active region of the CNFETs (protecting CNTs in these regions with photoresist), and etch all CNTsoutside these regions in oxygen plasma. The photoresist is then stripped in a solvent rinse, leaving CNTspatterned only in the intended locations (that is, in the channel regions of the CNFETs) on the wafer (Fig. A2.1.1h). We use solution-based CNTs here, but an alternative method for depositing CNTs on the substrate is aligned growth of CNTs on a crystalline substrate followed by transfer of the CNTs ontothe wafer used for circuit fabrication; both methods have shown the ability to achieve high-drive-currentCNFETs[5,17].

MIXED method for CNT CMOS

After the active etch of the CNTs (described in the paragraph above), the p-CNFET source and drain metal contacts are lithographically patterned and defined. We deposit the p-CNFET contacts (0.6-nm- thick titanium for adhesion followed by 85-nm-thick platinum) using electron-beam evaporation, and the contacts are patterned through a dual-layer lift-off process (Fig. A2.1.1i). This third metal layer actsas both the p-CNFET source contact and the p-CNFET drain contact, as well as the local interconnect.

After establishing the p-CNFET source and drain contacts, we passivate the p-CNFETs by depositing 100-nm-thick SiO_2 over only the p-CNFETs (Fig. A2.1.1j). Following p-CNFET passivation, the waferundergoes an oxide densification anneal in forming gas (dilute H_2 in N_2) at 250 °C for 5 min. This concludes the p-CNFET fabrication. To fabricate the n-CNFETs, the fourth metal layer (100-nm-thicktitanium, n-CNFET source and drain contacts) are defined (Fig. A2.1.1k, similar to the p-CNFET source and drain contact definition). For the electrostatic doping, nonstoichiometric HfO_x is deposited throughatomic-layer deposition at 200 °C uniformly over the wafer. Finally, we lithographically pattern and etch contact vias (Fig. A2.1.1m) through the HfO_x for metal contacts to the bottom metal layers, and then etch the HfO_x covering the p-CNFETs (the p-CNFETs are protected during this etch by the SiO_2 passivation oxide deposited previously). Additional experimental characterization of the MIXEDmethod (step two of our MMC) is shown in Fig. A2.8.1.

Back-end-of-line metal routing

Following the CNT CMOS fabrication, conventional back-end-of-line metallization is used to define additional metal layers over the CNFETs (for example, for power distribution and signal routing). As the metal layers below the CNFETs are primarily used for signal routing, we use the top (fifth) metal layer in the process for power distribution (Fig. A2.1.1n). Additional metal can

be deposited over the input/output pads for wire bonding and packaging. At the end of the process, the wafer undergoes a final anneal in forming gas at 325 °C. The finished wafer is diced into chips, and each chip can be packaged for testing or probed for standard cell library characterization.

This 3D physical architecture (with metal routing below and above the CNFETs) is uniquely enabled by the low-temperature processing of the CNFETs. The solution-based deposition of the CNTs decouples the high-temperature CNT synthesis from the wafer, enabling the entire CNFET to be fabricated with a maximum processing temperature below 325 °C. This enables metal layers and the gate stack to be fabricated before the CNFET fabrication takes place. This is in contrast to silicon CMOS, which requires high-temperature processing (for example, >1,000 °C) for steps such as doping activation annealing. This prohibits the fabrication of silicon CMOS over pre-fabricated metal wires, asthe high-temperature silicon CMOS processing would damage or destroy these bottom metal layers[35,36].

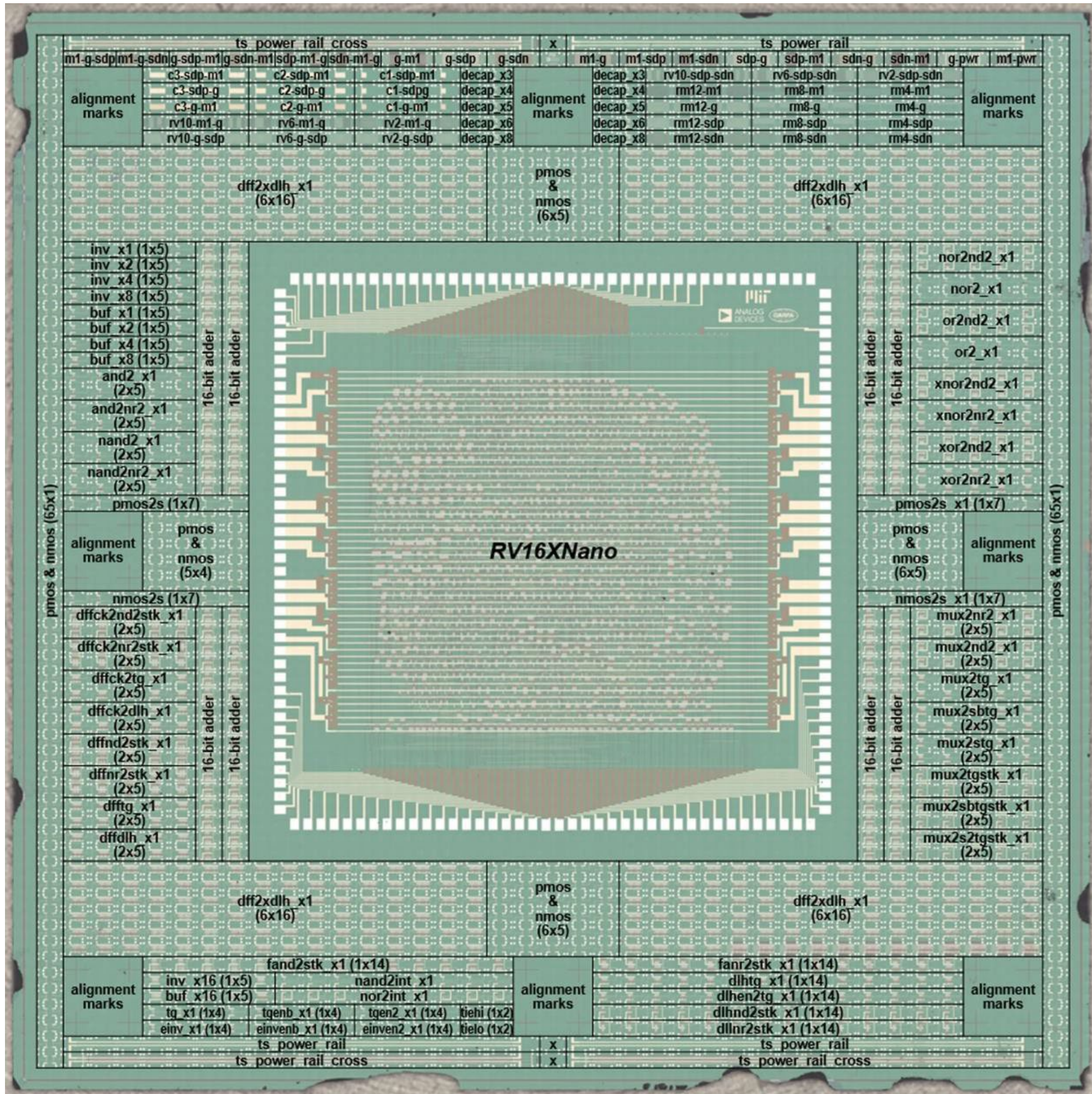


Figure A2.1.2: Microscopy image of a full fabricated RV16X-NANO die. The processor core is in themiddle of the die, with test circuitry surrounding the perimeter (when the RV16X-NANO is diced for packaging, these test structures are removed). The test structures include test structures for monitoringfabrication, as well as for measuring and characterizing all of the 63 standard cells in our standard celllibrary.

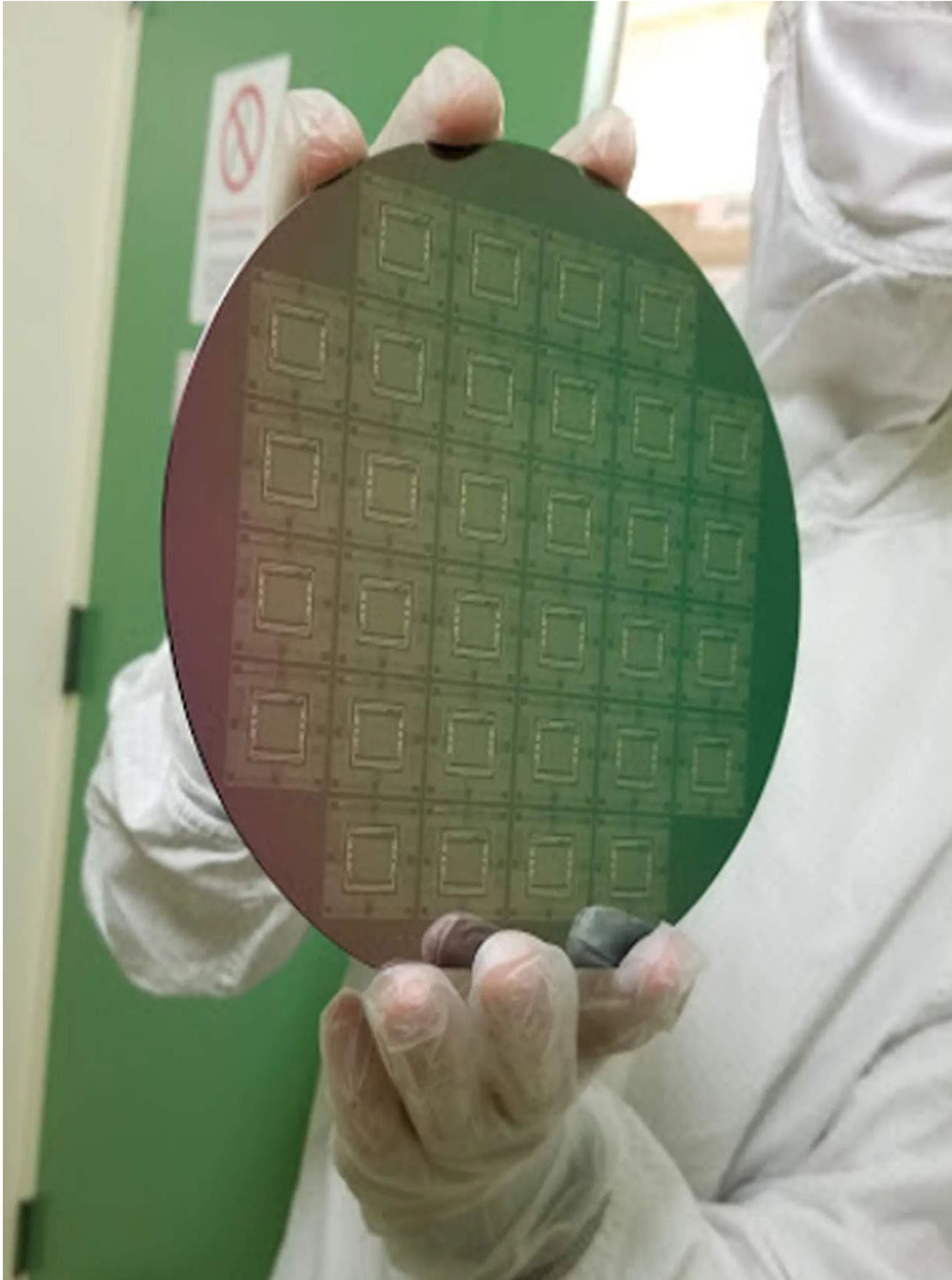


Figure A2.1.3: Image of a completed RV16X-NANO 150-mm wafer. Each wafer includes 32 dies.

Appendix 2.2 Experimental measurements of RV16X-NANO

A supply voltage (V_{DD}) of 1.8 V is chosen to maximize the noise resilience of the CNT CMOS digital logic, given the experimentally measured transfer characteristics of the fabricated CNFETs (noise resilience is quantified by the SNM metric (see main-text section 'DREAM'). To interface with each RV16X-NANO chip, we use a high channel count data acquisition system (120 channels) that offers amaximum clock frequency of 10 kHz while simultaneously sampling all channels. This limits the frequency we run RV16X-NANO at to 10 kHz, at which the power consumption is 969 μW (dominatedby leakage current). However, this is not the maximum clock speed of RV16X-NANO; during physical design, using an experimentally calibrated CNFET compact model and process design kit in an industry-practice VLSI design flow, the maximum reported clock frequency is 1.19 MHz, reported by Cadence Innovus following placement-and-routing of all logic gates. Future work may improve CNFET-level metrics (for example, improvements in contact resistance, gate stack engineering, CNT density and CNT alignment to increase CNFET on-current) to further speed up clock frequency.

Appendix 2.3 VLSI design methodology

The design flow of RV16X-NANO leverages only industry-standard tools and techniques. We have created a standard process design kit for CNFETs as well as a library of standard cells for CNFETs thatis compatible with existing EDA tools and infrastructure without modification. This enables us to leverage decades of existing EDA tools and infrastructure to design, implement, analyse and test arbitrary circuits using CNFETs, which is important to enable CNFET circuits to be widely adopted inthe mainstream. This is the first experimental demonstration of a complete process design kit and libraryfor an emerging beyond-silicon nanotechnology.

A high-level description of RISC-V implementation is written in Bluespec and then compiled into

a standard RTL hardware description language: Verilog. Bluespec enables testing of all instructions (listed in Extended Data Table 1) written in assembly code (for example, using the assembly language commands) to verify proper functionality of the RV16X-NANO. The functional tests for each instruction are also compiled into waveforms and tested on the RTL generated by Bluespec, they are verified using Verilator to verify proper functionality of the RTL (inputs and outputs are recorded and analysed as value change dump (.vcd) files). RTL descriptions of each module are shown in Fig. 3.2.

Next is the physical design of RV16X-NANO, including logic synthesis with a DREAM-enforcing standard cell library (see Methods section 'DREAM method implementation'), placement and routing,parasitic extraction, and design sign-off (that is, design rule check, layout versus schematic, verification of the final Graphic Database System, GDSII), as shown in Fig. 3.4. The RTL is synthesized into digitallogic gates using Cadence Genus, using the following components of the CNFET process design kit and standard cell library: the LIBERTY file (.lib) containing power/timing information for all standardlibrary cells, the cell macro library exchange format file (.macro.lef) containing abstract views of all standard library cells (for example, signal/power pin locations and routing blockage information), the technology library exchange format file (.tech.lef) containing metal routing layer information (for example, metal/via width/spacing), and the back-end-of-line parasitic information (.qrcTech file). To enforce DREAM, we use a subset of library cells in the standard cell library, including cells with inverter- and nand2-based logic stages (for combinational logic), and logic stages using tri-state inverters (for sequential logic), as well as fill cells (to connect power rails) and decap cells (to increasecapacitance between power rails V_{DD} and V_{SS}); specifically, these 23 cells comprise (see Fig. A2.5.1): and2_x1, buf_x1, buf_x2, buf_x4, buf_x8, decap_x3, decap_x4, decap_x5, decap_x6, decap_x8,dff2xdlh_x1, fand2stk_x1, inv_x1, inv_x2, inv_x4, inv_x8, inv_x16, mux2nd2_x1, nand2_x1, nor2nd2_x1, or2nd2_x1, xnor2nd2_x1 and xor2nd2_x1. During synthesis, all output pads are bufferedwith library cell buf_x8 to drive the

output pad so that no signal simultaneously drives an output pad aswell as another logic stage to prevent excessive capacitive loading in the core. Also, to minimize routing congestion in preparation for place-and-route, the register file (containing four registers, as described in Fig. 3.2) is directly synthesized from the Verilog hardware description language (instead of being designed 'by hand' or using a memory compiler) so that the D-flip-flops (dff2xdlh_x1: Fig. A2.5.1) comprising the state elements (registers) can be dispersed throughout the chip to lower the overall totalwire length. The final netlist is flattened so there is no hierarchy, and so logic can be optimized across module boundaries, and is then exported for place and route. Placement-and-routing is performed using Cadence Innovus, loading the synthesized netlist output fromCadence Genus. The core floorplan for standard library cells is defined as 6.912 mm × 6.912 mm. Given the standard cell library and logic gate counts from synthesis (and2_x1: 188, buf_x1: 3, buf_x8:82, buf_x16: 25, dff2xdlh_x1: 68, fand2stk_x1: 15, inv_x1: 75, inv_x2: 15, inv_x4: 10, inv_x8: 27, mux2nd2_x1: 189, nand2_x1: 625, nor2nd2_x1: 27, or2nd2_x1: 211, xnor2nd2_x1: 14 and xor2nd2_x1: 8), the resulting standard cell placement utilization is 40%. The pad ring for input/outputis defined as another cell with 160 pads: 40 on each side, with minimum width 170 μm and minimum spacing 80 μm, totalling pitch 250 μm. Inputs are primarily towards the top of the chip, outputs are primarily on the bottom, and power/ground (V_{DD}/V_{SS}) pads are on the sides (Fig. 3.1). 1. In addition to the core area, an additional boundary of 640 μm is permitted for signal routing around the core area (containing all standard library cells), for example, for relatively long global routing signals. Placementis performed while optimizing for uniform cell density and low routing congestion. The power grid is defined on top of the core area using the fifth metal layer (as shown in Fig. 3.1), while not consuming any additional routing resources within the metal layers for signal routing. The clock tree is implemented as a single high-fanout net loaded by all 68 D-flip-flops (for each of CLK and the invertedclock: CLKN), which is directly connected to an input pad, to minimize clock skew variations betweenregisters. All routing signals and vias are defined on a grid, with routing jogs enabled on each metal layer to enable optimization targeting

maximum spacing between adjacent metal traces. After this stageof routing, incremental placement is performed to further optimize congestion, and then filler cells anddecap cells are inserted to connect the power rails between adjacent library cells and to increase capacitance between V_{DD} and V_{SS} to improve signal integrity. After this incremental placement, the finalrouting takes place, reconnecting all the signals and routing to the pads, including detailed routing to fix all design rule check violations (for example, metal shorts and spacing violations). Finally, parasiticresistance and capacitances are extracted to finalize the power/timing analysis, and the final netlist is output to quantify the SNM for all pairs of connected logic stages. The GDSII is streamed out from Cadence Innovus and is imported into Cadence Virtuoso for final design rule check and layout versus schematic, using the standard verification rule format files with Mentor Graphics Calibre. The synthesized netlist is again used in the RTL functional simulation environment to verify proper functionality of all instructions, using Synopsys VCS, with waveforms for each test stored in a value change dump (.vcd) file. We note that these waveforms constitute the input waveforms to test the finalfabricated CNFET RV16X-NANO, as well as the expected waveforms output from the core, as shownin Fig. 3.3.

Once the GDSII for the core is complete, it is instantiated in a full die, which contains the core in the middle, alignment marks and test structures (including all standard library cells, CNFETs and test structures to extract wire/via parasitic resistance and capacitance) around the outside of the core as shown in Fig. A2.1.2. This die (2 cm × 2 cm) is then tiled onto a 150-mm wafer, each of which comprises 32 dies (6 × 6 array of dies minus 4 dies in the corners). Each layer in the GDS is flattened for the entire wafer and then released for fabrication.

DREAM method implementation

To implement DREAM:

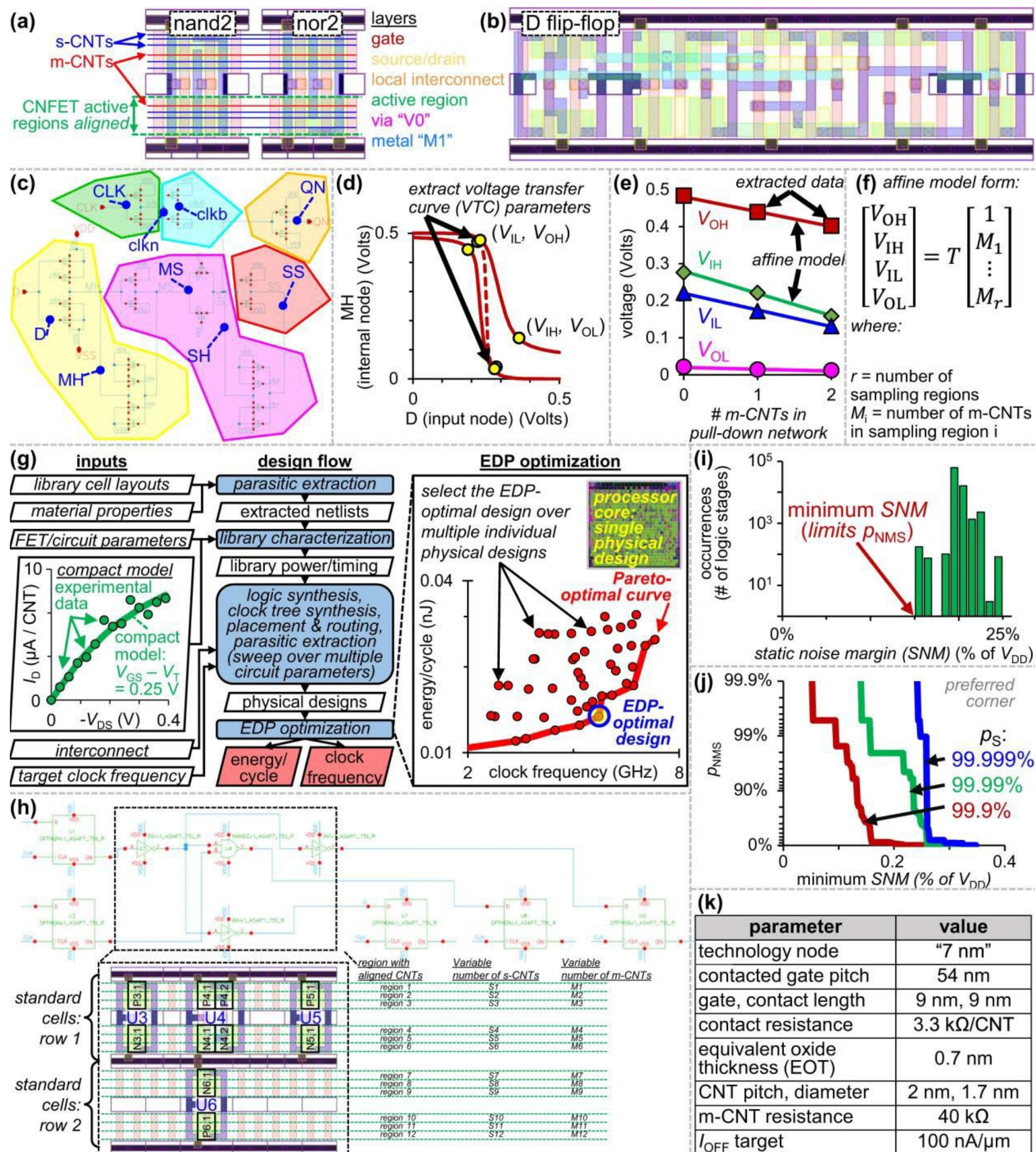
1) Generate the DREAM SNM table—for each pair of logic stages in the standard cell library, quantify the susceptibility of the pair to metallic CNTs as follows: use the variation-aware CNFET SNM model (Fig. A2.9.2) to compute SNM for all possible combinations of whether or not each CNFET comprises an metallic CNT (for example, in a (nand2, nor2) logic stage pair, there are 256 such combinations because there are 8 total CNFETs ($2^8 = 256$)). Record theminimum computed SNM in the DREAM SNM table (Fig. 3.6b, Fig. A2.9.2).

2) Determine prohibited logic stage pairs—choose an SNM cut-off value (SNM_C), such that alllogic stage pairs whose SNM in the DREAM SNM table is less than SNM_C are prohibited during physical design (see example in Fig. 3.6b: green entries satisfy SNM_C whereas red entries prohibited cascaded logic gate pairs). The method of choosing SNM_C is described below.

3) Physical design—use industry-practice design flows and EDA tools to implement VLSI circuits without using the prohibited logic stage pairs. Ideally, EDA tools will enable designersto set which logic stage pairs to prohibit during power/timing/area optimization, but this is currently not a supported feature. To demonstrate DREAM in this work, we create a DREAM-enforcing library that comprises a subset of library cells such that no possible combination of cells can be connected to form a prohibited logic stage pair.

To choose SNM_C, we use a bisection search. A larger SNM_C prohibits more logic stage pairs, resultingin better p_{NMS} with higher energy/delay/area cost (and vice versa). To satisfy target p_{NMS} constraints (forexample, $p_{NMS} \geq 99\%$), while minimizing cost, we optimize SNM_C as follows. Step 1: Initialize a lowerbound L and upper bound U for SNM_C. $L = 0$, and U is the maximum value of SNM_C that enables EDAtools to synthesize arbitrary logic functions (for example, prohibiting all logic stage pairs except (inv, inv) would be insufficient). Step 2: Find p_{NMS} using $SNM_C = (L$

+ U)/2, using the design flow inFig. A2.3.1. Record the set of prohibited logic stage pairs, as well as the circuit physical design, p_{NMS}, energy, delay and area. Step 3: If p_{NMS} satisfies the target constraint (for example, $p_{NMS} \geq 99\%$), set $U = SNM_C$. Otherwise set $L = SNM_C$. Step 4: Set $SNM_C = (L + U)/2$. If p_{NMS} has already been analysed for the resulting set of prohibited logic stage pairs, terminate. Otherwise, return to step 2.



parameter	value
technology node	"7 nm"
contacted gate pitch	54 nm
gate, contact length	9 nm, 9 nm
contact resistance	3.3 kΩ/CNT
equivalent oxide thickness (EOT)	0.7 nm
CNT pitch, diameter	2 nm, 1.7 nm
m-CNT resistance	40 kΩ
I_{OFF} target	100 nA/µm

Figure A2.3.1: DREAM implementation and methodology. a) Standard cell layouts (derived using the'asap7sc7p5t' standard cell library37), illustrating the importance of CNT correlation: because the length of CNTs (which can be of the order of hundreds of micrometres) is typically much longer compared with the CNFET contacted gate pitch (CGP, for example about 42–54 nm for a 7-nm node37), the number of s-CNTs and m-CNTs in CNFETs can be uncorrelated or highly correlated depending on the relative physical placement of CNFET active regions38. For many CMOS standard cell libraries at sub-10-nm nodes (for example refs 37,39), the active regions of

FETs are highly aligned,resulting in highly correlated number of m-CNTs among CNFETs in library cells, further degrading VTCs (because one m-CNT can affect multiple CNFETs simultaneously). **b**–**f**) Generating a variation-aware CNFET SNM model, shown for a D-flip-flop (dff) derived from the asap7sc7p5t standard cell library37. **b**) Layout used to extract netlists for each logic stage. **c**, Schematic: CNFETs are grouped bylogic stage (with nodes arbitrarily labelled 'D', 'MH', 'MS', 'SH', 'SS', 'CLK', 'clkn', 'clkb' and 'QN'for ease of reference). **d**) For each extracted netlist, there can be multiple VTCs: for each logic stage output, a logic stage input is sensitized if the output state (0 or 1) depends on the state of that input (given the states of all the other inputs). For example, for a logic stage with Boolean function: Y = !(A*B+C), C is sensitized when (A, B) = (0, 0), (0, 1) or (1, 0). We simulate all possible VTCs (over all logic stage outputs and sensitized inputs), and also in the presence of m-CNTs. For example,panel **d** shows a subset of the VTCs for the logic stage in panel **b** with output node 'MH' (labelled in panel **c**), and sensitized input 'D' (with labelled nodes ('clkb', 'clkn', 'MS') = (0, 1, 0)). The dashed line indicates VTC with no m-CNTs, and the solid lines are example VTCs in the presence of m-CNTs(including the effect of CNT correlation). In each case, we model V_{OH}, V_{IH}, V_{IL} and V_{OL} as affine functions of the number of m-CNTs (M_i) in each of r regions (M_1, ..., M_r), with calibration parameters in the static noise margin (SNM) model matrix T (shown in panel **f**). **e**) Example calibration of the SNMmodel matrix T for the VTC parameters extracted in panel **d**; the symbols are VTC parameters extractedfrom circuit simulations (using Cadence Spectre), and solid lines are the calibrated model. **f)** Affine model form. **g**–**j**) VLSI design and analysis methodology. **g**) Industry-practice physical design flow tooptimize energy and delay of CNFET digital VLSI circuits, including: (1) library power/timing characterization (using Cadence Liberate) across multiple V_{DD} and using parasitics extracted from standard cell layouts (derived from the asap7sc7p5t standard cell library), in conjunction with a CNFETcompact model8. (2) Synthesis (using Cadence Genus), place-and-route (using Cadence Innovus) withback-end-of-line (BEOL) wire parasitics from the ASAP7 process design kit (PDK). (3) Circuit EDP optimization: we sweep both V_{DD} and target clock frequency (during synthesis/place-and-route) to create multiple physical designs. The one with best EDP is used to compare design options (for example,DREAM versus baseline). **h**) Subset of logic gates in an example circuit module, showing the effect ofCNT correlation at the circuit level (for example, the m-CNT counts of CNFETs P3,1 and P5,1 are both equal to $M_1 + M_2 + M_3$)40. **i**) Distribution of SNM over all connected logic stage pairs, for a single sample of the circuit m-CNT counts. The minimum SNM for each trial limits the probability that all noise margin constraints in the circuit are satisfied (p_{NMS}). **j**) Cumulative distribution of minimum SNMover 10,000 Monte Carlo trials, shown for multiple target p_S values, where p_S is the probability that a given CNT is a semiconducting CNT. These results are used to find p_{NMS} versus p_S for a target SNM requirement (SNM_R), where p_{NMS} is the fraction of trials that meet the SNM requirement for all logic stage pairs. We note that p_{NMS} can then be exponentiated to adjust for various circuit sizes based on thenumber of logic gates. **k**) CNFET compact model parameters (for example, 7-nm node).

For all physical designs recorded in step 2 we choose the physical design that satisfies the target pNMS constraint with minimum energy/delay/area cost. Importantly, the cost of implementing DREAM is ≤10% energy, ≤10% delay and ≤20% area. To integrate DREAM within EDA tools— enabling pNMS optimization simultaneously with power/timing/area optimization— is a goal for future work on improving p_S versus power/timing/area trade-offs. The effect that the

remaining metallic CNTs have on EDP is shown in Extended Data Fig. A2.9.1.

Appendix 2.4 Comparing RV16X-NANO with prior works on CNFET circuits

A detailed summary and comparison with prior work is given below and in Supplemental Table 1. In 2013, progress in the field of CNTs resulted in the first miniature CNT computer. While an important milestone for the technology, there were major and fundamental disconnects between that work and a modern microprocessor today. All FETs were PMOS (it did not use energy-efficient CMOS logic), andit was limited to <60 logic gates totaling 178 CNFETs. Moreover, operationally, it only operated on a single bit of data, and could only execute a signal instruction (the SUBNEG instruction, and thus avoided all decoding and MUX operations). While limited, this work did demonstrate key advances forthe field, such as a complete digital system integrating both combinational logic as well as sequential logic. In stark contrast, this work demonstrates a processor based off of the modern RISC-V processor which is already gaining acceptance in commercial products. The side-by-side comparison of these twoworks is shown below:

Supplemental Table 1		
	Prior CNT miniature computer	This work
Gate count	<60	4,000
Transistor Count	178	14,000
Logic family	PMOS-only	Full CMOS
Design flow	manual	Industry-standard design flow
# of bits in data path	1	16
# of instructions	1 (SUBNEG)	31 (RV32-I)
# of bits in instruction	10-bit	32-bit

More recently, the largest system fabricated from CNFETs was demonstrated in 2017. This is a three- dimensional (3D) nanosystem, integrating vertical layers of logic, memory, and sensing, and was another important demonstration (illustrating the new monolithic 3D systems enabled by

CNTs). However, while this system contained >2 million CNFETs, the vast majority of these CNFETs were used as gas sensors (e.g., not for logic, which are a completely different technology with completely different - *and substantially relaxed* - constraints). Moreover, similar to the prior miniature CNT computer discussed above, it used PMOS-only only and was not a complete system (e.g., the 3D nanosystem only performed sensing and computing, all control flow was performed off-chip with an external computer).

While prior works have demonstrated CNFET CMOS, no complete CNFET CMOS digital system hasever been fabricated. The most complex CNFET CMOS demonstration resulted in a 4-bit adder, comprising of 132 CNFETs. Our manufacturing methodology for CNTs is essential for transforming CNFET CMOS from small-scale demonstrations to complex digital systems such as our RV16X- NANO (RV16X-NANO actually also contains a 16-bit adder within its design within the execute unit,Figure 3.2).

work	description	Type of logic	# of gates/ # o FETs	Additional points
THIS WORK	RV16X-NANO	Full CMOS	4000 gates/ 14,000 CMOS CNFETs	See manuscript for details.
[1]	first single-bit, single instruction CNT miniature computer	PMOS	<60 gates/ 178 CNFETs	
[2]	3D sensing chip	PMOS	2 million p-CNFET ***gas sensors***	Used as gas sensors, not as cascaded logic. All p-CNFETs, no CMOS.
[3]	Hyper-dimensional chip	PMOS	1932 p-CNFETs	78%% stuck-at faults (faulty logic)

[4]	Sensor interface circuit	PMOS	20 gates/ 45 p-CNFETs	
[5]	4-bit full adder	CMOS (pass-gate logic)	132 CNFETs	Pass-gate logic
[6]	inverter	CMOS	2	
[7]	SRAM cell	CMOS	6	Not solid state, no yield reported.
[8]	Ring oscillator	CMOS	12	34% yield

[1] Shulaker, M.M., Hills, G., Patil, N., Wei, H., Chen, H.Y., Wong, H.S.P. and Mitra, S., 2013. Carbonnanotube computer. *Nature*, *501*(7468), p.526.

[2] Shulaker, M.M., Hills, G., Park, R.S., Howe, R.T., Saraswat, K., Wong, H.S.P. and Mitra, S., 2017.Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature*, *547*(7661), p.74.

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Appendix 2.5 CNFET Standard Cell Library

As part of the CNFET PDK, parameterized cells (Pcells) are created using Cadence Virtuoso® for bothNMOS and PMOS CNFETs, with the following open access (OA) layers: CNFET gate, goxcut (via between CNFET gate and source/drain), active, sdp (PMOS source/drain), sdn (NMOS source/drain). CNFET Pcells offer the following user-controlled component description format (CDF) parameters, which are both provided as inputs by the designer, and extracted using layout vs. schematic (LVS) rules: CNFET width, physical gate length, channel length, gate underlap, source/drain/gate extension width over the horizontal edge of the CNT active region, and source/drain extension length over the vertical edge of the CNT active region. These CDF parameters are also automatically checked using DRC, alongwith other design rules such as minimum spacing between CNT active region and goxcut via (connecting layers: gate and sdp). CNFET devices extracted using LVS (using Standard Rule Verification Format (SVRF) compatible with Mentor Graphics Calibre® integrated within Cadence Virtuoso®) instantiate CNFETs using the widely-used virtual source FET model calibrated to experimentally measured data from CNFETs (compact model written in Verilog-A).

The CNFET Pcell is used in conjunction with other OA layers in the PDK (e.g., m1 = metal routing layer, v1g = via between m1 and CNFET gate, v_sd_m5 = via between nmos source/drain and metal 5power distribution) to create 63 cells in the standard library cell; images, layouts, schematics, and experimentally measured waveforms for each standard cell are shown in Figure A2.5.1. To facilitate automated and compact placement and routing, standard cells are designed with the convention of having standard cell height equal to 16 metal tracks, including one shared power rail (VDD) and one shared ground (VSS) rail (shared between vertically adjacent rows of

standard cells), and some cells are “double height cells” comprising 32 metal tracks and conforming to the same conventional site- based placement method used by placement-and-routing tools (e.g., Synopsys IC Compiler® and Cadence Innovus®). Standard library cells also conform to conventional CMOS-based layout styles with PMOS FETs aligned horizontally (e.g., on the top half of the layout towards the VDD rail) and NMOS FETs aligned horizontally (e.g., on the bottom half of the layout toward the VSS rail). Of the 16 metal tracks for standard cells, 3 are used for power rails, 3 are used for each of NMOS and PMOS CNFET width, and 7 are used for signal routing (2 tracks between PMOS and VDD, 2 tracks between NMOS and VSS, and 3 tracks between NMOS and PMOS), creating routing resources for local interconnects (e.g., within standard cells and between standard cells), and for global signal routing (forplace-and-route tools).

library cell (63)	description
and2_x1	2-input AND
and2nr2_x1	2-input AND (comprising nor2/inv logic stages)
buf_x1	buffer, drive strength 1x
buf_x2	buffer, drive strength 2x
buf_x4	buffer, drive strength 4x
buf_x8	buffer, drive strength 8x
buf_x16	buffer, drive strength 16x
decap_x3	capacitance between power rails, size 1x
decap_x4	capacitance between power rails, size 2x
decap_x5	capacitance between power rails, size 4x
decap_x6	capacitance between power rails, size 8x
decap_x8	capacitance between power rails, size 16x
dff2xdlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), input separate clocks for master/slave
dffck2dlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), input clock and inverted clock
dffck2nd2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), input clock and inverted clock, 2x cell height
dffck2nr2stk_x1	positive edge-triggered D-flip-flop (comprising nor2/inv logic stages), input clock and inverted clock, 2x cell height
dffck2tg_x1	positive edge-triggered D-flip-flop (comprising D-latch and transmission gate), input clock and inverted clock
dffdlh_x1	positive edge-triggered D-flip-flop (comprising 2x D-latches), inverted clock generated locally
dffnd2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), 2x cell height
dffnr2stk_x1	positive edge-triggered D-flip-flop (comprising nand2/inv logic stages), 2x cell height
dfftg_x1	positive edge-triggered D-flip-flop (comprising D-latch and transmission gate), inverted clock generated internally
dlhen2tg_x1	high-enable D-latch (comprising transmission gates), input enable and inverted enable
dlhnd2stk_x1	high-enable D-latch (comprising nand2/inv logic stages)
dlhtg_x1	high-enable D-latch (comprising transmission gates), inverted enable generated internally
dllnr2stk_x1	high-enable D-latch (comprising nor2/inv logic stages)
einv_x1	tri-state inverter, inverted enable generated internally
einven2_x1	tri-state inverter, input enable and inverted enable
einvenb_x1	tri-state inverter, enable (and inverted enable) buffered internally
fand2stk_x1	full-adder (comprising nand2/inv logic stages)
fanr2stk_x1	full-adder (comprising nor2/inv logic stages)
fill_x1	fill cell (extends power rails), size 1x
fill_x2	fill cell (extends power rails), size 2x
fill_x4	fill cell (extends power rails), size 4x
fill_x8	fill cell (extends power rails), size 8x
fill_x16	fill cell (extends power rails), size 16x
inv_x1	inverter, drive strength 1x
inv_x2	inverter, drive strength 2x
inv_x4	inverter, drive strength 4x
inv_x8	inverter, drive strength 8x
inv_x16	inverter, drive strength 16x
mux2nd2_x1	2-input multiplexer (comprising nand2/inv logic stages)
mux2nr2_x1	2-input multiplexer (comprising nor2/inv logic stages)
mux2s2tg_x1	2-input multiplexer (comprising transmission gates), input select and inverted select
mux2s2tgstk_x1	2-input multiplexer (comprising transmission gates), input selected and inverted select, 2x cell height
mux2sbtg_x1	2-input multiplexer (comprising transmission gates), select (and inverted select) buffered internally
mux2sbtgstk_x1	2-input multiplexer (comprising transmission gates), select (and inverted select) buffered internally, 2x cell height
mux2tg_x1	2-input multiplexer (comprising transmission gates), inverted select generated internally
mux2tgstk_x1	2-input multiplexer (comprising transmission gates), inverted select generated internally, 2x cell height
nand2_x1	2-input NOT-AND
nand2nr2_x1	2-input NOT-AND (comprising nor2/inv logic stages)
nor2_x1	2-input NOT-OR
nor2nd2_x1	2-input NOT-OR (comprising nand2/inv logic stages)
or2_x1	2-input OR
or2nd2_x1	2-input OR (comprising nand2/inv logic stages)
tg_x1	transmission gate, inverted enable generated internally
tgen2_x1	transmission gate, input enable and inverted enable
tgenb_x1	transmission gate, enable (and inverted enable) buffered internally
tiehi_x2	output is tied high (to VDD)
tielo_x2	output is tied low (to VSS)
xnor2nd2_x1	2-input EXCLUSIVE-NOT-OR (comprising nand2/inv logic stages)
xnor2nr2_x1	2-input EXCLUSIVE-NOT-OR (comprising nor2/inv logic stages)
xor2nd2_x1	2-input EXCLUSIVE-OR (comprising nand2/inv logic stages)
xor2nr2_x1	2-input EXCLUSIVE-OR (comprising nor2/inv logic stages)

library cell (63)	optical image	layout	schematic	experimental waveform
inv_x1 • CNFETs: 2				
inv_x2 • CNFETs: 4				
inv_x4 • CNFETs: 8				
inv_x8 • CNFETs: 16				
inv_x16 • CNFETs: 32				
mux2nd2_x1 • CNFETs: 14				
mux2nr2_x1 • CNFETs: 14				
mux2s2tg_x1 • CNFETs: 10				
mux2s2tgstk_x1 • CNFETs: 10				
mux2sbtg_x1 • CNFETs: 14				
tgen2_x1 • CNFETs: 2				see caption
tgenb_x1 • CNFETs: 6				see caption
tiehi_x2 • CNFETs: 3				see caption

library cell (63)	optical image	layout	schematic	experimental waveform
and2_x1 • CNFETs: 6				
and2nr2_x1 • CNFETs: 10				
buf_x1 • CNFETs: 4				
buf_x2 • CNFETs: 6				
buf_x4 • CNFETs: 10				
buf_x8 • CNFETs: 20				
buf_x16 • CNFETs: 40				
decap_x3 • CNFETs: 2				see caption
decap_x4 • CNFETs: 4				see caption
decap_x5 • CNFETs: 6				see caption
tielo_x2 • CNFETs: 3				see caption
xnor2nd2_x1 • CNFETs: 18				
xnor2nr2_x1 • CNFETs: 16				

library cell (63)	optical image	layout	schematic	experimental waveform
decap_x6 • CNFETs: 8				see caption
decap_x8 • CNFETs: 12				see caption
dff2xdlh_x1 • CNFETs: 32				
dffck2dlh_x1 • CNFETs: 22				
dffck2nd2stk_x1 • CNFETs: 34				
dffck2nr2stk_x1 • CNFETs: 34				
dffck2tg_x1 • CNFETs: 20				
dffdlh_x1 • CNFETs: 26				
dffnd2stk_x1 • CNFETs: 38				
dffnr2stk_x1 • CNFETs: 38				
dfftg_x1 • CNFETs: 24				
dlhen2tg_x1 • CNFETs: 12				
dlhnd2stk_x1 • CNFETs: 18				
dlhtg_x1 • CNFETs: 16				
dllnr2stk_x1 • CNFETs: 18				
einv_x1 • CNFETs: 6				
einven2_x1 • CNFETs: 4				
einvenb_x1 • CNFETs: 8				
fand2stk_x1 • CNFETs: 36				
fanr2stk_x1 • CNFETs: 36				
mux2sbtgstk_x1 • CNFETs: 14				
mux2tg_x1 • CNFETs: 12				
mux2tgstk_x1 • CNFETs: 12				
nand2_x1 • CNFETs: 4				
nand2nr2_x1 • CNFETs: 10				
nor2_x1 • CNFETs: 4				
nor2nd2_x1 • CNFETs: 10				
or2_x1 • CNFETs: 6				
or2nd2_x1 • CNFETs: 8				
tg_x1 • CNFETs: 4				see caption
xor2nd2_x1 • CNFETs: 16				
xor2nr2_x1 • CNFETs: 18				

Figure A2.5.1: CNFET standard cell library. List of all of the standard cells comprising our standard cell library, along with a microscopy image of each fabricated standard cell, the schematic of each cell, and a typical measured waveform from each fabricated cell. As expected for static CMOS logic stages, the CNFET logic stages exhibit output voltage swing exceeding 99% of V_{DD}, and achieve gain

of >15. Experimental waveforms are not shown for cells whose functionality is not demonstrated by output voltage as a function of either input voltage or time; for example, for cells without outputs (forexample, fill cells: cell names that start with ‘fill_’ or decap cells: cell names that start with ‘decap_’),for cells whose output is constant (tied high/low: cell names that start with ‘tie_’), or for transmission gates (cell names that start with ‘tg_’).

Layouts for each cell are shown in Figure A2.5.1, as well as schematics for each standard cell that are automatically extracted using LVS (and verified against drawn schematics in virtuoso). These netlists are then used in conjunction with Cadence Liberate for library power/timing characterization, e.g., to compute rise/fall delay/output slew rate/energy consumption as functions of output load capacitance and input slew rate. Additional metrics quantified by Liberate are cell leakage power and timing constraint tables for sequential logic (e.g., setup time, hold time, minimum clock pulse width). The results are written to standard file formats (LIBERTY file: .lib) for synthesis & place-and-route. In addition to .lib files, layout exchange format (.lef) files (defining abstracted standard cell views for place and route, including pin locations, power rail locations, and blockage information) are created using Cadence Abstract®. These .lib and .lef files for standard library cells are then used for synthesis& place and route, in conjuction with other technology files in the PDK (.lef for technology layers, e.g.,defining layers and rules for metal routing, and .ict/.qrcTech files defining parasitic information between technology layers), as described in Section X below.

To experimentally characterize and calibrate the standard cell library, we fabricate each of the standardcells alongside the RV16X-NANO. As shown in Figure A2.1.2, each die contains the RV16X-NANO processor core in its center, surrounded by test circuitry on the perimeter. For packaging, these test structures are removed during dicing to isolate the RV16X-NANO processor core. The test circuitry contains both test structures for process monitoring throughout the >100 fabrication process steps utilized for RV16X-NANO, but also contains all of the standard cells. Figure A2.5.1 shows images, schematics, and measurements for each of the standard cells in the

library, illustrating correct functionality, rail-to-rail swing (>99% V_{DD} swing on average), and high gain (>15, limited by the step size in our measurement).

Appendix 2.6 RISC-V: Operational Details

The RV16X-Nano Processor is implemented as a finite state machine (FSM) with 3 different states: INST FETCH (when it is requesting an instruction from memory), EXECUTE (when it is executing aninstruction), and LOAD FINISH (when it is loading data from memory). It comes out of reset initializedin INST FETCH, with the program counter set to 0, and so it fetches the instruction from address 0 in the memory and advances to the EXECUTE state. Adhering to RISC-V specification, the 32-bit instruction is one of 4 base instruction types (R-type, I-type, S-type, or U-type) with 5 immediate variations within the instruction (I-immediate, U-immediate, S-immediate, B-immediate, J-immediate),forming 6 possible instruction formats (type-immediate): R, I-I, I-U, S-B, S-S, U-J: see Table X for bit-level descriptions of these instructions. The instruction is decoded as one of these formats in the "decode" block (Figure A2.5.1), which then access to the register file (e.g., which registers to read) andprovides inputs the execute block. These inputs include: 16-bit values read from the register file, immediate values decoded from the instruction, the current value of the program counter, and control signals to select instructions from the sub-blocks including: add, shift, bitwise-and, bitwise-or, bitwise-xor, less than comparison, equal comparison. The outputs of these control blocks determine which values to write back into registers (e.g., for arithmetic operation such as add/subtract), and values to write back into memory. The execute block also computes the next value of the program counter, e.g.,based on either incrementing (next pc = pc + 4) or otherwise for conditional branch or unconditional jump. After the instruction is executed (during state EXECUTE), the processor returns to either state INST FETCH (for requesting the next instruction), or LOAD FINISH (to load a data word from memory). This mode of operation continues during full execution of programs and adheres to the specification in riscv.org according to RV32E specification, but a reduced number of registers (4

insteadof 16) and with 16-bit data words instead of 32-bit data words (all registers in the register file are 16- bit instead of 32-bit), though instructions remain 32-bits. A full list of all instructions is in Figure A2.5.1,which is the full list for the RV32E in the RISC-V specification. To adjust RV32E to 16-bit, the instruction length remains 32 bits, and all data operations are performed on 16-bit values instead of 32-bit values, by truncating the upper-32 bits.

Appendix 2.7 RINSE Characterization

In addition to demonstrating the ability for RINSE to reduce CNT aggregate defect density by >250×, we further characterize RINSE to show that the RINSE process does not negatively impact CNFET performance. As shown in Figure A2.7.1, scanning electron microscopy (SEM) images of CNT deposition pre- and post-RINSE show negligible change in the CNT density. Therefore, RINSE does not remove CNTs from the wafer surface, even after >60 minutes of performing RINSE sonication. Moreover, CNFETs fabricated on samples that have and have not undergone RINSE exhibit minimal change in electrical characteristics (Figure A2.7.1c, note minimal change in the I_D-V_{GS} for a set of CNFETs). Importantly, not only does RINSE not impact the PMOS CNFETs, the CNFETs can still undergo the MIXED doping process (including the electrostatic doping oxide) to realize NMOS CNFETs (Figure A2.7.1d).

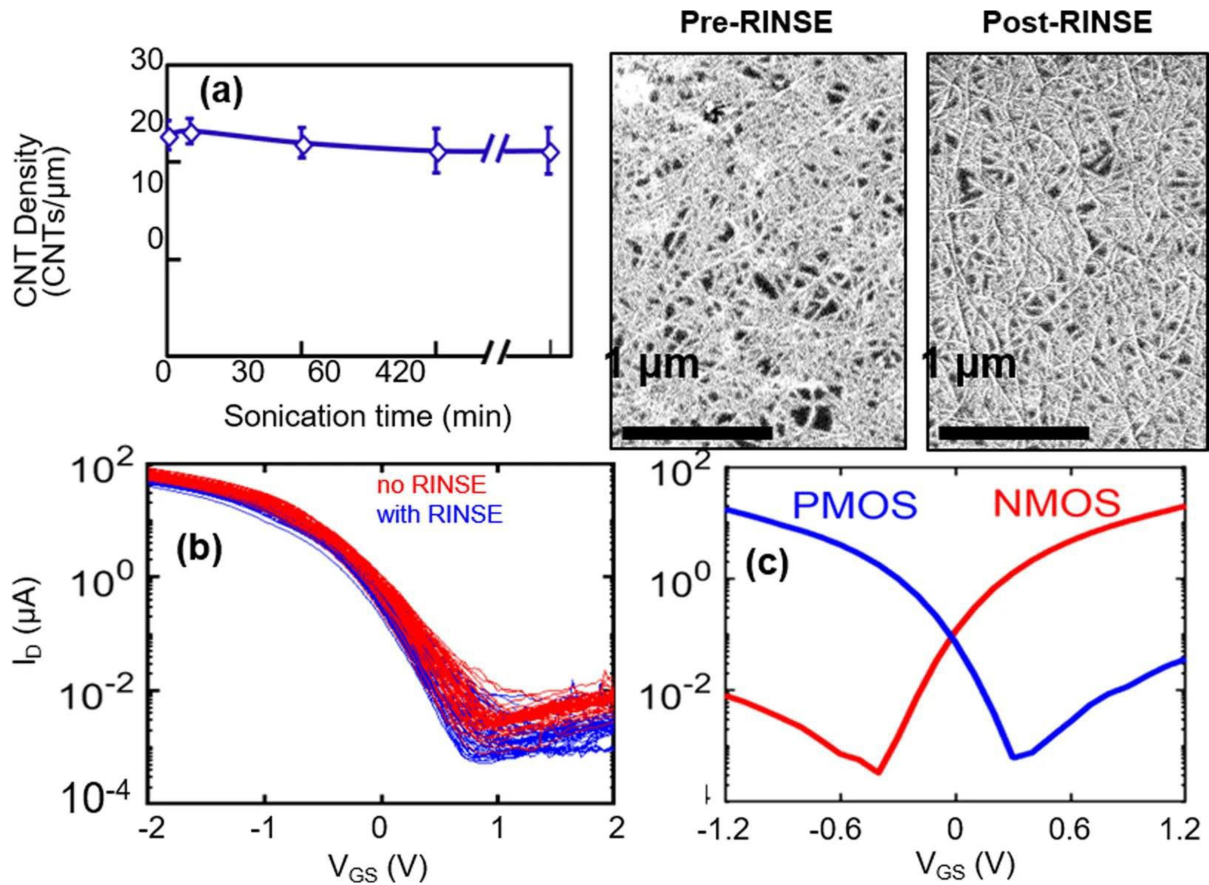

Figure A2.7.1: **a**) CNT density is the same pre- versus post-RINSE. **b)** CNFET I_D–V_{GS} exhibit minimalchange for sets of CNFETs fabricated with and without RINSE ($V_{DS} = -1.8$ V for all measurements shown). Both samples came from the same wafer, which was diced after the CNT deposition but before the RINSE process. One sample underwent RINSE while the other sample did not. **c**) CNFETs can stillbe doped NMOS after the RINSE process, leveraging our MIXED process ($V_{DS} = -1.2$ V for all measurements shown).

Appendix 2.8 MIXED Characterization

Figure A2.8.1 provides additional characterization of the MIXED CNFET CMOS process, realizing the first demonstration of large-area (150 mm substrates), uniform, and high-yield CNFET CMOS logic.

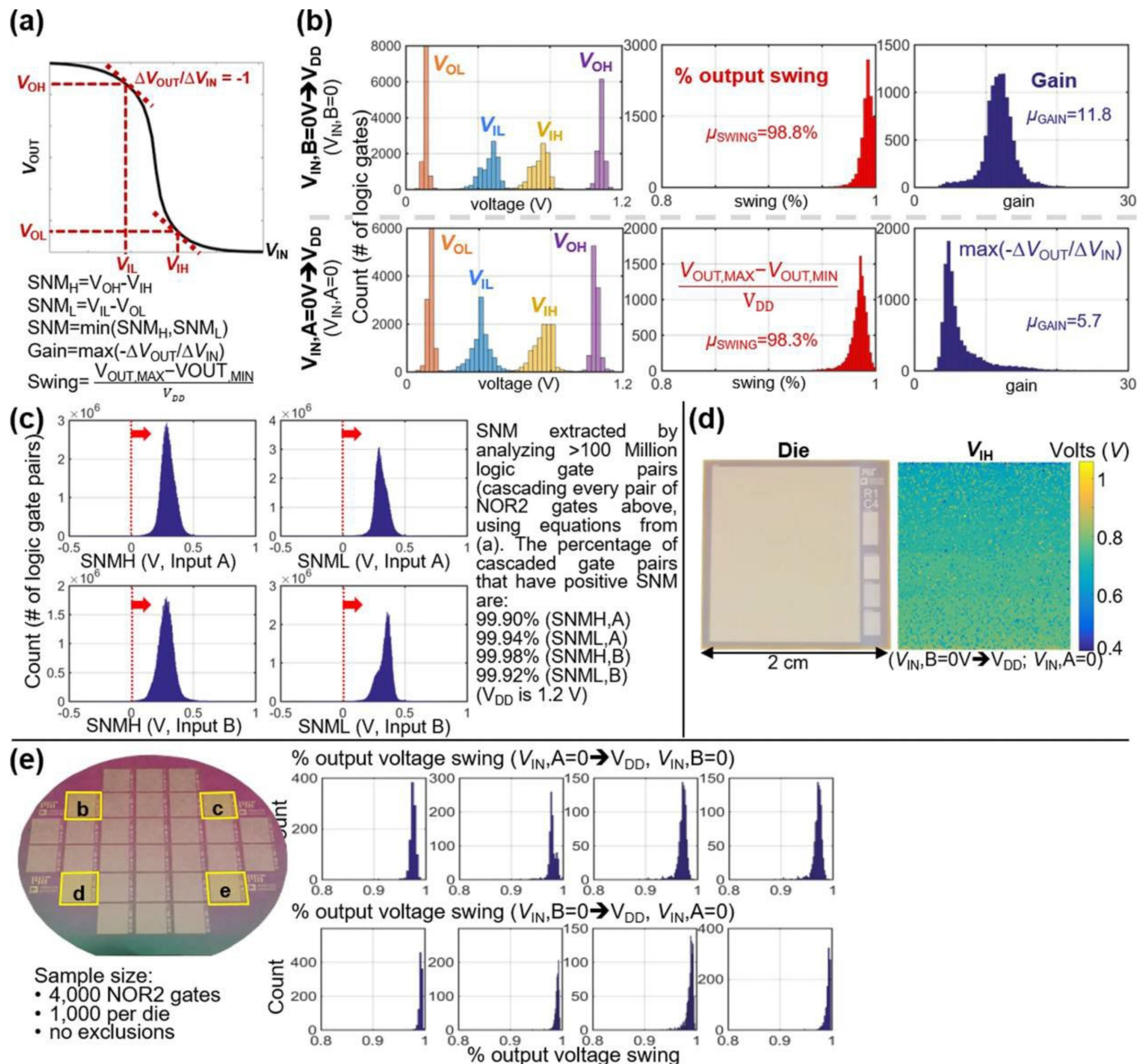

Figure A2.8.1: MIXED CNFET CMOS characterization. **a**, Definitions of key metrics for characterizing logic gates, including SNM, gain and swing. V_{OH}, V_{IH}, V_{IL} and V_{IL} (labelled on the VTCs in **a**, where (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) are the points on the VTC where $\Delta V_{OUT}/\Delta V_{IN} = -1$) are usedto extract the noise margin: SNM = min(SNM_H, SNM_L). **b**, Key metrics extracted for the 10,400 CNFET CMOS nor2 logic gates measured in Fig. 3.5 (metrics defined in **a**). This is the

largest CNT CMOS demonstration to date, to our knowledge. V_{DD} is 1.2 V. **c**, SNM is extracted based on the distributions from **b**. We analyse >100 million logic gate pairs based on these experimental results. **d**, Spatial dependence of V_{IH} (as an example parameter to compute SNM). Each pixel represents the V_{IH} ofthe nor2 at that location in the die. Importantly, V_{IH} increases across the die (from top to bottom). The change in V_{IH} corresponds with slight changes in CNFET threshold voltage. The fact that the threshold voltage variations are not independently and identically distributed (i.i.d.), but rather have spatial dependence, illustrates that a portion of the threshold voltage variations (and therefore variation in SNM) is due to wafer-level processing-related variations (CNT deposition is more uniform across the 150-mm wafer). Future work should optimize processing steps, for example, increasing the uniformityof the atomic-layer-deposition oxide deposition used for electrostatic doping to further improve SNM for realizing VLSI circuits. **e**, Wafer-scale CNFET CMOS characterization. Measurements from 4 diesacross 150-mm wafer (1,000 CNFET CMOS nor2 logic gates are sampled randomly from the 10,400 such logic gates in each die). No outliers are excluded. Yield and performance variations are negligibleacross the wafer, illustrated by the distribution of the output voltage swing.

Figure 3.5 shows the 150 mm wafer with the test patterns (each die has 10,400 CNFET CMOS two-input "not-or" (NOR2) logic gates). We fabricate and measure separate NOR2 logic gates as it enablescharacterization of key gate-level metrics, *e.g.* the voltage transfer curves (VTCs, which are used to compute the static noise margin of cascaded logic gates)[6], gain, and output voltage swing. Definitionsof these key metrics are shown in Figure A2.8.1a. Figure A2.8.1b shows the extracted distributions of these key metrics for all of the experimentally measured VTCs from the 10,400 logic gates shown in Figure 3.5 (importantly, these are the VTCs for all 10,400 CNFET CMOS NOR2 logic gates within a die, no logic gates have been excluded). To illustrate uniformity, the functional yield (output voltage swing >70%) for all logic gates within the die is 10,400/10,400, and the average output voltage swing is >98% with a standard deviation of <2%. Importantly, by extracting V_{OH}, V_{OL}, V_{IH}, V_{IL} from the VTCsassociated with each of the 10,400 logic gates, we are able to calculate the static noise margin (SNM) of all combinations of two cascaded NOR2 gates (i.e., with *driving* logic gate and *loading* logic gate). Figure A2.8.1c shows the distributions of the SNM for the ***>100 Million*** possible combinations of cascaded logic gate pairs (*i.e.*, with a *driving*

[6] VTCs allow extracting V_{OH}, V_{OL}, V_{IH}, V_{IL} (Figure A.2.9.2), which are essential for analyzing the noise resilience of cascadeddigital logic gates.

logic gate and a *loading logic gate*): 99.93% of logic gatepairs have positive noise margin *(i.e.*, $V^{(DR)} > V^{(LD)}$ and $V^{(DR)} < V^{(LD)}$, where (DR) is for the driving logic gate and (LD) is for the loading logic gate), indicating correct cascaded logic gate functionality. All of this characterization is performed at the scaled supply voltage of 1.2 V_{DD}.

Moreover, Figure A2.8.1d shows the noise margin violations (SNM < 0) can partially be attributed to the wafer processing (*i.e.*, not the CNTs), and therefore can be improved by optimizing processing (e.g.,ALD doping oxide uniformity over the 150 mm wafer)[7]. As can be seen in Figure A2.8.1d, there is a

spatial dependence of V_{IH} (as an example parameter to compute SNM; the other parameters exhibit similar spatial dependence): V_{IH} increases across the die (increasing from top to bottom). The change in V_{IH} corresponds with slight changes in CNFET threshold voltage. The fact that the threshold voltage variations are not uniformly distributed, but rather have spatial dependence, illustrates that a portion ofthe threshold voltage variations (and therefore variation in SNM) is due to wafer-level processing- related variations (CNT deposition is more uniform across the 150 mm wafer). Future work should optimize processing steps such as optimizing uniformity of the ALD oxide deposition used for electrostatic doping to further improve SNM for realizing VLSI circuits.

Additionally, to demonstrate that MIXED is wafer-scalable across 150 mm substrates, Figure A2.8.1e shows the first 150 mm wafer-scale CNFET CMOS characterization: measurements across 4 additionaldies distributed across the 150 mm wafer (1000 CNFET CMOS NOR2 logic gates are sampled randomly from the 10,000 ensemble in each die; as before *no logic gates are removed*) illustrating yield

across the 150 mm wafer (total yield across wafer: 14,400 logic gates, 57,600 CNFETs). This is the first demonstration of large-area, uniform, and high-yield CNFET CMOS logic, enabled by

[7] Fig. A2.8.1 shows the VIH has spatial dependency. The CNT deposition is highly uniform across the substrate and exhibits no spatial dependencies, which is therefore indicative that sources of threshold variations are processing induced.

combiningRINSE with our robust MIXED CNFET CMOS process.

Appendix 2.9 Prior work for overcoming metallic CNTs

The presence of m-CNTs have been a major obstacles in the field of CNTs since the first CNFET demonstrations over a decade ago. While a wide range of techniques have been developed in responseto m-CNTs, no technique achieves the required s-CNT purity for realizing CNFET digital VLSI systems. While previous works have set p_S requirements based on limiting m-CNT-induced leakage power, *no existing works have provided guidelines for p_S based on both increased leakage and degradedSNM due to m-CNTs for physical designs of VLSI circuits;* while 99.999% p_S is sufficient to limit EDPdegradation to <5%, Figure A.2.9.1 shows that SNM imposes far stricter requirements on purity: p_S
~99.999,999% to achieve $p_{NMS} \geq 99\%$ (for 1 million gate circuits).

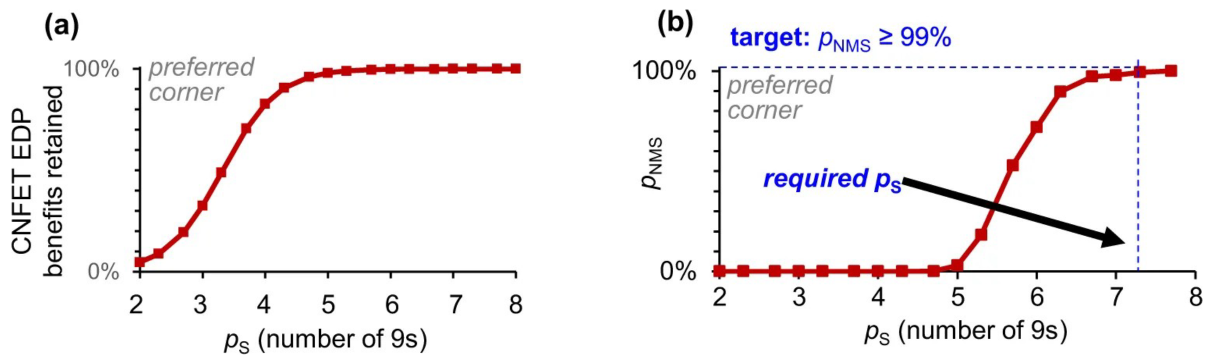

Figure A2.9.1: Effect of metallic CNTs on digital VLSI circuits. **a**) Reduction in CNFET EDP benefits versus p_S (metallic CNTs increase I_{OFF}, degrading EDP). $p_S \approx 99.999\%$, sufficient to minimize EDP cost due to metallic CNTs to ≤5%. **b**) p_{NMS} versus p_S (metallic CNTs degrade SNM), (shown for $SNM_R = V_{DD}/5$, and for a circuit of one million logic gates). Although 99.999% p_S is sufficient to limit EDP degradation to ≤5%, panel **b** shows that SNM imposes far stricter requirements on purity: $p_S \approx 99.999999\%$ (that is, number of 9s is 8) to achieve $p_{NMS} \geq 99\%$ (number of 9s is 2). Results inpanels **a** and **b** are simulated for VLSI circuit modules from a 7-nm node processor core (see Supplementary Information and Methods for additional details).

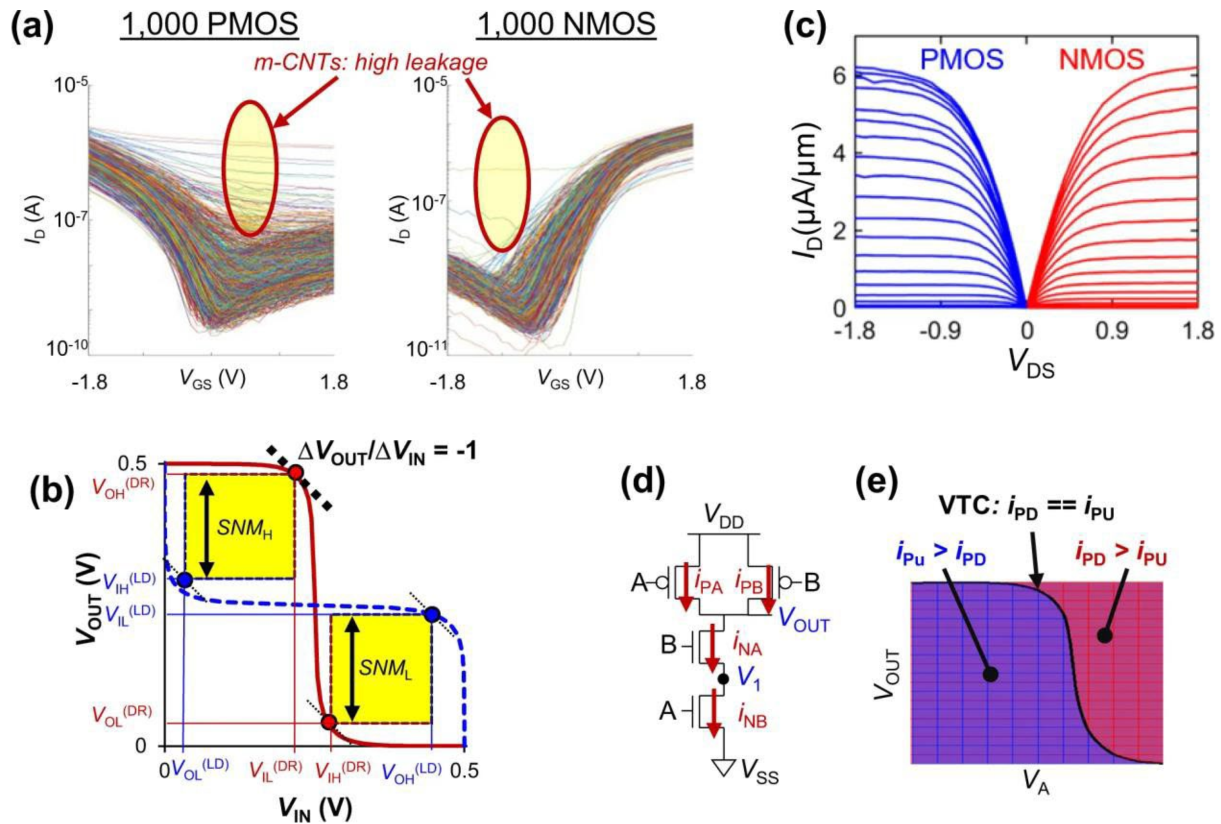

Figure A2.9.2: Methodology to solve VTCs using CNFET I-V measurements. **a**) Experimentally measured I_D versus V_{GS} for all 1,000 NMOS (V_{DS} = 1.8 V) and 1,000 PMOS CNFETs (V_{DS} = −1.8 V), with no CNFETs omitted. Metallic CNTs (m-CNTs) present in some CNFETs result in high off-state leakage current (I_{OFF} = I_D at V_{GS} = 0 V). **b**) VTC and SNM parameter definitions, for example, for (nand2, nor2). DR is the driving logic stage; LD is the loading logic stage. SNM = min(SNM_H, SNM_L),where SNM_H = $V^{(DR)}$ – $V_{IH}^{(LD)}$ and SNM_L = $V_{IL}^{(LD)}$ – $V^{(DR)}$. **c–e)** Methodology to solve VTCs (for example, for nand2) using experimentally measured CNFET *I–V* curves. **c**, Example I_D versus V_{DS} for NMOS and PMOS CNFETs (V_{GS} is swept from −1.8 V to 1.8 V in 0.1-V increments). **d)** Schematic. To solve a *V*TC (for example, V_{OUT} versus V_A with V_B = V_{DD}): for each V_A, find V_1 and V_{OUT} such that $i_{PA} + i_{PB} = i_{NA} = i_{NB}$ (DC, direct current, convergence). **e)** Current in the pull-up network (i_{PU}, where $i_{PU} = i_{PA} + i_{PB}$, and i_{PA} and i_{PB} are the labelled drain currents of the PMOS FETs gated by A and B, respectively) and current in the pull-down network (i_{PD}, where $i_{PD} = i_{NA} = i_{NB}$, and i_{NA} and i_{NB} are thelabelled drain currents of the NMOS FETs gated by A and B, respectively) versus V_{OUT} and V_A. The VTC *i*s seen where these currents intersect. CNFETs are fabricated at a ~1 μm technology node, and the CNFET width is 19 μm in panel **a**.

To quantify the impact of m-CNTs on VLSI circuits, we analyze circuit modules synthesized from theprocessor core of OpenSparc T2, a large multi-core chip that closely resembles the commercial Oracle/SUN Niagara 2 system [1]; thus, our results account for effects present in realistic VLSI

circuits

– such as wire parasitics, buffer insertion to meet timing constraints, and SNM for cross-coupled logicstages in sequential logic elements – that are not present in small circuit benchmarks. We leverage standard cell libraries derived from the reference library "asap7sc7p5t" included with the ASAP7 process design kit (*PDK*) to create physical designs of the OpenSparc modules at an example 7 nm technology node [2], to compare optimized energy, delay, area, and p_S required to achieve $p_{NMS} = 99\%$for VLSI circuits. The baseline case ("non-DREAM"), which permits all pairs of logic stages, requires$p_S \geq 99.999,996,3\%$ to achieve $p_{NMS} \geq 99\%$ (for $SNM_R = V_{DD}/5$). See Methods for additional details on digital VLSI system analysis.

[1] *OpenSparc T2 Processor Core*. Online: http://www.opensparc.net/opensparc-t2.

[2] Clark, Lawrence T., Vinay Vashishtha, Lucian Shifren, Aditya Gujja, Saurabh Sinha, Brian Cline, Chandarasekaran Ramamurthy, and Greg Yeric. "ASAP7: A 7-nm finFET predictive process design kit." Microelectronics Journal 53 (2016): 105-115.

Below is a table summarizing s-CNT purity achieved through a range of techniques. None meet the required target of 99.999,999% purity to achieve PNMS > 99% for 1 million gate circuits; state-of-the-art purity is 99.99% s-CNT: a factor of >10,000× below the required s-CNT purity. The majority of prior CNT circuits have dealt with m-CNTs through either removing m-CNTs pre- or post- deposition. Pre-deposition techniques include both solution-based sorting to selectively remove m-CNTs while theCNTs are suspended in solution, as well as selective s-CNT growth. Unfortunately, while there has beenextensive work on both approaches, s-CNT purity remains at ~99.99%. Commercially available purified CNTs also approach 99.99% s-CNT purity; none exceed this threshold. Alternatively, CNTs can be removed post-CNT deposition. For this approach, an ensemble of s-CNTs and m-CNTs (conventional CNT synthesis yields ~30% m-CNTs) is deposited on the wafer, and the m-CNTs are then selectively removed. Electrical

breakdown is performed by biasing the gates of the CNFETs off and applying a large source-drain bias. The s-CNTs do not conduct current due to the gate biasing, but the m-CNTs still flow current (by virtue of being an m-CNTs). With sufficient source-drain bias, the m-CNTs flowenough current that they heat up due to Joule self-heating and eventually oxidize and are removed (similar to a fuse). However, electrical breakdown (and techniques leveraging electrical breakdown) can also only remove 99.99% of m-CNTs, require CNFETs to be fabricated to withstand large breakdown voltages (which requires thicker oxides, for instance, degrading CNFET performance), and remove and degrade s-CNTs inadvertently. Variations on electrical breakdown (such as VMR or thermocapillary reflow) require either significant additional processing steps and time, or the use of non-conventional and non-silicon CMOS compatible materials. Moreover, they similarly can achieve only 99.99% s-CNT purity.

Work	Technique	Highest Purity	Challenge
This work	DREAM	Leverages DREAM design to enable VLSI systems with commercially-available 99.99% s-CNT purity.	
[1]	Thermocapillary reflow	99.99% s-CNT	Insufficient purity; non-standard processing
[2]	Electrical breakdown (VMR)	99.99% s-CNT	Insufficient purity; non-standard processing; high voltage damages circuits; inadvertent s-CNT removal and damage while removing m-CNTs

[3]	Solution-based sorting	99.99% s-CNT	Insufficient purity
[4]	Column chromatography	99.99% s-CNT	Insufficient purity
[5]	Gas phase etching	<98% s-CNT	Insufficient purity, low CNT density
[6]	Selective CNT growth	99.9% s-CNT	Insufficient purity, low CNT density

[1] Shulaker, M.M., Hills, G., Wu, T.F., Bao, Z., Wong, H.S.P. and Mitra, S., 2015, December. Efficientmetallic carbon nanotube removal for highly-scaled technologies. In *Electron Devices Meeting (IEDM),2015 IEEE International* (pp. 32-4). IEEE.

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Appendix A3: Extended Discussion on CNT Reliability

Appendix 3.1 Additional Data on Si_3N_X Encapsulation

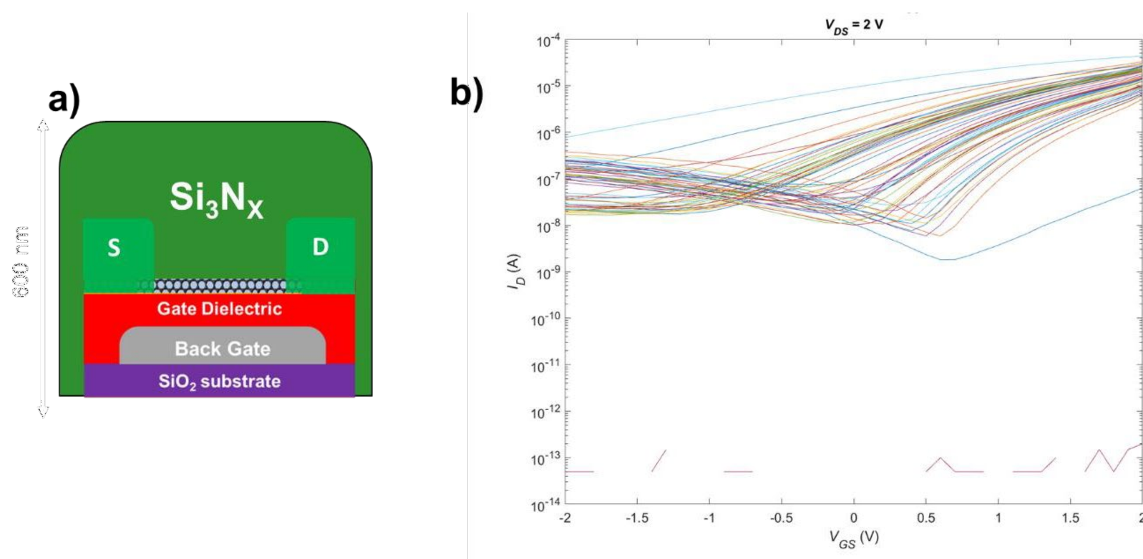

Figure A3.1.1: Silicon nitride deposited directly over channel region. In order to electrostatically dope the CNT channel *n*-type, an ALD deposited HfO_X film was used as the nonstoichiometric dopingoxide (NDO) layer. However, silicon nitride films have been shown to perform a similar electrostatic doping effect when deposited directly over the CNT channel[1]. In (a), we show a schematic of such a NMOS CNFET, where the CNFET is fabricated identically to the NMOS CNFET in Figure 1a, but without a HfO_X NDO layer. Figure (b) shows the resulting I_D-V_{GS} data for 100 NMOS CNFETs fabricated using this method after annealing the film in N_2 at 275 °C. CNFETs fabricated using this technique exhibit large uncontrollable variations. Moreover, one CNFET measured <1 pA drain current. Previously published work has suggested that the PECVD deposition may damage underlyingCNTs in the channel through the generation of ionized reactants when forming the nitride film,[2] leading to increased variations among CNFETs. Thus, the HfO_X NDO film used in our study not only serves to controllably *n*-type dope the CNT channel, but also effectively shields the CNTs from plasma induced degradation during the nitride deposition. To obtain optimal *n*-type doping of NMOS CNFETs, a HfO_X NDO film should be used in between the CNFET channel and nitride encapsulation film.

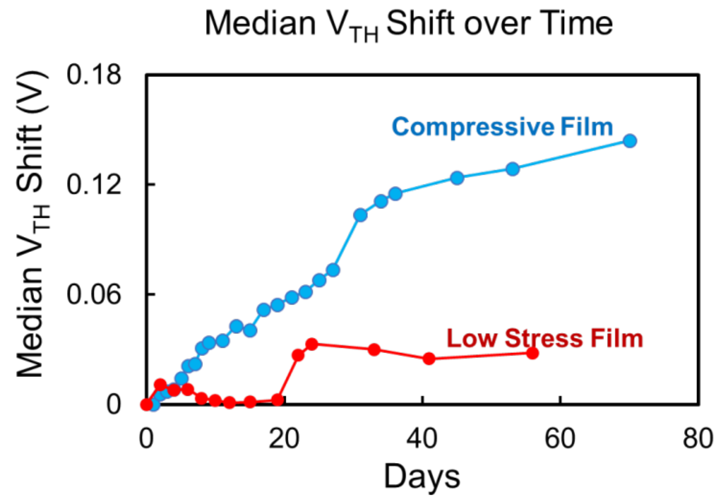

Figure A3.1.2: Tuning film stress in PECVD silicon nitride encapsulation films. The long term stability of nitride encapsulated CNFETs can be further improved by optimizing the silicon nitride filmstress. The stress of silicon nitride films is precisely controlled by varying the high frequency and low frequency deposition pulses during PECVD. In particular, low frequency (100-350 kHz) pulses are usedto form dense and compressive films, while high frequency (13.56 MHz) pulses are used to form tensilefilms. A mixture of low frequency and high frequency pulses can be used to achieve films with low stress. In Fig S2, we report the median V_{TH} shift for NMOS CNFETs encapsulated in compressive silicon nitride and low stress silicon nitride films. The low stress silicon nitride films show superior air stability compared to the compressive films. Specifically, for devices encapsulated in low stress siliconnitride, the median V_{TH} shift saturates at <40 mV after 25 days and remains at <40 mV for 50 days. In comparison, NMOS CNFETs encapsulated in compressive silicon nitride films show a continued shiftin V_{TH}, with a maximum V_{TH} shift > 150 mV over 70 days. Importantly, all NMOS CNFETs were encapsulated in silicon nitride films deposited at 250 °C, making this encapsulation scheme compatiblewith back-end-of-line processing.

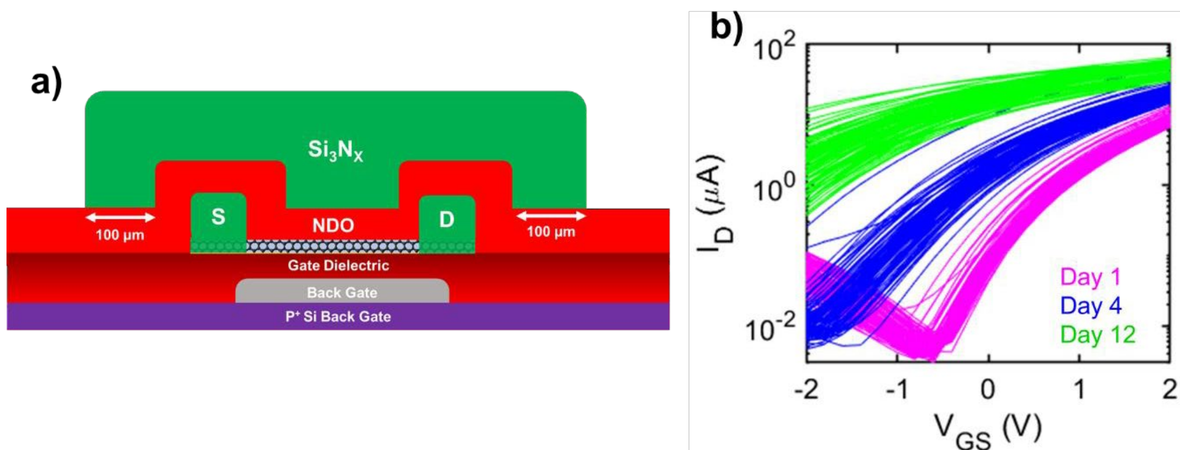

Figure A.3.1.3: NDO degradation due to partial air exposure. In order to prevent unwanted V_{TH} shifts over time, the Si_3N_X film must encapsulate the entire NDO film. The schematic in

Figure S3a shows an example NMOS CNFET that is *not* fully encapsulated. In the schematic, a Si_3N_X film is deposited directly over the NMOS CNFET and all of the Si_3N_X film 100 μm beyond the CNFET perimeter is etched away. This device structure leaves part of the NDO layer along the perimeter of the Si_3N_X film exposed to air. Figure S3b shows the I_D-V_{GS} curves of 100 of these partially encapsulated CNFETs after 1, 4, and 12 days. Unlike the I_D-V_{GS} curves in Figure 3c, which are completely encapsulated in Si_3N_X, these electrostatically doped CNFETs with partially exposed NDO suffer from substantial V_{TH} shifts over just 12 days. Though the NDO regions exposed directly to air are 100 μm away from the NMOS channel, NDO degradation and large V_{TH} shifts are still observed in these devices over time. Thus, careful design of encapsulated NMOS CNFETs is required to ensure that the NDO film is completely encapsulated in the Si_3N_X film.

Appendix 3.2 Previous works on reducing CNFET variability

Method	Number of CNFETs	V_{TH} standard deviation (σV_{TH})	CNFET Dimensions	Ref.
HMDS Coating	52	Before: 270 mV After: 160mV	L_{CH} = 300 nm Width = 15 um (0-3 CNTs per FET) T_{ox} = 10nm SiO_2	[3]
PECVD Silicon Nitride	30	Before: Not reported After: 1.6 V	L_{CH} = 4 μm Width = 50 μm T_{ox} = 50nm SiO_2	[1]
Thermal Annealing	100	Before: 668 mV After: 48 mV	L_{CH} = 3 μm Width = 10 μm T_{ox} = 12nm HfO_2 + 12nm Al_2O_3	This work

Figure A3.2.1: Prior work on reducing variability in CNFETs. Work by Franklin *et al*. have shown that HMDS coatings can be employed to repel ambient molecules away from the CNT channel, thereby mitigating the impact of ambient molecules on CNFET electrical performance and reducing V_{TH} standard deviation by ~1.7×.[3] A study by Ha *et al*. attempted to deposit PECVD silicon nitride directly over the CNT channel to simultaneously passivate and *n*-type dope the CNFETs.
However, a direct comparison of CNFET variation before and after the nitride encapsulation was not presented in that study. Note that absolute values of σV_{TH} measured in different studies are difficult to compare due to the differences in CNFET dimensions (*i.e.* increasing channel dimensions or shrinking the oxide thickness can reduce σV_{TH}).

Appendix 3.3 Additional Details on Bias Temperature Instability measurements

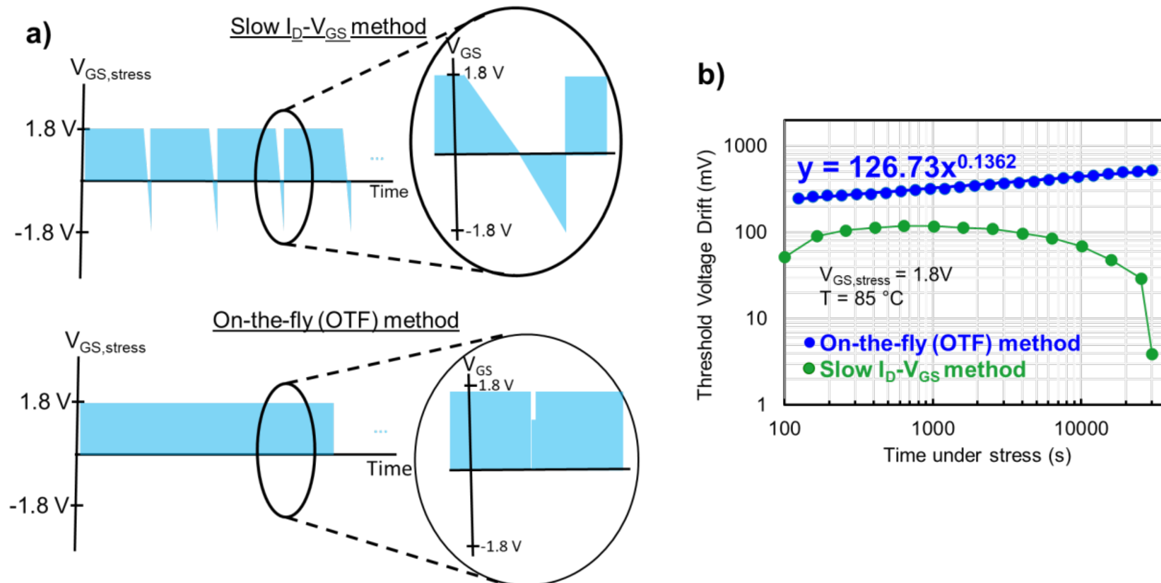

Figure A3.3.1: Comparison of slow I_D-V_{GS} vs. On-the-fly (OTF) method for extracting V_{TH}. (a) Voltage plots showing how $V_{GS,stress}$ changes over time using the two methods. The slow I_D-V_{GS} method allows for full V_{GS} sweep of the transfer characteristics, but disrupts the applied PBTI stress when taking the measurement. The OTF method takes a single current measurement (~600 μs duration) and the V_{TH} is extrapolated, resulting in minimal disruption to the PBTI stress. (b) V_{TH} drift measured using the corresponding two methods. The V_{TH} degradation trend measured using the OTF method follows a power law, whereas the trend measured using the slow I_D-V_{GS} method suggests thatthe devices partially recover V_{TH} drift during the long measurement intervals.

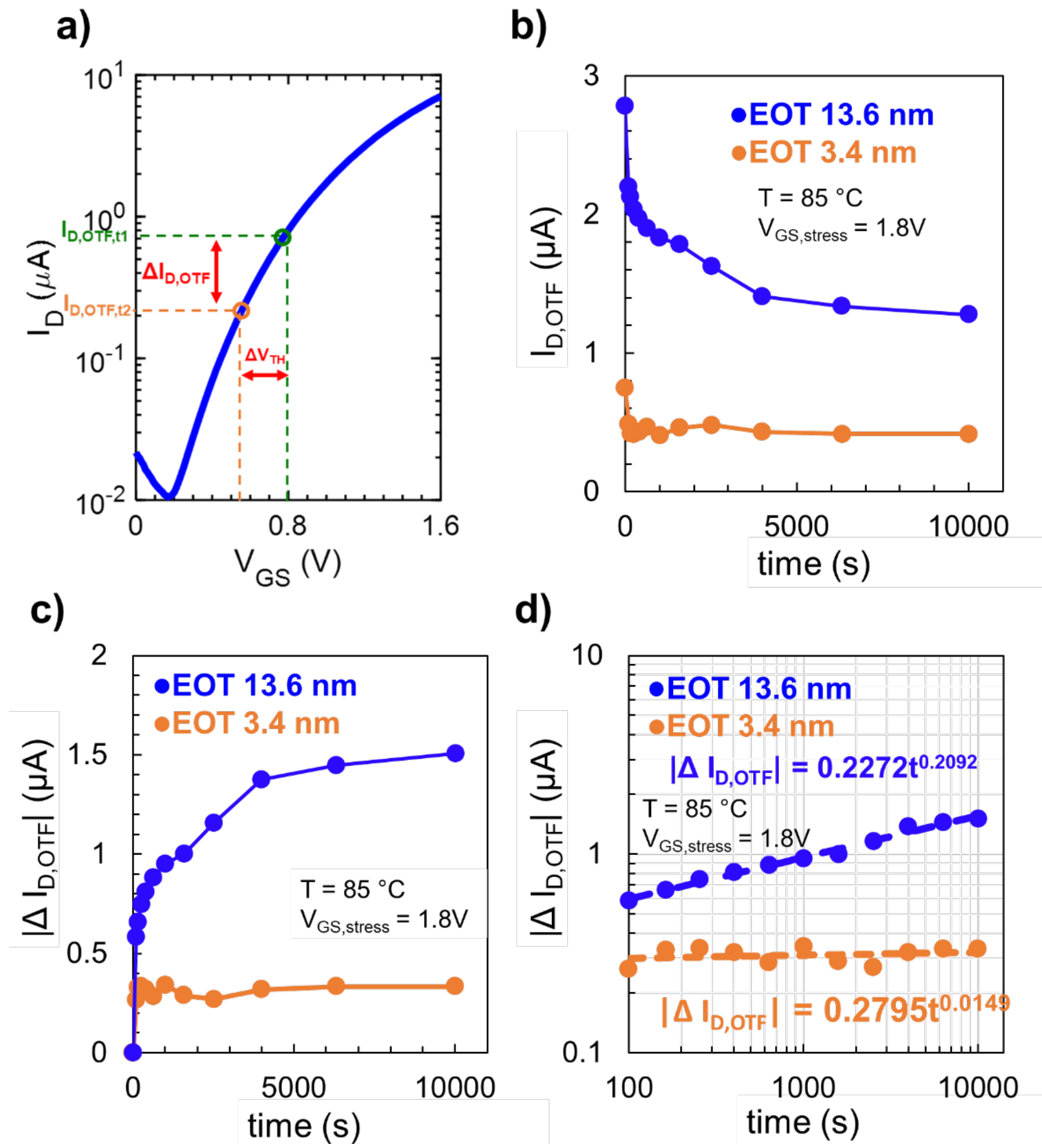

Figure A3.3.2: On-the-fly current measurements. (a) Illustration of how V_{TH} drift is extracted froman on-the-fly current measurement. (b) On the fly current ($I_{D,OTF}$) measurements when 1.8V stress is applied to the gate of a thick gate oxide and thin gate oxide device. (c) Linear and log-log plot showing change in on-the-fly current ($\Delta I_{D,OTF}$) over time when 1.8V stress is applied to the gate.

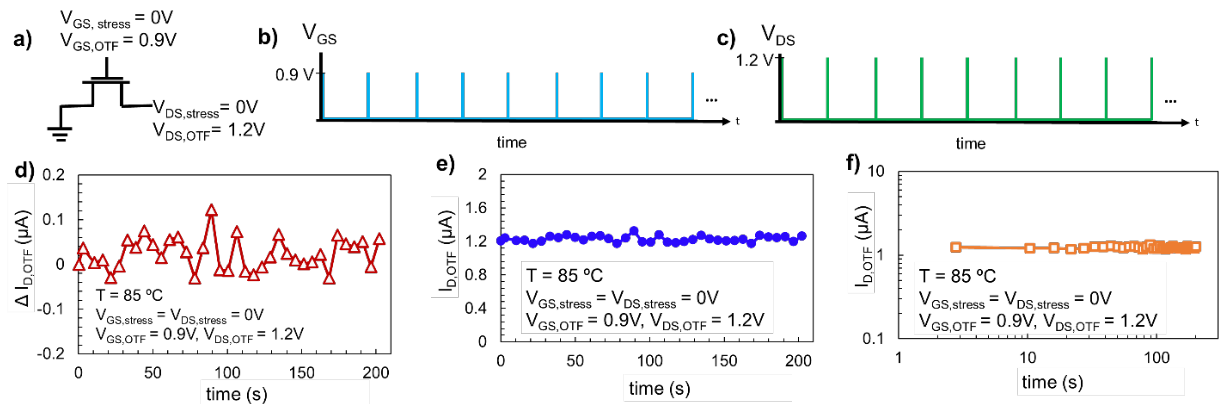

Figure A3.3.3: Effect On-the-fly measurement on V_{TH} drift when zero bias stress is applied. (a)FET biasing conditions during stress period and when the on-the-fly measurement is being taken.

Voltage plots of (b) gate bias and (c) source/drain bias when the zero bias stress test was performed (voltage is only applied at moments when OTF measurement is taken). (d) change in current on-the-fly current over time when no electrical bias stress is applied. (e) Linear and (f) log-log plots of on- the-fly current ($I_{D,OTF}$) measurements when no electrical bias stress is applied.

Appendix 3.4 Burn-In Procedure for BTI Testing

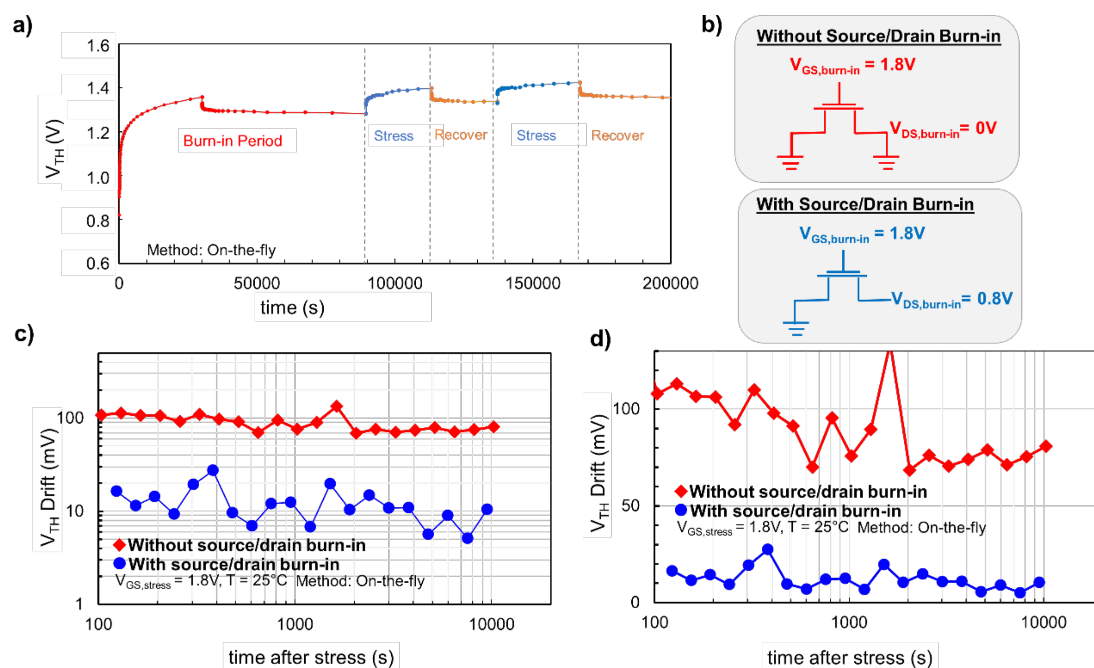

Figure A3.4.1: Burn-in procedure for reducing initial V_{TH} drift. (a) V_{TH} of a nitride encapsulatedCNFET (EOT = 13.6 nm) during the initial burn-in period and subsequent stress-recovery cycles.
During the burn-in period, V_{GS} = 1.8V for 30,000 seconds, followed by a period of zero stress. After the burn-in procedure, the device is stressed at V_{GS}=1.8V for 30,000s, followed by a recovery period of zero stress. The device's V_{TH} degradation follows a similar trend after an additional stress-recoverycycle. (b) The burn-in procedure can be modified by adding a V_{DS} bias during the burn-in procedure.
(c) Log-log and (d) semi-log plots of average reduction in V_{TH} drift for 3 NMOS CNFETs that underwent source/drain burn-in and 3 NMOS CNFETs that did not undergo source/drain burn-in. Alldevices used in (c, d) are nitride encapsulated NMOS CNFETs with EOT = 3.4 nm.

Despite the potentially advantageous time decay exponent and rapid recovery characteristics of electrostatically doped CNFETs, the measured CNFETs had large initial V_{TH} shifts immediately after stress was applied before stabilizing at a near constant V_{TH} value. For example, in Figure 5c, the first V_{TH} measurement taken in the stress phase showed >100 mV V_{TH} shift compared to the initial V_{TH} value before stress. To explore the origins of this large initial V_{TH} drift, in Figure S8 we perform burn- in tests, which are commonly used in the reliability testing of emerging

semiconductor devices to eliminate traps and fixed charges formed during non-ideal fabrication processes that have yet to be fully optimized[4–9]. Figure S8a demonstrates how employing a burn-in period (where a gate bias, $V_{GS,burn-in}$, is applied for several hours) can reduce the magnitude of V_{TH} drift in subsequent stress- recovery cycles. We employed this gate bias burn-in procedure and then allowed devices to rest at room temperature without bias for >50,000s before performing the reliability tests on all the devices used for PBTI testing in this manuscript. Moreover, capturing reliability data after burn-in is performed more accurately resembles the operating conditions that the CNFETs would experience when deployed in real commercial products where System on Chip (SoC) products are commonly burned-in for several hours at high voltage after packaging.[10–15]

Beyond this gate bias burn-in procedure, in Figure S8c and S8d, we find that including a positive V_{DS}bias during burn-in ($V_{DS,burn-in}$) can reduce the CNFET's initial V_{TH} drift from ~100mV to ~10mV. Such results suggest that, by applying $V_{DS,burn-in}$ before the actual PBTI test, current can flow throughthe contacts and channel thereby filling traps created during the fabrication of the CNFET. These traps that are eliminated during burn-in may originate from imperfect processing conditions (*i.e.* reduced quality of ALD deposited thin films or ionic contaminants that may be introduced at various phases of the fabrication flow). Thus, further optimizations to the CNFET fabrication process beyondprocess control capabilities of an academic fabrication lab may eliminate the need for burn-in procedures.

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