

# A Ballistic Transport Model for HEMTs and III-V MOSFETs

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by

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**B.S. Electrical Engineering  
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## **ABSTRACT**

As silicon MOSFETs keep scaling down in size, the continued improvement on their logic performance is threatened by their fundamental physical limits. With silicon approaching these limits, MOSFETs designed with III-V semiconductors have emerged as promising candidates to replace them. The low-effective mass of various III-V materials such as InGaAs and InAs allow both faster and more power efficient performance.

One of the key challenges, particularly as devices continue to shrink, is to understand the important of non-idealities in FET structures. High-electron mobility transistors, or HEMTs, are III-V Quantum-Well FETs that we can use to explore many issues of relevance to future III-V MOSFETs. HEMTs are worthwhile transistors in their own right, but are also simpler than III-V MOSFETs and therefore allow a more thorough exploration into the basic transport physics of a quantum-well III-V device.

We know from HEMT experimental data that electrons travel ballistically at gate lengths of 30-40 nm, suggesting that a ballistic transport model will only become more accurate as channel lengths are scaled down to 10 nm. We would like to investigate to what extent this is true in III-V MOSFETs, and also to study the impact of short channel effects and other parasitics inherent to a III-V design.

To accomplish these goals, we have developed a flexible transistor model in MATLAB based on a ballistic theory of transport. We will first verify the model with HEMT experimental data coming from devices fabricated at MIT, and then focus our attention on peculiarities specific to III-V MOSFETs, namely a buried-channel design and the presence of traps at the oxide-semiconductor interface. We will use the model to extract the trap density as a function of energy, and then make measurements independent of interface trap effects to extract the 2D sheet carrier concentration and mobility, two figures of merit important in characterizing FET devices. The ability to correctly model and predict device behavior will help identify the problems ahead that need improvement in the iterations of future device fabrication.

Thesis supervisor: Jesús A. del Alamo

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# CHAPTER 1. INTRODUCTION

Moore's law demands that logic devices must continue to shrink, but silicon-based MOSFETs are fast approaching their fundamental limits and may not be a viable option for gate lengths below 10 nm [1]. MOSFETs designed with III-V semiconductors, however, have become promising candidates to replace them. Their improved transport properties and efficiency stem from the low-effective mass of typical III-V materials such as InAs or InGaAs. In this study, we will explore not only the III-V MOSFET but also the III-V high electron mobility transistor, or HEMT. The HEMT will give us insight into the fundamental transport properties common to all quantum-well FETs, and from there we can address the unique characteristics that arise from the presence of an oxide layer in the III-V MOSFET.

## *1.1 Introduction to III-V HEMTs and MOSFETs*

Whereas many traditional semiconductor devices use p-n homojunctions, high electron mobility transistors exploit the characteristics of a heterojunction. The use of a large-bandgap, highly doped material next to an undoped, narrow-bandgap material creates sheet of electrons within which the electrons can move with far less scattering and a higher velocity. This concept of modulation doping, where there is a spatial separation between the dopants and the electrons, results in the formation of a two-dimensional electron gas (2DEG) at the interface between the different bandgap materials [2]. The electrons in the quantum well have a high mobility and can move quickly without colliding with any impurities, due to the fact that the channel is made out of an undoped material.

Commonly used material combinations for HEMTs include AlGaAs/GaAs, AlGaN/GaN, and InAlAs/InGaAs. These pairs are chosen by the need to have a close lattice match but also large conduction band discontinuity between the two materials, and the specific pair is determined by the desired device application be it high power or high frequency performance. In this work, we

will study InAlAs/InGaAs HEMTs. Figure 1-1 shows the schematic for a typical HEMT structure. An InAlAs buffer layer is grown on top of an InP substrate, and the channel is either InAs or InGaAs with a high-indium content, surrounded by InGaAs cladding layers. The choice of an InAs or  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  channel is because both materials have been shown to exhibit high injection velocities and relatively low effective mass [3]. Above the channel is an InAlAs barrier layer with a  $\delta$  doping layer of Si that provides carriers to the channel. The highly doped InGaAs capping layer improves the contact resistance of the HEMT.

There are various aspects of the HEMT to consider when characterizing its operation. A few key parameters of the device include  $L_g$ , the gate length,  $L_{\text{side}}$ , the distance between the edge of the gate and the edge of the cap as depicted in Figure 1-1, and both the channel and barrier thicknesses. These parameters greatly impact many figures of merit important to HEMTs, including the transconductance  $g_m$  that is a measure of how steeply the current rises above threshold, and the subthreshold swing, which is the rate of the current drop-off below the threshold voltage  $V_T$ . The drain-induced barrier lowering (DIBL) which is the dependence of the threshold voltage on the drain-to-source voltage  $V_{DS}$  is another parameter of interest. Parasitic resistances and capacitances inherent to the structure of the material also play a role in determining the operational behavior of the HEMTs [3],[4].

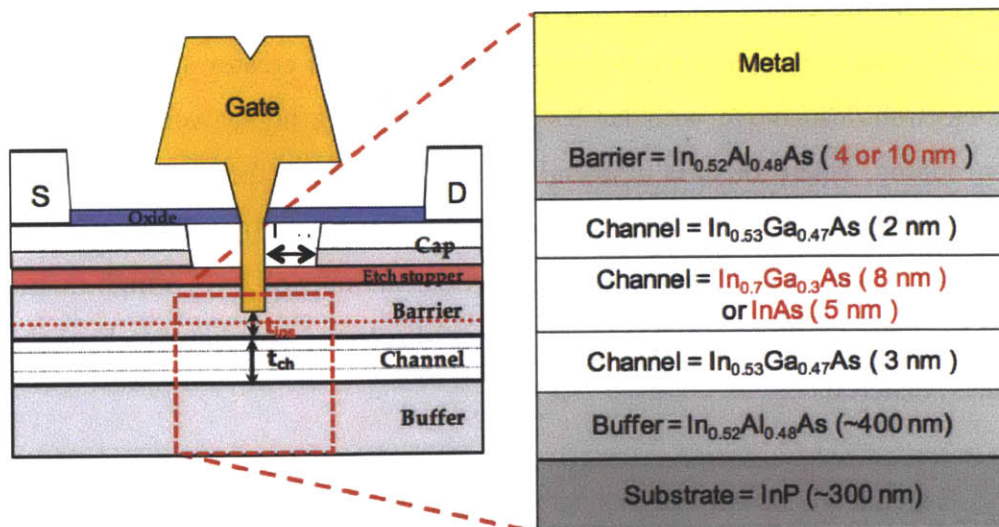


Figure 1-1. Schematic of a HEMT structure, reproduced from D. Jin *et al.* [5]. The red dotted line in the schematic indicates the location of the  $\delta$  doping layer, and the channel consists of either InGaAs or InAs.

Until now, HEMTs have been used in high speed and high frequency applications, but not for logic applications. They cannot present a viable alternative to silicon-based logic devices because of their high gate leakage current. III-V quantum-well MOSFETs address this problem by inserting an oxide layer between the gate and the barrier layer, as shown in Figure 1-2. In fact, III-V MOSFETs employing high- $\kappa$  dielectrics are already in development and have been demonstrated with excellent performance [5, p. 2], making them promising candidates for future generations of CMOS technology. However, the presence of the oxide layer introduces a density of interface state traps,  $D_{it}$ , that can degrade the subthreshold swing and yield a poorer  $I_{ON}/I_{OFF}$  ratio [7].

It is important, then, to consider not only the device characterization of HEMTs, but also the unique issues that arise in the transition from III-V HEMTs to MOSFETs. These two objectives will be the focus of this study.

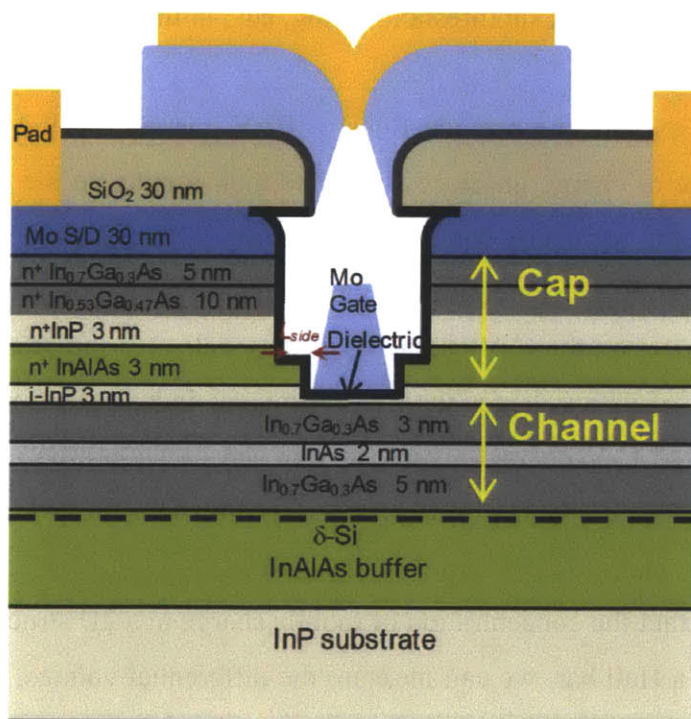


Figure 1-2. Schematic of a MOSFET structure, reproduced from J. Lin *et al.* [6]. The black layer represents a thin high- $\kappa$  dielectric, and the  $\delta$  doping layer is located underneath the channel.

## *1.2 Motivation – A Compact Model for Device Studies*

As discussed above, there are many characteristics of a transistor, both intrinsic and extrinsic, that will have an effect on device performance. This leads to the desire for a flexible, compact model based on the ballistic transport of electrons as a 2DEG, which at 30 nm gate lengths, should be an accurate representation of the current in a FET and which will only become more accurate as channel lengths are scaled down to 10 nm. Experimental verification of this assumption comes from devices fabricated at MIT, where the source injection velocity of electrons at gate lengths of 30-40 nm is seen to approach saturation [3]. The saturation of the injection velocity suggests that the HEMT devices are close to operating in a purely ballistic regime.

One goal of this project is to develop a hybrid approach where the quantum-mechanical portion of the simulation, through means of Poisson-Schrödinger simulations, is accurate but the device transport is simplified and short-channel effects are neglected so as to focus on the role of various parasitics, such as DIBL, subthreshold swing, etc., in limiting device performance.

A need also exists to explore the non-idealities of III-V quantum-well MOSFET structures; in particular, the presence of charge interface states and their impact on the I-V characteristics is a phenomenon that has not been fully studied. We can use C-V measurements to characterize the device and extract the sheet carrier concentration and mobility,  $n_s$  and  $\mu$  respectively. However, because  $D_{it}$  has an impact on the C-V characteristics as well, it is important to be able to obtain  $n_s$  and  $\mu$  over a range of gate voltages through techniques independent of  $D_{it}$ , and to juxtapose them with the measured C-V characteristics. In this way, a  $D_{it}$  profile could be extracted and compared with other methodologies of finding interface trap densities [8].

A common way to extract the concentration of mobile charge in a 2D structure is to perform Hall measurements. Using a Hall bar, we can measure the differential voltage, or Hall voltage, in the presence of a magnetic field when current is injected down the length of the bar. This voltage,  $V_{Hall}$ , as well a determination of the sheet resistance, will yield the values of mobile charge and mobility independently. With a gated Hall bar,  $n_s$  and  $\mu$  can be found across all regimes of

operation and compared with experimental C-V to yield a complete picture of  $D_{it}$ . The second goal of this study, therefore, will be to construct a complete capacitance-voltage model that accurately incorporates the role of  $D_{it}$  and to compare this against measurements on actual structures.

### ***1.3 Thesis Outline***

In this project, we develop a compact transistor model in MATLAB. This HEMT current-voltage model is based on ballistic transport and incorporates many parasitic elements such as DIBL and source and drain resistances with the intent of exploring the impact of these parasitics on device behavior.

We also build upon an existing quantum capacitance model for HEMTs [5] to incorporate  $D_{it}$  effects, and compare experimental C-V characteristics with simulated ones. As an integral piece of the C-V work, gated Hall measurements were carried out that resulted in extracted mobilities significantly higher than those measured by split C-V techniques [6].

This thesis is organized in the following way. Chapter 2 is a detailed theoretical discussion of both the ballistic current model and the gate capacitance model. The central physics of ballistic transport are outlined and a simulation process flow is introduced that allows the incorporation of non-idealities, each of which are also discussed in detail. The gate capacitance model is also described for both HEMTs and III-V MOSFETs. This theory results in a comprehensive framework against which experimental data can be compared.

In Chapter 3 we present the results of the theoretical model as they relate to the HEMT. We first discuss several important non-idealities, such as the effect of non-parabolic bands on the output and transfer characteristics. Then, we compare the simulated data against experimental data for HEMT devices.

Chapter 4 investigates the characteristics of the MOSFET, focusing first briefly on the effect of  $D_{it}$  on the I-V characteristics and in particular, the subthreshold swing. The primary focus of

Chapter 4, however, is to compare the C-V data for III-V MOSFETs against the quantum capacitance model, and to use this to extract  $D_{it}$ . To complement these results and demonstrate how large of an effect  $D_{it}$  can have on device figures of merit, conventional gated Hall measurements were performed and values of 2DEG sheet carrier concentration and channel mobility were obtained.

To conclude in Chapter 5, we summarize the results of this work on a ballistic compact model, and provide suggestions for future work in the field of III-V FET characterization.

## CHAPTER 2. I-V THEORETICAL MODEL

### *2.1 Introduction*

In this chapter, we use Poisson-Schrödinger simulations to construct the current-voltage characteristics of both HEMTs and III-V MOSFETs. For this, we have developed a ballistic transport model. The peculiarities associated with MOSFETs are discussed separately as additions to the model for the HEMT.

### *2.2 Previous Work*

#### **2.2.1 Current in a Ballistic Quantum-Well FET**

In a HEMT, electrons move in the undoped, narrow-bandgap channel material with minimal scattering. This is due to their spatial separation with the  $\delta$  doping layer in the barrier that provides the free carriers (see Figure 1-1: the  $\delta$  doping layer is located in the barrier, and carrier transport occurs inside the channel). For short enough gate lengths, the electrons actually travel at a ballistic velocity, where they do not scatter at all as they move through the channel. A detailed calculation of the current in a QW-FET is covered by [9], and summarized below.

For a QW-FET, the electrons are confined in one direction (normal to the wafer surface) and therefore create a two-dimensional electron gas. To simplify the analysis, we assume that only a single sub-band in the channel is occupied, as shown in Figure 2-1. This is actually the case in deeply scaled HEMTs and MOSFETs operating close to the peak transconductance point. The level labeled  $E_1$  is the bottom of the first 2D energy band that arises as a result of the quantum well structure of the channel.  $E_F$  is the location of the Fermi level in the material, whose level is extended beyond the channel for reference. The discontinuity in the barrier arises from the  $\delta$  doping layer, and we define the surface potential  $\phi_s$  as the distance between the Fermi level and the conduction band edge at the interface between the channel and the barrier.

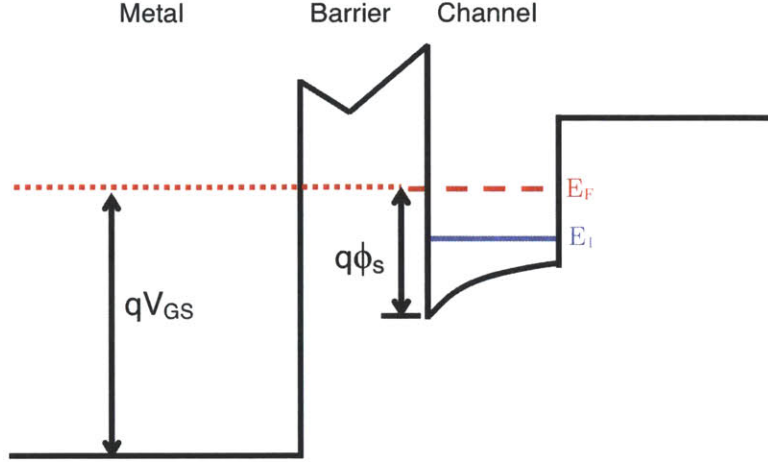


Figure 2-1 Energy band diagram for a QW-FET. The first sub-band is depicted as  $E_1$ , and the Fermi level in the material as  $E_F$ . The surface potential is shown as  $\phi_s$ .

The 2D density of states in the sub-band is known to be:

$$g_{2D}(E) = \frac{m^*}{\pi\hbar^2} \quad (1)$$

$m^*$  is the effective mass of the electrons in the channel material, and  $\hbar$  is the reduced Planck's constant. The sheet carrier concentration,  $n_s$ , which is needed in order to find the current in the FET, can be found by integrating the product of  $g_{2D}$  and the Fermi function  $f(E)$ :

$$n_s = \int_{E_1}^{\infty} g_{2D}(E)f(E)dE = \frac{m^*}{\pi\hbar^2} \int_{E_1}^{\infty} \frac{dE}{1 + e^{\frac{E-E_F}{kT}}} \quad (2)$$

$k$  is Boltzmann's constant, and  $T$  is the temperature of the material. Solving this integral yields the following simple expression:

$$n_s = N_{2D} \mathfrak{S}_0 \left( \frac{E_F - E_1}{kT} \right) \quad (3)$$

where  $N_{2D}$  is the 2D effective density of states,

$$N_{2D} = \frac{m^*kT}{\pi\hbar^2} \quad (4)$$

and  $\mathfrak{S}_0$  is the Fermi-Dirac integral of order 0:

$$\mathfrak{F}_0(x) = \ln(1 + e^x) \quad (5)$$

Figure 2-2 illustrates the concept of the virtual source model, where the current is limited by the injection of electrons over the barrier at the source [10]. For a high enough drain voltage, we assume there will be no back flow of electrons from the channel or the drain past the injection point.

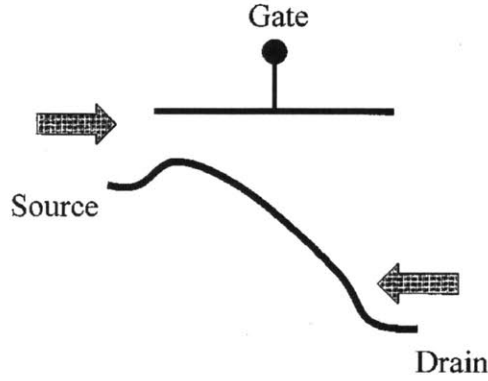


Figure 2-2 Conduction band along the length of the channel, for high drain bias, reproduced from [10]. Electrons injected from source and drain are labeled by arrows.

For such high drain biases, all the electrons at the virtual source contribute to the current, making the expression for current in the FET simply:

$$I_D = qn_s v_{inj} \quad (6)$$

where  $v_{inj}$ , the injection velocity, is the average velocity of the electrons as they move towards the drain.  $v_{inj}$  can be found by computing  $v(E)$  for electrons in the channel, integrating over  $E$ , and then dividing by the number of electrons. If we consider the channel to be oriented in the  $x$ -direction, then the velocity of electrons at a given energy  $E$  is given by [9]:

$$v_x(E) = \frac{2}{\pi} \sqrt{\frac{2(E - E_1)}{m^*}} \quad (7)$$

To find the injection velocity, we must consider both the occupation and the density of states at every energy  $E$ , and properly normalize:

$$v_{inj} = \frac{\int_{E_1}^{\infty} g_{2D}(E) v_x(E) f(E) dE}{\int_{E_1}^{\infty} g_{2D}(E) f(E) dE} \quad (8)$$

This yields:

$$v_{inj} = v_T \frac{\mathfrak{F}_{1/2}\left(\frac{E_F - E_1}{kT}\right)}{\mathfrak{F}_0\left(\frac{E_F - E_1}{kT}\right)} \quad (9)$$

where we have simplified the expression using the following definitions:

$$v_T = \sqrt{\frac{2kT}{\pi m^*}} \quad (10)$$

$$\mathfrak{F}_{1/2}(x) = \frac{2}{\sqrt{\pi}} \int_0^{\infty} \frac{\sqrt{\varepsilon}}{1 + e^{\varepsilon - x}} d\varepsilon \quad (11)$$

where  $v_T$  is the thermal velocity,  $\mathfrak{F}_{1/2}$  is the Fermi-Dirac integral of order one-half, and:

$$\varepsilon = \frac{E - E_1}{kT} \quad (12)$$

Combining Eqs. 3, 6 and 9 yields the final expression for the drain current:

$$I_D = qN_{2D}v_T\mathfrak{F}_{1/2}\left(\frac{E_F - E_1}{kT}\right) \quad (13)$$

The Fermi-Dirac integrals for both  $n_s$  and  $v_{inj}$  can be simplified in the non-degenerate limit where  $\frac{E_F - E_1}{kT} \ll 1$  to give a much simpler expression for the drain current. However, the HEMT operates in degenerate conditions where the Fermi level is close to or above the first sub-band  $E_1$ , and therefore we cannot take the non-degenerate limit of these expressions.

Measurements or predictions of the drain current,  $I_D$ , are important when studying both the output and transfer characteristics of a HEMT for logic purposes. Therefore, it is vital to have a

working model of  $I_D$  to provide a basis for understanding experimental data and for verifying that the theory adequately describes the observed behavior.

### 2.2.2 Gate Capacitance

In order to continue building our theoretical model of the HEMT, we need to consider the effects of capacitance on our gate voltage. The effects of insulator capacitance, as well as inversion-layer and parasitic capacitances, are considered by del Alamo [9].

In Figure 2-3,  $C_{ins}$  is the capacitance arising from the HEMT insulator layer,  $C_D$  is a linear capacitance to account for short channel effects,  $\phi_s$  is the surface potential at the barrier-channel interface as defined in Figure 2-1, and  $C_S$  is a non-linear capacitance related to the inversion layer in the channel:

$$C_S = q \frac{dn_s}{d\phi_s} \quad (14)$$

Since the charge across  $C_{ins}$  is equal to the charge across  $C_S$  and  $C_D$  in parallel, we can write an expression for the charge on the gate,  $Q_G$ :

$$Q_G(\phi_s) = \int_0^{\phi_s} [C_S(\phi_s) + C_D] d\phi_s \quad (14)$$

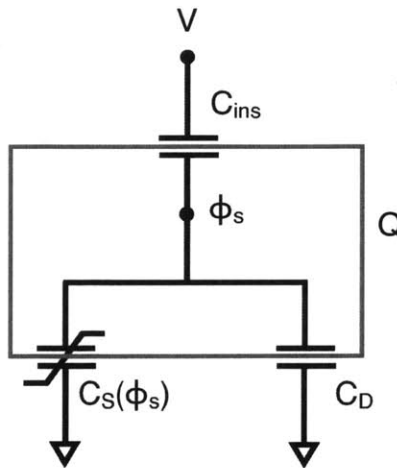


Figure 2-3 Model of the different factors that contribute to gate capacitance.

Then, the voltage applied to the gate,  $V_{GS,i}$ , can be written as:

$$V_{GS,i} = \phi_s + \frac{Q_G}{C_{ins}} = \phi_s \left( 1 + \frac{C_D}{C_{ins}} \right) + \frac{1}{C_{ins}} \int_0^{\phi_s} C_S(\phi_s) d\phi_s \quad (15)$$

With the theoretical models in Sections 2.2.1 and 2.2.2, we have a complete set from which to obtain current-voltage characteristics. These models have actually been validated by experiment [3]. In Figure 2-4, the I-V characteristics of a 30 nm InAs-channel HEMT are shown against the model developed above. Even though the models are a starting point for further development, we can already see that they match experimental data over several orders of magnitude.

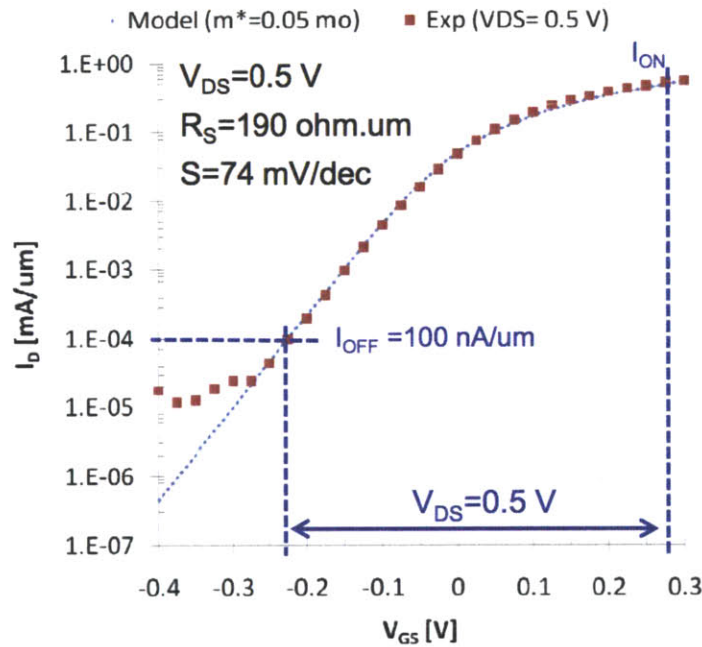


Figure 2-4 I-V characteristics of a 30 nm InAs HEMT compared with the HEMT theoretical model, reproduced from [11].

### 2.3 I-V Model for HEMT

As we have seen, we already have a foundation for a ballistic model that does quite well. However, there are many effects that have not been fully explored by this model. We have not yet considered the impact of the drain, which will be significant especially in the linear regime. There are additional effects, such as source and drain parasitics, heating in the device, the impact

of effective mass on device characteristics, and others, that we will consider here with the aim of building upon the previous work.

### 2.3.1 Simulation Process Flow

Before a detailed discussion on the work in this thesis can proceed, it is worthwhile to give brief mention to the simulation process flow that yields the results that will be compared with experimental data. Given knowledge of a HEMT heterostructure, we can model the device using a self-consistent Poisson-Schrödinger solver that we have chosen to be nextnano, which yields the charge-voltage characteristics of a one-dimensional structure. From the Poisson-Schrödinger simulator, we can extract information about the band structure of the device and pull such values as the surface potential and location of the quantized energy bands with respect to the Fermi level, as show in Figure 2-5. Extrinsic device parameters, such as parasitic source and drain resistances or DIBL, can be defined separately, and all components serve as input to the device model, constructed in MATLAB, that yields the sought-after transfer or output characteristics. We will now discuss the additions to the previous work, which covers both further intrinsic theory and the inclusion of extrinsic parameters.

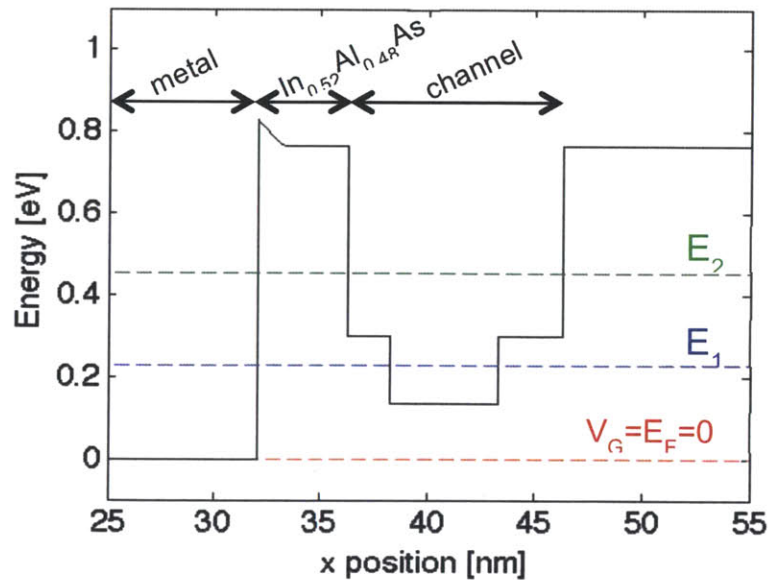


Figure 2-5 Conduction band simulation of a HEMT in nextnano under flatband conditions, with  $V_{GS}=0$ . The conduction band (black) as well as the quantum sub-bands  $E_1$  and  $E_2$  (blue and green) is plotted with respect to the Fermi level (red).

### 2.3.2 Impact of the Drain on $n_s$ and $v_{inj}$

For high values of the drain-to-source voltage  $V_{DS}$ , we need not be concerned about any impact that the drain may have on the source injection velocity and sheet carrier concentration,  $v_{inj}$  and  $n_s$  respectively. However, in the linear regime when  $V_{DS}$  is relatively small, electrons injected from the drain that oppose the direction of current flow can have a significant impact on the current. One way to think of the current is to consider it as the difference between fluxes in opposite directions [12]. One flux originates at the source, and the other at the drain and in the ballistic case, there will be no reflection. The charge density  $n_s$  will be the sum of the charge densities at these two points, but the velocity at the drain will have the opposite sign because electrons injected from the drain will oppose the overall flow of current.

We have to first obtain an expression for the overall charge density  $n_s$  at the virtual source point. We have the original contribution from the source to the charge density as given in (3), but we now have to add the charge that the drain will contribute at the virtual source point. This has a similar form as (3) but the potential is modified by a term for the intrinsic drain voltage  $V_{DS,i}$ . The sum of these two densities results in an overall expression for  $n_s$  given by:

$$n_s = N_{2D} \left\{ \mathfrak{F}_0 \left( \frac{E_F - E_1}{kT} \right) + \mathfrak{F}_0 \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right) \right\} \quad (16)$$

We must now modify our expression for the injection velocity. Using (8) we can write the injection velocity of the source electrons as:

$$v_{inj,source} = v_T \left\{ \frac{\mathcal{F}_{1/2} \left( \frac{E_F - E_1}{kT} \right)}{\mathfrak{F}_0 \left( \frac{E_F - E_1}{kT} \right) + \mathfrak{F}_0 \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)} \right\} \quad (17)$$

As with  $n_s$ , the injection velocity of electrons from the drain will contribute a term to the virtual source point, again with a term that accounts for  $V_{DS,i}$ . However, the direction of these electrons will be opposite to that of those from the source:

$$v_{inj,drain} = -v_T \left\{ \frac{\mathcal{F}_{1/2} \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)}{\mathfrak{F}_0 \left( \frac{E_F - E_1}{kT} \right) + \mathfrak{F}_0 \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)} \right\} \quad (18)$$

giving a net injection velocity:

$$v_{inj} = v_T \left\{ \frac{\mathcal{F}_{1/2} \left( \frac{E_F - E_1}{kT} \right) - \mathcal{F}_{1/2} \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)}{\mathfrak{F}_0 \left( \frac{E_F - E_1}{kT} \right) + \mathfrak{F}_0 \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)} \right\} \quad (19)$$

We recognize that the denominator is simply the expression for  $n_s$  divided by the constant  $N_{2D}$ , and so can write  $v_{inj}$  in the following way:

$$v_{inj} = N_{2D} v_T \left\{ \frac{\mathfrak{F}_{1/2} \left( \frac{E_F - E_1}{kT} \right) - \mathfrak{F}_{1/2} \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right)}{n_s} \right\} \quad (20)$$

Using this identity, therefore, the current through the channel will only be modified by the addition of the new term in the numerator of  $v_{inj}$ :

$$I_D = qN_{2D} v_T \left\{ \mathfrak{F}_{1/2} \left( \frac{E_F - E_1}{kT} \right) - \mathfrak{F}_{1/2} \left( \frac{E_F - E_1 - qV_{DS,i}}{kT} \right) \right\} \quad (21)$$

### 2.3.3 Parasitic Resistances: Source, Drain, and Access

The value of the drain-to-source voltage used in the calculations for  $n_s$  and  $v_{inj}$  was the intrinsic drain-to-source voltage,  $V_{DS,i}$ . Similarly, the gate-to-source voltage given by the gate capacitance model is also the intrinsic  $V_{GS,i}$  and therefore to compare against experimental data we need to be able to make the conversion to external  $V_{GS}$  and  $V_{DS}$ , as those are the values applied across the entire device in experiment. The difference between the intrinsic and extrinsic voltages arises from the presence of parasitic source and drain resistances. We will break each of these down into two components: a constant term that does not change with channel current, and a variable resistance in the access region. Figure 2-6 shows a cross-section for the HEMT structure, where we have defined all four terms.  $R_{CS}$  and  $R_{CD}$  are the constant resistances associated with the source and drain respectively, and  $R_{access}$  is a symmetric resistance occurring on both sides of the channel in the access region. We can define overall source and drain resistances as:

$$R_S = R_{CS} + R_{access} \quad (22)$$

$$R_D = R_{CD} + R_{access} \quad (23)$$

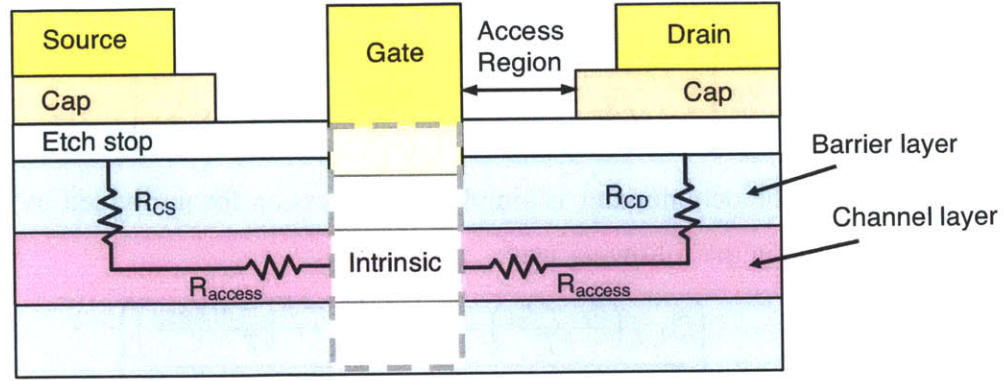


Figure 2-6 Cross-section of a simplified HEMT device.  $R_S$  and  $R_D$  are defined between the source and drain, and  $R_{access}$  is symmetric on both sides of the intrinsic region.

It is clear from Figure 2-6 that the access region is not modulated in any way by the gate. Therefore, we would expect that the location of the Fermi level with respect to the first quantum sub-band in the access region would not change, and we can find this value by completing Poisson-Schrödinger simulations for the access region. There is no Schottky barrier because there is no metal layer on top of the access region heterostructure, but Fermi level pinning at the heterostructure surface can be modeled as a Schottky barrier whose height is the location of the pinning in the semiconductor band gap relative to the conduction band edge. We will assume that the behavior of electrons in the access region is ballistic, just as in the channel, so therefore to find expressions for the current and the voltage drop in the access region we use the same approach as we do in the intrinsic region.

We can use Eq. (21), but instead of a drain-to-source voltage drop  $V_{DS,i}$ , we now just have the voltage drop across the access region,  $V_{access}$ :

$$I_{access} = qN_{2D}v_T \left\{ \mathfrak{F}_{1/2} \left( \frac{[E_F - E_1]_{access}}{kT} \right) - \mathfrak{F}_{1/2} \left( \frac{[E_F - E_1]_{access} - qV_{access}}{kT} \right) \right\} \quad (24)$$

$V_{access}$  is an unknown, but we use the fact that the current in the channel must be the same as the current in the access region, so for a given value of the current in the channel we can find  $V_{access}$ . It is trivial from here to find  $R_{access}$ .

Having found an expression for  $R_{\text{access}}$ , we can now define the extrinsic gate- and drain-to-source voltages.  $R_{\text{CS}}$  and  $R_{\text{CD}}$  will be values that can be set by the user. The current running through these resistances contributes extra voltage terms and therefore, the values of  $V_{\text{DS}}$  and  $V_{\text{GS}}$  are simply given by:

$$V_{\text{GS}} = V_{\text{GS},i} + I_D R_S \quad (25)$$

$$V_{\text{DS}} = V_{\text{DS},i} + I_D (R_S + R_D) \quad (26)$$

### 2.3.4 Non-parabolic Band Structure

In the previous equations for sheet carrier concentration and injection velocity, we have assumed that the conduction bands in the materials were completely parabolic—that is to say, that the effective mass is constant as a function of energy. It is known, however, that the effective mass of electrons in the conduction band of III-Vs is not perfectly parabolic [13]. In order to account for this change in effective mass as the energy of the electron moves up farther into the conduction band, therefore, the effective mass can be modeled as:

$$m^* = m_0^* (1 + 2\alpha E) \quad (27)$$

where  $m_0^*$  is the electron effective mass at the bottom of the conduction band,  $E$  is the difference in energy between the electron and the bottom of the conduction band, and  $\alpha$  is a non-parabolicity factor that signifies the departure from ideal behavior. It is easy to see that now, the term for effective mass further complicates the integrals for  $n_s$  and  $v_{\text{inj}}$ . Instead, the expression for  $n_s$  from the source must become:

$$n_{s,\text{source}} = \int_{E_1}^{\infty} g_{2D}(E) f(E) dE = \frac{m_0^*}{\pi \hbar^2} \int_{E_1}^{\infty} \frac{(1 + 2\alpha E) dE}{1 + e^{\frac{E - E_F}{kT}}} \quad (28)$$

which simplifies to:

$$n_{s,source} = N_{2D}(1 + 2\alpha E_1)\mathfrak{F}_0\left(\frac{E_F - E_1}{kT}\right) + 2\alpha kTN_{2D}\mathfrak{F}_1\left(\frac{E_F - E_1}{kT}\right) \quad (29)$$

This leads to a similar expression for  $n_s$  from the drain:

$$n_{s,drain} = N_{2D}(1 + 2\alpha E_1)\mathfrak{F}_0\left(\frac{E_F - E_1 - qV_{DS}}{kT}\right) + 2\alpha kTN_{2D}\mathfrak{F}_1\left(\frac{E_F - E_1 - qV_{DS}}{kT}\right) \quad (30)$$

The total sheet carrier concentration is again just the sum of  $n_{s,source}$  and  $n_{s,drain}$ . Now we can see that there is no simple analytical solution for even the sheet carrier concentration, and the expression must be evaluated numerically. The same approach to the injection velocity yields:

$$v_{inj} = \frac{2}{\pi^2 \hbar^2} \frac{1}{n_s} \left\{ \int_{E_1}^{\infty} \frac{\sqrt{2m_0^*(1 + 2\alpha E)(E - E_1)}}{1 + e^{\frac{E - E_F}{kT}}} dE - \int_{E_1}^{\infty} \frac{\sqrt{2m_0^*(1 + 2\alpha E)(E - E_1)}}{1 + e^{\frac{E - E_F + qV_{DS}}{kT}}} dE \right\} \quad (31)$$

This finally gives the new drain current:

$$I_D = \frac{2q}{\pi^2 \hbar^2} \left\{ \int_{E_1}^{\infty} \frac{\sqrt{2m_0^*(1 + 2\alpha E)(E - E_1)}}{1 + e^{\frac{E - E_F}{kT}}} dE - \int_{E_1}^{\infty} \frac{\sqrt{2m_0^*(1 + 2\alpha E)(E - E_1)}}{1 + e^{\frac{E - E_F + qV_{DS}}{kT}}} dE \right\} \quad (32)$$

### 2.3.5 Drain-Induced Barrier Lowering

For short channel devices, it has been experimentally observed that as the value of the drain-to-source voltage,  $V_{DS}$ , increases, the threshold voltage of the device decreases [14]. This behavior has the consequence of a non-zero output conductance in the saturation regime. One of the causes of this output conductance is a phenomenon known as drain-induced barrier lowering (DIBL), where the barrier that electrons see at the source end of the channel is reduced as  $V_{DS}$  increases, thus allowing a larger number of electrons to be injected into the channel [15].

Though DIBL is not a linear phenomenon and there are more complex expressions to capture its behavior [16], we will model the effect of DIBL as a linear shift of the threshold voltage with increasing  $V_{DS}$ . This can be achieved by incrementally changing the surface potential:

$$\phi_s = \phi_{s,nextnano} - DIBL * V_{DS,i} \quad (33)$$

### 2.3.6 Self-heating

For a given value of current through the channel, we would expect a finite thermal resistance to demand an increase in temperature from that of the device in the off state. Through the use of Monte Carlo simulations for other HEMT structures [17], a varying a temperature profile is demonstrated and can be seen in Figure 2-7. We must therefore consider the effects of heating in the device and its effect on the transfer and output characteristics.

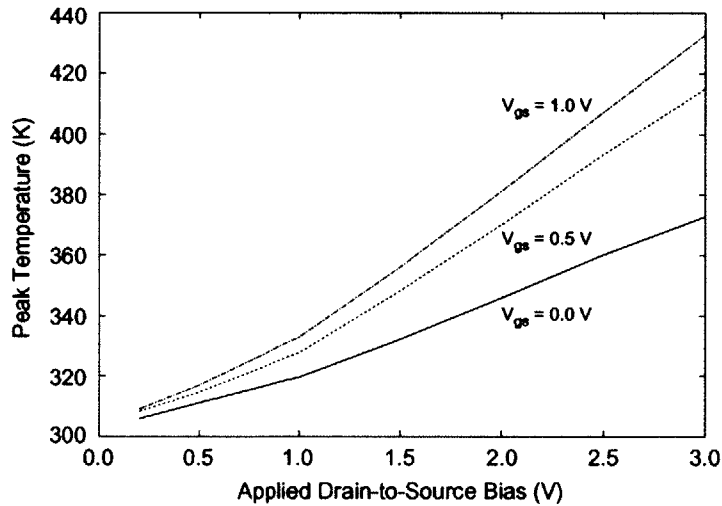


Figure 2-7 Variation of peak temperature as a function of  $V_{DS}$  and  $V_{GS}$ , reproduced from [17].

There is no straightforward approach to addressing the issue of heating in the device, so what we implement instead is a series of Poisson-Schrödinger simulations at varying temperatures. With a user-defined thermal resistivity, we can iteratively find the right combination of current and given temperature by interpolating between the results of the different simulations.

### 2.3.7 Ballistic Factor

Though for shorter gate lengths it has been shown that devices operate close to the ballistic limit [3], for wider applicability of the model for longer gate lengths, we consider the possibility that the HEMT may not be entirely ballistic. We can modify the current by means of a so-called ballisticity factor. The ballisticity factor  $B$ , introduced by Lundstrom [18], is the ratio of the actual current in the device divided by its ballistic current:

$$B = \frac{I_D}{I_{D,ballistic}} \quad (34)$$

The ballisticity factor can be determined from the backscattering coefficient  $r$ :

$$B = \frac{1 - r}{1 + r} \quad (35)$$

where  $r$  follows also a rather simple expression:

$$r = \frac{\ell}{\ell + \lambda} \quad (36)$$

$\ell$  is denoted as a critical length for backscattering [19], whose value is given by the length it takes for the potential to drop by  $(kT/q)$  from the top of the barrier to the channel.  $\lambda$  is the carrier momentum relaxation length, which is valid even in high-bias conditions because the field at the source can be considered small and slowly varying. We concern ourselves primarily here with the ballistic current in the saturation regime.

We will first discuss the carrier momentum relaxation length  $\lambda$ . The expression for  $\lambda$  in non-degenerate conditions is a rather simple expression that depends on both the mobility and  $v_T$ , the thermal velocity (Eq. 10), but we must go further and consider the degenerate conditions under which a HEMT operates. In this scenario, we cannot simplify the Fermi-Dirac integrals to solely exponential expressions. With the electric field close to zero at the source end of the channel, the diffusive limit in combination with McKelvey's flux method yields the degenerate momentum relaxation length [12]:

$$\lambda = \left( \frac{2\mu kT}{v_T q} \right) \frac{\left\{ \mathfrak{I}_0 \left( \frac{E_F - E_1}{kT} \right) \right\}^2}{\mathfrak{I}_{-1} \left( \frac{E_F - E_1}{kT} \right) \mathfrak{I}_{1/2} \left( \frac{E_F - E_1}{kT} \right)} \quad (37)$$

Unfortunately, there is no simple analytical solution for the length of the kT-layer  $\ell$ . We are left, then, to approximate this value using a simplified form of the potential in the channel from source to drain [16]:

$$\eta(x) = \frac{\eta_S \sinh \left( \frac{L_G - x}{\lambda_{sl}} \right) + \eta_D \sinh \left( \frac{x}{\lambda_{sl}} \right)}{\sinh \left( \frac{L_G}{\lambda_{sl}} \right)} \quad (38)$$

where  $L_G$  is the gate length,  $\eta_S$  is the height of the potential barrier seen from the source to the channel, and:

$$\eta_D = \eta_S + V_{DS} \quad (39)$$

$\lambda_{sl}$  is the natural scale length of the potential and will be discussed momentarily.  $\eta$ ,  $\eta_S$ , and  $\eta_D$  are not to be confused with the surface potential  $\phi_s$ , but are in fact related to the surface potential in the following way:

$$\eta_S = -\phi_{schannel} + \phi_{ssource} \quad (40)$$

The potential profile looks parabolic, as is shown in Figure 2-8.

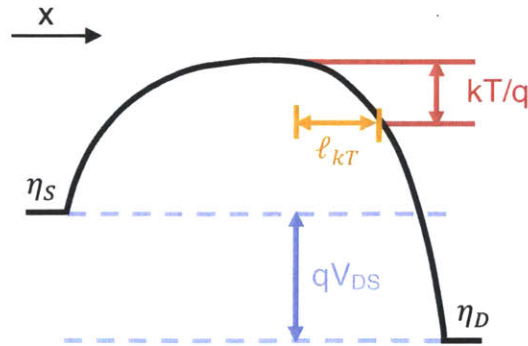


Figure 2-8 Potential profile from source to drain for large  $V_{DS}$ . The potential drop of  $(kT/q)$  is labeled in red with the corresponding kT-layer  $\ell$  in orange.

$\lambda_{sl}$ , the natural scale length of the potential, is a characteristic length of the channel and is given by [20]:

$$\lambda_{sl} = \sqrt{\frac{\epsilon_{chan}}{\epsilon_{ins}} t_{chan} t_{ins}} \quad (41)$$

Here, we have modified the more conventional expressions for silicon MOSFETs to be applicable to the HEMT.  $t_{ins}$  is the thickness of the barrier layer, and  $t_{chan}$  is the thickness of the entire channel. Because the channels in HEMTs are often a composite of a higher-mobility core surrounded by lower-mobility cladding for the purposes of lattice matching, we have weighted the dielectric constant of the channel by the proportions of the charge in the core and cladding layers:

$$\epsilon_{chan} = \frac{n_{s,cladding}}{n_{s,cladding} + n_{s,core}} \epsilon_{cladding} + \frac{n_{s,core}}{n_{s,cladding} + n_{s,core}} \epsilon_{core} \quad (42)$$

It is clear that the expression for the channel potential will change as a function of drain bias, but it will also change as a function of gate bias because the barrier to the channel will be lowered as the gate voltage increases. From (38), we could analytically find an expression for the value of  $x$  for which the potential peaks and then find the length at which it drops by a factor of  $(kT/q)$ , but we have found it is much simpler to find this value numerically. Then we will have both components we need to calculate the backscattering coefficient  $r$  and the ballisticity factor  $B$ .

## ***2.4 III-V MOSFET: Additions to the HEMT Model***

Having discussed the ballistic transport model in context of a HEMT, we will now turn our attention to the additions we must make for the III-V MOSFET. The MOSFET differs from the HEMT in that there is an oxide layer inserted between the metal and the semiconductor. There are two different types of MOSFETs: surface-channel MOSFETs, where the oxide is directly on top of the channel, and buried-channel MOSFETs, where an additional barrier layer is inserted between the channel and the oxide. The presence of an oxide in the heterostructure also introduces traps at the oxide interface that degrade device performance. In this section, we will

discuss the effects of these traps, and how the gate capacitance will change as a result. We will consider both the surface-channel and buried-channel designs.

### 2.4.1 Interface State Traps

A persistent problem in III-V MOSFETs is the presence of interface traps at the surface between the semiconductor and the oxide. Interface traps can play an important role in the subthreshold characteristics of an FET, as well as shift the threshold voltage.

To model the interface states, we can define our own distribution of trap states,  $D_{it}$ , as a function of energy, as shown in Figure 2-9. We can find the total charge accumulated in those traps by integrating across the distribution and accounting for occupation probabilities given by the Fermi-Dirac distribution function. Thus, the charge from interface states can be written as:

$$Q_{it} = q \int_{-\infty}^{\infty} D_{it}(E) f(E) dE \quad (43)$$

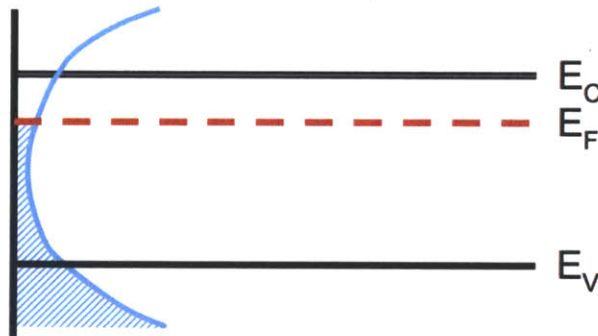


Figure 2-9  $D_{it}$  across the energy gap, shown in blue. The filled states are those below the Fermi level.

In actuality, there can be two types of interface states: donor states and acceptor states. Both states are filled as the Fermi level sweeps upwards towards the conduction band. However, acceptor states are neutral until they take an extra electron as they are filled, leaving the states negatively charged as the Fermi level passes through them. This will cause a positive  $V_T$  shift, relative to a case with no  $D_{it}$ . Conversely, donor states naturally give up an electron, making them positively charged until the Fermi level reaches them and they become neutral. Therefore,

donor states cause a negative  $V_T$  shift until the Fermi level sweeps through them and they become neutral.

The presence of charge from interface states can be described as a parasitic capacitance that will affect the gate capacitance of the system. The differential capacitance arising from  $D_{it}$  can be written as:

$$C_{it} = \frac{dQ_{it}}{d\phi_{it}} \quad (44)$$

$Q_{it}$  is the value obtained in (41), and  $\phi_{it}$  is the potential at the location of the interface traps. As we will see shortly,  $\phi_{it}$  is identical to  $\phi_s$  in a surface-channel MOSFET, where the edge of the channel is the semiconductor-oxide interface where the traps occur. With a buried-channel MOSFET, the two potentials are not the same, and we will discuss this in further detail in Section 2.4.3.

### 2.4.2 Surface-Channel MOSFET

The addition of  $C_{it}$  will change the gate capacitance model by adding another capacitance in parallel with the existing  $C_S$  and  $C_D$ , as shown in Figure 2-10. The traps are located at the interface between the channel and the gate oxide.

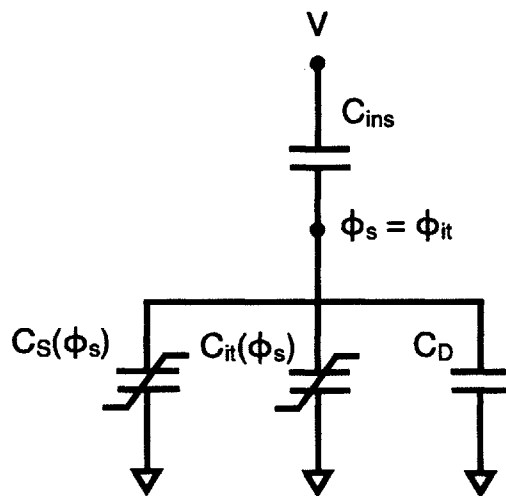


Figure 2-10 Gate capacitance model for surface-channel MOSFET.  $C_S$ ,  $C_D$ , and  $C_{it}$  are as previously defined, and  $C_{ins}$  is the oxide capacitance.

As mentioned earlier, with a surface-channel MOSFET the channel interfaces directly with the oxide. Therefore, it is clear that  $\phi_{it}$  should be the same as  $\phi_s$ . We can write a new expression for the charge on the gate that incorporates the effects of  $C_{it}$ :

$$Q_G(\phi_s) = \int_0^{\phi_s} [C_S(\phi_s) + C_{it}(\phi_s) + C_D] d\phi_s \quad (45)$$

This yields a total voltage on the gate of:

$$\begin{aligned} V_{GS,i} &= \phi_s + \phi_s \frac{C_D}{C_{ins}} + \frac{1}{C_{ins}} \int_0^{\phi_s} [C_S(\phi_s) + C_{it}(\phi_s)] d\phi_s \\ &= \phi_s + \frac{1}{C_{ins}} (qn_s + \phi_s C_D + Q_{it}) \end{aligned} \quad (46)$$

### 2.4.3 Buried-Channel MOSFET

The presence of a barrier layer between the oxide and the channel can offer various advantages to the performance of a III-V MOSFET, and it is for that reason that MOSFETs are often designed with a buried-channel structure such as that in [6]. This separates the interface states from the channel, and helps to reduce scattering. The buried-channel design leads to a gate capacitance model like the one shown in Figure 2-11.

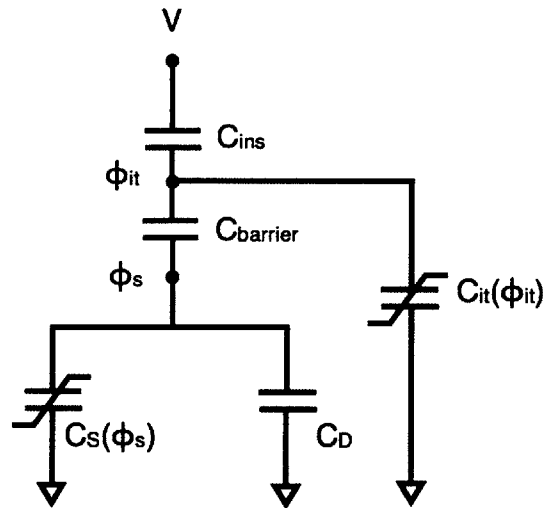


Figure 2-11 Gate capacitance model for buried-channel MOSFET. Capacitances are as previously defined, and  $C_{\text{barrier}}$  is due to the barrier layer between the channel and oxide.

The interface traps manifest in a different location in the buried-channel MOSFET because they always occur at the semiconductor-oxide interface. With the surface-channel MOSFET this happened to be at the surface of the channel, but with the buried-channel design it is at the edge of the barrier and so  $\phi_{it}$  is no longer the same as  $\phi_s$ . Therefore, the derivation of the gate voltage  $V_{GS,i}$  becomes more complicated. The charge across the barrier layer is equal to the sum, in parallel, of the charge across  $C_S$  and  $C_D$ , and can be found as:

$$Q_{barrier}(\phi_s) = \int_0^{\phi_s} [C_S(\phi_s) + C_D] d\phi_s \quad (47)$$

If we remember that the charge accumulated in the interface traps is  $Q_{it}$ , then the total charge on the gate becomes:

$$Q_G(\phi_s, \phi_{it}) = Q_{it}(\phi_{it}) + Q_{barrier}(\phi_s) \quad (48)$$

And thus,  $V_{GS,i}$  can be written as:

$$V_{GS,i} = \phi_s + \frac{Q_{barrier}}{C_{barrier}} + \frac{Q_G}{C_{ins}} \quad (49)$$

which yields:

$$V_{GS,i} = \phi_s + \frac{1}{C_{barrier}} (qn_s + \phi_s C_D) + \frac{1}{C_{ins}} (Q_{it} + qn_s + \phi_s C_D) \quad (50)$$

We have now developed a methodology for finding the charge from interface states, and accounting for their behavior in both surface-channel and buried-channel MOSFET designs. This, then, completes our considerations for the additions that need to be made to the model in order to accurately describe III-V MOSFET behavior.

## 2.5 Summary

In this chapter, we have introduced the ballistic transport model for quantum-well FETs that is the basis for a study of experimental data of MOSFETs and HEMTs. We have then extended this model to various first-order effects that will have a significant impact upon the I-V characteristics of this model. We have also discussed theory specific to HEMTs and III-V

MOSFETs in turn. In the following chapters, we will discuss the results of our ballistic transport modeling, and in comparing them against the experimental work, gain insight into the behavior of these FETs and the areas in which we should extend our model further.



# CHAPTER 3. SIMULATION RESULTS & EXPERIMENTAL WORK: HEMT

## 3.1 Introduction

In this chapter, we use the results of the theory in Chapter 2 to examine the output and transfer characteristics of an experimental HEMT device. We explore first the impact of several key parameters on device characteristics using the simulation environment of Ch. 2. We then compare simulations and experimental data, and detail the process and selection of extrinsic device parameters to best fit the data.

## 3.2 Device Under Study

The structure of a HEMT was explained in Chapter 1, but we reintroduce the heterostructure in Figure 3-1 so as to specify the choices made by Kim *et al.* [21], whose experimental data will be the basis upon which we make our comparison. The channel is a 5 nm layer of InAs surrounded by 2 nm and 3 nm  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  cladding layers, and the barrier layer, which is  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ , is estimated to be about 4 nm. The gate length is about 30 nm.

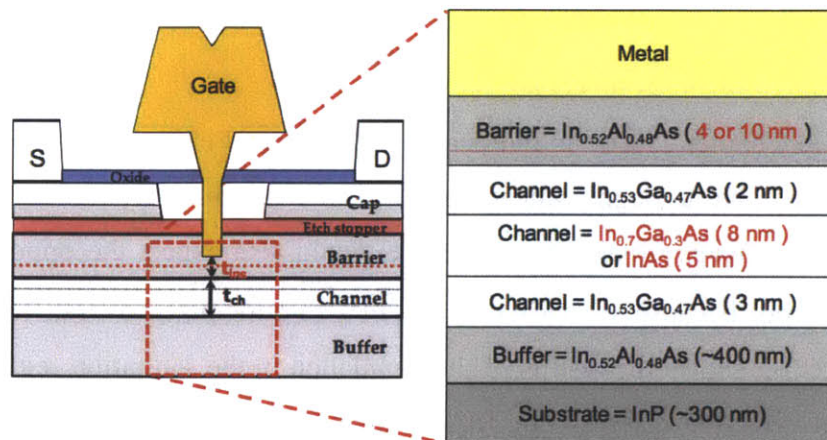


Figure 3-1 Schematic of a HEMT structure, reproduced from D. Jin *et al.* [5]

### ***3.3 Simulation Study of Parameters***

Before we do a detailed study of our simulation with respect to the experimental device characteristics, it is worthwhile first to take a look at the impact of various parameters on the simulated I-V characteristics. With this understanding, it will be easier for us to both fit the experimental data and to ultimately make meaningful conclusions about any discrepancies.

#### **3.3.1 Significance of $m^*$**

The main advantage that III-V materials possess over the more traditional silicon is their low-effective mass, leading to increased mobility and therefore the capacity to drive more current. Studies suggest, however, that the effective mass of electrons in the channel of HEMTs and other FETs is larger than that given by the bulk as a consequence of a combination of tensile strain and band non-parabolicity [5]. We must therefore consider the effective mass to be a parameter in the Poisson-Schrödinger simulations that can be increased to better fit the data and give us a sense for the real effective mass in the channel. The Poisson-Schrödinger simulations will allow us to account for any increase in the effective mass from the bulk resulting from strain, and we will treat non-parabolicity effects separately in the next section. Here, we explore the effect of varying the effective mass on the sheet carrier concentration, injection velocity, and lastly the transfer characteristics of the HEMT. We will also take a look at the impact of effective mass on the C-V characteristics, but will only consider this in the simulation regime, as experimental data are not available.

From the theory in Chapter 2, we can guess at the influence of effective mass on  $n_s$  and  $v_{inj}$ . We would expect, since  $n_s$  has a roughly linear dependence on  $m^*$ , that the sheet carrier concentration will increase as the effective mass increases. We would also expect the opposite effect on the injection velocity, but because  $v_{inj}$  varies as  $1/\sqrt{m^*}$ , an anticipated overall increase in current will result. Figure 3-2 shows the results of the simulation in the saturation regime for  $n_s$  and  $v_{inj}$  for four different effective masses. The InAs bulk value of  $0.026 m_0$  is compared to heavier values that are suspected to be closer to the actual experimental value of  $m^*$  in the channel [5].

We can see that  $n_s$  rises steadily as  $V_{GS}$  increases, with a kink at around  $V_{GS} = 0.35$ , and  $v_{inj}$  also rises steadily until this same point but then dramatically decreases. This is where the device begins to transition from the saturation to the linear regime for high values of  $V_{GS}$ , and is caused by nonzero source and drain resistances  $R_S$  and  $R_D$ . More on this behavior will be discussed in Section 3.3.3, where we investigate the impact of the parasitic resistances in detail.

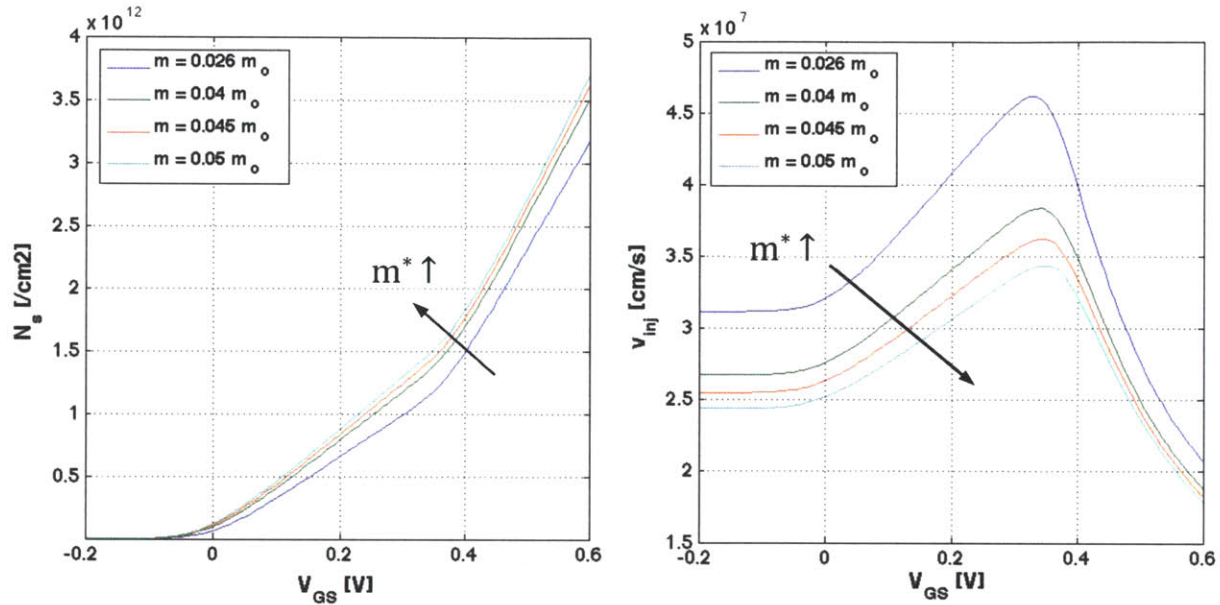


Figure 3-2 Effect of  $m^*$  on  $n_s$  (left) and  $v_{inj}$  (right). Arrows indicate direction of increasing  $m^*$ .

While the general behavior is as predicted by theory—lower  $v_{inj}$  and higher  $n_s$  for larger  $m^*$ —the actual impact on transistor characteristics is somewhat more subtle. Figure 3-3 shows the I-V transfer characteristics and  $g_m$  versus  $V_{GS}$ , as well as the C-V characteristics. The value of the  $m^*$  changes the results of the Poisson-Schrödinger simulation, in part by affecting how quickly the Fermi level sweeps upwards through the conduction band and the first quantum sub-band, but also by determining in part the location of the sub-bands themselves. The different sheet carrier concentrations with  $m^*$  also affect the calculation of the gate capacitance as we have described it, which we can see most clearly in the C-V characteristics where the higher effective masses yield a higher capacitance. The sharp rise in the C-V characteristics at high  $V_{GS}$  indicate that the second quantum sub-band is beginning to be populated. The overall result, however, is that the total drain current  $I_D$  does not change much with effective mass. What is more important is the effect on the transconductance  $g_m$ . The general shape of  $g_m$  is peaked, where  $g_m$  increases as the

transistor is driven harder into saturation but drops when the device is pushed back into the linear regime; again, we will explain this phenomenon in more detail when we consider the extrinsic parasitic resistances. Figure 3-3 shows that the smaller values of  $m^*$  give a taller and narrower  $g_m$  peak than the larger values do. Because we do not have experimental C-V characteristics,  $g_m$  will actually be the most significant determinant in our selection of the effective mass, as it is a more accurate way of determining whether or not the simulation is faithful to the rise of current in experiment.

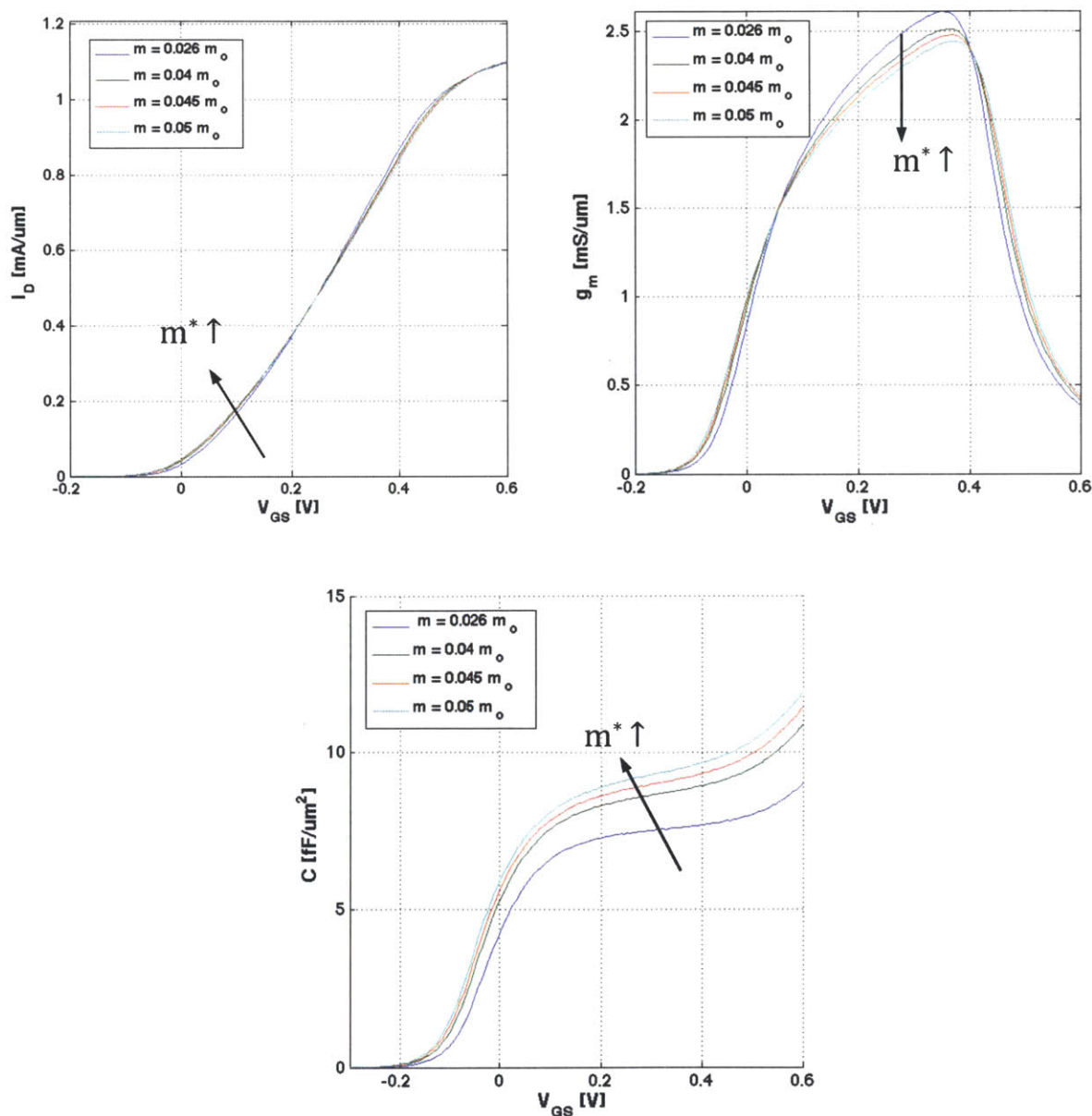


Figure 3-3 Effect of  $m^*$  on  $I_D$  (top left),  $g_m$  (top right), and gate capacitance  $C_G$  (bottom). Arrows indicate direction of increasing  $m^*$ .

### 3.3.2 Impact of Nonparabolicity

It is well-known that the electron effective mass is expected to increase as the Fermi level penetrates farther into the conduction band, and to a first order we can approximate this as a linear increase in  $m^*$  for a given energy above the conduction band [22]. We introduce a number of different values for the nonparabolicity factor  $\alpha$ , to see its effects on the transfer characteristics. In Figure 3-4, we look at  $n_s$ ,  $v_{inj}$ , and  $I_D$  as a function of  $\alpha$ . The behavior is essentially what we would expect: there is an increase in  $n_s$  and a decrease in  $v_{inj}$  for increasing values of the nonparabolicity factor, yielding an overall slight increase in the current. This is because the higher  $\alpha$  is, the larger the effective mass will be in the conduction band and therefore, the higher the current will be.

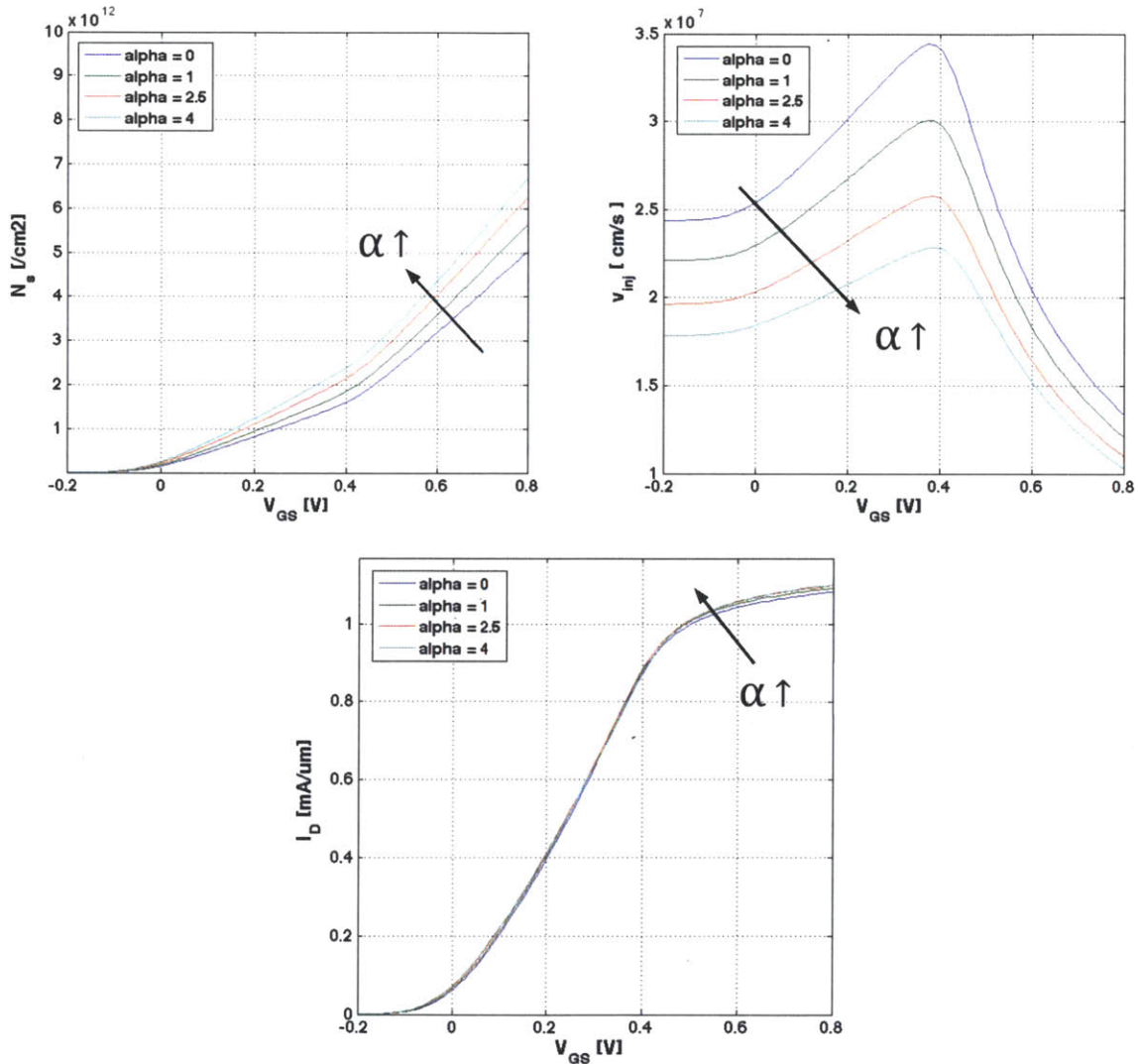


Figure 3-4 Effect of  $\alpha$  on  $n_s$ ,  $v_{inj}$ , and  $I_D$ . Arrows indicate the direction of increasing  $\alpha$ .

### 3.3.3 Effect of $R_{CS}$ , $R_{CD}$ , and $R_{access}$

Now that we have taken a look at a few parameters that affect the intrinsic behavior of the simulated device, we will turn our attention to the extrinsic parasitic resistances that will influence the I-V characteristics. The presence of these parasitics will dampen the rise of current in both the linear and saturation regimes, and we will see this clearly in both  $I_D$  and the transconductance  $g_m$ .

We show the impact of these parasitics in Figure 3-5, where we explore the effects of each resistance on the transfer characteristics one by one. To begin, we look at the transfer characteristics for  $R_{CS}$  ranging from 100 to 300  $\Omega\text{-}\mu\text{m}$ , keeping  $R_{CD}$  and  $R_{access}$  at zero. We then look at  $R_{CD}$  for the same range for zero  $R_{CS}$  and  $R_{access}$ , and finally at  $R_{access}$  for zero  $R_{CS}$ ,  $R_{CD}$ .

We see that  $R_{CS}$  and  $R_{CD}$  have substantially different effects in the saturation regime, but essentially the same effect in the linear regime. We consider the saturation regime first. The presence of a source resistance affects both the external  $V_{DS}$  and  $V_{GS}$ , but a parasitic drain resistance will affect only  $V_{DS}$ . Therefore for a given value of current,  $V_{GS}$  and  $V_{DS}$  are higher for higher  $R_{CS}$ , and this higher  $V_{GS}$  causes the I-V characteristics to stretch. Eventually,  $V_{DS}$  will become large enough to push the device out of the saturation regime and back into the linear regime, and this is what we see when the current begins to level off, and the transconductance peaks and starts to decrease. For the drain parasitic resistance  $R_{CD}$ ,  $V_{GS}$  remains unchanged and we only see the effects of  $R_{CD}$  when  $V_{DS}$  becomes large enough to suddenly push the device back into the linear regime, giving a much sharper decline to the transconductance. The same principles for  $V_{DS}$  and  $V_{GS}$  apply in the linear regime where the transfer characteristics are very similar for both  $R_{CS}$  and  $R_{CD}$ , but what we see more pronounced than any effects on  $V_{GS}$  is the fact that for higher  $R_{CS}$  or  $R_{CD}$  and thus  $V_{DS}$ , the device is pushed quickly lower into the linear regime. This dominates the behavior in the linear regime.

We would expect that the effects of access resistance  $R_{access}$  would be a combination of  $R_{CS}$  and  $R_{CD}$ , because  $R_{access}$  occurs on both the source and drain sides of the device. Indeed, that is what we see when we compare the transfer characteristics for  $R_{access}$  against those for no parasitic

resistance at all, and in fact  $R_{\text{access}}$  looks as if it is increasing for higher currents, which is the nonlinear behavior we anticipated in Section 2.3.2. Because the value of  $R_{\text{access}}$  is determined by the location of the Fermi level with respect to the first quantum sub-band in the access region (which is a fixed value for a specific heterostructure), it is not a value we can set arbitrarily as we did with  $R_{\text{CS}}$  and  $R_{\text{CD}}$ . If  $R_{\text{access}}$  is zero, and  $R_{\text{CS}}$  and  $R_{\text{CD}}$  are also both set to zero, there are no parasitic resistances present and the device will never transition from the saturation to the linear regime because the internal  $V_{\text{DS},i}$  translates directly to the external  $V_{\text{DS}}$  and is not affected by the current running through the channel.

### ***3.4 Comparison with Experimental Data***

Having examined a few of the key parameters that enter as inputs to the ballistic model, we now present a detailed comparison against experimental data. We will be using the transfer and output characteristics of the HEMT detailed in Section 3.2. This section begins with an investigation of the transfer characteristics, and having fit our model to the experimental transfer characteristics we will then change our focus to the output characteristics.

#### **3.4.1 Transfer Characteristics**

To find a good set of extrinsic device parameters, we first make a selection of the effective mass to use in our simulation. With this, we will start with the characteristics in the subthreshold regime to fit the subthreshold swing SS and DIBL, and from there we will find the combination of  $R_{\text{CS}}$  and  $R_{\text{CD}}$  that gives the best overall fit to the current and transconductance.

Before we can find the extrinsic device parameters, we choose the effective mass that we will use for the rest of this comparison. This decision is easiest when looking at the transconductance in Figure 3-6, shown for several values of effective mass versus the experimental value. We will essentially have a tradeoff between a sharper, narrower peak and a lower, wider peak.

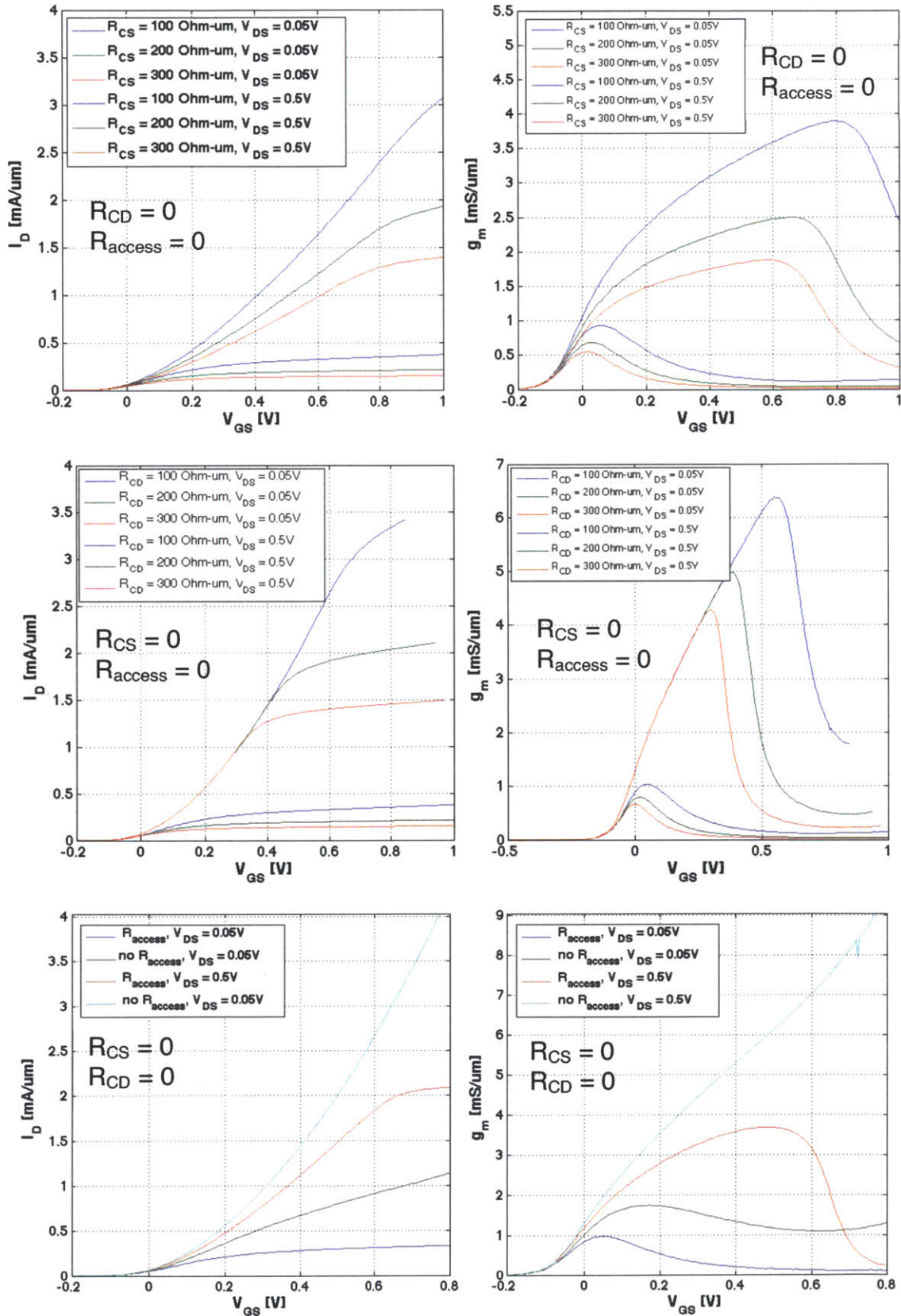


Figure 3-5  $I_D$  and  $g_m$  vs.  $V_{GS}$  for  $R_{CS} \neq 0$  (top),  $R_{CD} \neq 0$  (middle), and  $R_{access} \neq 0$  (bottom).

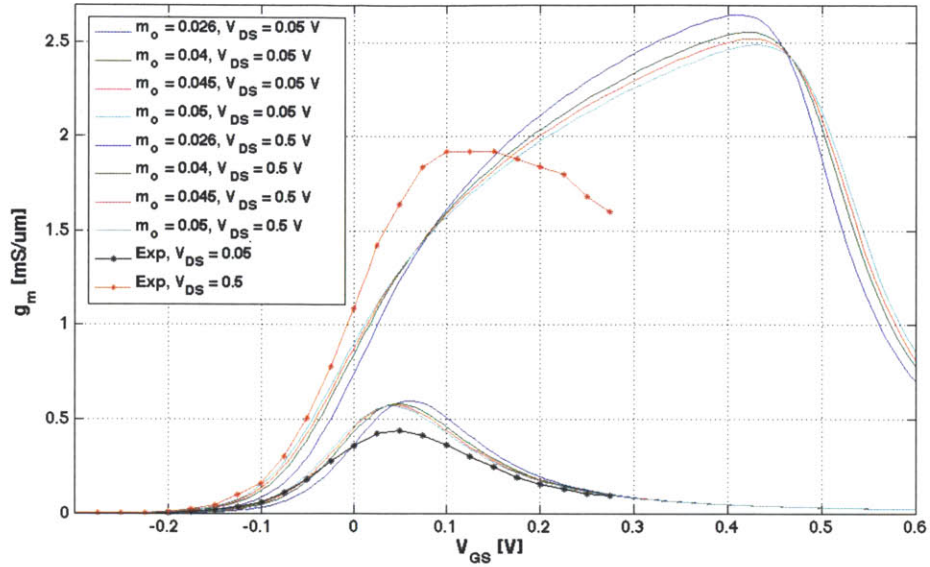


Figure 3-6  $g_m$  for several values of  $m^*$ , plotted against experimental  $g_m$ .

It becomes distinctly clear that the too-sharp characteristics from the bulk effective mass,  $0.026m_0$ , will not adequately describe the transconductance. However, for the heavier effective masses, we begin to move away from the steep rise of the experimental  $g_m$ , so it is best to choose an effective mass that can capture both the rise of  $g_m$  as well as its gentler decline. For this reason, we will select  $m^* = 0.05m_0$  to be the effective mass we use in matching the rest of the characteristics, with the expectation that an  $m^*$  that is higher will cause too much degradation in the  $g_m$  behavior. This corresponds to the value suggested in [5], and had we had the C-V characteristics available for this device, we could have used them to confirm more accurately what effective mass would have been optimal for this study.

From here, we will begin with the subthreshold characteristics of the device. This will allow us to match the subthreshold swing SS and DIBL before finding appropriate values of  $R_{CS}$  and  $R_{CD}$ . Because there are no interface states in a HEMT, we use  $C_D$ , a fixed lump capacitance to represent short channel effects covered in Section 2.2.2, to match the experimental SS of 80 mV/dec. The drain-induced barrier lowering, DIBL, will determine the spacing between the subthreshold characteristics of the linear and saturation regimes as described in Section 2.3.5. We find that the values giving the best fit in the subthreshold regime are  $C_D = 7.3$  fF/cm<sup>2</sup>, and

DIBL = 48 mV/V, as seen in Figure 3-7 which shows the subthreshold characteristics of the fitted simulation along with the experimental values.

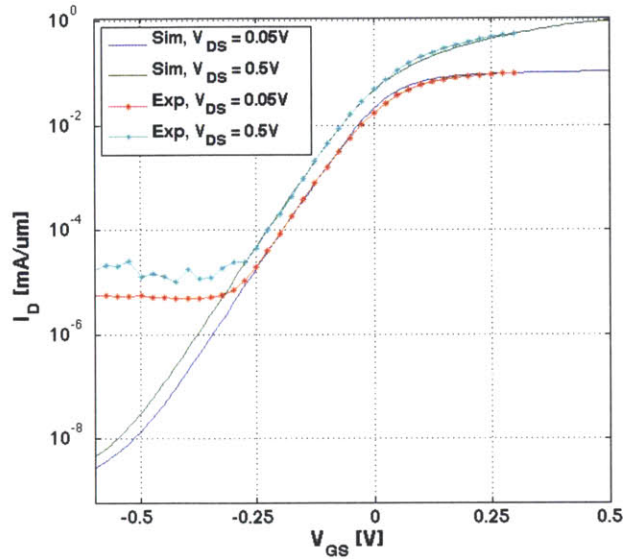


Figure 3-7 Subthreshold simulated vs. experimental data.

To find the best values of  $R_{CS}$  and  $R_{CD}$ , we fit the characteristics in the saturation regime primarily with  $R_{CS}$  because as we saw in Section 3.3.3,  $R_{CD}$  will not affect the slope of  $I_D$  in saturation. We then select a value of  $R_{CD}$  that matches best the transconductance in the linear regime. This gives values of  $R_{CS} = 60 \Omega \cdot \mu\text{m}$  and  $R_{CD} = 260 \Omega \cdot \mu\text{m}$ . Figure 3-8 shows both the I-V characteristics and  $g_m$  vs.  $V_{GS}$  for the total configuration of extrinsic device parameters. This includes the effect of  $R_{access}$ , whose value ranges from 0, to a maximum of around  $60 \Omega \cdot \mu\text{m}$  in the saturation regime. As described in Section 2.3.3,  $R_{access}$  is determined dynamically and set by both the current in the access region and the location of the Fermi level with respect to the first sub-band in the access region.

Once again, we had to consider the tradeoffs of increasing and decreasing the value of parameters, in this case  $R_{CS}$  and  $R_{CD}$ . Larger values of  $R_{CS}$  will give a peak transconductance closer to the experimental value, but will also noticeably suppress the current and give a very poor match to the I-V characteristics. Similarly, we can increase the value of  $R_{CD}$  to lower  $g_m$  in the linear regime, but if  $R_{CD}$  increases too much, the latter half of  $g_m$  becomes a progressively worse fit.  $R_{access}$  acts much in the same way as  $R_{CS}$  and  $R_{CD}$ , suppressing  $I_D$  and lowering the

peak transconductance, but because it cannot be changed we must choose values of  $R_{CS}$  and  $R_{CD}$  that account for the role that the access region plays. While the I-V characteristics match quite well, even the best fit seems to severely overestimate the peak  $g_m$  in the saturation regime, in addition to placing that peak at a much higher  $V_{GS}$  than shown in experiment.

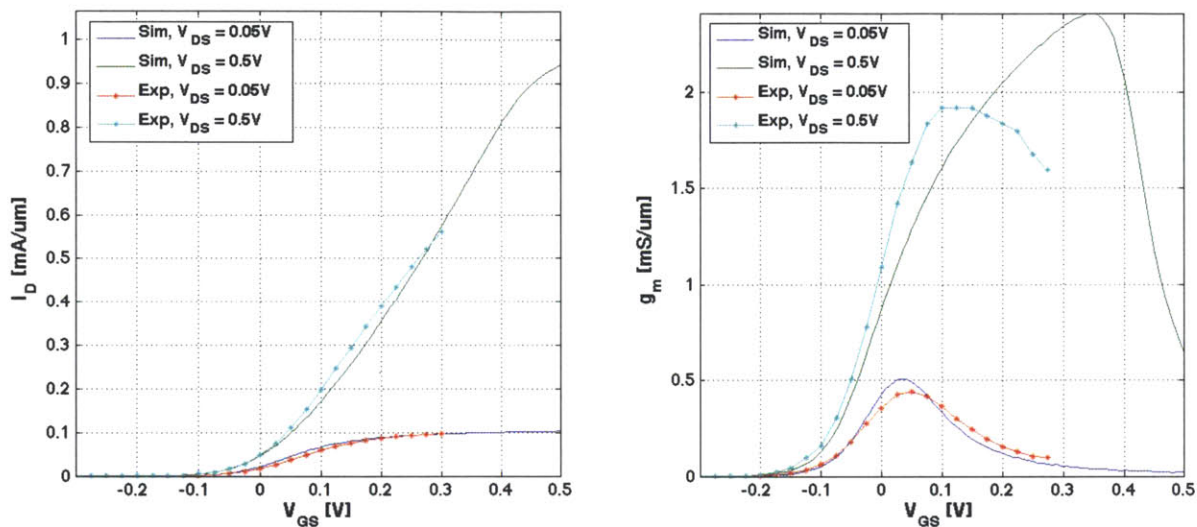


Figure 3-8 Transfer characteristics of simulation vs. experiment: I-V characteristics (left), and transconductance (right).

There are in fact several discrepancies between simulated and experimental values of extrinsic parameters. Aside from the differences we can observe on the graphs themselves, the experimental value for DIBL was obtained to be 80 mV/V, whereas the model has it to be 48. This is possibly from the oversimplified linear model we have chosen to represent DIBL; if we use a DIBL of 80 mV/V in our simulation, the separation of the saturation and linear currents in the subthreshold regime is too large. The most notable dissimilarity, however, is the imbalanced  $R_{CS}$  and  $R_{CD}$  we obtain from simulation but the balanced  $R_S = R_D = 240 \Omega \cdot \mu\text{m}$  from experiment. This suggests a need to examine in more careful detail the source and drain resistances, especially how they may change as a function of bias.

### 3.4.2 Output Characteristics

Having fit to the best of our abilities the transfer characteristics, we now examine the output characteristics. Because it is important for the model to be able to accurately capture both the output and transfer characteristics at the same time, we will use the same extrinsic device parameters to yield the results in Figure 3-9. It is immediately clear that the output conductance,  $g_o$ , of the model drastically underestimates that suggested by the experimental data. We also seem to be implementing values of  $R_{CS}$  and  $R_{CD}$  that are slightly too high, as evidenced by the slope in the linear regime that is lower than experimentally observed.

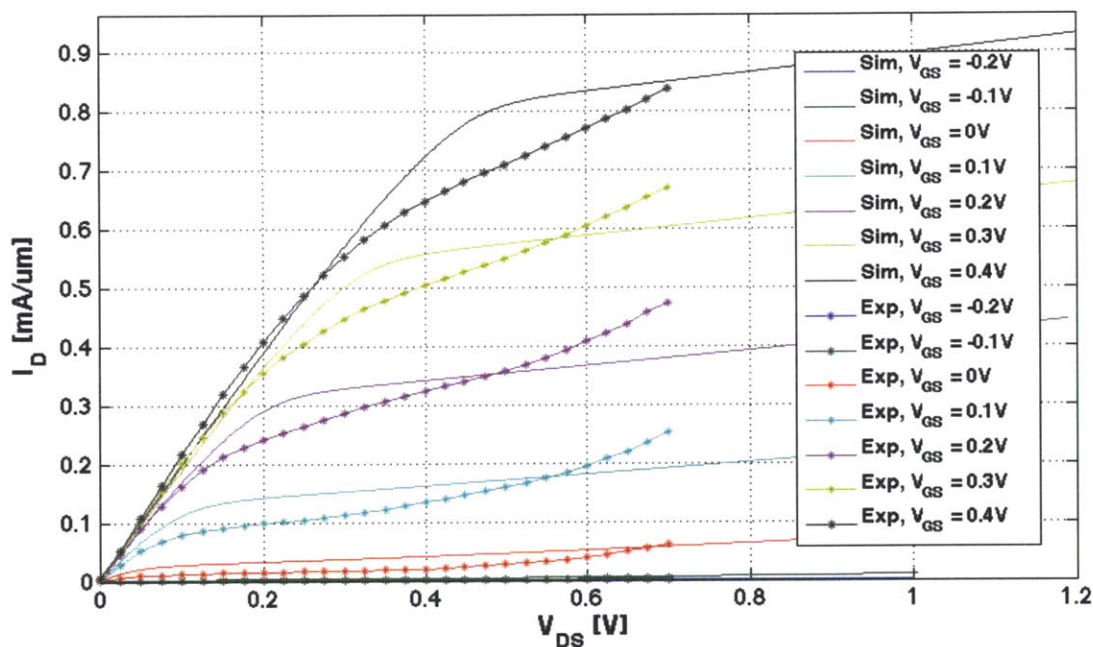


Figure 3-9 Output characteristics of simulation vs. experiment, for extrinsic device parameters extracted from transfer characteristics.

We can, in order to better understand the output characteristics, change the device parameters to achieve a better fit. This is achieved by marginally lowering the source and drain resistances, and increasing DIBL until the output conductance matches the experimental values. The results of this fitting can be seen in Figure 3-10, where we use a huge value of DIBL, 250 mV/V, to achieve the same  $g_o$  as in experiment. Unfortunately, the consequence of this measure leaves the simulated current overestimating the actual current but a large margin. The fact that DIBL needs

to be so large to come close to matching the output conductance suggests that there is some phenomenon at work that is not being accounted for in the saturation regime that has a considerable impact on the output characteristics. This will require further research.

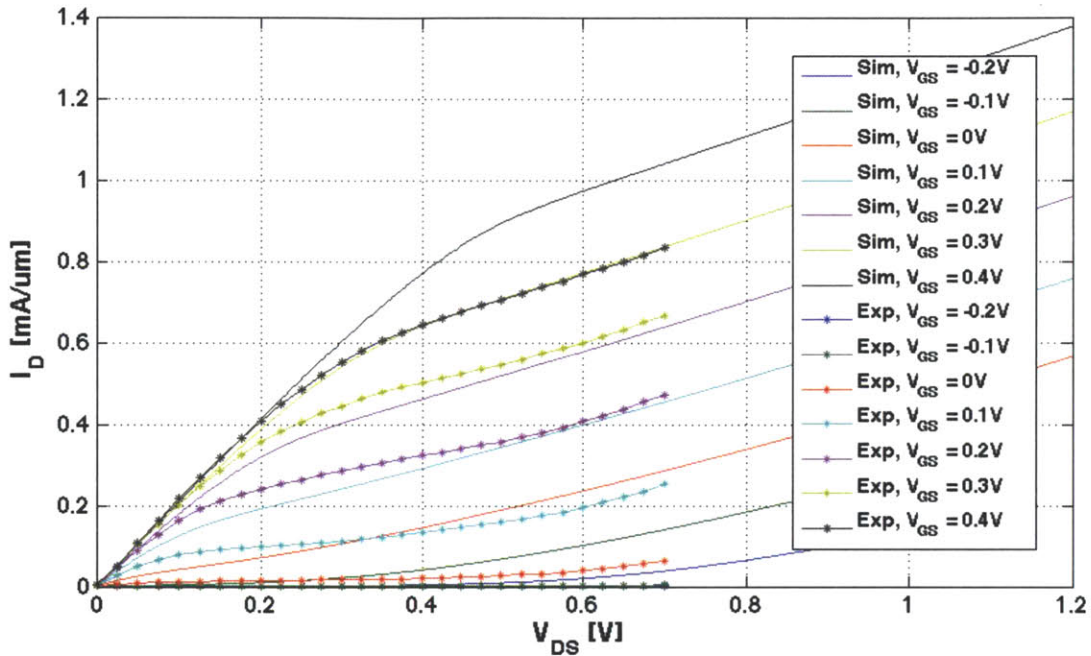


Figure 3-10 Output characteristics of simulation vs. experiment, for extrinsic parameters to match output conductance.

### 3.5 Summary

Using our theoretical ballistic model, we were able to achieve quite a good fit to the transfer characteristics of a ballistic HEMT, using components accounting for drain-induced barrier lowering, parasitic capacitances to represent short-channel effects, and parasitic source and drain resistances. The most notable discrepancies were seen in the transconductance  $g_m$  and the output characteristics, where  $g_o$  in the saturation regime suggested a much higher value of DIBL than the value obtained from the subthreshold characteristics. In the next chapter, we will focus on the III-V MOSFET, turning our attention specifically to the C-V characteristics and the impact of  $D_{it}$ .



## CHAPTER 4. C-V CHARACTERISTICS & $D_{it}$ : III-V MOSFET

### *4.1 Introduction*

In this chapter, we continue the work from Chapter 2 to explore the effects of interface traps on the behavior of III-V quantum-well MOSFETs. We first take a look at the basic principles of the quantum capacitance model, from which we can better understand the breakdown of the C-V characteristics. Then, we look explicitly at the expected effects of  $D_{it}$  on the subthreshold characteristics, as this is the final goal of using C-V to extract  $D_{it}$ . Having done so, we can move on to compare experimental and simulated C-V to obtain the distribution of interface states. This chapter concludes with a look at the sheet carrier concentration and mobility obtained independently of  $D_{it}$  using Hall effect measurements.

### *4.2 Quantum Capacitance Model*

The quantum capacitance model, detailed in [5], is briefly introduced here to better understand the components contributing to the overall gate capacitance. In Figure 4-1, we can see the gate capacitance modeled as the series combination of the insulator capacitance  $C_{ins}$  and the capacitance  $C_S$  arising from the inversion layer. The inversion-layer capacitance itself can be thought of as having a quantum capacitance  $C_{Q_i}$  and a centroid capacitance  $C_{cent_i}$ , where the contributions from each quantum sub band  $i$  sum in parallel with each other. We can think of the quantum capacitance as arising from the penetration of the Fermi level into the finite 2D density of states in the quantum well. The centroid capacitance arises from the movement of the centroid of charge in the channel as the Fermi level moves through the conduction band.

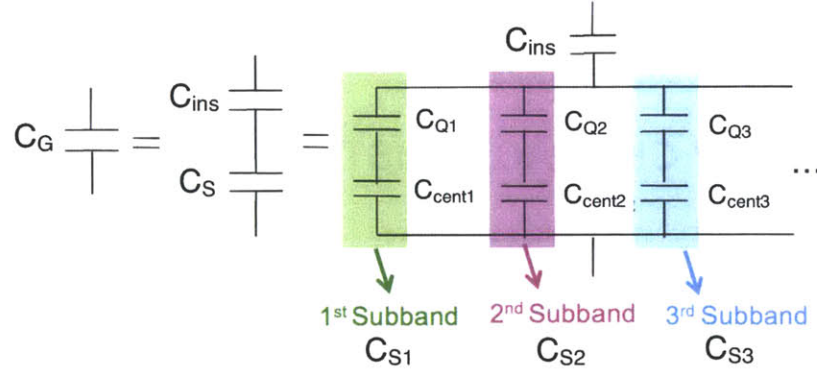


Figure 4-1 Equivalent circuit diagram for quantum capacitance modeled, from D. Jin *et al.* [5]

The overall inversion capacitance,  $C_S$ , can be written as:

$$C_S = \frac{\partial(-Q_s)}{\partial\phi_s} = \frac{q\partial(-Q_s)}{\partial(E_F - E_C)} \quad (51)$$

where  $\phi_s$  is the surface potential, and  $Q_s$  is the 2D sheet carrier concentration, which is the sum of the contributions  $Q_i$  from each sub band as found from (15) in Ch. 2.  $E_C$  is the location of the conduction band at the interface between the barrier and the channel. By breaking up the expression for the surface potential in the following way:

$$\begin{aligned} q\phi_s &= \partial(E_F - E_C) \\ &= \partial(E_F - E_i) + \partial(E_i - E_C) \end{aligned} \quad (52)$$

we can then express the inversion capacitance from one sub band as:

$$\left( \frac{q\partial(-Q_i)}{\partial(E_F - E_C)} \right)^{-1} = \left( \frac{q\partial(-Q_i)}{\partial(E_F - E_i)} \right)^{-1} + \left( \frac{q\partial(-Q_i)}{\partial(E_i - E_C)} \right)^{-1} \quad (53)$$

This can be rewritten more simply as:

$$\frac{1}{C_{S_i}} = \frac{1}{C_{Q_i}} + \frac{1}{C_{cent_i}} \quad (54)$$

It is also simple to see that the centroid capacitance is related to the quantum capacitance in the following way:

$$C_{cent_i} = C_{Q_i} \cdot \frac{\partial(E_F - E_i)}{\partial(E_i - E_C)} \quad (55)$$

This circuit model, of course, is constructed without the presence of parasitics or interface traps, but those are easily incorporated as was shown in Ch. 2. When we investigate the C-V characteristics of a III-V MOSFET, it will be useful to break down the overall gate capacitance and see how the different components discussed here have an effect on the complete behavior. It is for this reason that this short overview of the quantum capacitance model will be valuable in our study.

### 4.3 Device Under Study

The structure of the III-V MOSFET was described in Chapter 1, but as with the HEMT we reintroduce it in Figure 4-2 to discuss the design by Lin *et al.* [6], whose experimental work is the basis for our comparisons. The channel consists of 2 nm of InAs surrounded by 3 nm and 5 nm  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  cladding layers. This is a buried channel design, so there is a 1 nm barrier layer of InP between the channel and the oxide, which consists of 2 nm of either  $\text{Al}_2\text{O}_3$  or  $\text{HfO}_2$ . In extracting  $D_{it}$ , we will consider these two oxide materials separately.

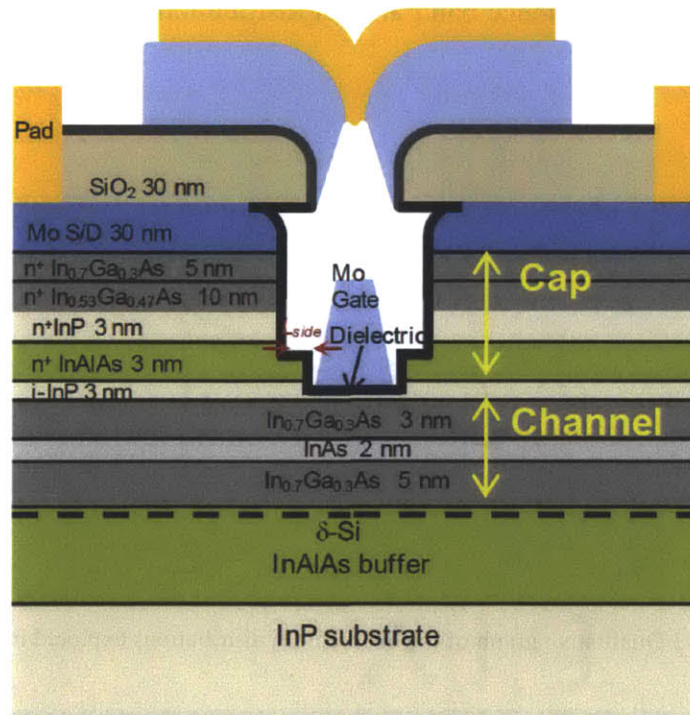


Figure 4-2. Schematic of a MOSFET structure, reproduced from J. Lin *et al.* [6].

#### 4.4 Effect of $D_{it}$ on Subthreshold Swing

Our ultimate goal is to be able to use our knowledge of the interface state trap density  $D_{it}$  to understand the non-ideal subthreshold swing, so it is from this perspective that we will first examine the effects of  $D_{it}$ . We consider several hypothetical distributions of trap states so as to see how the distribution can have a large impact on the subthreshold swing. Experimental long-channel devices are used to compare the subthreshold characteristics, so we do not have to concern ourselves with other parasitic capacitances.

We have chosen three different trap distributions to examine: a linear, Gaussian, and an exponential distribution. Though the shapes of these distributions are different, we make sure that the total charge from these states from the valence band edge to the conduction band edge integrates to the same value, which we have chosen arbitrarily to be  $2 \times 10^{13} / \text{cm}^2$  just to illustrate our point. This value is within the correct order of magnitude of what we might see in a real device. A sketch of the distributions is shown in Figure 4-3, with the linear distribution beginning at the edge of the valence band and all distributions limited to the inside of the band gap.

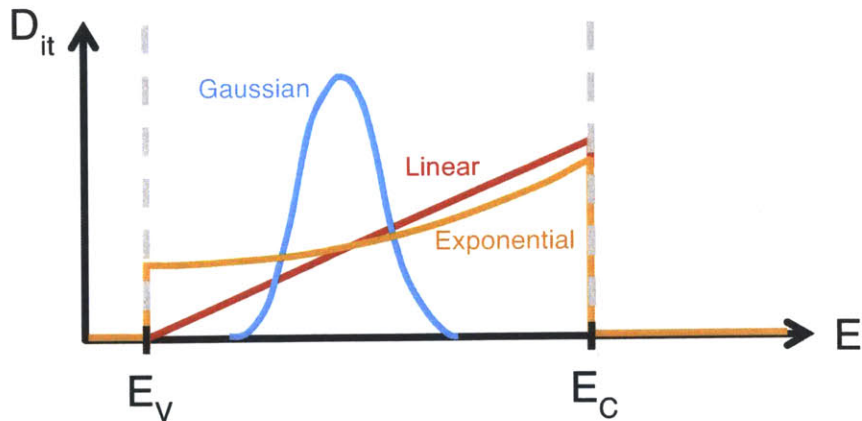


Figure 4-3 Qualitative graph of the different  $D_{it}$  distributions explored in this study.

To achieve the same total charge in the three cases, we use the following distributions:

- Linear: 0 at valence band edge,  $\sim 3 \times 10^{13} / \text{cm}^2$  at conduction band edge

- Exponential: peak value of  $2.7 \times 10^{13} / \text{cm}^2$  at conduction band edge with decay constant of 1 eV
- Gaussian: peak of  $4 \times 10^{13} / \text{cm}^2$ , with  $\sigma = 0.2$  eV located 0.7 eV below the conduction band edge

Having done this, we can see the results of these trap distributions on the subthreshold characteristics in Figure 4-4. We have used the structure of Figure 4-2 with  $\text{Al}_2\text{O}_3$  as the oxide layer, and have chosen to model  $D_{it}$  with acceptor states. The acceptor states are filled when the Fermi level sweeps upward through the bandgap and they accept an electron, leaving them negatively charged. If part of the applied gate voltage is being used to fill the trap states, the I-V characteristics will stretch and shift to the right because interface traps do not supply mobile charge and it will take a larger  $V_{GS}$  to achieve the desired current levels. The ideal case with no  $D_{it}$  and perfect subthreshold swing is shown in Figure 4-4 as well, for comparison. Here we can see that the shape of the distribution can in fact make quite a large difference, where the Gaussian has the largest effect in all likelihood because of its tall and relatively concentrated peak.

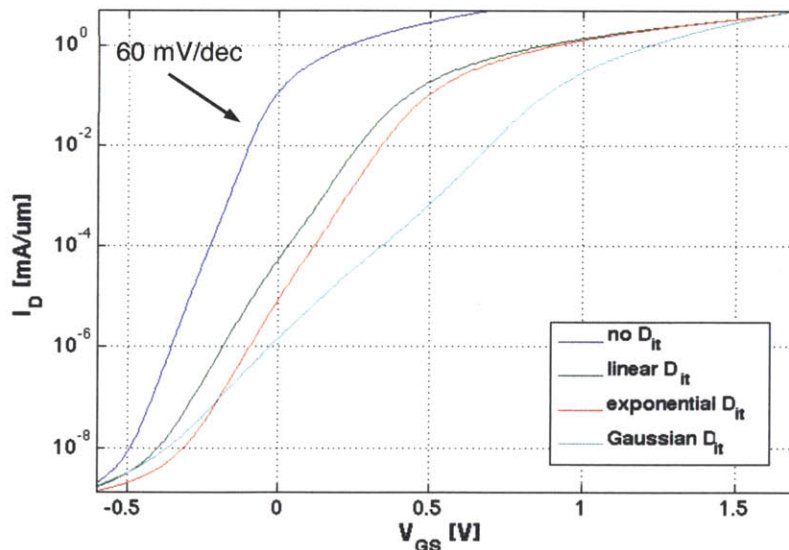


Figure 4-4  $I_D$  vs.  $V_{GS}$  in the subthreshold regime (logarithmic scale). Ideal case of perfect subthreshold swing is shown in blue.

An important point to note, however, is that eventually all the simulated currents for different  $D_{it}$  distributions do converge onto the same current value. This is because the Fermi level has swept beyond all the traps, and the total charge in the traps is no longer changing. However, because we have used acceptor states, we will have a fixed negative charge in the traps that causes a permanent threshold voltage shift relative to the case with no  $D_{it}$ . We can see this more clearly in Figure 4-5, where we show the transfer characteristics above threshold. Aside from the fixed voltage shift, all scenarios with  $D_{it}$  end up with the same current in strong saturation.

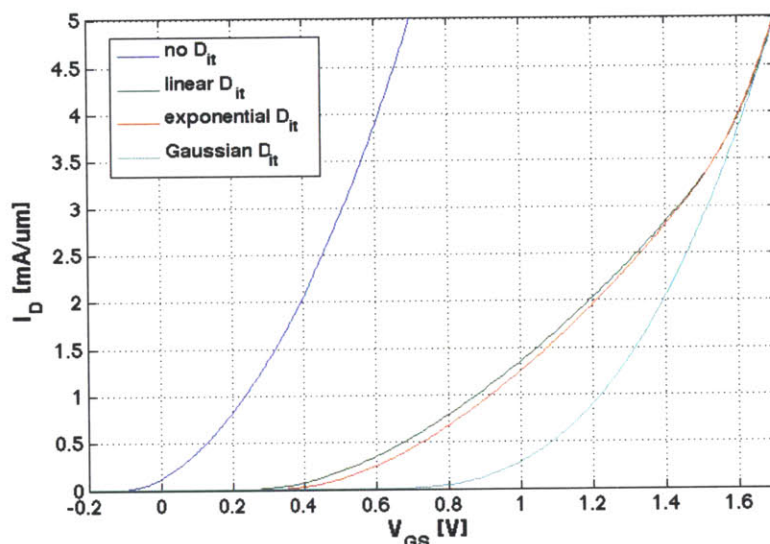


Figure 4-5  $I_D$  vs.  $V_{GS}$  in the saturation regime. Ideal case of perfect subthreshold swing is shown in blue.

While the choice of  $D_{it}$  distribution has the potential to make a substantial difference, what this exercise also makes clear that it is not straightforward to extract the  $D_{it}$  distribution from the subthreshold characteristics, in part because the integrated  $D_{it}$  is what actually affects the I-V characteristics, but also because the mapping of current into charge is not clear-cut. This is now why we will turn to the C-V regime, where it is much easier to extract a  $D_{it}$  distribution that could then in turn explain the subthreshold behavior of the device.

#### 4.5 Comparison with Experimental Data

We will now focus our attention on the C-V characteristics of the III-V MOSFET. In the first section, we use lower-temperature experimental measurements to best match our simulation to

the actual device, assuming that the lower temperature lessens the effects of  $D_{it}$  because the traps are frozen out and cannot necessarily respond to the frequency of the C-V sweep. The second section discusses the extraction of  $D_{it}$  at room temperature.

### 4.5.1 C-V Characteristics at Low Temperature

We will take a look at both the  $Al_2O_3$  and  $HfO_2$  designs, as we expect that the  $D_{it}$  from the two different interfaces will be different. We start with the  $Al_2O_3$  III-V MOSFET. In reality, there is some uncertainty about the thickness of the oxide layer, so we have increased the oxide thickness to 2.5 nm in our simulations in order to better fit the experimental results. Figure 4-5 shows the C-V characteristics of both the experimental device and the simulation at  $-65^\circ C$ . The simulation does not include any interface states— $D_{it}$  will be found in the next section when we examine room temperature data.

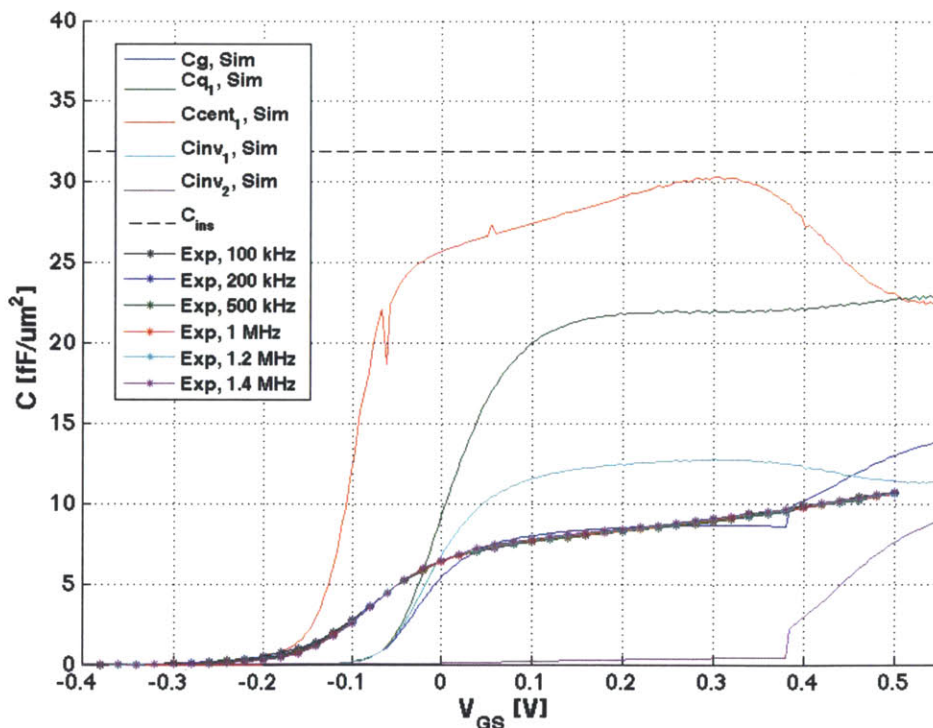


Figure 4-6 C-V characteristics of simulation (smooth lines) plotted against experiment (marked lines) for  $Al_2O_3$  oxide,  $-65^\circ C$ . The simulated  $C_G$  is in blue, the quantum capacitance  $C_{Q1}$  of the first sub-band in green, the inversion capacitance of the first sub-band in aqua, and the second inversion capacitance in purple. The value of the  $Al_2O_3$  capacitance  $C_{ins}$  is plotted as the black dashed line for reference.

We compare here the experimental data in the marked lines and the simulated gate  $C_G$  shown in dark blue. We can still see that  $D_{it}$  is present even at the lower temperature, and that there is an additional discrepancy above the threshold voltage whose origin is unknown. There is reasonable matching between experiment and simulation when the device is on, but the worse match and gentler experimental slope when the device is being turned off indicate the presence of traps. There is also very little frequency dispersion in the experimental data, all of which sit essentially on top of one another, which is consistent with low  $D_{it}$  responding at this temperature. We have also plotted the different components of the capacitance that we discussed in our gate capacitance model so that we can easily see what components contribute to the experimental data. The centroid capacitance (red) combined with the quantum capacitance (green) in parallel yields the inversion capacitance for the first sub band, shown in light blue. The behavior of the inversion layer is mirrored in the experimental data, just as we can see that the continued rise in capacitance for high values of  $V_{GS}$  most likely corresponds to the initial population of the second sub band.

For completeness, we show the C-V characteristics at  $-65^\circ\text{C}$  for the  $\text{HfO}_2$  device in Figure 4-6. As with the  $\text{Al}_2\text{O}_3$ , we have increased the simulation oxide thickness to 2.5 nm.  $C_{ins}$  is not plotted because the high dielectric constant of  $\text{HfO}_2$  puts the value of  $C_{ins}$  at around  $80 \text{ fF}/\mu\text{m}^2$ , well off scale. The regions where there seem to be interface states have much the same behavior—a gentler rising slope at lower  $V_{GS}$ , and at higher  $V_{GS}$  around the second sub-band population, but there is some noticeable frequency dispersion for larger values of  $V_{GS}$ . This is most likely due to the fact that the dielectric constant for  $\text{HfO}_2$  is more than twice as large as that of  $\text{Al}_2\text{O}_3$ , and thus we are penetrating farther into the conduction band for the same value of  $V_{GS}$  than we were for the  $\text{Al}_2\text{O}_3$ . This dispersion is most likely due to gate leakage effects instead of  $D_{it}$ , as we will see in the room temperature data.

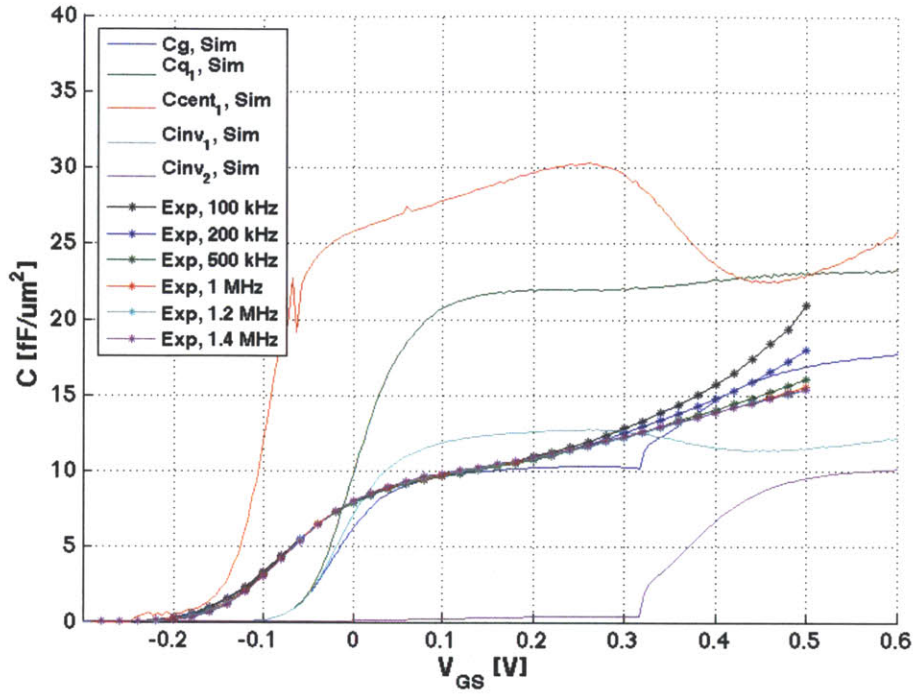


Figure 4-7 C-V characteristics of simulation plotted against experiment for HfO<sub>2</sub> oxide, -65°C.

#### 4.5.2 $D_{it}$ Extraction

Having matched to the best of our abilities the simulation at lower temperature to the experimental characteristics, we can now move on to extract the  $D_{it}$  in the device at room temperature. The same C-V characteristics for the Al<sub>2</sub>O<sub>3</sub> oxide, now at room temperature, are shown in Figure 4-7.

It is clear right away that there is substantially more  $D_{it}$  present at room temperature than there was at -65°C. We can also see that there is some frequency dispersion for low and high values of  $V_{GS}$ , indicating that not all of the traps may be able to respond to the higher frequencies. It is for that reason that we choose the 50 kHz experimental C-V data from which to obtain our  $D_{it}$  distribution. To first find the capacitance  $C_{it}$  from the traps, we use our buried-channel capacitance model from Figure 2-8 setting  $C_D$  to zero. We can lump the capacitance from the InP barrier and the capacitance from the inversion layer into a single term,  $C_L$ :

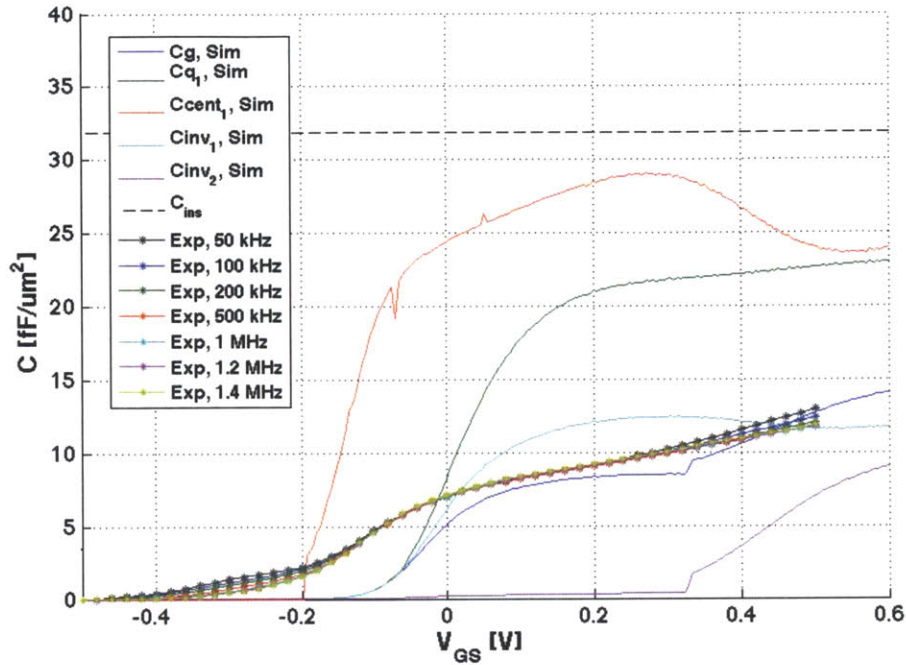


Figure 4-8 C-V characteristics of simulation with  $D_{it} = 0$  against experiment for  $Al_2O_3$  oxide, room temperature.

$$C_L = \frac{C_S \cdot C_{barrier}}{C_S + C_{barrier}} \quad (56)$$

As in our simulations, an ideal capacitance model does not contain any  $D_{it}$  and we can solve for  $C_L$  in terms of the gate voltage  $C_G$  and the insulator capacitance  $C_{ins}$ :

$$C_L = \frac{C_{G,D_{it}=0} \cdot C_{ins}}{C_{ins} - C_{G,D_{it}=0}} \quad (57)$$

Now that we have an expression for  $C_L$ , it is simple to use this in the complete gate capacitance model that includes  $D_{it}$ , and from there, extract an expression for  $C_{it}$ :

$$C_{it} = \frac{C_{G,with D_{it}}(C_{ins} + C_L) - C_{ins} \cdot C_L}{C_{ins} - C_{G,with D_{it}}} \quad (58)$$

Having solved for  $C_{it}$  we can obtain the charge from interface traps,  $Q_{it}$  by integration.  $Q_{it}$  is then related to  $D_{it}$  by (41) in Chapter 2 and so from here, we have decided to fit the charge  $Q_{it}$  by assuming a constant value of  $D_{it}$  over short intervals of 50 mV of the interface surface potential  $\phi_{it}$ . This does not yield discontinuous steps in  $C_{it}$  because of the thermal smearing that occurs as

the Fermi level sweeps upwards in the conduction band. By tailoring  $D_{it}$  in this way, we obtain the results in Figure 4-8, where we have essentially a perfect match to the experimental data up to the region of high  $V_{GS}$ .

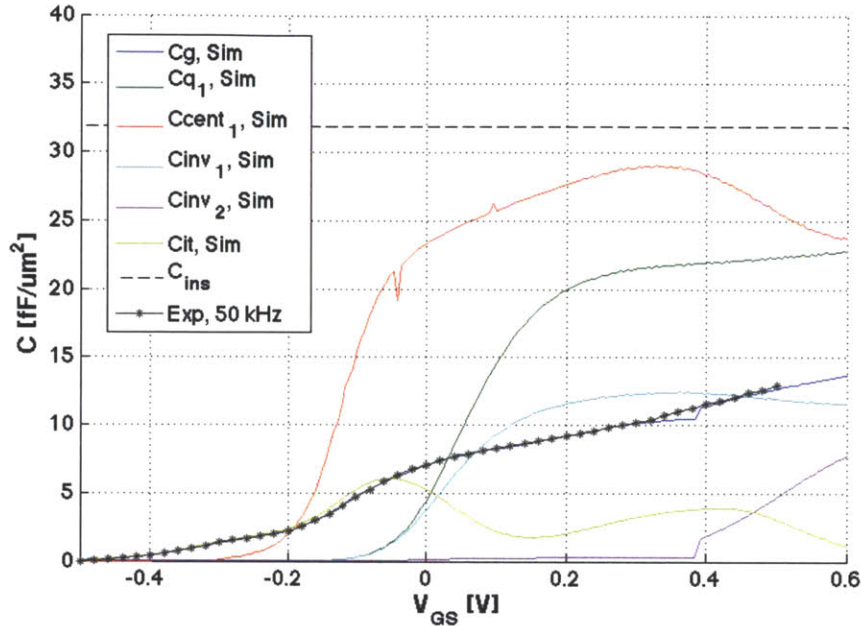


Figure 4-9 C-V characteristics of simulation & experiment for  $Al_2O_3$  with  $D_{it}$  fit.

We can see the shape of  $C_{it}$  in the graph, with the peak values corresponding to areas where there is the largest gap between the simulated C-V characteristics and the experimental characteristics. The simulated  $C_G$  discontinuity and area around  $V_{GS} = 0.4V$  is due to the discontinuity in the inversion capacitance of the second sub band. This, in turn is most likely an error arising from the fact that the voltage steps in the Poisson-Schrödinger simulations are too large, and can be solved by completing the simulations for a finer grid.

From the distribution of interface states, we can construct a plot of  $D_{it}$  in the InP band gap. This is seen in Figure 4-9. The distribution consists of two peaks: the larger peak is slightly above mid-gap at about 0.8 eV above the valence band edge with a maximum value of  $4.4 \times 10^{12} /eV\text{-cm}^2$  and the second, smaller peak is closer to the conduction band at 1.15 eV above the valence band edge with a value of  $3 \times 10^{12} /eV\text{-cm}^2$ .

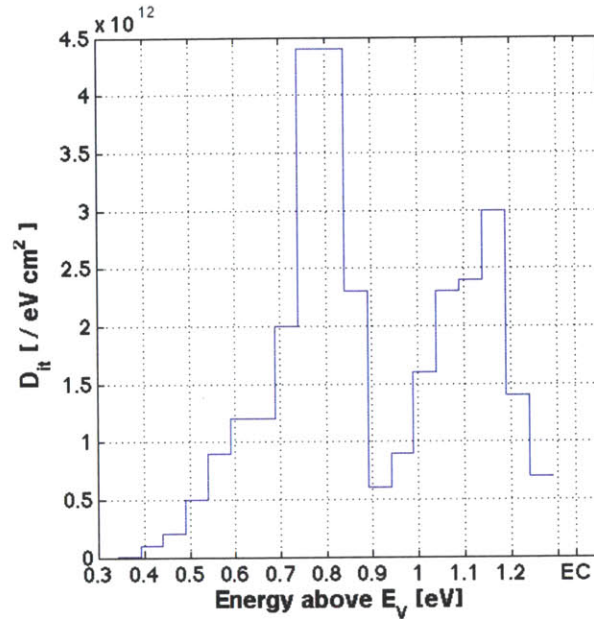


Figure 4-10  $D_{it}$  distribution for  $\text{Al}_2\text{O}_3$  in the InP band gap, extracted from C-V.

The second peak closer to the conduction band edge is most likely due to the discontinuity discussed earlier, so we predict that if it were eliminated,  $D_{it}$  would continue its trend of decreasing down towards the conduction band. Unfortunately, for the experimental data available, we cannot extract  $D_{it}$  into the conduction band both because the Fermi level does not penetrate far enough into the conduction band of the InP barrier, but also because at large  $V_{GS}$  gate leakage becomes a problem and the discrepancies in C-V data are not reliably due just to  $D_{it}$  effects.

The effects of interface traps have been studied before, and we can in fact compare our results for  $D_{it}$  with other experimental data. Figure 4-10 shows data from [23], where the  $D_{it}$  has been found in the upper half of the bandgap for the  $\text{Al}_2\text{O}_3/\text{InP}$  interface. If it were not for the discontinuities in the simulations, both sets show  $D_{it}$  decreasing towards the conduction band edge to quite low values. However, our distribution puts our peak  $D_{it}$  value at 0.8 eV above the valence band edge, with a maximum  $D_{it}$  value of  $4.4 \times 10^{12} /eV\text{-cm}^2$  but Figure 4-10 shows  $D_{it}$  still on an upwards trend even at 0.7 eV above the valence band edge. The measured value of  $D_{it}$  is also roughly  $10^{13} /eV\text{-cm}^2$ . It is not clear from that data whether or not the peak of the  $D_{it}$  distribution would be at 0.7 eV or would be closer to the valence band edge, though our work shows a clear trend of decreasing  $D_{it}$  into the middle of the gap. The inherent uncertainties in our

approach do not allow for an exact answer, but do give an order of magnitude result that provides us with valuable qualitative insight.

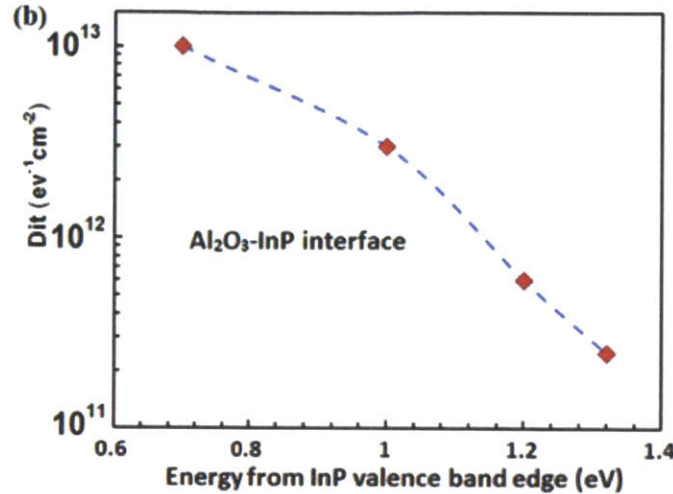


Figure 4-11  $D_{it}$  distribution in the InP band gap, reproduced from [23].

We will now take a brief look at the  $\text{HfO}_2$  device, using the same procedure as we did for the  $\text{Al}_2\text{O}_3$  MOSFET. We showed the C-V characteristics for  $-65^\circ\text{C}$  in Figure 4-6. Having found a fit at lower temperature, we look at the room temperature data again, and obtain an appropriate  $D_{it}$  distribution. Figure 4-11 shows the room temperature C-V characteristics with and without  $C_{it}$ , and then the corresponding  $D_{it}$  distribution as a function of energy. Gate leakage was judged to be a problem past about  $V_{GS} = 0.3\text{V}$ , so  $D_{it}$  was not fit any farther, however, it is mostly likely that the high peak towards the conduction band is really stemming from these same gate leakage problems.

We can conclude from this study that the  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  interfaces have roughly the same  $D_{it}$  distribution, and  $D_{it}$  levels extracted are consistent with what is observed from the subthreshold characteristics of [6]. Though it is not completely certain whether the  $D_{it}$  peak for the  $\text{HfO}_2$  near the conduction band edge is due entirely to  $D_{it}$  or possibly to gate leakage effects, it seems that  $\text{Al}_2\text{O}_3$  may give a slightly better interface.

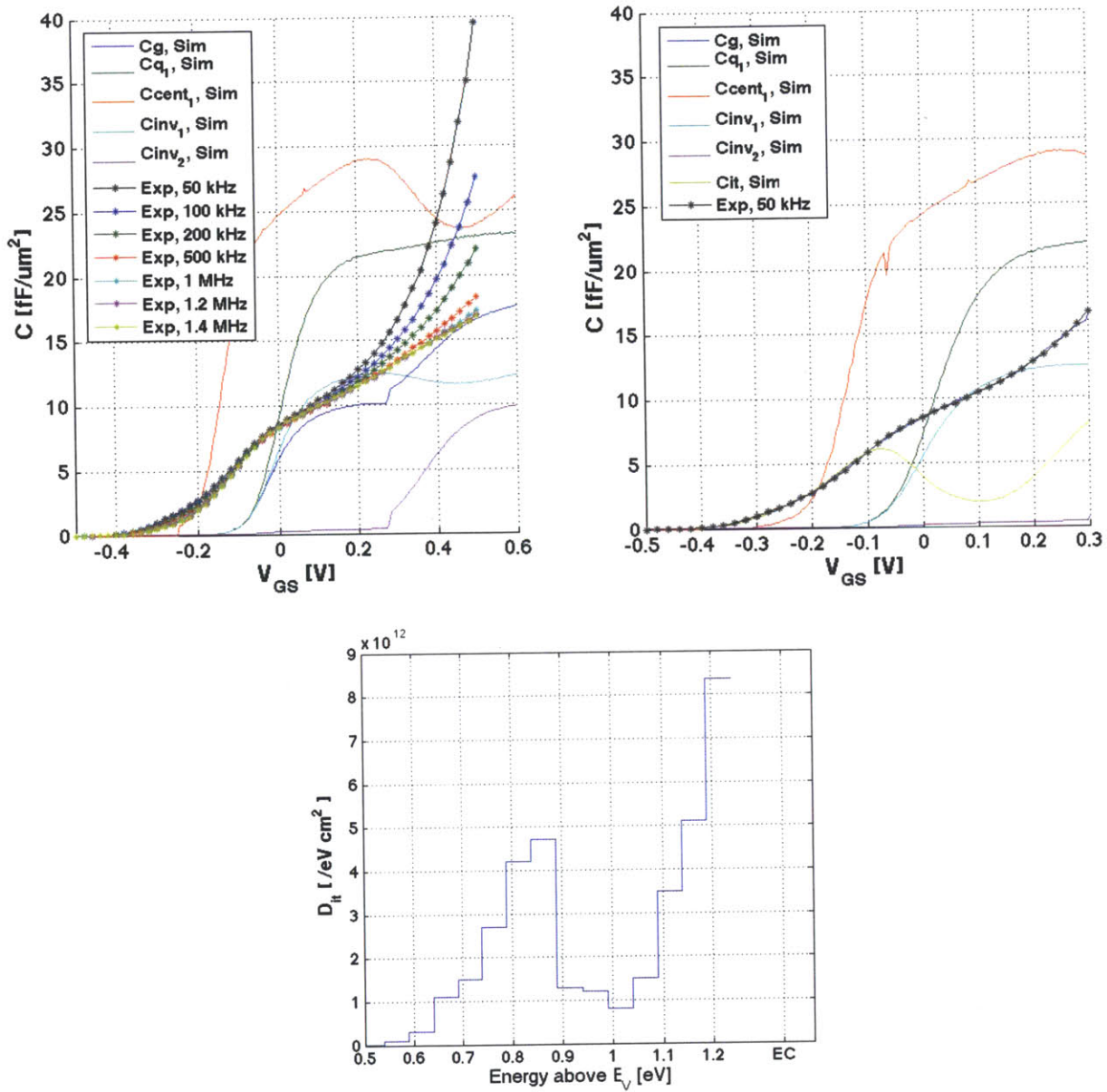


Figure 4-12 Room temperature C-V for simulation vs. experiment for HfO<sub>2</sub> (top left), C-V for simulation fitted with D<sub>it</sub> (top right), D<sub>it</sub> distribution in InP bandgap (bottom).

It is worth mentioning again that the discussion above is approximate, not exact. Both the uncertainty in the oxide and barrier thickness, as well as the possibility of other effects, especially at high  $V_{GS}$ , are not factors that can be ignored. There is also uncertainty about the effective mass in the channel. Here, we have used the bulk value of  $0.026m_0$  for InAs but in all likelihood the effective mass will be higher, and has a non-negligible effect on the C-V

characteristics. In order to do a more in-depth study, we would need to consider both the I-V and C-V characteristics at the same time.

#### 4.6 Hall Effect Measurements

A study of  $D_{it}$  gives us valuable information that can help us understand the subthreshold behavior of a device, but it is also useful to know the 2D sheet carrier concentration and mobilities of these devices as a function of  $V_{GS}$ , independent of  $D_{it}$  effects. For this, we turn to Hall effect measurements, which exploit the movement of electrons in a magnetic field to find these two figures of merit.

##### 4.6.1 Theory for the Hall Effect

Before discussing the experimental results from this work, it is valuable to have some knowledge of how the Hall effect measurements are taken. An in-depth explanation of this theory is covered in [24], but we will briefly cover the most important pieces here. The Hall bar is drawn again for convenience in Figure 4-12. It has a width  $w$ , and a length  $\ell$ , and a current  $I$  runs down the length of the bar. The Hall voltage is measured across the width of the device, and the longitudinal voltage  $V_x$  is measured along the direction of current flow.

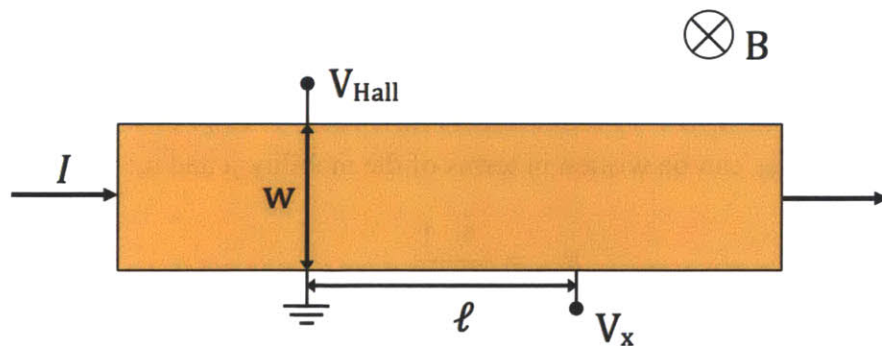


Figure 4-13 Schematic of a simple Hall bar.

To first find the sheet resistance of the Hall bar, we measure the longitudinal voltage  $V_x$  in the absence of a magnetic field:

$$V_x = \frac{\ell R_{Sh}}{w} I \quad (59)$$

where  $R_{Sh}$  is the sheet resistance of the bar. To obtain more accuracy than by using a single value of current and measuring  $V_x$ , we can actually find  $R_{Sh}$  through the resistivity in the longitudinal direction:

$$R_{Sh} = \frac{w}{\ell} \frac{dV_x}{dI} \quad (60)$$

To find the sheet carrier concentration and mobility, we now consider the Hall bar in the presence of a magnetic field. As current flows down the Hall bar, the magnetic field diverts electrons to the sides. Eventually, an equilibrium state will develop where the force driving the electrons to the sides of the bar is balanced and opposed by the presence of an electric field arising from the higher concentration of electrons on one side of the bar. This equilibrium electric field is measured as the Hall voltage:

$$V_H = \frac{BI}{qn_s} \quad (61)$$

where  $q$  is the unit of charge,  $n_s$  is the 2D sheet carrier concentration in the Hall bar, and  $B$  is the magnetic field. We can find  $n_s$  by a similar approach as (60), using the resistivity in the lateral direction:

$$n_s = \frac{B}{q} \left( \frac{1}{\frac{dV_H}{dI}} \right) \quad (62)$$

The sheet resistance  $R_{Sh}$ , can be written in terms of the mobility  $\mu$  and  $n_s$ :

$$R_{Sh} = \frac{1}{qn_s \mu} \quad (63)$$

As a result,  $\mu$  can be written in terms of the sheet carrier concentration and the sheet resistance:

$$\mu_H = \frac{1}{qn_s R_{Sh}} \quad (64)$$

This gives us complete expressions for obtaining  $R_{Sh}$ ,  $n_s$ , and  $\mu$  using the Hall bar setup.

#### 4.6.2 $\mu$ and $n_s$ for the III-V Quantum-Well MOSFET

We will now show our experimental measurements for both  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$  oxide devices. We can repeat the process described in the previous section and find the sheet carrier concentration and mobility for a variety of different gate voltages. We begin first with  $\text{Al}_2\text{O}_3$  in Figure 4-13. The parameters of interest are shown on the right, and on the left we show either  $V_x$  or  $V_H$  as a function of current in the bar for qualitative understanding only. These qualitative graphs show the slopes from which we derive our values of  $R_{sh}$ ,  $n_s$ , and  $\mu$ . There are two graphs for the Hall voltage because we measure the Hall voltage using two different orientations of magnetic fields with north and south polarities, and average these results.

It is important to note that we cannot accept the values of  $n_s$  and  $\mu$  for both very small and very large gate voltages. At very negative  $V_{GS}$ ,  $V_H$  goes negative for zero current, which probably indicates the occurrence of gate leakage. At large  $V_{GS}$ , the gate leakage current is again so high that it overwhelms the current running down the Hall bar. We see this qualitatively from the fact that there are several lines for  $V_x$  and  $V_H$  that no longer intersect the origin. These correspond to large values of the gate voltage. We have not performed any sort of offset elimination procedures on these values, as in all likelihood the gate leakage at both extremes of  $V_{GS}$  is high enough to make even the compensated values questionable anyway. Therefore, we can accept as valid our results between the voltage range of about  $V_{GS} = 0\text{V}$  to  $V_{GS} = 0.25\text{V}$ . Though this is not as wide of a span as we might desire, with better devices that have less gate leakage we have the potential to make valid measurements over a much larger span.

Regardless of these shortcomings, we can see that the mobility shown in these devices is noticeably better than as reported elsewhere [6], going well above  $6000\text{ cm}^2/\text{V}\cdot\text{s}$ . We see similar results for the  $\text{HfO}_2$  MOSFET, shown in Figure 4-14. The gate leakage problem does seem to be more severe with the  $\text{HfO}_2$ , but even so, the mobility goes to about  $9000\text{ cm}^2/\text{V}\cdot\text{s}$ .

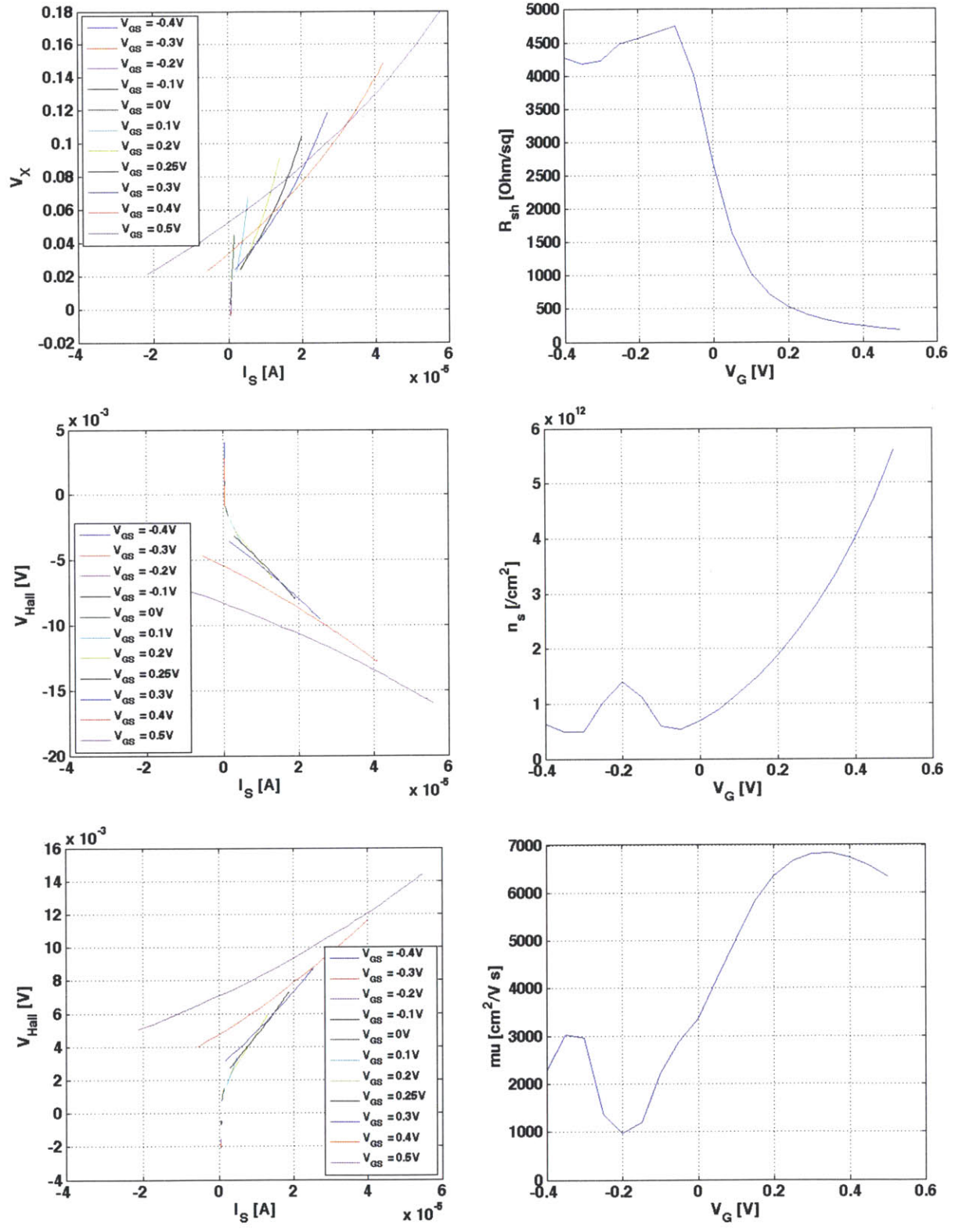


Figure 4-14 Sheet resistance (top right), sheet carrier concentration (middle right), and mobility (bottom right) for  $Al_2O_3$  device.

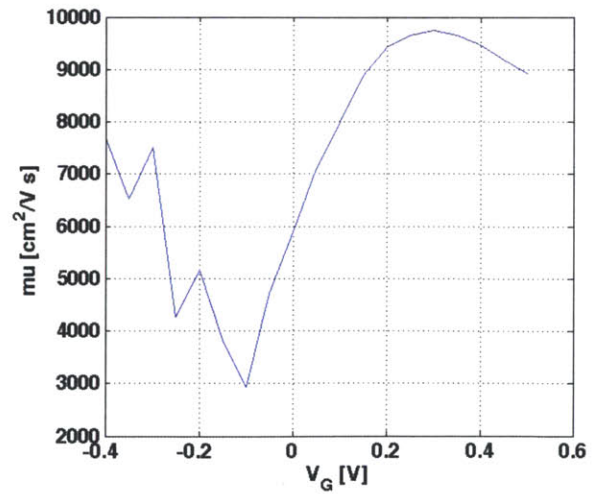
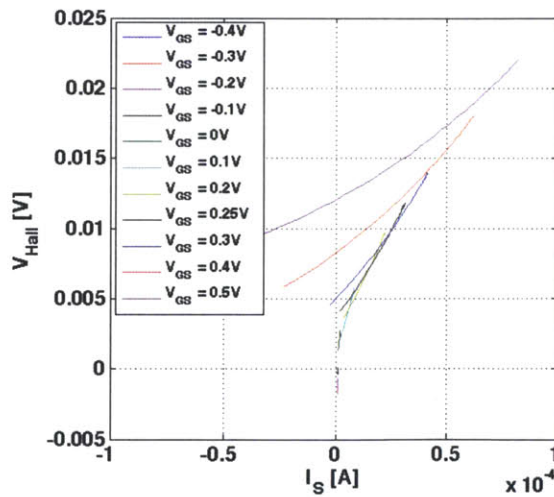
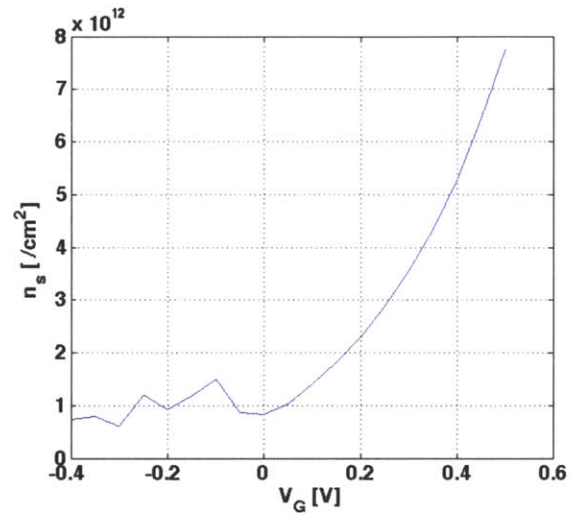
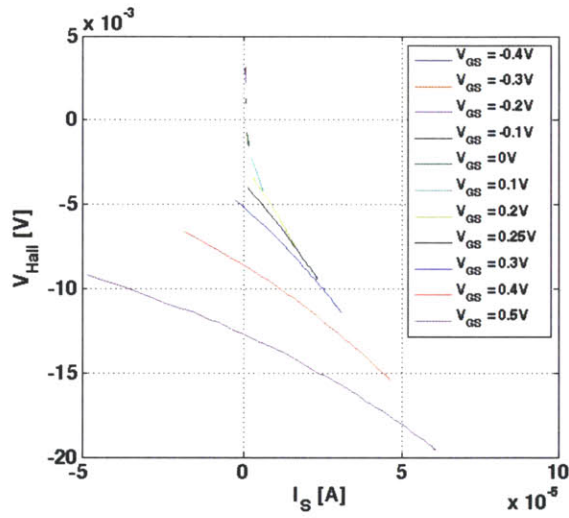
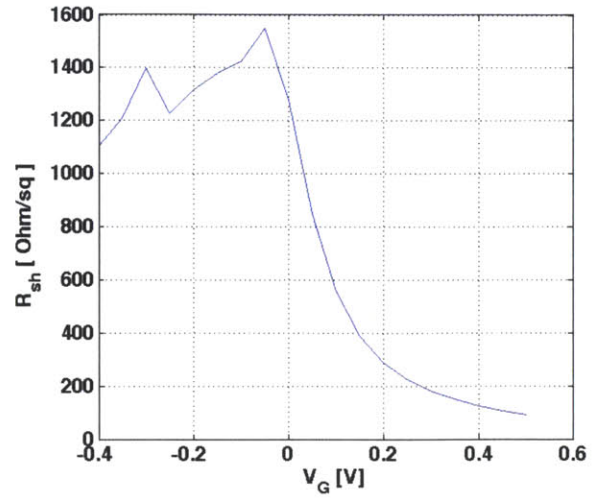
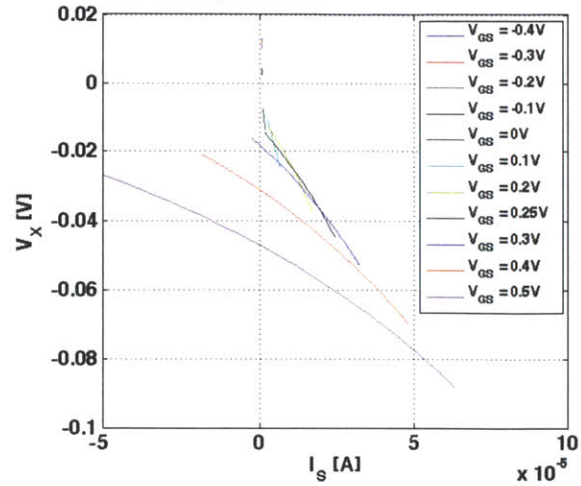


Figure 4-15 Sheet resistance (top right), sheet carrier concentration (middle right), and mobility (bottom right) for  $HfO_2$  device.

It is also often valuable to examine the mobility in the context of the sheet carrier concentration. For this reason, we have plotted  $\mu$  versus  $n_s$  in Figure 4-15 for  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$ . Both curves show an increasing trend for increasing  $n_s$ , but look as if they are nearing saturation. In fact, [6] predicts that the mobility will peak at a certain  $n_s$  and then begin to decrease. In future work, for larger  $V_{GS}$  we would in all likelihood see this same behavior.

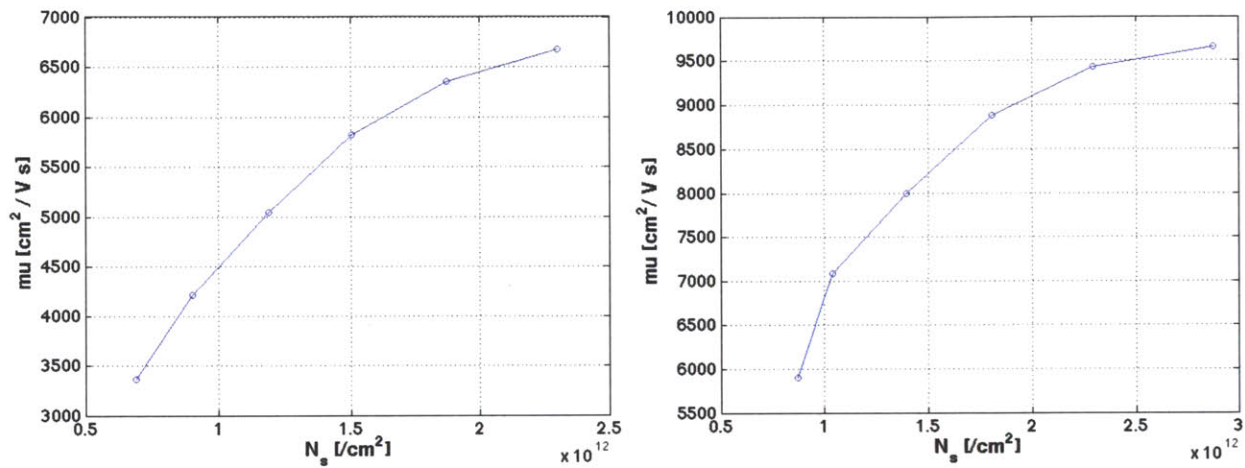


Figure 4-16  $\mu$  vs.  $n_s$  for  $\text{Al}_2\text{O}_3$  (left) and  $\text{HfO}_2$  (right).

As the mobility is a very important figure of merit, it is quite useful to have a fast way to find its value for a range of applied gate voltages and therefore sheet carrier concentrations. As this work is mostly limited by gate leakage, with more robust devices we would be able to expand to a wider range of gate voltages and sheet carrier concentrations, giving further insight into device behavior.

#### 4.7 Summary

In a continuation of our work with the ballistic model, we were able to apply the model to the III-V quantum-well MOSFET, examining the effect of  $D_{it}$  on subthreshold characteristics and then going on to extract the actual  $D_{it}$  distribution using C-V characteristics for both  $\text{Al}_2\text{O}_3$  and  $\text{HfO}_2$ . We found that there is some qualitative agreement between this work and other experimental work on  $D_{it}$ , but acknowledge that we are limited by various uncertainties that make the precise determination of  $D_{it}$  difficult. We concluded by examining two figures of merit in FET devices, the 2D sheet carrier concentration and the mobility, with techniques independent of  $D_{it}$ . In the

next chapter, we continue our discussion on the ballistic transport model, and provide suggestions for future study on both HEMTs and III-V MOSFETs.



## CHAPTER 5. CONCLUSIONS & SUGGESTIONS

In this thesis, we have developed a flexible, compact model for III-V quantum-well FETs based on the ballistic theory of transport. We have compared our model with experimental data for the III-V HEMT, and have examined the III-V quantum-well MOSFET from the perspective of the C-V characteristics. We have also carried out Hall effect measurements to obtain two figures of merit, the 2D sheet carrier concentration and mobility, independently of any effects from trap states, which in turn indicates room for improvement if the effects of interface traps can be reduced. We will summarize in this chapter our key findings, and provide suggestions for future work.

### *5.1 Conclusions*

We have built upon existing transport theory to incorporate many first-order and second-order effects into our ballistic model, and explored the impact of these effects on the output and transfer characteristics of a III-V device. We then validated this model against experimental data for a short-channel HEMT, extracting parameters of interest such as the source and drain parasitic resistances  $R_S$  and  $R_D$ , and the drain-induced barrier lowering DIBL. We found that while there is good agreement in the transfer characteristics, we still significantly overestimate the transconductance  $g_m$ . We also found that experimental output conductance indicates the need for a much higher value of DIBL than the one we use to match the subthreshold characteristics.

We then took the model further and looked at the unique characteristics associated with the III-V MOSFET. We examined the eventual impact of interface states on the subthreshold characteristics, and then using the C-V characteristics of the device we estimated the distribution of interface states  $D_{it}$ . The extracted values of  $D_{it}$  are of the same order of magnitude as other reports in the literature. The  $D_{it}$  distribution qualitatively follows the behavior we would expect,

despite being limited by our knowledge of uncertainties in effective mass, oxide thickness, gate leakage, and other potential parasitics.

To complete our study of the III-V MOSFET, we carried out experimental measurements of the sheet carrier concentration  $n_s$  and the mobility  $\mu$ . We were able to measure mobilities of over  $6000 \text{ cm}^2/\text{V-s}$  for the  $\text{Al}_2\text{O}_3$  MOSFET, and over  $9000 \text{ cm}^2/\text{V-s}$  for its  $\text{HfO}_2$  counterpart. These measurements can be further validated once more robust devices with better gate leakage characteristics have been fabricated.

## ***5.2 Suggestions for Future Work***

There are a number of studies that could be carried out as valuable continuations to the research described in this work.

- Extend the ballistic model further to investigate the discrepancies between the transconductance  $g_m$  and the output conductance of the simulated work versus experimental results.
- Independently determine the real value of effective mass of electrons in the channel as a function of the applied gate voltage. As this is an important input to the model, a precise understanding of what the effective mass is and how it changes is crucial to the accuracy of future work. A possible methodology for achieving this would be to exploit the Shubnikov-de Haas Effect [22].
- Use I-V and C-V characteristics in tandem to better fit experimental work for both the III-V HEMT and the III-V MOSFET. In the case of the MOSFET, this will give us a more quantitative and exact view of the  $D_{it}$  distribution for the oxide/InP interface.
- Extend the Hall effect measurements to devices with less gate leakage to explore a wider range of  $n_s$  and mobility behavior. Combine with C-V and I-V measurements for a complete understanding of the electrostatics of the III-V MOS structure.

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