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$In_{0.49}Ga_{0.51}P$/GaAs heterojunction bipolar transistors (HBTs) on 200 mm Si substrates: Effects of base thickness, base and sub-collector doping concentrations

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We report performance of InGaP/GaAs heterojunction bipolar transistors (HBTs) fabricated on epitaxial films directly grown onto 200 mm silicon (Si) substrates using a thin 100% germanium (Ge) buffer layer. Both buffer layer and device layers were grown epitaxially using metalorganic chemical vapor deposition (MOCVD). With the assistance of numerical simulation, we were able to achieve high performance GaAs HBTs with DC current gain of ~100 through optimizing the base doping concentration (C-doped, ~ $1.9\times10^{19}/cm^3$), base layer thickness (~55 nm), and the sub-collector doping concentration (Te-doped, > $5\times10^{18}/cm^3$). The breakdown voltage at base (BV_{ceo}) of higher than 9.43 V was realized with variation of < 3% across the 200 mm wafer. These results could enable applications such as power amplifiers for mobile phone handsets and monolithic integration of HBTs with standard Si-CMOS transistors on a common Si platform.
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I. INTRODUCTION

The future integrated circuit will likely include the monolithic integration of silicon complementary metal oxide semiconductor (Si-CMOS) transistor with the high performance III-V materials for additional RF and/or opto-electronic applications.[1] The integration of the Si-CMOS and III-V materials has been demonstrated successfully through our well-established wafer bonding and layer transfer techniques.[2–4]

III-V heterojunction bipolar transistors (HBTs) are known to have higher current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) compared to Si-CMOS transistors. Gallium arsenide (GaAs)-based HBTs have been the dominant technology for wireless handset power amplifier (PA) applications due to their excellent performance, reliability and manufacturability. In this work, $In_{0.49}Ga_{0.51}P$/GaAs HBT is studied because the lattice constant of GaAs is more closely matched to Si (~4%) substrate which introduces lesser misfit and threading dislocations compare to $In_{0.3}Ga_{0.7}As$-, or InP- based HBTs (~6% to 8% lattice mismatch to Si substrate). They also provide higher collector efficiency compared to AlGaAs/GaAs HBTs because of their lower conduction band and higher valence band offset.[5]

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Although SiGe HBTs are more natural for integration with Si-CMOS, both f_T and f_{max} frequencies are comparable to the state-of-the art of the GaAs HBTs, the peak f_T can be scaled up only with newer technology nodes, i.e. scaling of the transistors. In terms of RF performance, the performance of III-V HBTs can be improved drastically by incorporating more indium into the GaAs HBTs, such as $In_{0.3}Ga_{0.7}As$- or InP-based HBTs.[6,7] Hence, the performance of the III-V HBTs can be improved not only by the scaling alone but also by tuning the III-V compositions. In addition, III-V HBTs have a higher breakdown voltage than SiGe HBTs.[8–10]

There are several approaches to realize the III-V HBTs on Si substrates. One approach is using germanium-on-insulator (GOI) substrate,[11] which is fabricated from Ge donor wafer. With this approach, HBTs with DC current gain of ~120-140 can be achieved, due to the low defect level ($\sim 10^5/cm^2$). However, this approach is limited by the Ge donor wafer size, hence not suitable for large scale integration. The other approach is utilizing a thick compositional graded Si_xGe_{1-x} buffer layer (~10 μm) to accommodate the lattice mismatch between the GaAs/Ge layer and the Si substrate. Using this approach, AlGaAs/GaAs and InGaP/GaAs HBTs with DC current gain of about 100 and 25, respectively, were demonstrated.[12,13]

In this paper, we report the InGaP/GaAs HBT demonstrated on epitaxial films grown directly on a thin Ge layer (800 nm, 100%, buffer-less) on a Si substrate and DC performance of the HBT devices. We focused on the study of the effect of the base doping concentrations, base layer thickness and sub-collector doping concentration on the HBT performances, with assistant of numerical simulation.

II. MATERIAL GROWTH AND DEVICE FABRICATION

The epitaxial Ge layer with threading dislocation density (TDD) of low-$10^7/cm^2$ was grown on a (001)-oriented Si substrate (diameter = 200 mm, *p*-type, resistivity = 1-100 Ω-cm) with a 6° off-cut toward the [110] direction using MOCVD. The details of the buffer-less Ge on Si growth can be found in the Refs. 14 and 15.

The $In_{0.49}Ga_{0.51}P$/GaAs HBT structure was subsequently grown on the epitaxial Ge layer. The growth started with a 600 nm thick *n*-GaAs sub-collector (with varying doping concentration $N_{sub\text{-}collector}$, from 7×10^{17} to $> 5 \times 10^{18}/cm^3$), followed by a 600 nm thick *n*-GaAs collector ($1.3 \times 10^{17}/cm^3$). Next, a *p*-GaAs base layer (thickness t_{base} varying from 85 to 55 nm and doping concentration N_{base} varying from 1.9×10^{19} to $4.0 \times 10^{19}/cm^3$) was grown. Then, a 40 nm thick *n*-$In_{0.49}Ga_{0.51}P$ layer ($1.5 \times 10^{17}/cm^3$) emitter and a 120 nm thick *n*-GaAs ($5.0 \times 10^{17}/cm^3$) sub-emitter were grown. Lastly, a 40 nm thick compositionally graded *n*-InGaAs ($1.0 \times 10^{19}/cm^3$) and a 40 nm thick *n*-$In_{0.6}Ga_{0.4}As$ ($6.0 \times 10^{19}/cm^3$) cap were grown for ohmic contact formation. Si and tellurium (Te) were used as *n*-type dopants and carbon (C) was used as a *p*-type dopant in the MOCVD growth. Details of the layer structures are shown in Table I. The HBT devices were fabricated using standard photolithography technique. The emitter and base mesas were formed by wet etching process, with emitter area of 40 μm × 50 μm. Ni/GeAu/Ni/Au and Ti/Au were deposited as *n*-type and *p*-type contact, respectively.

TABLE I. Epitaxial structure of the InGaP/GaAs HBTs on Si substrate.

Layer	Material	Thickness (nm)	Growth Temperature (°C)	Polarity	Dopant	Doping ($/cm^3$)
Contact	$In_{0.6}Ga_{0.4}As$	40	550	*n*	Si & Te	6.0×10^{19}
Contact	$In_{0\rightarrow0.6}Ga_{1.0\rightarrow0.4}As$	40	550	*n*	Si & Te	1.0×10^{19}
Sub-emitter	GaAs	120	550	*n*	Si	5.0×10^{17}
Emitter	$In_{0.49}Ga_{0.51}As$	40	550	*n*	Si	1.5×10^{17}
Base	GaAs	t_{base}	550	*p*	C	N_{base}
Collector	GaAs	600	630	*n*	Si	1.3×10^{17}
Sub-collector	GaAs	600	630	*n*	Si or Te	$N_{sub\text{-}collector}$
Buffer	Ge	800	350 & 650	-	-	UID
Substrate	Si	-	-	*p*	B	-

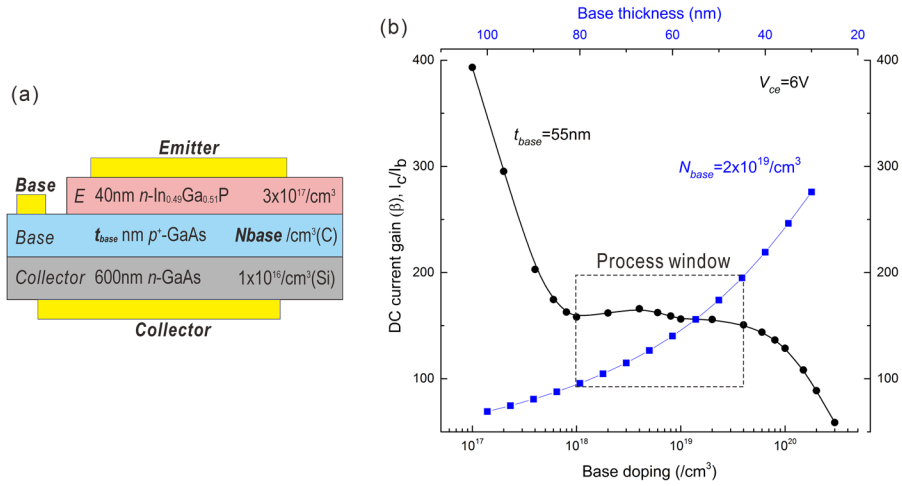

FIG. 1. (a) Schematic of the ideal HBT structure used for numerical simulation. (b) Simulation results of DC current gain of the HBT for various base doping concentrations (N_{base}) with the same base thickness of 55 nm (black curve), and base thicknesses (t_{base}) with the same base doping concentration of 2×10^{19}/cm^3 (blue curve). The DC gain is calculated at V_{ce}=6V.

III. NUMERICAL SIMULATION

A simplified HBT structure was used to establish a numerical simulation to understand the effects of the base thickness and the base doping concentration on the HBT performance, especially for the DC current gain, as shown in Fig. 1(a). The simulation suggested a wide process window of base doping level ranging from $\sim 1.0 \times 10^{18}$ to 3.0×10^{19}/cm^3 where the DC current gain is not affected significantly, with fixed base layer thickness of 55 nm, as shown in Fig. 1(b). Although low doping concentration in the base region can further increase the DC current gain, the base resistance (especially for case of thinner base) will be increased and hence affecting the HBT's RF performances. Extreme high doping concentration ($>1 \times 10^{20}$/cm^3) in the base region should also be avoided as it will reduce the DC current gain drastically due to high recombination rate in the base region.[16,17] On the other hand, the DC current gain is extremely sensitive to the base thickness. The current gain can be varied from 60 to over 200 by reducing the base thickness from 100 to 40 nm as depicted from Fig. 1(b), with base doping concentration fixed at 2×10^{19}/cm^3.

In order to achieve HBT devices with good DC and RF performances, the base thickness and doping concentration need to be designed and optimized. We'll study the effect of both base doping concentration and base thickness on the DC current gain experimentally in the following section.

IV. EXPERIMENTAL RESULT AND DISCUSSION

The bright-field cross-sectional TEM in Fig. 2(a) shows the overall InGaP/GaAs HBT structure grown on the 200 mm Si substrate with 100% Ge buffer layer. Most of the misfit dislocations are confined along the Ge and Si interface. TDD of 3.4×10^7/cm^2 is obtained on the Ge film surface, estimated by the etch-pit density (EPD) method, as shown in Fig. 2(b). Beyond the Ge layer, very few dislocations can be observed from the TEM image. Threading dislocations that propagate into the device layer are detrimental to the overall device performance, therefore its density has to be kept as low as possible.[18,19] The TDD of the HBT base layer estimated by electron beam-induced current (EBIC) method is 1.8×10^7/cm^2, as shown in Fig. 2(c), which is close to the TDD of the Ge film prior to the HBT structure growth, suggesting that a negligible amount of new dislocation is generated during the HBT device layers growth. The TEM images shows a rough top $In_{0.6}Ga_{0.4}As$ contact surface. This is due to the abrupt grading from GaAs to $In_{0.6}Ga_{0.4}As$ contact layer during the epitaxial growth. The TDD of the emitter surface cannot be readily revealed due to this high roughness. However, the rough $In_{0.6}Ga_{0.4}As$ contact does not affect the

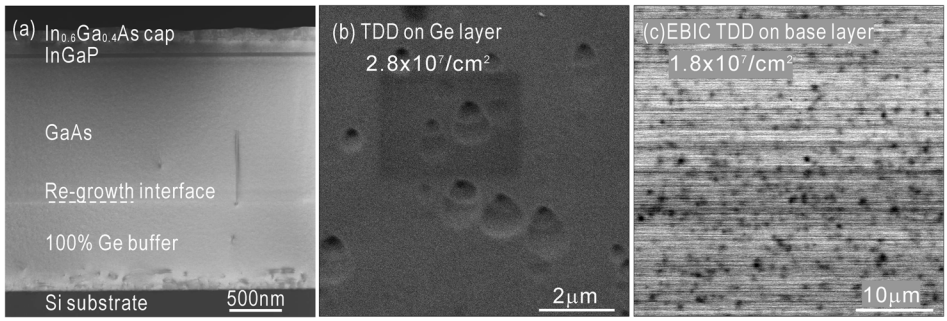

FIG. 2. (a) Cross-sectional TEM bright field image shows the overall view of an InGaP/GaAs HBT layer structure on a 200 mm Ge/Si substrate. (b) Threading dislocation density (TDD) of the Ge film on Si substrate measured by etched-pit density (EPD) method. (c) TDD of the HBT base layer surface measured by electron beam-induced current (EBIC) method.

performance of the HBT devices in terms of the DC current gain as evidenced from data in the next section.

The InGaP/GaAs HBTs with varying base thickness and base doping concentrations are fabricated, and the common emitter current-voltage (I_c-V_{ce}) characteristics are shown in Fig. 3. By reducing the base thickness from 85 to 55 nm while keeping the same base doping concentration, the DC current gain (β) increases from 20 to 50 as can be seen from Fig. 3(a). Since the base doping concentration is close to the borderline of the simulated current gain curve as shown in Fig. 1(b), we reduce the base doping concentration from 4.0×10^{19}/cm^3 to 1.9×10^{19}/cm^3. As shown in Fig. 3(b), HBTs with higher current gain of > 150 are achievable. These findings are closely matched to our numerical simulation results.

Although we are able to achieve a high DC current gain, the knee voltage of the HBTs is too large (>1 V at base current density (J_b) = 6 A/cm^2 for HBT with t_{base}=55nm, N_{base}=1.9×10^{19}/cm^3). The large knee voltage is attributed to the high sheet resistance of the sub-collector layer, due to the low doping concentration ($N_{sub\text{-}collector}$). To address this problem, the dopant species of the sub-collector layer is changed from Si to Te to further increase the doping concentration from 7×10^{17}/cm^3 to $> 5 \times 10^{18}$/cm^3. The common emitter I_c-V_{ce} characteristics of the fabricated HBT devices are shown in Fig. 4(a), with higher sub-collector doping concentration of $> 5 \times 10^{18}$/cm^3 while keeping the same base thickness of 55 nm and base doping concentration of 1.9×10^{19}/cm^3. The knee voltage is improved to ~ 0.6 V at J_b = 6 A/cm^2. The Gummel

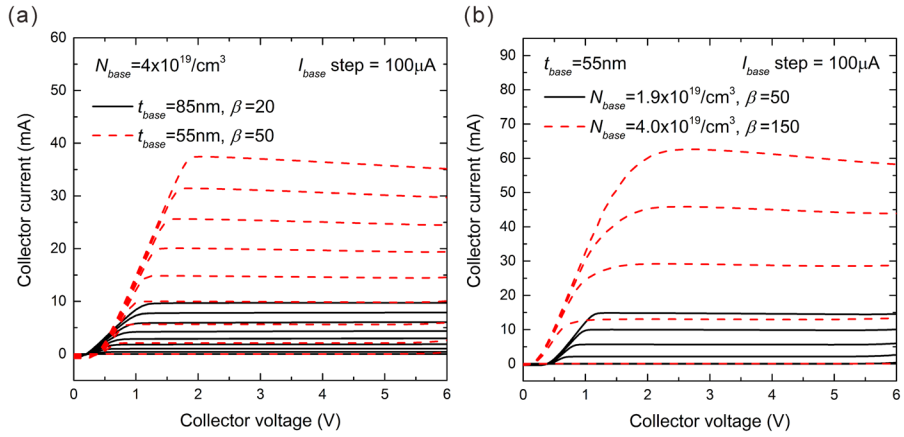

FIG. 3. I_c-V_{ce} characteristics of InGaP/GaAs HBTs with different base doping concentrations (N_{base}) and base thicknesses (t_{base}). (a) HBTs with same base doping concentration of 4×10^{19}/cm^3 (measured by SIMS), and different base layer thickness t_{base} = 55 nm and 85 nm, (b) HBTs with same base layer thickness of 55nm and different base doping concentration N_{base} = 4.0×10^{19}/cm^3 and 1.9×10^{19}/cm^3.

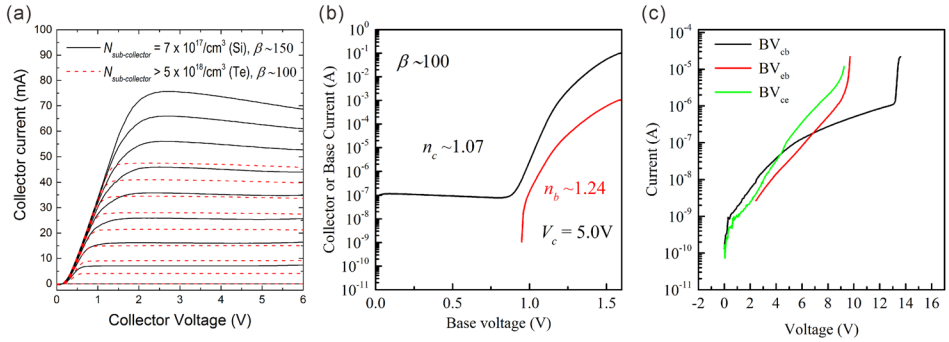

FIG. 4. (a) I_c-V_{ce} characteristic, with I_{step}=60 μA. (b) Gummel plot and (c) breakdown voltages (BV_{ceo}, BV_{cbo} and BV_{ebo}) of InGaP/GaAs HBTs with base doping concentration of 1.9×10^{19}/cm^3, base thickness of 55 nm and sub-collector concentration of $> 5 \times 10^{18}$/cm^3 with Te as sub-collector dopant species.

plot in Fig. 4(b) shows the DC current gain (β) of 100, collector current and base current ideality factors (n_c and n_b) of 1.07 and 1.24, respectively. In addition, the breakdown voltages at base (BV_{ceo}), emitter (BV_{cbo}) and collector open circuit (BV_{ebo}) are 9.25 V, 13.6 V, and 9.25 V, respectively. This performance is comparable with the device performance on GaAs substrate,[20] with a slightly lower breakdown voltage which could be due to the dislocations originated from the starting Ge film.

To test the uniformity of device performance across the wafer, we have fabricated large quantity devices on 1″×1″ samples diced from 200 mm wafer at different locations to statistically understand the HBT's performance variation. Table II shows the mean and variation of the DC current gain, breakdown voltages, turn-on voltage and ideality factors of the HBTs across the 200 mm wafer. The mean value of the collector and base ideality factors are 1.06 and 1.42, with variation ~ 1.3% and 7.8 %, respectively. The mean value of the BV_{ceo}, BV_{cbo} and BV_{ebo} are 9.43 V, 13.8V and 9.48 V, respectively. The variation of the breakdown voltage is < 3% across the 200 mm wafer. Approximately 16% variation in DC current gain is observed, which largely depends on the variation of the base current. The variation of the base current may be attributed to several factors, such as defect density, non-uniform base thickness during structure growth, and slight variation in device fabrication process from sample to sample.

Based on the HBT DC performance presented in Fig. 4, the RF performance of the HBT with an emitter area of 1 μm × 1 μm is numerically simulated. The current gain cutoff (f_T) is estimated to be about 20 GHz. A much higher f_T could be expected by reducing the dimension of the emitter area. From the simulation, we also noticed that a stable AC beta gain can be achieved when the base doping concentration is in between 1×10^{18} and 3×10^{19}/cm^3, as shown in Fig. 5(a). The AC beta gain decreases significantly in the low frequency regime when the base doping concentration is above 1×10^{20}/cm^3. In addition, the AC current gain is not affected significantly by the base thickness, as shown in Fig 5(b).

In terms of reliability, the high level of defect density appears in the device layer (which is originated from the starting layer) has a major impact.[19,21,22] In this study, the TDD of both the Ge layer and device layer are in low-10^7/cm^2. To address this problem, high quality Ge substrates with TDD of mid-to low- 10^6/cm^2 which had been developed in our group previously can be used.[23,24]

TABLE II. HBT performances across the entire 200 mm wafer.

	Gain (I_c/I_b)	BV_{cbo} (V)	BV_{ebo} (V)	BV_{ceo} (V)	V_{on} (V) (at J_c= 1A/cm^2)	Ideality factor n_c	Ideality factor n_b
Mean	81.4	13.8	9.48	9.43	1.06	1.06	1.42
Variation (%)	15.6	3.0	2.2	2.9	0	1.3	7.8

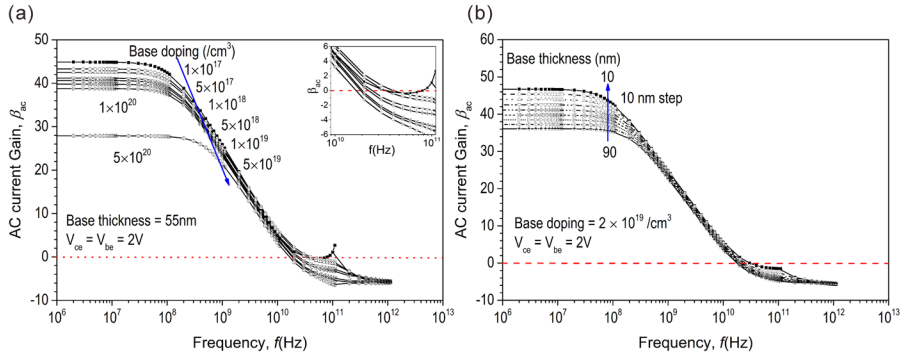

FIG. 5. Numerical simulation of RF performances of InGaP/GaAs HBTs based on the DC performance presented in Fig. 4. The AC current gain of the HBTs for various (a) base doping concentrations with the same base thickness of 55 nm and (b) base thicknesses with the same base doping concentration of 2×10^{19}/cm^3, with respect to the operating frequency.

V. CONCLUSION

We have demonstrated $In_{0.49}Ga_{0.51}P$/GaAs HBT devices with good DC performances on 200 mm silicon substrates through 100% Ge buffer layer. With the assistant of numerical simulation, HBT devices with DC current gain (β) of 100, collector current and base current ideality factor (n_c and n_b) of 1.07 and 1.24 are achievable, with optimized base doping concentration (N_{base}), base layer thickness (t_{base}), and sub-collector doping concentration ($N_{sub\text{-}collector}$). By reducing the base thickness and base doping concentration, the DC current gain can be increased. The average breakdown voltages of BV_{ceo}, BV_{cbo}, and BV_{ebo} is 9.43, 13.8 and 9.48 V, respectively. We have also conducted numerical simulation of RF performance of the HBT devices based on the measured DC parameters, the current gain cutoff frequency (f_T) of 20 GHz is expected. This result enables the potential for monolithic integration of InGaP/GaAs HBTs with Si CMOS control circuitry on a common Si platform for applications such as power amplifiers.

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