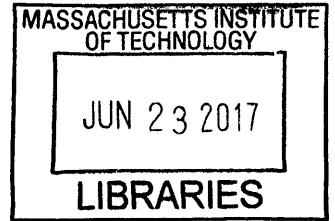


A Pipelined Analog-to-Digital Converter with Low-gain, Low-bandwidth Op-amps

by

Taehoon Jeong

B.S., Electrical and Computer Engineering
Seoul National University (2015)



Submitted to the Department of Electrical Engineering and Computer Science **ARCHIVES**

in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering and Computer Science

at the

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Abstract

Designing a high-gain, high-bandwidth op-amp for pipelined ADCs in fine-line CMOS technology has become increasingly challenging. In order to address this issue, this thesis presents the shadow-ADC-assisted digital calibration technique. The proposed technique relaxes op-amp performance requirements by removing op-amp-induced charge-transfer errors in the digital domain. A proof-of-concept pipelined ADC has been designed in 28nm FDSOI CMOS technology and is currently being fabricated.

Thesis Supervisor: Anantha P. Chandrakasan

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Thesis Supervisor: Hae-Seung Lee

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For the past two years at MIT, I have greatly enjoyed my life as a graduate student. I have been very fortunate to be surrounded by many people who have been willing to help me. I hope that I can return their favors a little bit by mentioning their names here.

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Chapter 1

Introduction

Analog-to-digital converters (ADCs) are key building blocks for electronic systems that need to interface with the real world analog signals. Numerous ADC topologies have been developed to satisfy different kinds of resolution and speed requirements. Among various ADC architectures, pipelined ADCs are well suited for applications that need medium to high resolution at a few Msample/s to 1Gsample/s sampling rate. The performance space covered by pipelined ADCs is shown in Figure 1-1. Especially, pipelined ADCs can achieve both high resolution and sampling rate, which cannot be easily reached by any other topology [3].

Conventional pipelined ADCs employ high-gain, fast-settling op-amps to provide high precision and sampling rate. However, such op-amp design has become increasingly difficult due to the low intrinsic gain and reduced voltage headroom that accompany CMOS technology scaling. In an advanced CMOS technology, an op-amp that meets the gain and bandwidth requirements of conventional high performance pipelined ADC may burn prohibitively large power. In this work, a digital calibration scheme addresses this issue by eliminating inaccuracies associated with low-gain, low-bandwidth op-amp.

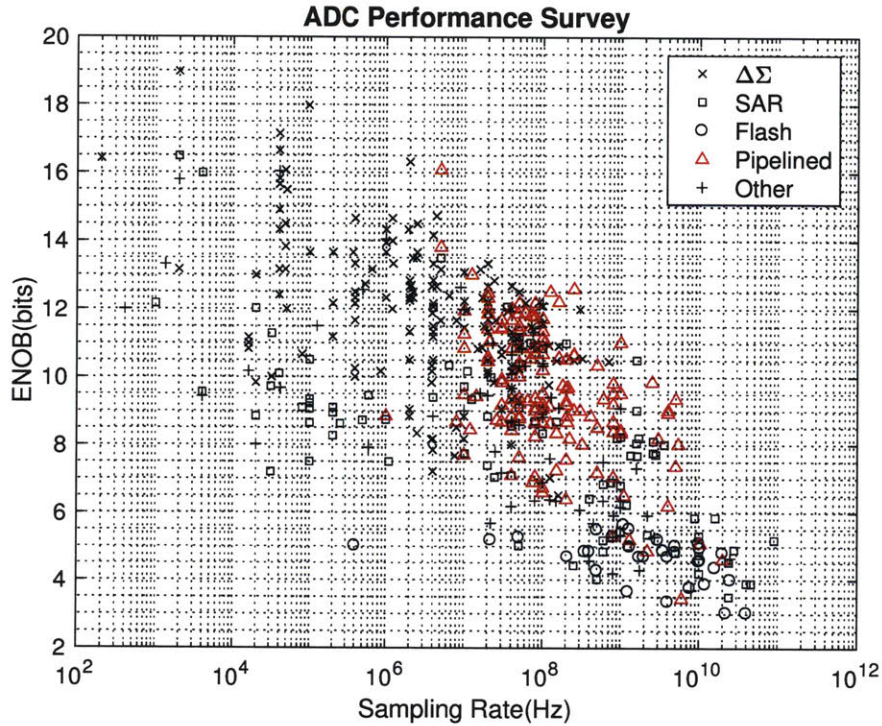


Figure 1-1: ADC performance survey (ISSCC 1997-2016 and VLSI 1997-2016) [1]

1.1 Previous Literature

In a deep-submicron technology, high-performance op-amp design has proven to be extremely challenging. Ever decreasing intrinsic gain calls for either gain-enhancement technique or multi-stage topology at the expense of increased power consumption, noise and stability issues. Low power supply is also problematic, as it reduces output range and requires larger capacitance to satisfy the signal-to-noise ratio (SNR) requirement. Figure 1-2 shows the performance of pipelined ADCs that are implemented in technologies below 32nm. Compared to Figure 1-1, the highest ENOB achieved by pipelined ADC architecture became lowered, which implies the effects of technology scaling. As summarized in Table 1.1, various techniques have been proposed to circumvent these issues and exhibit their own pros and cons.

Digital calibration has been one of popular ways to employ low-gain, slow-settling op-amps in a pipelined ADC. By taking advantage of digital computation, the principle of this approach is to digitally calibrate the multiplying digital-to-analog con-

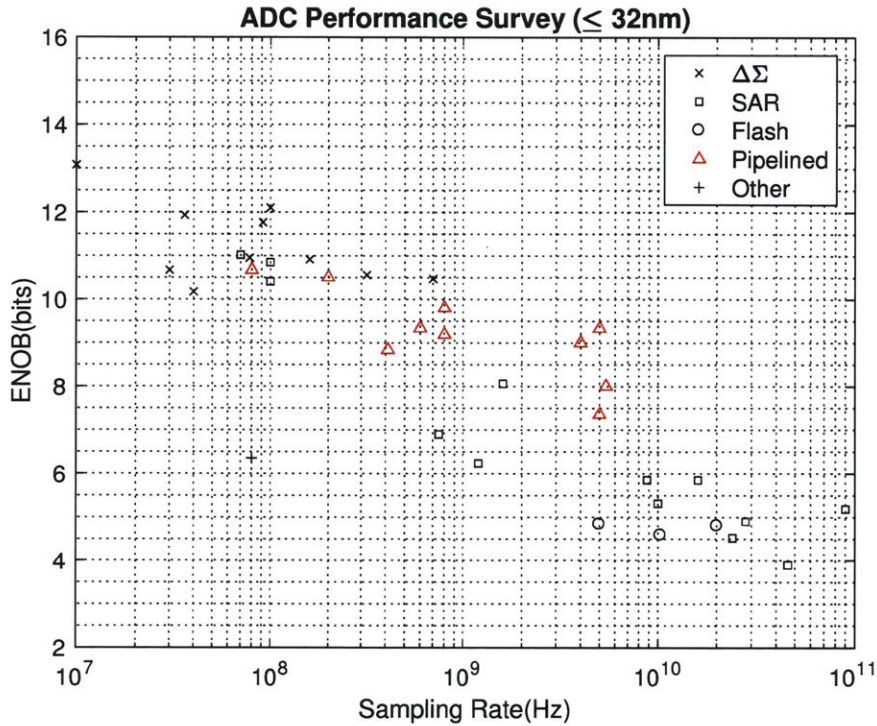


Figure 1-2: ADC performance survey (technology node below 32nm) [1]

verter (MDAC)’s charge-transfer error caused by non-ideal op-amps [4–13]. In one approach, the inter-stage gain error and/or weakly-nonlinear charge-transfer error is digitally measured and corrected by pseudo-random dithering injection and dithering correlator [4–9]. While this technique successfully cancels out the MDAC non-ideality, a portion of the op-amp output range should be allocated to the dithering injection

Category	Reference	Approach
Digital Calibration	[4–9]	Pseudo-random dithering injection
	[10–13]	Least mean square (LMS) algorithm
	This Work	Shadow-ADC-assisted
Analog Circuit Technique	[14]	Virtual ground reference buffer (VGRB)
	[15, 16]	Correlated level shifting (CLS)
	[17]	Summing-node signal amplifier
Op-amp Replacement	[18, 19]	Open-loop gain amplifier
	[20–22]	Zero-crossing-based (ZCB)
	[23, 24]	Bucket brigade
	[25–27]	Ring amplifier

Table 1.1: Summary of previous literature

and make this technique undesirable in an advanced CMOS technology. Least mean square (LMS) algorithms have also been exploited to model the gain error or MDAC nonlinearity and calibrate it [10–13]. Provided a proper cost function is defined, the LMS algorithm estimates model constants of charge-transfer error that minimizes its cost function. However, in these techniques, pre-estimated feedback factor can differ considerably from the real value [10, 11] or very accurate test input signal is needed [12].

In the context of relaxing op-amp requirements, novel analog circuit techniques have also been invented [14–17]. Virtual ground reference technique (VGRB) improves overall MDAC performance including loop gain, bandwidth and noise by using bootstrapping action of reference buffers [14]. Because of less-than-unity gain and finite bandwidth of reference buffers, its bootstrapping action is not ideal and improvements of VGRB technique can be limited. Correlated level shifting (CLS) effectively increases MDAC loop gain and output swing by sampling the MDAC gain error at op-amp output node and cancel it in the feedback path [15, 16]. However, the increased load capacitance and additional time for level shifting result in lower speed. In [17], an adjustable gain amplifier forms an auxiliary path between the first stage and the second stage summing nodes and transfers the amplified first stage summing node voltage error to the second stage. Having amplifier’s gain adjusted as same as the inverse of the feedback factor, the charge-transfer error is compensated. The drawback is the increased power consumption to employ a highly-linear, fast-settling adjustable gain amplifier, as well as the need for continuous background calibration of the amplifier gain.

Rather than using a conventional op-amp-based MDAC, some pipelined ADCs completely replace their op-amps with other circuitries that are more energy-efficient and amenable to fine-line technologies [18–27]. Open-loop residue amplifier in [18, 19] achieves significant power reduction compared to its closed-loop counterpart, utilizing an LMS algorithm to find its nonlinear transfer function polynomial coefficients. The downside is that the open-loop amplifier characteristics are greatly affected by ambient supply and temperature variations and thus the background calibration must

run continuously. Op-amps in a zero-crossing-based (ZCB) pipelined ADC are replaced by a simple zero-crossing detector and current sources based on an observation that the ideal charge-transfer happens when the virtual ground condition is achieved [20–22]. Although ZCB pipelined ADCs are more power efficient than traditional pipelined ADCs, the nonlinearity of current sources should be addressed to attain high-resolution [22]. Residue amplification of bucket brigade circuits is done when the sampled charge of one stage is transferred to its scaled down following stage without loss of signal component [23,24]. Unfortunately, the charge transfer action of bucket brigade circuit is inherently nonlinear and must be corrected by using complex digital calibration techniques. The most recently proposed alternative MDAC topology uses ring amplifiers. Ring amplifier is essentially a ring oscillator with a dead-zone inserted into the last stage inverter to make it function as an amplifier [25–27]. Ring-amplifier-based pipelined ADCs show remarkable power efficiency, but its speed is limited and the PVT tolerances have yet to be addressed.

1.2 Thesis Organization

This thesis is organized as follows. Chapter 2 provides a brief review of the conventional pipelined ADC and serves as a foundation for later chapters. The general architecture and conversion process of a pipelined ADC are explained first. Then, the chapter discusses performance limitations induced by each circuit component. In Chapter 3, a shadow-ADC-assisted digital calibration technique is introduced. The key concepts, calibration procedure and design considerations of the proposed scheme will be described. A proof-of-concept pipelined ADC has been designed to show the effectiveness of the proposed scheme, and its circuit implementation and simulation results will be detailed in Chapter 4 and Chapter 5, respectively. Finally, Chapter 6 summarizes the contributions of this work and suggests future research directions.

Chapter 2

Pipelined ADC Review

Chapter 2 first focuses on the general overview of a pipelined ADC architecture. Then, the structure and the operation of conventional op-amp-based pipelined ADCs are described. Finally, the chapter analyzes various error sources in the conventional pipelined ADC designs with an emphasis on op-amp. The op-amp-induced inaccuracies are addressed by the digital calibration technique presented in Chapter 3.

2.1 Pipelined Analog-to-Digital Conversion

Figure 2-1 illustrates the architecture of a pipelined ADC. The ADC is a cascade of multiple stages that are functionally equivalent. Each stage consists of a sub-ADC, a DAC and a residue amplifier, except for the last stage that only contains a sub-ADC. The DAC and the residue amplifier are usually integrated in one circuit block called multiplying digital-to-analog converter (MDAC).

As its name indicates, a pipelined ADC adopts the divide-and-conquer strategy to perform an analog-to-digital conversion. The first stage samples the system input and its low-resolution sub-ADC digitizes the sampled value. The sub-ADC bits are then fed into the DAC whose output is subtracted from the stage input and amplified by a factor of 2^n to recover the full signal range. The resulting residue is passed onto the second stage and further quantized by performing the same operation. After quantization completes at the sub-ADC-only final stage, decision bits from each stage

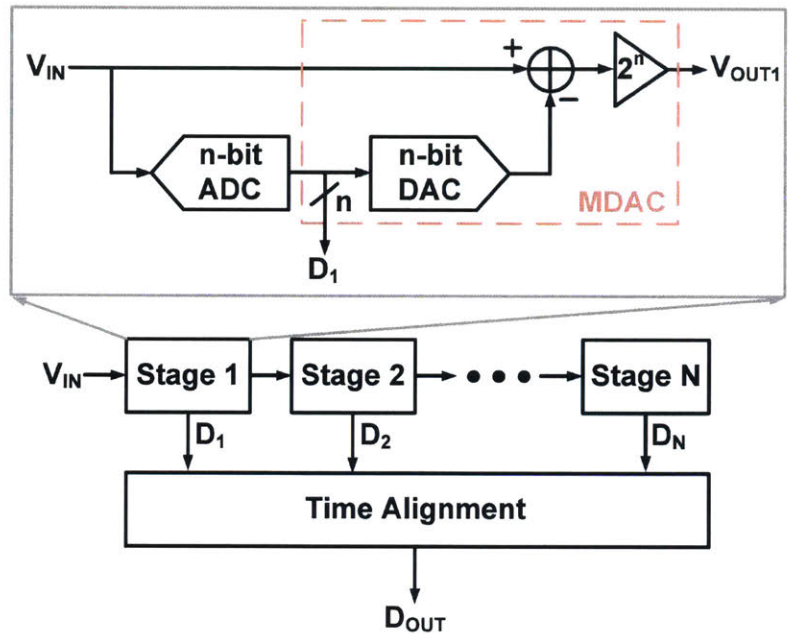


Figure 2-1: Pipelined ADC architecture

are combined together in the time-alignment block to provide a high-resolution digital equivalent of the system input. In order to clarify the pipelined analog-to-digital conversion process, a three-bit example with 1bit/stage architecture is shown in Figure 2-2.

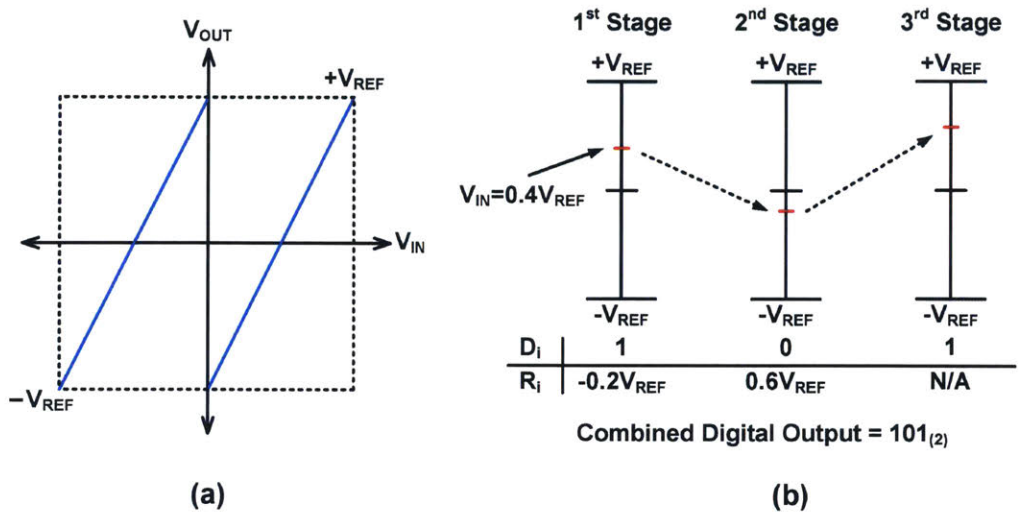


Figure 2-2: A three-bit example of pipelined analog-to-digital conversion (a) One-bit stage residue plot (b) Conversion process

2.1.1 Redundancy

Due to the circuit non-idealities, sub-ADC thresholds often deviate from their ideal values. When this happens, the stage residue exceeds its regular range ($\pm V_{ref}$) and wide codes and missing codes occur. Figure 2-3a shows the two-bit first stage residue plot when a sub-ADC threshold error exists. It is observed that the first stage residue (V_{OUT1}) becomes larger than $+V_{REF}$, which saturates subsequent stages. As a result, the overall ADC transfer curve is obtained as Figure 2-3b. Information is lost as different input levels become indistinct in the digital domain.

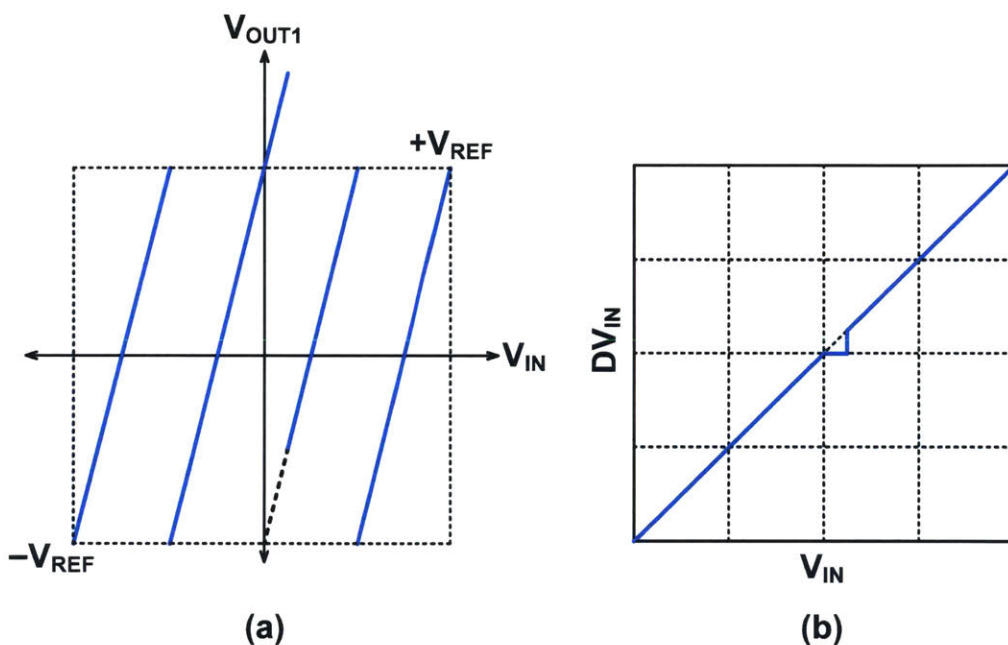


Figure 2-3: Sub-ADC threshold error example (a) 2-bit first stage residue plot (b) Overall ADC transfer curve

In order to prevent this problem, redundancy is employed in many pipelined ADCs [28]. By adding extra bit decision levels to the sub-ADC without increasing the interstage gain, the entire pipelined ADC becomes tolerant to a certain amount of sub-ADC threshold deviations. Figure 2-4a illustrates how the residue plot is changed after one-bit redundancy is applied to the first stage sub-ADC of Figure 2-3a. Although the first stage sub-ADC still makes a mistake, backend stages can always resolve the first stage residue and thereby compensate the error as in Figure 2-3b.

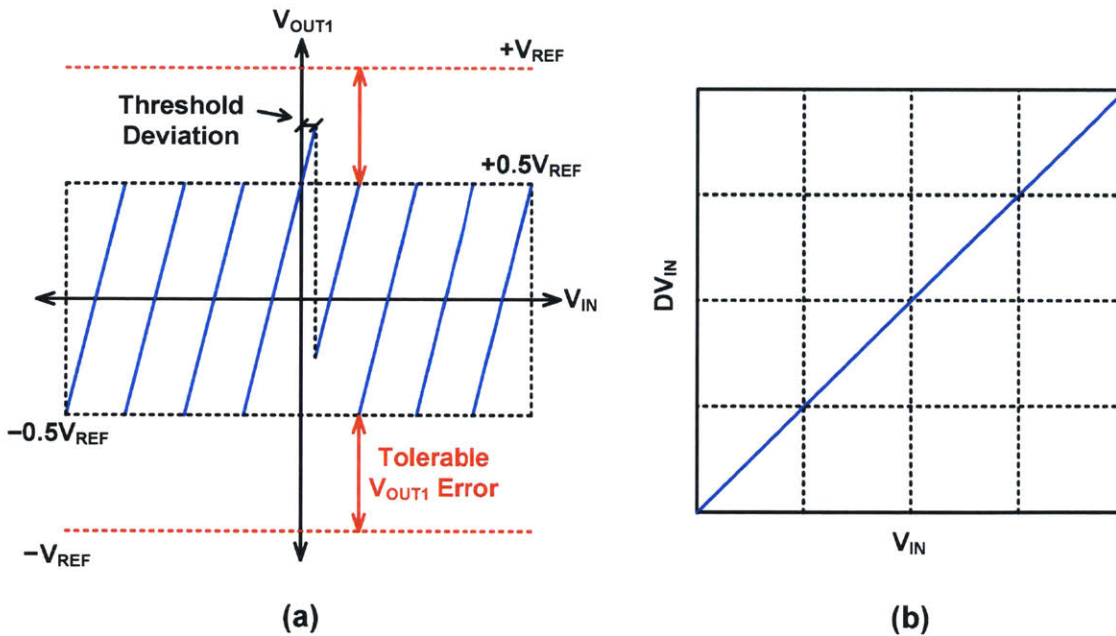


Figure 2-4: Redundancy example (a) (2+1)-bit first stage residue plot (b) Overall ADC transfer curve with redundancy

When the decision bits are combined in the time-alignment block, the LSB of the first stage and the MSB of the second stage are overlapped since the interstage gain has been maintained as 4.

2.2 Conventional Pipelined ADC

When it comes to the circuit implementation of a pipelined ADC, flash ADC has been the most popular topology for the sub-ADC. As previously mentioned, each pipeline stage does not resolve many bits and thus flash ADC becomes a viable option. More importantly, the bit decision time of flash ADC is superior to other types of ADC and it makes flash ADC be compelling to high-speed pipelined ADCs. For the MDAC, conventional pipelined ADCs have used op-amp-based switched capacitor circuits in a negative feedback configuration. The negative configuration provides accurate and reliable amplification for pipeline stages, provided that the op-amp has a high gain and settles fast, which is a difficult task in nanoscale CMOS.

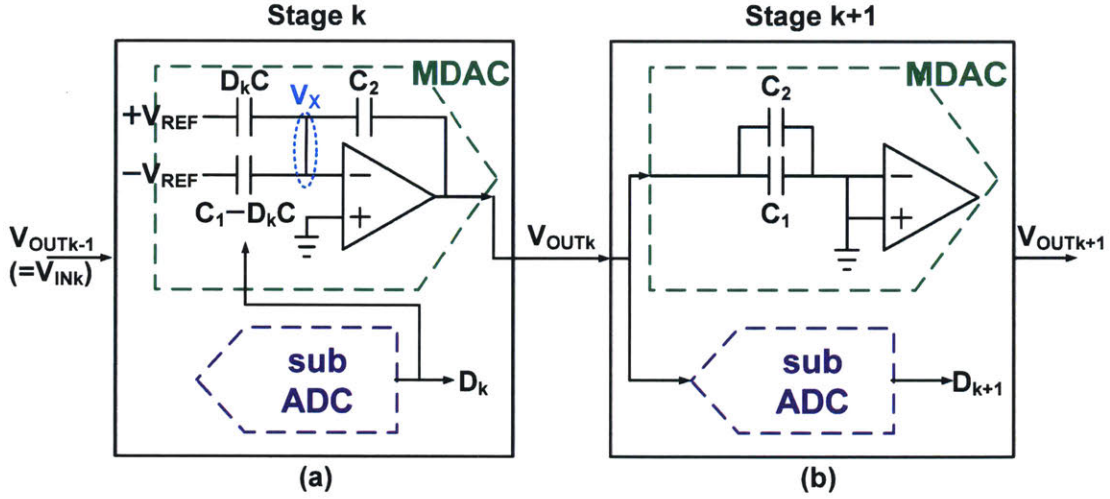


Figure 2-5: Two adjacent stages of conventional pipelined ADC (a) Charge-transfer phase (b) Sampling phase

Figure 2-5 describes how conventional pipeline stage works. Each stage operates in two clock phases. During the sampling phase, the stage input voltage is sampled on C_1 , C_2 , and the sub-ADC sampling capacitor. Note that C_1 consists of multiple unit capacitors in a multi-bit pipeline stage. Then, the charge transfer phase begins and the sub-ADC performs bit decisions. Resulting digital bits are delivered to the time-alignment block and MDAC. Having received the digital bits, the MDAC flips C_2 around the op-amp and connects its output node and summing node. Unit capacitors of C_1 are driven by either positive or negative reference voltage depending on the sub-ADC bit decision results. In this negative feedback network, the op-amp forces its inverting input voltage to be same as its non-inverting input voltage. Ideal op-amp whose gain and bandwidth are infinite can achieve this virtual ground condition. By assuming this ideal op-amp, the k -th stage residue voltage is derived as given below after solving a charge conservation equation at the summing node.

$$(C_1 + C_2)(V_{INk} - 0) = D_k C (V_{REF} - V_X) + (C_1 - D_k C)(-V_{REF} - V_X) + C_2 (V_{OUT} - V_X) \quad (2.1)$$

$$V_X = 0 \quad (2.2)$$

$$V_{OUTk} = \frac{C_1 + C_2}{C_2} V_{INk} - \frac{2CD_k - C_1}{C_2} V_{REF} \quad (2.3)$$

In reality, ideal sampling and charge-transfer operations cannot be achieved because of circuit non-idealities. The next section elaborates on these non-idealities.

2.3 Performance Limitations

In this section, performance-limiting factors of pipelined ADCs are enumerated and discussed.

2.3.1 Sampling Network

During the sampling phase, the sampling network of a pipeline stage can be modeled as a low-pass filter that consists of a MOS switch resistor and a sampling capacitor (Figure 2-6). Without sufficient bandwidth, the sampling network may introduce significant error to its sampled signal and hence degrade the overall ADC linearity. The nonlinear dependence of switch resistance on its input voltage can also contribute to the linearity error. The nonlinear dependence mainly comes from the varying gate-to-source voltage of the MOS switch. A bootstrapping technique proposed in [2] can provide a first-order solution for this issue. The charge-pump circuit turns on the sampling switch with a nearly-constant gate-to-source voltage, thereby reducing the first-order on-resistance dependence on the input signal and enabling rail-to-rail swing of the signal.

In addition to the nonlinearity, the MOS switch adds noise to the sampled signal.

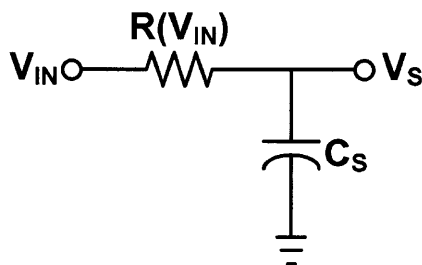


Figure 2-6: Sampling network model

In the frequency bandwidth where pipelined ADCs are designed, the total noise power of a sampling network is usually dominated by thermal noise. The thermal noise power at the output node of a sampling network can be derived as [29]

$$P_{smp,n} = \frac{kT}{C_S} \quad (2.4)$$

where k , T and C_S are the Boltzmann constant, temperature and sampling capacitance, respectively. In the design process, the sampling capacitance is determined prior to the sampling switch size by signal-to-noise ratio (SNR) specification or mismatch requirements. Then, the sampling switch size must be chosen carefully to cover the input signal bandwidth.

2.3.2 Clock Source

Electronic noise of the clock source degrades ADC performance. Noise makes the actual clock edge not occur at its ideal timing and such timing deviations are referred to as clock jitter. The outcome of the clock jitter is the input sampling noise as described in Figure 2-7. Clock jitter can be modeled as a random variable with zero mean and standard deviation σ_{jitter} . When a pure sine wave ($V_{IN}(t) = A \sin \omega t$) is input to the ADC, the SNR of the input signal and clock jitter noise is calculated as below:

$$P_{noise} = E[\Delta V_{IN}^2] = E\left[\frac{dV_{IN}}{dt} \cdot \Delta t^2\right] = E[A^2 \omega^2 \cos^2 \omega t] E[\Delta t^2] = \frac{A^2 \omega^2 \sigma_{jitter}^2}{2} \quad (2.5)$$

$$SNR_{jitter} = \frac{P_{sig}}{P_{noise}} = \frac{\frac{1}{2} A^2}{\frac{1}{2} A^2 \omega^2 \sigma_{jitter}^2} = \frac{1}{\omega^2 \sigma_{jitter}^2} \quad (2.6)$$

From Equation 2.6, it can be known that the SNR decreases when the input signal frequency gets higher. Therefore, care should be taken with the clock source design to minimize the degradation of the Nyquist frequency input SNR.

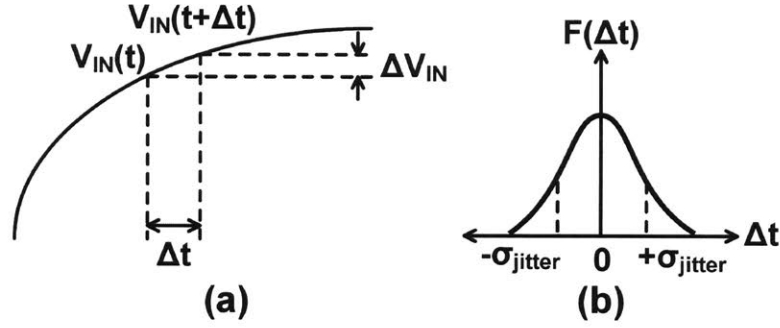


Figure 2-7: (a) Effect of clock jitter (b) Clock jitter model

2.3.3 Op-Amp

In most pipelined ADC designs, op-amps are the most important building blocks that determine overall performance of the ADC. Lack of op-amp open-loop gain and/or unity-gain bandwidth can result in severe ADC linearity degradation. Along with $\frac{kT}{C}$ noise of the sampling network, op-amps also constitute a great portion of the noise source and reduce SNR. Therefore, the relationship between op-amp non-idealities and ADC performance must be well analyzed.

Open-Loop Gain

Figure 2-8a illustrates a typical op-amp DC characteristic and how the open-loop gain is defined. Since the charge-transfer operation is a large-signal behavior, op-amp's open-loop gain is defined as

$$A = \frac{V_{OUT}(V_{IN})}{V_{IN}} \quad (2.7)$$

where V_{IN} is the voltage difference between the non-inverting node and the inverting node.

The finite open-loop gain alters Equation 2.2 and leads to slightly different result from Equation 2.3. For simplicity, other non-ideal features of op-amp are ignored.

$$V_{OUT} = \frac{\frac{C_1 + C_2}{C_2} V_{IN} - \frac{2D_{IN} - C_1}{C_2} V_{REF}}{1 + \frac{1}{A\beta}} \quad (2.8)$$

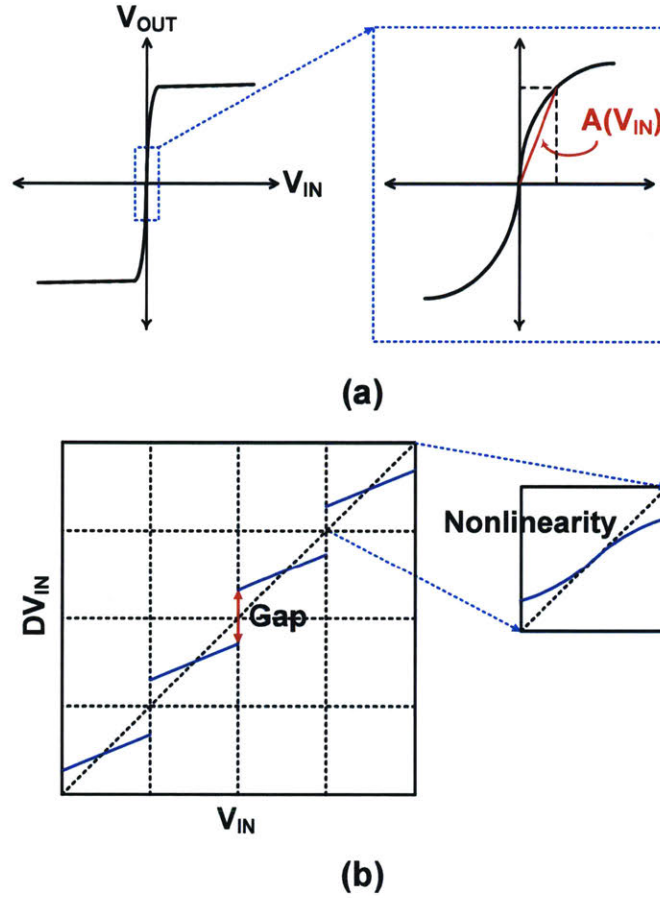


Figure 2-8: (a) Op-amp DC characteristic (b) Overall ADC transfer curve with finite gain errors

In Equation 2.8, β is the feedback factor of MDAC and defined as follows.

$$\beta = \frac{C_2}{C_1 + C_2} \quad (2.9)$$

Finite gain error is now calculated by subtracting Equation 2.8 from Equation 2.3.

$$\epsilon_{gain} = V_{OUT,ideal} - \frac{V_{OUT,ideal}}{1 + \frac{1}{A\beta}} \approx \frac{V_{OUT,ideal}}{A\beta} \quad (2.10)$$

Because of the finite gain error, the overall ADC transfer curve has discontinuities at sub-ADC threshold levels shown in Figure 2-8b. In addition to these gaps, the transfer curve segment is not linear due to the inherent op-amp nonlinearity. Therefore, the

open-loop gain must be large enough to suppress this nonlinearity in the negative feedback loop. Considering other nonlinearity factors, it is desirable to make the segment discontinuities be smaller than a quarter LSB of the backend stages.

Unity-Gain Bandwidth

Another important factor that causes ADC nonlinearity is the finite bandwidth of op-amps. A typical MDAC settling behavior is shown in Figure 2-9. A frequency compensated, single-pole op-amp is assumed. When the charge-transfer phase starts, initial switching transient may make op-amp drive its output with a constant current which is referred to as slewing. After slewing completes, linear settling begins and the remaining part of MDAC settling is done exponentially. Unless the op-amp bandwidth is infinite, the MDAC settling behavior always results in charge-transfer error. Assuming infinite open-loop gain ($V_{OUT,fin} = V_{OUT,ideal}$) and negligible slewing ($T_{slew} \approx 0$), this settling error is derived as

$$\epsilon_{BW} = V_{OUT,ideal} - V_{OUT,ideal}(1 - e^{-2\pi\beta f_u \times 0.5T_{clk}}) = V_{OUT,ideal}e^{-\pi\beta f_u/f_{clk}} \quad (2.11)$$

where f_u is the unity-gain bandwidth of op-amp. Same as the open-loop gain error, the incomplete settling error also introduces gaps in ADC transfer curve and should be minimized for ADC linearity.

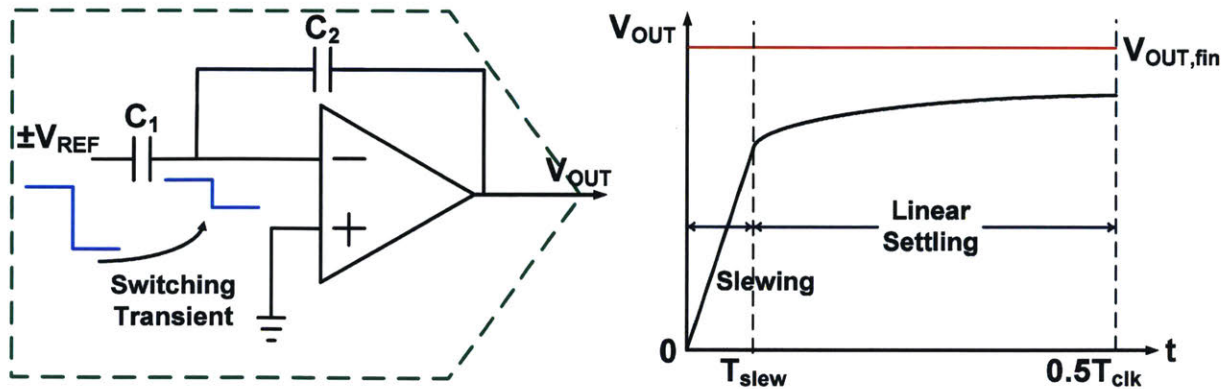


Figure 2-9: MDAC settling behavior

Noise

During the charge-transfer phase, op-amp adds its own noise to the MDAC output. In order to evaluate the output-referred total integrated noise power of op-amp, the transfer function from the op-amp input to the output is needed. Figure 2-10 shows a first-order model for the MDAC with a single-stage op-amp. It is assumed that the first pole dominates the overall frequency response of the op-amp. In Figure 2-10, $S_n(f)$, G_m , R_o and C_L stand for input-referred op-amp noise power spectral density, transconductance, output impedance and the load capacitance, respectively. For the two-stage op-amp case, C_L is replaced by C_C , which is the compensation capacitance between the stages. By Kirchhoff's law,

$$G_m(V_N - V_X) = \frac{V_{OUT}}{R_o} + sC_L V_{OUT} + sC_2(V_{OUT} - V_X) \quad (2.12)$$

$$V_X = \frac{C_2}{C_1 + C_2} V_{OUT} = \beta V_{OUT} \quad (2.13)$$

From Equation 2.12 and Equation 2.13, the op-amp noise transfer function is derived.

$$H_n(s) = \frac{1}{\beta + \frac{1}{G_m R_o} + s \frac{C_L + (1 - \beta)C_2}{G_m}} \approx \frac{1}{\beta \left(1 + \frac{s}{j2\pi\beta f_u}\right)} \quad (2.14)$$

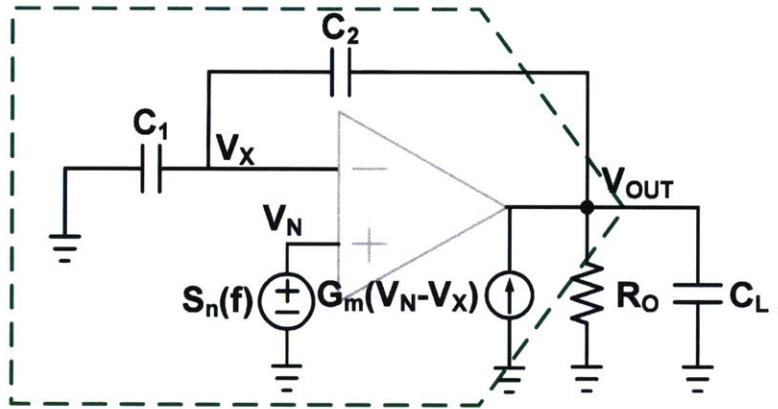


Figure 2-10: MDAC charge-transfer noise model

By integration, the op-amp total noise power at the MDAC output is obtained.

$$P_{n,opamp} = \int_0^{\infty} |H_n(f)|^2 S_n(f) df \quad (2.15)$$

Thermal noise usually outweighs other noise sources and therefore,

$$P_{n,opamp} \approx \frac{\pi}{2} S_{n,thermal}(f) \frac{f_u}{\beta} \quad (2.16)$$

Having Equation 2.16 divided by the square of MDAC gain, MDAC input-referred op-amp noise power can be calculated. The op-amp should be properly designed to meet the SNR target of the ADC.

2.3.4 Capacitor Mismatch

Mismatches between MDAC capacitors make the capacitance ratios deviate from their ideal values and thus produce ADC nonlinearity. Following charge-transfer equation helps to figure out the effects of capacitor mismatch. The elements of S_P and S_N are unit capacitors of C_1 that are connected to the positive reference voltage and the negative reference voltage, respectively. Note that the elements of S_P and S_N depend on the sub-ADC decision code.

$$\begin{aligned} V_{OUT} &= \frac{\sum_k C_{1,k} + C_2}{C_2} V_{IN} - \frac{\sum_{k \in S_P} C_{1,k} - \sum_{k \in S_N} C_{1,k}}{C_2} V_{REF} \\ &= V_{OUT,ideal} + V_{IN} \sum_k \epsilon_k - V_{REF} \left(\sum_{k \in S_P} \epsilon_k - \sum_{k \in S_N} \epsilon_k \right) \end{aligned} \quad (2.17)$$

In Equation 2.17, two effects of capacitance ratio error $\epsilon_k = \frac{C_{1,k} - C}{C_2}$ are identified. Firstly, the slope of ADC transfer curve segment increases or decreases from its ideal value. Secondly, each transfer curve segment is shifted vertically from its ideal location and the amount of shift differs from segment to segment.

To improve capacitor matching, dummy capacitors are often placed around the MDAC capacitors. Also, digital calibration algorithms such as decision boundary gap

estimation (DBGE) technique can be exploited without increasing hardware complexity [30].

2.3.5 Bit Decision Comparator

The input offset voltage and the input-referred noise of bit decision comparator are major sources of sub-ADC threshold deviation. A zero-mean random variable with standard deviation σ can be used to model the sub-ADC threshold deviation. As illustrated in Figure 2-4, redundancy does not provide infinite amount of tolerable sub-ADC threshold deviation. Therefore, bit decision comparators should be properly designed to meet below condition to prevent wide codes and missing codes.

$$(\text{MDAC Gain}) \times (3\sigma) < (\text{Tolerable Residue Error}) \quad (2.18)$$

For example, if a gain-of-eight MDAC exhibits good linearity in the output range of $\pm 400\text{mV}$ while its nominal output range is $\pm 320\text{mV}$, the tolerable residue error becomes 80mV . In this case, 3σ should be smaller than 10mV .

2.3.6 Summing Node Parasitic Capacitance

Arising from routing capacitance, op-amp input capacitance, and MDAC capacitor parasitics, summing node parasitic capacitance affects MDAC performance in various ways. When a parasitic capacitance C_P loads the MDAC summing node, MDAC feedback factor decreases as follows:

$$\beta = \frac{C_2}{C_1 + C_2 + C_P} \quad (2.19)$$

This feedback factor reduction increases open-loop gain error (Equation 2.10), settling error (Equation 2.11) and output noise power (Equation 2.16).

2.4 Summary

This chapter has reviewed basic operations and performance limiting factors of pipelined ADCs. In fine-line technologies, the major challenge of low-power, high-performance pipelined ADC design comes from op-amps due to the reduced device gain and supply voltage. As previously discussed, op-amp non-idealities aggravate the linearity and signal-to-noise ratio of pipelined ADCs. The next chapter proposes a digital calibration technique that addresses this issue.

Chapter 3

Shadow-ADC-Assisted Digital Calibration

In this chapter, the shadow-ADC-assisted digital calibration scheme is introduced. The intuitions and the advantages of the proposed technique are explained first. Then, a global ADC architecture that realizes the calibration concept is described. Specific calibration procedure follows the global architecture. Finally, a number of design considerations are discussed.

3.1 Calibration Concept

Until now, the behavior of MDAC output node has only been focused. However, it is also important to analyze how the summing node of MDAC is affected by op-amp-induced errors. Figure 3-1 shows the settling behavior of an MDAC including its summing node voltage. For simplicity, slewing is assumed to be negligible. Note that the parasitic capacitance C_P loads the summing node. By ignoring the op-amp for a moment, one can notice that the rest of MDAC is just a capacitive divider. Therefore, the voltage change at the MDAC summing node is proportional to that at the output node. The ratio between these two voltage changes is equal to the MDAC feedback factor.

$$\Delta V_X = \frac{C_2}{C_1 + C_2 + C_P} \Delta V_{OUT} = \beta \Delta V_{OUT} \quad (3.1)$$

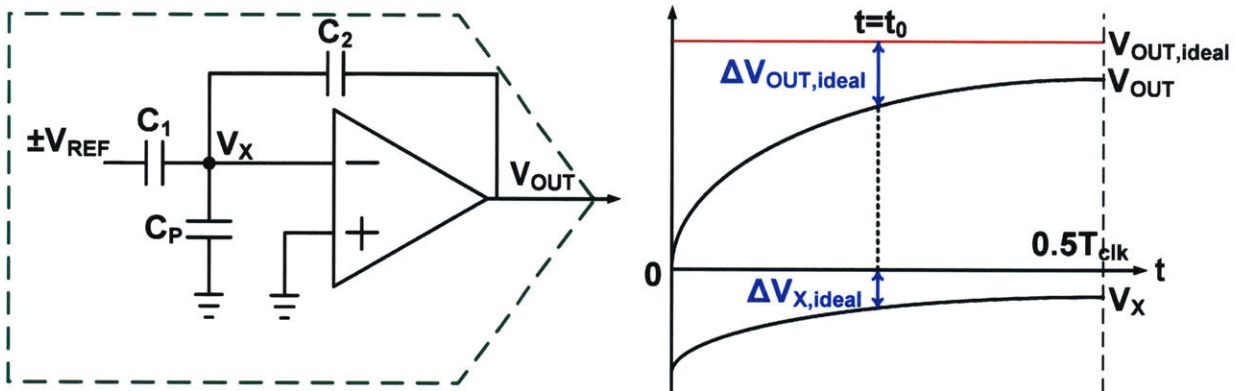


Figure 3-1: Settling behavior of critical nodes in a MDAC

The ideal charge-transfer happens when the MDAC summing node voltage becomes equal to the virtual ground ($V_X = 0$). At an arbitrary time t_0 , the summing node voltage V_X must increase by $\Delta V_{X,ideal}$ to achieve the virtual ground condition. Increasing V_X by $\Delta V_{X,ideal}$ is equivalent to increasing V_{OUT} by

$$\Delta V_{OUT,ideal} = \frac{\Delta V_{X,ideal}}{\beta} = \frac{0 - V_X}{\beta} = -\frac{V_X}{\beta} \quad (3.2)$$

Equation 3.2 leads to an interesting conclusion as follows.

$$V_{OUT,ideal} = V_{OUT} + \Delta V_{OUT,ideal} = V_{OUT} - \frac{1}{\beta} V_X \quad (3.3)$$

According to Equation 3.3, the ideal MDAC output voltage can be obtained by subtracting $\frac{1}{\beta} V_X$ from V_{OUT} even in the middle of settling. This means that if the MDAC feedback factor β and the summing node voltage V_X are known accurately, the errors caused by finite op-amp gain and bandwidth will be completely cancelled out. In addition to these nonlinearity errors, the input-referred noise and offset voltage of op-amp can also be removed as their gains from the op-amp input to the MDAC output node are equal to $\frac{1}{\beta}$. This property was recognized in [10], but the paper used pre-estimated feedback factor which can limit the calibration performance in actual ADC implementations.

3.2 Global Architecture and Calibration Procedure

Figure 3-2 shows the global architecture of an ADC that corrects its first stage op-amp-induced errors. In order to measure the summing node voltage and the feedback factor, a low-resolution shadow ADC is employed. Due to the small signal range of the summing node voltage, two switched-capacitor amplifiers are placed before the shadow ADC to provide enough gain. An unity-gain buffer is inserted between the switched-capacitor amplifiers and the first stage summing node to minimize the first stage parasitic capacitance loading from the switched-capacitor amplifier.

The proposed calibration is executed in the digital domain by using Equation 3.4. Before the normal operation of the ADC begins, the feedback factor value is precisely measured. Once the feedback factor is determined, its value is frozen throughout the entire analog-to-digital conversion. During the normal ADC operation, the summing node voltage is measured by the shadow ADC for every input sample.

$$DV_{OUT,calibrated} = DV_{OUT} - \frac{1}{\beta}DV_X \quad (3.4)$$

The remainder of this section explains how the feedback factor is acquired.

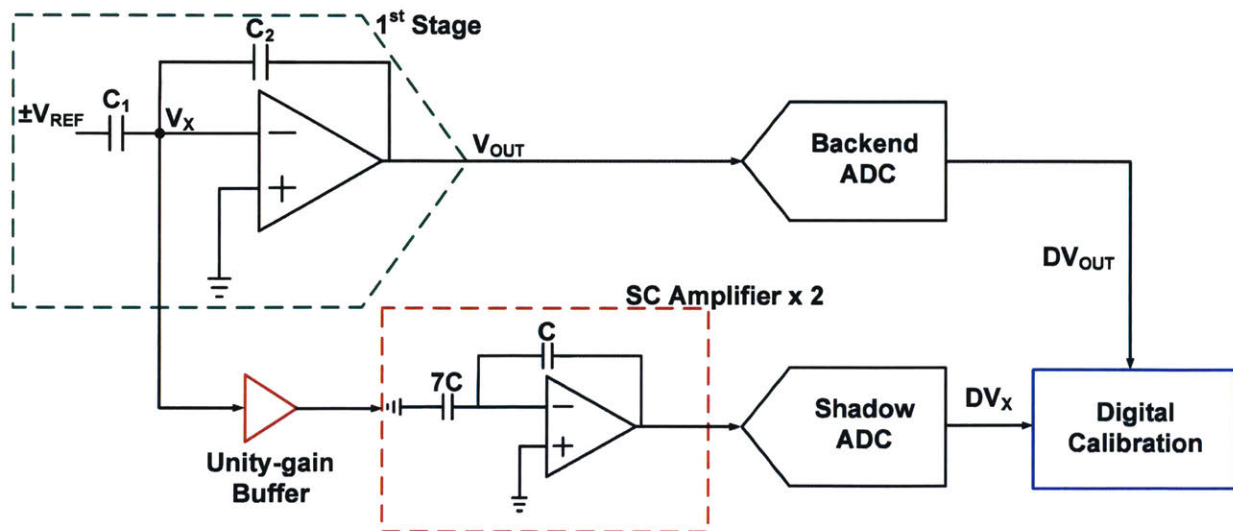


Figure 3-2: Global ADC architecture

3.2.1 Feedback Factor Measurement

Due to the device mismatches, an op-amp always has a small amount of input offset. Having recognized this input offset voltage (V_{OS}), Equation 2.7 is modified:

$$V_{OUT} = A(V_{IN} + V_{OS}) \quad (3.5)$$

The charge conservation equation is now solved again with Equation 3.5. For this time, the summing node voltage is also evaluated.

$$V_{OUT} = \frac{\frac{C_1 + C_2}{C_2} V_{IN} - \frac{2D_k - C_1}{C_2} V_{REF} + \frac{1}{\beta} V_{OS}}{1 + \frac{1}{A\beta}} \quad (3.6)$$

$$V_X = \frac{\frac{1}{A} \frac{C_1 + C_2}{C_2} V_{IN} - \frac{2D_k - C_1}{AC_2} V_{REF} - V_{OS}}{1 + \frac{1}{A\beta}} \quad (3.7)$$

Let's say that two pairs of (V_{OUT}, V_X) are measured for DC test inputs $+V_{TEST}$ and $-V_{TEST}$. Then, the relationship between the feedback factor and these test results is derived from Equation 3.6 and 3.7,

$$\frac{1}{\beta} = -\frac{V_{OUTP} + V_{OUTN}}{V_{XP} + V_{XN}} \quad (3.8)$$

where the subscripts P and N denote the positive and negative test input cases, respectively. Therefore, after two test measurements, the MDAC feedback factor value can be obtained by using Equation 3.8. It should be noted that only sign inversion is needed to implement two test voltages. Neither their absolute values nor settling behaviors are important [12].

Because the MDAC output voltage and the summing node voltage are measured by ADCs, quantization noise exists in each measurement. Thanks to the random circuit noise, averaging many digital outputs reduces the quantization noise to a negligible level. It is possible since the test inputs are DC signals. During the feedback factor

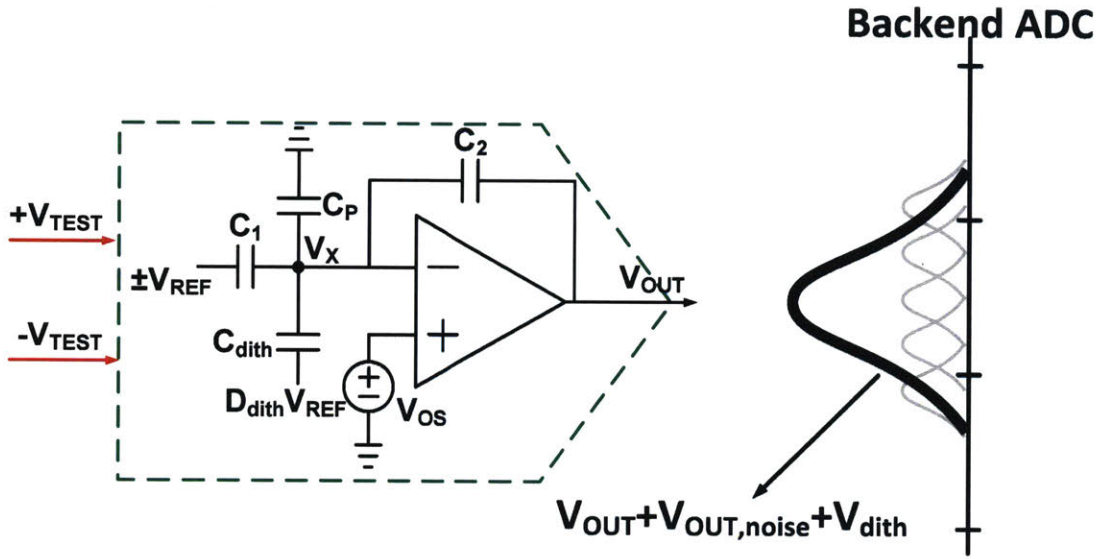


Figure 3-3: Feedback Factor Extraction

measurement, a small amount of dithering is injected to facilitate the V_{OUT} averaging process. As shown in Figure 3-3, the dithering makes V_{OUT} distribution cover multiple LSBs of the backend ADC and thereby the averaged V_{OUT} converges faster than the no-dithering case. During the normal conversion, this dithering injection does not operate and the output range of op-amp remains intact [4–9]. For V_X averaging, no dithering injection is necessary as the unity-gain buffer and two switched-capacitor amplifiers provide enough noise to the shadow ADC.

3.3 Design Considerations

In this section, a number of architecture-level design considerations are discussed.

3.3.1 Offset Error

Offset error of ADCs are usually well tolerated in most applications. However, it can be problematic during the feedback factor measurement. If either the backend ADC or the shadow ADC (including the shadow ADC signal conditioning chain) has an offset error, the error is not cancelled out in Equation 3.8 as the signal components.

Thus, the measured feedback factor value deviates from the real value. This degrades the calibration performance.

Two chopping switches can resolve this issue (see Figure 4-1). For each test voltage case, offset-error-free results are obtained by taking the difference of two measurement results, one measured in the normal switch configuration and the other measured in the crossed switch configuration. Once the feedback factor is acquired, the chopping switches are frozen in their normal configuration since the ADC can live with offset errors during the normal analog-to-digital conversion.

3.3.2 Summing Node Signal Conditioning Path

Even the feedback factor is perfectly measured, the proposed digital calibration still suffers from the quantization noise of both the backend ADC and the shadow ADC (Equation 3.4). Especially, the quantization noise introduced in DV_X can be significant as it gets amplified in the digital domain. Therefore, the summing-node-referred resolution of the shadow ADC has to be large enough. In order to enhance this effective resolution of the shadow ADC, two gain-of-eight switched-capacitor amplifiers are employed in the prototype ADC.

The gain of the summing node signal conditioning path does not need to be known accurately. In the actual feedback factor measurement process, the obtained value is equal to

$$\frac{1}{A_{con}\beta} = -\frac{\text{MEAN}(DV_{OUTP}) + \text{MEAN}(DV_{OUTN})}{\text{MEAN}(DA_{con}V_{XP}) + \text{MEAN}(DA_{con}V_{XN})} \quad (3.9)$$

where A_{con} is the total gain of the conditioning path. During the normal ADC operation, the shadow ADC digitizes the summing node signal which is amplified by the same path. Therefore, A_{con} is cancelled out in the digital domain,

$$DV_{OUT,calibrated} = DV_{OUT} - \frac{1}{A_{con}\beta}D(A_{con}V_X) = DV_{OUT} - \frac{1}{\beta}DV_X \quad (3.10)$$

and the calibration result becomes exactly same as Equation 3.4.

One might worry about the linearity of the summing node signal conditioning

path since the switched-capacitor amplifiers have to use low-gain op-amps. For the 12-bit prototype ADC, the summing node signal conditioning chain does not introduce nonlinearity. It is because the op-amp gain is high enough in such a small signal range of the summing node signal. The nonlinearity of op-amp is well suppressed in the negative feedback configuration.

In terms of noise, care must be taken with the shadow ADC path design. Same as the op-amp input-referred noise, the input-referred noise of conditioning path also gets amplified when it is referred to the MDAC output. Although the first stage op-amp noise is removed by the shadow ADC during the normal conversion, the frontend blocks of the shadow ADC path can add comparable noise power. In the prototype ADC, the first switched-capacitor amplifier has a larger unit capacitor than that of the first pipeline stage to decrease the unity-gain buffer's noise contribution.

3.4 Summary

In this chapter, the shadow-ADC-assisted calibration scheme has been proposed. The proposed calibration removes op-amp-induced errors in pipelined ADCs and thereby relaxes the design constraints of op-amps in deep-submicron technologies. Architecture-level implementation and important design considerations of the calibration technique have also been discussed.

Chapter 4

Circuit Implementation

In order to demonstrate the proposed shadow-ADC-assisted digital calibration scheme, a proof-of-concept pipelined ADC was designed in 28nm FDSOI CMOS technology and has been submitted for fabrication. In this chapter, implementation details of the prototype ADC are described.

4.1 Overall Structure

Figure 4-1 shows the block diagram of the prototype ADC. The ADC resolves its input to 11.9 bits with a sampling rate higher than 200MS/s. By using the proposed shadow-ADC-assisted calibration, the first stage op-amp-induced errors are removed to meet the target performance. The digital portion of the calibration, including feedback factor measurement is implemented off-chip.

The main ADC consists of five stages. The first stage uses 14 bit decision comparators in its sub-ADC ($\log_2(14 + 1) = 3.9\text{bit}$) and amplifies its residue by a factor of 8. From the second stage to the fourth stage, 6 bit decision comparators ($\log_2(6 + 1) = 2.8\text{bit}$) are employed in each stage and the MDAC gain of these stages is 4. The final sub-ADC-only stage digitizes its input to 4.5 bits using 22 comparators. Except for the sub-ADC in the first stage, sub-ADC input ranges are not fully utilized due to the redundancy. As a result, the 2.8-bit and 4.5-bit sub-ADCs effectively resolve 2 bits and 4 bits, respectively. Therefore, the main ADC quantizes its

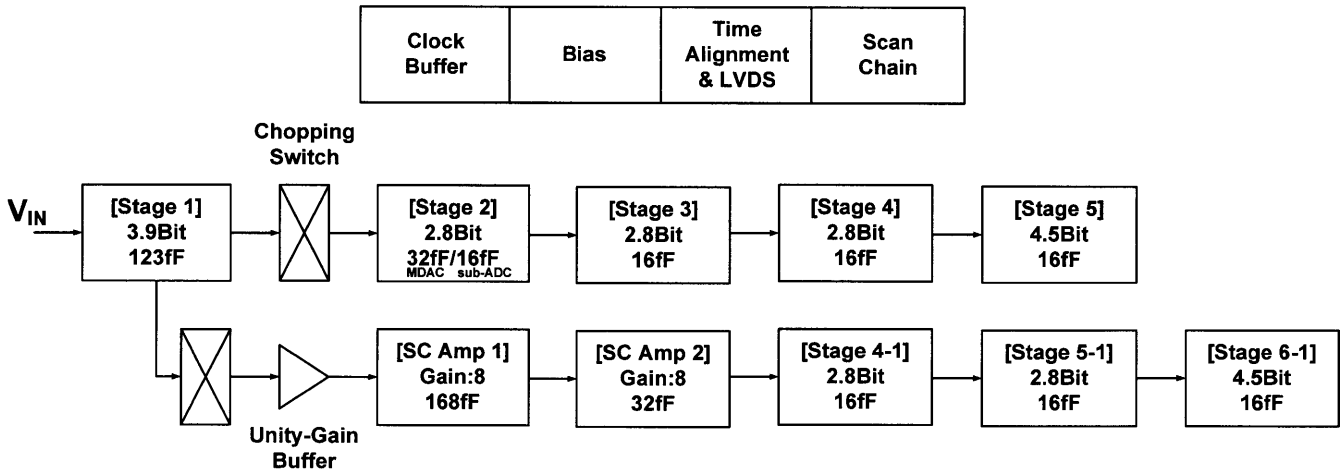


Figure 4-1: Block Diagram of the prototype ADC

input to $3.9+2\times 3+4=13.9$ bits, and 2 bits are later truncated.

The shadow ADC and its signal conditioning path contain three stages, two switched-capacitor amplifiers, and a unity-gain buffer. The signal conditioning path interfaces with the first stage summing node and amplifies the summing node signal. Because of the reduced input signal range, the effective resolution of the shadow ADC is roughly 2 bits lower than its 8.8-bit nominal resolution.

For power reduction, backend stages are scaled down. Sizes of unit capacitors and switches are reduced together by considering input-referred noise power and capacitor mismatch effects. Then, op-amp sizes are decreased accordingly. As a result, the op-amps in the first two stages of the main ADC and the first switched-capacitor amplifier consume more power than the op-amps in other stages.

4.2 MDAC

The schematic and clock waveforms of MDAC are shown in Figure 4-2. As explained in section 2.2, MDAC samples its input first (sampling phase Φ_1) and then amplifies the stage quantization error (charge-transfer phase Φ_2). Since the sub-ADC begins its bit decision (Φ_{BDC}) earlier than the charge-transfer phase, digital bits become valid before the charge-transfer phase starts. In order to prevent input-dependent charge

injection, NMOS sampling switches are turned off earlier (Φ_{1e}) than the bootstrapped tracking switches [29].

Chopping switches in Figure 4-1 are realized by adding additional bootstrapped switches to the first and the second stage MDACs for offset-free feedback factor measurement. The chopping switches are configured by the digital bits stored in the scan chain.

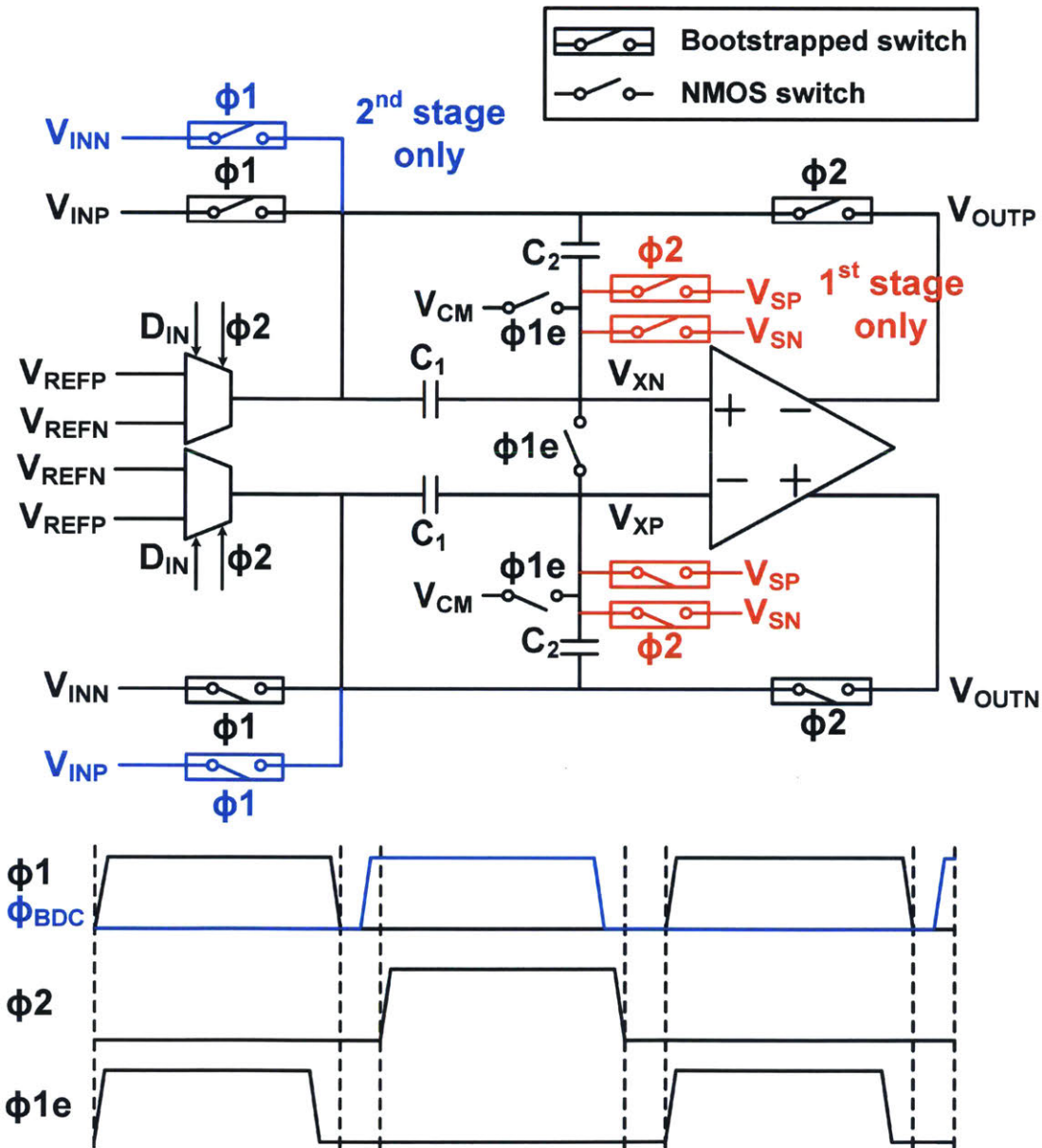


Figure 4-2: Schematic and clock waveforms of MDAC

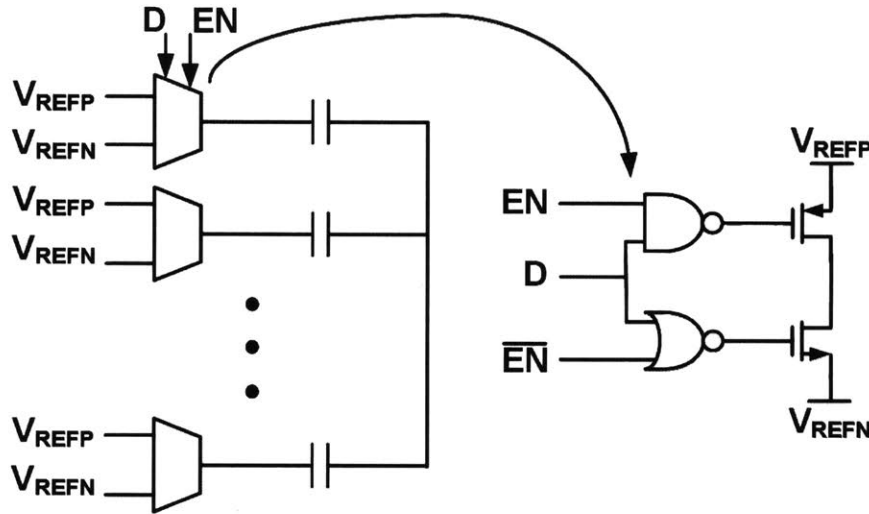


Figure 4-4: Schematic of a reference switch

4.2.3 Op-amp

Figure 4-5 depicts the schematic of a single-stage gain-boostered telescopic op-amp used in the prototype ADC [14]. Two folded-cascode op-amps enhance the gain of main telescopic op-amp in a fully-differential manner. Although the performance requirements of the first stage cannot be met with the chosen topology, the proposed shadow-ADC-assisted calibration scheme compensates the consequent inaccuracies and enables the ADC to achieve the target performance.

In order to regulate its output common-mode level, the main telescopic op-amp utilizes a standard switched-capacitor negative feedback. The output common-mode of the gain-boosting amplifier is controlled by a single transistor and a dedicated R-2R digital-to-analog converter (DAC) [31]. Because each cascode device of the main op-amp form a local unity-gain feedback loop with the corresponding gain-boosting op-amp, the R-2R DAC that determines the input common-mode of the gain-boosting amplifier can set the output common-mode as well.

Since the denominator of Equation 3.8 is proportional to the op-amp input offset voltage (V_{OS}), the divide-by-zero situation can happen when V_{OS} is too small. In such cases, the programmable minimum-sized PMOS devices (blue devices in Figure 4-5) introduce sufficient amount of input offset voltage by making a current difference. In

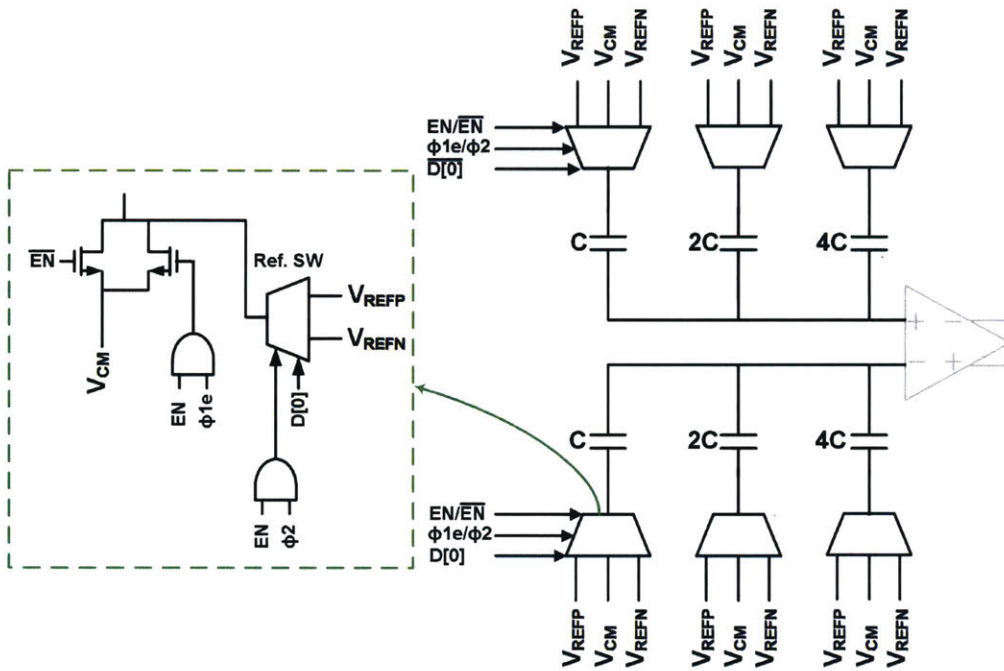


Figure 4-6: Dithering DAC schematic

increase the variance of MDAC output voltage and expedites the averaging process, capacitor mismatch is not a concern. The zero-mean of injected dithering voltage is achieved by controlling the number of averaged samples to be multiples of 8.

4.3 Sub-ADC

Figure 4-7 shows the schematic and clock waveforms of the sub-ADC. The sub-ADC consists of multiple slices that perform bit decisions with different threshold levels. During the sampling phase (Φ_1), the stage input voltage is sampled on C_S . Each bootstrapped switch shares the corresponding bootstrapping circuit with the MDAC. For the bottom plate sampling, NMOS switches are turned off earlier than the bootstrapped tracking switches (Φ_{1e}). When the sampling operation is completed, each slice connects its capacitors to the reference ladder (Φ_{REF}) and thereby generates the voltage difference between the sampled input voltage and its own threshold level at the input nodes of the comparator. After the input voltage of comparator settles, Φ_{BDC} goes high and the comparator determines its output before the MDAC charge-

transfer phase (Φ_2) starts. Note that the time difference between Φ_{REF} and Φ_{BDC} must be long enough. Otherwise, the incomplete settling of the comparator input voltage translates to the sub-ADC input offset voltage.

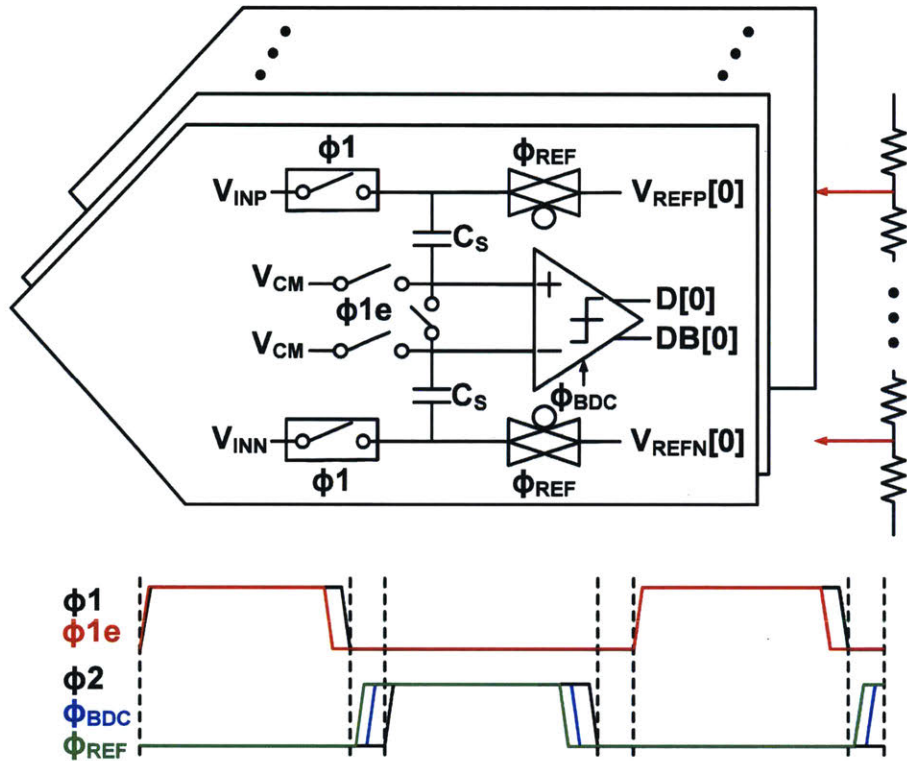


Figure 4-7: Schematic and clock waveforms of sub-ADC

4.3.1 Bit Decision Comparator

A standard strongArm comparator is adopted as the bit decision comparator topology [33]. The schematic of the comparator is shown in Figure 4-8. Since the first stage sub-ADC has a tighter input offset voltage requirement than its backend counterpart, the comparator has additional input devices for offset calibration. A dedicated reference ladder supplies dc voltages to the gates of calibration input pair. The backend comparators are sized to have small input offset voltages so that they do not exceed redundancy limits.

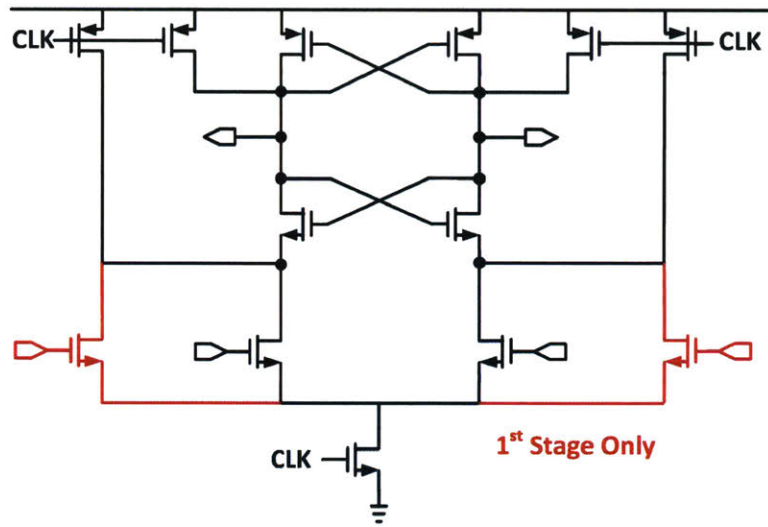


Figure 4-8: Schematic of bit decision comparator

4.4 Summing Node Signal Conditioning Circuit

4.4.1 Unity-Gain Buffer

The flipped voltage follower shown in Figure 4-9 has been chosen as the unity-gain buffer topology [34]. The flipped voltage follower features higher DC gain than the conventional source follower due to its local feedback loop. Thanks to the flipped-well structure of the low- V_T NMOS device in the given technology, the body of the input device is tied to the source without using a deep N-well device. This further increases the gain and reduce the buffer nonlinearity that arises from the backgate effect. In the small signal sense, the unity-gain buffer can introduce some phase difference between the first stage MDAC output voltage and its summing node voltage and thereby can degrade cancellation of incomplete settling error. To prevent this, the buffer is designed to have much higher bandwidth than the closed-loop bandwidth of the first MDAC.

4.4.2 Switched-Capacitor Amplifier

As shown in Figure 4-10, the schematic and clock waveforms of the switched-capacitor amplifier are identical to those of the normal MDAC except for the reference switches.

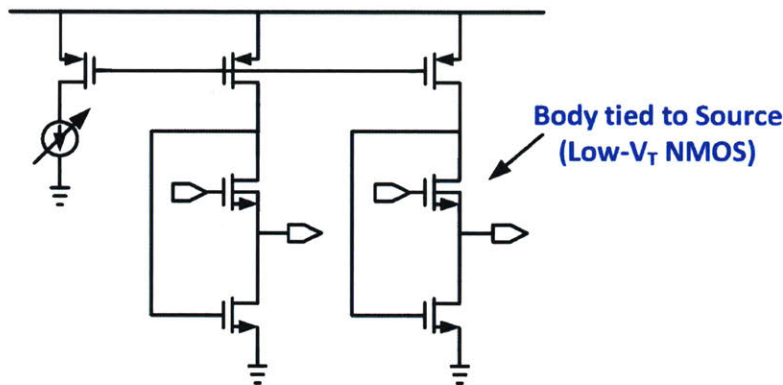


Figure 4-9: Schematic of unity-gain buffer

During the charge-transfer phase, the switched-capacitor amplifier connects the unit capacitors of C_1 to the same DC voltage. For the DC voltage, the first switched-capacitor amplifier uses the output common-mode of the unity-gain buffer while the second amplifier uses V_{CM} . It is because the first amplifier interfaces with the unity-gain buffer whose output common-mode is lower than V_{CM} . If the first amplifier connects its C_1 to V_{CM} for amplification, its summing node common-mode level can increase by hundreds of millivolts and the op-amp performance will be severely degraded. Connecting C_1 to the output common-mode of the buffer reduces this increase to tolerable amount, roughly 45mV. The buffer output common-mode level is obtained by shorting input ports of the buffer to V_{CM} .

4.5 Clock Generator

Figure 4-11 illustrates the clock generator of the prototype ADC. The low-voltage differential signal (LVDS) receiver converts its differential input to a single-ended clock. The non-overlapping clock generator takes this single-ended clock and outputs P1 and P2. P1 and P2 are delivered to the local clock buffer of each stage where various clock waveforms are generated for stage operations.

As discussed in section 2.3.2, the sampling clock jitter of the first stage affects the SNR of overall ADC. In order to minimize the sampling clock jitter, a separate signal path is dedicated to the first stage sampling clock PS. Rather than passing through

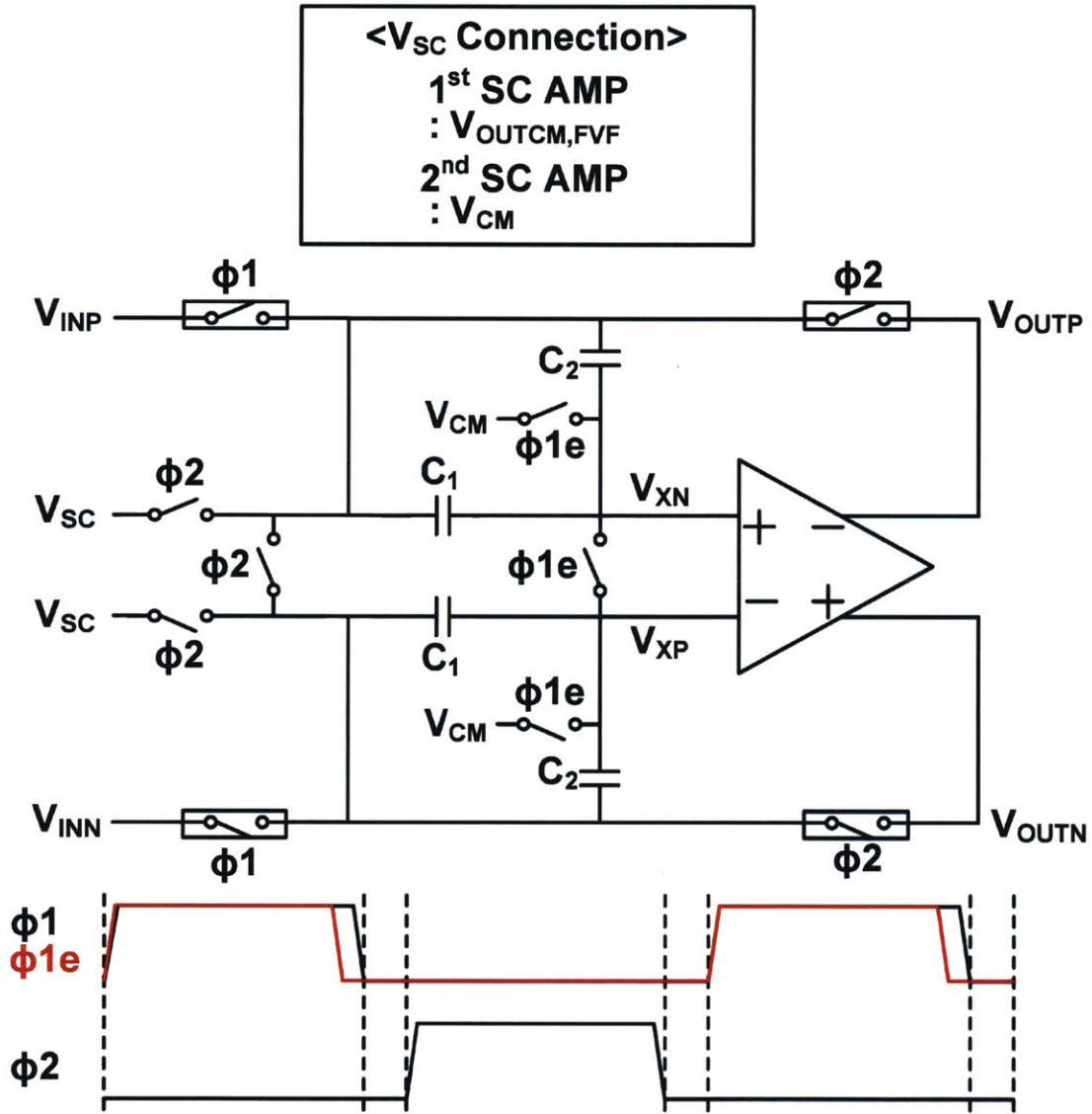


Figure 4-10: Schematic and clock waveforms of switched-capacitor amplifier

the local clock buffer of the first stage, PS is directly supplied to the gates of NMOS switches in the first stage MDAC and sub-ADC. The delay between P1 and PS is adjusted by a delay line.

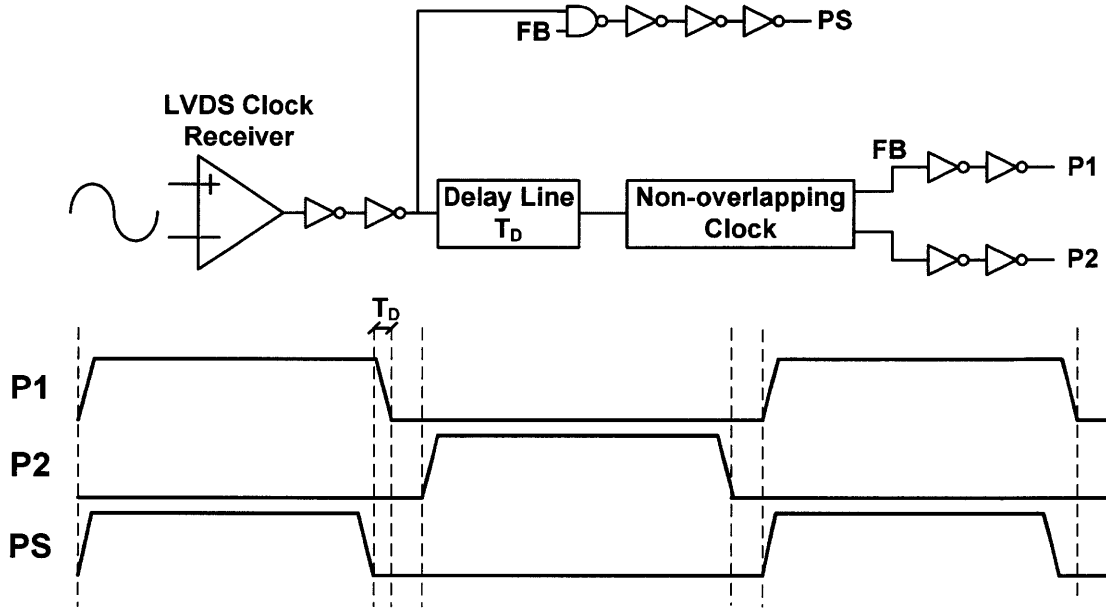


Figure 4-11: Schematic of clock generator

4.6 Layout

4.6.1 Overall Layout

The overall layout view of the prototype ADC is shown in Figure 4-12. The ADC is implemented on a $2.5\text{mm} \times 1.5\text{mm}$ die. In the given technology, total 10 metal layers are available with three levels of thickness. The thickest metal layers, metal 10 and metal 9, are allocated for power rails. The second thickest metal layers, metal 8 and metal 7, are used by the bias block to deliver bias currents and voltages for op-amps and unity-gain buffer. The thinnest metal layers (metal 1 - metal 6) route inter-stage and intra-stage signal paths.

Each block of ADC is carefully placed and routed. To minimize the inter-stage distance, all stages of the main ADC are placed in a straight line. The shadow

ADC places its stages in the same manner. Reference ladders are located in a way that minimizes their routing distances to the corresponding sub-ADCs. In addition to these block placement considerations, three sensitive signal paths are shielded. Routings for the main ADC input, clock generator input, and inter-ADC summing node signal path are protected from interferences by surrounding them with clean ground planes.

In the prototype ADC, the analog and digital power supplies are separated. Power supply separation not only makes the analog blocks be immune to the digital supply noise but also enables the power consumption measurement of each block. Grounds are shared by the entire ADC circuitry except for the LVDS output drivers since they carry a large amount of transient current. Along with the power supply separation, the power rails are drawn as wide as possible to minimize the IR drop. Also, sufficient decoupling capacitors are employed for all power supplies and reference voltages to keep them constant on the chip.

4.6.2 First Stage Layout

Figure 4-13 shows the layout of the first stage. Backend stages have almost identical layout to Figure 4-13 and hence they are not shown here. In order to match the routings between differential signals, all components of the first stage are drawn to have perfect symmetry. Also, each block is placed in a way that minimizes the summing node parasitic capacitance. For the same reason, the unity-gain buffer is laid out in the middle of the first stage rather than in front of the first switched-capacitor amplifier. Guard-rings are widely utilized in the stage to protect sensitive blocks from the substrate noise.

The prototype ADC only uses metal-oxide-metal (MOM) capacitors. Parasitic capacitance from the substrate is reduced by avoiding the lowest metal layer. The matching within the MDAC capacitor array is improved by surrounding the array with dummy capacitors.

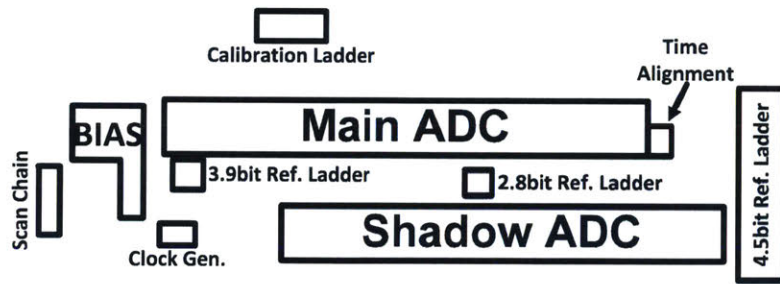
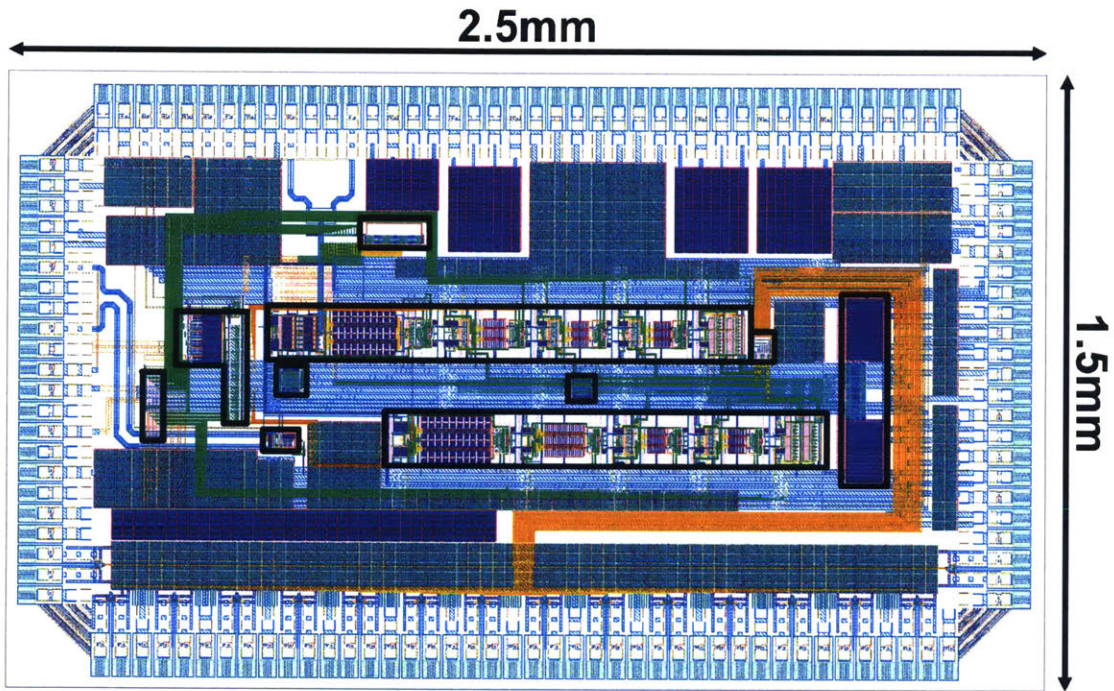


Figure 4-12: Overall Layout

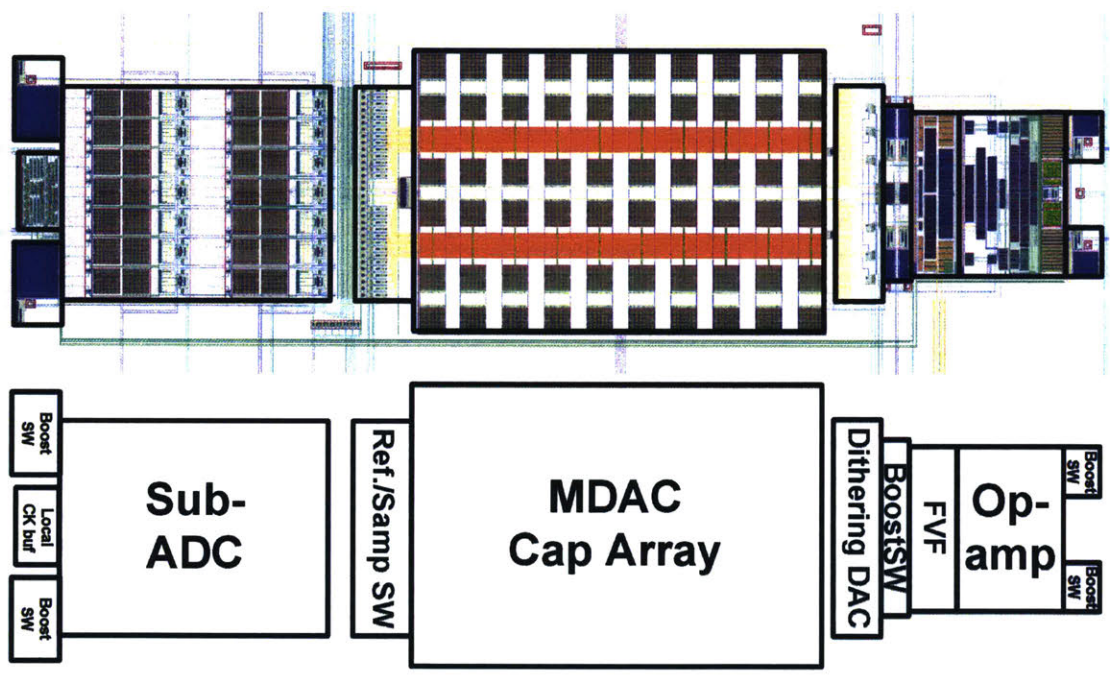


Figure 4-13: First stage layout

Chapter 5

Simulation Results

Chapter 5 presents the top-level post-layout simulation results of the prototype ADC. The chapter validates the functionality of the proposed shadow-ADC-assisted calibration scheme and analyzes the simulation results.

5.1 Feedback Factor Measurement

In order to measure the first stage feedback factor, two transient noise simulations have been performed. In each simulation, the ADC samples either +300mV or -300mV as its DC test voltage at the sampling rate of 220MS/s. The dithering injection is turned on to accelerate the averaging process. Since the bandwidth of the unity-gain buffer is much higher than the closed-loop bandwidth of the MDAC, the upper noise limit (f_{max}) is set as 30GHz to fully cover its noise power. Initial transients are discarded to exclude the effects of power-on transients.

From each simulation, 128 backend/shadow ADC samples are obtained and put into Equation 3.9 after averaging. As a result,

$$\frac{1}{A_{con}\beta} = 0.1830 \quad (5.1)$$

is acquired and used for later simulations. As discussed in section 3.3.2, this value is equal to the inverse of feedback factor times the signal conditioning path gain since

the summing node signal gets amplified before it arrives to the shadow ADC input. Intuitively, the effective resolution of the backend ADC and the shadow ADC can be increased by one-bit after increasing the number of averaged samples by 4 times. Therefore, it is expected that the measurement accuracy can be further improved in the real measurement.

5.2 Normal Operation

After the feedback factor measurement, the normal operation of the prototype ADC has been characterized by performing transient noise simulations with a pure sine wave input. A $1.2V_{pp}$ sine wave is input to the ADC that runs at 220MS/s. The input frequency for each simulation is chosen to meet the coherent sampling condition. The upper noise limit is set as 30GHz for the same reason in section 5.1.

Figure 5-1 and 5-2 show low-frequency input FFT plots of the ADC before and after applying the proposed calibration scheme, respectively. By comparing Figure 5-1 and 5-2, it is observed that the proposed calibration technique effectively corrects the op-amp-induced errors of the first stage. When the calibration is not used, the ADC achieves an effective number of bits (ENOB) of 8.73bit. The ENOB gets improved to 10.51bit when the calibration is applied. The ADC performance has also been measured by inputting the near-Nyquist frequency sine wave. Figure 5-3 shows the near-Nyquist frequency FFT plot after calibration. It can be seen that the ENOB slightly degrades from 10.51bit to 10.27bit, which is mostly due to the sampling clock jitter. In all cases, spurious free dynamic range (SFDR) is not measured because of the small window size of FFT plots.

At 220MS/s sampling rate, the simulation shows that the prototype ADC consumes total 32.72mW from 1.0V supply excluding 2.33mW LVDS clock receiver power. Corresponding Walden's figure of merit (FoM) is 101.9fJ/conv-step [35]. Figure 5-4 describes the power consumption breakdown of the ADC. The power consumption of sub-ADC reference ladders and $V_{REFP,N}/V_{CM}$ are calculated by multiplying 1.0V to the currents that they draw from external voltage regulators.

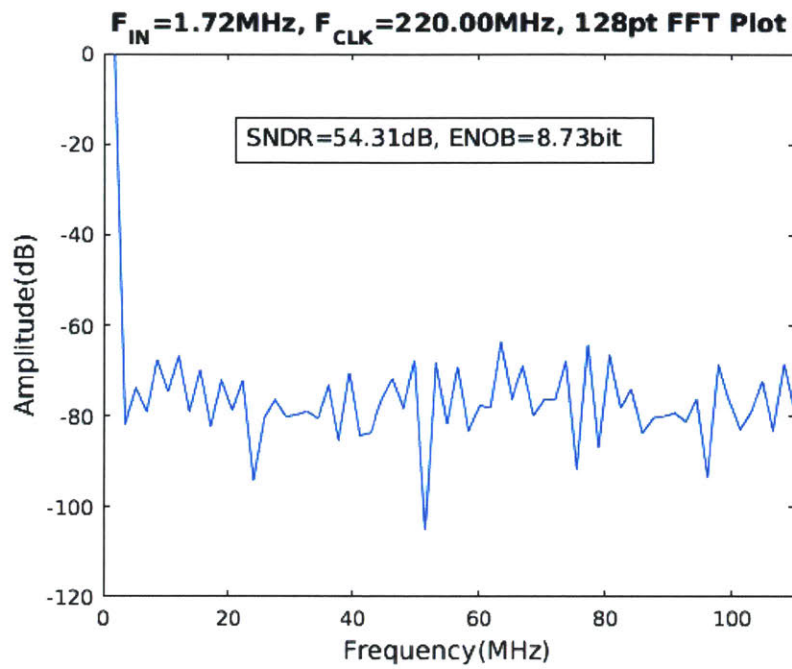


Figure 5-1: Simulated 128-pt FFT plot of ADC before calibration with low-frequency input (1.71875MHz)

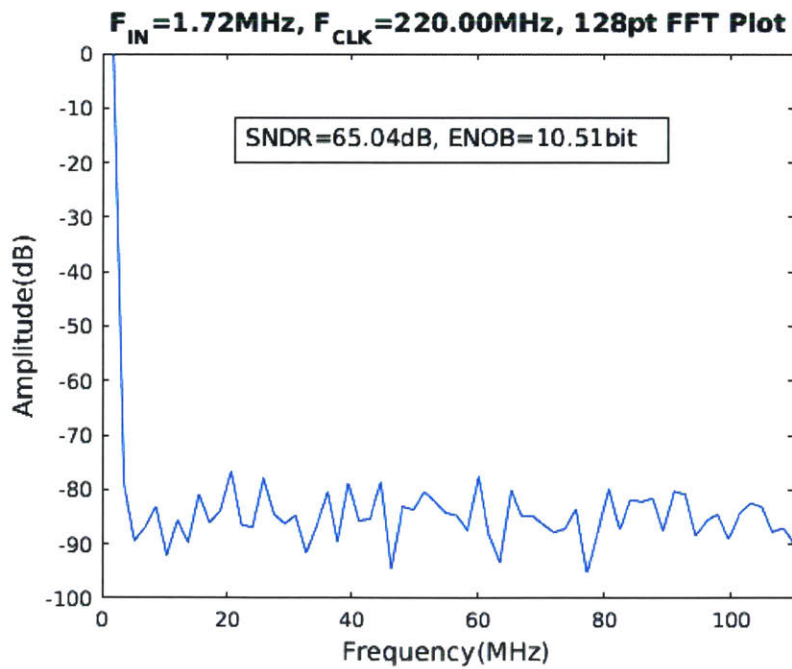


Figure 5-2: Simulated 128-pt FFT plot of ADC after calibration with low-frequency input (1.71875MHz)

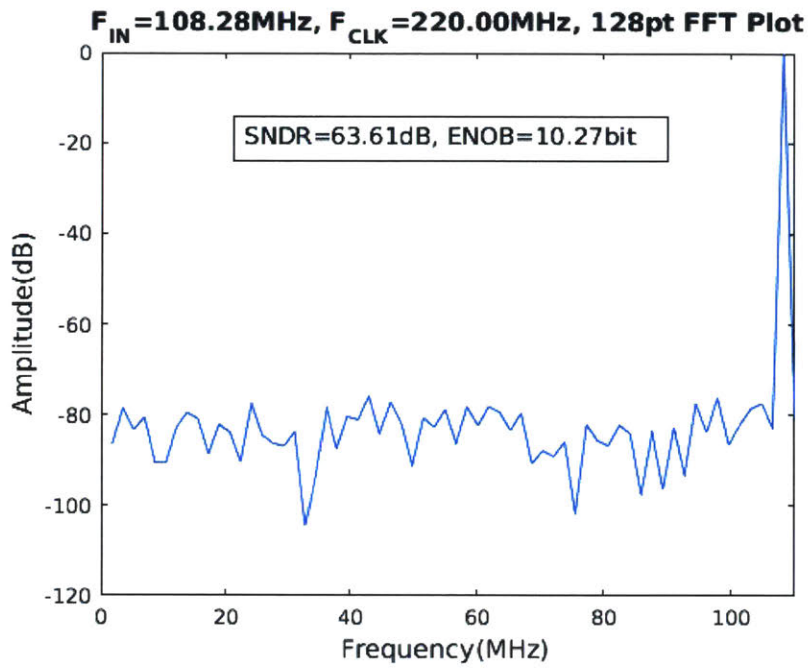


Figure 5-3: Simulated 128-pt FFT plot of ADC after calibration with Nyquist frequency input (108.28125MHz)

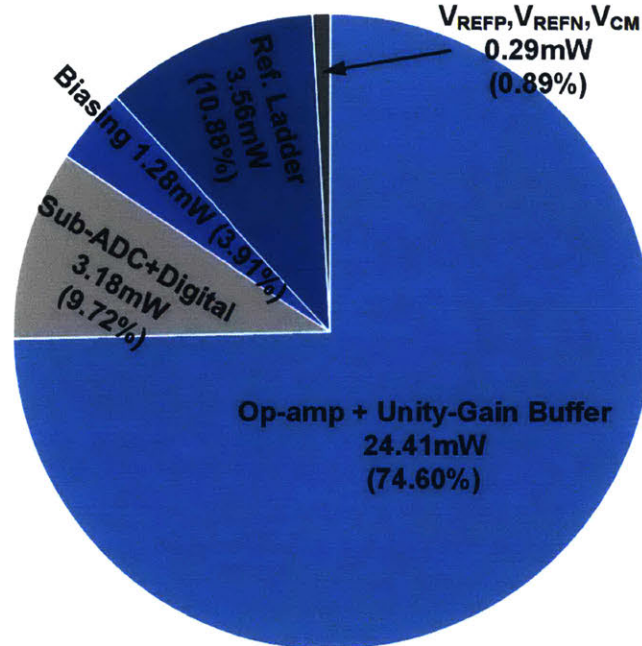


Figure 5-4: Simulated power consumption of each circuit block at 220MS/s

In the real measurement setup where ADC characterization is much faster than simulations, a number of things can be experimented to enhance the ADC performance. In the prototype ADC, the current flows of op-amps and unity-gain buffer are digitally adjustable. When more current flows through the op-amp, its bandwidth increases at the expense of decreased open-loop gain, and vice versa. Since the backend stages have enough op-amp-induced error margins at 220MS/s, further power optimization is available by decreasing their op-amp currents. Also, the ADC sampling rate can be improved by raising the current flows of frontend stages and unity-gain buffer. This is possible until the reduced settling error outweighs the increased open-loop gain error. Finally, as mentioned in section 5.1, a more precise feedback factor can be obtained to better the calibration performance.

Chapter 6

Conclusion

6.1 Thesis Contribution

As CMOS technology scaling continues, op-amp has become the most critical circuit block that determines the overall performance of pipelined ADCs. In order to relieve op-amp design constraints, previous works on pipelined ADCs have exploited digital calibration [4–13], analog circuit techniques [14–17], and circuit blocks that replace op-amps [18–27].

In this work, the shadow-ADC-assisted digital calibration technique is proposed to implement low-power, high-performance pipelined ADCs in a deep-submicron technology. The proposed calibration removes MDAC charge-transfer errors that are induced by insufficient op-amp open-loop gain and unity-gain bandwidth. Not only these non-linearity errors, but the op-amp noise and offset are also cancelled out. Therefore, the proposed technique can be adopted by all pipelined ADC architectures to relax major op-amp performance requirements, even the ADC is not designed in a scaled CMOS technology.

Compared to other digital calibration techniques, the output range of op-amp is not compromised [4–9] and there is no need to rely on pre-estimated feedback factor value [10, 11] or accurate voltage sources [12]. In addition to these advantages, the proposed technique features a simple digital algorithm that minimizes the overhead costs to implement calibration engine.

In order to demonstrate the calibration concept, a 12-bit, 220MS/s prototype ADC has been designed in 28nm FDSOI CMOS technology and is currently being fabricated. At the target sampling rate of 220MS/s, the simulated ENOB and power consumption of the prototype ADC are 10.51bit and 32.72mW, respectively. The simulation results show the effectiveness of the shadow-ADC-assisted calibration scheme.

6.2 Future Work

In order to achieve higher resolution and sampling rate, the proposed calibration scheme can be merged with the virtual ground reference buffer (VGRB) technique [14]. Since the VGRB technique greatly improves overall MDAC performance, a much better FoM is expected. When it is needed, the calibration scheme can be expanded to the second stage. This will further reduce the op-amp gain and bandwidth requirements. In addition to these topics, exploring an optimization of shadow ADC and its signal conditioning path is also promising. For example, a buffer-less signal conditioning path can be examined to eliminate the buffer noise contribution. In this case, trade-offs arising from the reduced feedback factor of the first stage and its effects on main ADC performance should be rigorously analyzed.

Bibliography

- [1] B. Murmann, "ADC Performance Survey 1997-2016." [Online]. Available: <http://web.stanford.edu/~murmann/adcsurvey.html>
- [2] A. M. Abo and P. R. Gray, "A 1.5V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
- [3] B. Murmann, "The Race for the Extra Decibel," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 3, pp. 58–66, Summer 2015.
- [4] E. Siragusa and I. Galton, "A Digitally Enhanced 1.8-V 15-bit 40-MSample/s CMOS Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.
- [5] A. Panigada and I. Galton, "Digital Background Correction of Harmonic Distortion in Pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 9, pp. 1885–1895, Sept. 2006.
- [6] ———, "A 130mW 100MS/s Pipelined ADC With 69dB SNDR Enabled by Digital Harmonic Distortion Correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.
- [7] N. Rakuljic and I. Galton, "Suppression of Quantization-Induced Convergence Error in Pipelined ADCs with Harmonic Distortion Correction," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 3, pp. 593–602, Mar. 2013.
- [8] A. M. A. Ali, H. Dinc, P. Bhoraskar, C. Dillon, S. Puckett, B. Gray, C. Speir, J. Lanford, J. Brunsilius, P. R. Derounian, B. jeffries, U. Mehta, M. McShea, and R. Stop, "A 14Bit 1GS/s RF Sampling Pipelined ADC With Background Calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, Dec. 2014.
- [9] A. M. A. Ali, H. Dinc, P. Bhoraskar, S. Puckett, A. Morgan, N. Zhu, Q. Yu, C. Dillon, B. Gray, J. Lanford, M. McShea, U. Mehta, S. Bardsley, P. Derounian, R. Bunch, R. Moore, and G. Taylor, "A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither," in *Proc. IEEE Symp. VLSI Circuits*, 2016, pp. 206–207.

- [10] A. M. A. Ali and K. Nagaraj, "Background Calibration of Operational Amplifier Gain Error in Pipelined A/D Converters," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 7, pp. 631–634, Sept. 2003.
- [11] A. M. A. Ali, A. A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, H. Dinc, M. Hensley, R. Stop, S. Bardsley, D. Iattimore, J. Bray, C. Speir, and R. Sneed, "A 16-bit 250-MS/s IF Sampling Pipelined ADC With Background Calibration," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2602–2612, Dec. 2010.
- [12] A. Verma and B. Razavi, "A 10-Bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.
- [13] B. D. Sahoo and B. Razavi, "A 12-Bit 200-MS/s CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2366–2380, Sept. 2009.
- [14] H. H. Boo, D. S. Boning, and H.-S. Lee, "A 12b 250MS/s Pipelined ADC With Virtual Ground Reference Buffers," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2912–2921, Dec. 2015.
- [15] B. R. Gregoire and U.-K. Moon, "An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30dB Loop Gain," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2620–2630, Dec. 2008.
- [16] B. Hershberg, S. Weaver, and U.-K. Moon, "Design of a Split-CLS Pipelined ADC With Full Signal Swing Using an Accurate But Fractional Signal Swing Opamp," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2623–2633, Dec. 2010.
- [17] Y. Miyahara, M. Sano, K. Koyama, T. Suzuki, K. Hamashita, and B. sup Song, "A 14b 60MS/s Pipelined ADC Adaptively Cancelling Opamp Gain and Nonlinearity," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 416–425, Feb. 2014.
- [18] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
- [19] E. Iroaga and B. Murmann, "A 12-bit 75-MS/s Pipelined ADC Using Incomplete Settling," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 748–756, Apr. 2007.
- [20] L. Brooks and H.-S. Lee, "A 12b, 50MS/s, Fully Differential Zero-Crossing-Based Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, Dec. 2009.
- [21] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 12b 5-to-50MS/s 0.5-to-1V Voltage Scalable Zero-Crossing Based Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1603–1614, July 2012.

- [22] D.-Y. Chang, C. Munoz, D. Daly, S.-K. Shin, K. Guay, T. Thurston, H.-S. Lee, K. Gualti, and M. Straayer, "A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13 μ m CMOS with 74dB SNDR," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 204–205.
- [23] M. Anthony, E. Kohler, J. Kurtze, L. Kushner, and G. Sollner, "A Process-Scalable Low-Power Charge-Domain 13-bit Pipeline ADC," in *Proc. IEEE Symp. VLSI Circuits*, 2008, pp. 222–223.
- [24] N. Dolve, M. Kramer, and B. Murmann, "A 12-bit, 200-MS/s, 11.5-mW Pipeline ADC using a Pulsed Bucket Brigade Front-End," in *Proc. IEEE Symp. VLSI Circuits*, 2013, pp. 98–99.
- [25] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring Amplifiers for Switched Capacitor Circuits," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012.
- [26] Y. Lim and M. P. Flynn, "A 100MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015.
- [27] —, "A 1mW 71.5dB SNDR 50MS/s 13bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.
- [28] S. H. Lewis, H. S. Fetterman, G. Gross, and T. R. Viswanathan, "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, Mar. 1992.
- [29] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York, NY: McGraw-Hill, 2001.
- [30] L. Brooks and H.-S. Lee, "Background Calibration of Pipelined ADCs Via Decision Boundary Gap Estimation," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 10, pp. 2969–2979, Nov. 2008.
- [31] J. Lloyd and H.-S. Lee, "A CMOS Op Amp with Fully-Differential Gain-Enhancement," *IEEE Trans. Circuits Syst. II*, vol. 41, no. 3, pp. 241–243, Mar. 1994.
- [32] J. Bach, "Capacitor array," Unites States Patent, 2011.
- [33] B. Razavi, "The StrongArm Latch," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, Spring 2015.
- [34] R. G. Carvajal, J. Ramnrez-Angulo, A. J. Lspez-Martn, A. Torralba, J. A. G. Galn, A. Carlosena, and F. M. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 7, pp. 1276–1291, July 2005.

- [35] R. H. Walden, "Analog-to-Digital Converter Survey and Analysis," *IEEE J. Select. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.