

Use of Competitive Benchmarking Information to Improve Equipment Utilization and Throughput in a Semiconductor Manufacturing System

by
Manish H. Bhatia

S.B. Mechanical Engineering, Massachusetts Institute of Technology 1993

Submitted to the Sloan School of Management and the
Department of Mechanical Engineering in partial fulfillment
of the requirements for the degrees of

**Master of Business Administration
and
Master of Science in Mechanical Engineering**

in conjunction with the
Leaders for Manufacturing Program

At the
Massachusetts Institute of Technology
June 1999

©1999 Massachusetts Institute of Technology, All rights reserved

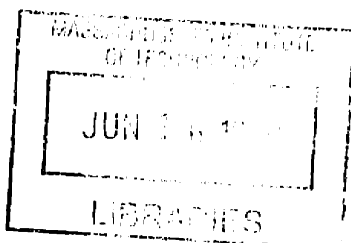
Signature of Author _____
Sloan School of Management
Department of Mechanical Engineering

Certified by _____
Jung-Hoon Chun, Thesis Advisor
Associate Professor of Mechanical Engineering

Certified by _____
Robert S. Gibbons, Thesis Advisor
Sloan Distinguished Professor of Management

Accepted by _____
Ain A. Sonin, Chairman of the Graduate Committee
Department of Mechanical Engineering

Accepted by _____
Lawrence S. Abeln, Director of the Masters Program
Sloan School of Management



ARCHIVES

Use of Competitive Benchmarking Information to Improve Equipment Utilization and Throughput in a Semiconductor Manufacturing System

by
Manish H. Bhatia

S.B. Mechanical Engineering, Massachusetts Institute of Technology 1993

Submitted to the Sloan School of Management and the
Department of Mechanical Engineering in partial fulfillment
of the requirements for the degrees of

**Master of Business Administration
and
Master of Science in Mechanical Engineering**

Abstract

The use of contract manufacturers is becoming more common in the semiconductor industry. These foundries, as they are known in the industry, focus their efforts on achieving operational excellence in order to manufacture semiconductor products more cost effectively than their customers can internally. Intel has started using Foundries for non-microprocessor products in order to help them reserve internal production capacity for their microprocessors. A side benefit of the outsourcing process for Intel, is the opportunity to benchmark their own operational efficiency against that of their supplier. This thesis will discuss the process used for this benchmark study, its results and managerial implications of the findings.

A benchmarking problem statement was defined including a rationale for focussing on the lithography area as the highest leverage point in the operation, and a description of the wafer throughput metric that was used for the comparison. The raw results of this study show a 33% deficit for Intel compared with Supplier X in lithography throughput. These data, however, included effects of both different machine types and different operational practices. Because Intel has strategic reasons for selecting its equipment vendors, the focus of this study was not to suggest that they switch lithography equipment vendors. Rather, the goal was to understand how much of this deficit could be attributed to Supplier X's superior operational practices.

In order to remove the convolving effects of different equipment run rates, a set of experiments was performed to separate machine effects from operational effects allowing for a direct comparison of operational efficiencies. These experiments showed that Intel has a 15% deficit in lithography throughput when compared with Supplier X, after normalizing for equipment effects. Reasons for this deficit could include Intel's excessive use of testing procedures, Intel's risk averse operational culture and Intel's possible managerial hubris.

Thesis Advisors:

Jung-Hoon Chun, Associate Professor of Mechanical Engineering
Robert S. Gibbons, Sloan Distinguished Professor of Management

Acknowledgements

I gratefully acknowledge the support of the Leaders for Manufacturing Program at MIT and Intel Corporation as sponsor of this project. I have appreciated the opportunity to learn and grow through my activities and coursework at the Sloan School, in the School of Engineering and at Intel.

I would like to thank my MIT thesis advisors Jung-Hoon Chun and Bob Gibbons for their sage advice and patience with me throughout this project. I regard them both very highly, for their help with this thesis and for what they have taught me through my interactions with them.

At Intel Corporation I received tremendous support from my supervisor Mike Rastery and from Dave Friedman, who is responsible for the genesis of this project. They spent many hours obliging my speculative curiosities as we shaped the scope and goals of this work. I would also like to thank Maribel Sierra from Fab 19 for her help in getting data from the Hudson operation and Mark Schaeffer from Fab 11 for lending high-level credibility to the project.

I would like to thank my fellow Intel LFM Interns (ILI's) Ajay Amar, Shafali Rastogi and Gary Tarpinian and my collegiate friends Aaron and Jessica Barzilai, who helped me keep my head above water (literally and figuratively) while I was out in Santa Clara.

Back at MIT, I would like to thank my classmates Vinay Bhargava, Michelle LeBlanc and Tom Wala, who helped make sure I stayed focused on my goal and didn't allow me to wait until the last minute to start work on my thesis. Their influence will be remembered fondly.

Finally, I would like to thank my parents Hasso and Champa Bhatia, and my sister Kapila, who encouraged me to return to school and pursue bigger and better things than I ever could have in Buffalo. Without their stabilizing influence and effective counsel, I might never have gotten to experience this exciting two year period in my life.

TABLE OF CONTENTS

1.0 INTRODUCTION.....	7
1.1 INTEL MANUFACTURING OPERATIONS	7
1.2 INTEL INTEGRATED CIRCUIT PROCUREMENT AND ENABLING DIVISION (IPED).....	8
1.3 THESIS OUTLINE	8
2.0 BASIC SEMICONDUCTOR MANUFACTURING.....	10
2.1 CHAPTER OVERVIEW	10
2.2 WAFER FABRICATION REVIEW.....	10
2.2.1 THIN FILM DEPOSITION	11
2.2.2 OPTICAL IMAGING	12
2.2.3 ETCH AND ION IMPLANTATION	13
2.2.4 PLANARIZATION	14
2.3 PROCESS FLOW- REENTRY.....	14
2.4 CHAPTER SUMMARY	15
3.0 BENCHMARKING PROBLEM STATEMENT AND RESULTS .	16
3.1 CHAPTER OVERVIEW.....	16
3.2 SELECTION OF COMPANY TO BENCHMARK.....	16
3.3 SELECTION OF SPECIFIC OPERATIONAL AREA TO BENCHMARK.....	17
3.3 METRIC'S FOR COMPARING THE PERFORMANCE OF THE TWO AREAS	20
3.4 BENCHMARK DATA RESULTS AND COMPARISONS.....	21
3.5 CHAPTER SUMMARY	23
4.0 ANALYSIS AND CLEANSING OF BENCHMARK DATA.....	24
4.1 CHAPTER OVERVIEW.....	24
4.2 KEY PROBLEM WITH DIRECT BENCHMARK COMPARISON.....	24
4.3 PERFORMANCE FEATURES FOR LITHOGRAPHY EQUIPMENT	25
4.4 CHAPTER SUMMARY	27
5.0 EXPERIMENTS TO SEPARATE EQUIPMENT EFFECTS FROM OPERATIONAL EFFECTS.....	28
5.1 CHAPTER OVERVIEW.....	28
5.2 MOTIVATION FOR EXPERIMENT.....	28
5.3 CAVEAT TO THE TEST	29
5.4 EXPERIMENTAL PARAMETERS	29
5.5 MODELING ASSUMPTIONS FOR THE DEFLATED THROUGHPUT CALCULATION	30
5.6 RESULTS.....	30
5.7 CHAPTER SUMMARY	32
6.0 REASONS FOR SUPPLIER X OPERATIONAL ADVANTAGE AND MANAGERIAL IMPLICATIONS	34
6.1 CHAPTER OVERVIEW.....	34
6.2 THE COST/QUALITY TRADEOFF	34
6.2.1 EXPLANATION OF THE POINT	34
6.2.2 SUPPORTING DATA OR INFORMATION	36
6.2.3 THE ALIGNMENT MARK STORY	36
6.3 INTEL'S RISK AVERSION.....	39
6.3.1 EXPLANATION OF THE POINT	39
6.3.2 SUPPORTING DATA AND INFORMATION.....	40

6.4 INTEL CENTRIC VIEW	41
6.4.1 EXPLANATION OF THE POINT	41
6.4.2 THE XEROX STORY AND THE POWER OF BENCHMARKING.....	41
6.4 IMPLICATIONS AND METHODS OF MEASURING THE EXTENT OF THESE ISSUES.....	43

TABLE OF FIGURES AND TABLES

FIGURE 2.1 DIAGRAM OF OPERATIONS AND REENTRANT FLOW.....	11
FIGURE 3.2 BERKELEY CSM BENCHMARK COMPARISON OF SEMICONDUCTOR PRODUCTIVITY.....	19
FIGURE 3.3 LITHOGRAPHY THROUGHPUT BENCHMARK SUMMARY.....	23
FIGURE 6.1 YIELD IMPROVEMENT OVER TIME-DIMINISHING RETURNS.....	38
FIGURE 6.2 THEORETICAL YIELD/COST TRADEOFF.....	38
TABLE 3.1 ANALYSIS OF DIFFERENCE BETWEEN SUPPLIER COST AND INTEL COST.....	17
TABLE 3.2 NORMALIZED INTEL WEIGHTED AVERAGE OUTS/TOOL/WEEK.....	22
TABLE 5.1 NORMALIZED RUN RATE RESULTS FROM EXPERIMENT AT DIGITAL FACILITY.	32

1.0 Introduction

Intel is the world's largest semiconductor manufacturing company with 1998 revenues of nearly \$25 billion and over 60,000 employees. While microprocessors are their largest and most recognizable product, Intel has other divisions that manufacture networking products, consumer appliances, flash memory, and computer motherboards.

1.1 Intel manufacturing operations

Intel's manufacturing operations are organized functionally into a single entity called the Technology and Manufacturing Group or TMG. This group supports the manufacturing needs of all of the different business divisions that are responsible for marketing Intel's products. Semiconductor manufacturing can be divided into three sets of facilities: wafer fabrication, assembly and test, and cartridge and motherboard assembly. Chapter 2 will describe the differences between these processes in more detail. Intel has 14 wafer fabrication facilities world wide, each producing different generations of Intel products. These wafer facilities produce three types of products, microprocessors, flash memory (not used in conjunction with other Intel products), and other logic chips (such as chip sets, clock chips and graphics chips used in Intel's cartridges and motherboards). Although the attributes of these products are very different, the manufacturing process for them is fairly similar, and Intel is able to use the same equipment to manufacture all three products.

Because of the enormous complexity involved with semiconductor manufacturing, Intel strives to reduce variation in process instructions and execution between facilities. They have set up their operations in order to leverage the learning curve from their pilot facilities directly into start-ups in their production facilities. In order to do this, Intel uses identical process instructions between their pilot facilities and production facilities. This manufacturing strategy is known as "Copy Exactly!", owing to the fact that the process sequences, process parameters, plant layout and equipment type are copied exactly from

one facility to another in order to minimize variation. These concepts will be explained in more detail in chapters 2 and 5, but it is important to understand the organization and focus of Intel's wafer fabrication operations in order to introduce the topic of this study.

As mentioned above, Intel uses similar processes and equipment for microprocessors, flash memory and logic chips. For strategic reasons, Intel is committed to manufacturing all of their own microprocessors. Flash memory is operated as a separate business, and will not be studied in this thesis. The logic chips are products that complement Intel's internal microprocessor cartridge and motherboard assembly operations. Although they are an important part of Intel's technology and product portfolio, they are not as critical as microprocessors. Accordingly, Intel can choose either to manufacture them internally or to source them externally if microprocessor demand takes up all of their manufacturing capacity. Intel will never choose to bump microprocessor loading to manufacture logic chips because the profit margins on microprocessors are significantly higher.

1.2 Intel Integrated Circuit Procurement and Enabling Division (IPED)

In order to support the cartridge and motherboard assembly operations, Intel purchases both logic and memory chips to complement the microprocessors. The IPED group is responsible for design and procurement of all externally sourced chips. All products sourced by IPED are used in internal operations- this is not a separate group, but rather a support group to Intel's final cartridge and motherboard assembly. IPED is not responsible for deciding which products are outsourced, but rather facilitates the procurement of products after the decision has been made not to manufacture them internally.

1.3 Thesis outline

This thesis describes a benchmarking study that was performed between Intel's internal semiconductor manufacturing operations and one of their IC supplier's operations. This project emerged from the relationship that IPED developed with this particular supplier

during the negotiation of a contract to supply logic chips. Chapter 2 of this thesis will give background on semiconductor manufacturing process and operational principles that Intel uses to run their facilities. Chapter 3 will summarize the benchmarking problem statement and explain the rationale behind the choice of company and areas for the study. Chapters 4 and 5 will explain a specific methodology to cleanse the initial benchmarking results in order to isolate specific causes of operational variation. Chapter 6 will explore managerial implications of the study's results.

2.0 Basic Semiconductor Manufacturing

2.1 Chapter Overview

There are three process steps associated with semiconductor manufacturing at Intel: wafer fabrication, assembly and test, and motherboard assembly. This thesis will focus exclusively on the wafer fabrication step in the overall semiconductor manufacturing process (not assembly and test or motherboard assembly).

This chapter will describe the terminology and processes associated with wafer fabrication at Intel. Section 2.2 will explain the basic product characteristics and nomenclature used with Intel's facilities. Subsections of 2.2 will briefly summarize the key processes in the wafer fabrication operation. Section 2.3 will describe the flow of wafers through the fab and the iterative and sequential nature of the flow.

2.2 Wafer fabrication review

Integrated Circuits (IC's) are produced on circular individual silicon discs called wafers. Each wafer holds hundreds of identical integrated circuits- at this stage these IC's are referred to as "die." Intel currently has production of both 150 mm and 200 mm diameter wafers, although the bulk of their operations are on the larger (200 mm) wafers. Die sizes vary for individual products, but are roughly 10 mm x 10 mm square. The size of the die and geometry used to lay the pattern out are key drivers of the cost of an IC.

Because of the extremely small feature size on modern IC's, wafers are manufactured in ultra-clean environments called clean rooms. Typical critical dimensions of circuit features are between .25 μm and .50 μm , and therefore have tremendous potential for contamination from dust and other airborne particles. These clean room facilities are referred to in the industry as "Fabs".

Wafer fabrication involves hundreds of processing steps which are designed to build up anywhere from one to two dozen material layers on top of the base silicon wafer. Each die is designed to carry millions of mini electrical devices (transistors, diodes, resistors) which are all connected together to form a functioning integrated circuit. Each individual processing step has different process specifications that determine machine parameters, processing times, and material used for the operation. The collection of these specifications is referred to as the product recipe.

Wafer fabrication is an iterative process, with the buildup of each layer following a similar sequence of machine steps. The basic steps of this process cycle are thin film deposition, optical imaging (involving coating, lithography exposure and develop), etch or ion implantation and planarization.

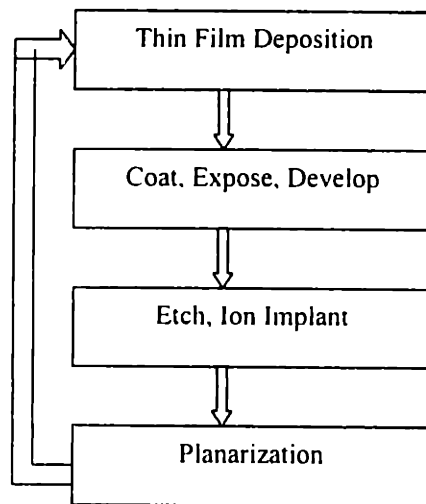


Figure 2.1 Diagram of operations and reentrant flow.

2.2.1 Thin Film Deposition

Thin film deposition includes the addition of oxide (and other dielectrics such as aluminum nitride) or metal layers to the wafer in order to build up specific layers. Primary processes used for depositing oxide include oxygen diffusion (in oxygen controlled furnaces) and chemical vapor deposition (for extremely small and precise

oxide requirements). Most metal layers are deposited with physical vapor deposition processes, the most common of which is sputtering. Metals that are typically deposited onto wafers include aluminum, aluminum alloys, copper, gold, titanium and tungsten.

2.2.2 Optical imaging

Optical imaging involves the definition and transfer of a specific pattern to the die that creates features of the individual material layers. Optical imaging is divided into coat, lithography exposure, and develop steps.

During the coat step, the wafer is primed and uniformly covered with a specified thickness of photoresist. Photoresist is a chemical that is sensitive to ultra-violet light and changes physical state when exposed to specific wavelengths. This physical property allows certain areas of the die to be kept differentiated from others, and thus allows for circuit feature creation.

Photolithography exposure involves the focusing and alignment of the ultra-violet source to the template or mask/reticle that defines the pattern, and the wafer itself. The image will be permanently transferred to the part of the wafer surface not covered by the photoresist using the subsequent etch or ion implantation processes. The key parameter in evaluating lithography technology is the resolution. A tool's resolution is its ability to consistently create pattern features of a minimum specified size. It is typically measured in terms of the minimum 'linewidth' or width of a device feature (such as a single wire on a resistor) that can be produced repeatably. Current technology can produce linewidths in the submicron range. A typical IC has different levels of linewidth requirement for each of the process layers. The linewidth specified for a given product refers to the minimum linewidth required by the smallest device features on that product. Typically only a few of the layers of each product will require this minimum linewidth process, allowing different generations of equipment to be reused on less demanding layers.

Lithography is the key technology in semiconductor manufacturing, because it is used repeatedly in a process sequence that depends on the device design. It determines the device dimensions, which affect not only the device's quality but also its product amount and manufacturing cost.¹ Lithography is the specific area studied in detail in this thesis.

The develop step removes the exposed photoresist through the use of a dissolver solution after the pattern has been transferred by exposure.

2.2.3 Etch and Ion implantation

While optical imaging creates the pattern of the circuit device features, the etch and ion implantation processes permanently transfers that pattern to the unmasked regions of the wafer.

Etching is a material removal process. The operation is performed in order to remove unwanted material from the section of the die that was not protected with the photoresist applied in the previous step. Etch techniques consist of dry and wet etch methods. Dry methods include plasma etching, reactive ion etching and ion beam etching. Wet etching involves using targeted chemicals to remove specific materials which dry etching techniques are unable to provide adequate etch selectivity. Wet etching is used to remove polysilicon, silicon nitride and silicon dioxide layers.

Ion implantation is used to introduce atoms of specific materials directly onto the wafer in order to effect the material properties of the base silicon. This process, referred to as doping, involves injecting ions of boron or phosphorous into the wafer in order to change the electrical conductivity of the silicon. Like etching, this process permanently transforms the wafer, developing features in the areas that are left uncovered by the exposure process.

¹ ULSI Technology , pg 270

2.2.4 Planarization

The planar process or chemical mechanical planarization (CMP) is one of the latest and most important developments in wafer fabrication. Planarization is a polishing process that levels the wafer surface between material layers in order to improve the resolution of the subsequent lithography exposure step. Leveling or flattening of the wafer surface allows each layer to begin with an even topography and improves the resolution of the optical imaging process.

2.3 Process flow- Reentry

In general the different layers in wafer fabrication share the similar equipment between the different passes through the fab. Very few of the layers have equipment that is dedicated, typically only for critical geometries, which require the most advanced equipment. Because the bulk of this equipment is shared between layers of different wafers and products and the similar sequences each layer's build-up follows, the wafer manufacturing process is referred to as reentrant flow. Each wafer completes a layer pass through the sequences specified above, and then reenters the process at the top of the cycle again.

It is important to understand the reentry process because it becomes a driver in both design and selection of manufacturing equipment and in capacity planning and production scheduling. Again Figure 2.1 shows this reentry process schematically.

Wafers travel through the fab in batches of 25 called "lots." In order to minimize set up times between different products or layers, Intel will try to run lots with identical process instructions (i.e. similar layers and products) sequentially, or back to back. This practice is called cascading. This concept will be described further in Chapter 5 during the description of specific experiments associated with this benchmarking project.

2.4 Chapter Summary

Chapter 2 has given an overview of the basic terminology and product characteristics of wafer fabrication. A brief summary of the key processes in the manufacturing operation was also provided. Finally, a description of the scheduling issues involved in the operation, and Intel's approach to managing these issues was given.

3.0 Benchmarking Problem Statement and Results

3.1 Chapter Overview

This section will attempt to outline the key challenges in formulating the benchmarking study. The areas to be covered include the selection of the company to benchmark, the specific operational areas on which to gather data and study, the metrics which will be used to make comparisons between operations, and the selection of internal areas to use for the study.

3.2 Selection of company to benchmark

Intel IPED selected Supplier X as a supplier of peripheral components that would support a generation of their high performance and basic PC microprocessor products. Supplier X won the contract based on competitive price, ability to meet quality and product feature requirements, ability to meet lead time requirements, and flexibility to expand production to accommodate increases in demand. Supplier X is recognized as a leading Integrated Circuit contract manufacturer.

During the vendor selection process, Intel IPED performed a 'should-cost' analysis on Supplier X's operation. This analysis is meant to help Intel understand the processes their vendor will use to manufacture the product, and to understand the vendor's theoretical cost position. The should-cost results support both the vendor selection process and the subsequent negotiation with suppliers. The results of this cost analysis revealed that Intel's internal, fully loaded cost to manufacture a certain chipset product was more than 60% higher than IPED's estimate of Supplier X's fully loaded cost.² Even after correcting for labor cost differences, Intel's internal costs were still 60% higher than the should-cost. This variation helped launch the idea of a benchmarking study to understand the drivers of this cost difference.

3.3 Selection of specific operational area to benchmark

The largest component of both Intel and Supplier X's semiconductor manufacturing costs is capital equipment depreciation. This is true of the entire semiconductor industry, as the equipment is both expensive and becomes obsolete quickly, reducing the depreciation period, and hence increasing the depreciation charges. Figure 3.1 shows a comparison of Intel and Supplier X's cost differences by major area. From Table 3.1, it is clear that capital equipment depreciation also represents the largest portion of the estimated difference between Intel and Supplier X.

Table 3.1 Analysis of Difference between Supplier Cost and Intel Cost

Cost Component	Percent of Total Cost Difference Attributed to Cost Component
Equipment Depreciation	25%
Labor	23%
Floor space	13%
Silicon	19%
Spare parts	10%
Other	10%
Total	100%

Because of the precision optics, mechanics and reticles required in lithography, it is the most expensive process (on a cost per pass basis) among the capital equipment processes. For this reason, Intel designs their fab facilities with lithography tools as their bottleneck- the idea being that the most expensive equipment should have the highest equipment utilization. All other areas should have excess capacity, to ensure the bottleneck is always running. Because lithography is the bottleneck, any additional production through this area will result in additional capacity for the entire facility, because all other areas are designed to have more capacity than the bottleneck. This made the lithography area an attractive target for the benchmark study. Also, Intel's internal manufacturing strategy

group, and other industry benchmarking studies have noted Country X's (home country of Supplier X) semiconductor manufacturers as the world leader in lithography efficiency, throughput and cost. Figure 3.2 shows a study from the Competitive Semiconductor Manufacturing group at University of California at Berkeley that shows the Country X as best in class in equipment efficiency among foreign semiconductor manufacturers. .

For these two reasons, the lithography area was selected for study in the benchmarking project.

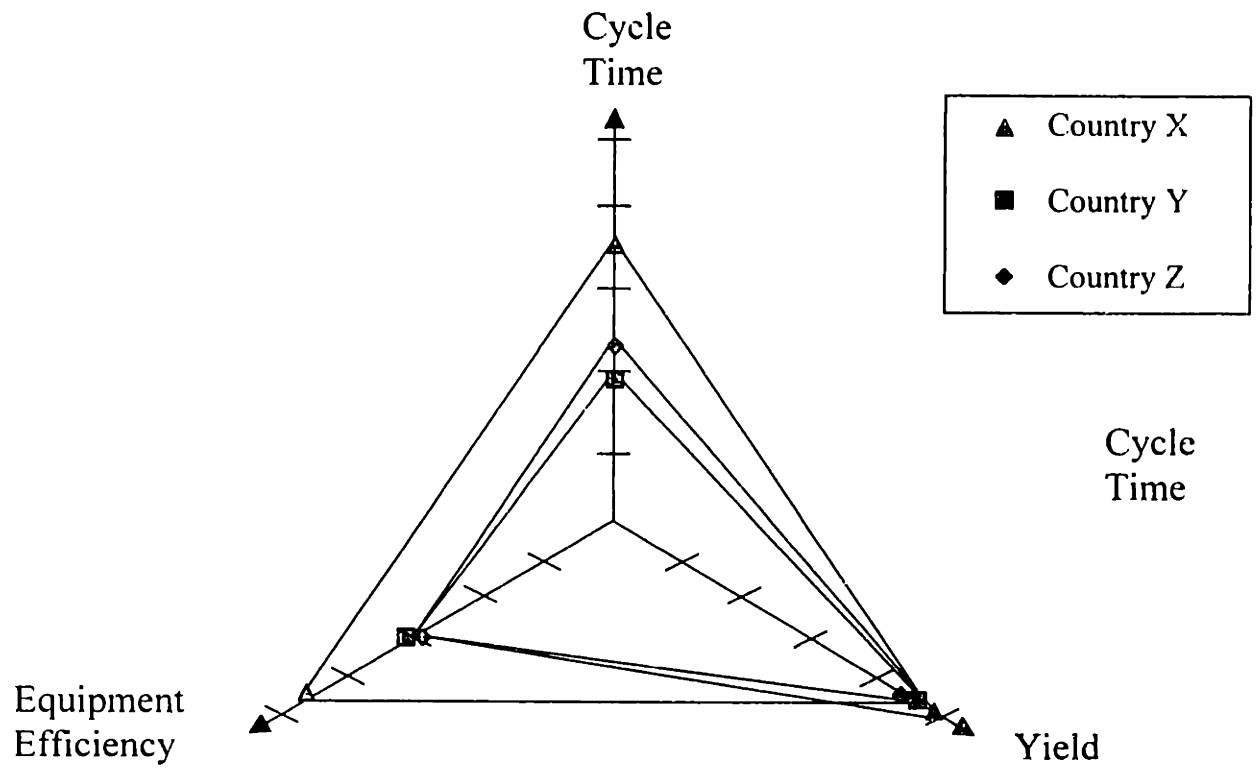


Figure 3.2 Berkeley CSM Benchmark Comparison of Semiconductor Productivity.

3.3 Metrics for comparing the performance of the two areas

Two different metrics were considered to compare the Intel and Supplier X operations, equipment utilization and wafer production or throughput.

Equipment utilization (U) was defined as:

$$U (\%) = \frac{\sum (\text{Production}_i + \text{Test}_i + \text{RW}_i \text{ outs} * \text{Layer RR}_i)}{168} \quad (1)$$

where Production = a layer of a saleable product wafer in individual units

Test = a layer of a product development or equipment wafer in individual units

RW = a layer of a reworked product wafers in individual units

Layer RR = specified run rate for each layer of the process in hours/unit

168 = total available hours/week

Throughput (T) was defined as wafer output / tool/ week or

$$T (\text{units/week}) = \underline{\sum} \text{Production} + \text{RW} \quad (2)$$

where Production = a layer of a saleable product wafer in individual units/week

RW = a layer of a reworked product wafers in individual units/ week

The utilization metric is a more sophisticated tool, giving a measurement of the effectiveness of a piece of equipment compared against the standard specified run rate provided by central process engineering. It also has a considerable amount of subjectivity in the definition. Among Intel engineers interviewed, there was no clear consensus on which types of test and non-product wafers should be counted toward

utilization. Also, it would be extremely difficult to obtain the layer run rates for each of Supplier X's processes.

The throughput metric is a simple tool, which is easily interpreted by everyone internally at Intel. Although it gives little guidance into the specific areas that may cause a difference between the operations, it was a figure that could be obtained fairly accurately and unambiguously from both Intel and Supplier X operations. Because this was a 'cleaner' measure, throughput was chosen as the metric on which to compare the two lithography operations.

3.4 Benchmark data results and comparisons

Through discussions with Supplier X engineering and operations personnel, wafer throughput data in Lithography for their .25 μm , .35 μm and .50 μm operations were obtained. Supplier X's stated average throughput for these processes was **1000 wafers out / tool / week**. Although these conversations were informal, this number was supported by two different sources internally at Supplier X. Also, this number was given as a minimum target for weekly throughput. Using this number as the benchmark can be taken as a conservative estimate of Supplier X's Lithography throughput capability.

Data for internal comparison came from Intel's 1998 Model of Record for their U.S. region Virtual Factory. The Model of Record is essentially Intel's annual operational plan that supports capital equipment and operational expense budgeting. Two issues which arose in attempting to compare Lithography throughput were the tools selected for comparison, and the weighting to be given to each tool in order to compute an average throughput to compare against Supplier X's benchmark. The Lithography tools selected were ones used for similar .25 μm , .35 μm and .50 μm linewidths. The throughput values for each tool were weighted by the number of layers that were assigned to that tool in the process recipe, to compute an overall normalized average throughput value of **752 wafers out / tool / week**. Table 3.2 shows the breakdown and calculation of the individual pieces of equipment.

Table 3.2 Normalized* Intel Weighted Average Wafer Outs/Tool/Week

	# of	FCST	Weighted
	Layers	O/T/W	Average
			O/T/W
.25 μ m linewidth tool	3.0	715	2,145
.35 μ m linewidth tool	2.0	477	954
.50 μ m linewidth tool	13	803	10,439
			752

*These data are not true values but represent values normalized to Supplier X.

Figure 3.3 shows a summary comparison of the benchmark data for Lithography throughput. The difference between the stated Supplier X throughput value and the weighted average normalized Intel value is **248 Outs / Tool / Week**. This number represents a 33% higher throughput in Lithography for Supplier X over Intel.

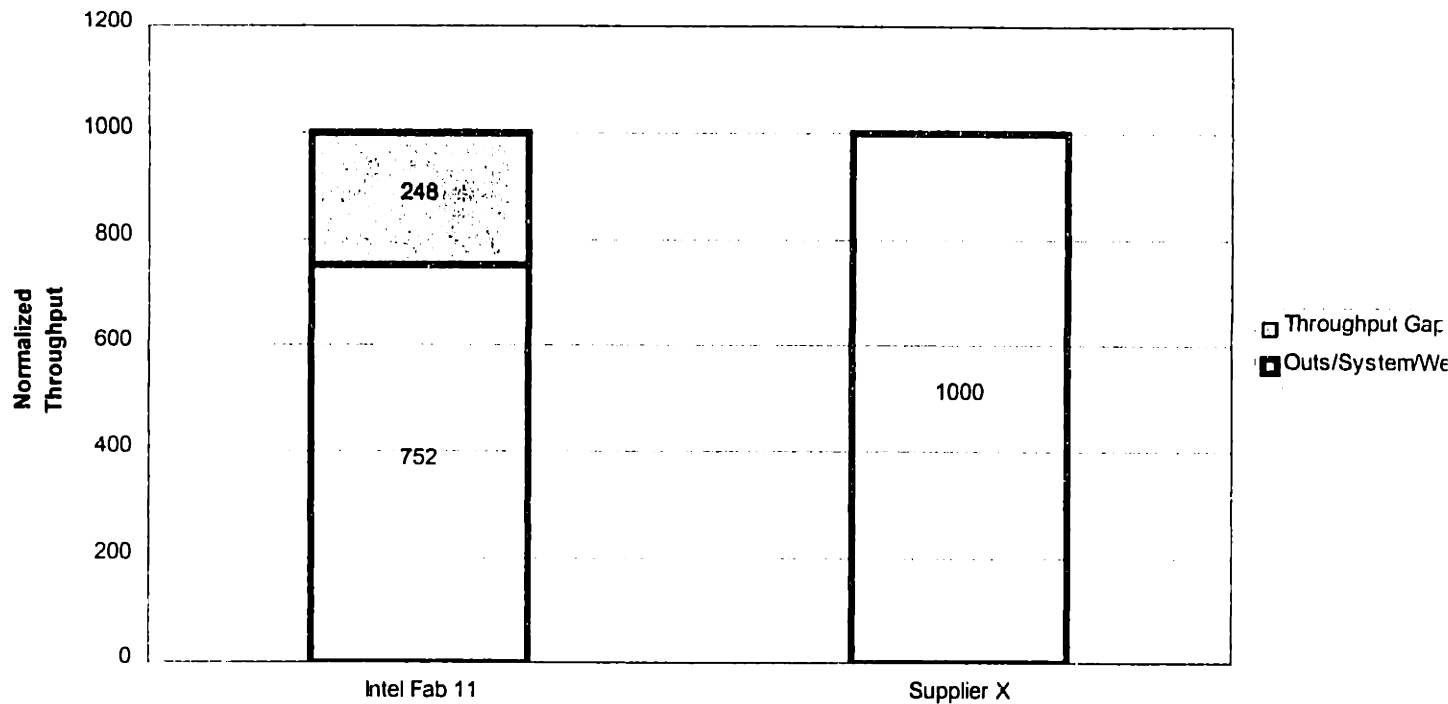


Figure 3.3 Lithography Throughput Benchmark Summary.

3.5 Chapter Summary

This chapter outlined the benchmarking problem statement that is the central focus of this project. A description of the supplier relationship that was the genesis of this benchmarking initiative was provided. An explanation was given for the selection of the Lithography department as the specific area to be compared between the two companies. A justification was given for the selection of Wafer throughput as the metric on which to compare the two departments. And finally, the results of the benchmarking study were provided, showing Intel to have a deficit of approximately 33% in Wafer Throughput compared with Supplier X.

4.0 Analysis and Cleansing of Benchmark Data

4.1 Chapter Overview

This chapter will describe the problem with directly comparing Intel and Supplier X's lithography operations. The specific reasons for this issue will be given, as well as an explanation of the key components of lithography equipment, and the differences between suppliers.

4.2 Key problem with direct benchmark comparison

The most significant problem with making a direct comparison between the Supplier X and Intel Lithography operations is the different equipment that is used in the two facilities.

Intel produces mainly microprocessors that require leading edge lithography equipment. Intel chooses to purchase equipment that is designed and optimized for obtaining the smallest linewidth possible with current technology.

In contrast Supplier X manufactures many products that do not demand the latest lithography technology. At any given point in time, Intel is typically 12 months ahead of Supplier X in terms of linewidth requirements for their products. Because they are technology followers in this area, Supplier X chooses to purchase lithography equipment that is optimized for reducing cycle times and down time in order to increase overall throughput. The difference between the raw machine throughput capability between the two equipment types is certainly a contributor to the overall throughput gap. However, there is also an operational component made up of items such as preventative maintenance, in process wafer testing, wafer production sequencing and scheduling and equipment dedication that contribute to the gap as well.

Intel has strategic reasons for their choice of equipment vendors, and the point of this thesis is not to examine that decision. Rather, the key problem addressed in this chapter and Chapter 5 is how to separate these two components of the throughput gap (machine-specific and operation-specific) in order to identify 'operational advantage' that Supplier X has through superior operational practices. This will allow Intel to understand the scope and priority for operational improvement activities that the benchmarked throughput gap represents (i.e. how much productivity improvement can Intel get by changing operating procedures rather than switching equipment).

4.3 Performance Features for Lithography Equipment

It is important to have an understanding of the aspects of lithography tools on which different vendors compete. This should help to explain the reasons certain tools will inherently provide higher throughput capability. It will also assist the reader to separate the equipment related effects from the purely operational effects on overall throughput. There are three key components to a lithography tool: staging, alignment and imaging.

Staging is the set of all wafer handling mechanisms on the tool. These are extremely precise, mechanical interactions that drive the raw run rate of each exposure, as well as much of the preventative maintenance and downtime associated with the tool. This area in particular represents a key difference between equipment vendors. Intel has typically chosen vendors that focus on imaging as their key performance area. Supplier X on the other hand has chosen vendors that optimize the staging, and are followers on the alignment technology. By focusing on staging, Supplier X's equipment vendors have built a competence in electro-mechanical devices and wafer handling. They also focus on building robust systems that have fewer failures and are easier to maintain. This enables them to provide higher throughput tools in terms of both higher raw run rates, and higher uptimes.

Alignment is the process by which the wafer and mask are aligned to each other and to the tool in order to ensure the pattern is printed in the proper location. The alignment process is a key driver of the tool cycle time (and thereby throughput). Alignment typically involves a closed circuit camera that matches up marks on the mask with marks on the wafer that are patterned on the first material layer. The number of marks and the speed of the mechanism determine the time required for each wafers alignment.

Alignment is a key factor driving the repeatability (or variability) of the lithography process. Also, because the largest portion of lithography set-up time involves mask changeovers, Supplier X's vendors have focused on reducing the time required to change masks, and have streamlined the process so that masks can be changed without stopping the tool (in effect using a turret to stage masks). This results in faster changeovers, and less overall setup time that leads to higher throughput.

Imaging involves the mechanisms that determine the resolution of the focused light source and mask onto the wafer. This ultimately determines the minimum linewidth and feature size that the tool is capable of producing. The complexity of the imaging system is the reason reducing the resolution (and linewidth) is so difficult. It is this complexity that makes a .25 μm tool more expensive and more precise than .50 μm equipment.

Components that determine a tool's imaging capability include the light source, the lens magnification, and the numerical aperture. The imaging mechanism is the most technically complex component, and therefore is a key driver of preventative maintenance and downtime on the tool.

Vendors that focus on optimizing tool throughput will have products that have higher raw run rates. The equipment is more robust to maintenance failures- thereby reducing required preventative maintenance and unanticipated downtime. All of these factors lead to higher throughput capability inherent to the tool. The key challenge in cleansing this data and making it applicable to Intel is understanding how to separate the tool specific throughput advantage (which Intel can presumably not get without switching vendors) from the throughput advantage that Supplier X gets from operational procedures.

Chapter 5 details a set of experiments performed on Intel products, using Supplier X type

equipment, in order to try to separate these two areas and better understand how much Intel could gain from improving their operational procedures.

4.4 Chapter Summary

This chapter explained the analysis of the data gathered in the Lithography benchmarking study. The key issue clouding the analysis is the difference in type of equipment used between the two facilities. An explanation was given for the different requirements and vendors selected by each of the companies. A description of the three main components in lithography equipment was provided, along with an assessment of the key operational metrics which each of these components affects. Finally, a brief introduction and motivation for the experiment detailed in Chapter 5 was given.

5.0 Experiments to separate equipment effects from operational effects

5.1 Chapter Overview

This chapter will explain a set of experiments that were conducted in order to better understand the effect of different lithography equipment on overall lithography throughput. The rationale and goals of the experiment will be given. The experimental parameters, as well as the model used to analyze the raw data will be explained. Finally, conclusions will be drawn about the effect of equipment specific run rate on overall tool throughput.

5.2 Motivation for Experiment

Chapters 3 and 4 outlined the findings from the lithography benchmark study and the key issues with resolving the data into a useful form. An experiment was proposed to separate the combined effects of equipment and operational procedures on overall wafer throughput. In June of 1998, Intel acquired a fab from Digital Equipment Corporation. This facility had equipment from the same lithography equipment vendor as Supplier X. Since it had only been used for Digital products, a direct comparison of throughput was not possible. This did, however, afford the opportunity to run tests with recipes for Intel products, on the Digital lithography equipment and evaluate the raw run rates. By using Intel product recipes we were able to simulate the potential run rate of the Supplier X type lithography equipment, in an Intel facility. By adding in Intel normal scheduling parameters of projected loading, number of cascaded batches, number of pilot (set-up test) wafers, projected set up time, and machine downtime, we were able to model the *deflated* throughput of the tool. (i.e. the throughput is less than the raw run rate because the tool is not operating 100% of the time). This deflated throughput number could then be compared against the Supplier X throughput number in order to calculate the theoretical throughput Intel could achieve, were they to use the higher throughput equipment. The expectation of the experiment was that this theoretical Intel/Digital throughput number would still be lower than Supplier X's, and that the difference

between these two numbers would be the throughput gap due to superior operational procedures.

5.3 Caveat to the Test

Because of the expense of buying masks for the Intel products compatible with the Digital lithography equipment (several hundred thousand dollars), the experiments performed did not manufacture actual die. Instead, only the lithography steps were done. But the parameters for the Intel products for each individual lithography step, including number of exposed cells, resist type, thickness, lamp exposure time and coat/develop procedures were matched exactly from Intel recipes.

Since no actual die were manufactured, there was no way of evaluating this equipment's ability to meet the technical requirements of Intel products. But because the goal was to understand the run rate variability and throughput impact of the tool, this was an acceptable tradeoff for the experiment.

5.4 Experimental parameters

The experiment tested five Intel products, all with minimum linewidth requirement of $.25\mu\text{m}$. Eight wafers of each product were run per batch. The goal of this experiment was to get the raw run rate (or cycle time) for each product, without consideration of the production scheduling, testing, preventative maintenance, or unplanned downtime. All of these operational issues were considered in the deflation model that uses the raw run rate as the key input. In order to get raw run rate times no set-up wafers were run for these experiments. Instead, the machine gave a cycle time between the loading of each of the eight wafers.

Key parameters of the experiment were:

- The identical exposure time, # of exposures/wafer, resist thickness and coat/develop procedures as the Intel product recipe were used.
- All of the products were 18-layer processes, and therefore involved 18 lithography steps. This is the same number of steps that would have been required on Intel

equipment. Because alignment plays a key role in determining raw run rate capability, the alignment procedures of the Digital equipment (rather than Intel equipment) were used.

- Based on the linewidth requirements of each layer, one of three different lithography tools was chosen. The different equipment models (.25 μm , .35 μm and .50 μm) were chosen to match the three levels used in the Intel's virtual factory for these products. The run rate calculations were then compared separately against the counterpart tools in order to give a more consistent comparison (rather than comparing a .25 μm tool against a .50 μm tool that might confuse the analysis).

5.5 Modeling assumptions for the Deflated Throughput Calculation

Intel's production scheduling model was used to take the raw run rates measured in the experiment, and convert them into deflated throughput numbers that would reflect the theoretical use of these tools in Intel fabs (on Intel products). The model is built in a Microsoft Excel spreadsheet with macros to allow easy simulation of multiple plant loading scenarios and changes in plant capacities and inventory levels. The basic assumptions for this model were:

- 25 wafers were used in any lot (i.e. no test wafers in each lot)
- 4 lots of .25 μm , 3 lots of .35 μm and 2 lots of .50 μm were cascaded back to back at each of those tools.
- Cascade efficiency (or amount of time where similar setups were run back to back) was assumed to be 70% for all linewidth tools.
- The loading and tool utilization were taken from Intel's plan for these .25 μm linewidth products.

5.6 Results

Table 5.1 shows a comparison of the deflated run rates for each of the Digital tools against their Intel counterparts. At first glance, the Digital tools appear to have about 19% higher throughput on tool 1 (.5 μm linewidth steps), 15% higher on tool 2 (.35 μm) and

23% higher throughput on tool 3 (.25 μm). To say that in aggregate, the Digital tools provide approximately 18% higher throughput would be a reasonably accurate statement, given that 13 of the 18 layers are run on tool 1 (19%), and therefore could be weighted most heavily. Although a weighted average gives only a rough analysis, it does give some insight into the throughput improvement provided by the Digital (Supplier X-type) equipment.

Table 5.1 Normalized* Run Rate results from Experiment at Digital facility.

	Intel Tool 1 .50μm (wph)	Digital Tool 1 .50μm (wph)	% diff.	Intel Tool 2 .35μm (wph)	Digital Tool 2 .35μm (wph)	% diff.	Intel Tool 3 .25μm (wph)	Digital Tool 3 .25μm (wph)	% diff.
Product 1	700	830	15.7%	761	916	16.9%	924	1152	19.7%
Product 2	582	583	0.2%	570	662	13.9%	743	1142	34.9%
Product 3	696	850	21.7%	881	1010	12.8%	898	1152	22.1%
Product 4	689	820	19.0%	851	997	14.7%	883	1152	23.4%
Product 5	689	820	19.0%	830	1009	17.8%	885	1152	23.2%
Average	671	801		779	919		867	1150	
No. Of layers	13	13		3	3		2	2	
Tool weight	8,723	10,413		2,340	2,757		1,734	2,300	
Weighted Average	711	860	18%						

*These data are not true values but represent values normalized to Supplier X.

5.7 Chapter Summary

Chapter 5 provided motivation for the experiments that were performed at the Digital facility and a specific goal for how data were to be collected used. The parameters of the test, along with the modeling assumptions for the calculation of the throughput were shown. The rationale behind testing only lithography run rates, without producing actual product was also explained. Finally, the results of the test were presented, showing approximately 18% of the previously calculated 33% throughput gap can be attributed to higher throughput capability of Supplier X's lithography equipment. This means the

remaining 15% can be thought of as operational improvements that Intel can attempt to achieve, without changing their equipment selection.

6.0 Reasons for Supplier X Operational Advantage and Managerial Implications

6.1 Chapter Overview

Chapter 6 will present three possible reasons for Supplier X's operational advantages. For each of these reasons the supporting data and information on which the conclusion is based is also presented. Much of this information is anecdotal. Finally for each issue, suggestions will be made to help Intel measure the effect of each of these influences.

6.2 The Cost/Quality Tradeoff

6.2.1 Explanation of the point

Intel has operated in a profitable market space that was capacity constrained (as opposed to market constrained) with a complex and capital intensive manufacturing process for the past decade. Because of this, Intel focused their process technology investment and operational objectives on maximizing die yield. The idea was that wafers or die that were defective, cost Intel both in terms of equipment capacity that was taken up by the product, and lost revenue from the potential sale. The capital costs of building fabs, and the lost revenue of each defective die were both huge amounts, and they dwarfed the operating costs of instituting increased levels of testing and preventative maintenance in order to maximize die yield.

In addition to increasing test and maintenance levels on the tools, Intel created the 'Copy Exactly!' program, where plant floor layout, equipment type, process recipes, and work instructions were standardized and strictly adhered to between plants. The complexity of the manufacturing process (over 200 process steps producing features in the sub-micron range) created a high potential for defects due to minor process deviations. This methodology was introduced in order to minimize this variation between production starts and between facilities.

Both the increase in testing and the Copy Exactly! program had the original intent of lowering cost and maximizing profit for Intel. Increases in testing and preventative maintenance, however, take away from the production time allocated to any particular tool and therefore reduce tool throughput. Copy Exactly!, by restricting operations to standardized procedures and recipes, limits the amount of process innovation that can occur from factory floor input. Instead most of the improvements are driven by central process engineering groups. But as Intel continued to improve their yield (reduce their defect rate), the law of diminishing returns began to apply. Figure 6.1 shows the effect of improvement versus time. As the die yield at Intel increases due to focus on the manufacturing process, it becomes more difficult to continue the pace of improvement. This means that Intel is getting diminished returns from its current investment in process improvement activities as compared to the earlier investments. Intel has not, however, deviated from their focus on yield, nor reorganized their operations and personnel to reduce infrastructure costs.

Figure 6.2 shows a theoretical yield-cost curve that shows the tradeoff between the two parameters. The idea behind the curve is that from a very low yield point, the cost savings associated with yield improvements are greater than the cost required to obtain the improvements, and therefore overall cost is lower. But at some point, the cost of process engineering and testing become more expensive than the savings from the improvement, and combined cost begins to rise. The point at which this occurs is the theoretical optimum for each company. This curve is different for each company (and different industries) based on their unique operational cost structure, product margins and improvement programs. There are two key points this figure makes. First, after years of focusing on yield, Intel may have moved to the right of the optimal yield target - meaning their yield is higher than optimal. Second, the operational infrastructure that Intel has built up to support this high test, high yield environment has put them on a curve that is higher than others in cost for comparable yields. With diminishing returns on process improvements at Intel, Supplier X and others have been able to catch up and approach Intel's yields. And since Supplier X and other suppliers have lower internal readiness requirements than Intel, they have been able to achieve their high yields without Intel's

extensive operational infrastructure. Figure 6.2 shows Supplier X to be on a lower Yield/Cost curve than Intel (theoretically).

6.2.2 Supporting Data or Information

The benchmarking study uncovered many data points which suggest that Intel has a higher operating cost structure than Supplier X, and that the main cause of these costs were higher test and preventative maintenance measures which led to lower throughput. Supplier X performs roughly three times fewer test steps than Intel does on comparable process technologies. These test steps require labor and inventory, and reduce throughput by taking up production equipment capacity to perform the tests. Supplier X also had higher equipment utilization than Intel. Many of the Intel engineers who visited the Supplier X facility felt that preventative maintenance was one of the key causes of this utilization gap. Supplier X performed far less preventative maintenance, and was therefore able to have higher throughput on their equipment, and lower depreciation costs per wafer. Finally, an excellent example of excessive testing leading to lower throughput was related by a development engineer in charge of setting Intel's alignment parameters for lithography on the .25 μm process.

6.2.3 The Alignment Mark story

As mentioned earlier in Chapter 4, the number of alignment marks is critical to the raw run rate of lithography equipment. While working on the development of the .25 μm logic process, development engineers at Intel's D1 site in Portland, Oregon were experiencing excessive noise during the alignment step of certain layers in the process. This meant that the alignment was not consistent and the variation was causing defective exposures in lithography steps. They were using X alignment marks at the time. Rather than systematically increasing the number of alignment marks on those steps to the point that the noise was just acceptable, the number of marks was increased to 3X (an almost arbitrarily large number). This reduced the noise problem during alignment, and reduced variation in the process to make it repeatable enough for release to manufacturing.

Tripling the number of alignment marks slowed down the wafer throughput of the machine by 1.5%. Because of the pressure to deliver this process on time though, the 3X marks were never questioned as being higher than necessary. Once instituted into the fabs, they were not reviewed for 24 months. The Copy Exactly! change control process was mentioned as being one impediment to getting the number of alignment marks to be examined. This is one clear example where excessive testing provided no added benefit to improve die yield, and yet reduced tool throughput substantially.

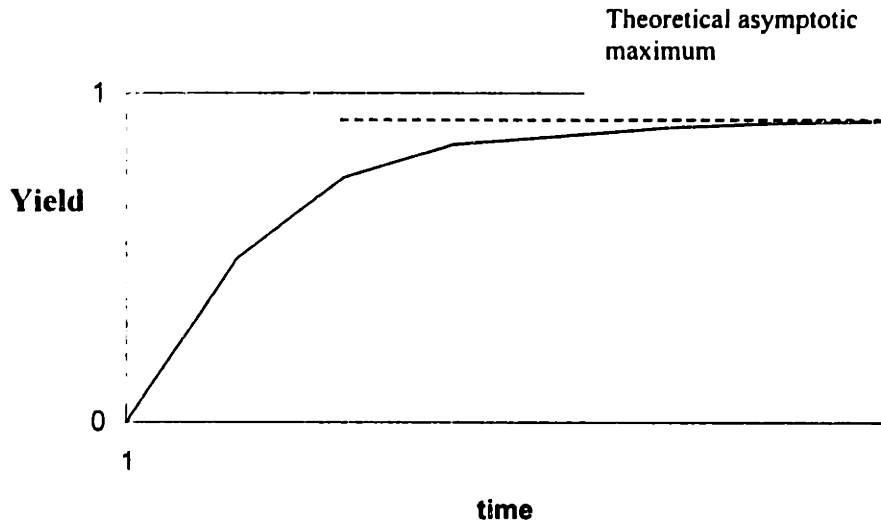


Figure 6.1 Yield Improvement over Time- Diminishing Returns

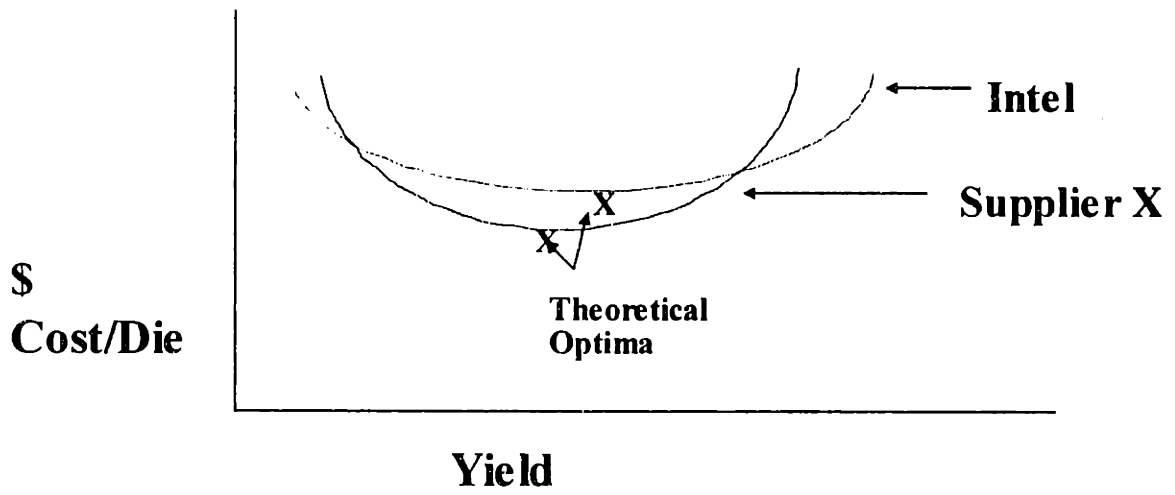


Figure 6.2 Theoretical Yield/Cost Tradeoff

6.3 Intel's Risk Aversion

6.3.1 Explanation of the point

As mentioned in Section 6.1, the combination of having a high margin product line and a complex capital intensive manufacturing process makes operating mistakes extremely expensive. This has created a culture at Intel where managers are averse to taking risks to improve or change their operations. This risk aversion manifests itself in many ways. Within the equipment procurement process, Intel negotiates specifications for items such as mean time between failure, interval between preventative maintenance activities, and throughput rates. Because Intel is very aggressive about holding their capital equipment suppliers to these specifications (often invoking penalties for non-performance), these suppliers have a tendency to understate the speed and robustness of their equipment, in order to ensure they escape penalties. This understatement or 'sandbagging' is exacerbated by fact that Intel engineering and operations managers may buffer these specifications further when building their capacity analyses, in order to ensure they are able to reach their targets reliably. This double understatement of process throughput can be referred to as 'cascading sandbagging'. A primary cause of this phenomenon is that Intel managers are incentivized based on predictability and consistency of throughput, rather than maximization of throughput. Though it may be possible to increase average throughput by pushing equipment specifications, the usual cost is variation in weekly supply. Throughput may increase in one week above target, only to fall below target in another because of unanticipated down time and unplanned maintenance. One Intel manager explained in an interview that the fabs are judged more on their ability to match their stated capacity on a weekly basis, rather than maximizing their capacity at the cost of fluctuation, even if the overall throughput is higher under the second scenario. The risk averse nature of the operating decisions then is an almost expected outcome of the focus on predictability.

6.3.2 Supporting Data and Information

Supporting information for this hypothesis come from both interviews with Intel engineering and operations managers, as well as from first tier equipment suppliers. One supporting example from Intel Fab 15 in Portland Oregon where a cross functional focus team was able to increase facility capacity by 12%, by tightening their estimates of process variability and working to improve throughput at the bottleneck operation. No capital expenditures were required to obtain this capacity increase. It was purely removal of the buffers that had been originally designed into the process that provided the increase in throughput. This is being taken as evidence that the buffers for variability and equipment throughput that Fab 15 had built into their capacity plan were cautious, and were limiting throughput potential.

The issue of sandbagging was also brought up in an interview by the vice president of corporate marketing from one of Intel's equipment suppliers. He explained that Intel was more aggressive than other firms in holding suppliers to specifications. Because of financial penalty clauses for not meeting performance specifications in their contracts with Intel, this company would intentionally publish numbers for time between equipment failures, and time to repair these maintenance failures that were conservative. They managed this process by first creating a distribution of expected times for each of these two metrics, and then using a high confidence interval to determine the published value (rather than using the mean of the distribution, or publishing the entire distribution). This particular supplier also made conservative recommendations for preventative maintenance schedules, i.e. maintenance was recommended to be performed more frequently at Intel than for the same equipment supplied to other customers.

6.4 Intel Centric View

6.4.1 Explanation of the point

Although managers at Intel claim their resistance to change operational practices is driven by the complexity of their manufacturing process, there is also a component that comes from Intel-centric beliefs about best practices. Intel does an excellent job of benchmarking and learning between their virtual factory facilities- Copy Exactly! facilitates this, and upper management pushes this with incentives. As mentioned earlier, however, Intel has very little experience benchmarking outside competitors- either directly or indirectly through organizations like Sematech and Berkeley's CSM. The combination of their strong profitability and their acknowledged industry leadership in process yield has helped cultivate an attitude that 'Intel knows what's best for Intel'. Intel creates and categorizes best practices in their business and operational areas as Best Known Methods (BKM's). A common saying from many younger Intel employees is that these methods are actually BKIM's or Best Known Intel Methods- the intent of the joke to mean that Intel is too self focussed and does not take full advantage of learning from non-Intel examples.

The risk of this managerial self focus leading to a lack of competitiveness at Intel is significant. An excellent and well documented example of a company losing leadership position in a market it invented is Xerox.

6.4.2 The Xerox story and the power of benchmarking

For 30 years after their invention and commercialization of the copier, Xerox dominated the markets for their products. While they allowed Japanese competitors to enter the low end of the copier market, they were confident that by pouring money into Research and Development and focussing on cost cutting through their internal organizations and established procedures, that they would maintain market share leadership and strong profitability. Gradually, the Japanese competitors began to move up from the low end

into intermediate segments in the market. The Japanese were growing capabilities to compete on product features and quality, not just cost. Xerox noticed this move, but failed to take action. Former Xerox CEO David Kearns in his book *Prophets in the Dark* writes,

“Despite what we were beginning to learn, however, we saw no reason to take any significant action... Once the Japanese got into our belly, it was only a matter of time before they began gnawing away at our vital organs...The important point is that we saw the Japanese coming but did not understand their ability to build good reliable products at significantly lower cost. We continually rationalized that we were investing in R & D and that we had plans that would keep us competitive.”²

Kearns describes how Xerox reacted to this by pushing harder on their existing organizations to reduce costs and improve product development. They went through the traditional route of reverse engineering the product to try and determine areas of their competitors cost advantage. This program, while allowing them to work within their existing organization, was unsuccessful in motivating significant change. They next turned to a benchmarking approach, and “haven’t looked back.”³

Xerox adopted a comprehensive benchmarking approach where they identified key business processes in need of review, and then examined best practices in those areas, regardless of industry. This means they did not focus on competitors, but rather, looked for best in class by function, e.g. they studied L.L. Bean to try and improve customer service practices. Xerox reorganized entire job functions in order to successfully adopt best practices, and improve quality. To continue the L.L. Bean example, Xerox restructured their customer service department to better track customer orders through manufacturing. By building an integrated benchmarking program that permeated all aspects of the company, Xerox was able to regain competitiveness (although not all of their lost market share) versus foreign copier companies.

² Prophets in the Dark, Kearns pg. 91

³ A Bible for Benchmarking, Camp

6.5 Implications and methods of measuring the extent of these issues

The data used to state these possible reasons for the throughput gap consist mostly of anecdotal evidence and some data collected through interviews and some simple modeling. Because the data and methods do not have the most rigorous origins, it is useful to consider methods of measuring the eventual effects on the organization that any of these issues may have. Often, organizational problems are ones which everyone agrees exist, but which affect the operation to a surprisingly higher degree than expected.

The possibility that Intel may have non-cost effective infrastructure and process for testing and maintenance can be measured by looking at historical yield improvement rates. The testing that Intel performs does not create high quality on current processes. It is the feedback loop from testing back to process improvements that eventually improve quality on future production runs. By understanding how much quality improvement is being provided by testing procedures, Intel can balance the future improvements in cost due to defect reduction against the infrastructure required to produce those improvements. Intel can also run experiments to reduce testing in specific areas in order to understand the effectiveness of a particular step. Times of low demand through the fab are ideal for performing this testing. Intel should take advantage of underloading situations to perturb their process and understand its stability.

Intel can better understand the risk aversion of their managers by working with their equipment suppliers to understand best practices on similar equipment at other companies. They can also push plants to increase fab capacity until they start to miss production targets every so often. By pushing until targets are missed, Intel can attempt to squeeze down the buffers in equipment throughput. To use a football analogy, if any long pass plays are not beating a defensive team, it probably means they are not playing aggressively enough against the shorter plays.

The Intel centric view is a much subtler problem and its diagnosis will be more difficult. It is important to continue working with suppliers such as Supplier X. By benchmarking through supply negotiations, Intel is assuring a steady stream of information into the top

level managers in the company. The reactions to this information will be a good indication of the level of openness Intel managers have to learning from outside companies. Equipment suppliers can also help supply information. Conducting interviews that are separate from the technical equipment negotiation process can give a good indication of the willingness Intel has to incorporate supplier suggestions into their own operations and specifications.

6.6 Chapter Summary

This chapter discussed three possible explanations for why Intel is behind Supplier X in lithography throughput- expending too much effort on quality controls and testing, Intel managers being incentivized against taking risks to improve the process, and managerial self-focus leading to complacency. For each of these points, an explanation and supporting data and information were given. Finally, an attempt was made to give insight into how Intel could measure to what extent these problems may permeate the organization, and be responsible for the throughput gap that was observed.

References

1. C.Y. Chang and S.M. Sze, ULSI Technology, McGraw Hill, New York, NY (1996).
2. D. Kearns and D. Nadler, Prophets in the Dark, Harper Collins, New York, NY (1992).
3. R. Camp, "A Bible for Benchmarking," *Financial Executive*, Vol. 9, No 4. Pg. 23 July 1993.